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# CICHLID 3

CPU : Intel Yonah 533/667(Merom)  
 Chip Set : Intel Calistoga PM & ICH7-M(B/H)  
 Remarks : Mobility Platform

Model Name : CICHLID 3  
 PBA Name : MAIN  
 PCB Code : BA41-00645A  
 Dev. Step : PRR  
 Revision : 1.4  
 T.R. Date :

DRAW	CHECK	APPROVAL

■ Owner : SESC R&D TEAM\_3 Signature :

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DRAW	SUN, LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU, SHIJIANG	DEV. STEP	PRR	COVER	PART NO.	
APPROVAL	KEVIN, LEE	REV	1.4		BA41- 00645A	
MODULE CODE	CAA059-107	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	1	OF 56

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# SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

## PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E, F, G
LAN	AD21	1	G
MiniPCI SLOT1	AD23	2	D, E
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

## Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for YONAH (1.308~1.068V)
VCCP	YONAH/CALISTOGA Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P2.5V_ALWS	2.5V power rail (Always On)
P3.3V_ALWS	3.3V power rail (Always On)
P5V_ALWS	5V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

## IC / SMB Address

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-410M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

## USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	SYSTEM PORT C
4	BLUETOOTH
5	PORT REPLICATOR
6	MINI PCIEXPRESS FINGER PRINT
7	EXPRESS CARD

## System Power States

- CHP3\_SLP1\* S1, Powered-On/Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3\_SLP3\* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3\_SLP4\* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3\_SLP5\* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

## Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICHT-M	Real Time Clock
Crystal	10MHz	MICOM	HD84F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz	VIDEO	PEG (G73m)

## CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 0	1.4875 V	0 1 0 1 0 0 0	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 0	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 0	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 1 0 0	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 0 1 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 0 1 0 0	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 0 1 0 1	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 1 0	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 0	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active: DPRSLPVR 0, DPRSTP\* 1, PSI2\* 0 or 1  
Deeper Slip: DPRSLPVR 1, DPRSTP\* 0, PSI2\* 0 or 1

\*\*11111111\*: 0V power good asserted.

\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

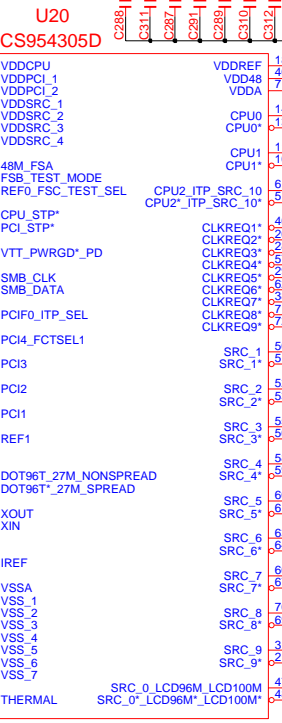
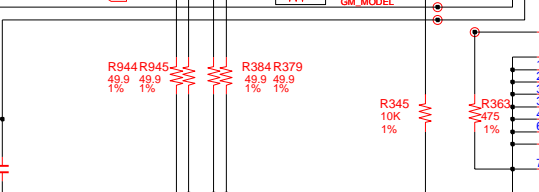
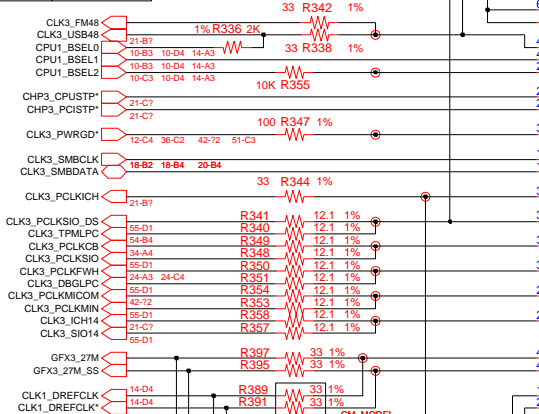
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CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		BOARD INFORMATION	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	7	OF 56

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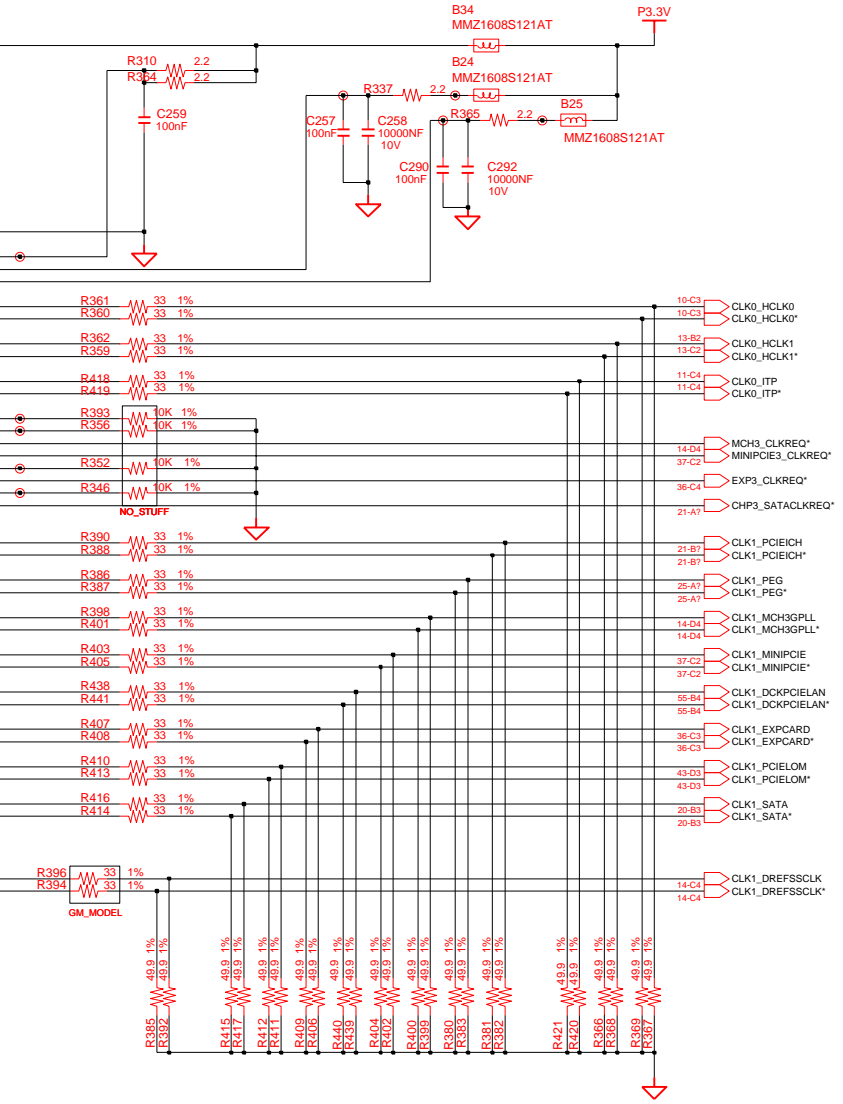
CPU			
FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

1 1 0 166 MHz



SMBUS Address "D2h"

CK-410M+	
w/ CLKREQ	ICS954305
w/ SS Clock	SLG8LP455
	CY28447

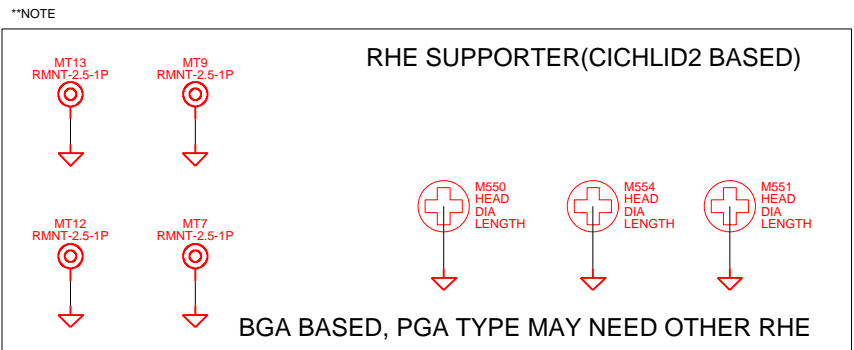
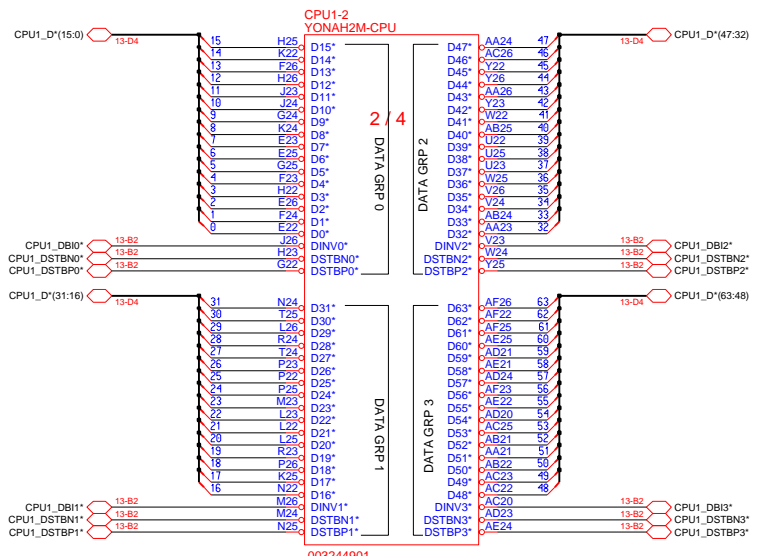
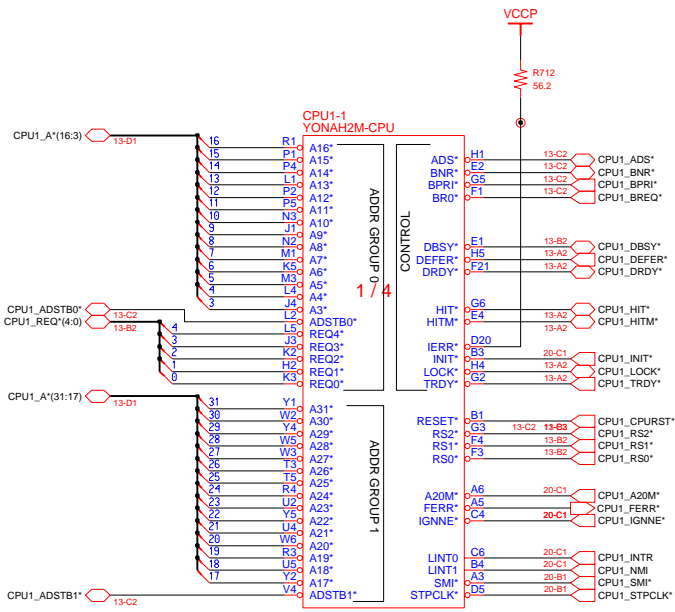


As close as possible on PCB  
Place 14.318MHz within 500mils of CK-410M

Place Termination close to CK-410M+

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN CLOCK GENERATOR	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR	REV		
APPROVAL	KEVIN LEE	REV	1.3	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE 8 OF 56

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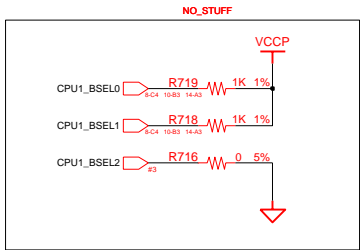


BGA Yonah CPU

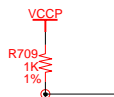
0902-001987	1.5G
0902-001988	1.66G
0902-001989	1.83G
0902-001990	2.0G
0902-001991	2.16G
0902-001992	2.33G

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		YONAH CPU (1/3)	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	9	OF 56

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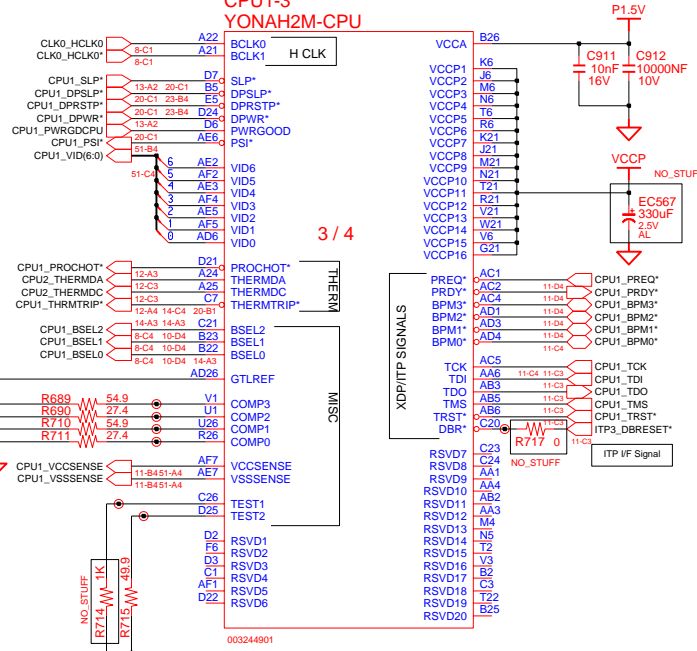
	Pull-up	Pull-down
FSB 533 MHz	BSEL0	BSEL1, BSEL2
FSB 667 MHz	BSEL0, BSEL1	BSEL2



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

STUFF R140(TEST2) FROM Yonah B0 ES



CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 0	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 1	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 1 0 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 1 1 1	0.9125 V	1 0 1 1 0 1 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 0	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 1	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 1 0	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 1	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 1 0 0	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 1	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 1 0	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 1	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 1 0 0 0	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 1	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 1 0	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 1	0.5750 V	1 1 1 0 1 0 0	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 0	0.5625 V	1 1 1 0 1 0 1	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 1	0.5500 V	1 1 1 0 1 1 0	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 1 0	0.5375 V	1 1 1 0 1 1 1	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 1	0.5250 V	1 1 1 1 0 0 0	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 1	0.0000 V
0 1 0 1 0 0 0	1.0000 V	1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 1 0	0.0000 V
0 1 0 1 0 0 1	0.9875 V	1 0 0 1 1 1 1	0.4875 V	1 1 1 1 0 1 1	0.0000 V
0 1 0 1 0 1 0	0.9750 V	1 0 0 1 1 1 1	0.4750 V	1 1 1 1 1 0 0	0.0000 V
0 1 0 1 0 1 1	0.9625 V	1 0 0 1 1 1 1	0.4625 V	1 1 1 1 1 0 1	0.0000 V
0 1 0 1 1 0 0	0.9500 V	1 0 0 1 1 1 1	0.4500 V	1 1 1 1 1 1 0	0.0000 V
0 1 0 1 1 0 1	0.9375 V	1 0 0 1 1 1 1	0.4375 V	1 1 1 1 1 1 1	0.0000 V
0 1 0 1 1 1 0	0.9250 V	1 0 0 1 1 1 1	0.4250 V		
0 1 0 1 1 1 1	0.9125 V	1 0 0 1 1 1 1	0.4125 V		

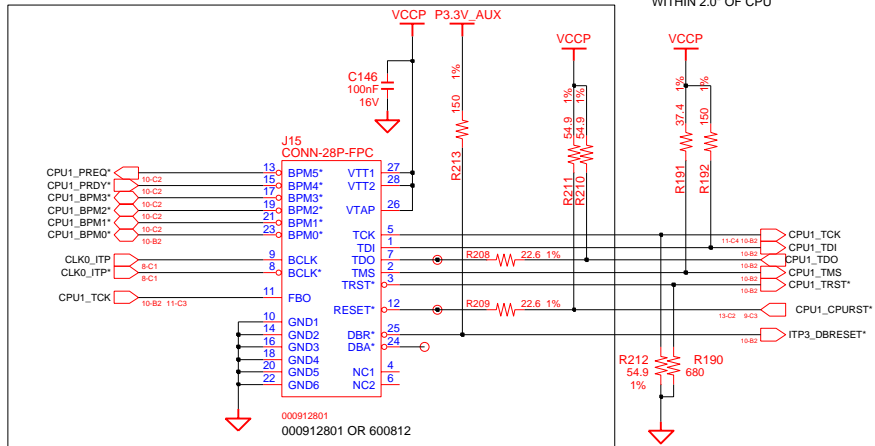
\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR			
APPROVAL	KEVIN LEE	REV	1.3			
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	10 OF 56	

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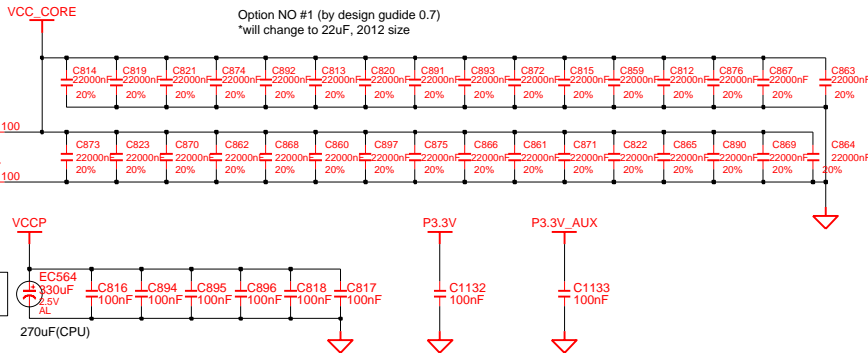
**NO\_STUFF**

WITHIN 2.0" OF CPU

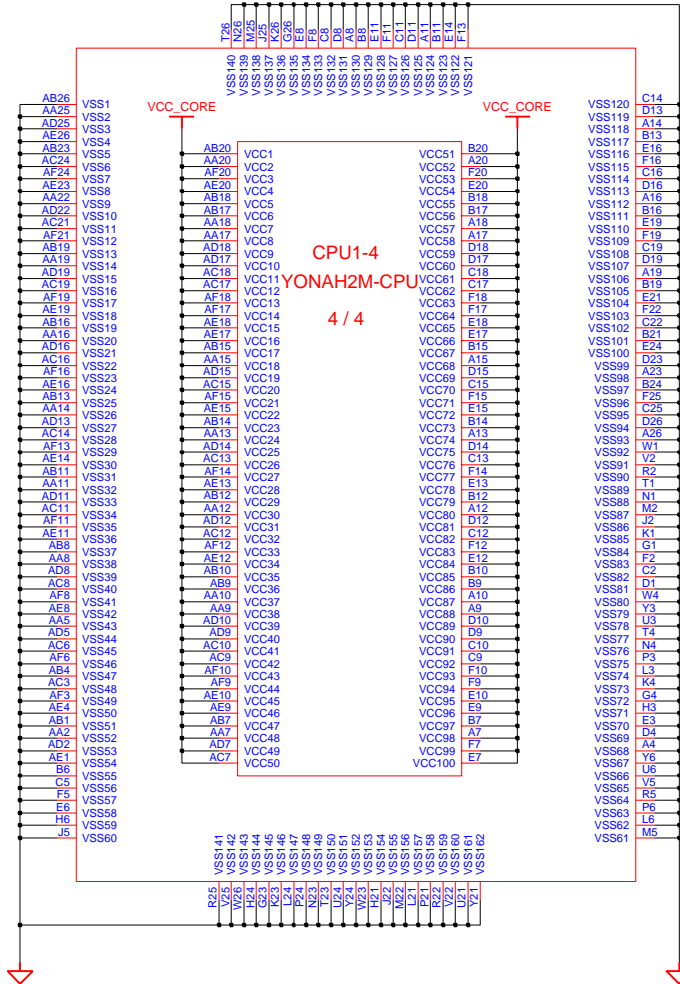
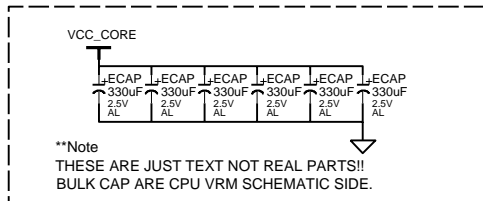


\*\*Note  
WHEN ITP NOT USED NO\_STUFF THIS BLOCK

**ITP/XDP**



CHECK BULK CAP USING  
IF IT DOUBLED



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		YONAH CPU(3/3)	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	11	OF 56

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**CPU / DDR2 Thermal Sensor**

**LAYOUT NOTE:**

ROUTE CPU2\_THERMDC AND CPU2\_THERMDA ON SAME LAYER W/10 MIL TRACE & 10 MIL SPACING ROUTE AWAY FROM NOISE SOURCES WITH GROUND GUARD TRACKS ON EACH SIDE.

**Refer To Thermal Sensor Layout Guidelines.**

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

**PLACE THE MIDDLE OF CPU & GMCH**

$V_{set} = (T_p - 75) / 16$   
 Guardian Temp-tolerance = +/- 3°C  
 1)  $T_p = 88C, \Rightarrow V_{set} = 0.9375$   
 $0.9375 = \frac{x}{3.3 + x} \quad x : y = 1 : 2.52$   
 when  $y = 30 \text{ Kohm}, \Rightarrow x = 11.91 \text{ Kohm}$   
 2)  $x = 12 \text{ Kohm}, y = 30.1 \text{ Kohm}$   
 $V_{set} = 3.3 \times \frac{12.0}{12.0 + 30.1}$   
 $T_p = V_{set} \times 16 + 75 = 90.0496C \pm / - 3$   
 Guardian Temp-tolerance = +/- 3°C

VCP voltage =  $5V \cdot \frac{TH1}{TH1 + 2.21K}$   
 WHEN TH1 IS 10Kohm, VCP is 4.1V  
 If TH1 is 1Kohm, VCP is 1.56V

**PLACE NEAR TO DDR2 SODIMM**

**THERMISTOR - NTC : 10Kohm 1%**

1. ERTJ1VG103FA - Panasonic  
 2. TH11-3H103FT - Mitsubishi  
 - Resistance ratios to R25 at each temperature

Temp(C)	Ratio	Temp(C)	Ratio
-40	20.238	40	0.5826
-30	11.569	50	0.4164
-20	6.984	60	0.3027
-10	4.322	70	0.2233
0	2.755	80	0.1670
10	1.803	90	0.1260
20	1.210	100	0.08570
25	1	110	0.07338
30	0.8309	120	0.05678
35	0.6941	125	0.05011

**FAN Control Logic**

PLACE FAN CONNECTOR NEAR CPU

Line Width = 20 mil

**Changed to Control Methode(EBL)**

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		THERMAL SENSOR/FAN CONTRL	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM			PAGE 12 OF 56

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C927 220nF 16V
C232 470nF 16V
C926 470nF 16V
VCCP

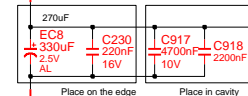
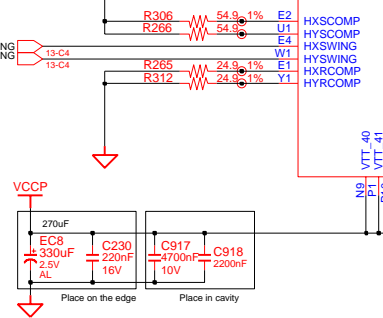
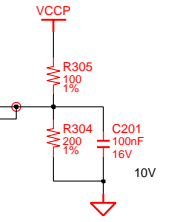
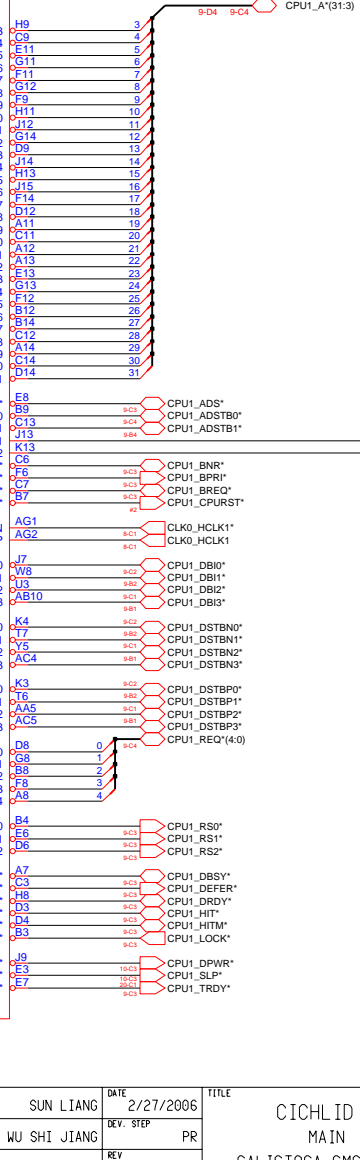
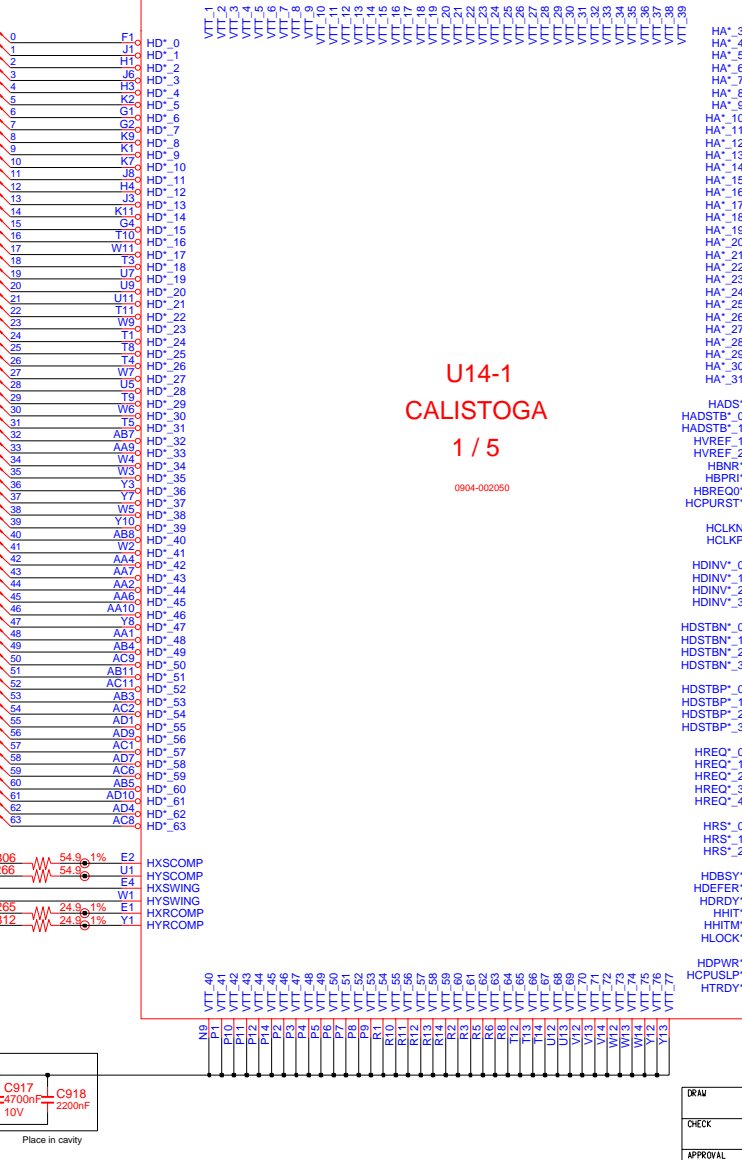
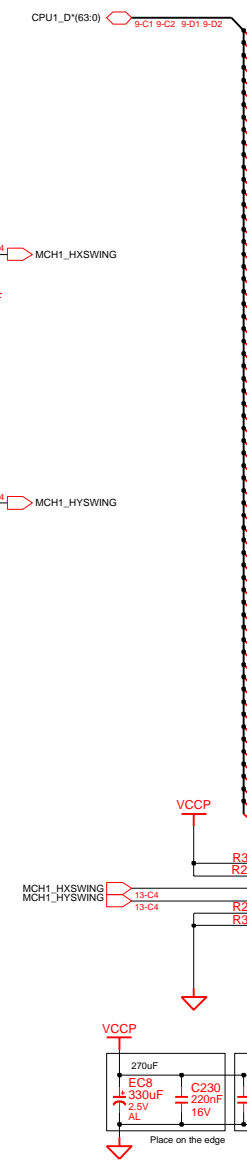
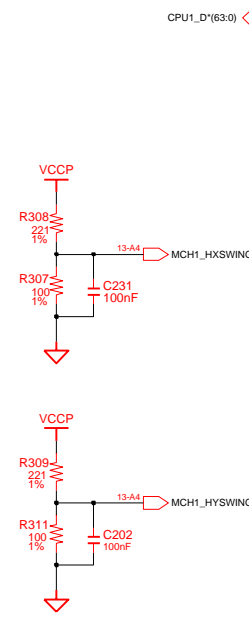


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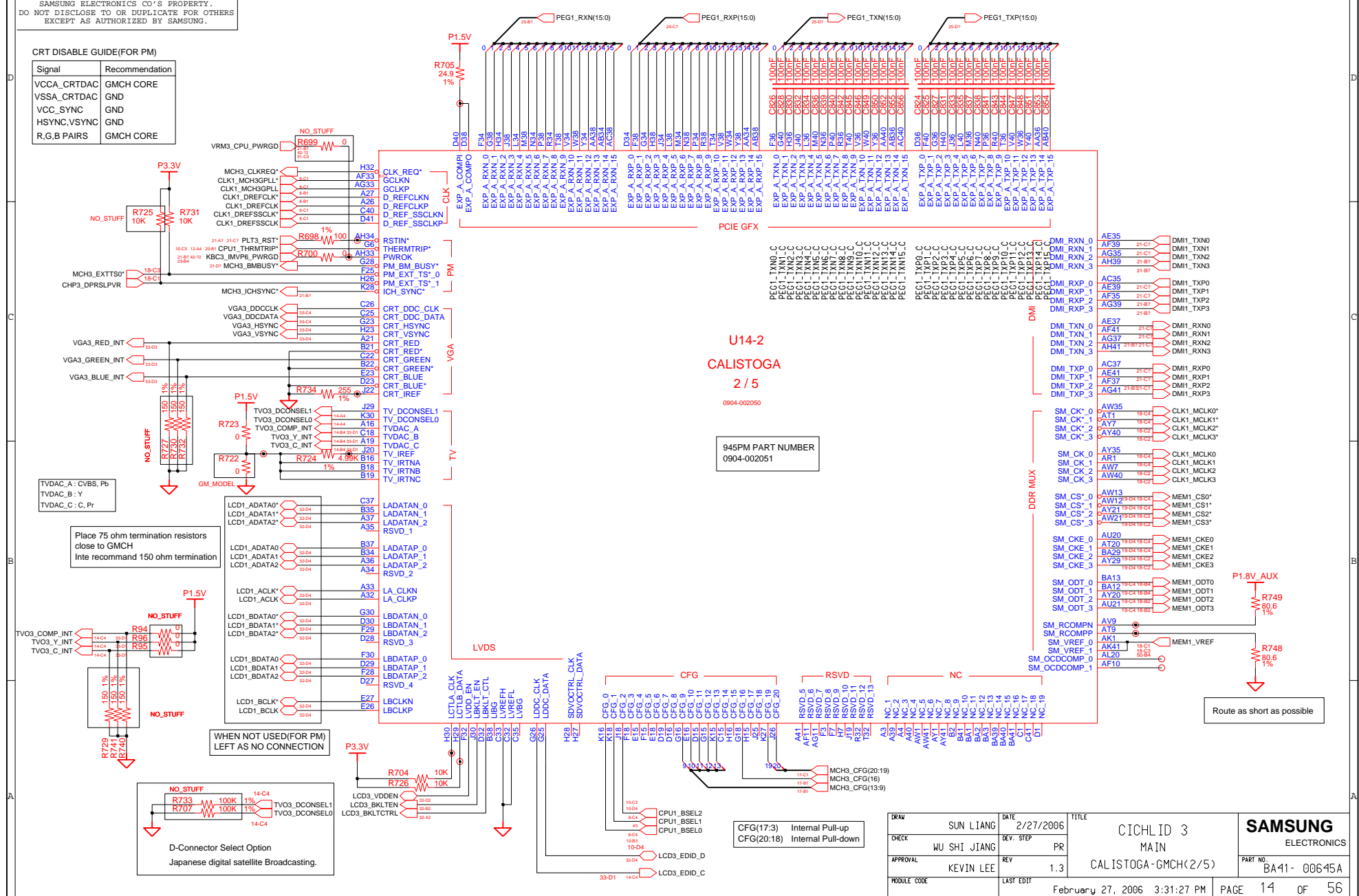


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**CRT DISABLE GUIDE(FOR PM)**

Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC_VSYNC	GND
R,G,B PAIRS	GMCH CORE



Place 75 ohm termination resistors close to GMCH  
Inte recommend 150 ohm termination

WHEN NOT USED(FOR PM)  
LEFT AS NO CONNECTION

D-Connector Select Option  
Japanese digital satellite Broadcasting.

**U14-2**  
**CALISTOGA**  
2 / 5  
0904-002050

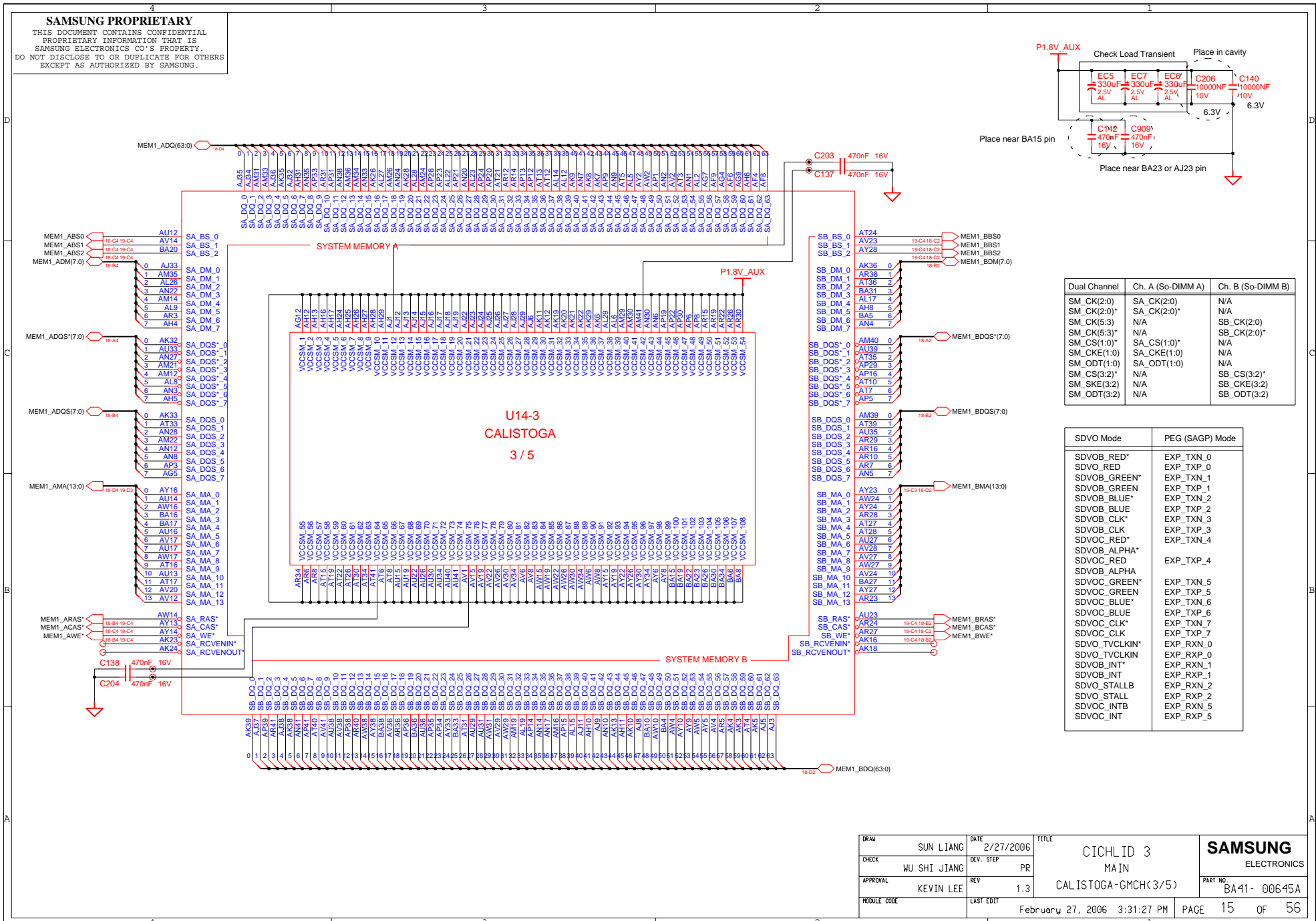
945PM PART NUMBER  
0904-002051

Route as short as possible

CFG(17:3) Internal Pull-up  
CFG(20:18) Internal Pull-down

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	KEVIN LEE	REV	1.3	CALISTOGA-GMCH(2/5)	BA1- 00645A	PAGE 14 OF 56
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM			

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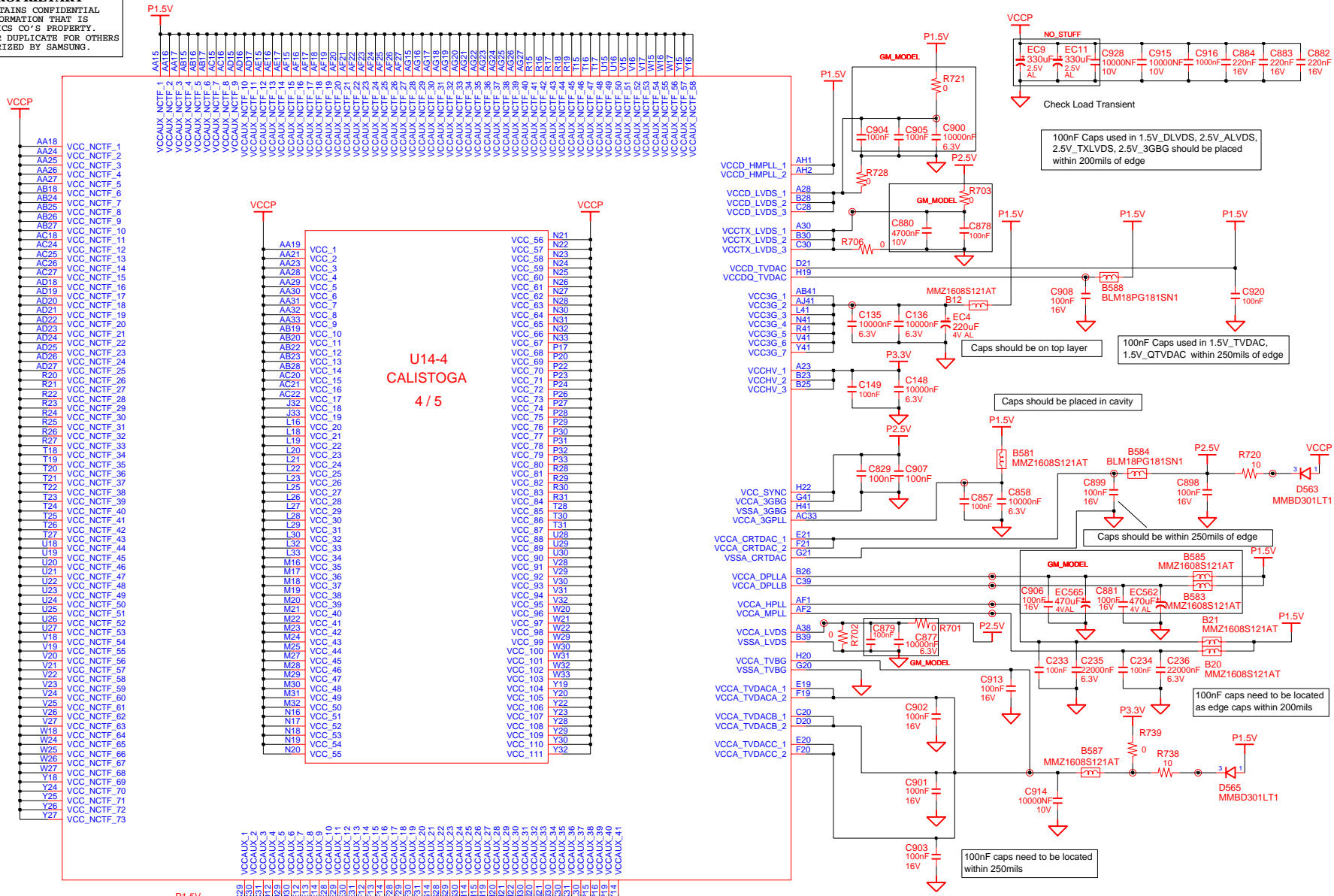


Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)	SA_CS(1:0)	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXP_4
SDVOC_RED	EXP_TXN_5
SDVOB_ALPHA	EXP_TXP_5
SDVOC_GREEN*	EXP_TXN_6
SDVOC_GREEN	EXP_TXP_6
SDVOC_BLUE*	EXP_TXN_7
SDVOC_BLUE	EXP_TXP_7
SDVOC_CLK*	EXP_TXN_8
SDVOC_CLK	EXP_TXP_8
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN CALISTOGA-GMCH(3/5)	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR			
APPROVAL	KEVIN LEE	REV	1.3			PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	15	OF 56

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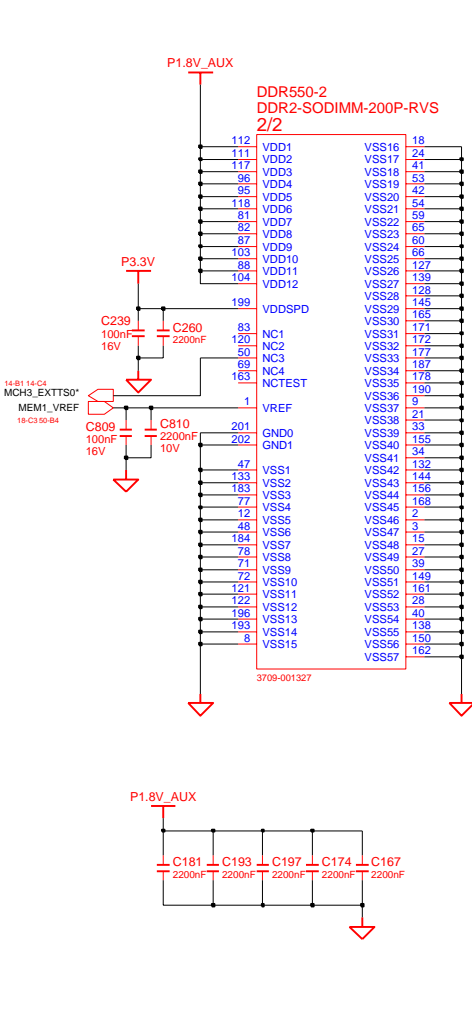
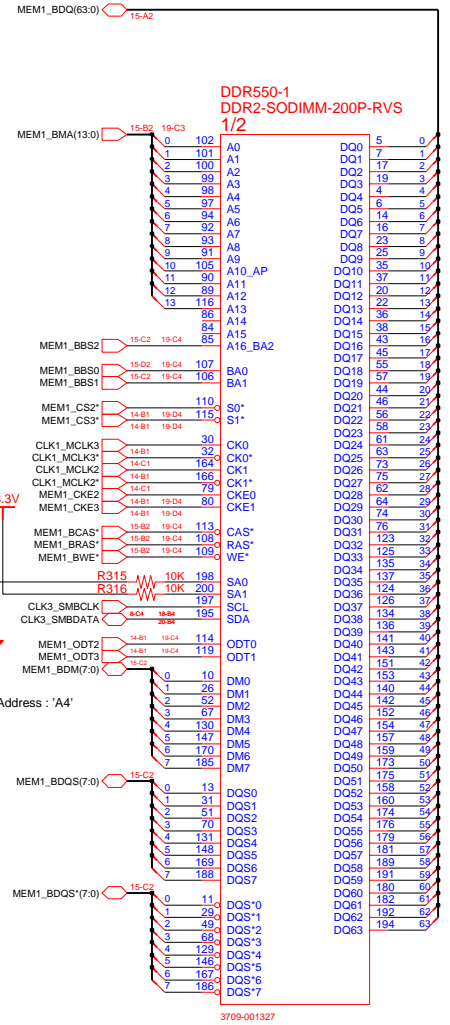
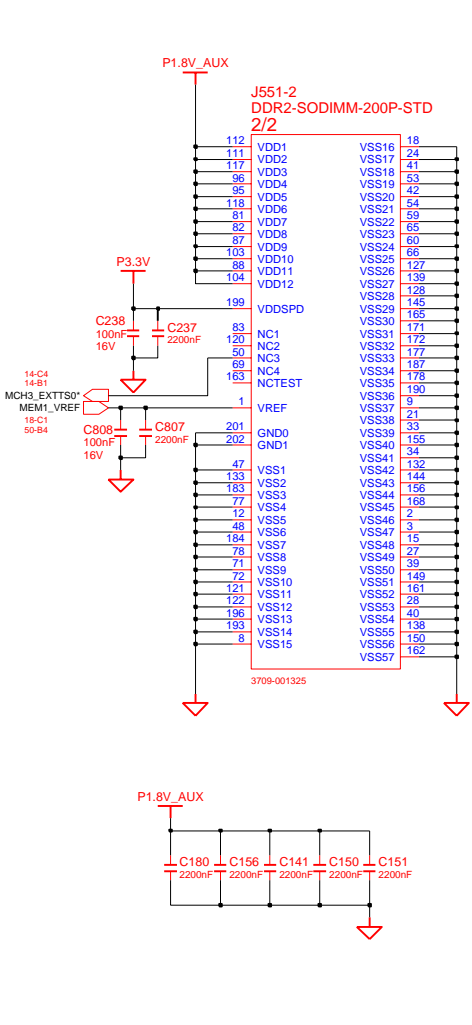
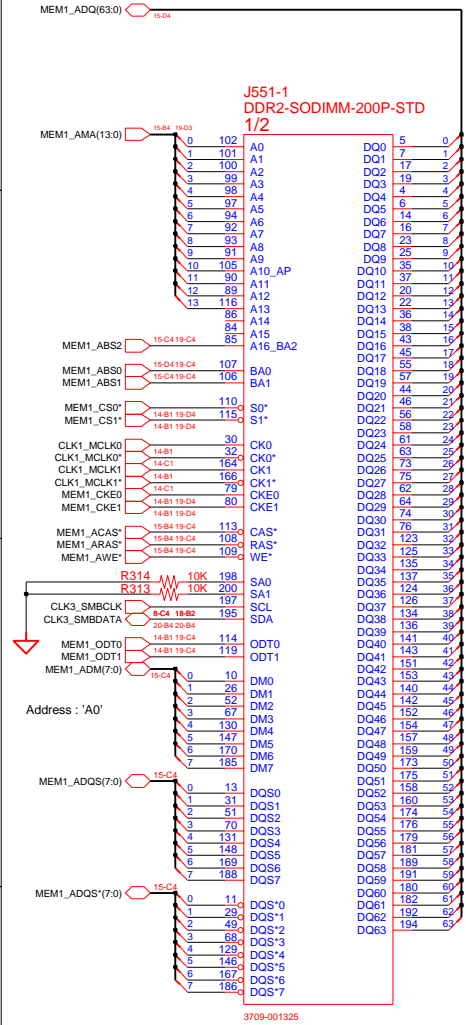
**U14-4  
CALISTOGA  
4 / 5**

AA18	VCC_NCTF_1	VCC_56	N21
AA24	VCC_NCTF_2	VCC_57	N22
AA25	VCC_NCTF_3	VCC_58	N23
AA26	VCC_NCTF_4	VCC_59	N24
AA27	VCC_NCTF_5	VCC_60	N25
AB18	VCC_NCTF_6	VCC_61	N26
AB24	VCC_NCTF_7	VCC_62	N27
AB25	VCC_NCTF_8	VCC_63	N28
AB26	VCC_NCTF_9	VCC_64	N29
AB27	VCC_NCTF_10	VCC_65	N30
AC18	VCC_NCTF_11	VCC_66	N31
AC24	VCC_NCTF_12	VCC_67	N32
AC25	VCC_NCTF_13	VCC_68	N33
AC26	VCC_NCTF_14	VCC_69	N34
AC27	VCC_NCTF_15	VCC_70	N35
AD18	VCC_NCTF_16	VCC_71	N36
AD19	VCC_NCTF_17	VCC_72	N37
AD20	VCC_NCTF_18	VCC_73	N38
AD21	VCC_NCTF_19	VCC_74	N39
AD22	VCC_NCTF_20	VCC_75	N40
AD23	VCC_NCTF_21	VCC_76	N41
AD24	VCC_NCTF_22	VCC_77	N42
AD25	VCC_NCTF_23	VCC_78	N43
AD26	VCC_NCTF_24	VCC_79	N44
AD27	VCC_NCTF_25	VCC_80	N45
R20	VCC_NCTF_26	VCC_81	N46
R21	VCC_NCTF_27	VCC_82	N47
R22	VCC_NCTF_28	VCC_83	N48
R23	VCC_NCTF_29	VCC_84	N49
R24	VCC_NCTF_30	VCC_85	N50
R25	VCC_NCTF_31	VCC_86	N51
R26	VCC_NCTF_32	VCC_87	N52
R27	VCC_NCTF_33	VCC_88	N53
T18	VCC_NCTF_34	VCC_89	N54
T19	VCC_NCTF_35	VCC_90	N55
T20	VCC_NCTF_36	VCC_91	N56
T21	VCC_NCTF_37	VCC_92	N57
T22	VCC_NCTF_38	VCC_93	N58
T23	VCC_NCTF_39	VCC_94	N59
T24	VCC_NCTF_40	VCC_95	N60
T25	VCC_NCTF_41	VCC_96	N61
T26	VCC_NCTF_42	VCC_97	N62
T27	VCC_NCTF_43	VCC_98	N63
U18	VCC_NCTF_44	VCC_99	N64
U19	VCC_NCTF_45	VCC_100	N65
U20	VCC_NCTF_46	VCC_101	N66
U21	VCC_NCTF_47	VCC_102	N67
U22	VCC_NCTF_48	VCC_103	N68
U23	VCC_NCTF_49	VCC_104	N69
U24	VCC_NCTF_50	VCC_105	N70
U25	VCC_NCTF_51	VCC_106	N71
U26	VCC_NCTF_52	VCC_107	N72
U27	VCC_NCTF_53	VCC_108	N73
V18	VCC_NCTF_54	VCC_109	N74
V19	VCC_NCTF_55	VCC_110	N75
V21	VCC_NCTF_56	VCC_111	N76
V22	VCC_NCTF_57		
V23	VCC_NCTF_58		
V24	VCC_NCTF_59		
V25	VCC_NCTF_60		
V26	VCC_NCTF_61		
V27	VCC_NCTF_62		
W18	VCC_NCTF_63		
W24	VCC_NCTF_64		
W25	VCC_NCTF_65		
W26	VCC_NCTF_66		
Y18	VCC_NCTF_67		
Y24	VCC_NCTF_68		
Y25	VCC_NCTF_69		
Y26	VCC_NCTF_70		
Y27	VCC_NCTF_71		
	VCC_NCTF_72		
	VCC_NCTF_73		

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		CALISTOGA-GMCH(4/5)	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	16	OF 56

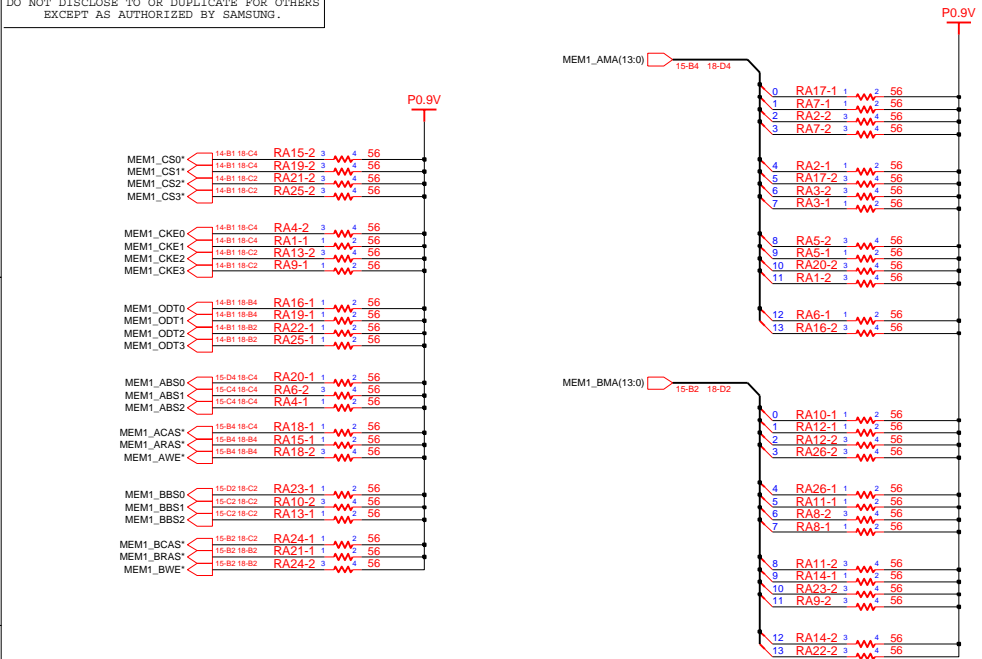


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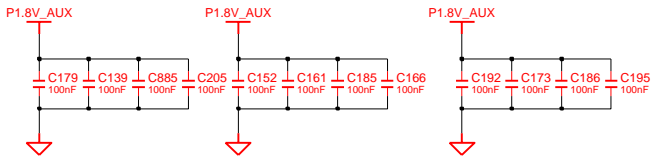
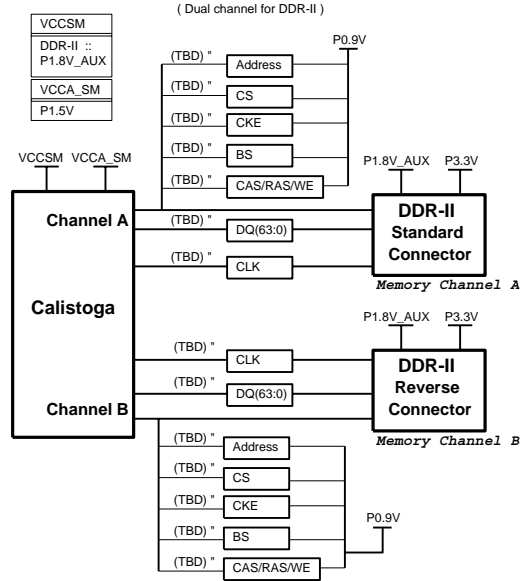


DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN		
APPROVAL	KEVIN LEE	REV	1.3	DDR2 - SODIMM		PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	18	OF 56

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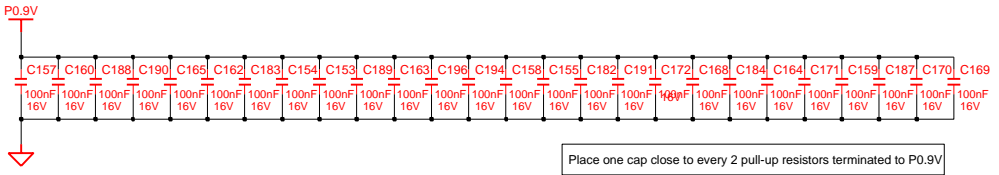
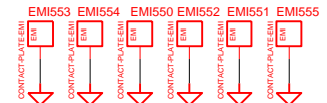


**Memory Topology**



Place near GMCH      Place near SO-DIMM0      Place near SO-DIMM1

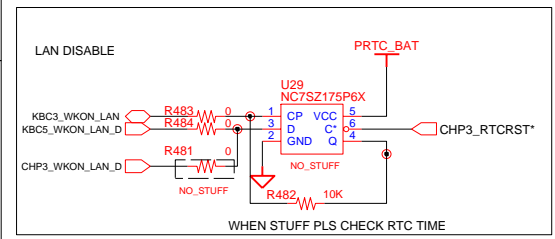
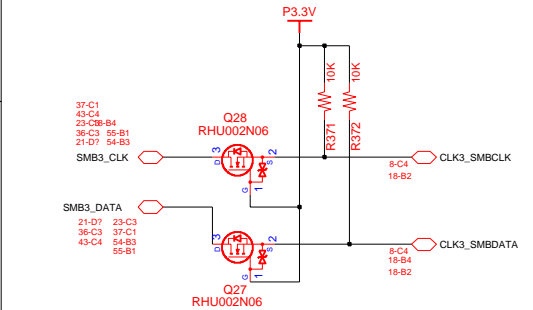
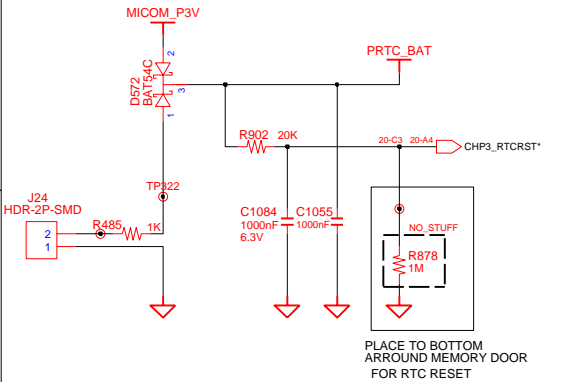
LOCATE EMI FINGER AT THE CORNER OF SODIMM CONNECTOR



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLD 3 MAIN DDR2 - TERMINATION	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR			
APPROVAL	KEVIN LEE	REV	1.3			
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE 19 OF 56		

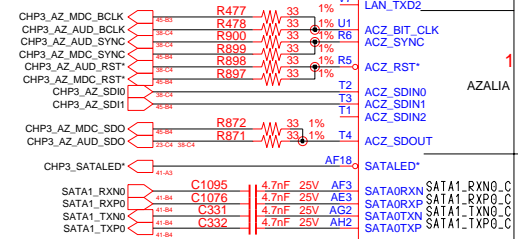
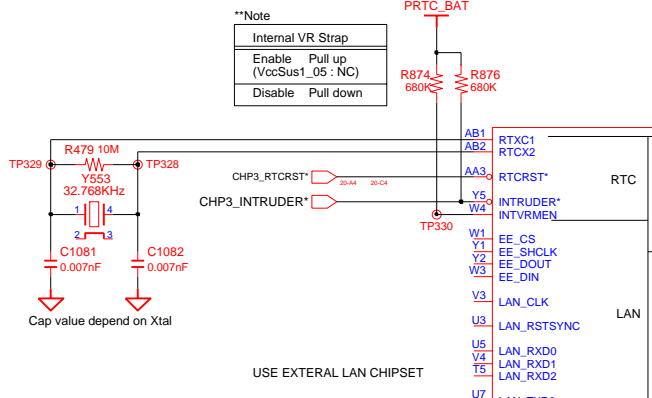
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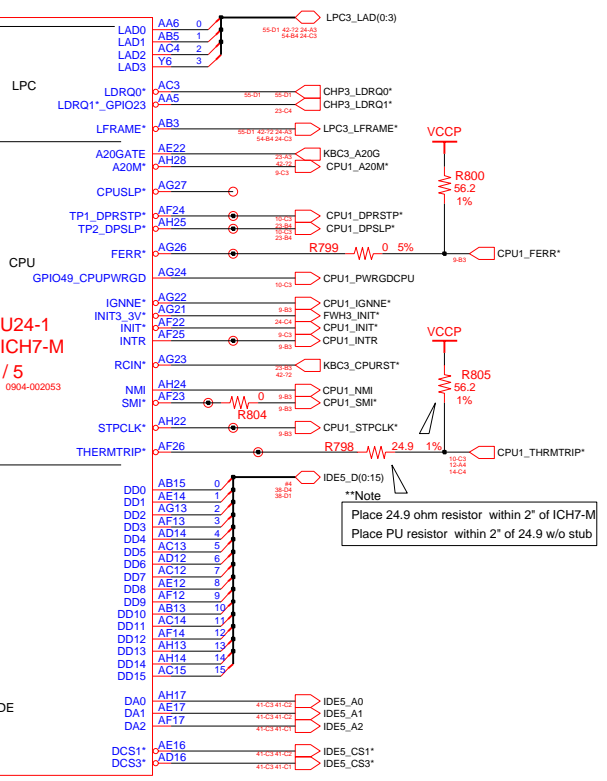
**\*\*Note**

Internal VR Strap	
Enable	Pull up (VccSus1_05 : NC)
Disable	Pull down



distance between the ICH7-M and cap on the "P" signal should be identical distance between the ICH7-M and cap on the "N" signal for same pair.

place 24.9 resistance within 500 mils of ICH7 ball

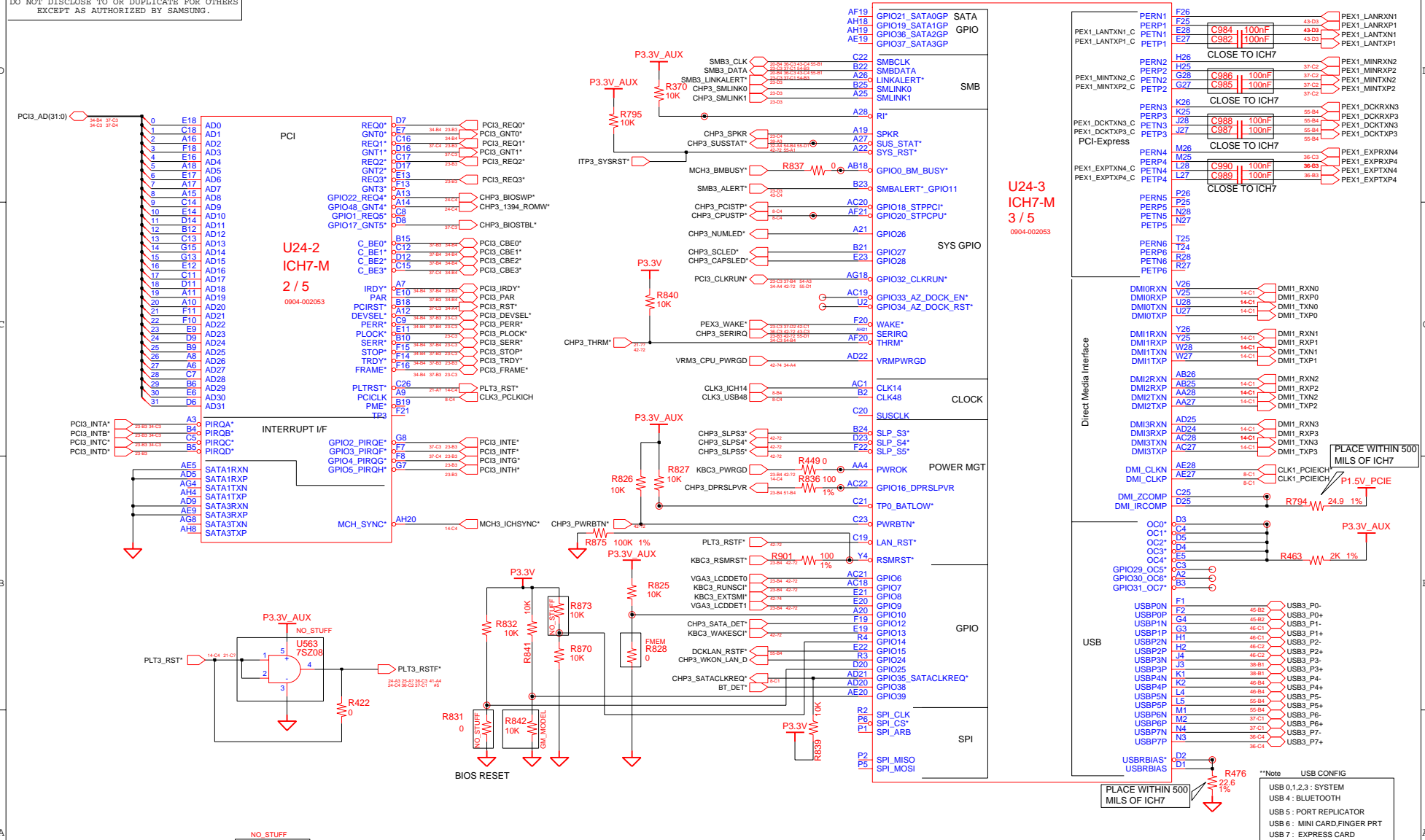


DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		ICH7 - M(1/4)	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	20	OF 56

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AC caps : PCIe need to be within 250mils of the driver  
Resistor for Test : Place Stuffing Option to minimize stubs

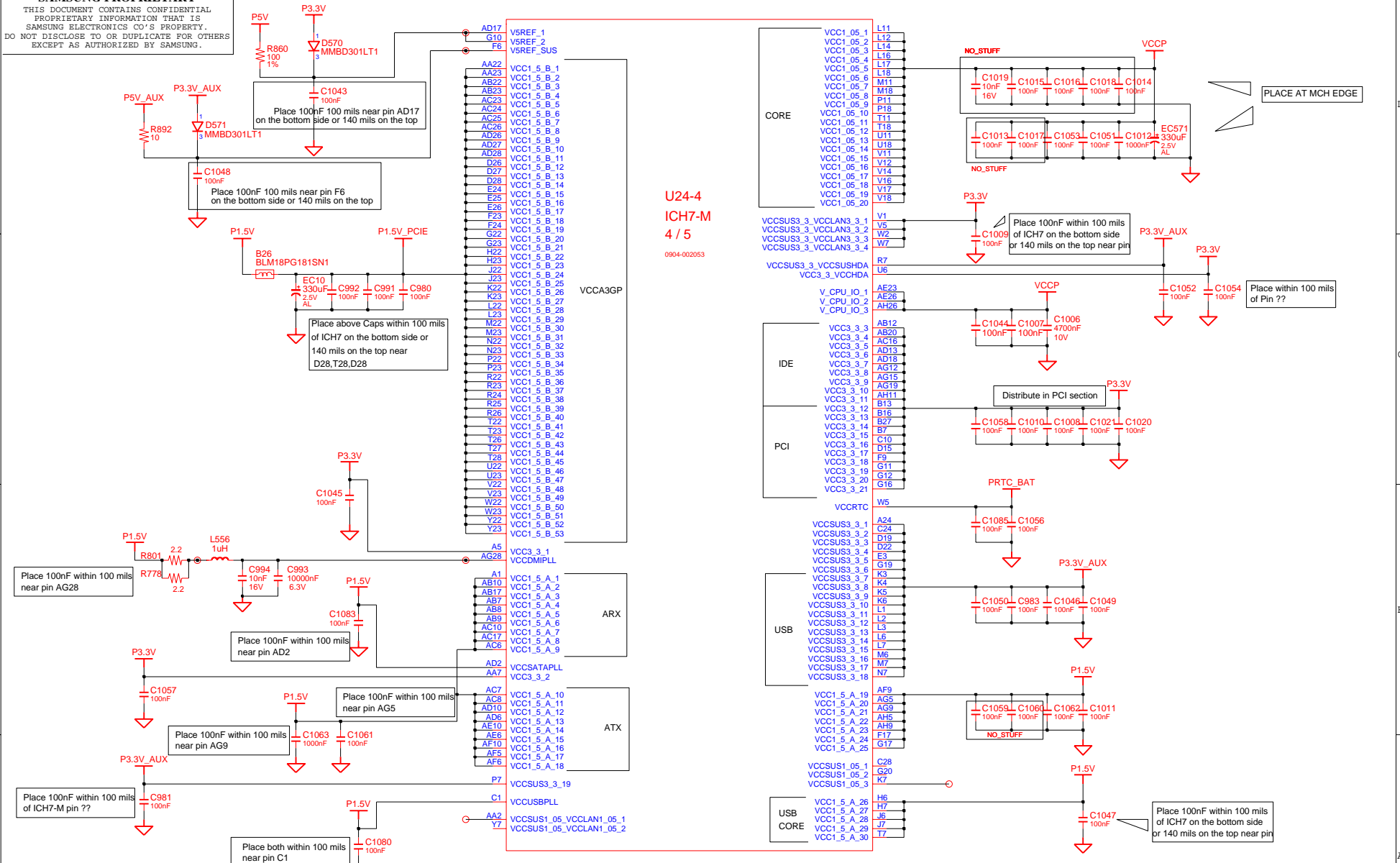


DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41- 00645A
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		ICH7 - M(2/4)	
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	21 OF 56	

\*\*Note USB CONFIG  
USB 0,1,2,3 : SYSTEM  
USB 4 : BLUETOOTH  
USB 5 : PORT REPLICATOR  
USB 6 : MINI CARD/FINGER PRT  
USB 7 : EXPRESS CARD



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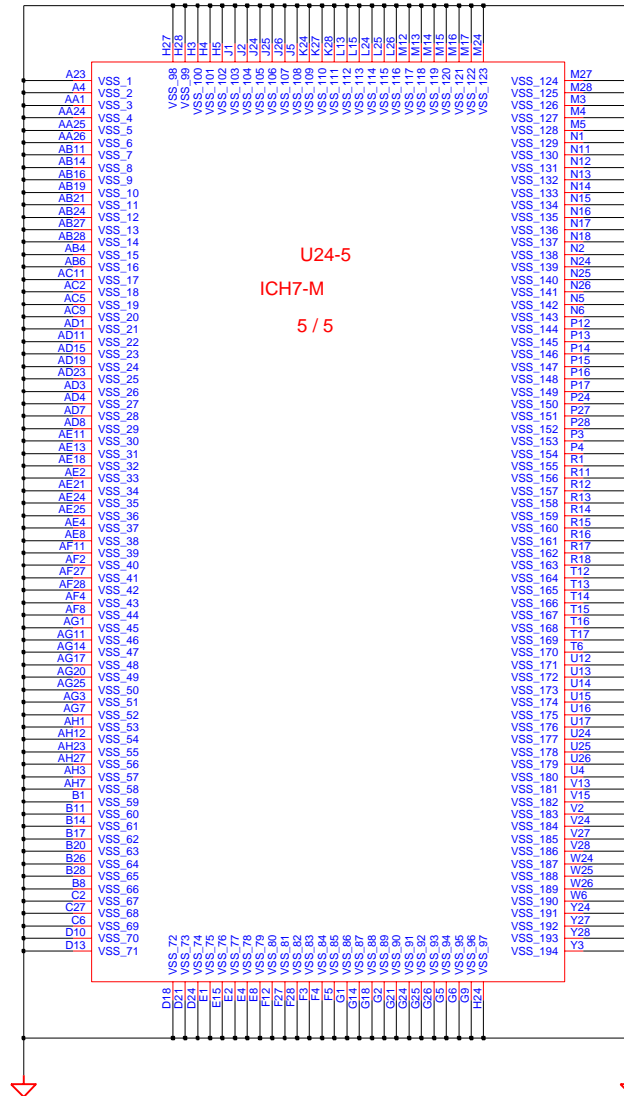
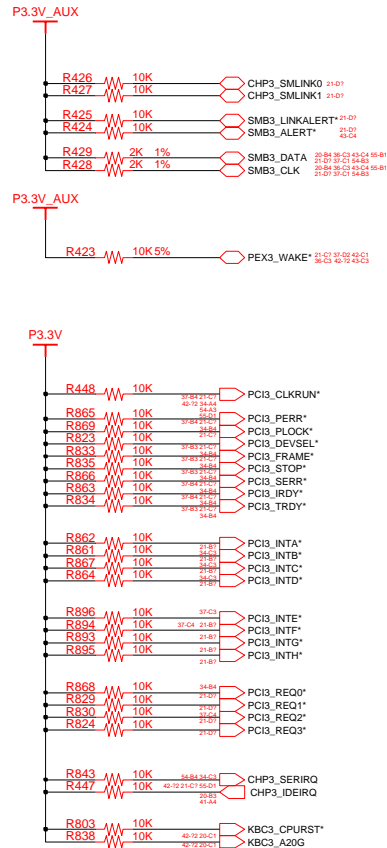
U24-4  
 ICH7-M  
 4 / 5  
 0904-002053

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		ICH7 - M(3/4)	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	22	OF 56

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**ICH7-m Options**

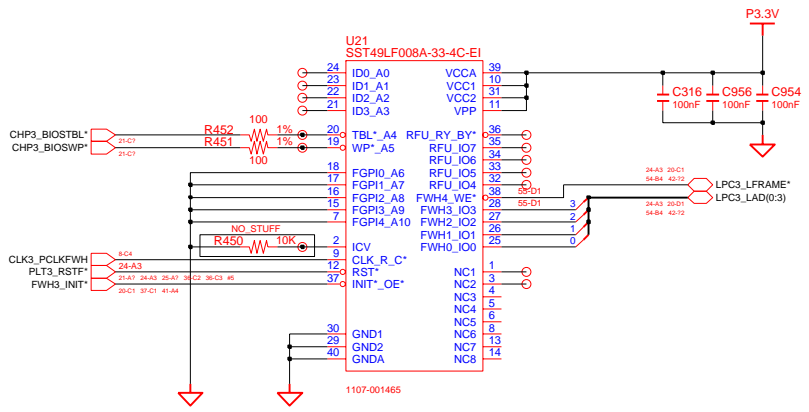
	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_GNT3	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
CHP3_GNT(5:4)	Boot BIOS Option	



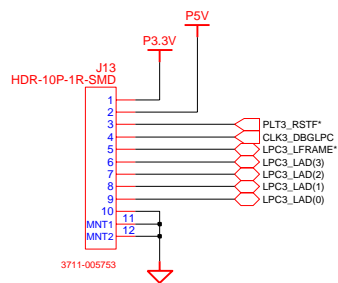
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CHECK	WU SHI JIANG	DEV. STEP	PR	REV		
APPROVAL	KEVIN LEE	REV	1.3	ICH7 - M(4/4)		PAGE 23 OF 56
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM			

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80 PORT CONNECTOR

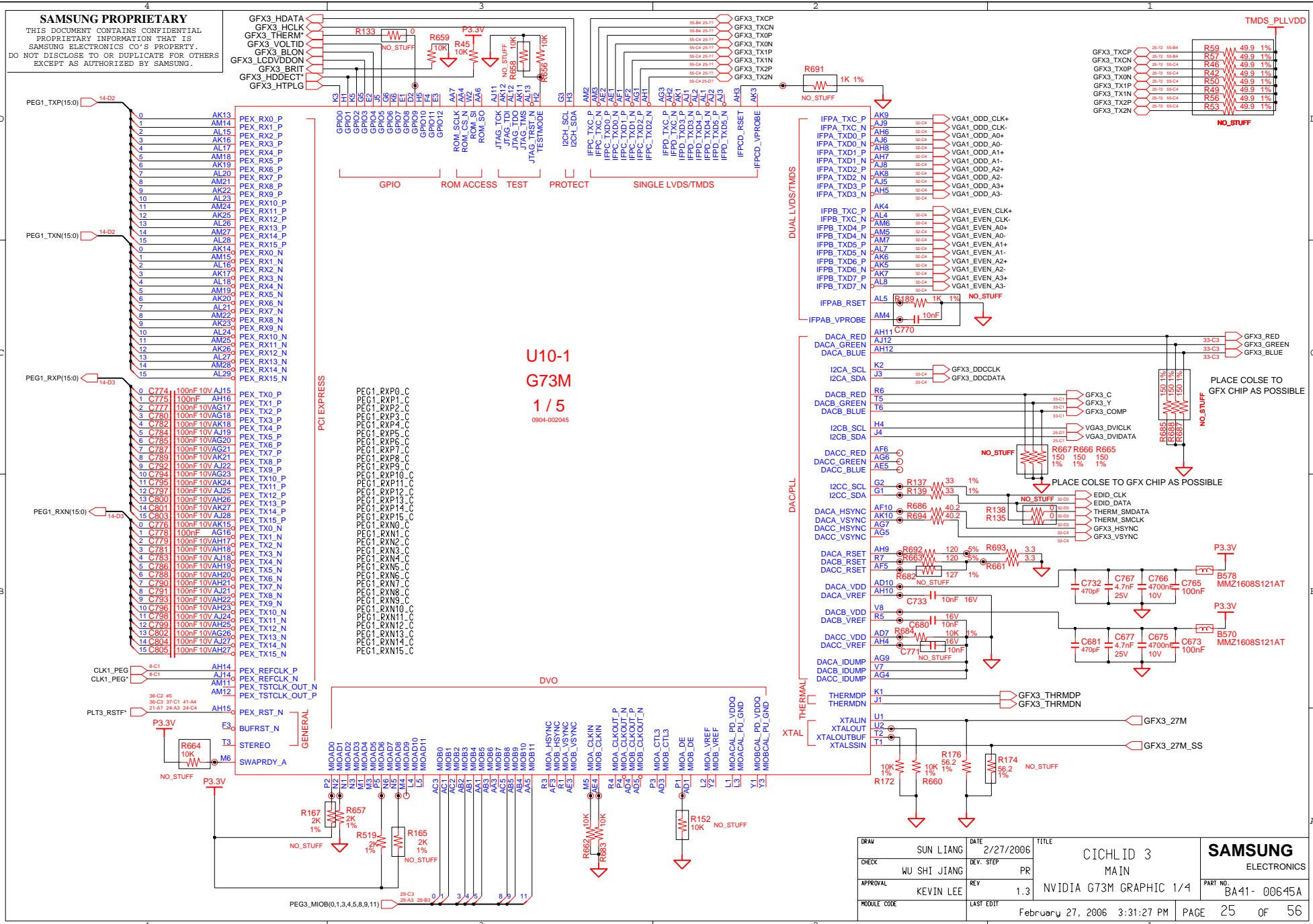


```

02 VERIFY REAL MODE
03 DISABLE NMI
04 GET CPU TYPE
06 INIT. SYSTEM H/W
08 INIT. CHIPSET REG.
09 SET IN POST FLAG
0A INIT CPU.REG
0B CPU CACHE ON
0C INIT.CACHE TO POST
0E INIT. I/O VALUE
0F ENABLE THE L-BUS IDE
10 INIT. POWER MANAGER
11 LOAD ALTERNATE REG.
13 PCI BUS MASTER RESET
    WITH INITIAL POST VALUE
14 INIT. KEYBOARD CONTROLLER
16 CHECK CHECKSUM
18 8254 TIMER INIT.
1A 8237 DMA CONTROLLER INIT.
1C RESET INTERRUPT CONTROLLER
20 TEST DRAM REFRESH
22 TEST 8742 KEYBOARD CONTROLLER
24 SET ES SEGMENT REG. TO 4GB
26 ENABLE A20
28 AUTO SIZING DRAM
32 COMPUTE THE CPU SPEED
34 TESET CMOS RAM
38 SHADOW SYSTEM BIOS ROM
3A AUTO SIZING CACHE
3C CONFIGURE ADVANCED CHIPSET REG.
3D LOAD ALTER REG. WITH CMOS VALUE
42 INIT. INTERRUPT VECTOR
44 INIT. BIOS INTERRUPT
46 CHECK ROM COPYRIGHT NOTICE
47 INIT. I20 SUPPORT IF INSTALLED
48 CHECK VIDEO CONFIGURE AGAINST CMOS
49 INIT. PCI BUS AND DEVICE
4A INIT. ALL VIDEO BIOS ROM
4C SHADOW VIDEO BIOS ROM
50 DISPLAY CPU TYPE AND SPEED
52 TEST KEYBOARD
54 SET KEYCLICK IF ENABLED
56 ENABLE KEYBOARD
58 TEST FOR UNEXPECTED INTERRUPTS
5A DISPLAY " PRESS ..... SETUP"
5C TEST RAM BETWEEN 512K AND 640K
60 TEST EXTENDED MEMORY
62 TEST EXTENDED MEMORY ADDRESS LINE
64 JUMP TO USER PATCH 1

66 CONFIGURE ADVANCE CACHE REG.
6A DISPLAY EXTERNAL CACHE SIZE
6C DISPLAY SHADOW MESSAGE
6E DISPLAY NON-DISPOSABLE SEGMENT
70 DISPLAY ERROR MESSAGE
72 CHECK FOR CONFIGURATION ERROR
74 TEST REAL-TIME CLOCK
76 CHECK FOR KEYBOARD ERROR
7C SETUP HARDWARE INTERRUPT VECTOR
7E TEST COPROCESSER IF PRESENT
80 DISABLE ON-BOARD I/O PORT
82 DETECT AND INSTALL EXT.RS232C
84 DETECT AND INSTALL EXT.PARALLEL
86 RE-INIT. ON-BOARD I/O PORT
88 INIT. BIOS DATA ROM
8A INIT.EXTENDED BIOS DATA AREA
8C INIT. FDD CONTROLLER
9A SHADOW OPTION ROMS
9C SETUP POWER MANAGEMENT
9E ENABLE H/W INTERRUPT
A0 SET TIME OF DAY
A4 INIT. TYPOMATIC RATE
A8 ERASE F2 PROMPT
AA SCAN FOR F2 KEY STROKE
AC ENTER SETUP
AE CLEAR IN POST FLAG
B0 CHECK FOR ERRORS
B2 POST DONE-PREPARE TO BOOT O/S
B4 ONE BEEP
B6 CHECK PASSWORD (OPTION)
B7 ACPI INIT
BA DMI INIT
BE CLEAR SCREEN
C0 TRY BOOT WITH INT19
D0 INTERRUPT HANDLER ERROR
D2 UNKNOWN INTERRUPT ERROR
D4 PENDING INTERRUPT ERROR
D6 SHUTDOWN 5
D8 SHUTDOWN ERROR
DA EXTENDED BLOCK MOVE
DC SHUTDOWN 10
E8 ENABLE NMI
90 INIT. HDD CONTROLLER
91 INIT. LOCAL BUS HDD CONTROLLER
92 JUMP TO USER PATCH 2
94 DISABLE A20 ADDRESS LINE
96 CLEAR HUGE ES.SEGMENT REG.
98 SEARCH FOR OPTION ROMS
    
```

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		FIRMWARE HUB	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	24	OF 56



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GFX3_TXCP	29-32	58-64	R59	49.9	1%
GFX3_TXCN	29-32	58-64	R57	49.9	1%
GFX3_TXOP	29-32	58-64	R45	49.9	1%
GFX3_TX0P	29-32	58-64	R42	49.9	1%
GFX3_TX1P	29-32	58-64	R50	49.9	1%
GFX3_TX1N	29-32	58-64	R49	49.9	1%
GFX3_TX2P	29-32	58-64	R56	49.9	1%
GFX3_TX2N	29-32	58-64	R53	49.9	1%

**U10-1  
G73M  
1/5**  
0904-002045

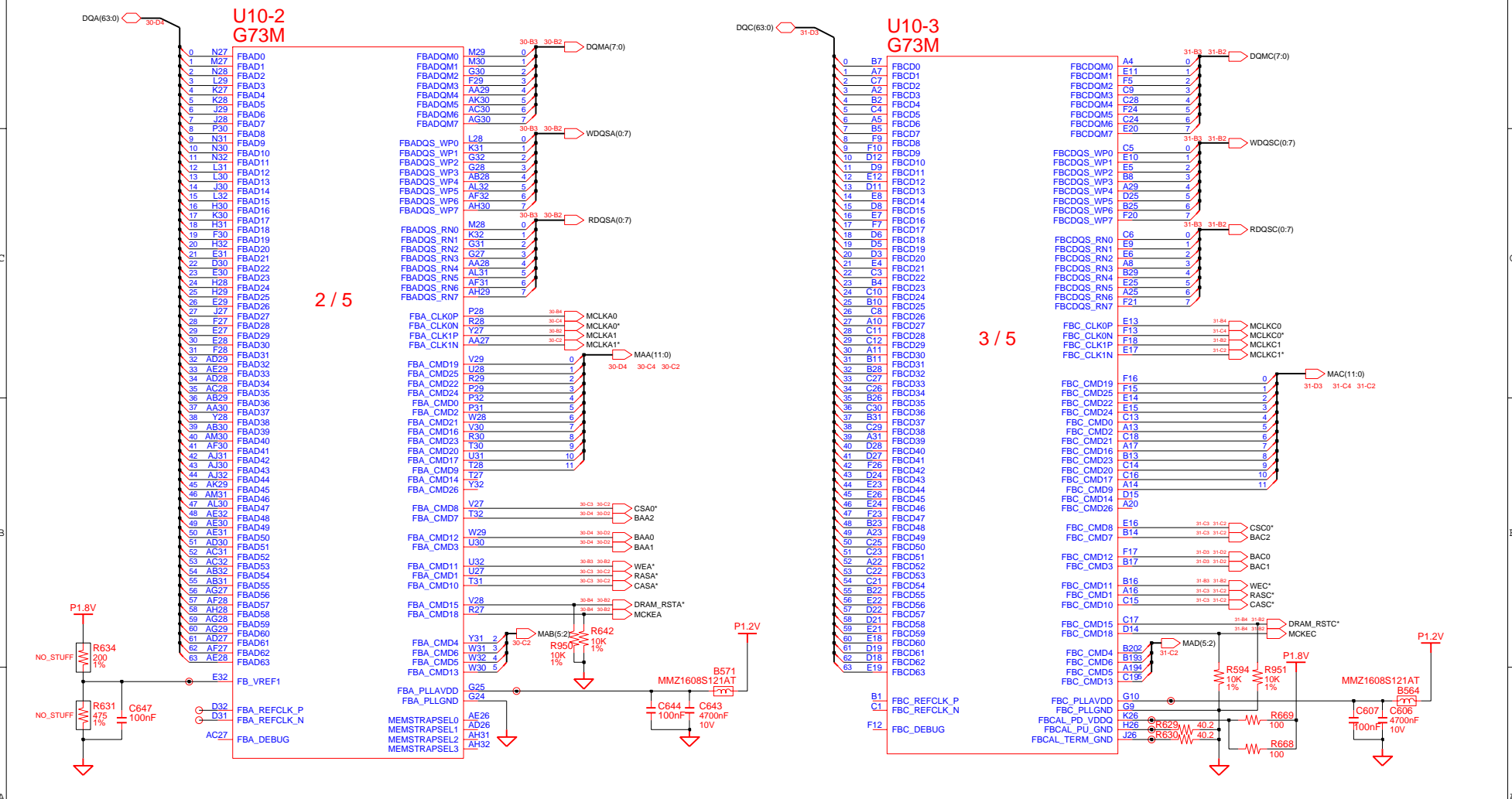
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CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN		
APPROVAL	KEVIN LEE	REV	1.3	NVIDIA G73M GRAPHIC 1/4	PART NO.	BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	25	OF 56

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**Graphic Memory I/F  
(Using FBA Channel)**

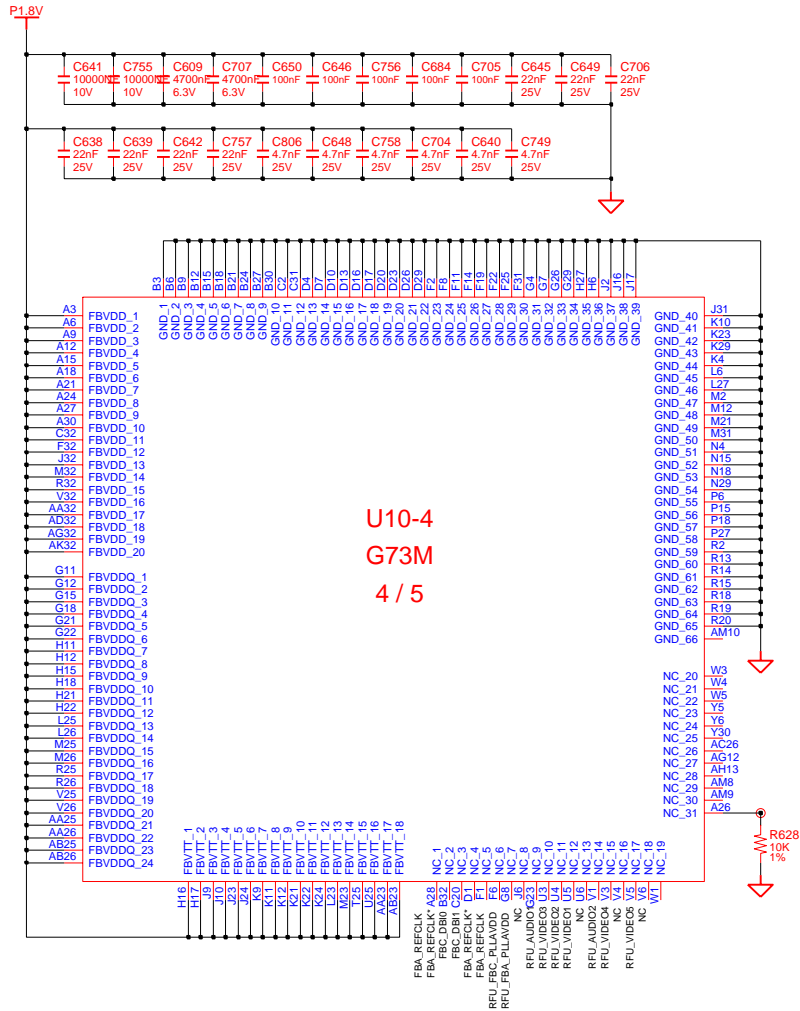
**Graphic Memory I/F  
(Using FBC Channel)**



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CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN		
APPROVAL	KEVIN LEE	REV	1.3	NVIDIA G73M GRAPHIC 2/4	PART NO.	BA41- 00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	26	OF 56

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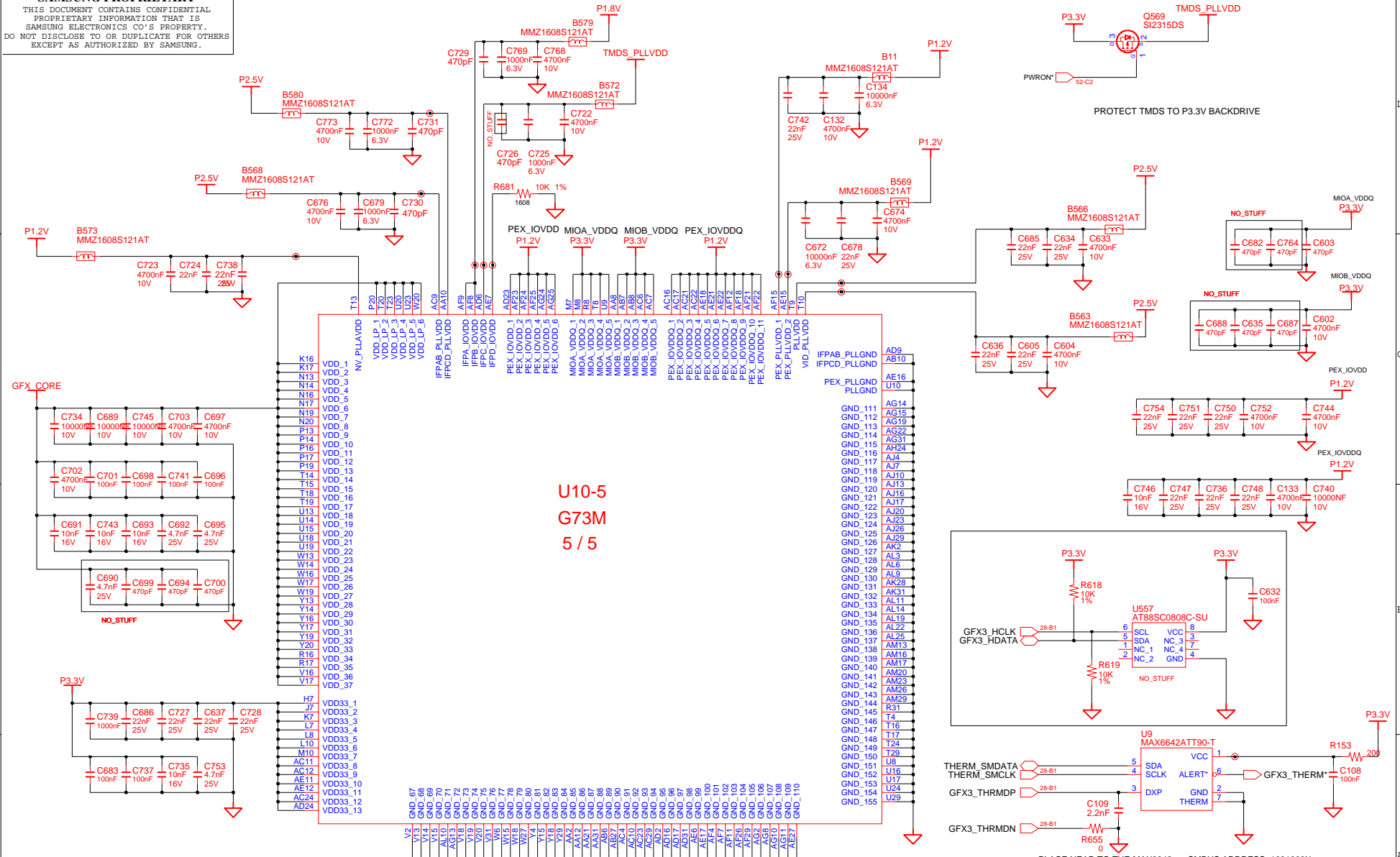


U10-4  
G73M  
4 / 5

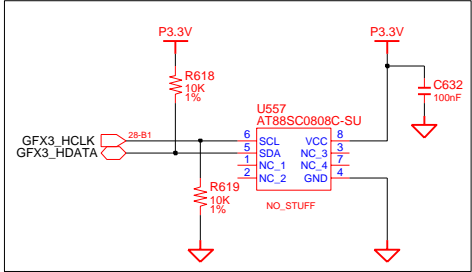
Pin	Description	ACTIVATE
GPIO(0)	DVI DETECT	HIGH
GPIO(1)	TV DETECT	LOW
GPIO(2)	PWM BRIGHTNESS CONTROL	HIGH
GPIO(3)	LCD VDD On ENABLE	HIGH
GPIO(4)	LCD Backlight On/OFF	HIGH
GPIO(5)	GPU Voltage ID0	HIGH=1.0V,LOW=1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU Voltage ID2	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan Control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	HIGH
GPIO(12)	HDTV DET	NC

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR			
APPROVAL	KEVIN LEE	REV	1.3	NVIDIA G73M GRAPHIC 3/4	PART NO.	BA41- 00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	27	OF 56

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U10-5  
 G73M  
 5/5

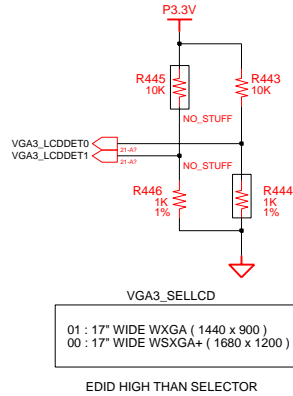


PLACE NEAR TO THE MAX6642 SMBUS ADDRESS: 1001000X

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN		
APPROVAL	KEVIN LEE	REV	1.3	NVIDIA G73M GRAPHIC 4/4	PART NO.	BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	28	OF 56

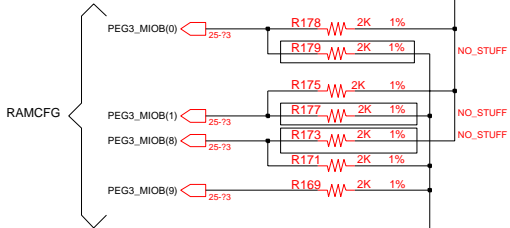
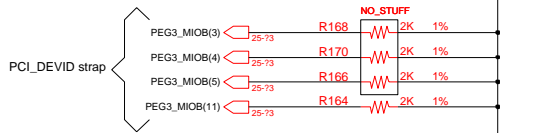
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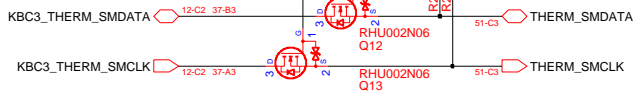
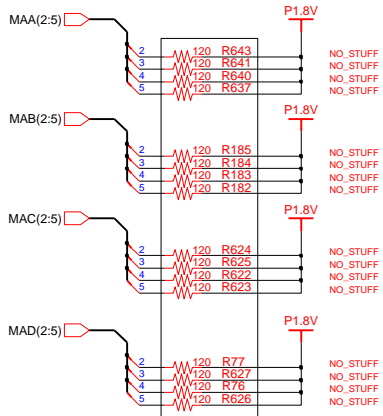
PCI\_DEVID strap

	R168(3)	R170(4)	R166(5)	R164(11)
73M	NO_STUFF	NO_STUFF	NO_STUFF	STUFF
72M	NO_STUFF	NO_STUFF	NO_STUFF	STUFF
72M-V	STUFF	STUFF	STUFF	NO_STUFF



RAMCFG

	R173(8H)	R171(8L)	R175(1H)	R177(1L)
SS 256Mbit	STUFF	NO_STUFF	STUFF	NO_STUFF
IF 256Mbit	STUFF	NO_STUFF	NO_STUFF	STUFF
SS 512Mbit	NO_STUFF	STUFF	STUFF	NO_STUFF
IF 512Mbit	NO_STUFF	STUFF	NO_STUFF	STUFF



Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : SAMSUNG GDDR3 256Mbit 0101 : INFINEON GDDR3 256Mbit 0011 : SAMSUNG GDDR3 512Mbit 0001 : INFINEON GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC 10 : PAL 11 : CRT
PCI_DEVID(3:0) [11,3,5,4]	MIOB(11) MIOB(3) MIOB(5) MIOB(4)	72M: 0X01D8 72M-V: 0X01D7 73M: 0X0398
ROM_TYPE(1:0)	MIOB(10) MIOBVSYN	NO ROM(NC)
USER STRAP	MIOAD(2:5)	EDID
GPIO(12:0)	Sheet 25	Refer to Sheet 25

Test Options for GPIO should be updated..

Samsung		Infineon	
256Mbit	512Mbit	256Mbit	512Mbit
K4J55323QG (1.2/1.4/1.6/2.0) K4J55323QF (1.4/1.6/2.0)	K4J52324QC (1.2/1.4/1.6/2.0)	HYB18H256321AF16(2.0) HYB18H256321AF16(1.6) HYB18H256324AF-20(2.0) HYB18H256321AF-14(1.4) HYB18H256321AF-12(1.2)	HYB18H512321AF16(2.0) HYB18H512321AF16(1.6) HYB18H512324AF-20(1.6) HYB18H512321AF-14(1.4) HYB18H512321AF-12(1.2)
8M*32BIT	16M*32BIT	8M*32BIT	16M*32BIT

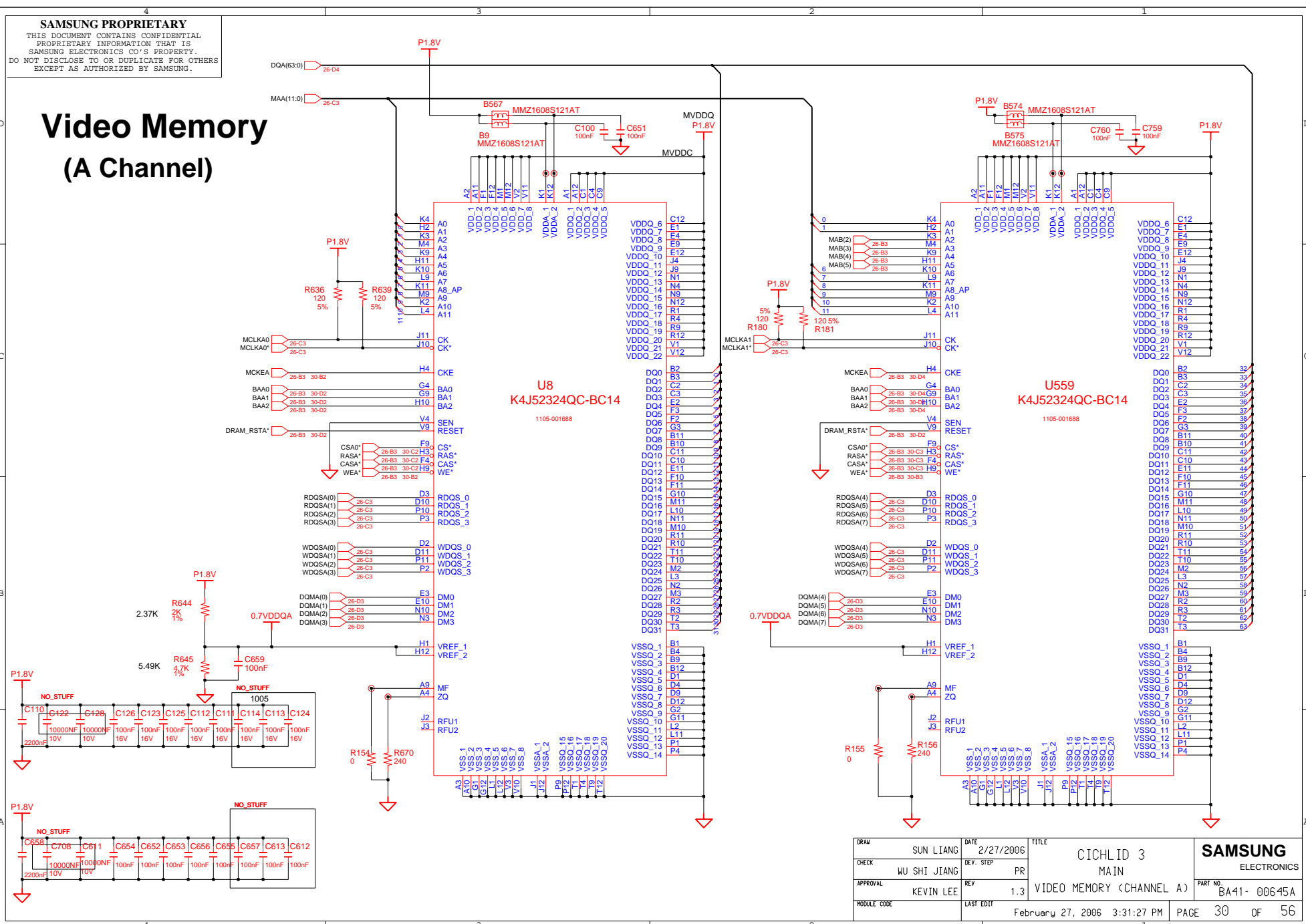
DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN		
APPROVAL	KEVIN LEE	REV	1.3	NVIDIA G73M STRAP		PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	29	OF 56



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# Video Memory (A Channel)



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	KEVIN LEE	REV	1.3	VIDEO MEMORY (CHANNEL A)	BA41-00645A	PAGE 30 OF 56
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM			

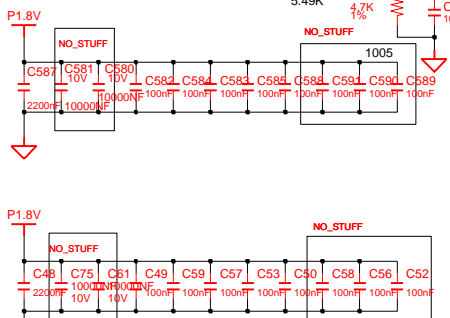
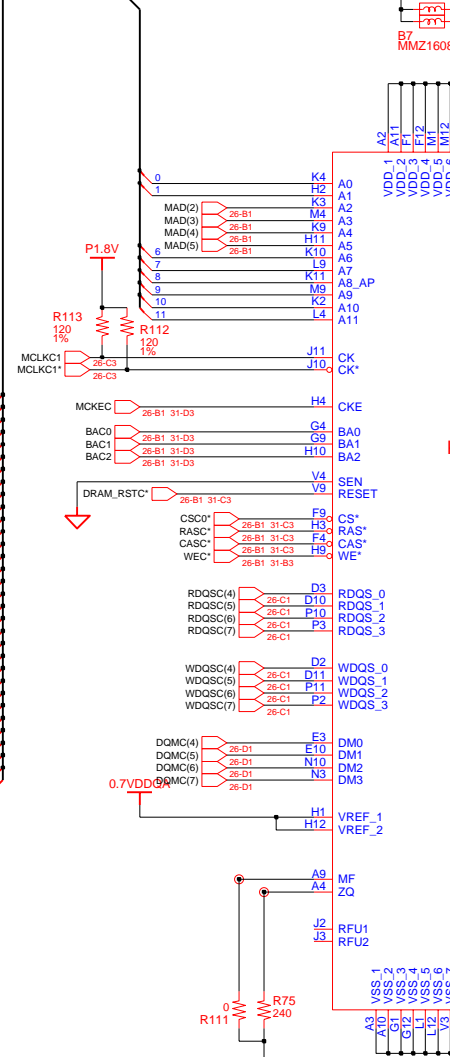
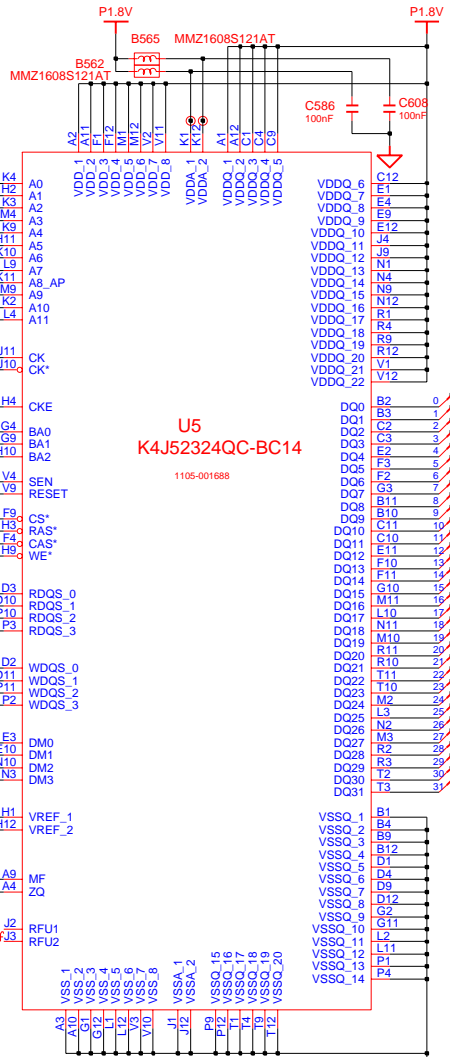
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# Video Memory (C Channel)

DOC(63:0) 26-D2

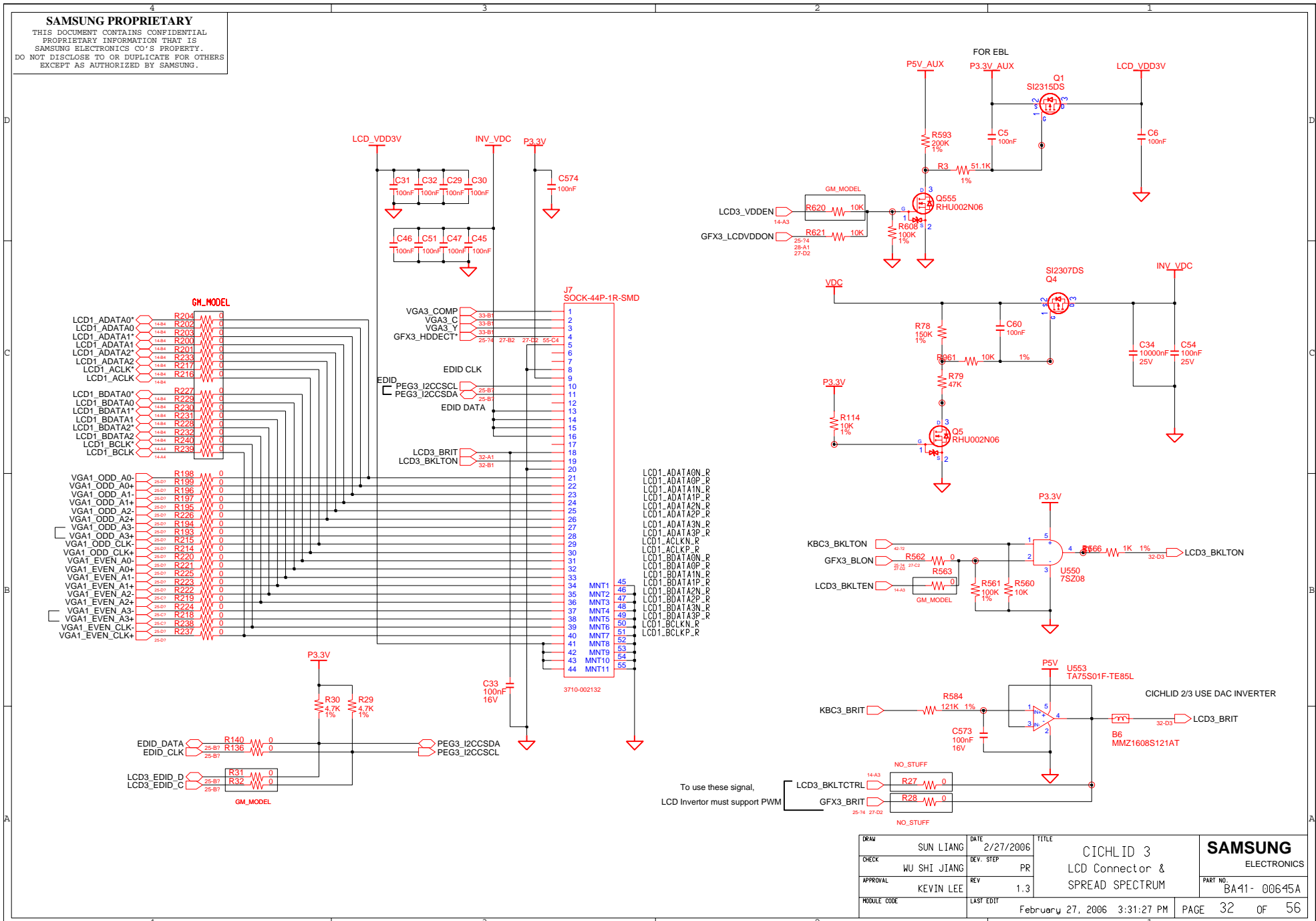
MAC(11:0) 26-C1



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN		
APPROVAL	KEVIN LEE	REV	1.3	VIDEO MEMORY (CHANNEL C)		PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	31	OF 56

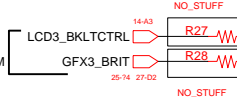
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- LCD1\_ADATA0N\_R
- LCD1\_ADATA0P\_R
- LCD1\_ADATA1N\_R
- LCD1\_ADATA1P\_R
- LCD1\_ADATA2N\_R
- LCD1\_ADATA2P\_R
- LCD1\_ADATA3N\_R
- LCD1\_ADATA3P\_R
- LCD1\_ACLKN\_R
- LCD1\_ACLKP\_R
- LCD1\_BDATA0N\_R
- LCD1\_BDATA0P\_R
- LCD1\_BDATA1N\_R
- LCD1\_BDATA1P\_R
- LCD1\_BDATA2N\_R
- LCD1\_BDATA2P\_R
- LCD1\_BDATA3N\_R
- LCD1\_BDATA3P\_R
- LCD1\_BCLKN\_R
- LCD1\_BCLKP\_R

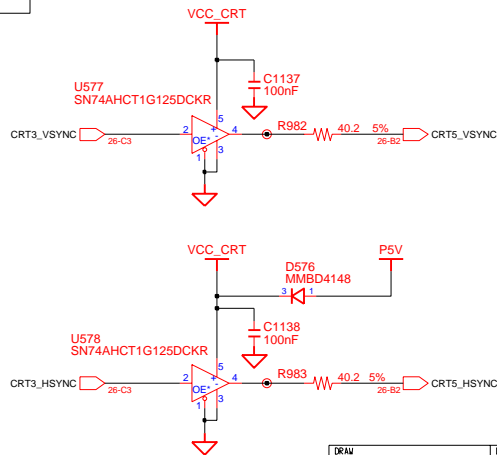
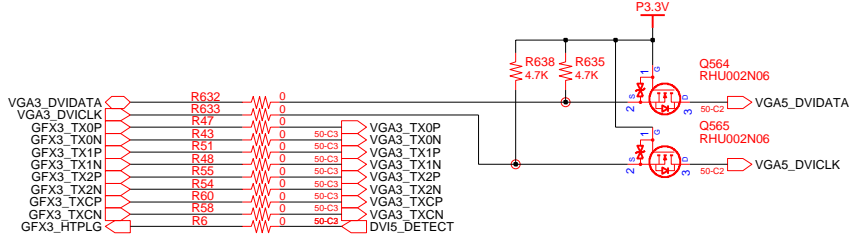
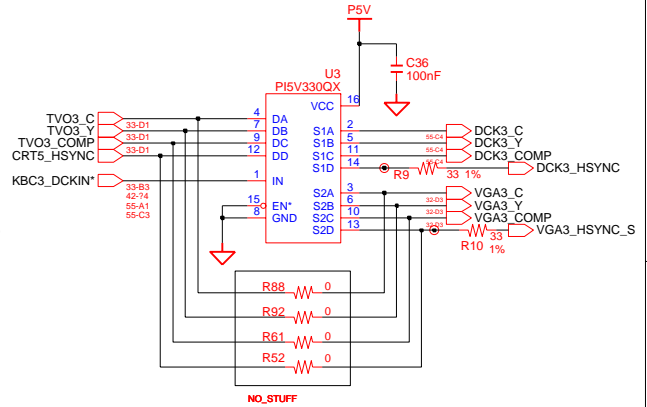
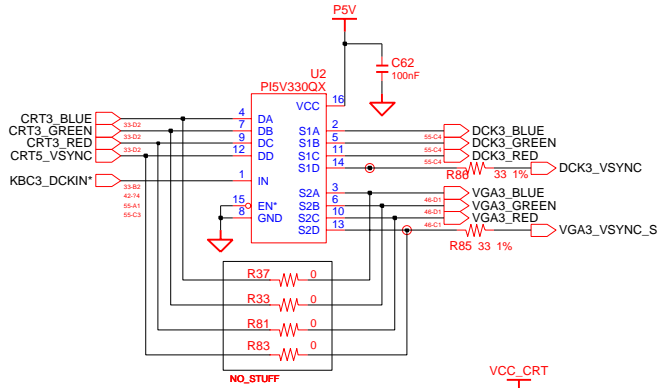
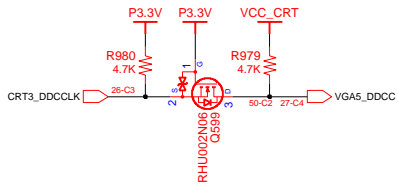
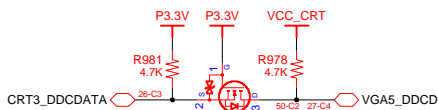
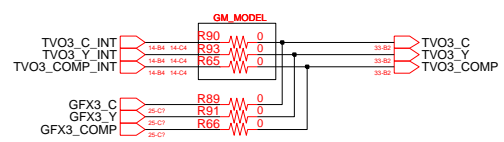
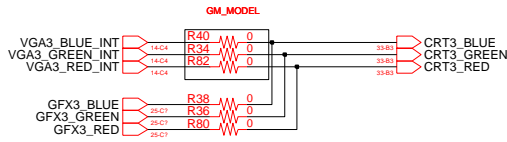
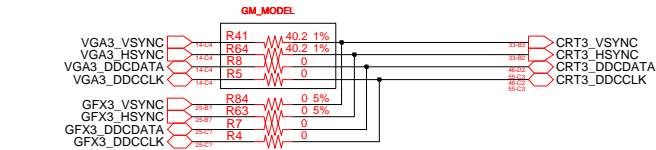
To use these signal, LCD Inverter must support PWM



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHlid 3 LCD Connector & SPREAD SPECTRUM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A	
CHECK	WU SHI JIANG	DEV. STEP	PR				
APPROVAL	KEVIN LEE	REV	1.3				
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE			32 OF 56

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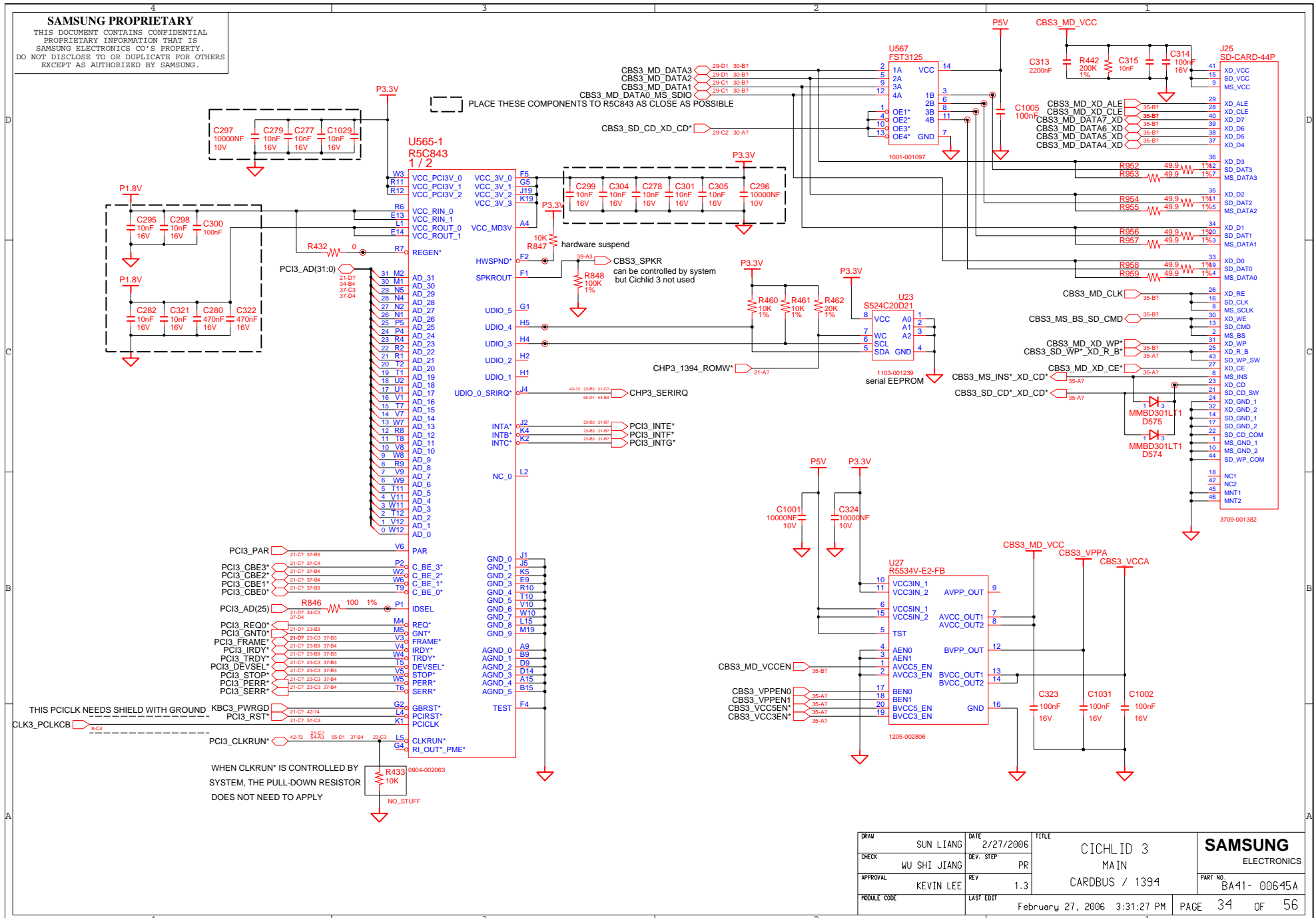
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DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN CRT PORT	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	PART NO.		
APPROVAL	KEVIN LEE	REV	1.3	February 27, 2006 3:31:27 PM	PAGE	33 OF 56
MODULE CODE		LAST EDIT				

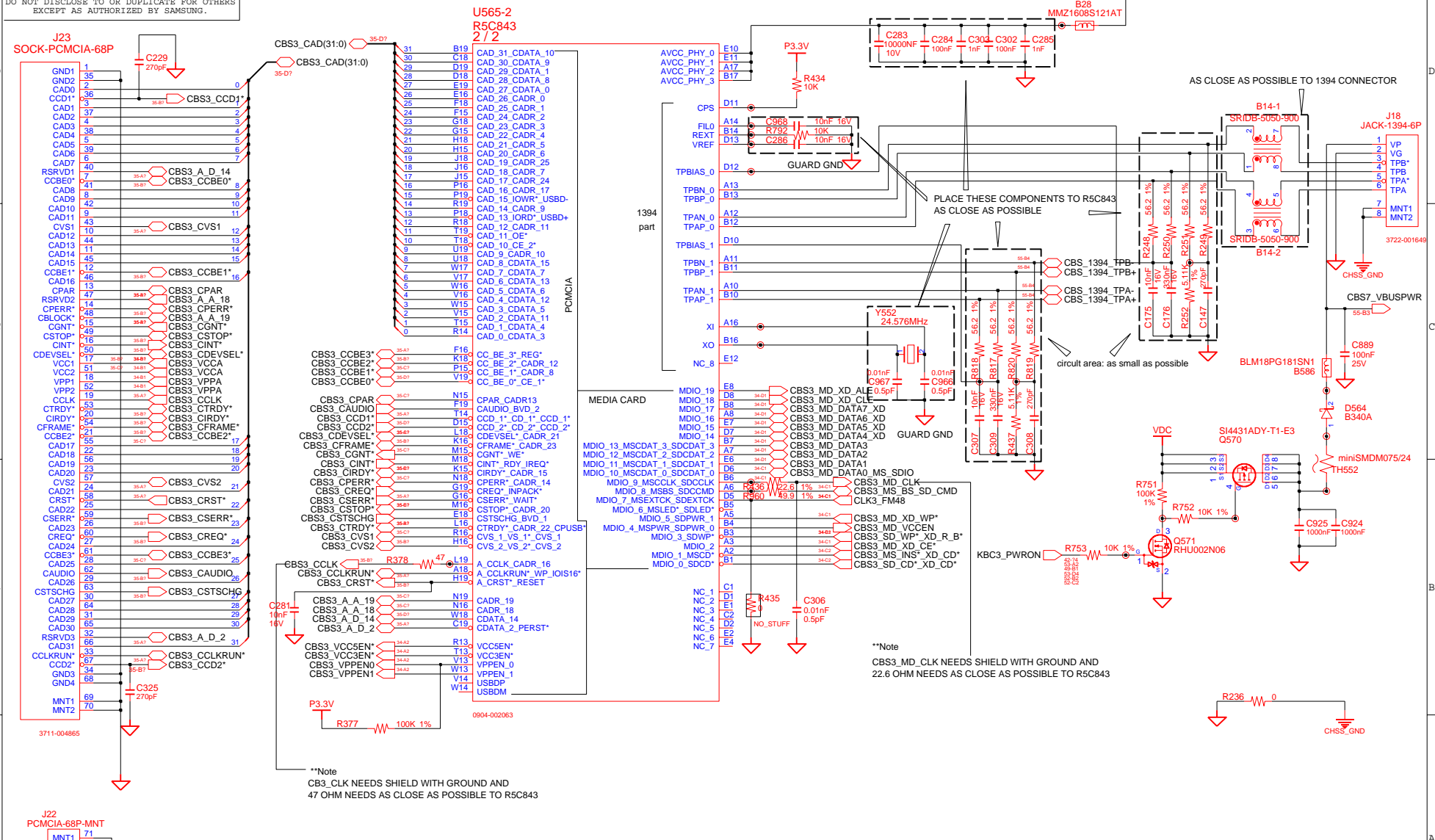
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DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN CARDBUS / 1394	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR	REV		
APPROVAL	KEVIN LEE	REV	1.3	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE 34 OF 56
MODULE CODE						

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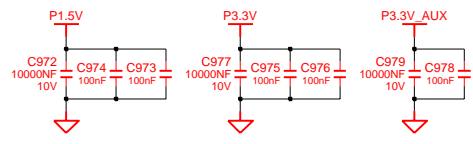
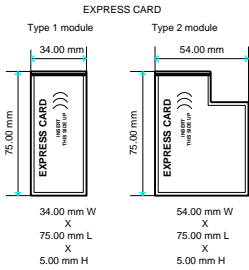
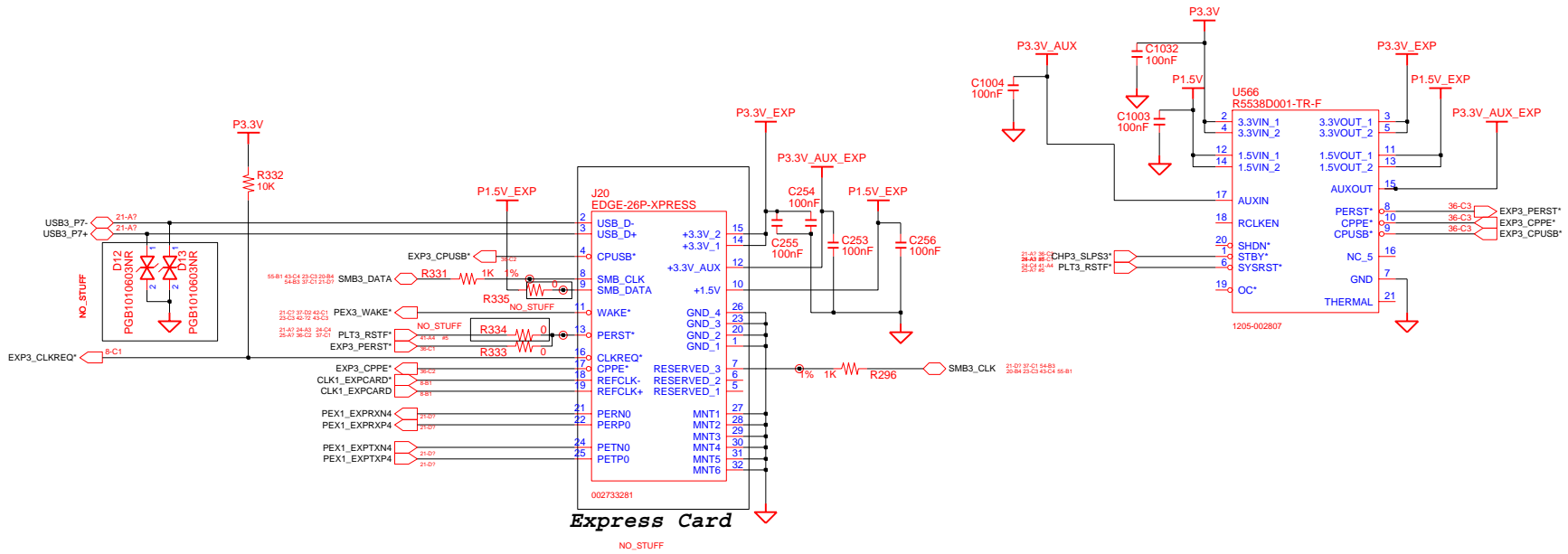
\*\*Note  
 CBS3\_CLK NEEDS SHIELD WITH GROUND AND  
 47 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

\*\*Note  
 CBS3\_MD\_CLK NEEDS SHIELD WITH GROUND AND  
 22.6 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C843

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN		
APPROVAL	KEVIN LEE	REV	1.3	CARDBUS SOCKET/MEDIA CARD	PART NO.	BA41- 00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	35	OF 56

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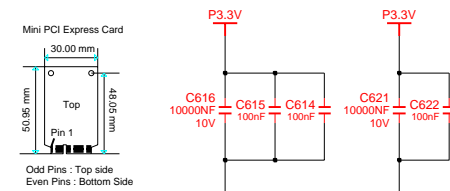
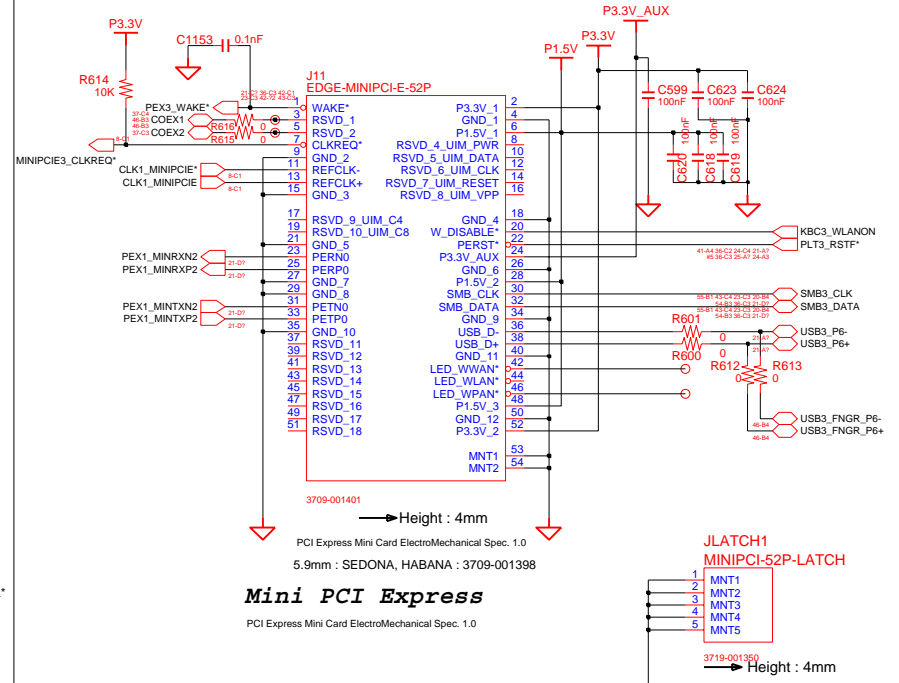
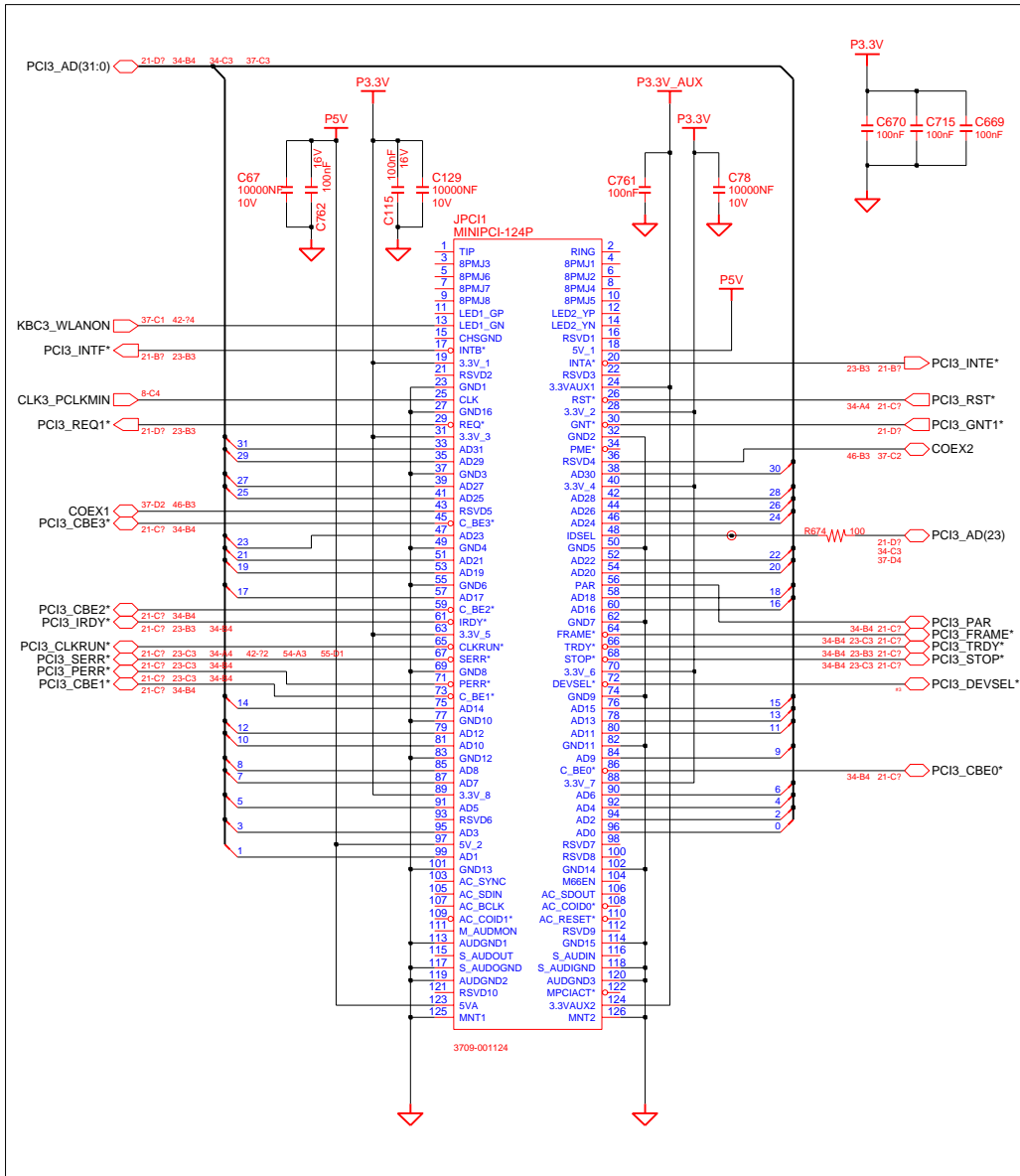
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DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR			
APPROVAL	KEVIN LEE	REV	1.3		EXPRESS CARD	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	36	OF 56

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**NO\_STUFF** (WHEN USE MINICARD CONNECTOR)

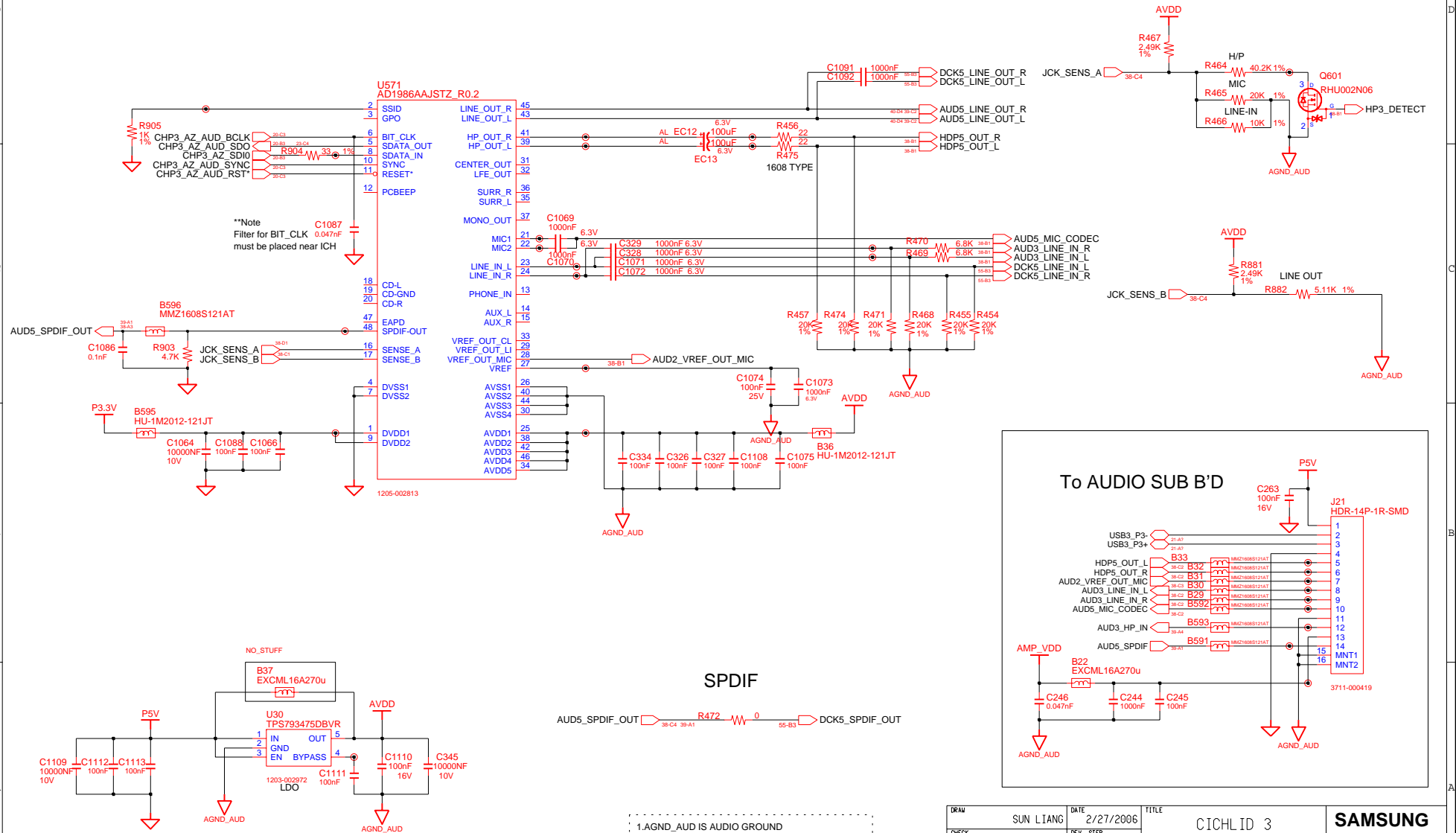


DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR	REV	1.3	
APPROVAL	KEVIN LEE	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	37	OF 56



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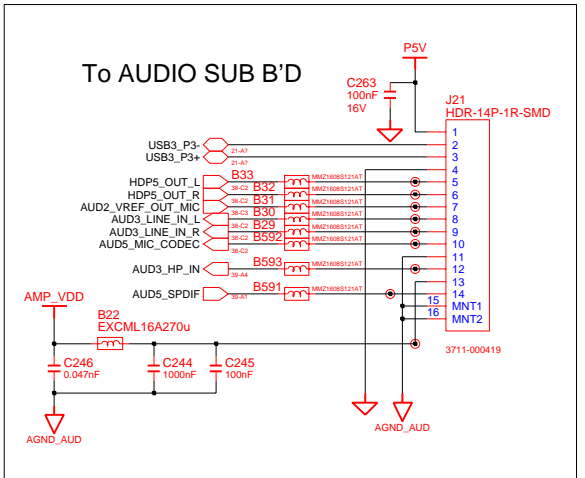


**\*\*Note**  
Filter for BIT\_CLK C1087  
must be placed near ICH

**SPDIF**

AUD5\_SPDIF\_OUT 38-C4 R472 0 55-B3 DCK5\_SPDIF\_OUT

- 1. AGND\_AUD IS AUDIO GROUND
- 2. GND is Digital Ground
- 3. AGND\_MIC IS MIC GROUND

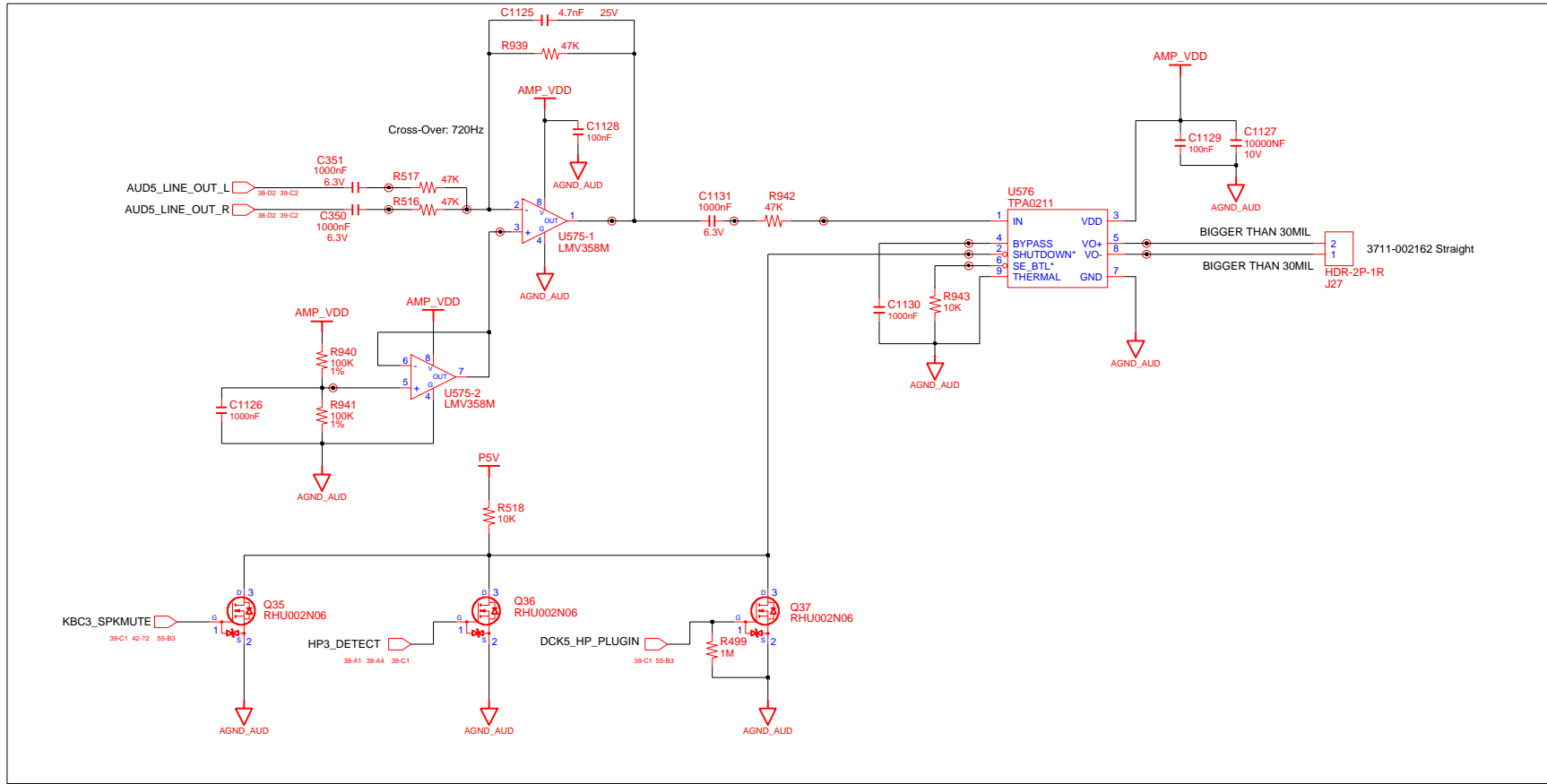


DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3	AUDIO CODEC & SUB B'D CONN		PART NO. BA41-00645A
MODULE CODE	undefined	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	38	OF 56

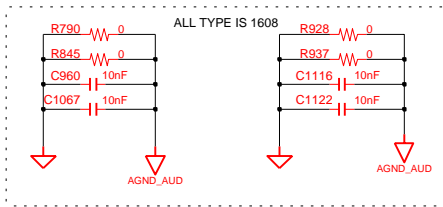


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NO\_STUFF



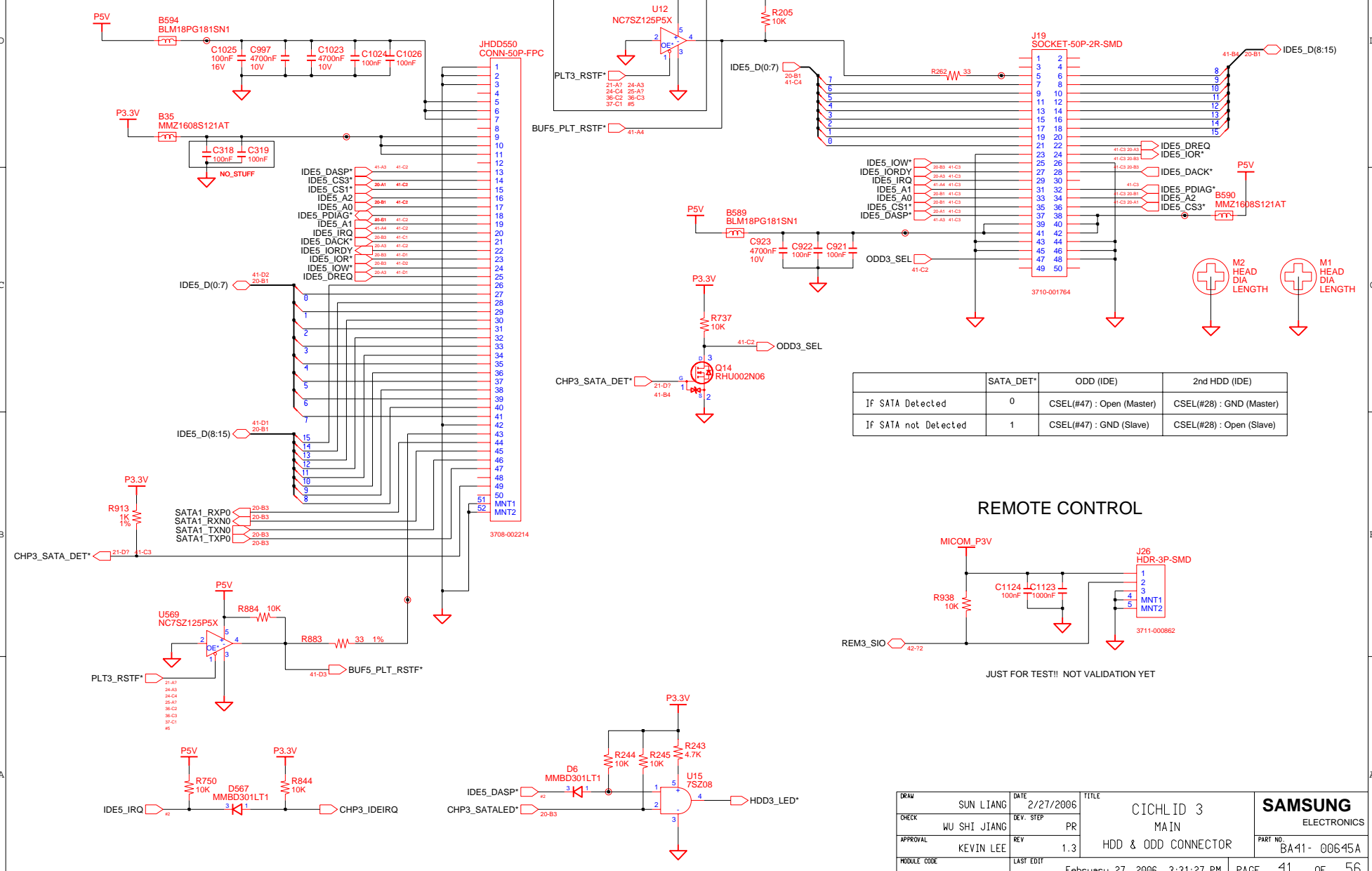
DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN UPPER & AUDIO CONN	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	PART NO.		
APPROVAL	KEVIN LEE	REV	1.3	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE 40 OF 56
MODULE CODE						

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**Main to HDD**

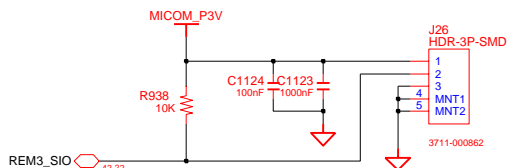
NO\_STUFF

**Main to Swap B'd**



	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)

**REMOTE CONTROL**

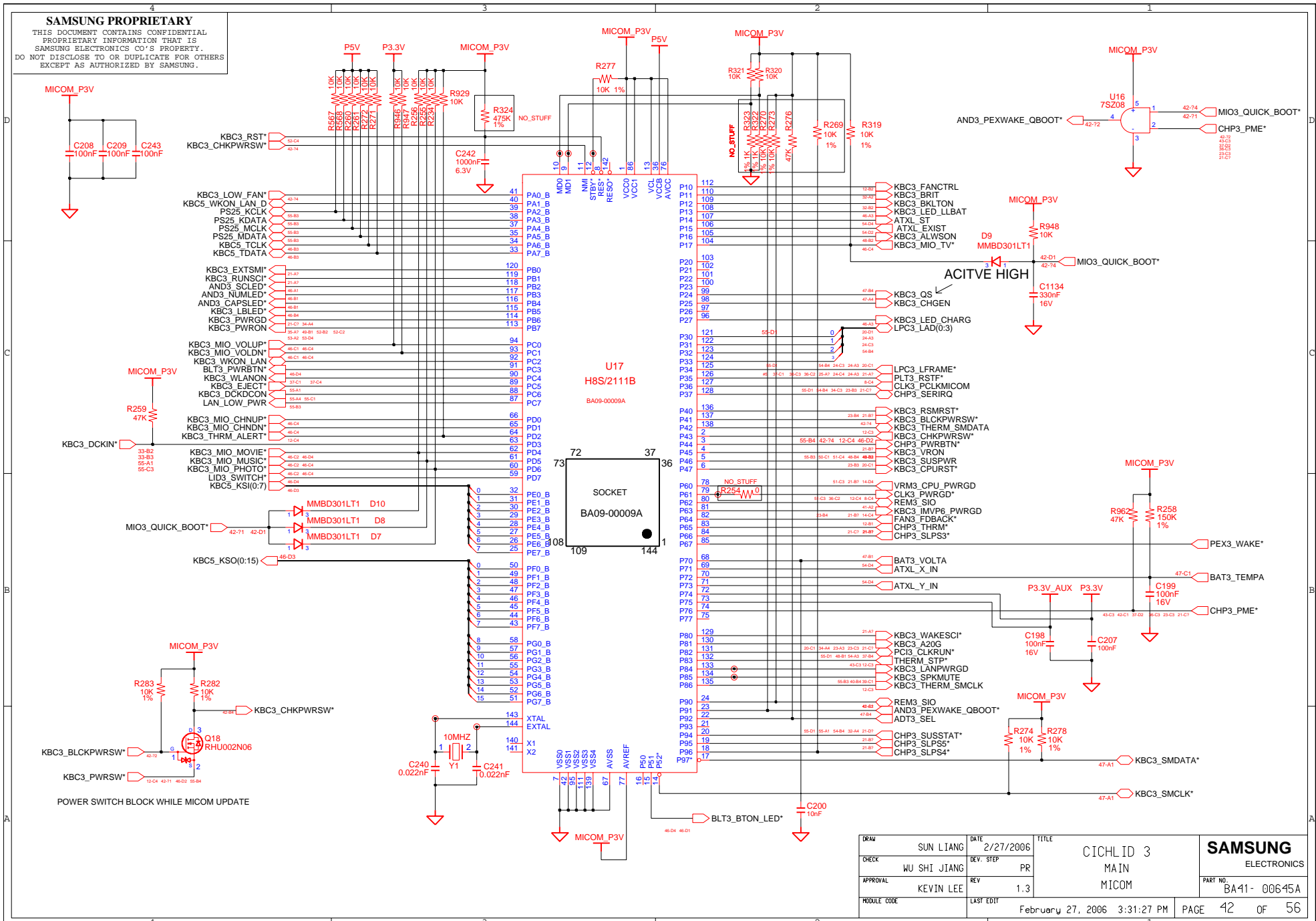


JUST FOR TEST!! NOT VALIDATION YET

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN HDD & ODD CONNECTOR	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR	REV		
APPROVAL	KEVIN LEE	REV	1.3	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE 41 OF 56

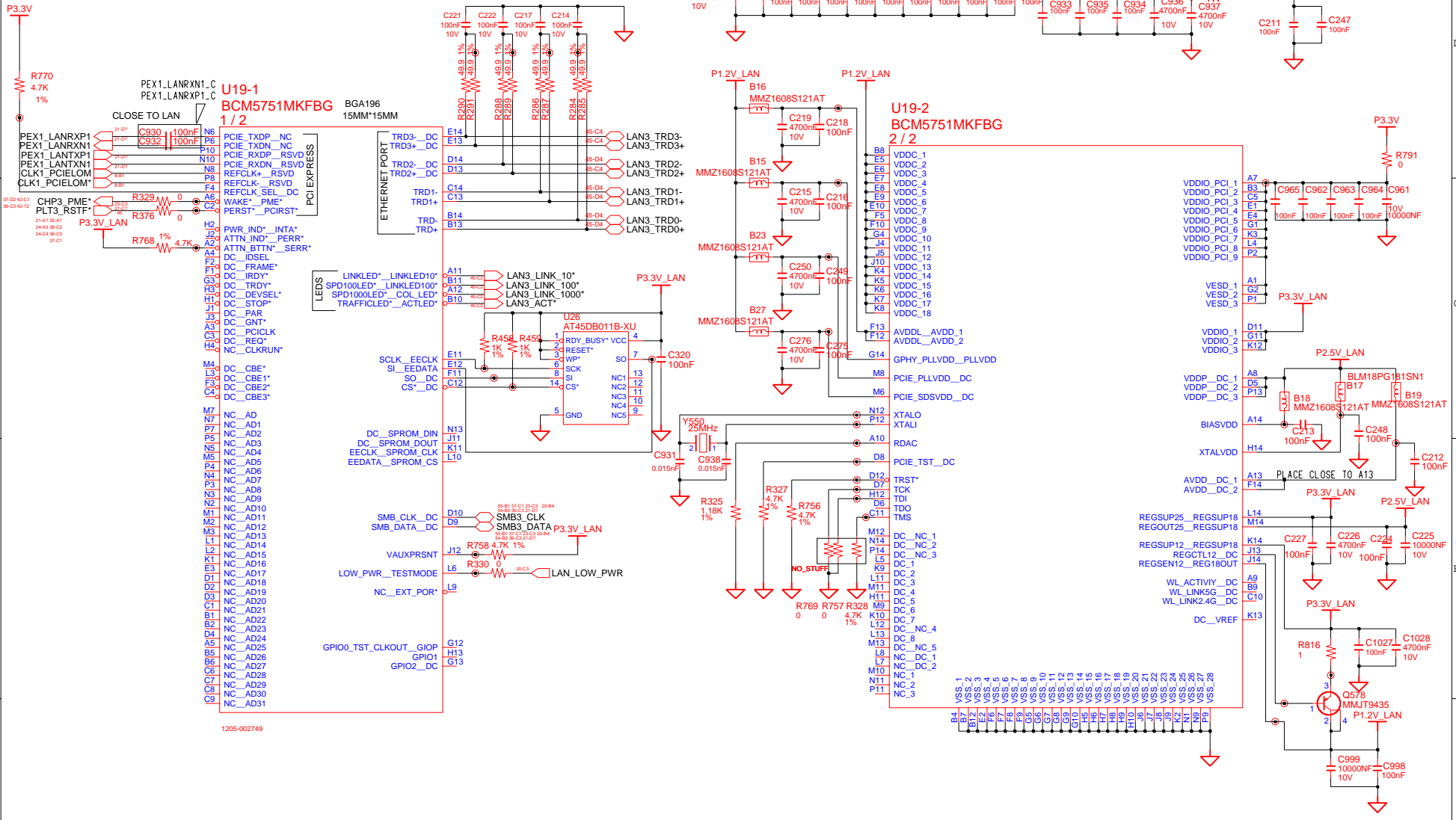
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DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	KEVIN LEE	REV	1.3	MICOM	BA41-00645A	
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	42 OF 56	

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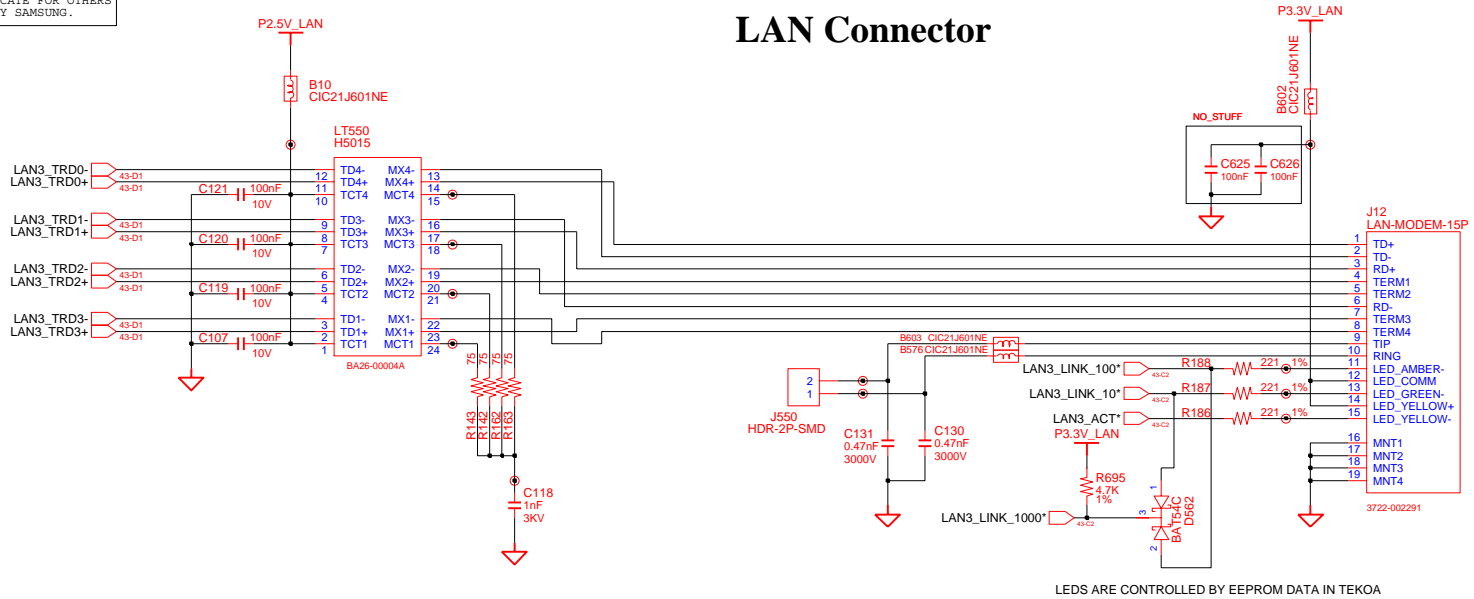
1205-002749

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3		LAN(BROADCOM BCM5751M)	PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	43	OF 56

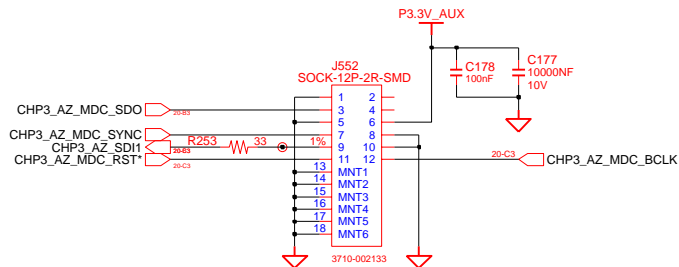
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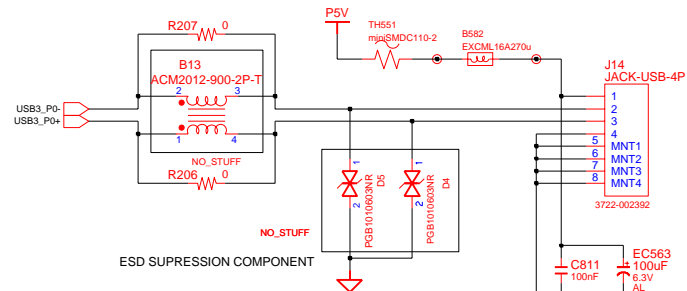
# LAN Connector



# MDC Connector



# USB0 Connector



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR		MAIN	
APPROVAL	KEVIN LEE	REV	1.3	LAN & USB0 & MODEM Conn.	PART NO.	BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	44	OF 56

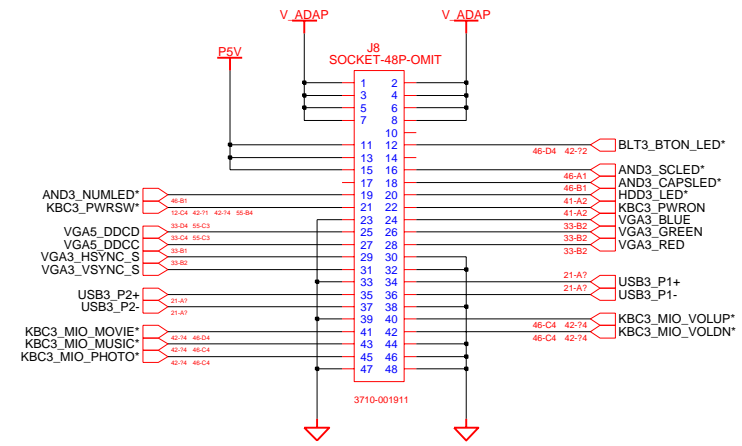
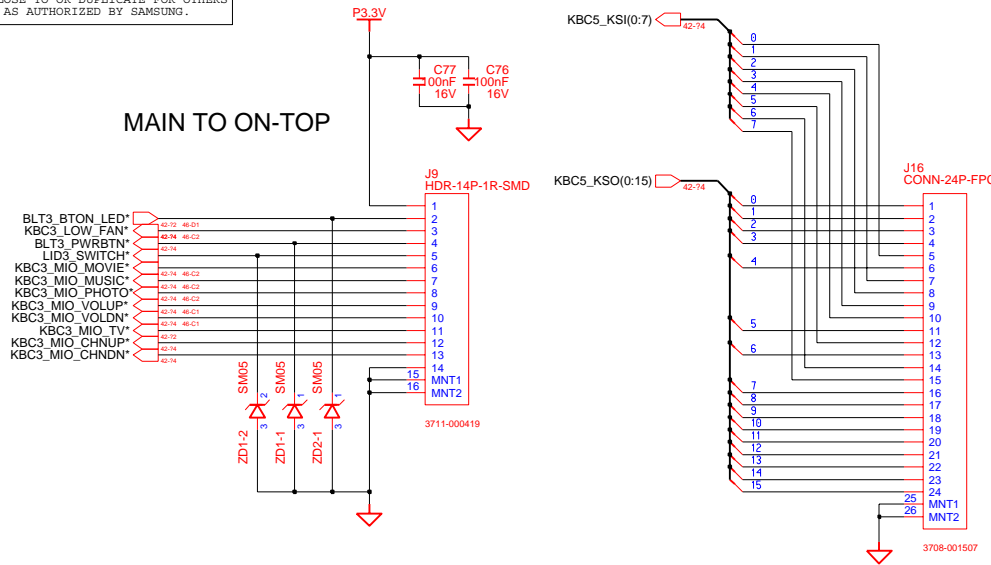
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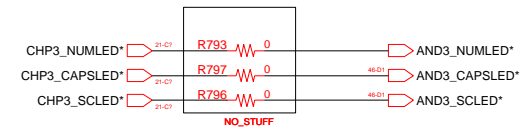
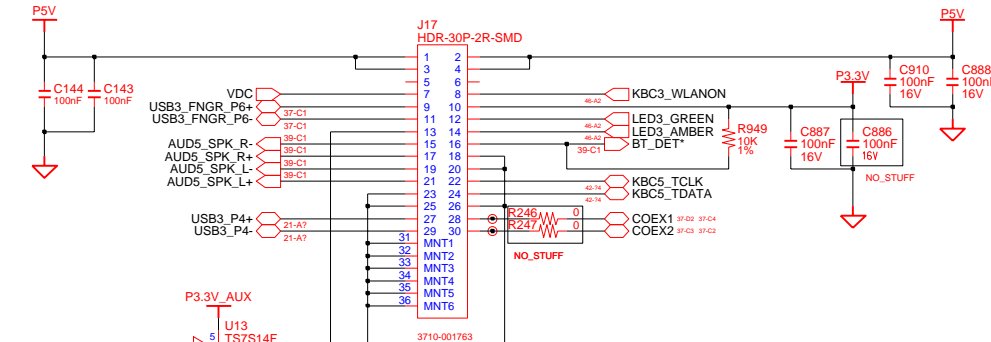
**KEYBOARD**

**Main to DC/DC BOARD**

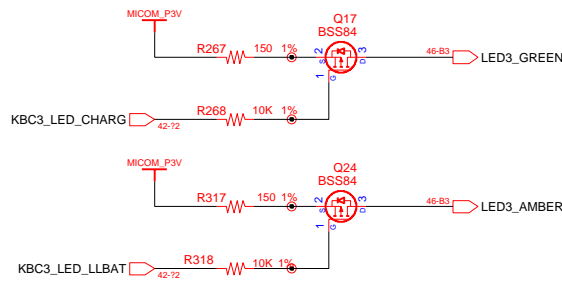
**MAIN TO ON-TOP**



**TOUCHPAD CONNECTOR**



**ADAPTERIN/CHARGING LED**

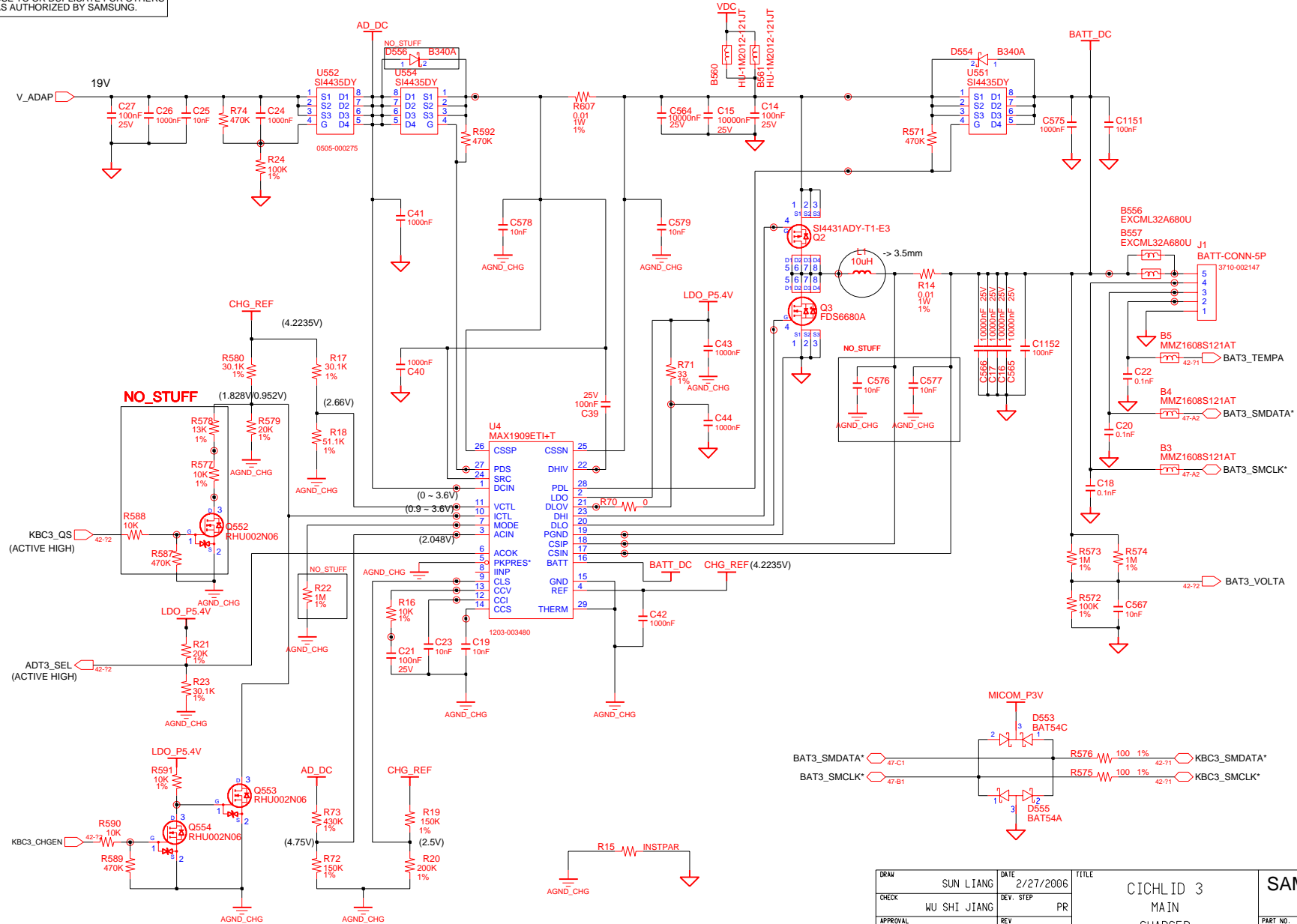


DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	MAIN		
APPROVAL	KEVIN LEE	REV	1.3	B'D TO B'D CONNECTOR		PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	45	OF 56



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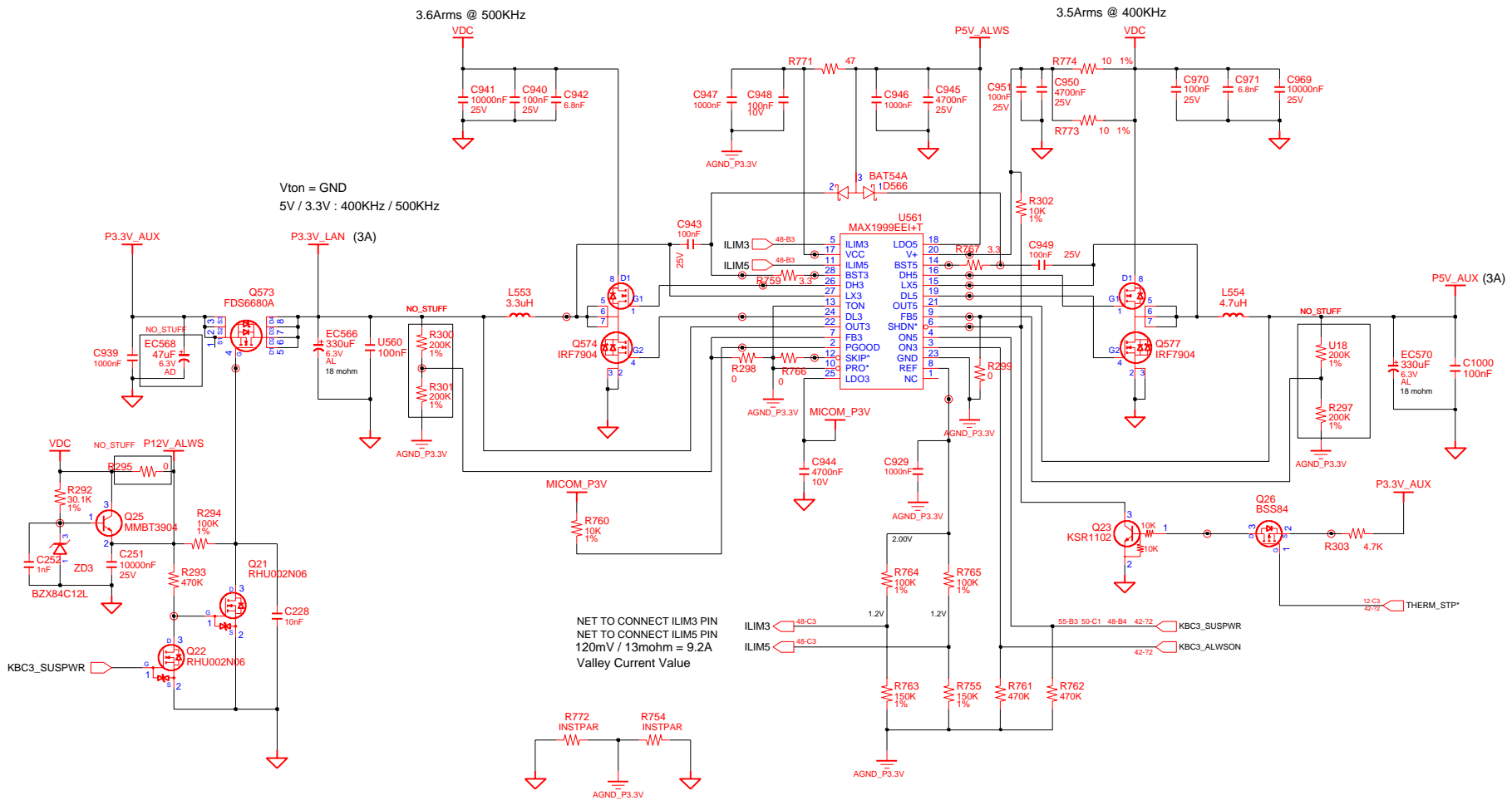
# CHARGER & POWER MANAGEMENT



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR	REV	1.3	
APPROVAL	KEVIN LEE	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	46	OF 56

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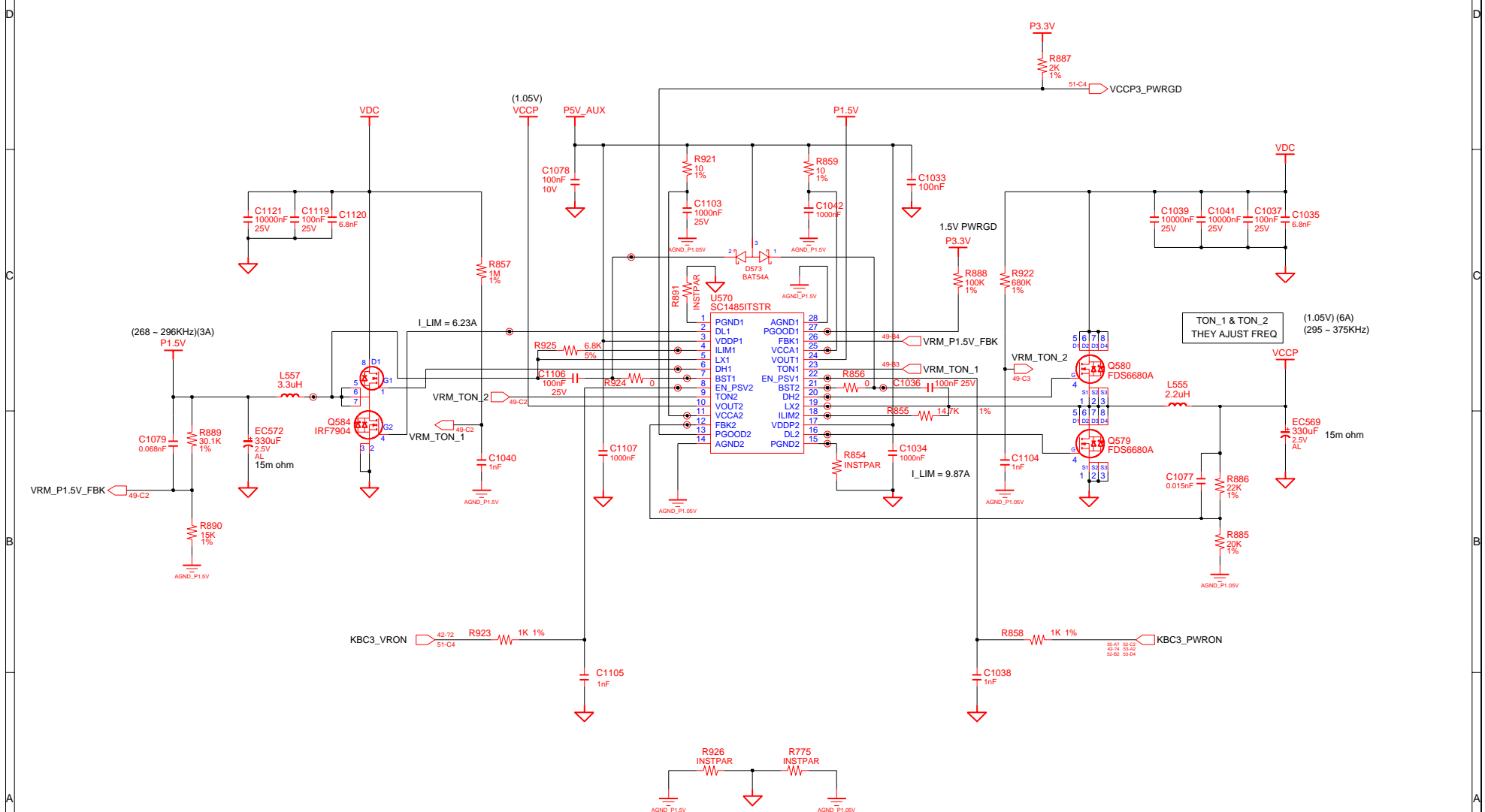
# P3.3V\_ALWAYS/AUX & P5V\_AUX



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 POWER	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	P3.3V ALWAYS & P5V_AUX		
APPROVAL	KEVIN LEE	REV	1.3			PART NO. BA41-00645A
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	47	OF 56

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# P1.5V & VCCP (1.05V)

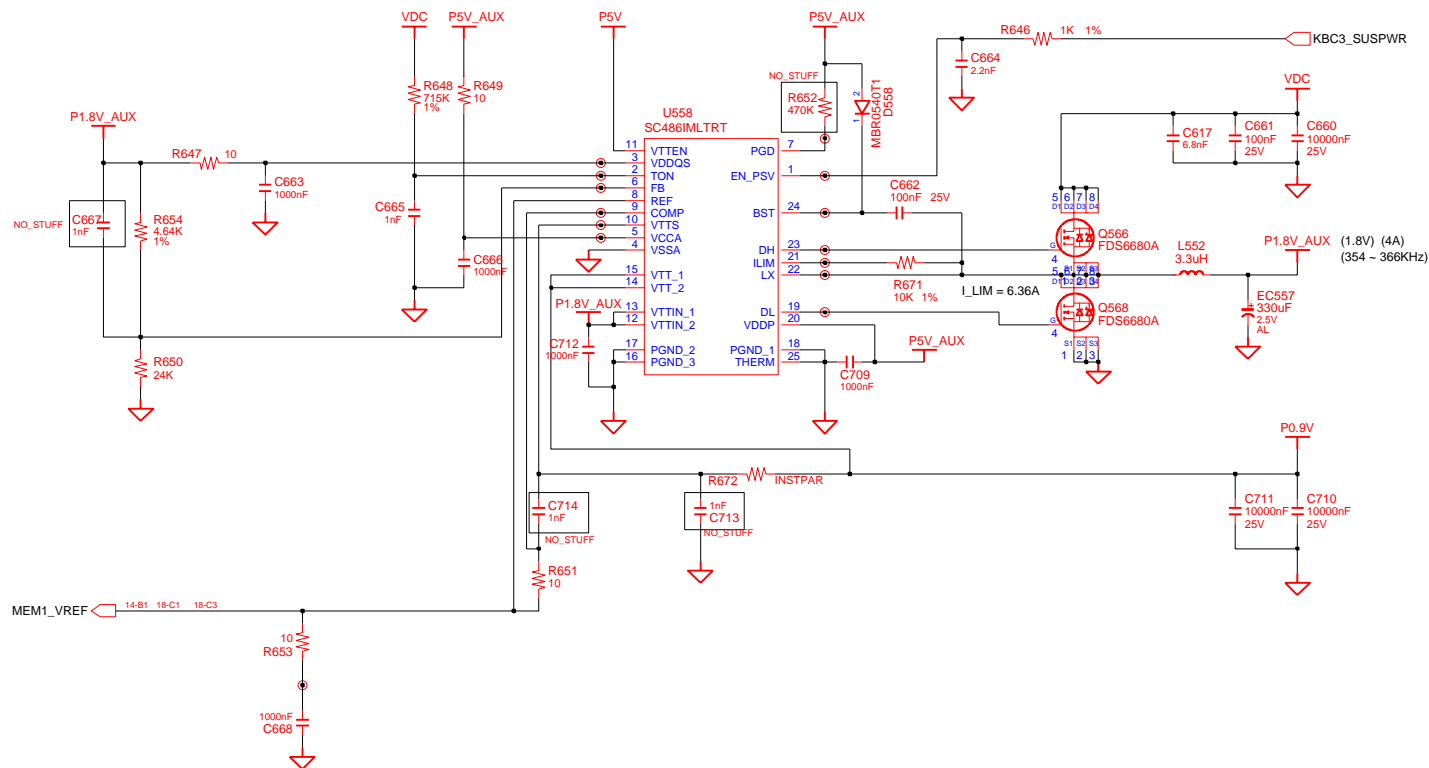


TON\_1 & TON\_2  
 THEY AJUST FREQ (1.05V) (6A)  
 (295 - 375KHz)

DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLD 3 POWER P1.5V & VCCP	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR			
APPROVAL	KEVIN LEE	REV	1.3			
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE 48 OF 56		

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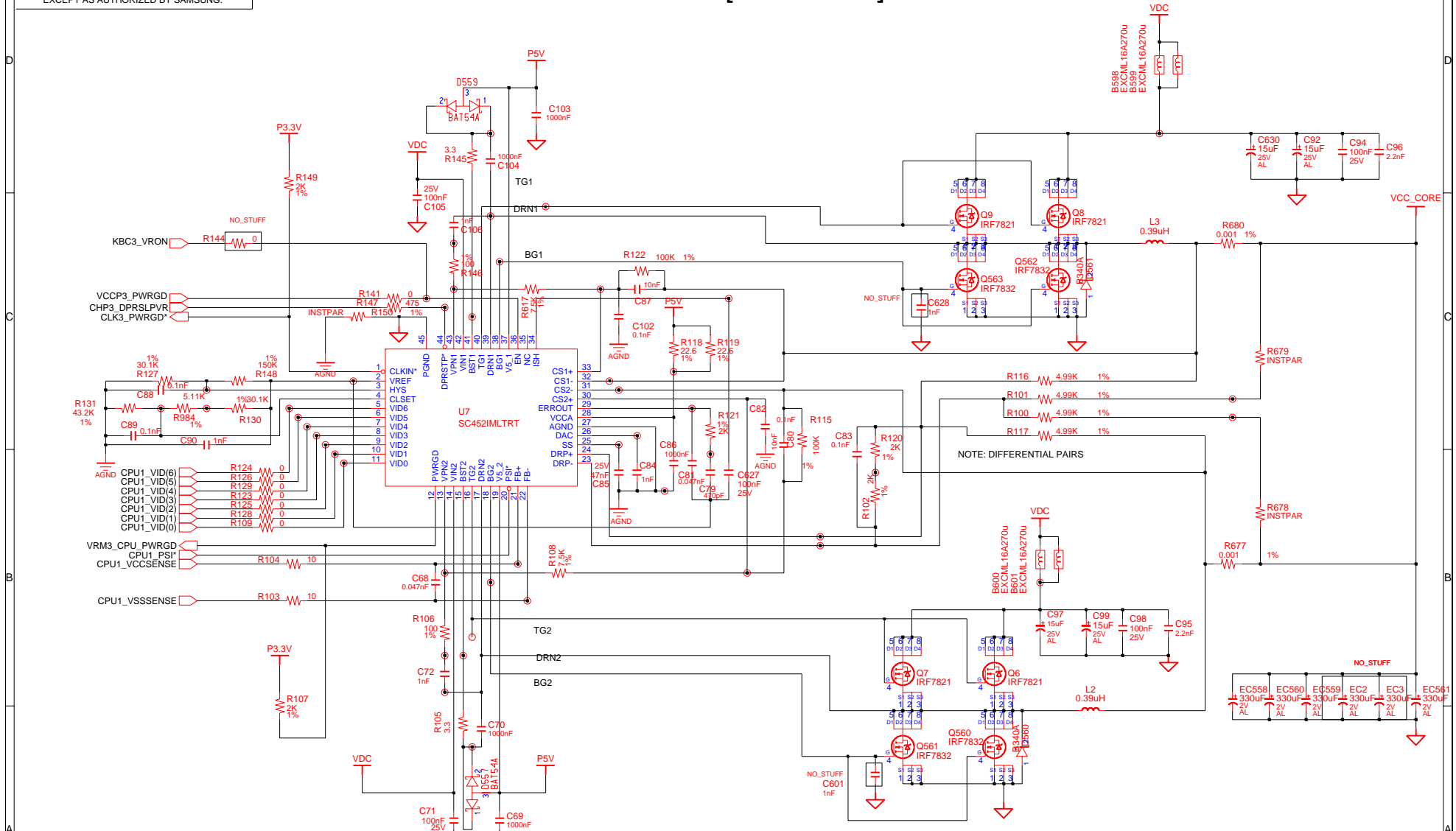
# DDR2 Power



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN DDR POWER	SAMSUNG ELECTRONICS	
CHECK	WU SHI JIANG	DEV. STEP	PR	PART NO.			BA41-00645A
APPROVAL	KEVIN LEE	REV	1.3	PAGE			49 OF 56
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM				

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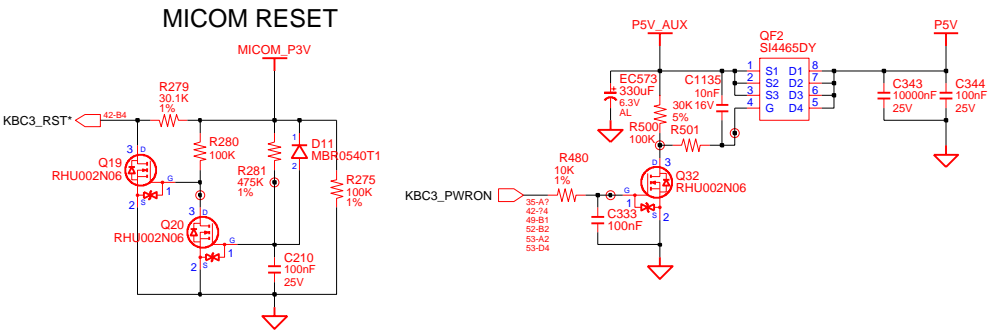
# CPU VRM [SEMTECH]



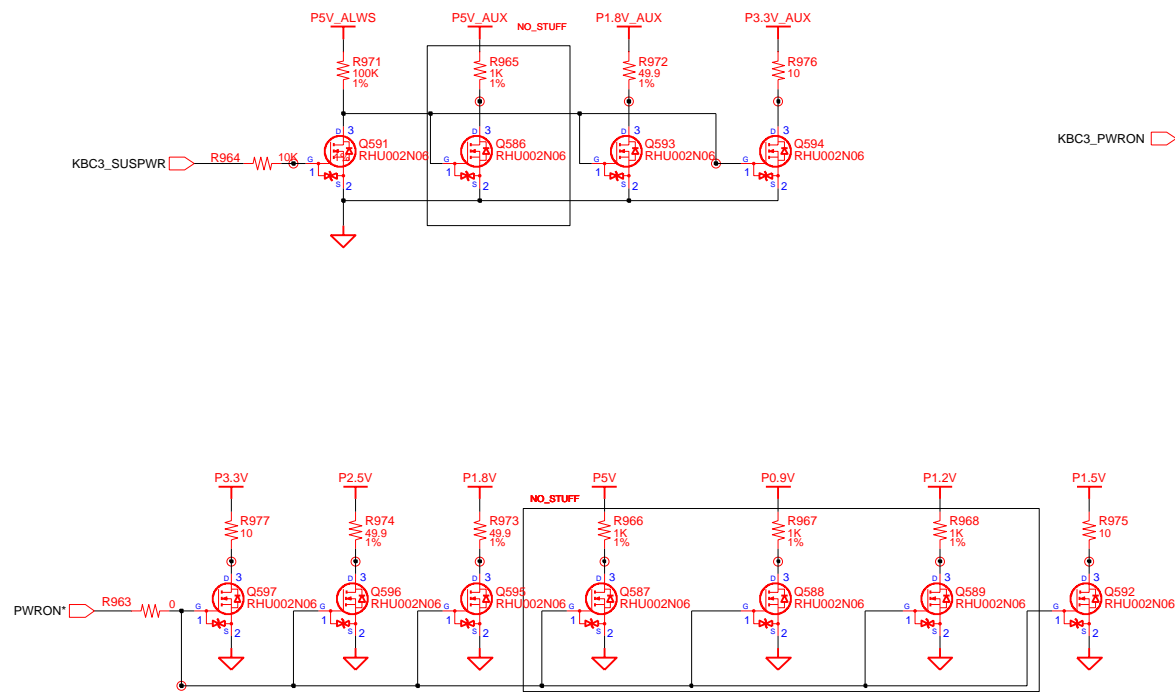
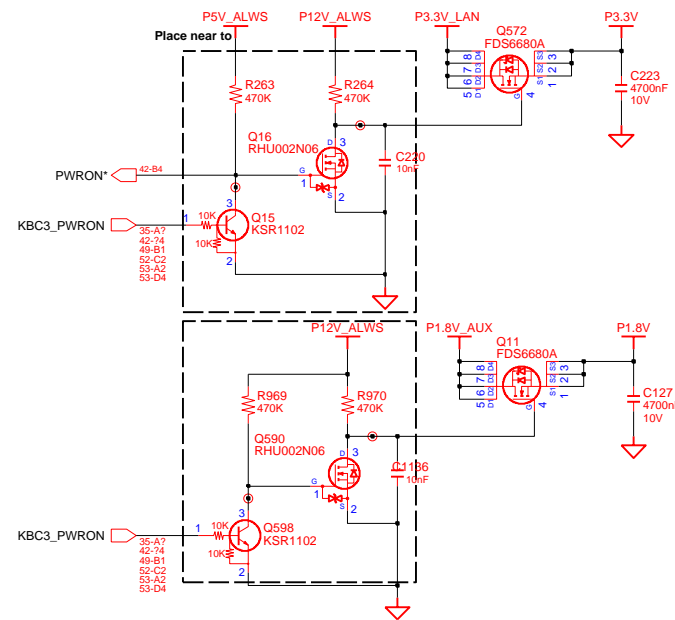
DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA41-00645A
CHECK	WU SHI JIANG	DEV. STEP	PR			
APPROVAL	KEVIN LEE	REV	1.3			
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	50	OF 56

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### Switched Power On (P5V)



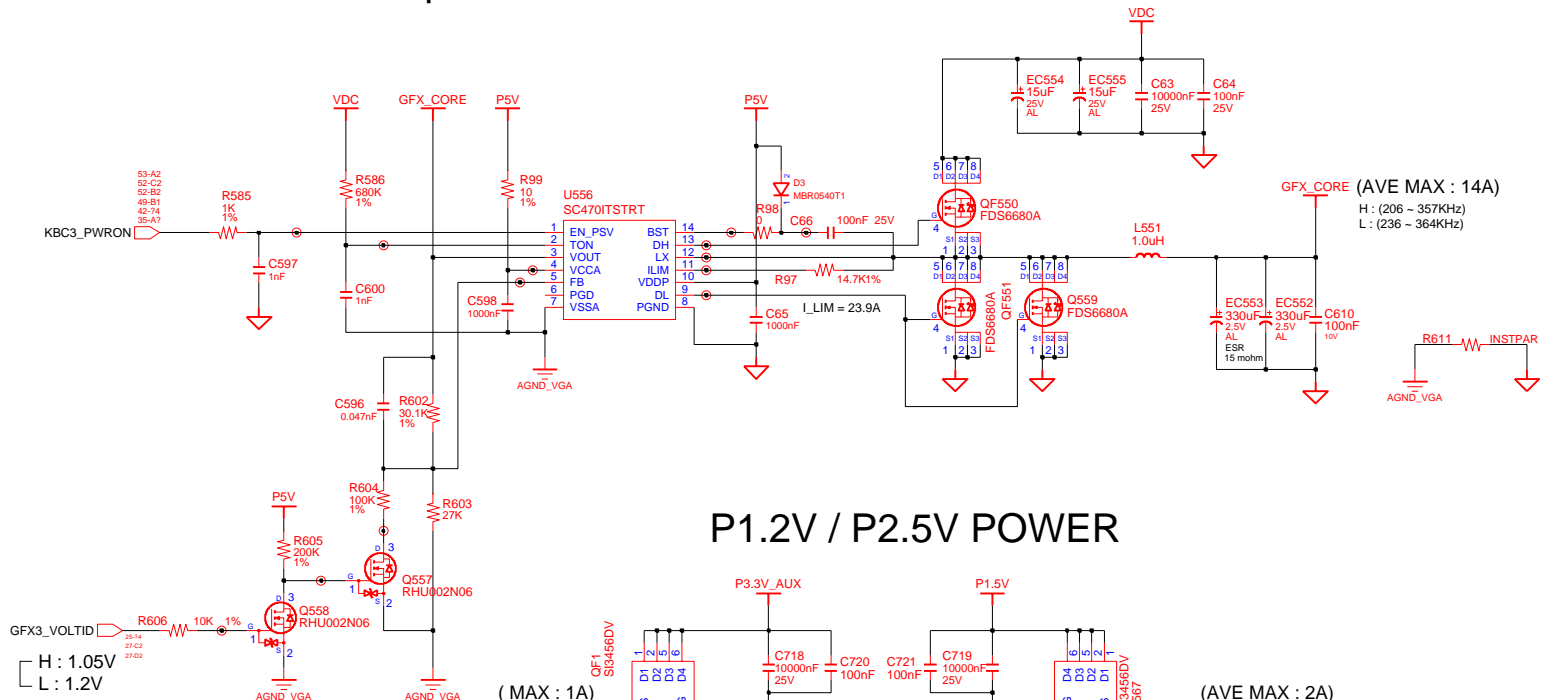
### Switched Power On (P3.3V & 1.8V)



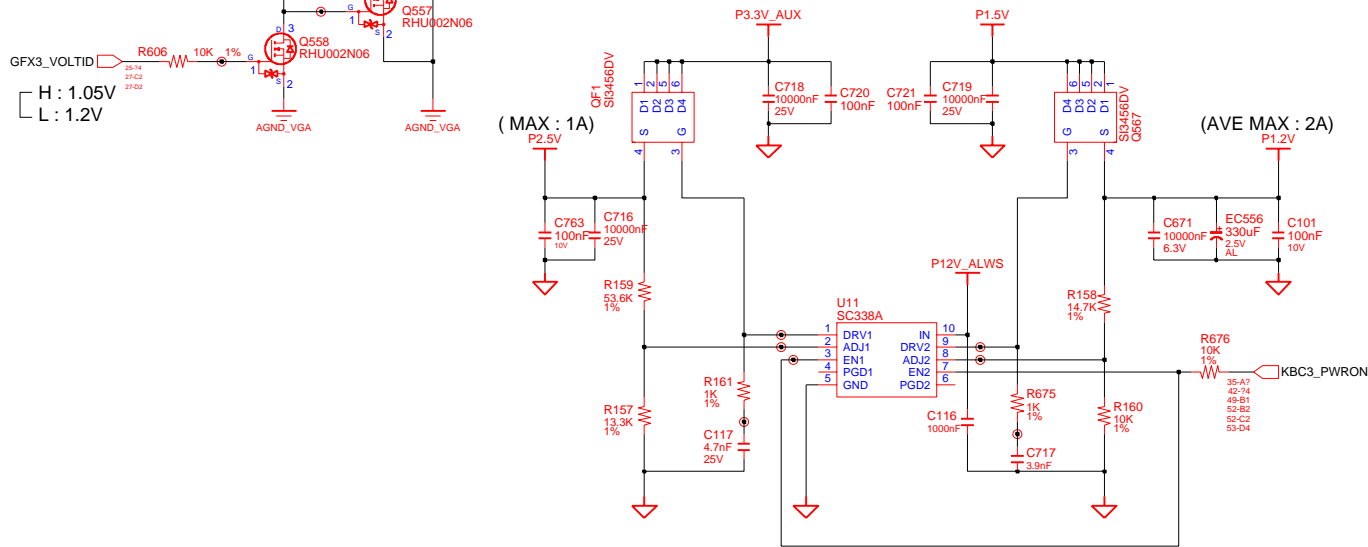
DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLD 3 MAIN MICOM & SWITCHED POWER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00645A	
CHECK	WU SHI JIANG	DEV. STEP	PR				
APPROVAL	KEVIN LEE	REV	1.3				
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM				
						PAGE	51 OF 56

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# Graphic Core Power



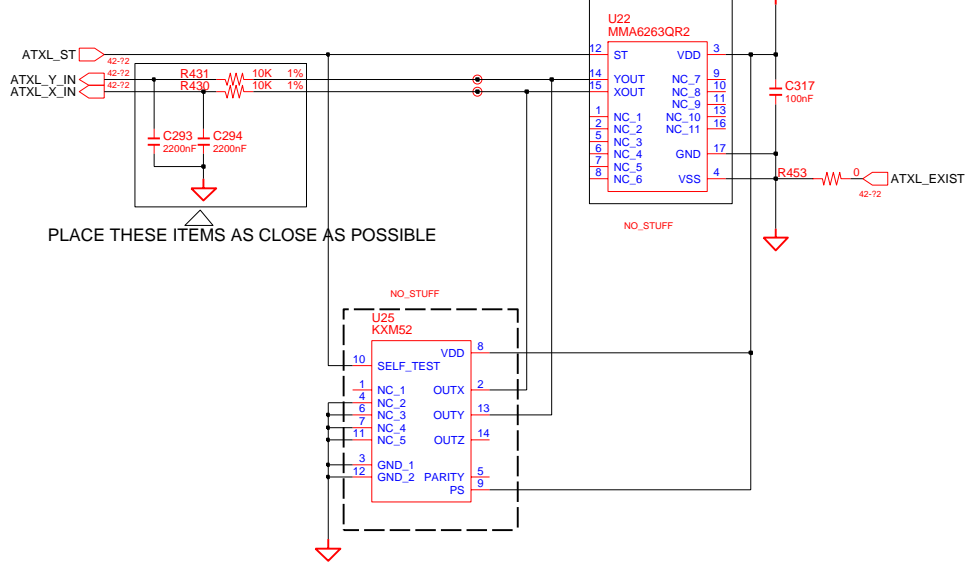
# P1.2V / P2.5V POWER



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 GFX POWER	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR			
APPROVAL	KEVIN LEE	REV	1.3	P1.2V & P2.5V AUX POWER		PART NO.
MODULE CODE		LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	52	OF 56

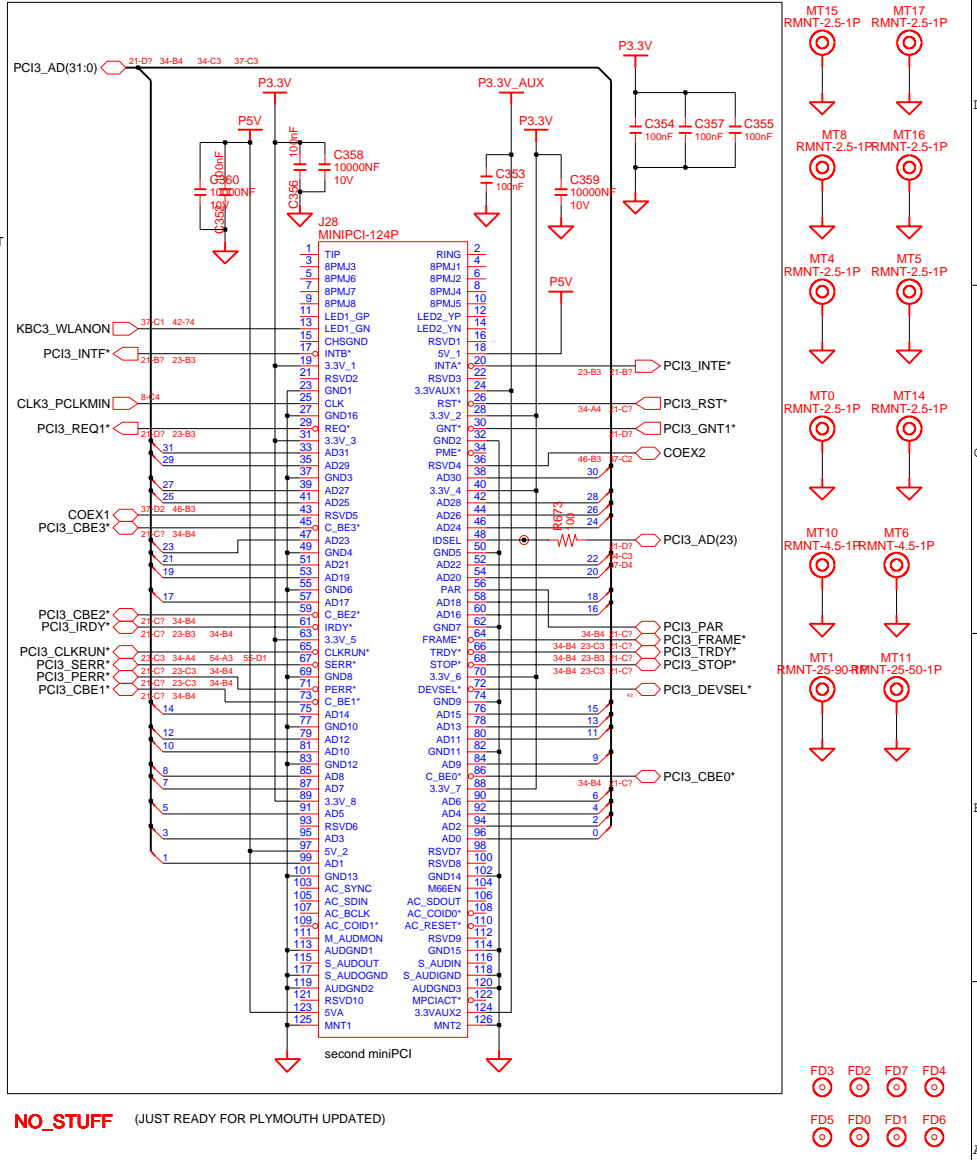
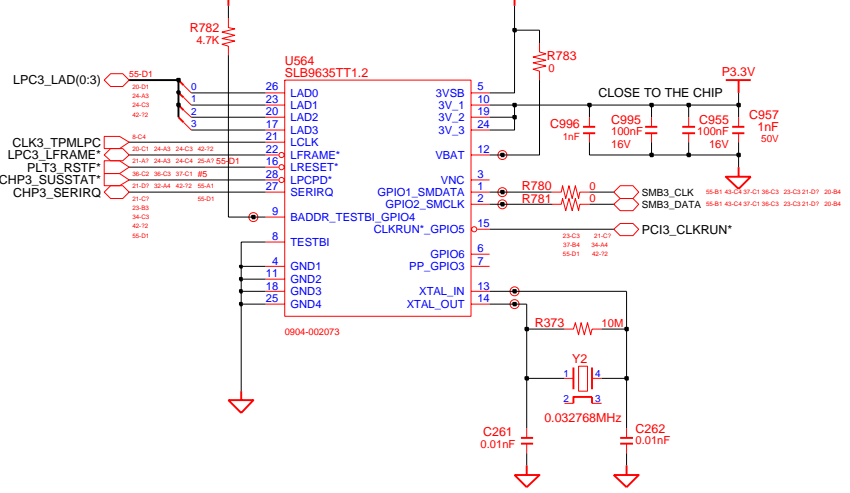
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### HDD PARKING



PLACE THESE ITEMS AS CLOSE AS POSSIBLE

### TPM 1.2

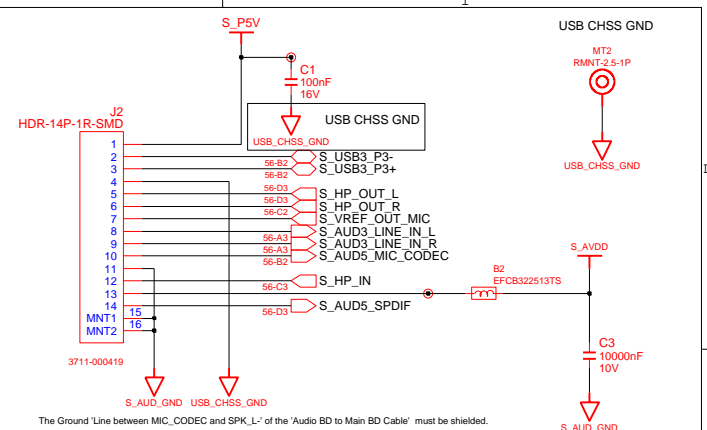
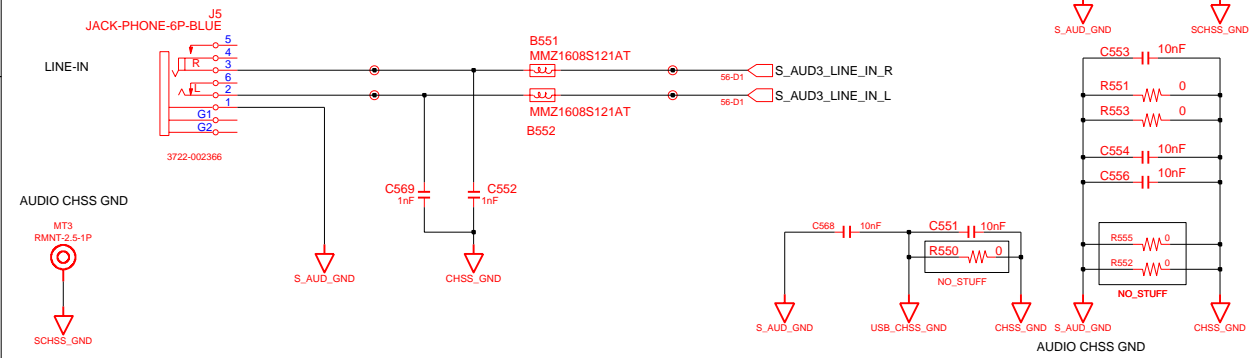
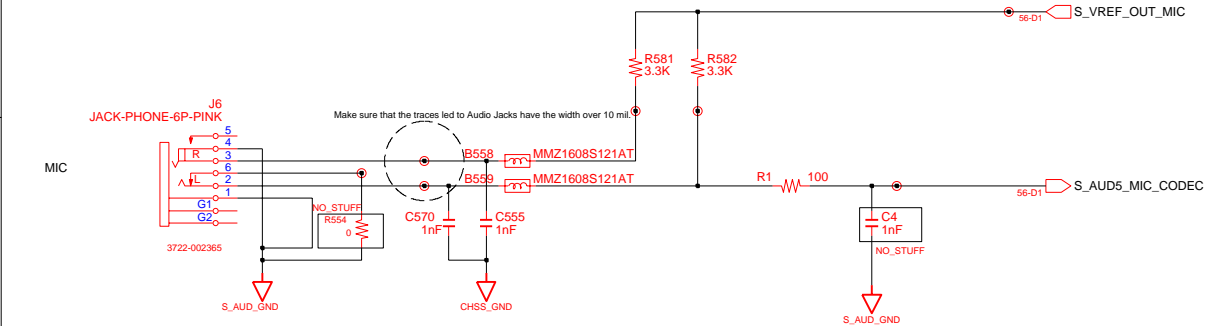
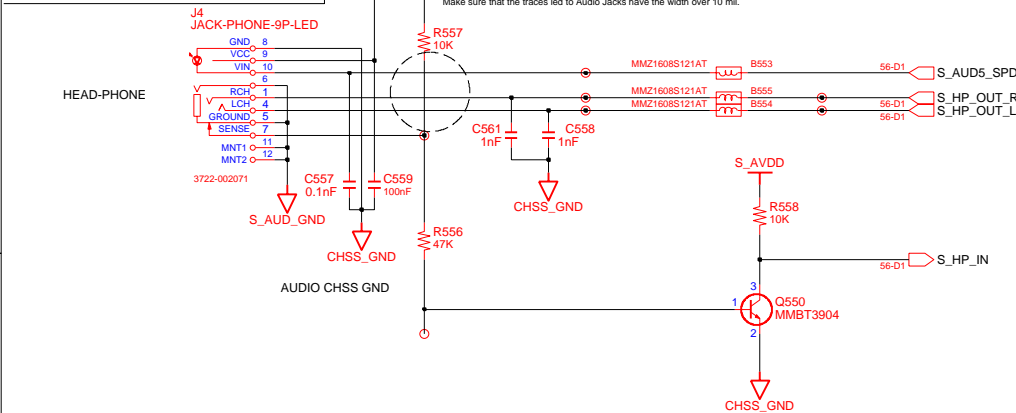


DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 MAINBD	SAMSUNG ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	REV	1.3	
APPROVAL	KEVIN LEE	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	53 OF 56	PART NO. BA41-00645A





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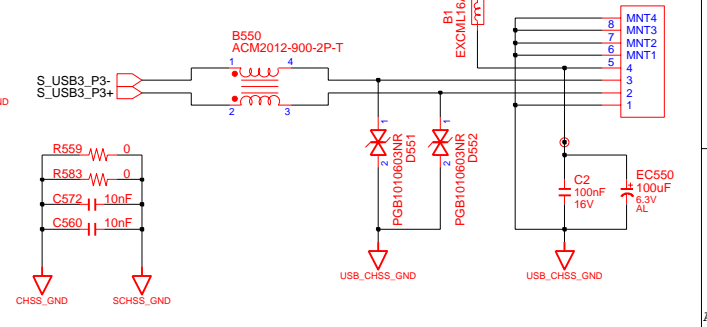


PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV550  
 1 O  
 2 O O3

**USB0 Connector**



DRAW	SUN LIANG	DATE	2/27/2006	TITLE	CICHLID 3 POWER	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHI JIANG	DEV. STEP	PR	REV	1.3	
APPROVAL	KEVIN LEE	LAST EDIT	February 27, 2006 3:31:27 PM	PAGE	55 OF 56	PART NO. BA41-00645A
MODULE CODE	undefined					

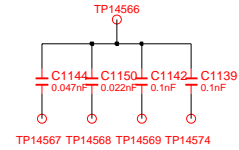


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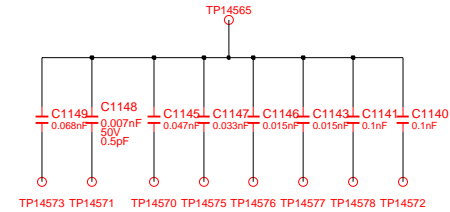
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TP1441 OAGND_VGA	TP1339 OP1_8V	TP1252 OVCC_CORE
TP1442 OAGND_VGA	TP1340 OP1_8V	TP1253 OVCC_CORE
TP1443 OAMP_VDD	TP1341 OP1_8V	TP1254 OVCC_CORE
TP1447 OAVDD	TP1342 OP1_8V	TP1255 OVDC
TP1448 OAVDD	TP1343 OP1_8V_AUX	TP1256 OVDC
TP1449 OAVDD	TP1344 OP1_8V_AUX	TP1257 OVDC
TP1386 OAVDD	TP1345 OP1_8V_AUX	TP1258 OV_ADAP
TP1387 OBATT_DC	TP1346 OP1_8V_AUX	TP1259 OV_ADAP
TP1388 OBATT_DC	TP1347 OP12V_ALWS	TP1260 OV_ADAP
TP1389 OBATT_DC	TP1348 OP12V_ALWS	TP1261 OV_ADAP
TP1390 OBATT_DC	TP1349 OP12V_ALWS	TP1450 OGROUND
TP1402 OCBS3_VCCA	TP1350 OP12V_ALWS	TP1451 OGROUND
TP1405 OCBS3_VPPA	TP1351 OP2_5V	TP1452 O_7VDDQA
TP1406 OCBS3_VPPA	TP1352 OP2_5V	TP1454 OAGND
TP1409 OCHG_REF	TP1353 OP2_5V	TP1455 OAGND_AUD
TP1410 OCHG_REF	TP1294 OP2_5V	TP1456 OAGND_CHG
TP1411 OCHSS_GND	TP1295 OP2_5V_LAN	TP1459 OAGND_P3_3V
TP1412 OCHSS_GND	TP1296 OP2_5V_LAN	TP1461 OCAMP_VDD
TP1413 OCHSS_GND	TP1297 OP2_5V_LAN	TP1462 OAVDD
TP1414 OCHSS_GND	TP1298 OP2_5V_LAN	TP1463 OBATT_DC
TP1415 OGF_X_CORE	TP1299 OP3_3V	TP1464 OCBS3_MD_VCC
TP1416 OGF_X_CORE	TP1300 OP3_3V	TP1465 OCBS3_VCCA
TP1417 OGF_X_CORE	TP1301 OP3_3V	TP1468 OCHSS_GND
TP1354 OGF_X_CORE	TP1302 OP3_3V	TP1469 OGF_X_CORE
TP1355 OGROUND	TP1303 OP3_3V_AUX	TP1470 OGROUND
TP1356 OGROUND	TP1304 OP3_3V_AUX	TP1471 OGROUND
TP1357 OGROUND	TP1305 OP3_3V_AUX	TP1475 OMICOM_P3V
TP1358 OGROUND	TP1306 OP3_3V_AUX	TP1476 OP0_9V
TP1360 OINV_VDC	TP1307 OP3_3V_AUX_EXP	TP1477 OP1_2V
TP1361 OINV_VDC	TP1308 OP3_3V_AUX_EXP	TP1478 OP1_2V_LAN
TP1362 OINV_VDC	TP1309 OP3_3V_AUX_EXP	TP1479 OP1_5V
TP1363 OLCD_VDD3V	TP1310 OP3_3V_AUX_EXP	TP1480 OP1_5V_EXP
TP1364 OLCD_VDD3V	TP1311 OP3_3V_EXP	TP1481 OP1_5V_PCIE
TP1365 OLCD_VDD3V	TP1312 OP3_3V_EXP	TP1482 OP1_8V
TP1366 OLCD_VDD3V	TP1313 OP3_3V_EXP	TP1483 OP1_8V_AUX
TP1367 OLDO_P5_4V	TP1314 OP3_3V_EXP	TP1484 OP12V_ALWS
TP1368 OLDO_P5_4V	TP1315 OP3_3V_LAN	TP1485 OP2_5V
TP1369 OLDO_P5_4V	TP1316 OP3_3V_LAN	TP1486 OP2_5V_LAN
TP1370 OLDO_P5_4V	TP1317 OP3_3V_LAN	TP1487 OP3_3V
TP1371 OMICOM_P3V	TP1318 OP3_3V_LAN	TP1488 OP3_3V_AUX
TP1372 OMICOM_P3V	TP1319 OP5V	TP1491 OP3_3V_LAN
TP1373 OMICOM_P3V	TP1320 OP5V	TP1492 OP5V
TP1374 OMICOM_P3V	TP1321 OP5V	TP1494 OP5V_AUX
TP1375 OP0_9V	TP1322 OP5V	TP1495 OPRTC_BAT
TP1376 OP0_9V	TP1323 OP5V_ALWS	TP1496 OSCHSS_GND
TP1377 OP0_9V	TP1324 OP5V_ALWS	TP1497 OSC_AUD_GND
TP1378 OP0_9V	TP1325 OP5V_ALWS	TP1498 OSC_AVDD
TP1379 OP1_2V	TP1326 OP5V_ALWS	TP1499 OTMDS_PLLVDD
TP1380 OP1_2V	TP1327 OP5V_ALWS	TP1500 OUSB_CHSS_GND
TP1381 OP1_2V	TP1328 OP5V_AUX	TP1501 OVCCP
TP1382 OP1_2V	TP1329 OP5V_AUX	TP1502 OVCC_CORE
TP1383 OP1_2V_LAN	TP1264 OP5V_AUX	TP1503 OVDC
TP1384 OP1_2V_LAN	TP1265 OP5V_AUX	TP1266 OTMDS_PLLVDD
TP1385 OP1_2V_LAN	TP1266 OP5V_AUX	TP1267 OTMDS_PLLVDD
TP1326 OP1_2V_LAN	TP1267 OPRTC_BAT	TP1268 OPRTC_BAT
TP1327 OP1_5V	TP1268 OPRTC_BAT	TP1269 OPRTC_BAT
TP1328 OP1_5V	TP1270 OPRTC_BAT	TP1289 OUSB_CHSS_GND
TP1329 OP1_5V	TP1271 OSCHSS_GND	TP1290 OUSB_CHSS_GND
TP1330 OP1_5V	TP1272 OSCHSS_GND	TP1291 OVCCP
TP1331 OP1_5V_EXP	TP1273 OSCHSS_GND	TP1292 OVCCP
TP1332 OP1_5V_EXP	TP1274 OSCHSS_GND	TP1293 OVCCP
TP1333 OP1_5V_EXP	TP1275 OSC_AUD_GND	TP1249 OVCCP
TP1334 OP1_5V_EXP	TP1276 OSC_AUD_GND	TP1250 OVCC_CORE
TP1335 OP1_5V_PCIE	TP1277 OSC_AUD_GND	TP1251 OVCC_CORE
TP1336 OP1_5V_PCIE	TP1281 OSC_AVDD	TP1282 OS_AVDD
TP1337 OP1_5V_PCIE	TP1282 OS_AVDD	TP14561 OVCC_CRT
TP1338 OP1_5V_PCIE	TP1283 OTMDS_PLLVDD	TP14564 OVCC_CRT
	TP1284 OTMDS_PLLVDD	TP14579 OV_ADAP
	TP1285 OTMDS_PLLVDD	TP14580 OV_ADAP

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