

Wistron Confidential

MV-1

2008/05/23

REV : -1

Datasheet Directory

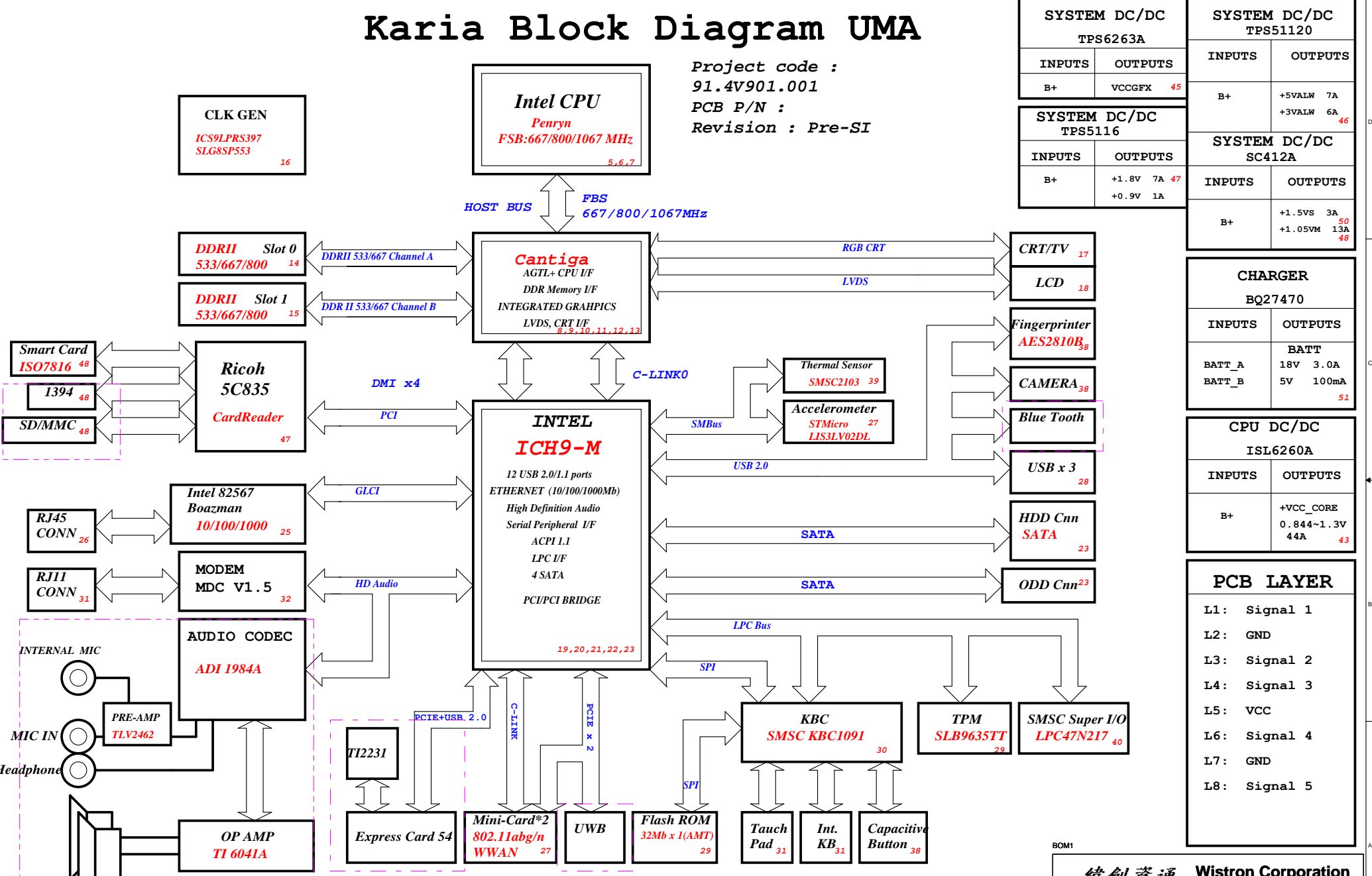
BOM1

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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Karia			
Size	Document Number	Rev	
A3	Karia	SF	
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Karia Block Diagram UMA

Project code :
91.4V901.001
PCB P/N :
Revision : Pre-SI



SYSTEM DC/DC TPS6263A		SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
B+	VCCGFX 45	B+	+5VALW 7A +3VALW 6A 46
SYSTEM DC/DC TPS5116		SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
B+	+1.8V 7A 47 +0.9V 1A	B+	+1.5VS 3A 50 +1.05VM 13A 48

CHARGER BQ27470	
INPUTS	OUTPUTS
BATT_A	BATT
BATT_B	1.8V 3.0A 5V 100mA 51

CPU DC/DC ISL6260A	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 44A 43

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5



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1. Page 43 - Change R542.2 to +3VALM from +3VS to power U86.39 (3V3) 0303 OK
2. Page 45 - Change R480 to NO INSTALL 0303 OK
3. Page 30 - Remove D48, connect signal directly to ADP_PRES, and uninstall R506 0303 OK
4. Page 51 - Chage R15 to 22K from 10K NOT DONE ON 0303 0312 OK

3/13

1. Page 27 - Add a 0 ohm series resistor on MC1_DISALBE and MC2_DISALBE RL: Don't need to add; use the 0 ohm at KBC.
2. Page 27 - Reserve a 1u 0603 cap (NO INSTALL) on MC2_DISALBE (same as MC1_DISABLE) 0312 OK
3. Page 19 - Add a 0 ohm series on PLT_RST# at U106.4 RL: Change R185 to 0 ohm; May need to change for damping.
4. Page 33 - Add a 0 ohm series on PM_PWROK_R at R166.2 RL: Pad is ok but needs to be on PM_PWROK_R from U89.40 (It's ok to put it near R541.2 on page43)
7. Page 30 - Change R598 to INSTALL (KBC GPIO08 has no internal PU) 0312 OK
8. Page 39 - Change R78 (SHDN_SEL) to 22K 1% to use External Diode2 for H/W critical shutdown 0312 OK
10. Page 24 - OPEN: May need to change U84 to Paricom level shifter. RL: Investigating
11. Page 25 - May require a discharging FET for +3VM_LAN at Q37.D RL: Change R104 to 470 ohm and change Q55.G to LAN_PY1
12. Page 32 - OPEN: May need to change RGB q-switches power to +5VALW or +5VS (depending on wavy impact) RL: Investigating
13. Page 51 - Change R101 to 33k from 1.27K 0312 OK
14. Page 41 - Change DAUGHT1 pin 52 and pin 54 to +5VS from +5VALW 0312 OK
15. Page 41 - Remove TCH_SMB_CLK/DATA from DAUGHT1 pin 32 and 34 0312 OK

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Change Notes List			
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Voltage Rails o MEANS ON x MEANS OFF

State \ power plane	+BB LDO3 LDO5	+5VALW +5VALW	+1.8V +5V +0.9V	+5VS +3VS +1.8VS +1.5VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader&l394	AD25	2	G, E

PCIe Devices

DEVICE	NUMBER	CHANNEL
WWLAN	1	4
WLAN	1	2
UWB	1	1
Express Card	1	3

USB PORT	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FingerPrint
9	Dock1
10	WEBCAM
11	DOCK2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything
1U16V2ZY-2GP	Caps 1U ,Size 0402 Y5V
2D2U6D3V3MX	Caps 2.2U ,Size 0603 X5R

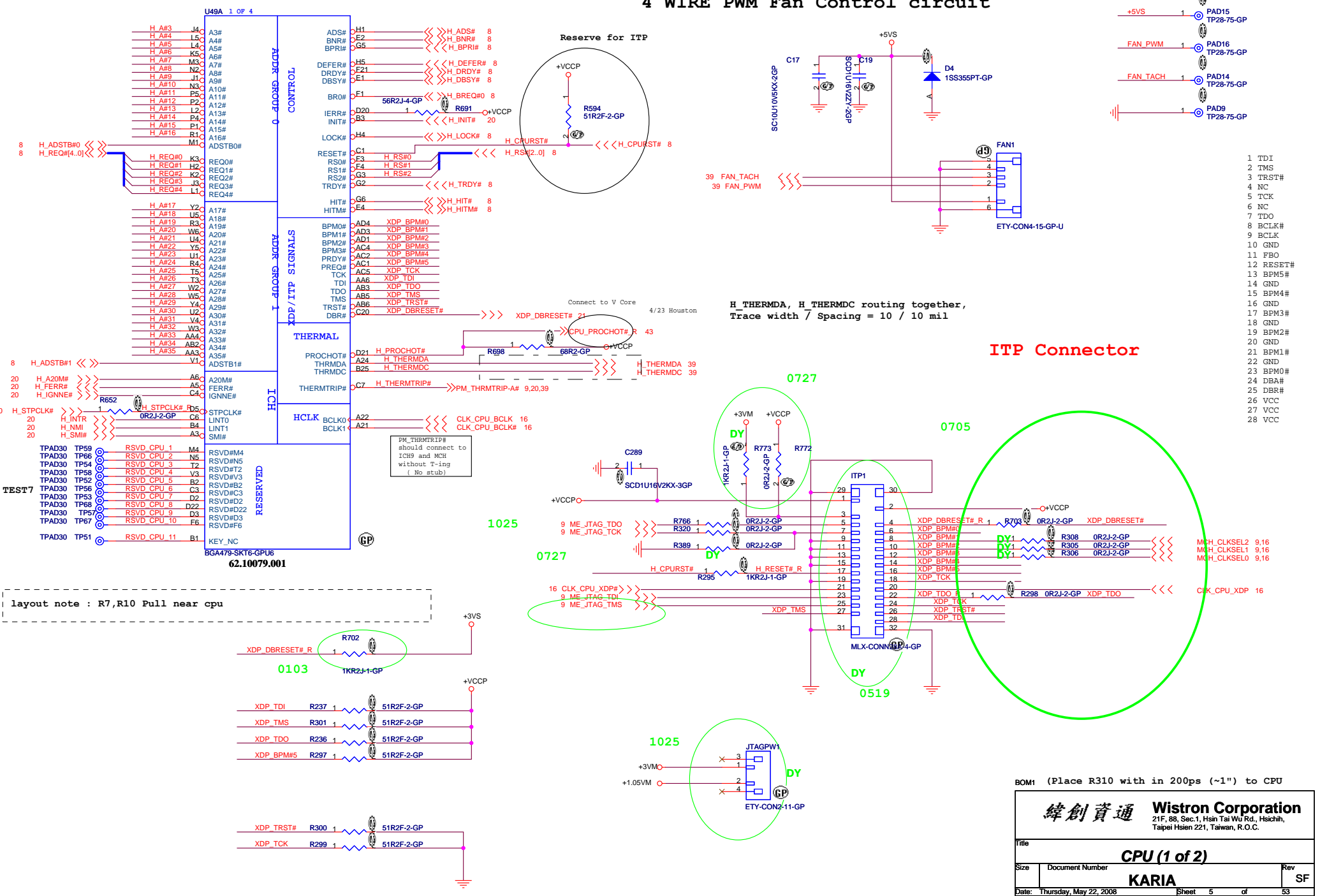
Fingerprint

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH9 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH9 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH9 Family) USB Universal Host Control
18	Intel 82801H (ICH9 Family) USB Universal Host Control Richo R5C835 Integrates FlashMedia Control Richo R5C835 Gemcore based SmartCard Control
19	Intel 82801H (ICH9 Family) PCI Express Root Port -27D6 Intel 82801H (ICH9 Family) USB Universal Host Control
20	Intel 82801H (ICH9 Family) USB Universal Host Control Intel 82801H (ICH9 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH9 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

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Karia List		
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4 WIRE PWM Fan Control circuit



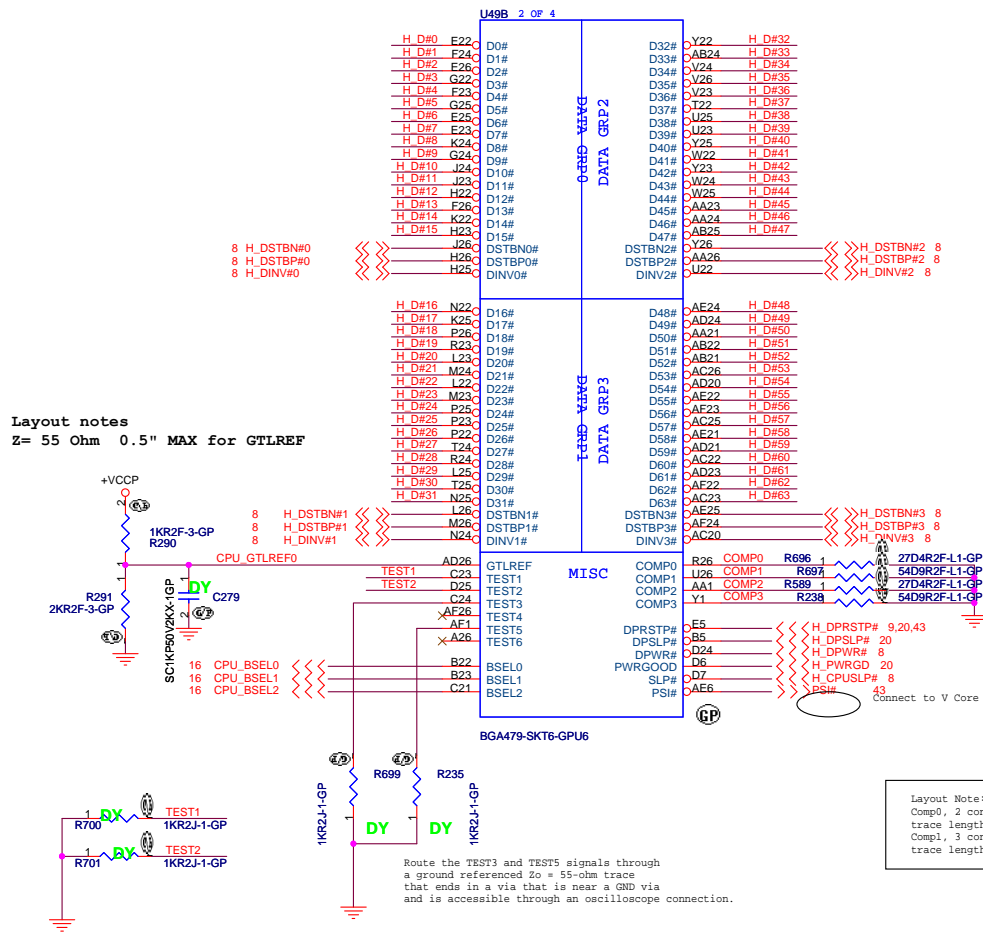
layout note : R7,R10 Pull near cpu

ITP Connector

BOM1 (Place R310 with in 200ps (~1") to CPU

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H_DINV#[3..0] <<>>H_DINV#[3..0] 8
 H_DSTBN#[3..0] <<>>H_DSTBN#[3..0] 8
 H_DSTBP#[3..0] <<>>H_DSTBP#[3..0] 8
 H_D#[63..0] <<>>H_D#[63..0] 8



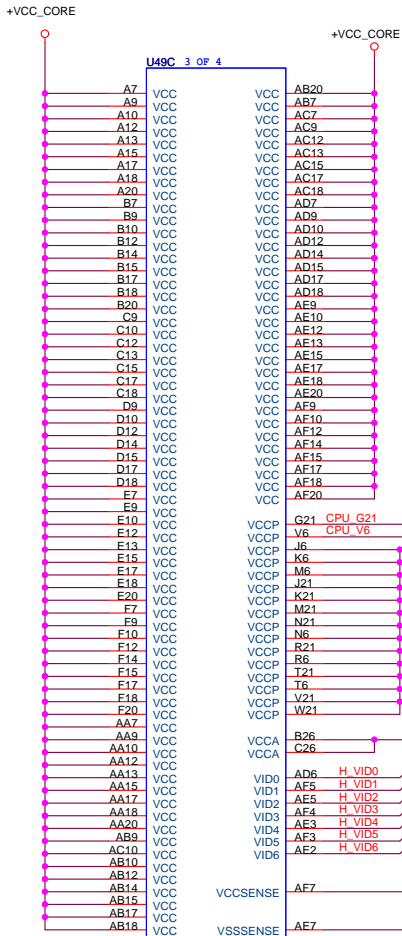
Layout notes
 Z= 55 Ohm 0.5" MAX for GTLREF

Layout Note:
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

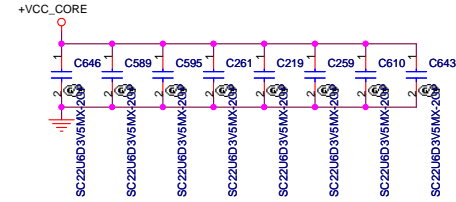
Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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Title CPU (3 of 2)	
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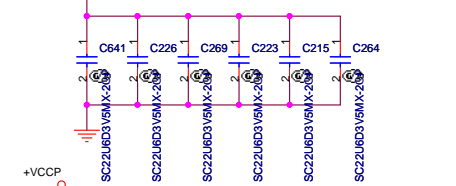
Please these inside socket cavity on L8(North side Secondary)



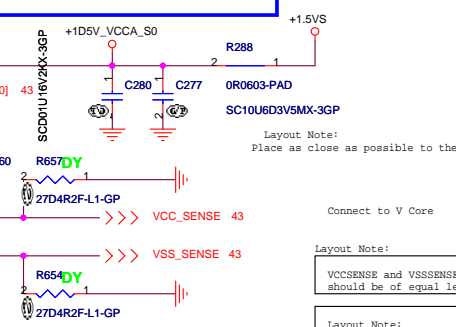
Please these inside socket cavity on L8(South side Secondary)



Please these inside socket cavity on L8(North side Primary)



layout note: "1D5V VCCA_S0" as short as possible



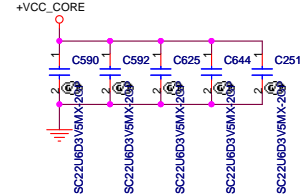
Layout Note: Place as close as possible to the CPU VCCA pin.

Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

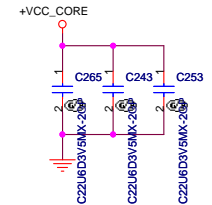
Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Please these inside socket cavity on L8(North side Secondary)

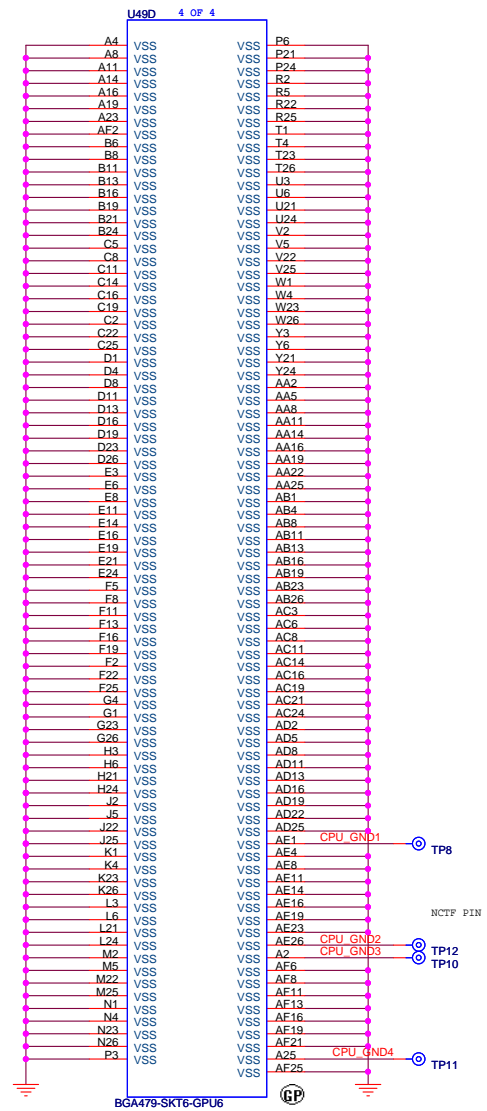
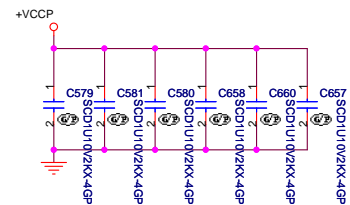
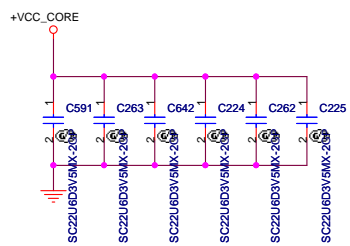
Please these outside socket cavity on L8(North side Secondary)



Please these outside socket cavity on L8(South side Secondary)

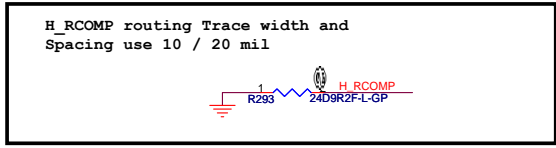
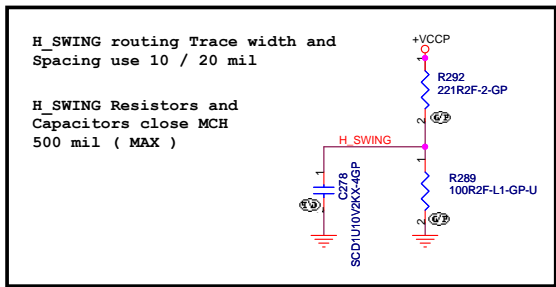


Please these inside socket cavity on L8(South side Primary)

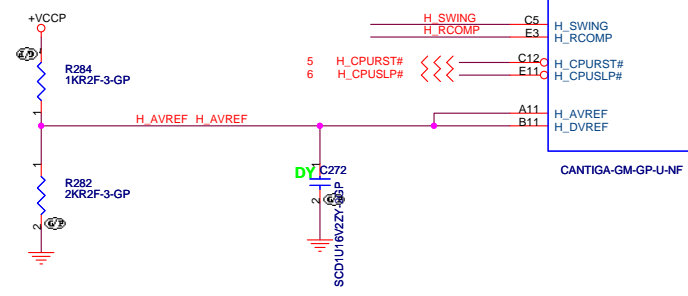


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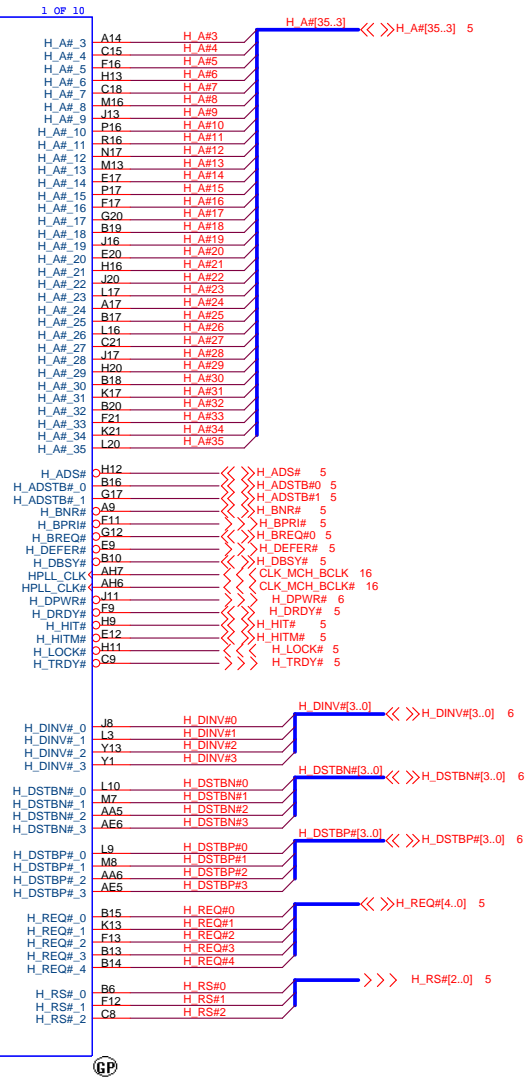


Place them near to the chip (< 0.5")



U51A		1 OF 10	
H_D#0	F2	H_D#_0	H_A#_3
H_D#1	G3	H_D#_1	H_A#_4
H_D#2	F8	H_D#_2	H_A#_5
H_D#3	E6	H_D#_3	H_A#_6
H_D#4	G2	H_D#_4	H_A#_7
H_D#5	H6	H_D#_5	H_A#_8
H_D#6	H2	H_D#_6	H_A#_9
H_D#7	F6	H_D#_7	H_A#_10
H_D#8	D4	H_D#_8	H_A#_11
H_D#9	H3	H_D#_9	H_A#_12
H_D#10	M1	H_D#_10	H_A#_13
H_D#11	M9	H_D#_11	H_A#_14
H_D#12	J1	H_D#_12	H_A#_15
H_D#13	J2	H_D#_13	H_A#_16
H_D#14	N12	H_D#_14	H_A#_17
H_D#15	J6	H_D#_15	H_A#_18
H_D#16	L2	H_D#_16	H_A#_19
H_D#17	R2	H_D#_17	H_A#_20
H_D#18	N9	H_D#_18	H_A#_21
H_D#19	M5	H_D#_19	H_A#_22
H_D#20	J3	H_D#_20	H_A#_23
H_D#21	N2	H_D#_21	H_A#_24
H_D#22	R1	H_D#_22	H_A#_25
H_D#23	N5	H_D#_23	H_A#_26
H_D#24	N6	H_D#_24	H_A#_27
H_D#25	P13	H_D#_25	H_A#_28
H_D#26	N8	H_D#_26	H_A#_29
H_D#27	L7	H_D#_27	H_A#_30
H_D#28	N10	H_D#_28	H_A#_31
H_D#29	M3	H_D#_29	H_A#_32
H_D#30	Y3	H_D#_30	H_A#_33
H_D#31	AD14	H_D#_31	H_A#_34
H_D#32	Y6	H_D#_32	H_A#_35
H_D#33	Y10	H_D#_33	H_A#_36
H_D#34	Y12	H_D#_34	H_A#_37
H_D#35	Y14	H_D#_35	H_A#_38
H_D#36	W2	H_D#_36	H_A#_39
H_D#37	W9	H_D#_37	H_A#_40
H_D#38	AA8	H_D#_38	H_A#_41
H_D#39	AA9	H_D#_39	H_A#_42
H_D#40	AA11	H_D#_40	H_A#_43
H_D#41	AD10	H_D#_41	H_A#_44
H_D#42	AD11	H_D#_42	H_A#_45
H_D#43	AD12	H_D#_43	H_A#_46
H_D#44	AE8	H_D#_44	H_A#_47
H_D#45	AE9	H_D#_45	H_A#_48
H_D#46	AE10	H_D#_46	H_A#_49
H_D#47	AE11	H_D#_47	H_A#_50
H_D#48	AE12	H_D#_48	H_A#_51
H_D#49	AE13	H_D#_49	H_A#_52
H_D#50	AE14	H_D#_50	H_A#_53
H_D#51	AE15	H_D#_51	H_A#_54
H_D#52	AE16	H_D#_52	H_A#_55
H_D#53	AE17	H_D#_53	H_A#_56
H_D#54	AE18	H_D#_54	H_A#_57
H_D#55	AE19	H_D#_55	H_A#_58
H_D#56	AG2	H_D#_56	H_A#_59
H_D#57	AD6	H_D#_57	H_A#_60
H_D#58		H_D#_58	H_A#_61
H_D#59		H_D#_59	H_A#_62
H_D#60		H_D#_60	H_A#_63
H_D#61		H_D#_61	
H_D#62		H_D#_62	
H_D#63		H_D#_63	

HOST



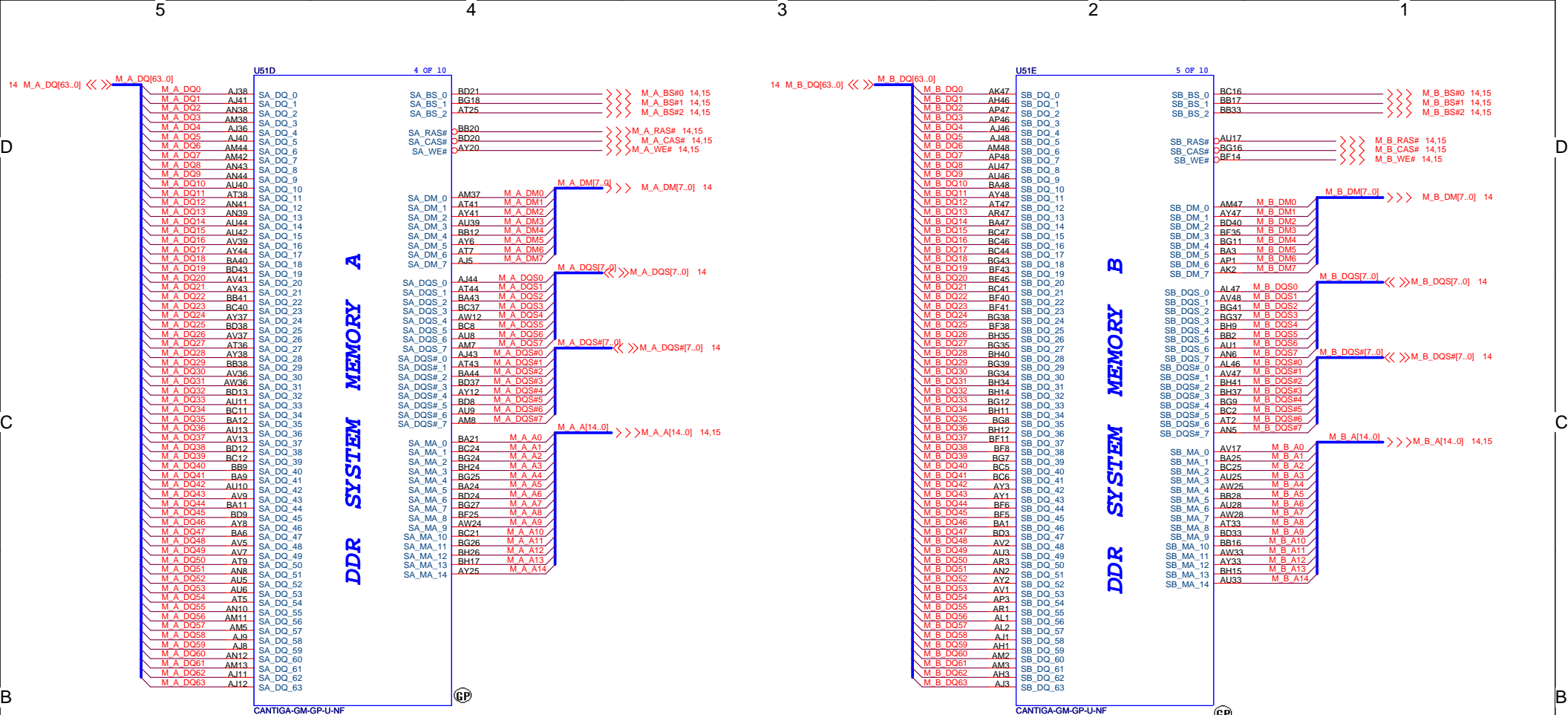
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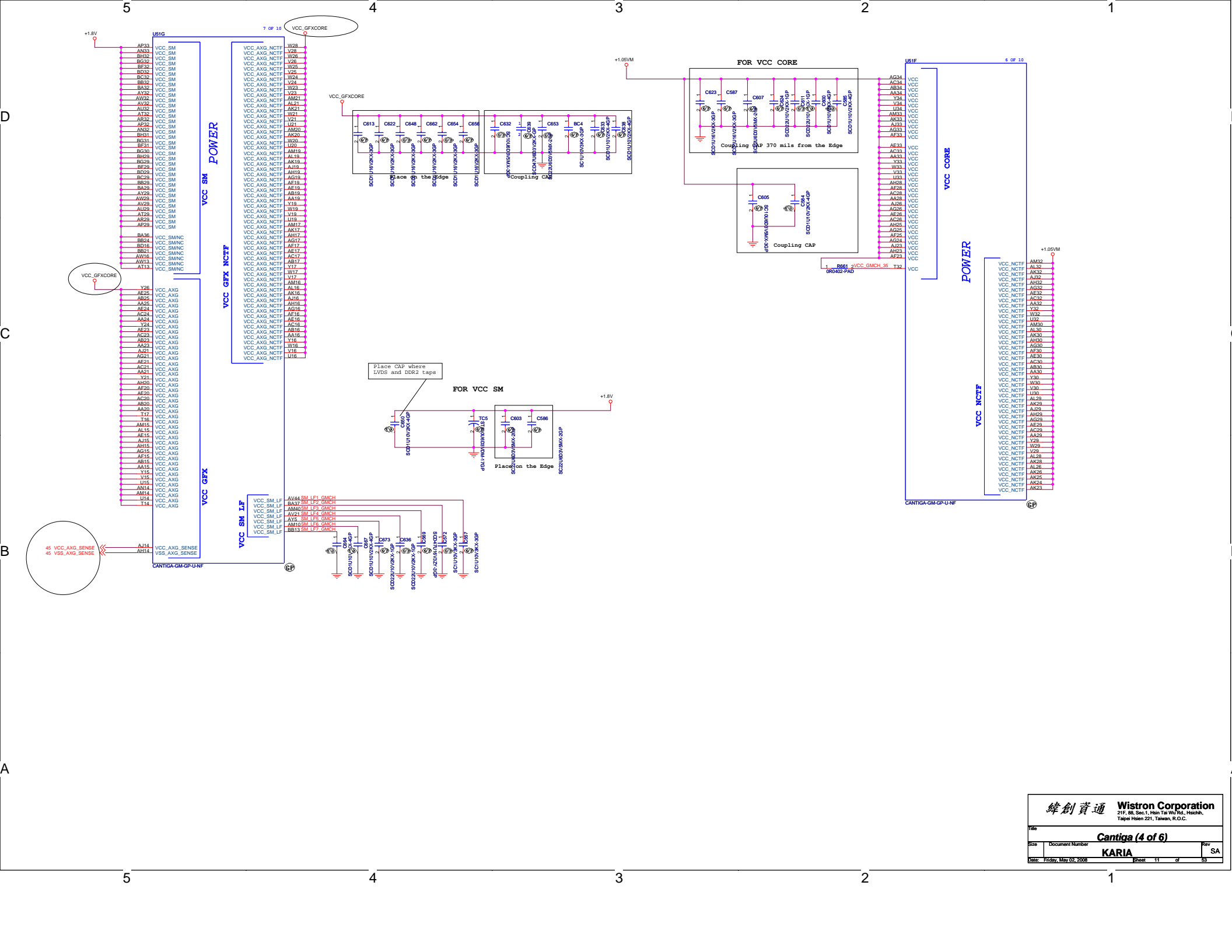
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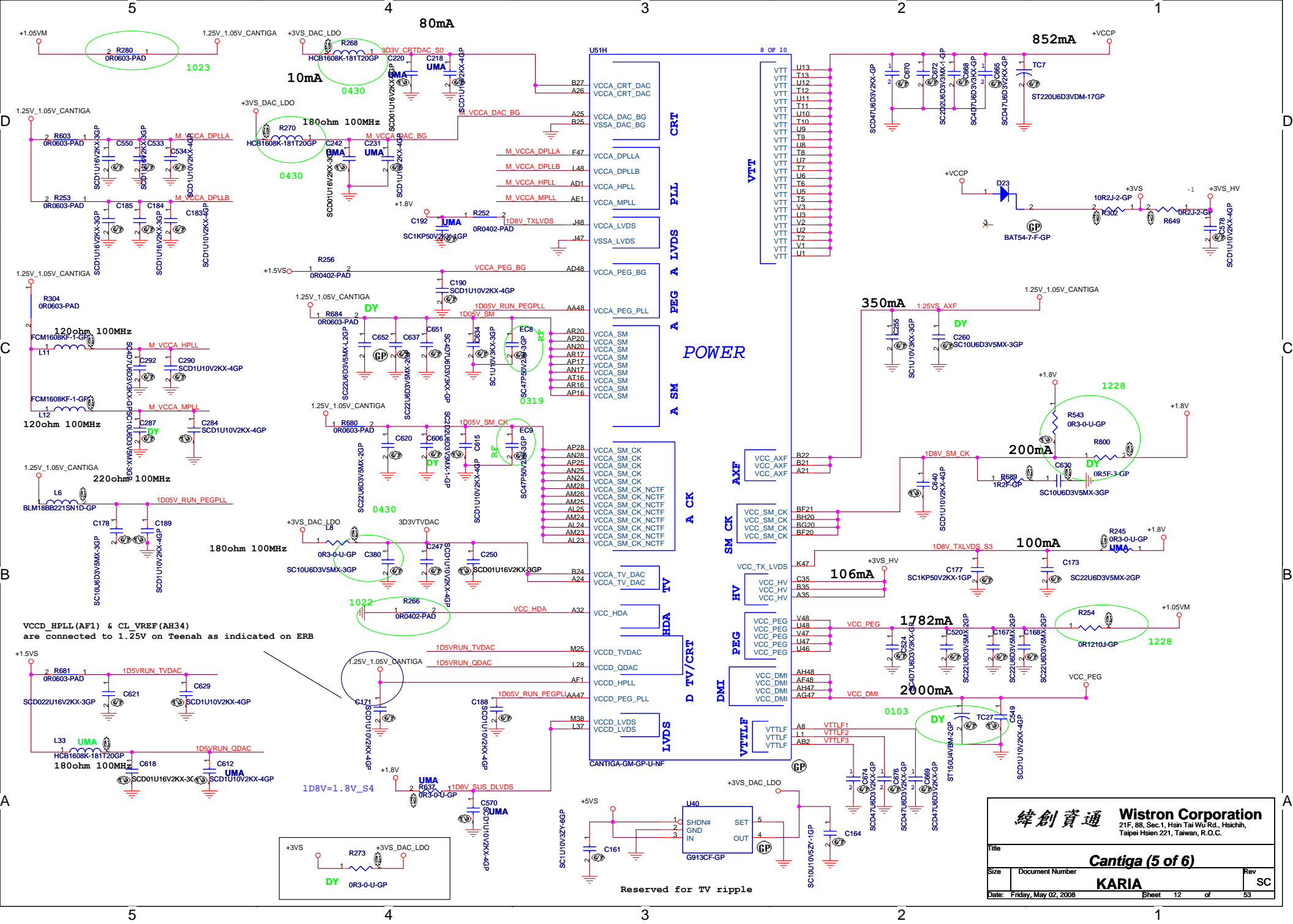
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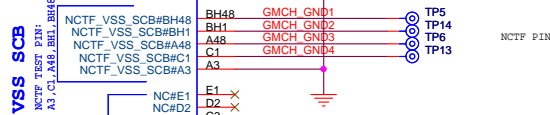
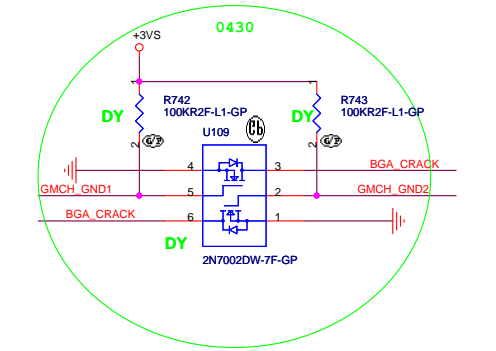
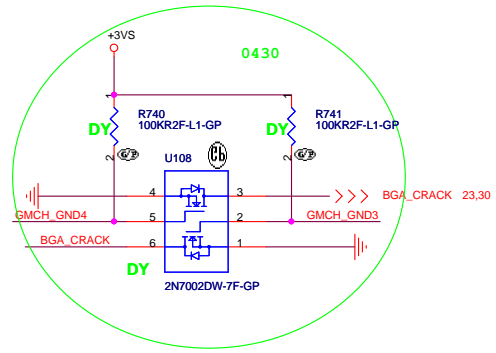
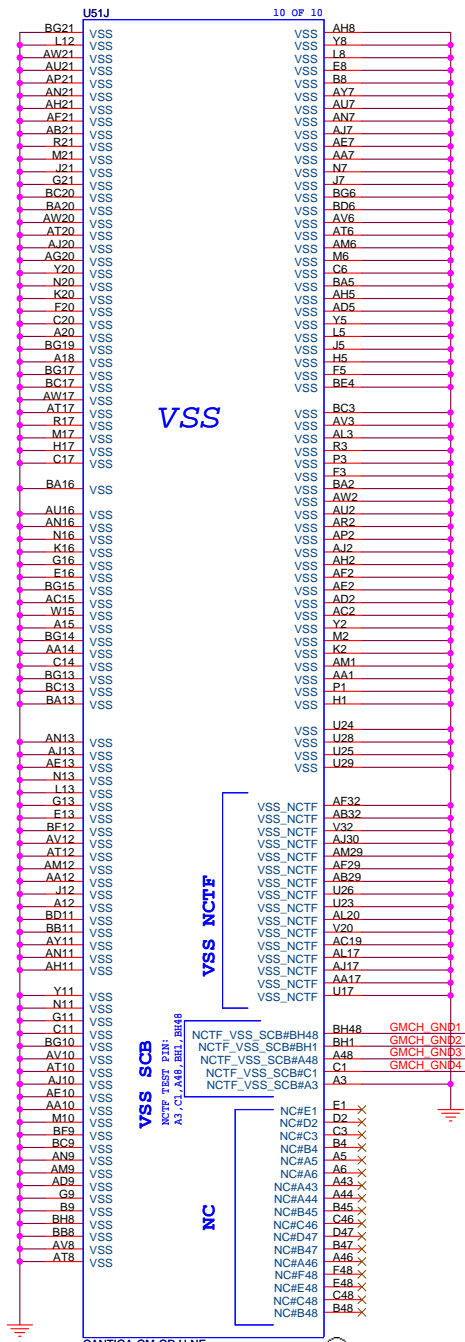
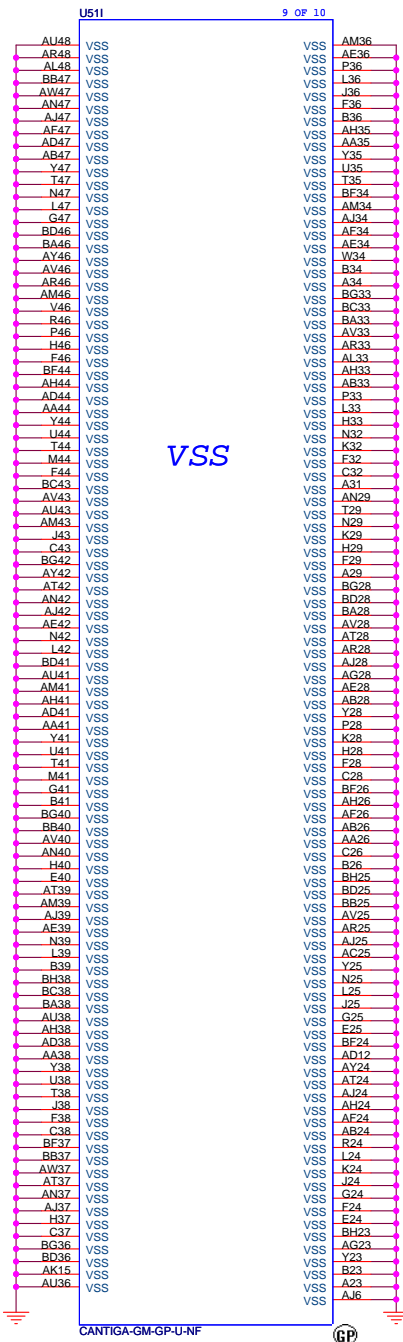


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Title			
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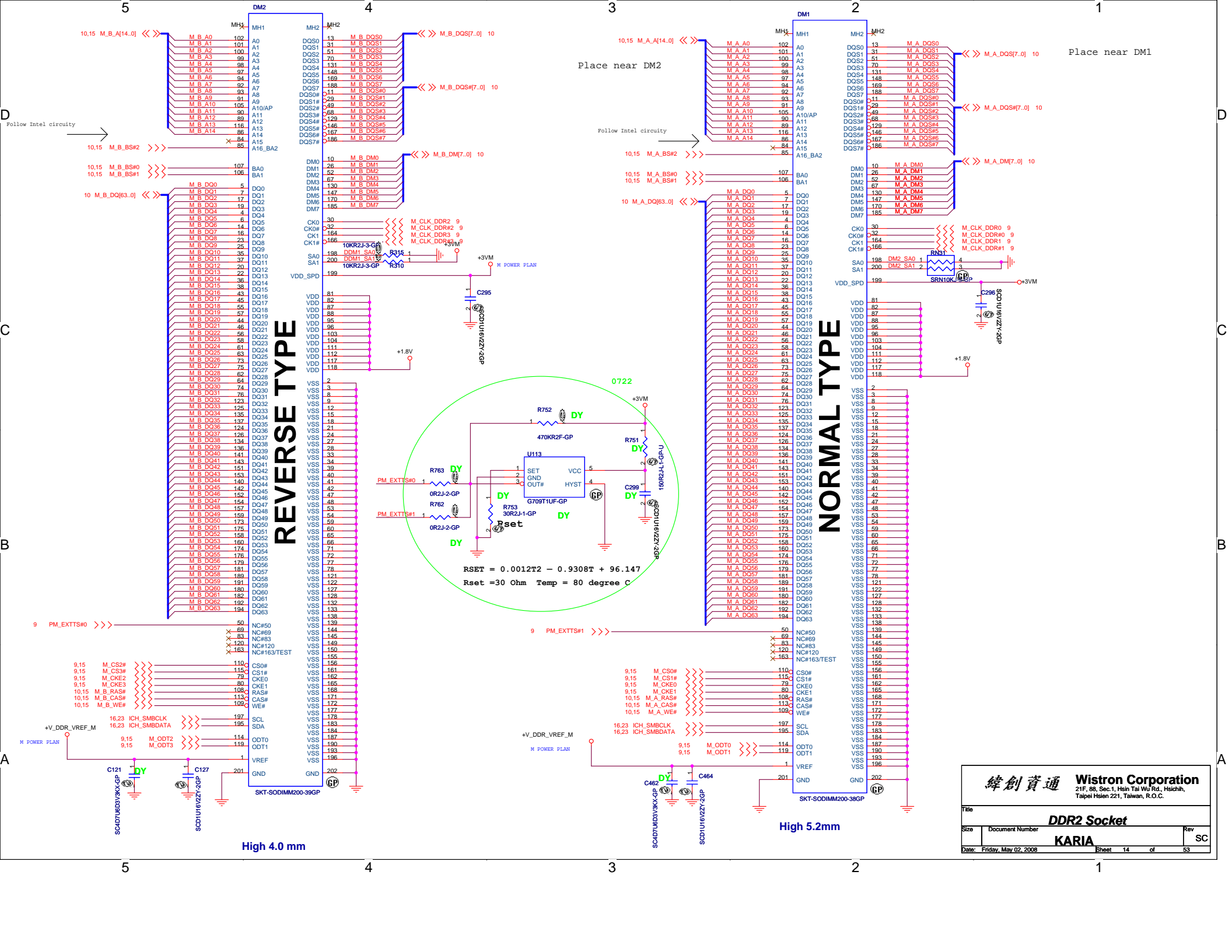


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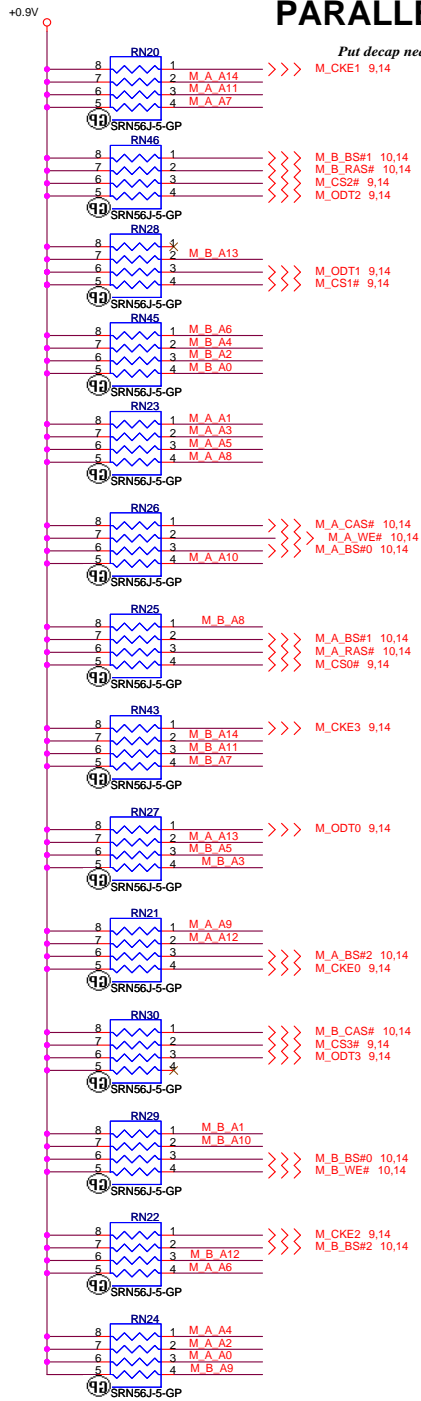
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File: **DDR2 Socket**

Size: Document Number: **KARIA** Rev: **SC**

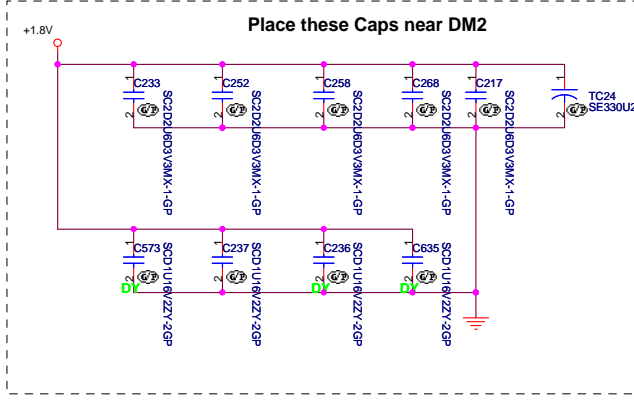
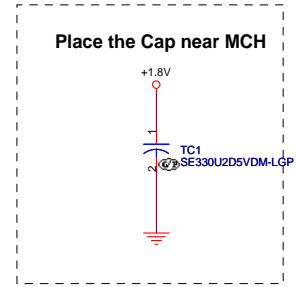
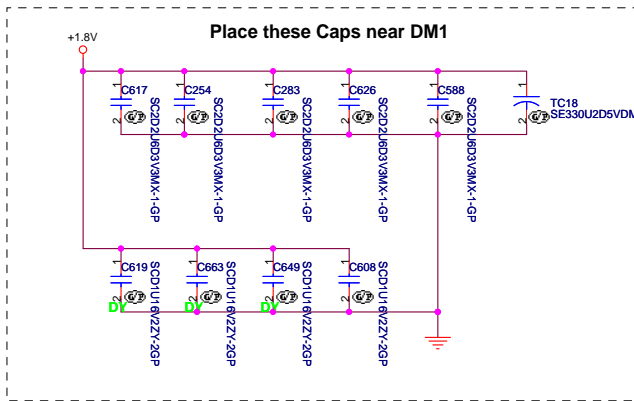
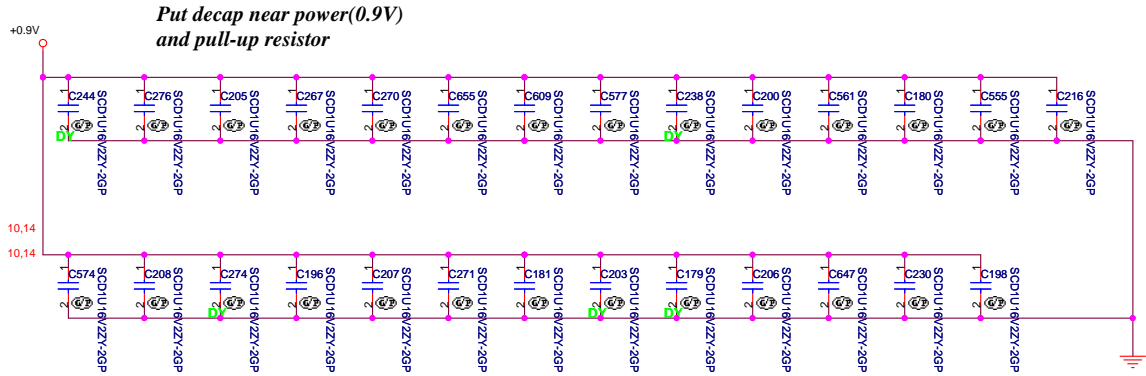
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PARALLEL TERMINATION

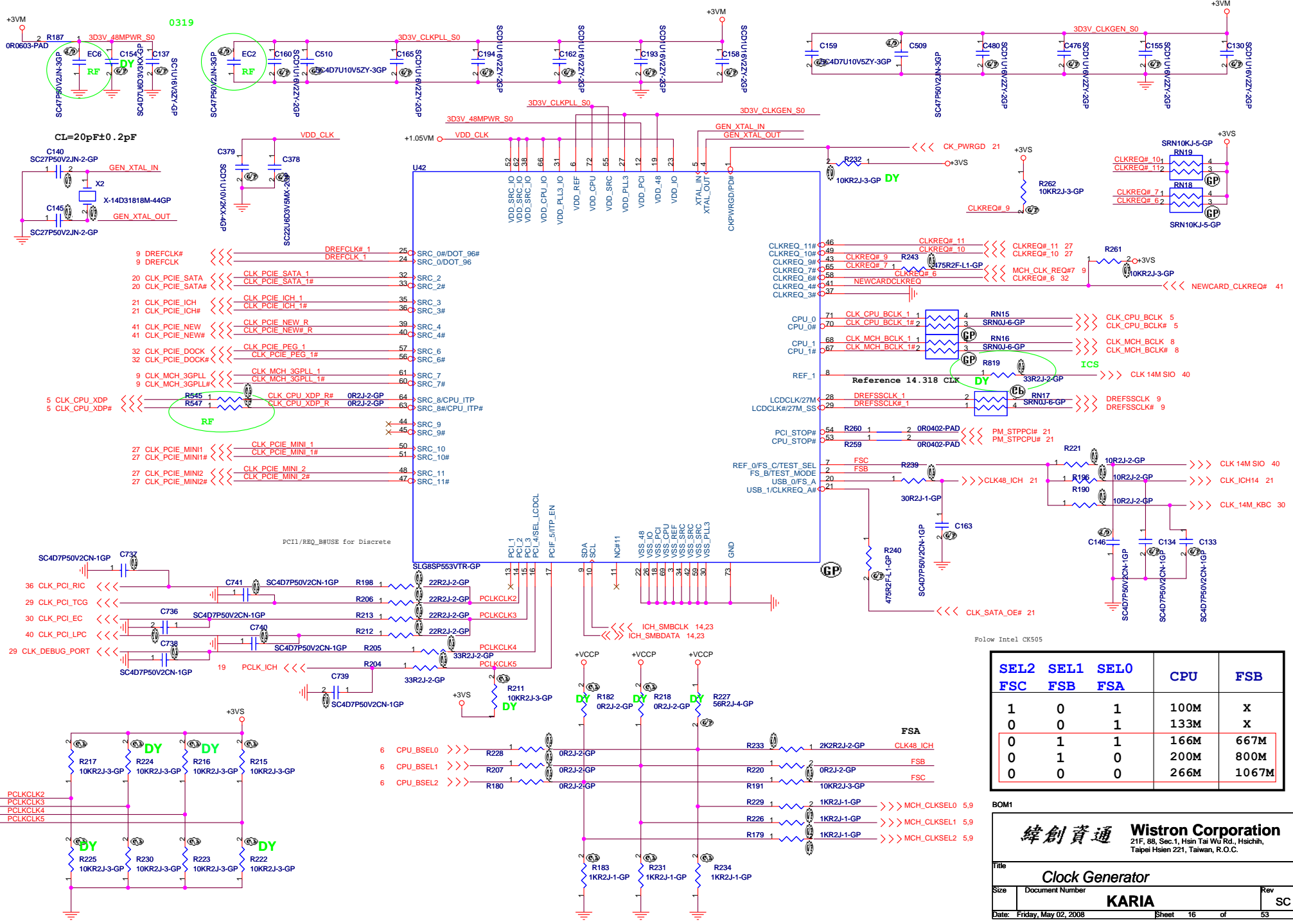


M.A. A[14..0] <<< M.A_A[14..0] 10,14
 M.B. A[14..0] <<< M.B_A[14..0] 10,14

Decoupling Capacitor



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File DDR2 Termination Resistor			
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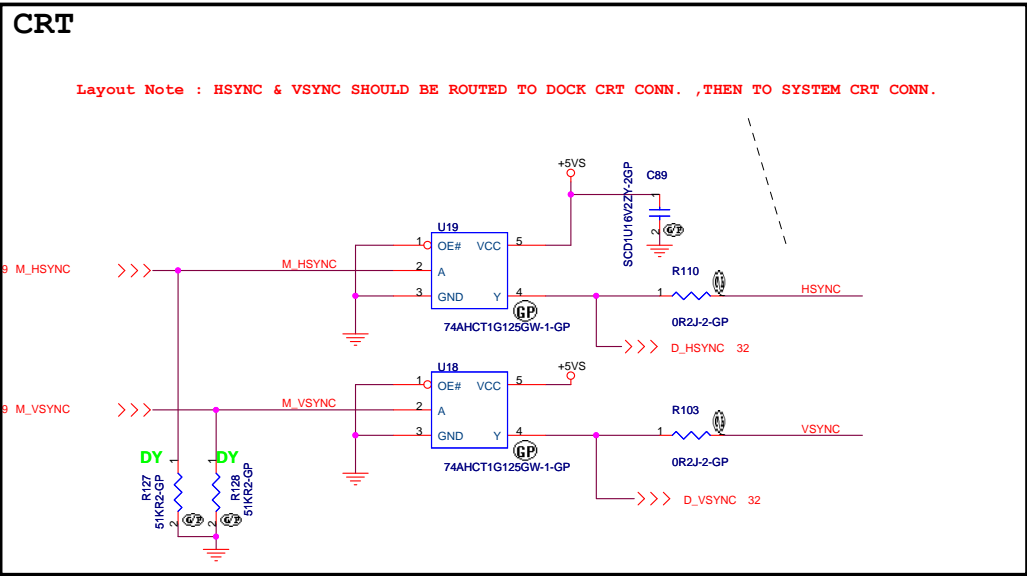
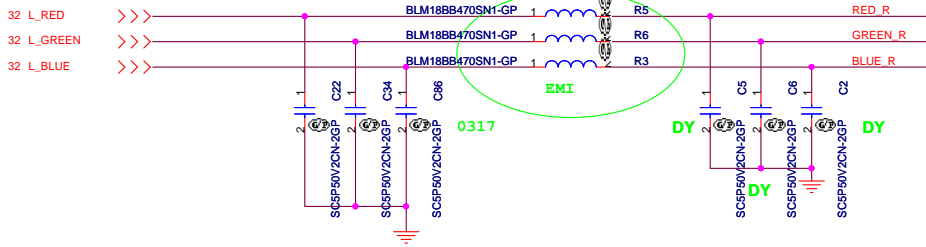


Follow Intel CK505

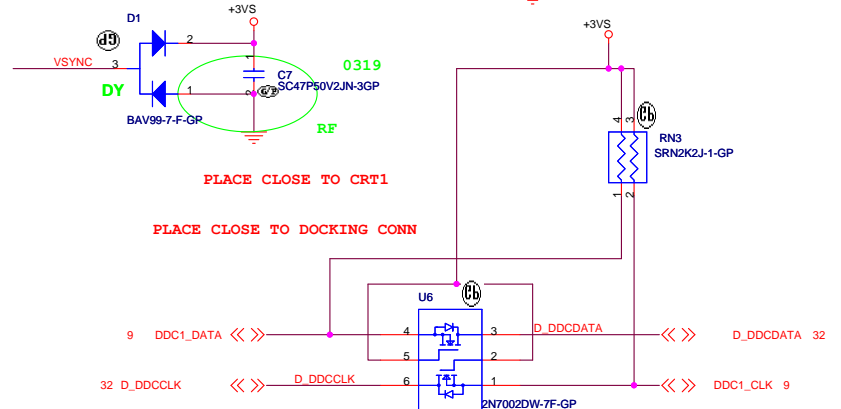
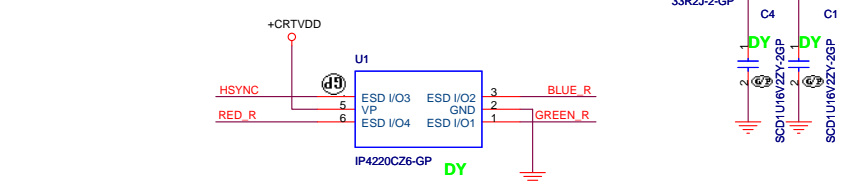
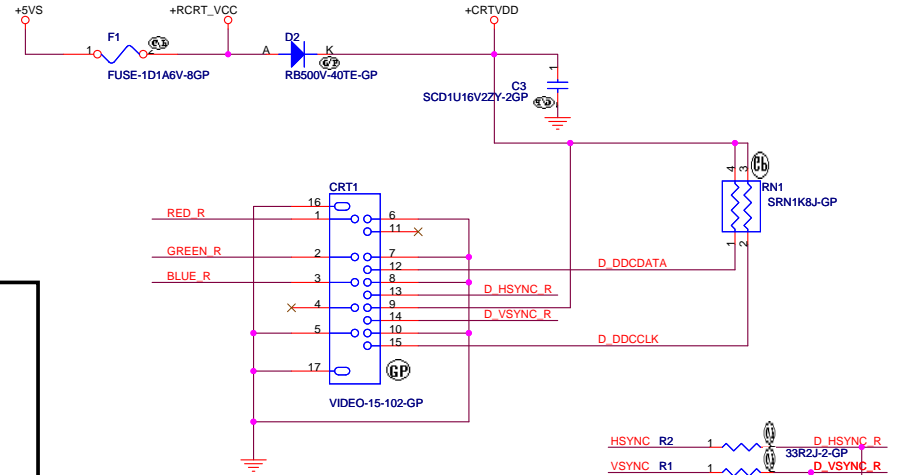
SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

BOM1

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.



DEL TV connector 1022



BOM1

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

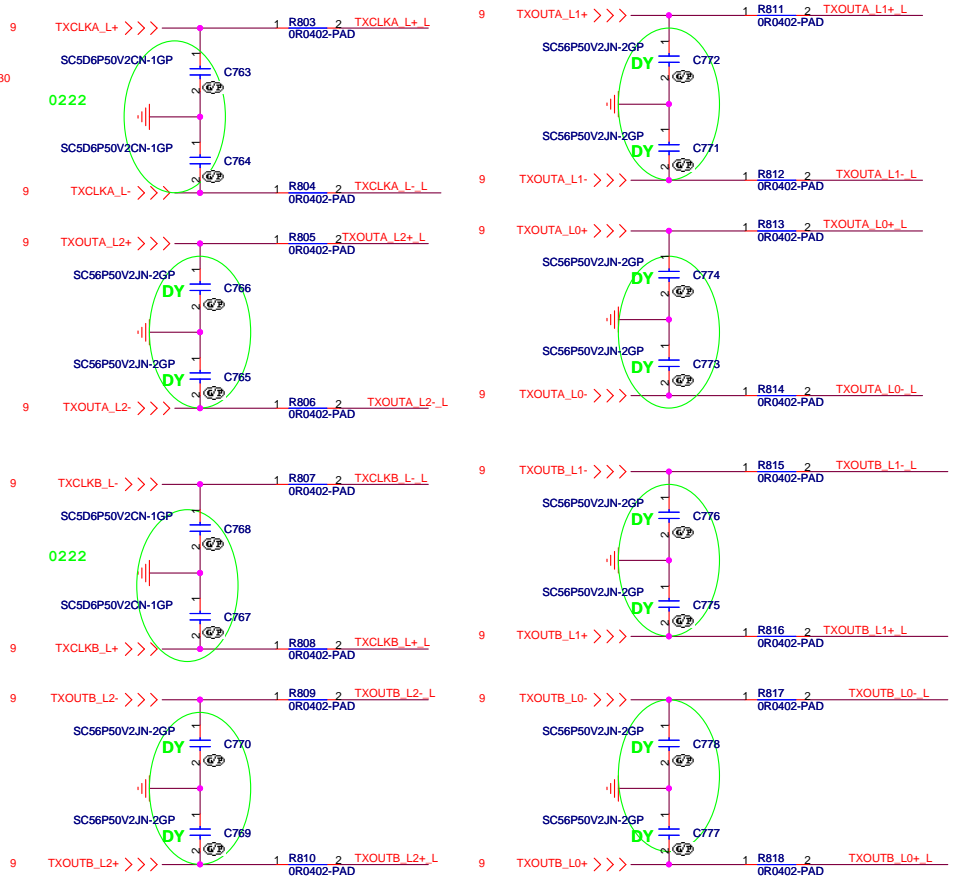
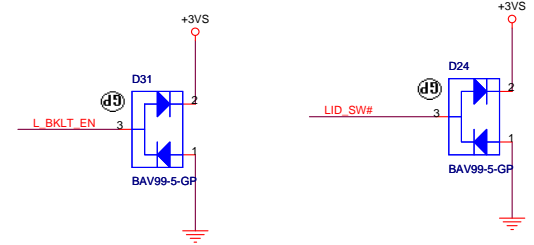
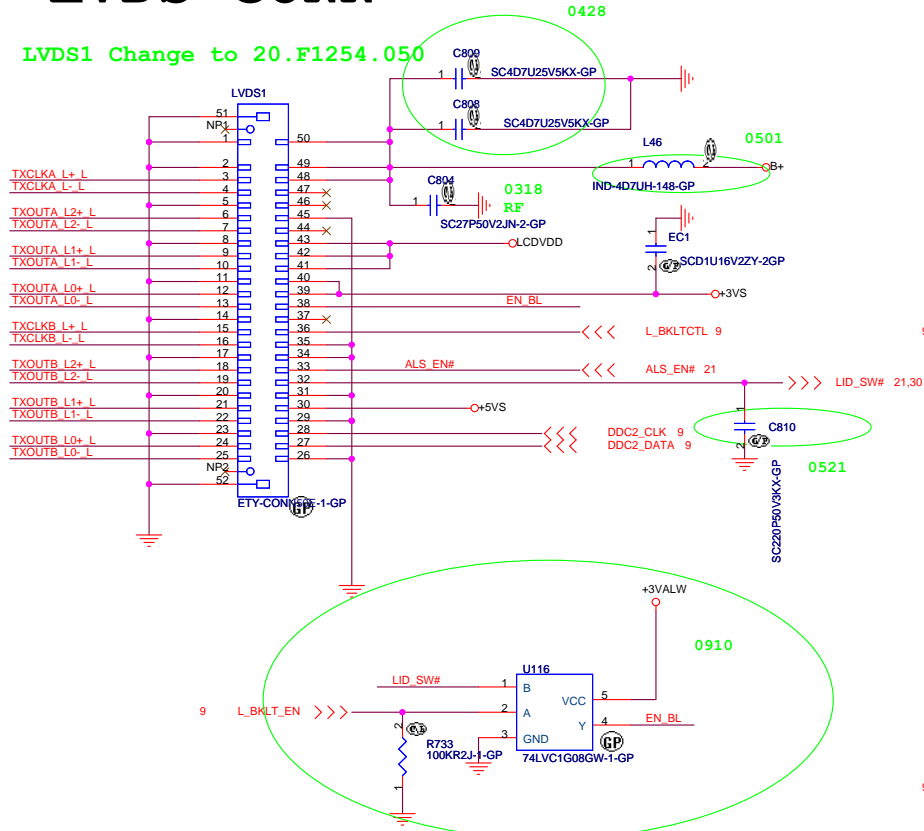
Title: **CRT CONNECTOR**

Size: A3 Document Number: **KARIA** Rev: **SC**

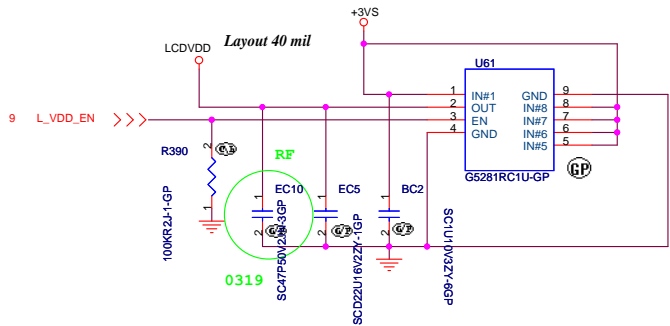
Date: Friday, May 02, 2008 Sheet: 17 of 53

LVDS CONN

LVDS1 Change to 20.F1254.050

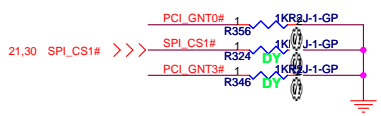
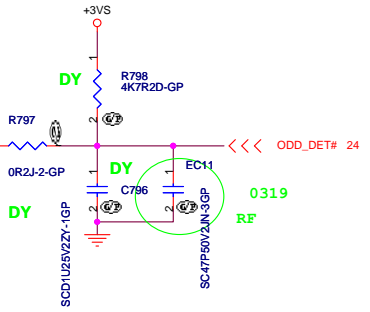
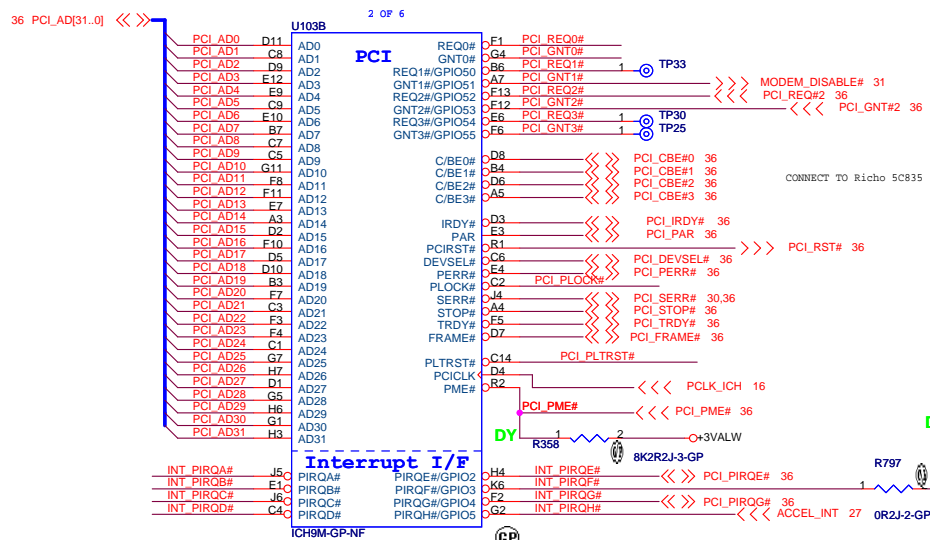
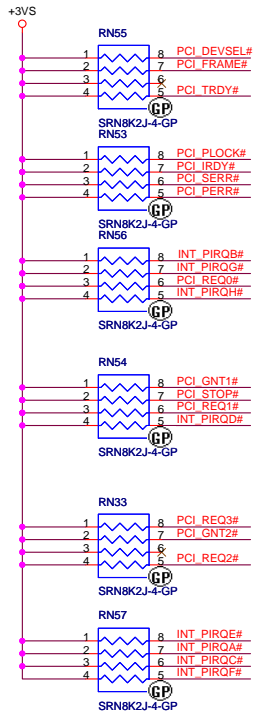


LCD POWER CIRCUIT

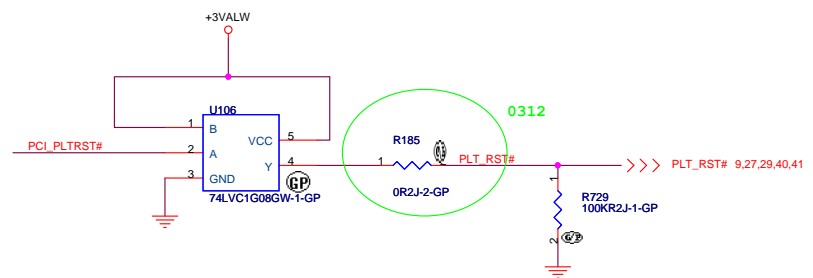


BOM1

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
LCD CONN.		
Size A3	Document Number KARIA	Rev SC
Date: Friday, May 23, 2008	Sheet 18	of 53



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	EEP(Defaulst)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



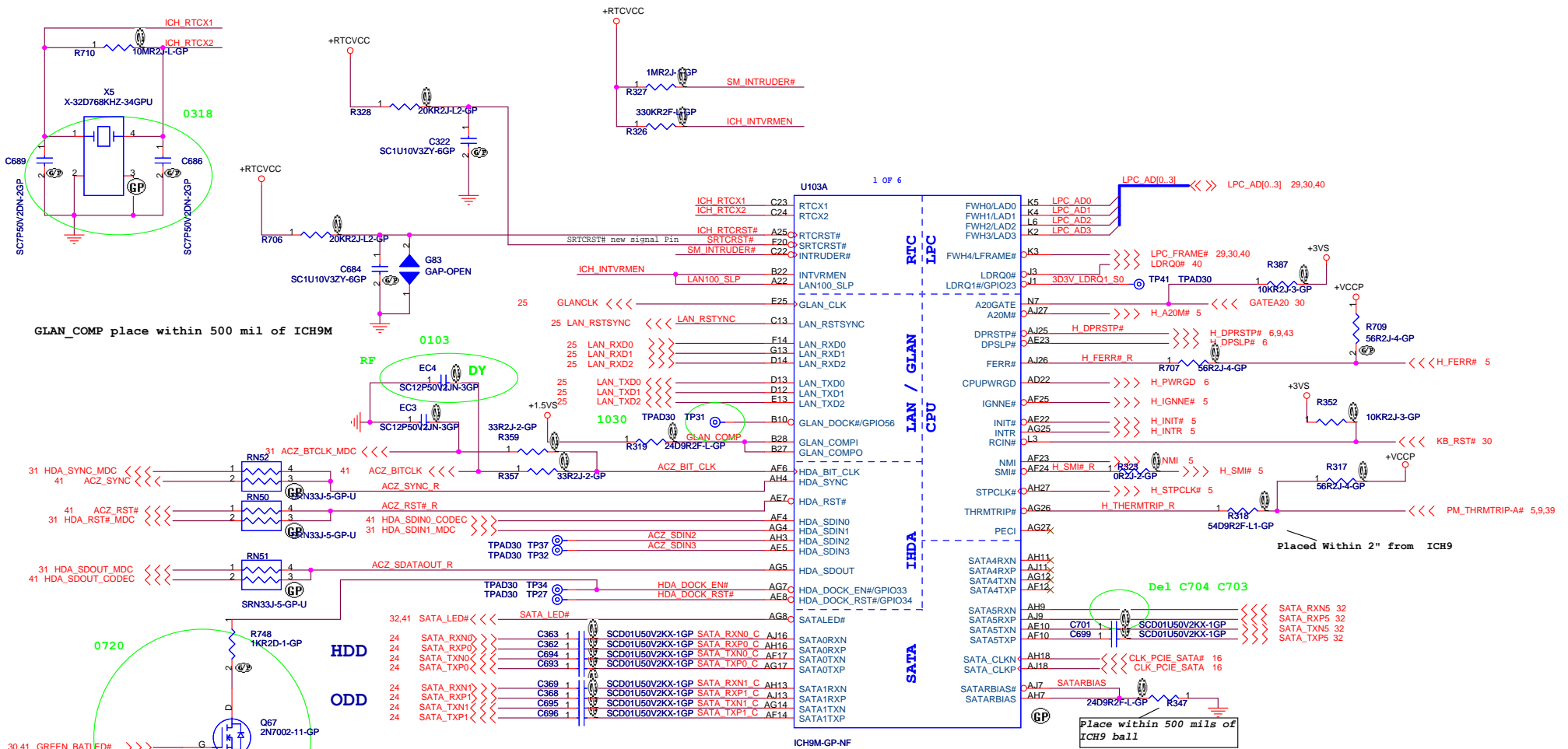
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

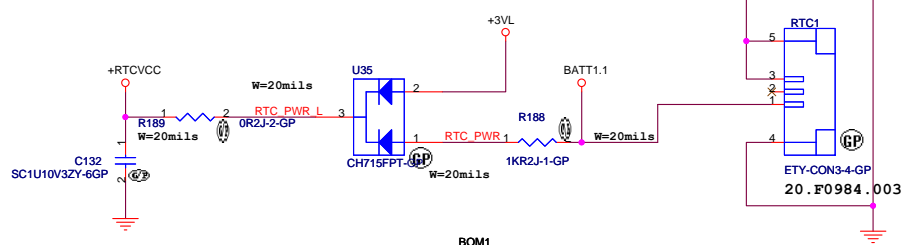
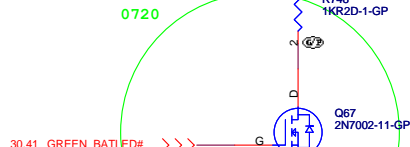
Title: **ICH9-M (1 of 5)**

Size: Document Number: **KARIA** Rev: SC

Date: Friday, May 02, 2008 Sheet: 19 of 53



GLAN_COMP place within 500 mil of ICH9M



integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable

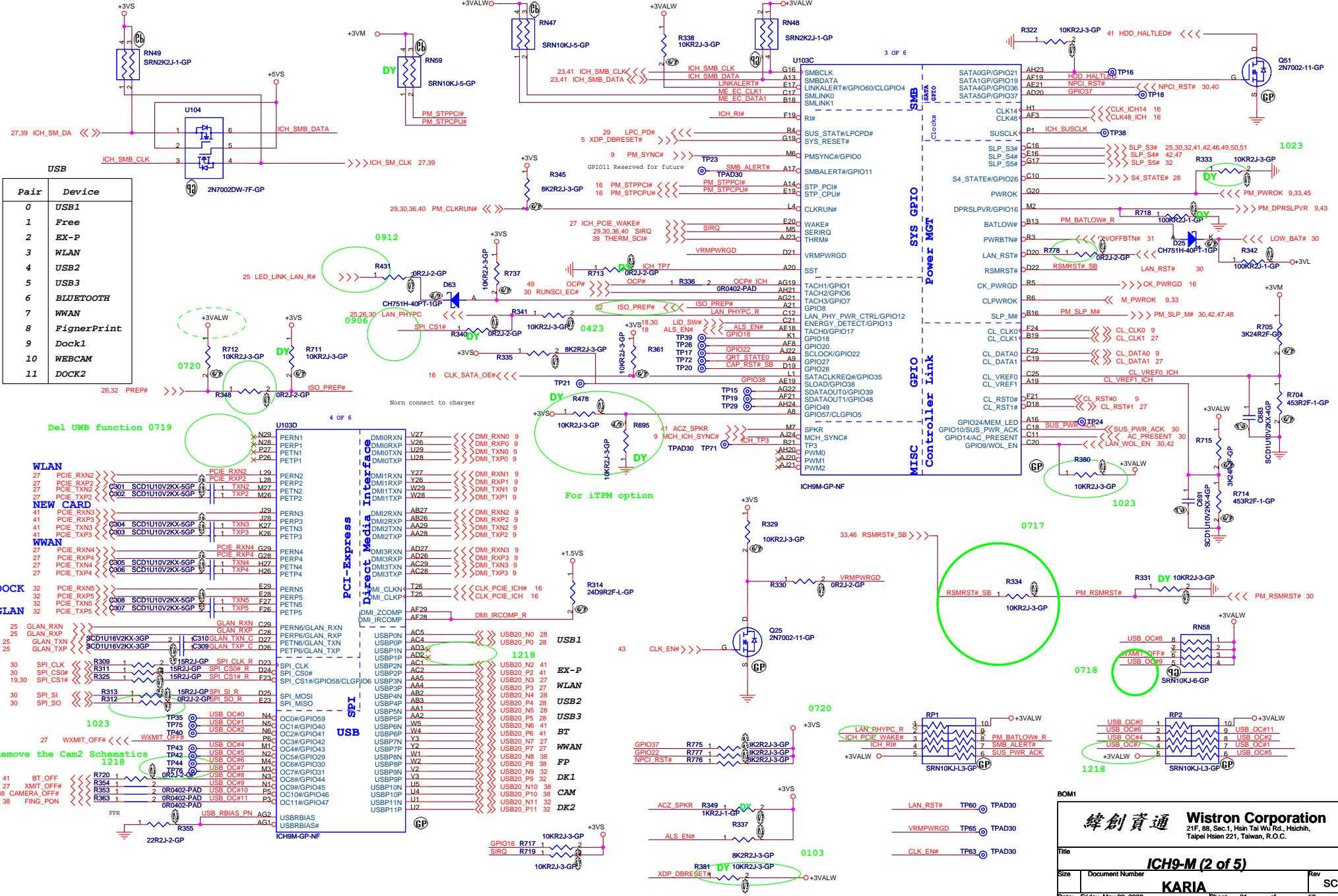
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **ICH9-M (2 of 5)**

Size: Document Number **KARIA** Rev: SC

Date: Friday, May 02, 2008 Sheet 20 of 53



Pair	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FingerPrint
9	Dock1
10	WEBCAM
11	DOCK2

Del UWB function 0719

Pair	Device
27	PCIE_RXN2
27	PCIE_RXP2
27	PCIE_TXN2
27	PCIE_TXP2
41	PCIE_RXN3
41	PCIE_RXP3
41	PCIE_TXN3
41	PCIE_TXP3
27	PCIE_RXN4
27	PCIE_RXP4
27	PCIE_TXN4
27	PCIE_TXP4
32	PCIE_RXN5
32	PCIE_RXP5
32	PCIE_TXN5
32	PCIE_TXP5
25	GLAN_RXN
25	GLAN_RXP
25	GLAN_TXN
25	GLAN_TXP
30	SPI_CLK
30	SPI_CS0#
19,30	SPI_CS1#
30	SPI_SI
30	SPI_SO
27	WXMIT_OFF#
41	BT_OFF
27	XMIT_OFF#
38	CAMERA_OFF#
38	FING_PON

Remove the Cam2 Schematics 1218

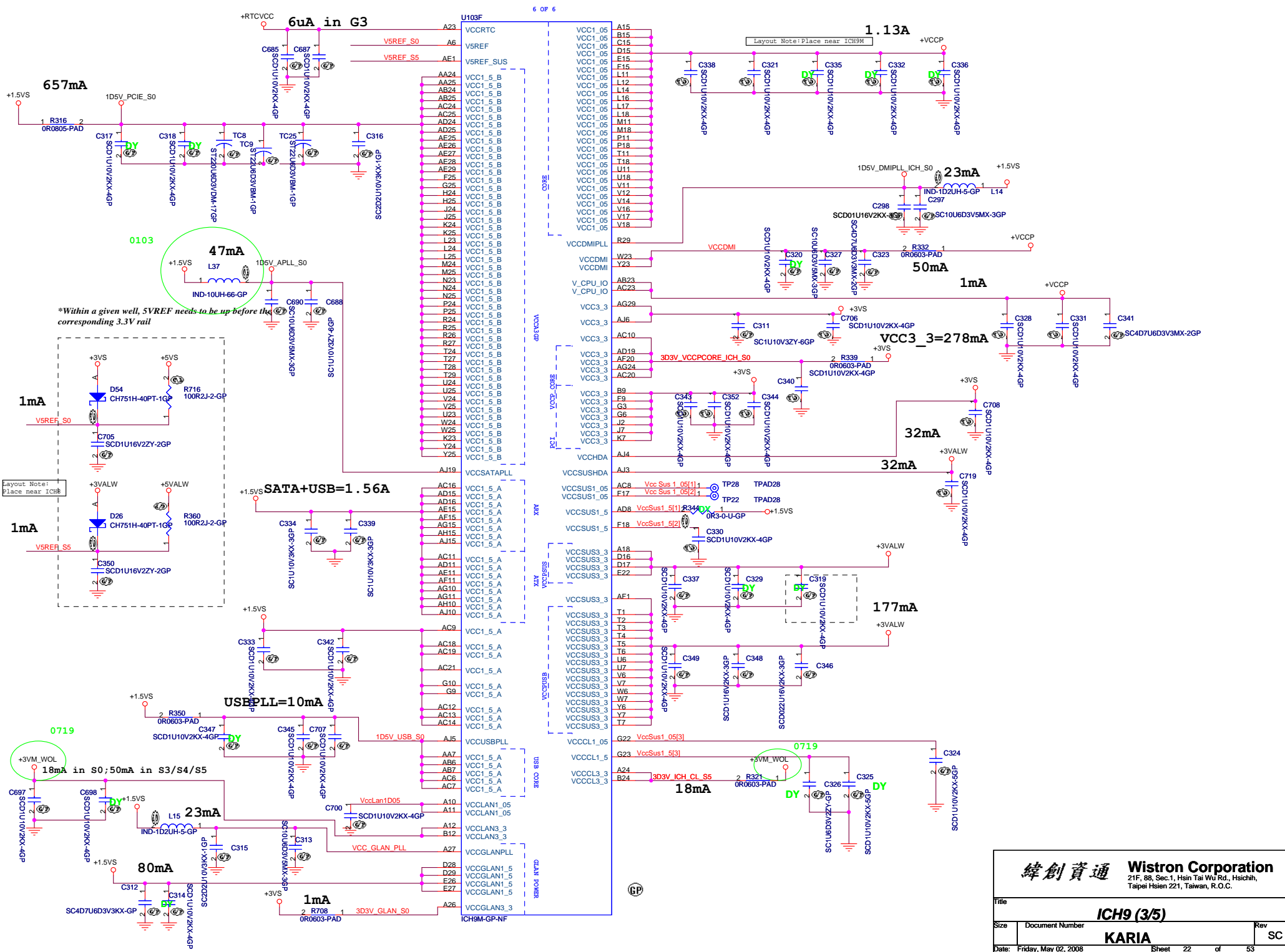
41	BT_OFF
27	XMIT_OFF#
38	CAMERA_OFF#
38	FING_PON

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

ICH9-M (2 of 5)

KARIA

Date: Friday, May 02, 2008 Sheet 21 of 53



緯創資通 Wistron Corporation

21F, 8R, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		ICH9 (3/5)	
Size	Document Number		
		KARIA	
Date: Friday, May 02, 2008	Sheet 22	of	53

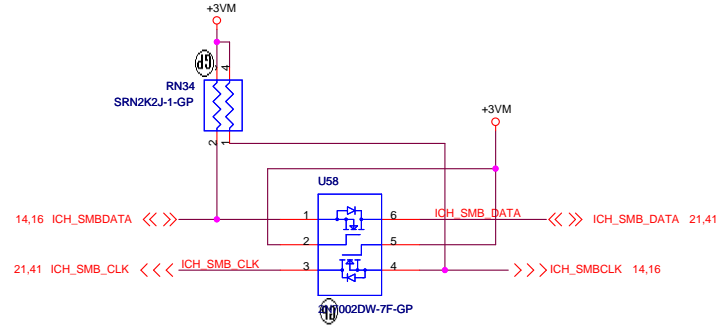
Rev SC

5 OF 6

AA26	VSS	H5
AA27	VSS	J23
AA3	VSS	J26
AA6	VSS	J27
AB1	VSS	AC22
AA23	VSS	K28
AB28	VSS	K29
AB29	VSS	L13
AB4	VSS	L15
AB5	VSS	L2
AC17	VSS	L26
AC26	VSS	L27
AC27	VSS	L5
AC3	VSS	L7
AD1	VSS	M12
AD10	VSS	M13
AD12	VSS	M14
AD13	VSS	M15
AD14	VSS	M16
AD17	VSS	M17
AD18	VSS	M23
AD21	VSS	M28
AD28	VSS	M29
AD29	VSS	N11
AD4	VSS	N12
AD5	VSS	N13
AD6	VSS	N14
AD7	VSS	N15
AD9	VSS	N16
AE12	VSS	N17
AE13	VSS	N18
AE14	VSS	N26
AE16	VSS	N27
AE17	VSS	P12
AE2	VSS	P13
AE20	VSS	P14
AE24	VSS	P15
AE3	VSS	P16
AE4	VSS	P17
AE6	VSS	P2
AE9	VSS	P23
AF13	VSS	P28
AF16	VSS	P29
AF18	VSS	P4
AF22	VSS	P7
AH26	VSS	R11
AF28	VSS	R12
AF27	VSS	R13
AF5	VSS	R14
AF7	VSS	R15
AF9	VSS	R16
AG13	VSS	R17
AG16	VSS	R18
AG18	VSS	R28
AG20	VSS	T12
AG23	VSS	T13
AG31	VSS	T14
AG6	VSS	T15
AG9	VSS	T16
AH12	VSS	T17
AH14	VSS	T23
AH17	VSS	B26
AH19	VSS	U12
AH2	VSS	U13
AH22	VSS	U14
AH25	VSS	U15
AH28	VSS	U16
AH5	VSS	U17
AH8	VSS	AD23
AJ12	VSS	U26
AJ14	VSS	U27
AJ17	VSS	U3
AJ8	VSS	V1
B11	VSS	V13
B14	VSS	V15
B17	VSS	V23
B2	VSS	V28
B20	VSS	V29
B23	VSS	V4
B5	VSS	V5
B8	VSS	W26
C26	VSS	W27
C27	VSS	W3
E11	VSS	Y1
E14	VSS	Y28
E18	VSS	Y29
E2	VSS	Y4
E21	VSS	Y5
E24	VSS	AG28
E5	VSS	AH6
E8	VSS	AF2
F16	VSS	B25
F28	VSS	
F29	VSS	A1 ICH_GND1 TP74
G12	VSS	A2
G14	VSS	A28
G18	VSS	A29 ICH_GND2 TP69
G21	VSS	AH1
G24	VSS	AH28
G26	VSS	AJ1 ICH_GND3 TP73
G27	VSS	AJ2
G8	VSS	AJ28
H2	VSS	AJ29 ICH_GND4 TP70
H23	VSS	B1
H28	VSS	B29
H29	VSS	

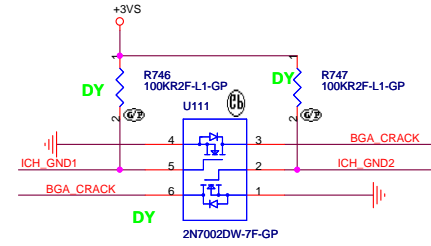
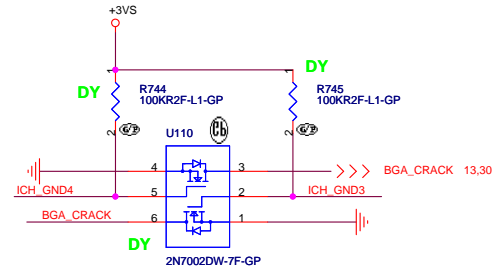
IC98M-GP-NF

NCTF PIN

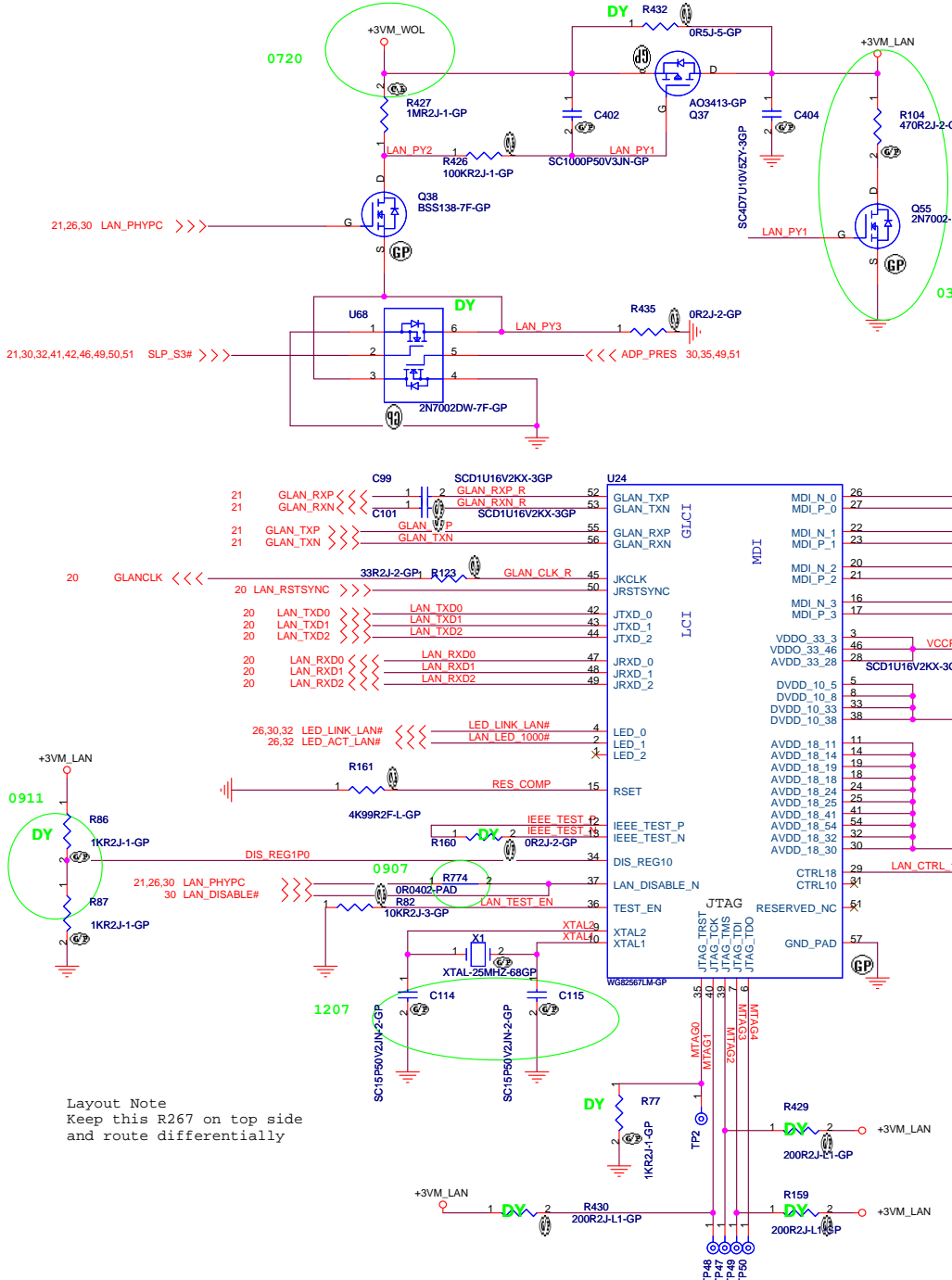


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

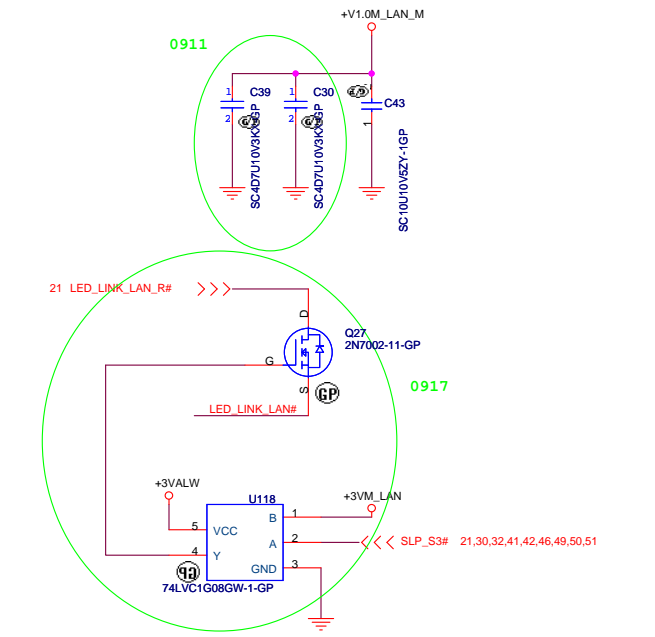
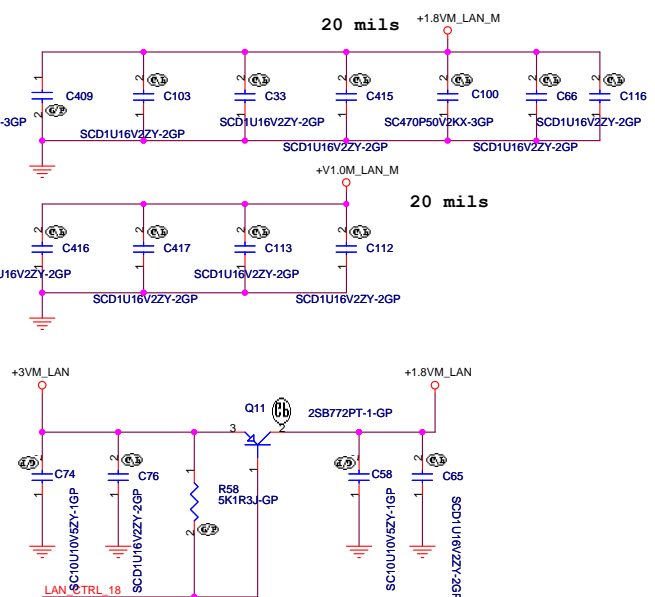
SMBUS



緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		ICH9-M (4 of 4)	
Size	Document Number	KARIA	
Date:	Friday, May 02, 2008	Sheet	23 of 53



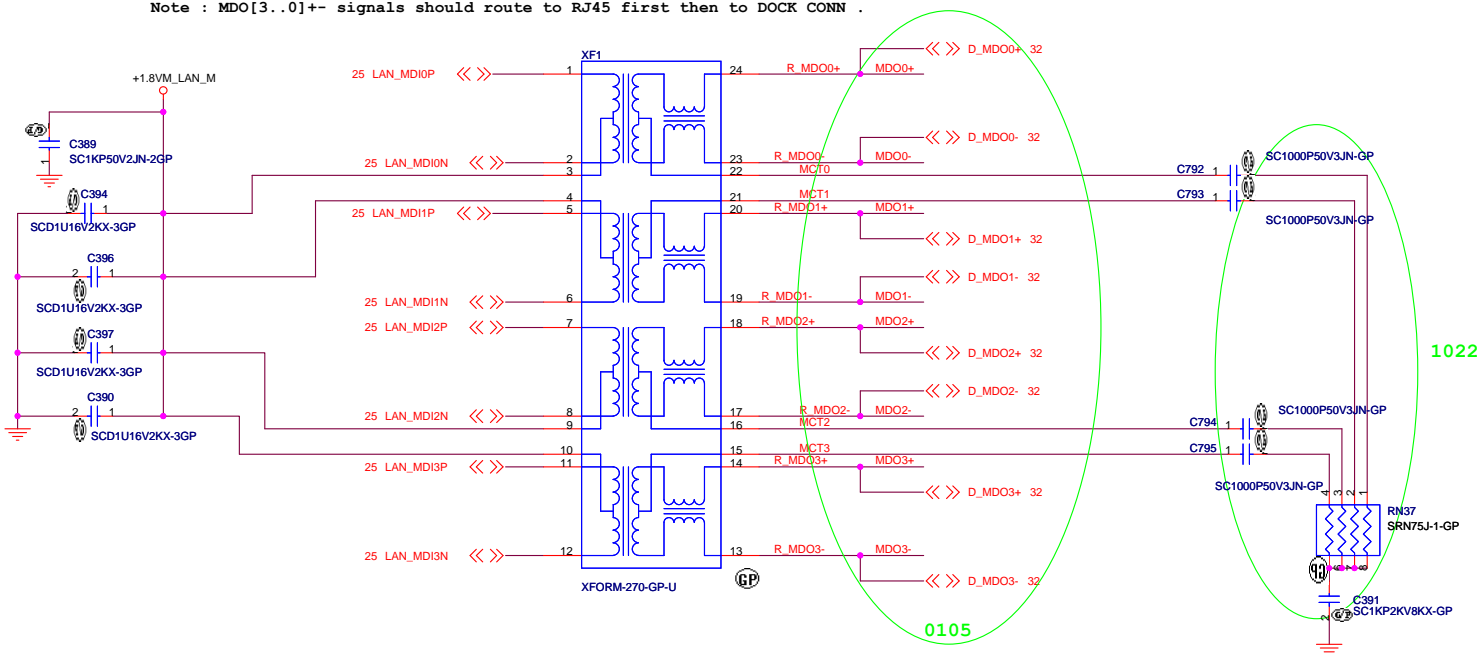
0801 Reserve R57 If RF request
Will replace bead
P/N: 68.00084.341



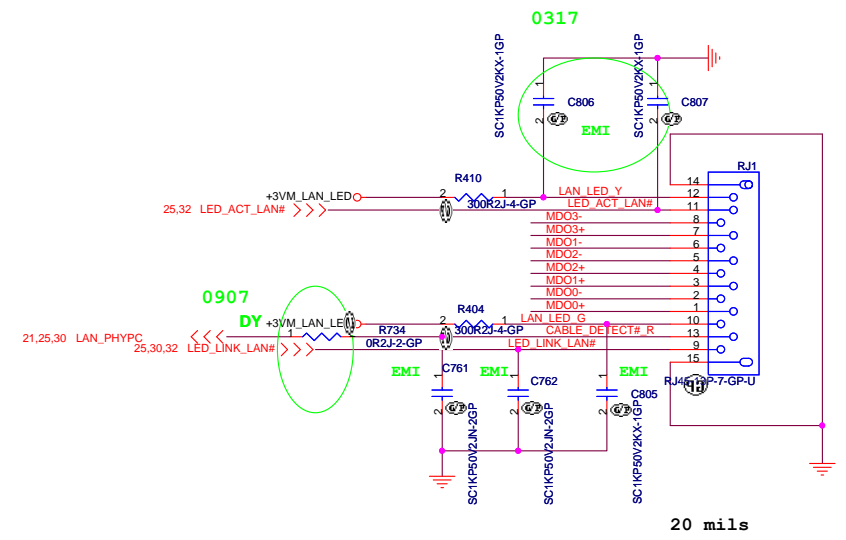
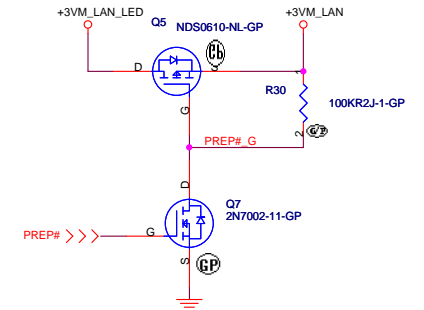
Layout Note
Keep this R267 on top side
and route differentially

BOM1
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.
 Title: **Intel 82567 Boazman**
 Size A3 Document Number: **KARIA** Rev: **PV**
 Date: Sunday, May 18, 2008 Sheet 25 of 53

Note : MDO[3..0]++ signals should route to RJ45 first then to DOCK CONN .

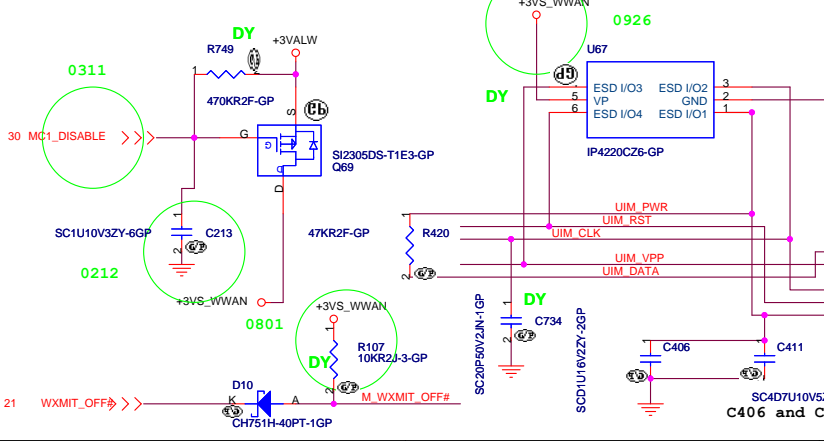
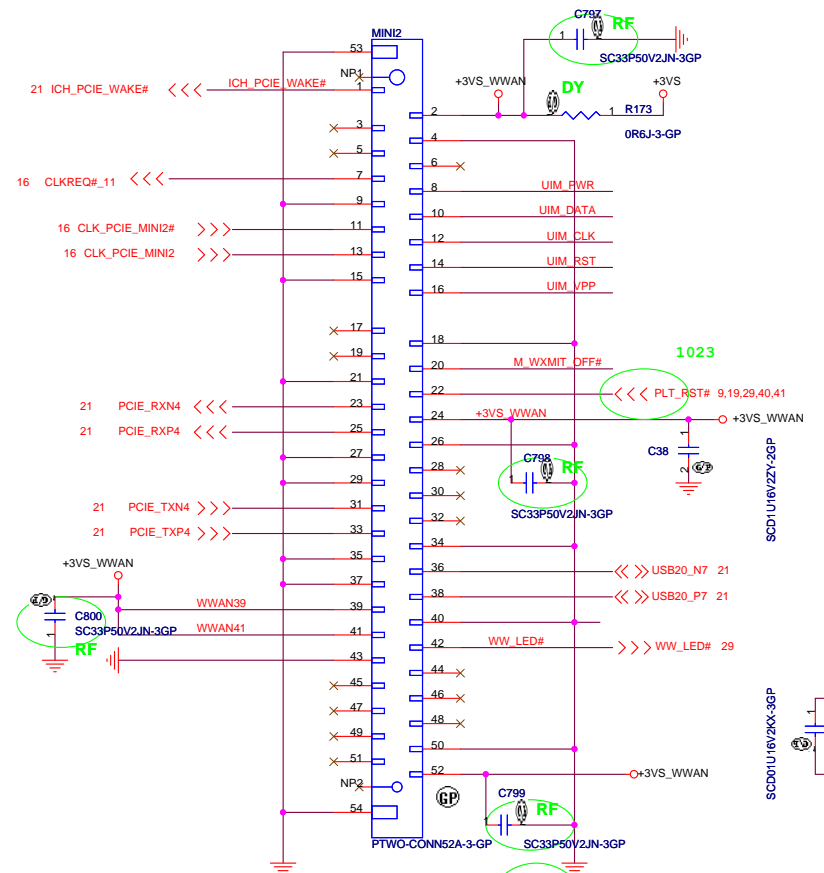


LAN ENERGY DET

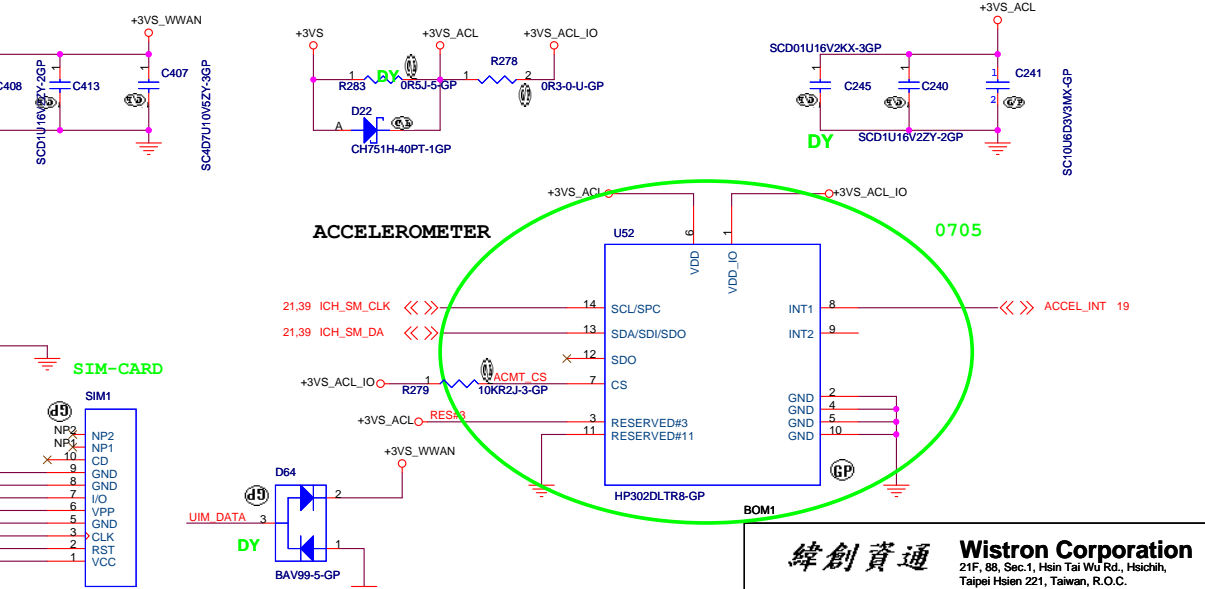
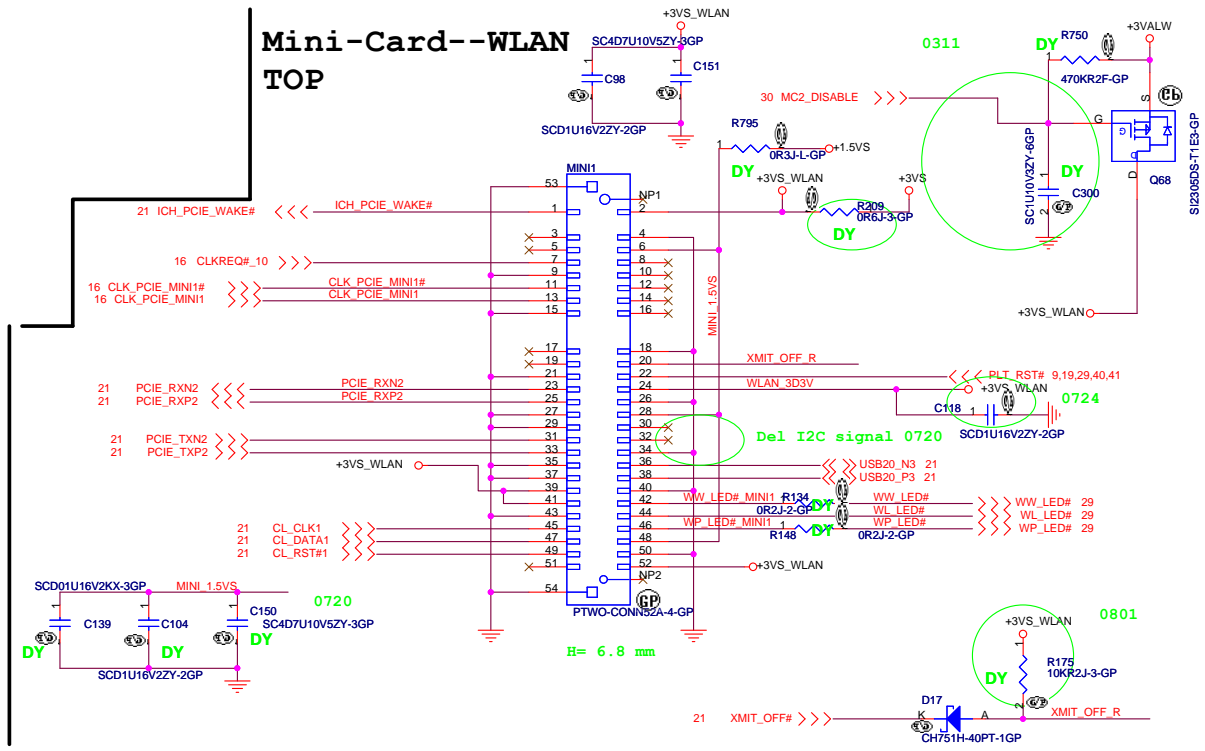


BOM1	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Magnetic & RJ45	
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Date: Friday, May 02, 2008	Sheet 26 of 53

Mini-Card--WWAN Bottom



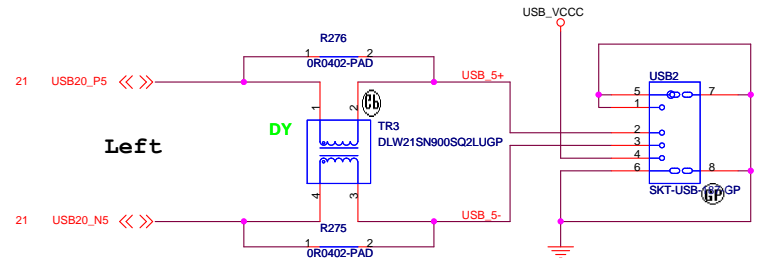
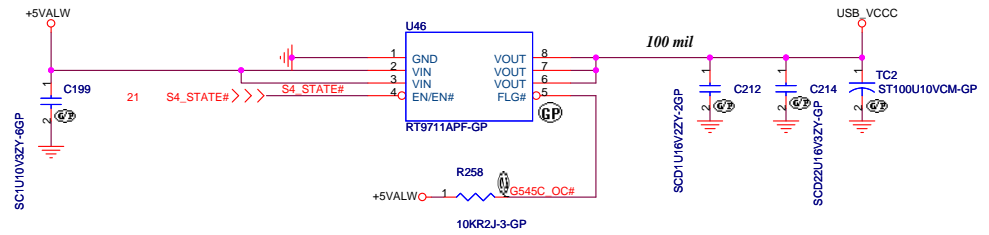
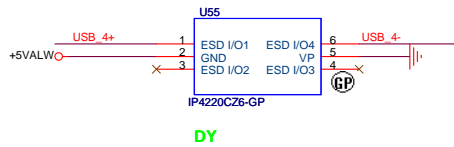
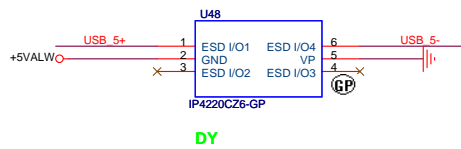
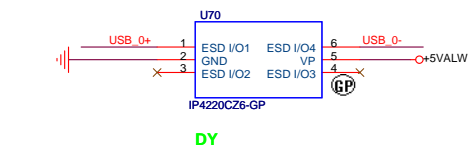
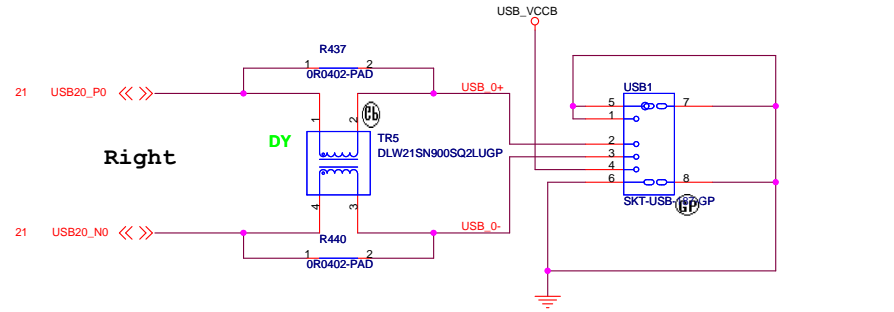
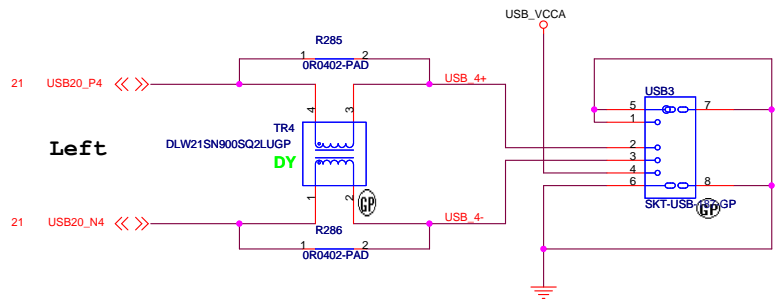
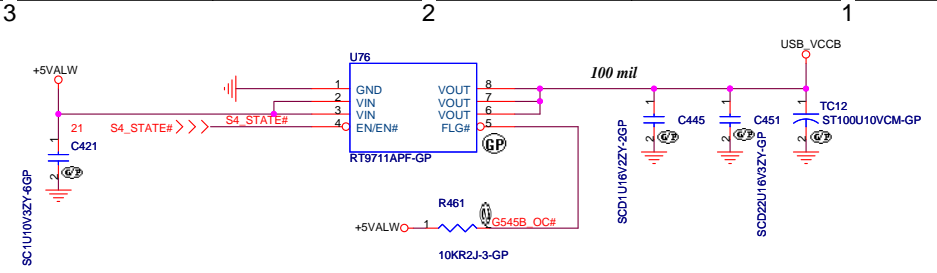
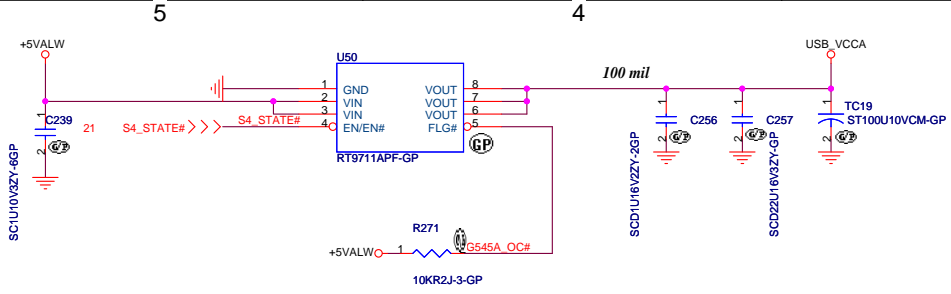
Mini-Card--WLAN TOP



C406 and C411 please close to SIM connector

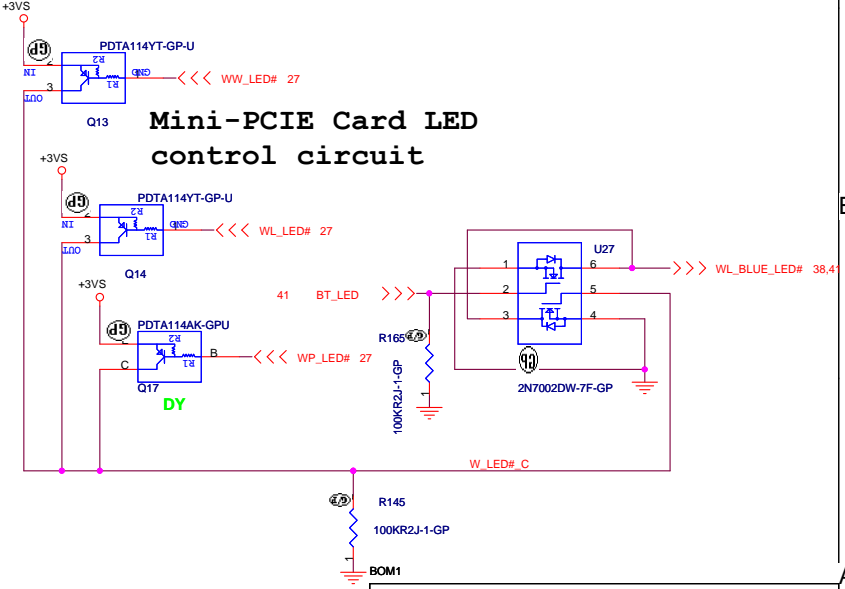
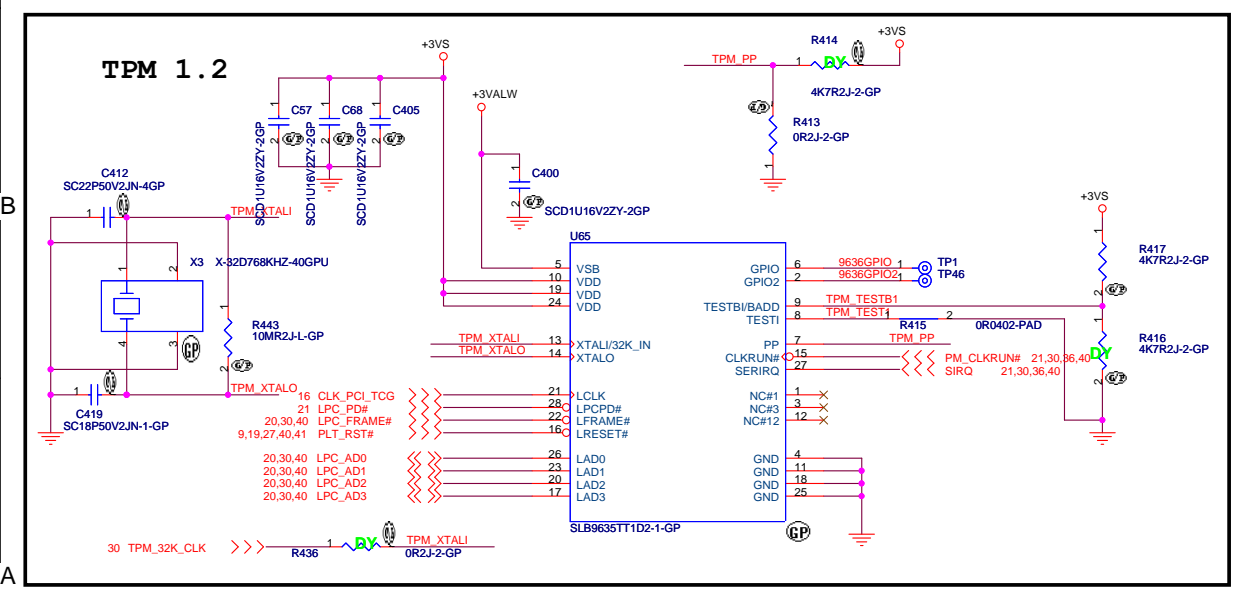
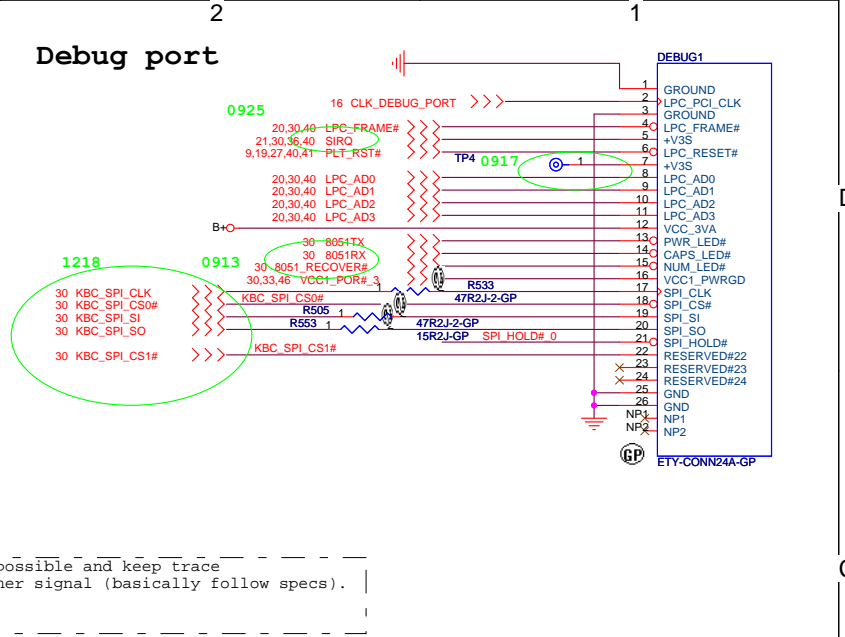
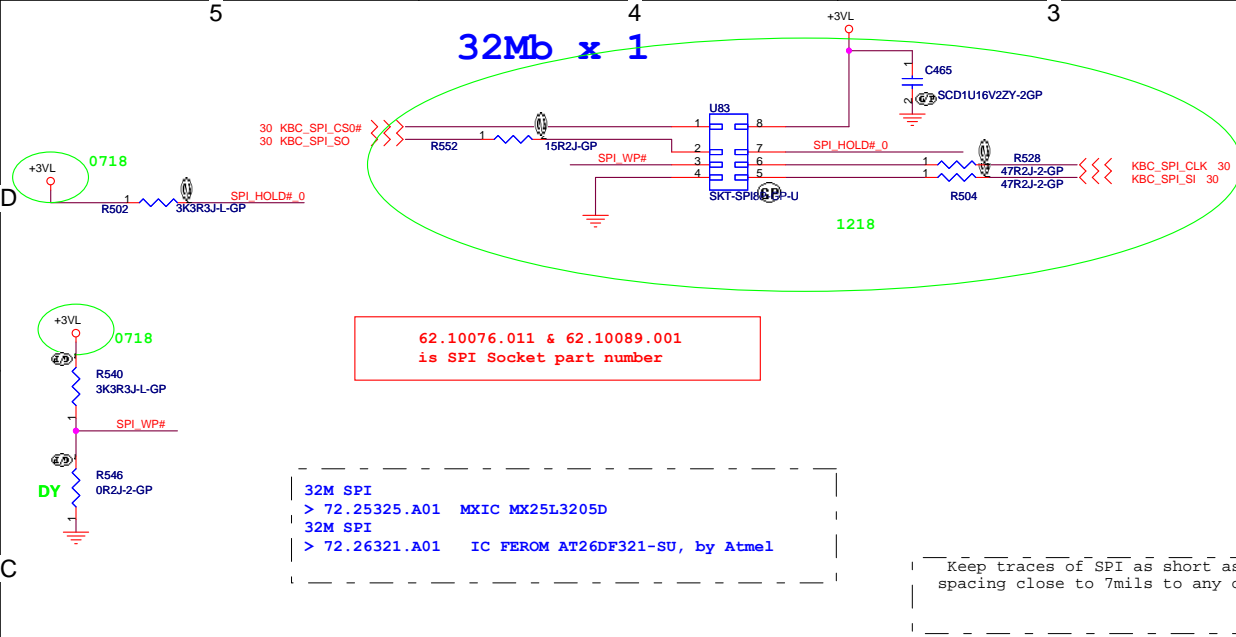
Must be placed in the center of the system

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Mini-Card/Accelerometer	
File	Rev
Size	SC
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	KARIA
Date: Wednesday, May 21, 2008	Sheet 27 of 53



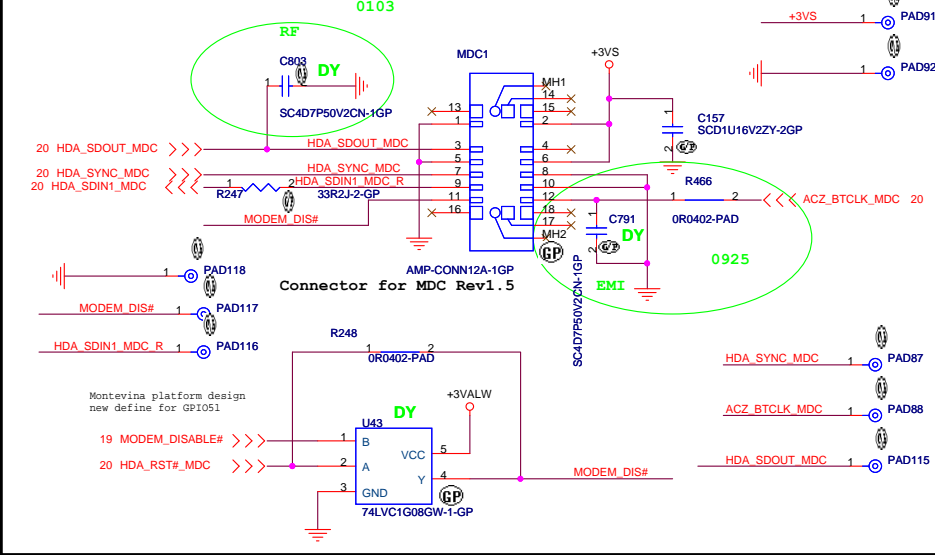
BOM1

緯創資通 Wistron Corporation	
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.	
USB Connector	
Title	
Size A3	Document Number
Date: Friday, May 02, 2008	KARIA
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of 53	

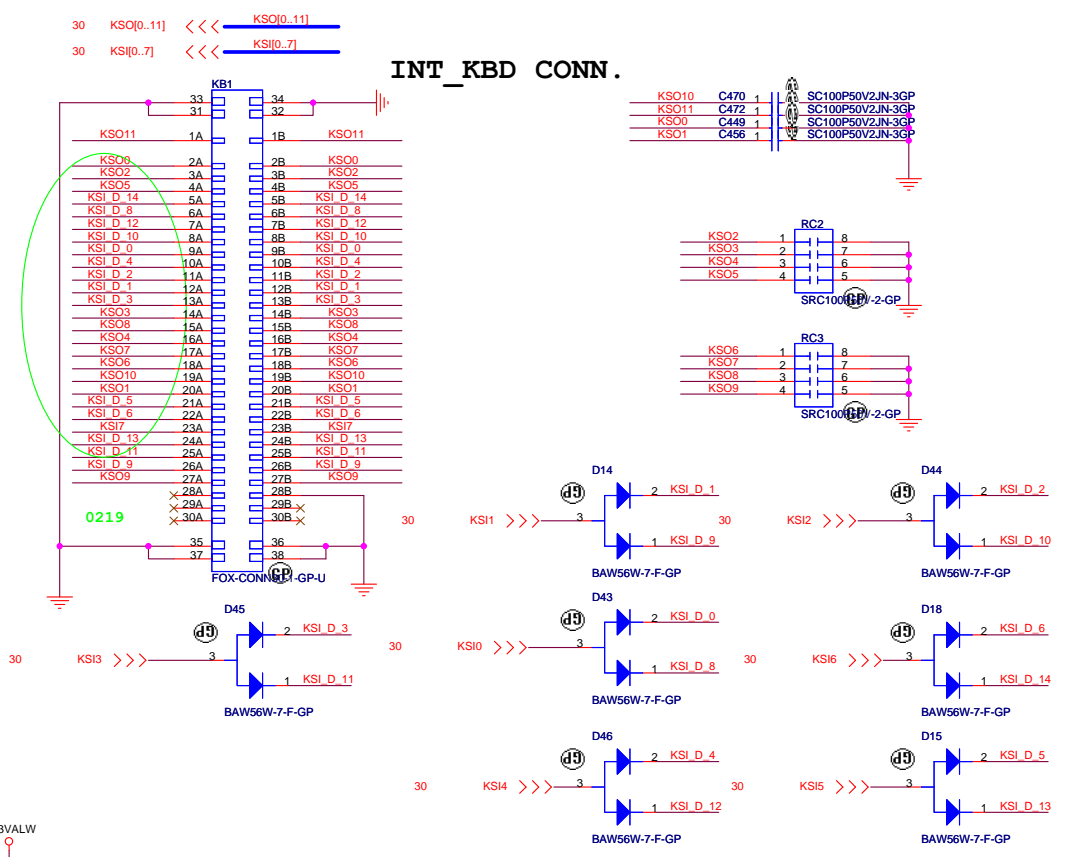


緯創資通 Wistron Corporation	
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title TPM/BIOS/24 DEBUG PORT	
Size A3	Document Number KARIA
Date: Thursday, May 15, 2008	Sheet 29 of 53
Rev SC	

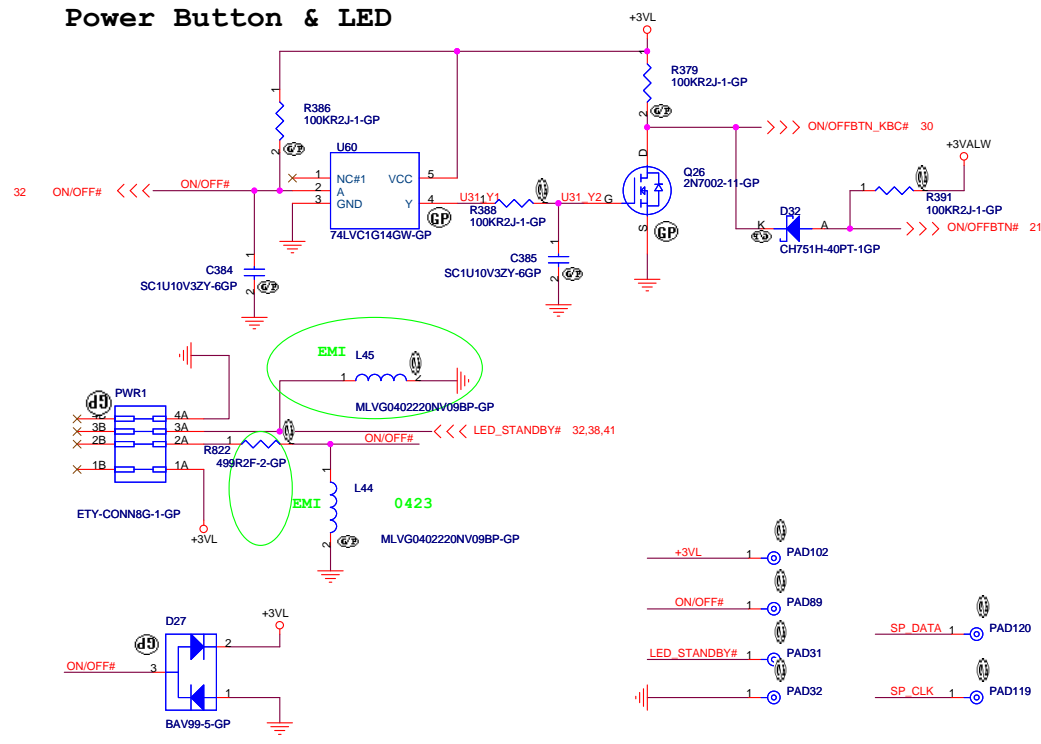
MDC 1.5 Conn.



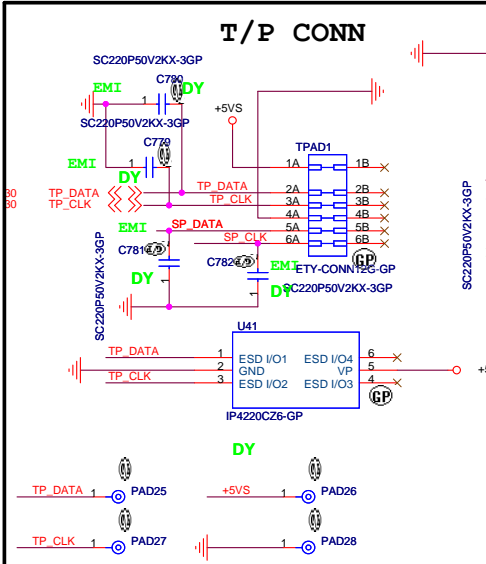
INT_KBD CONN.



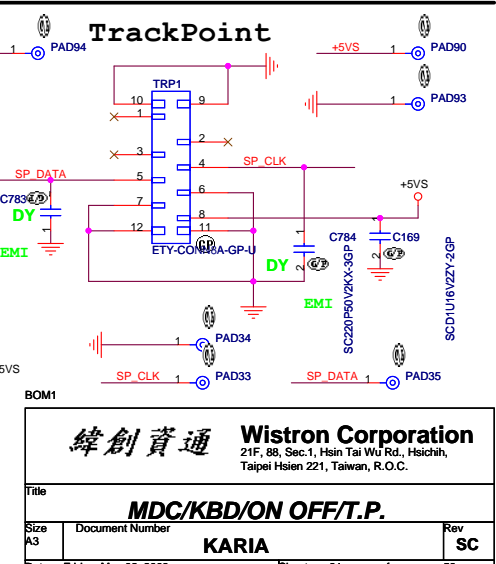
Power Button & LED



T/P CONN



TrackPoint



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

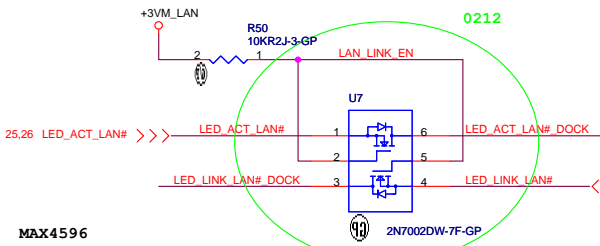
Title: **MDC/KBD/ON OFF/T.P.**

Size A3 Document Number: **KARIA** Rev: **SC**

Date: Friday, May 02, 2008 Sheet 31 of 53

Docking CONN. 164 PIN

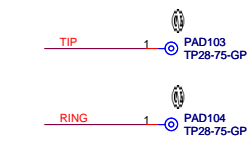
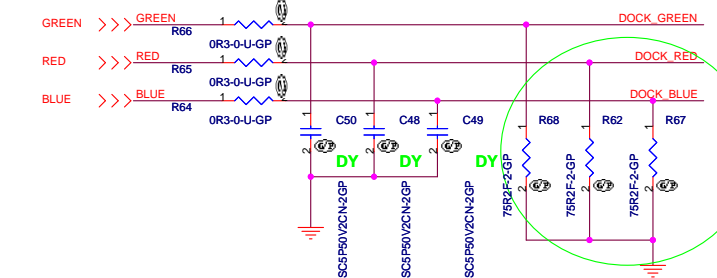
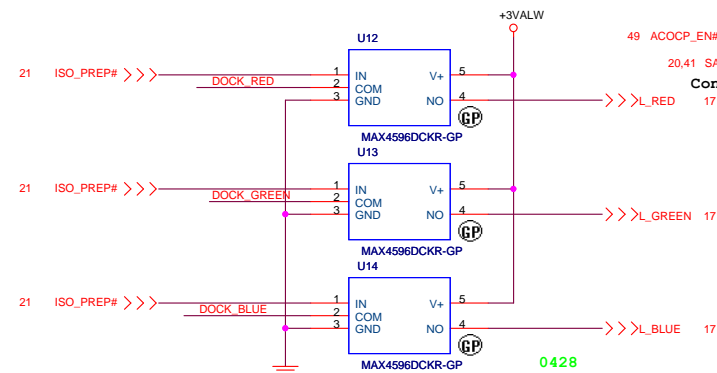
current rating 6A



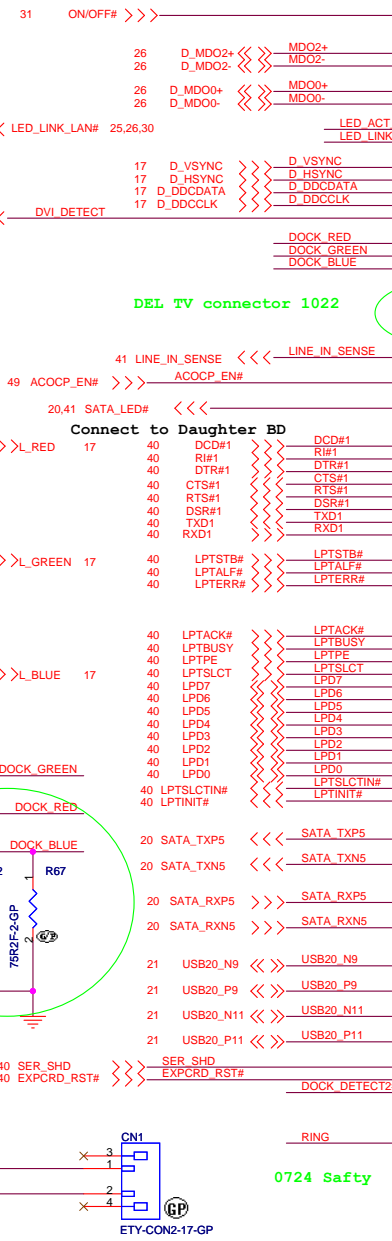
MAX4596

IN	NO TO COM	COM TO NO
L	OFF	
H	ON	

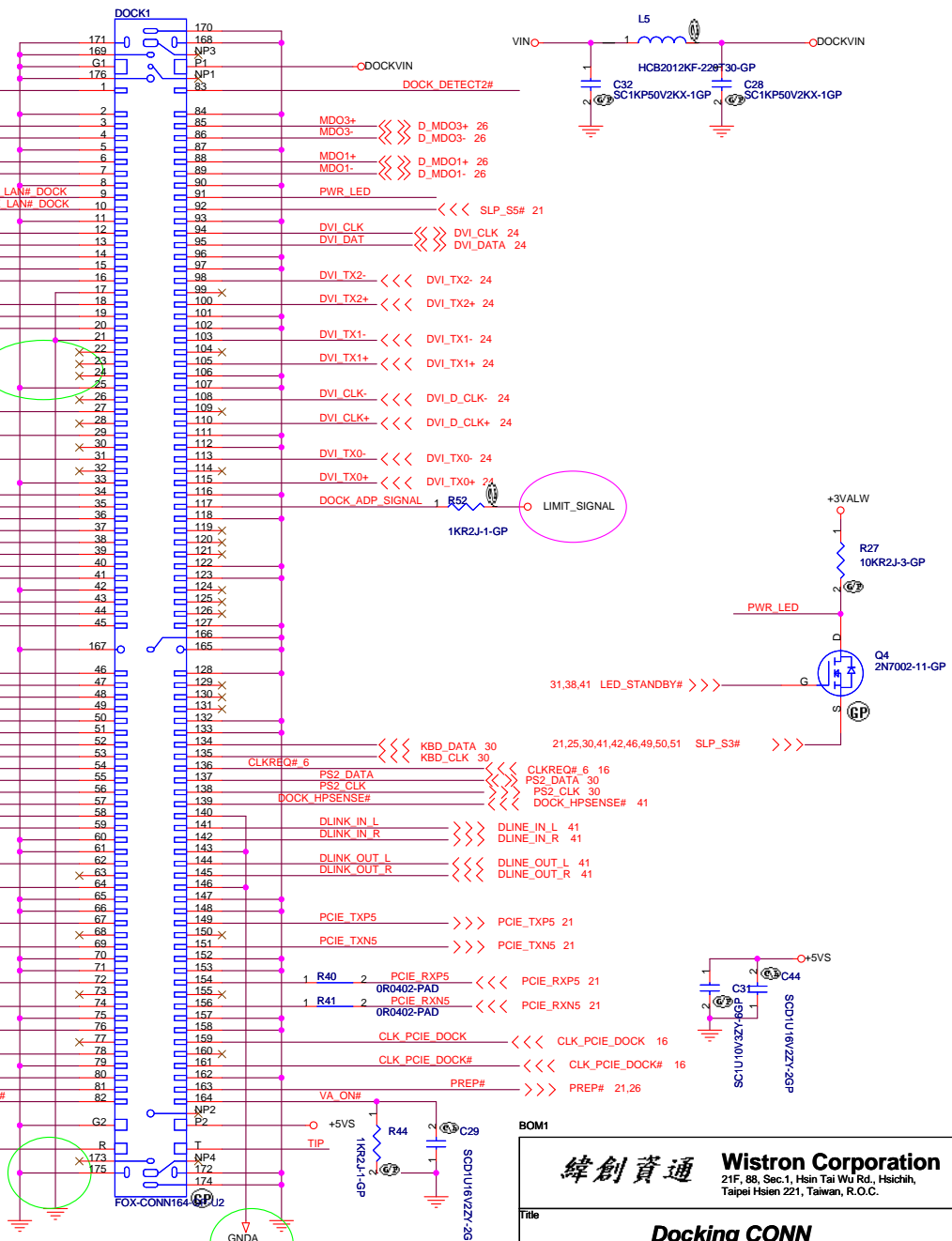
Close to DOCKING CONN.



Layout Notes :
Place MODEM1 & BEAD near Docking connector



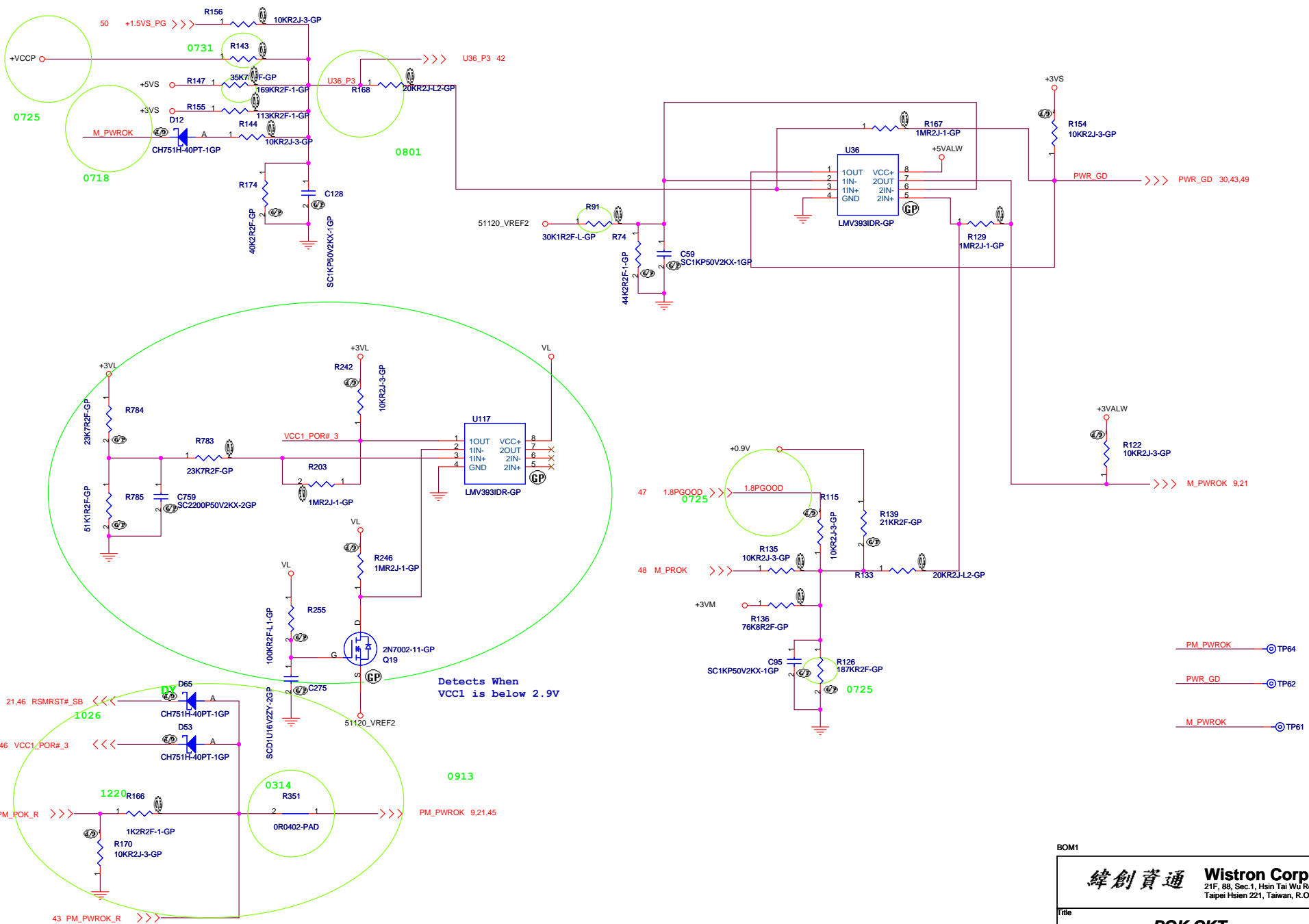
0724 Safty For TIP and Ring cut all layers



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Docking CONN		Rev
Size A3	Document Number	Karia	SC
Date: Thursday, May 15, 2008	Sheet	32	of 53

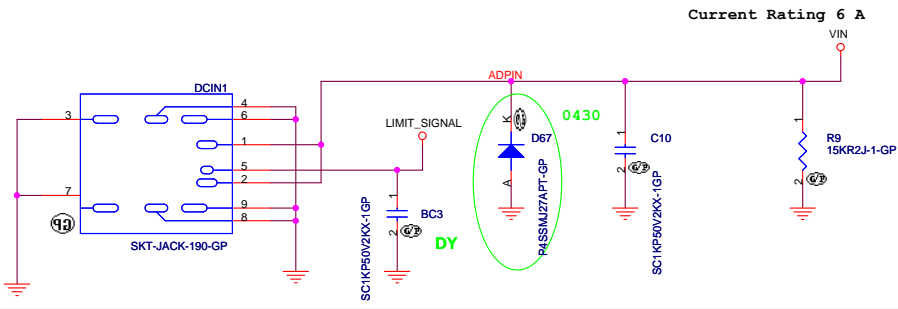


- PM_PWROK TP64
- PWR_GD TP62
- M_PWROK TP61

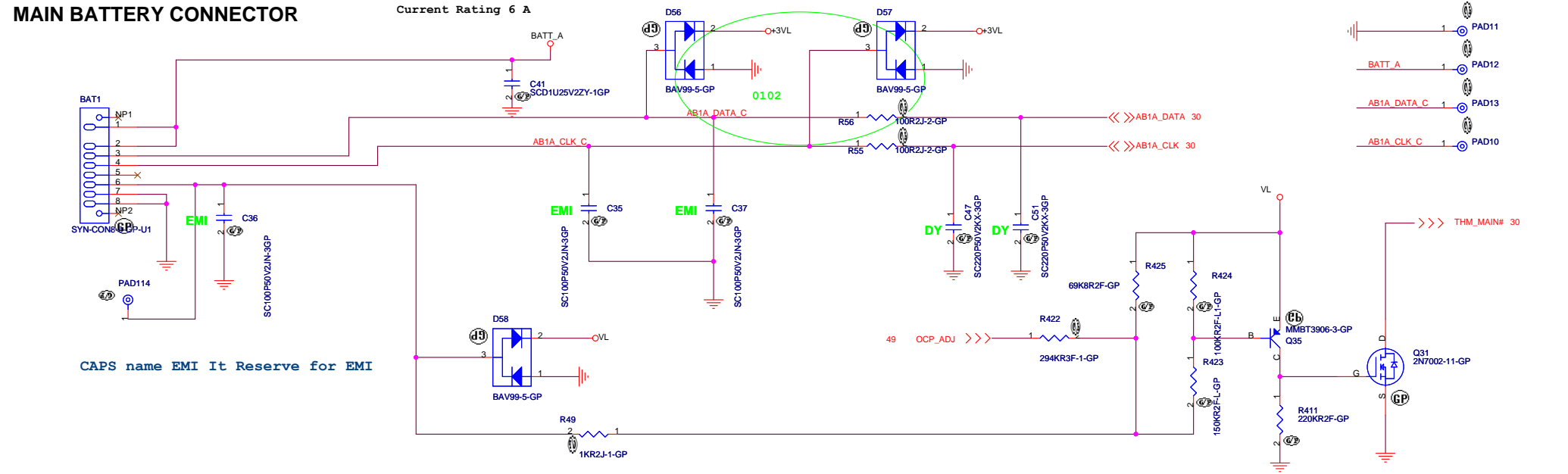
BOM1

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
POK CKT		
Size A3	Document Number	Rev
	KARIA	SC
Date: Friday, May 02, 2008	Sheet 33 of 53	

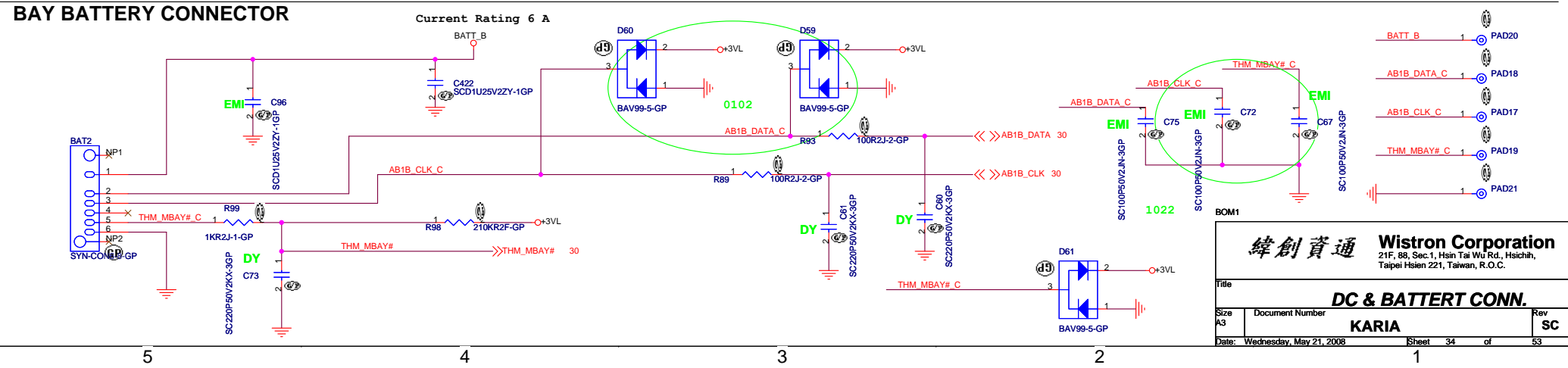
Adaptor in to generate DCBATOUT



MAIN BATTERY CONNECTOR



BAY BATTERY CONNECTOR



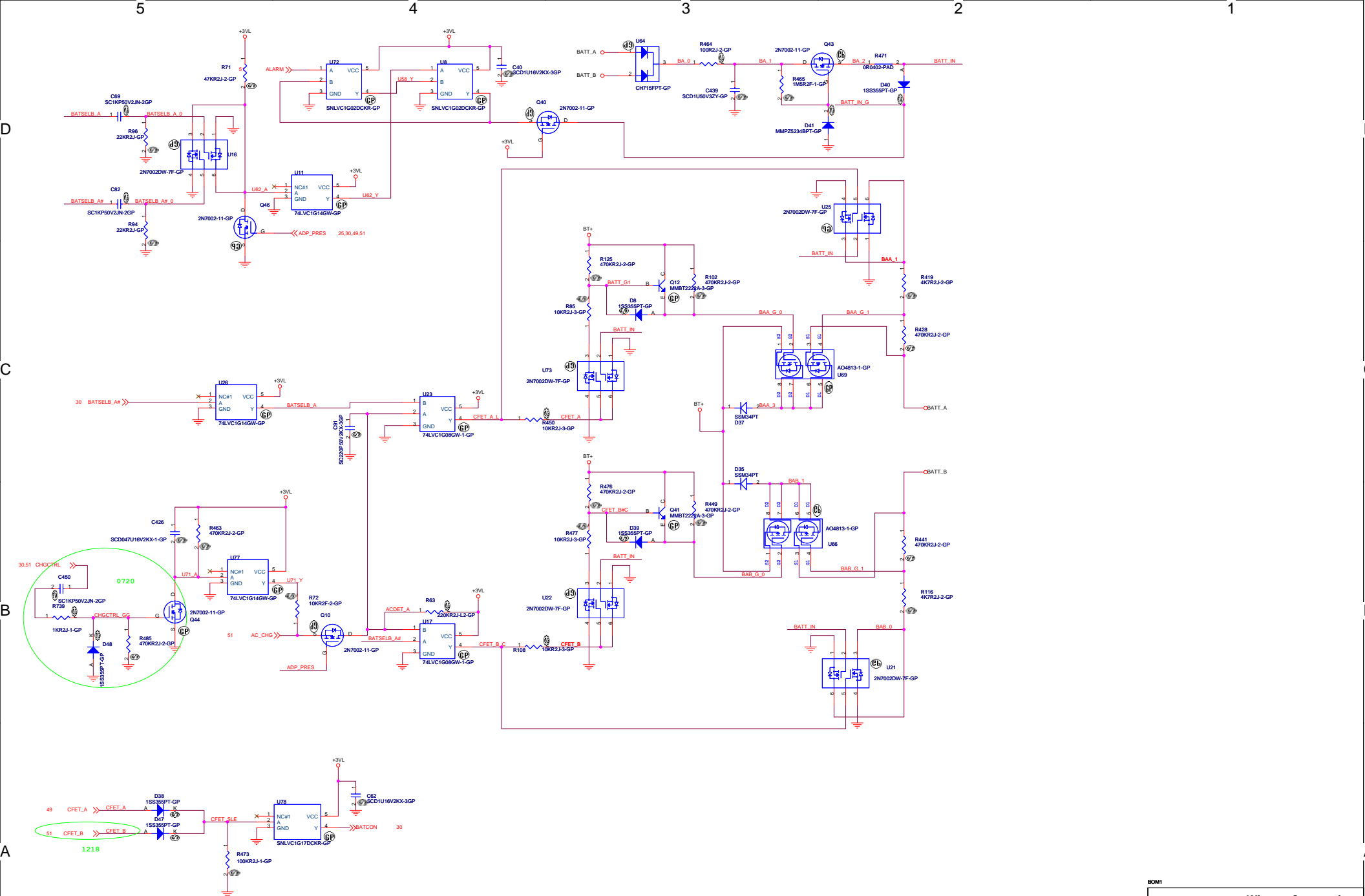
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

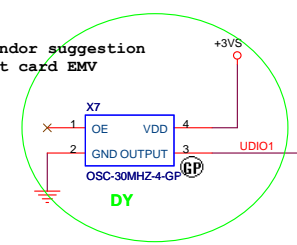
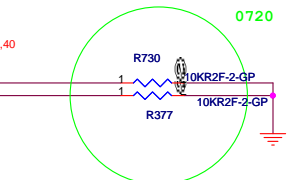
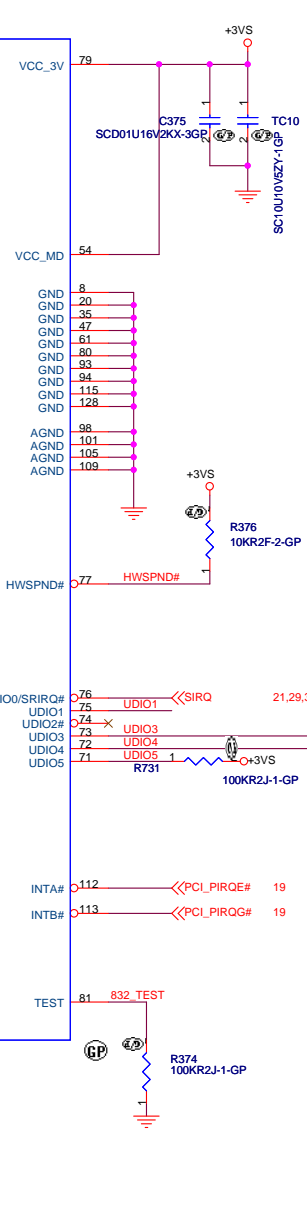
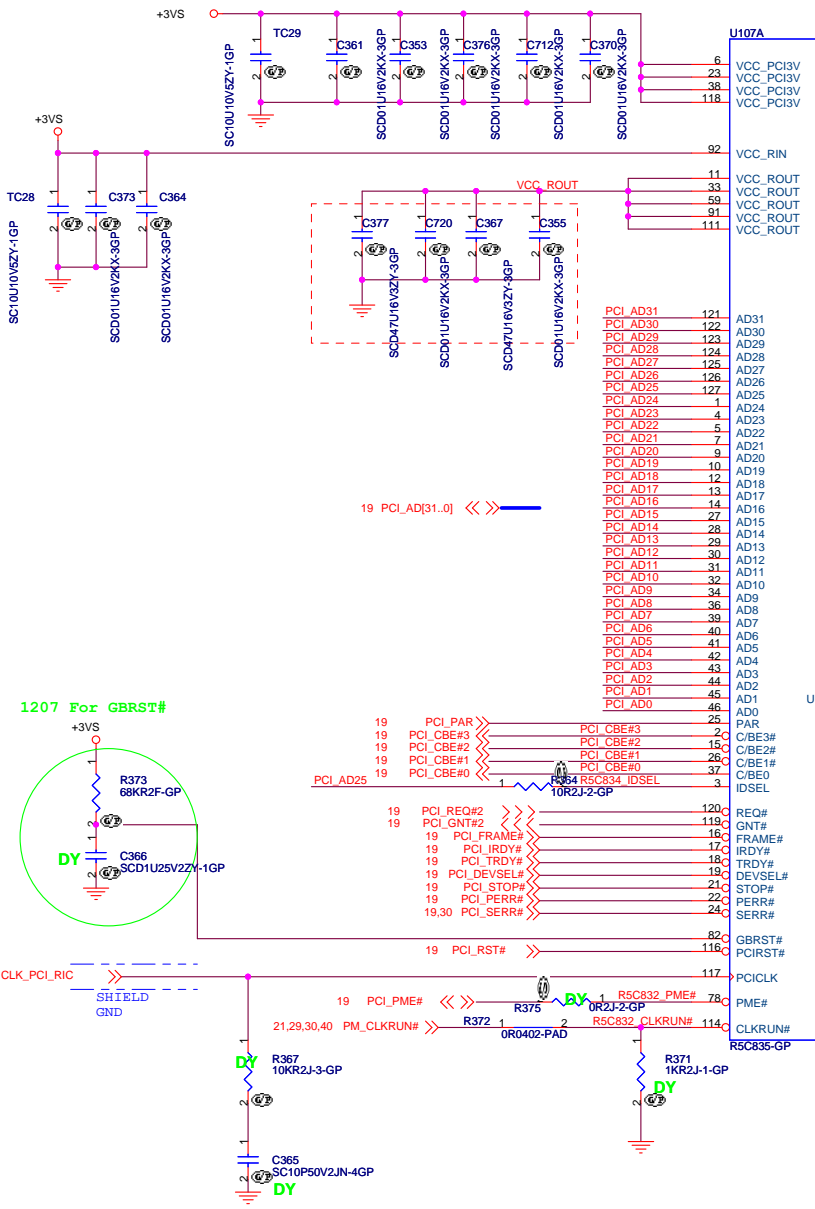
DC & BATTERY CONN.

KARIA

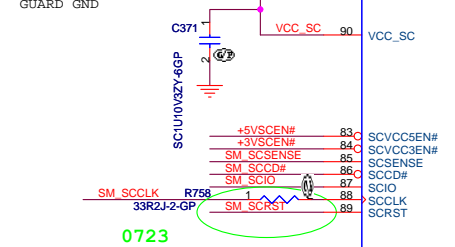
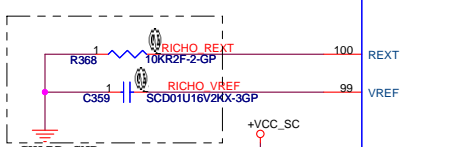
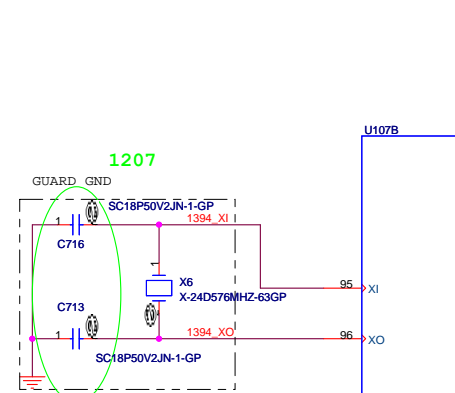
Rev SC

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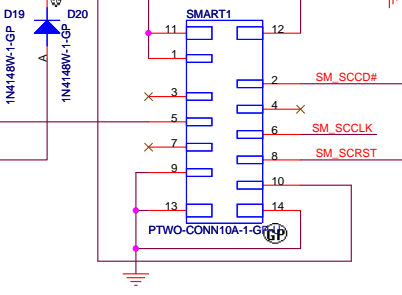
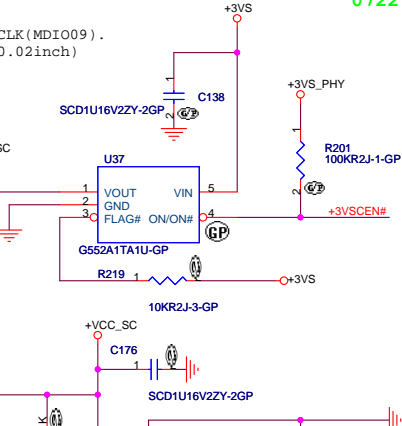
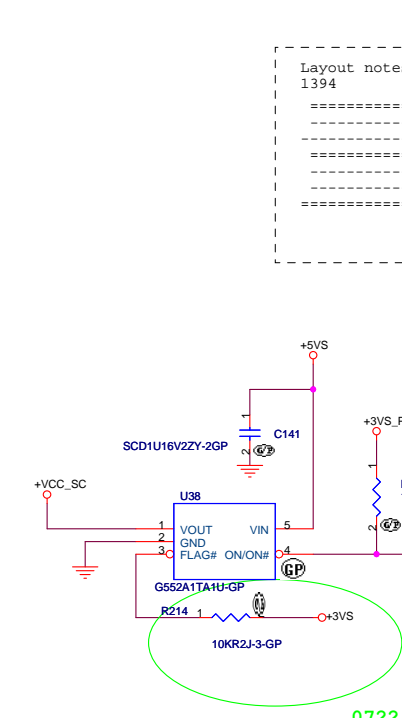
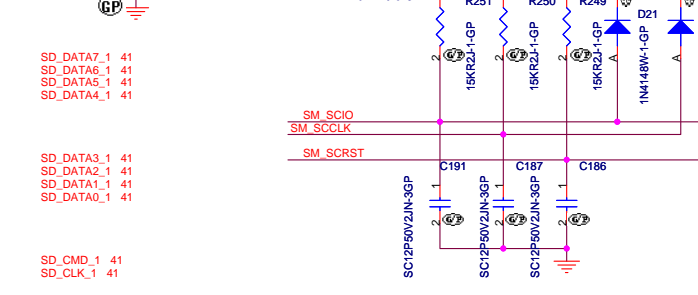
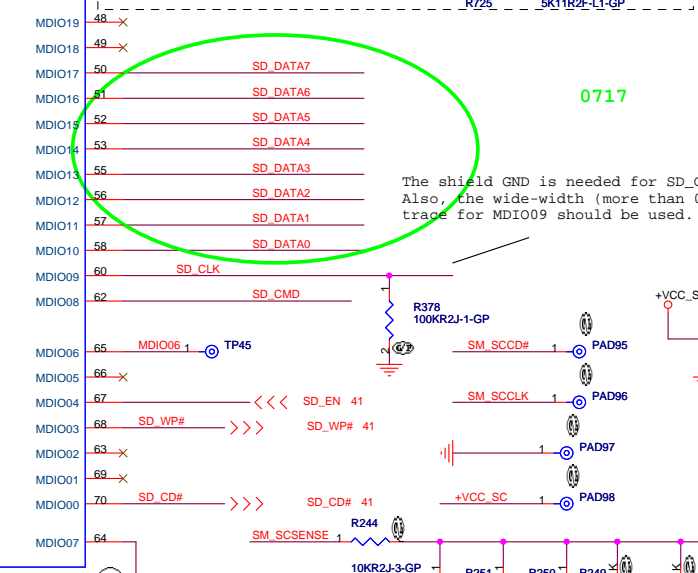
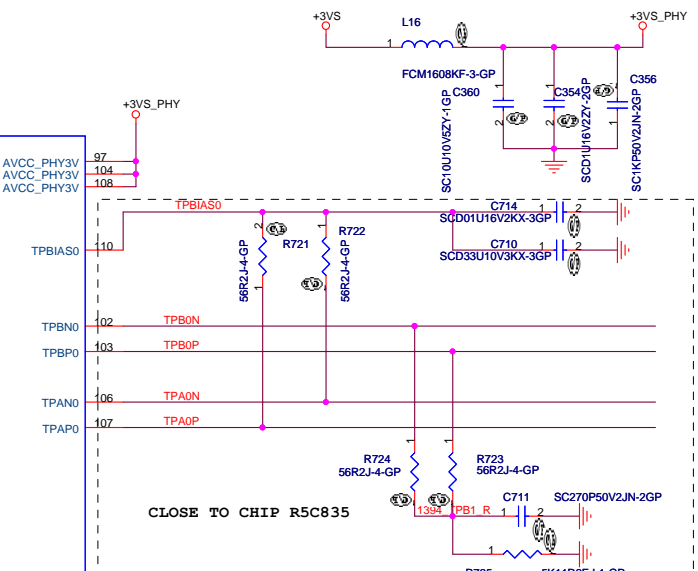
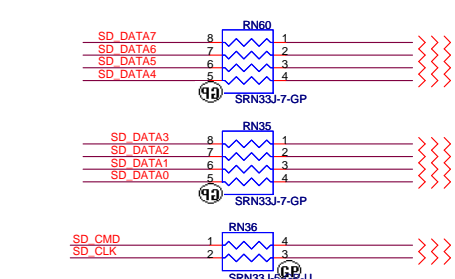




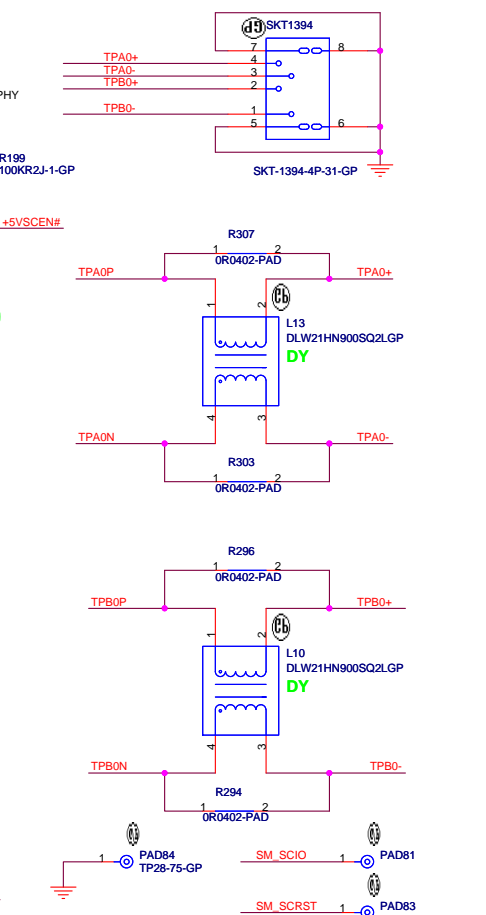
BOM1	
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
R5C835/PCI	
Size A3	Document Number
	KARIA
Date: Friday, May 02, 2008	Rev SC
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Layout notes :
external parts for
VREF, REXT and FIL0 as
close as possible to R5C833.



Layout notes :
1394
=====GND
-----TPB0-
-----TPB0+
=====GND
-----TPA0-
-----TPA0+
=====GND



0717
The shield GND is needed for SD_CLK(MDIO09).
Also, the wide-width (more than 0.02inch)
trace for MDIO09 should be used.

BOM1

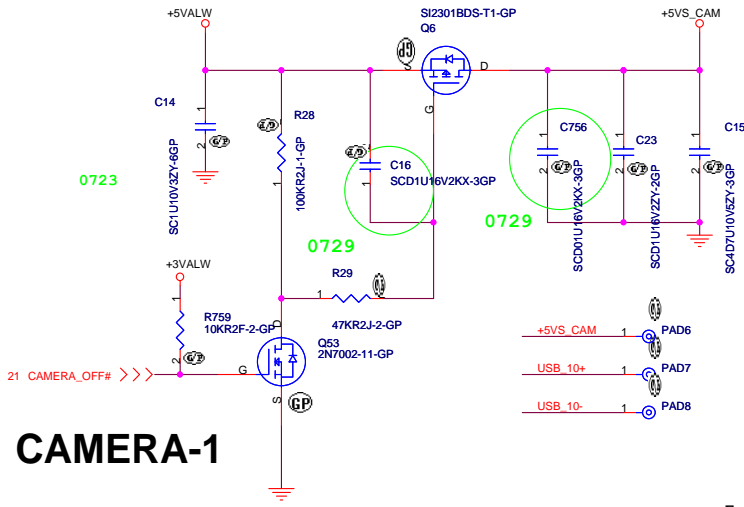
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **R5C835/1394/SD/Smart**

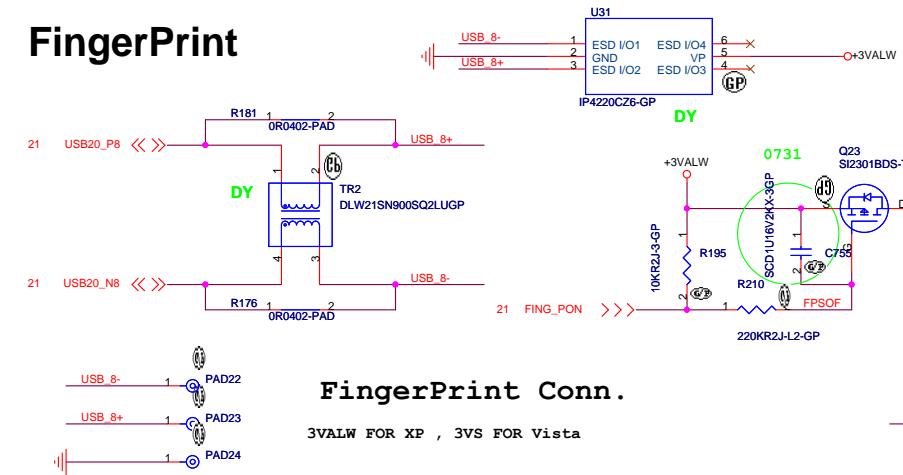
Size A3 Document Number **KARIA** Rev **SA**

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CAMERA-1

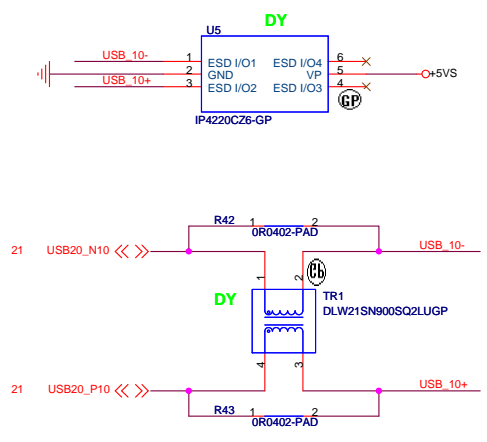


FingerPrint

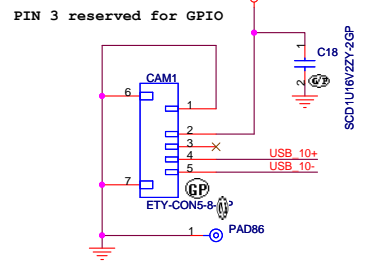


FingerPrint Conn.

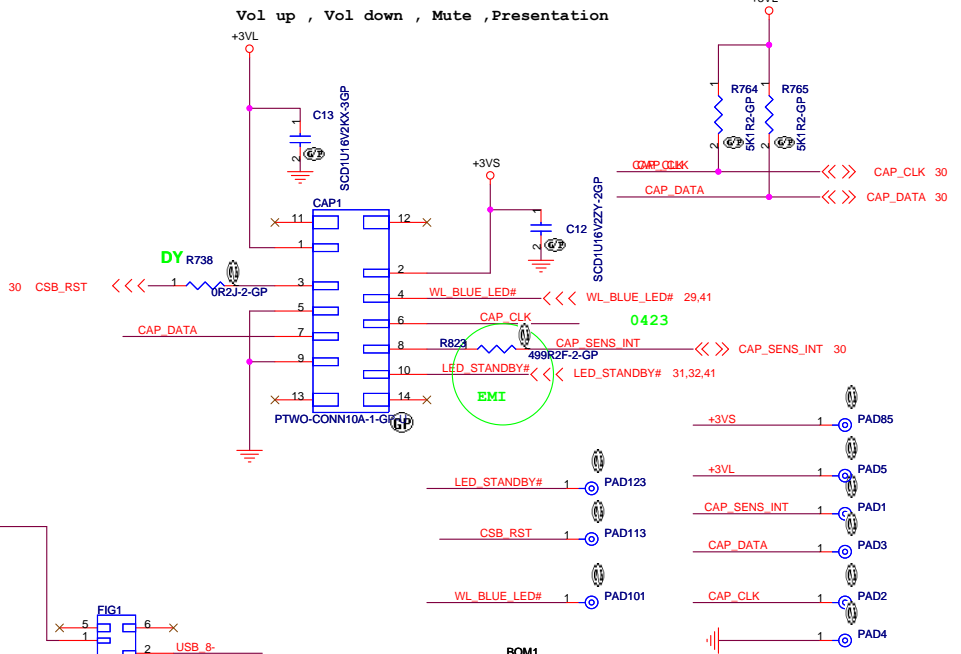
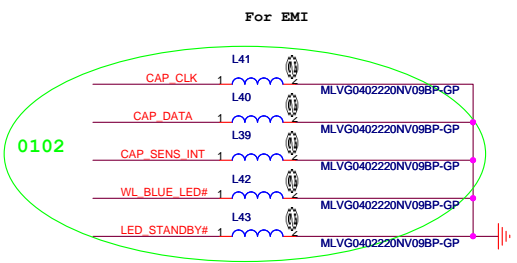
3VALW FOR XP , 3VS FOR Vista



CAMERA-1 Conn.



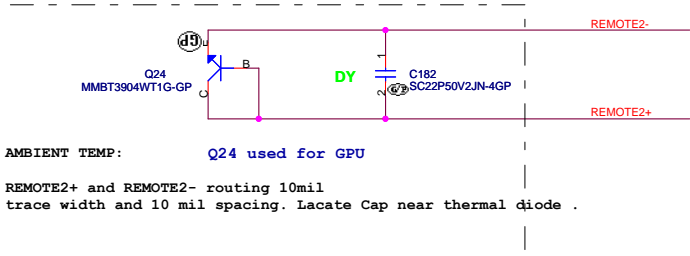
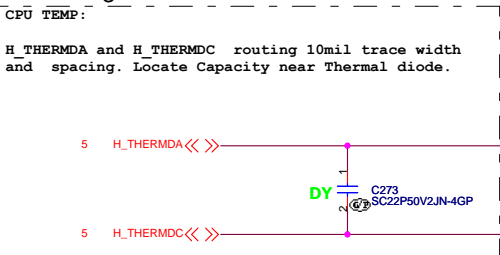
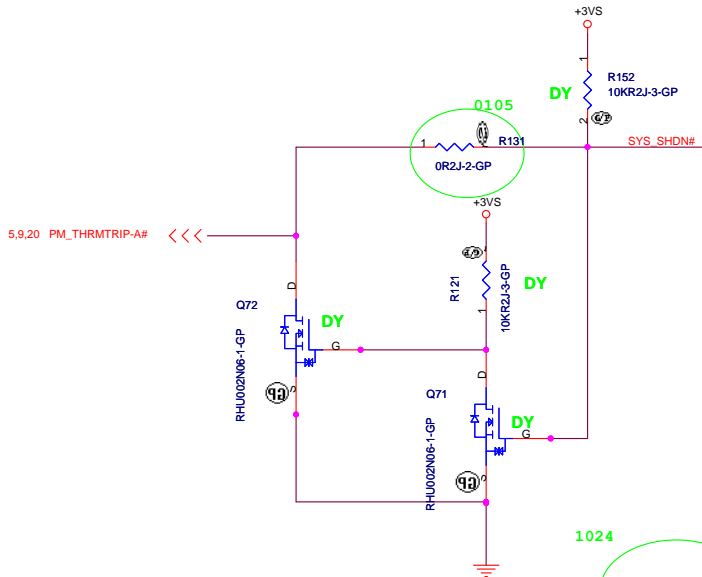
SYSTEM CAPACITY BOARD.



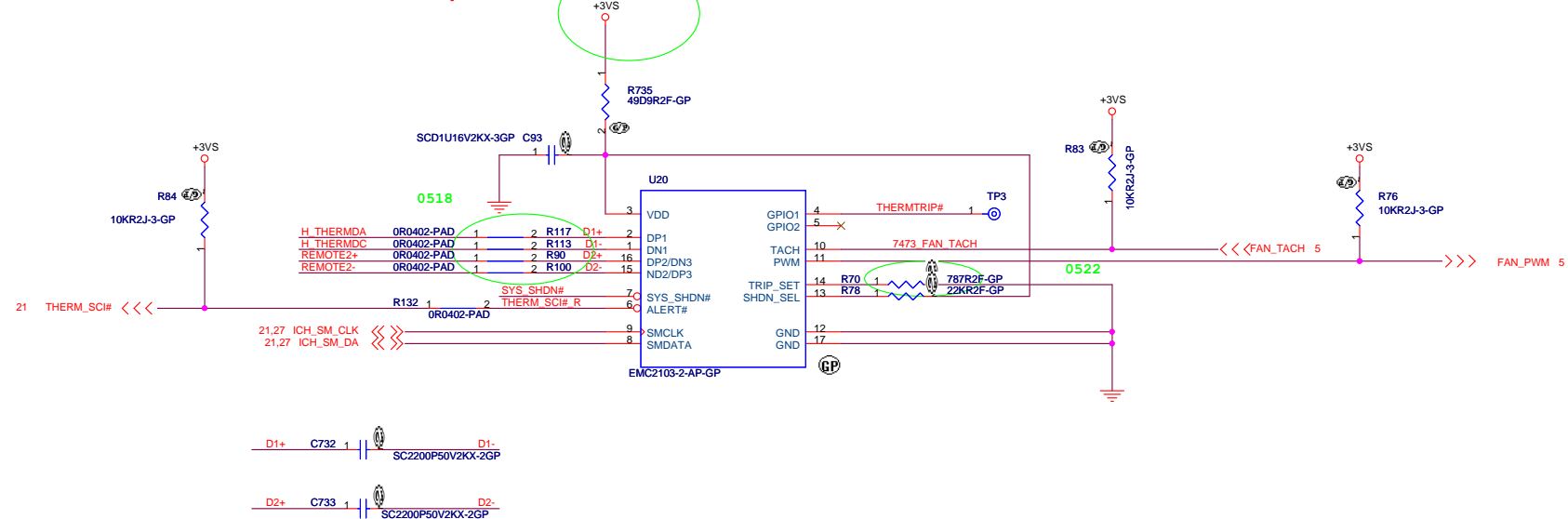
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title	Camera/W-COM		
Size A3	Document Number	KARIA	Rev SC
Date: Friday, May 02, 2008	Sheet 38 of 53		



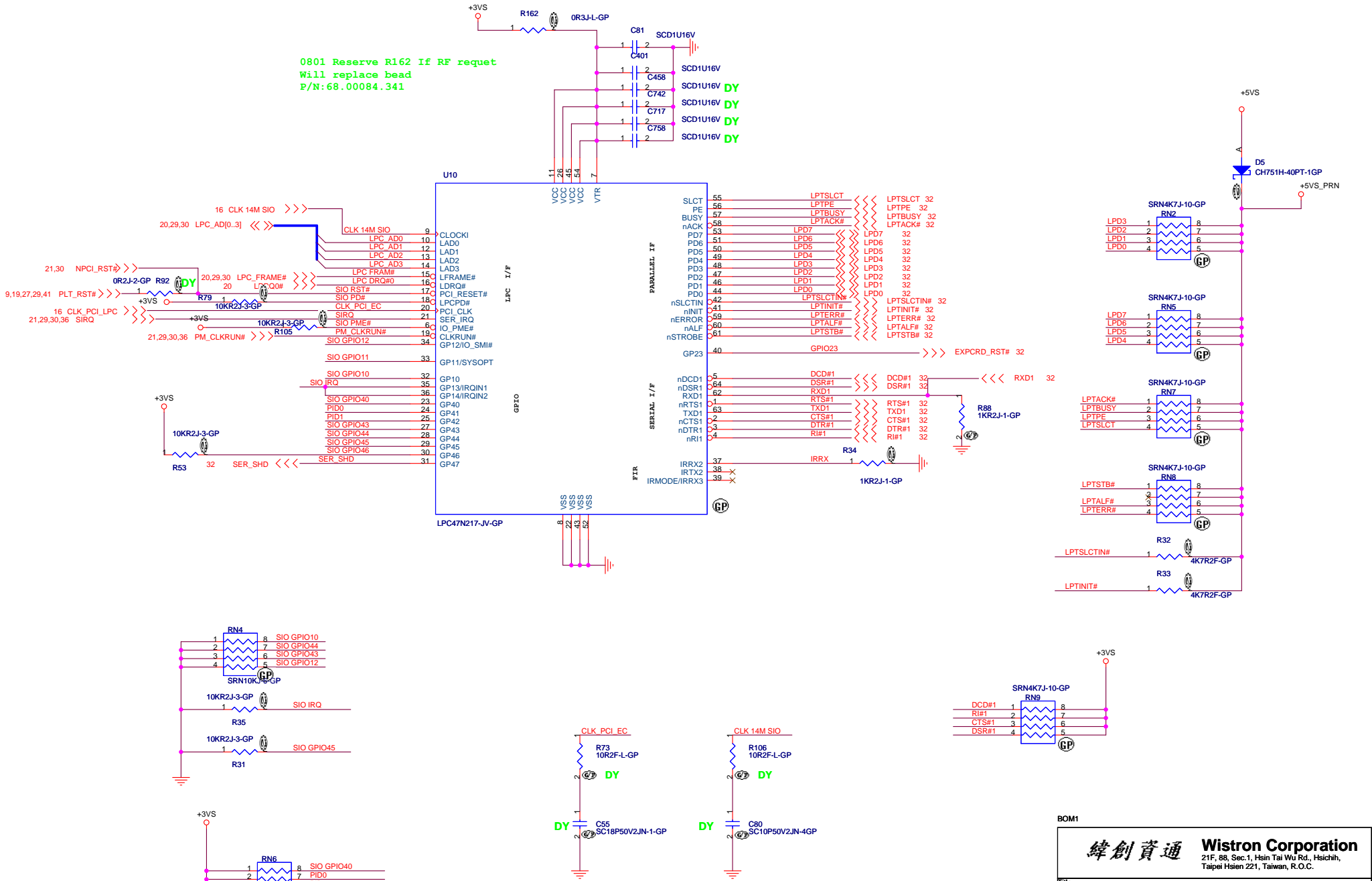
1024 Change Power to 3VS for A009 issue



BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.	
Title			
SMSC2103 Thermal Sensor			
Size	Document Number		Rev
A3	KARIA		SC
Date: Thursday, May 22, 2008		Sheet 39	of 53

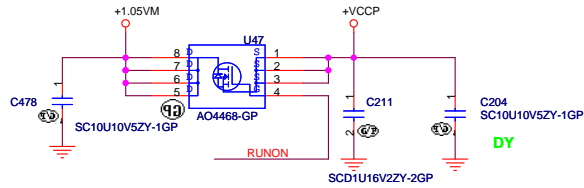
0801 Reserve R162 If RF request
 Will replace bead
 P/N:68.00084.341



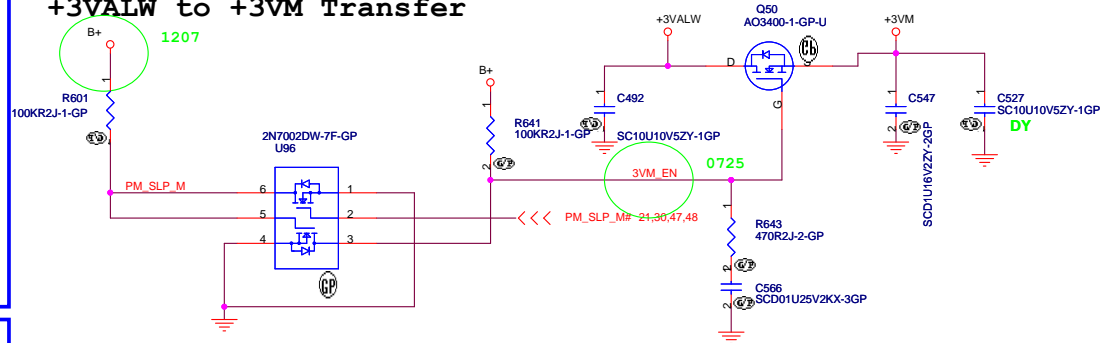
BOM1

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LPC47N217	
Size A3	Document Number KARIA
Date: Friday, May 02, 2008	Sheet 40 of 53
Rev PV	

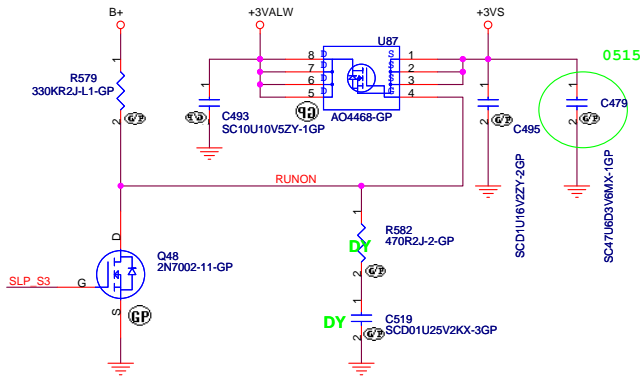
+1.05VM to +VCCP Transfer



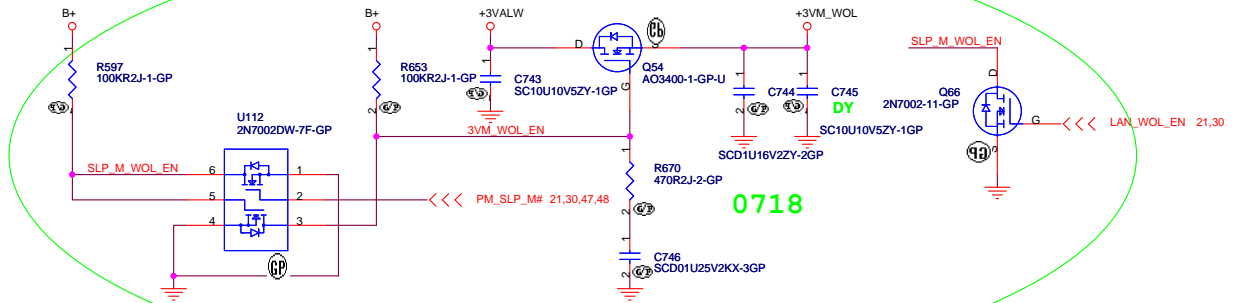
+3VALW to +3VM Transfer



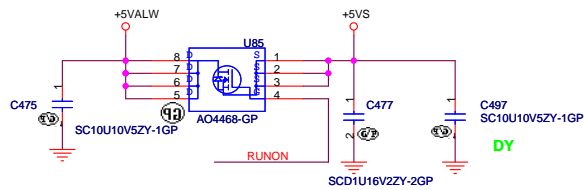
+3VALW to +3VS Transfer



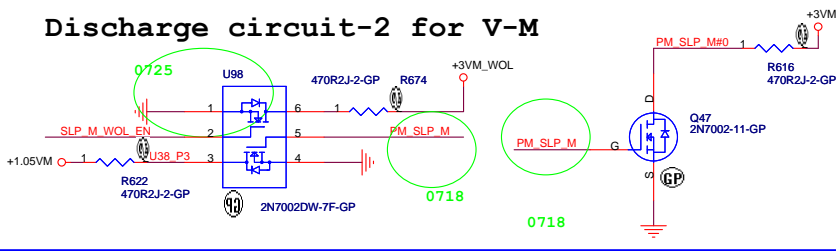
+3VALW to +3VM_WOL



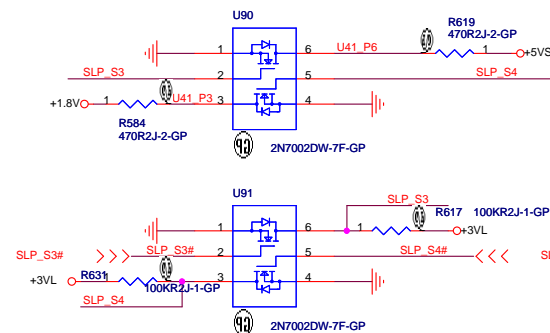
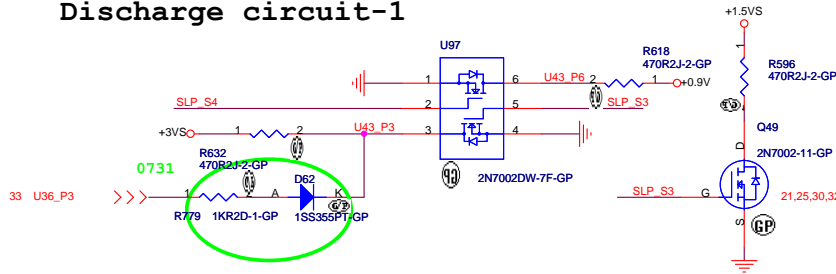
+5VALW to +5VS Transfer



Discharge circuit-2 for V-M



Discharge circuit-1

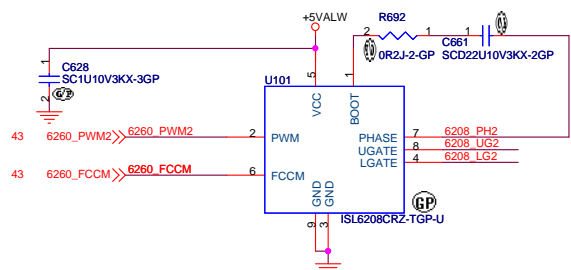


PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM	SYSTEM STATE
0	0	0V	0V	Moff / No WOL
0	1	3.3V	0V	Legacy WOL/ Moiff
1	0	3.3V	3.3V	M1
1	1	3.3V	3.3V	M1

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		DC/DC Circuit	
Size	Document Number	Rev	
A3	KARIA	SC	
Date:	Thursday, May 15, 2008	Sheet	42 of 53

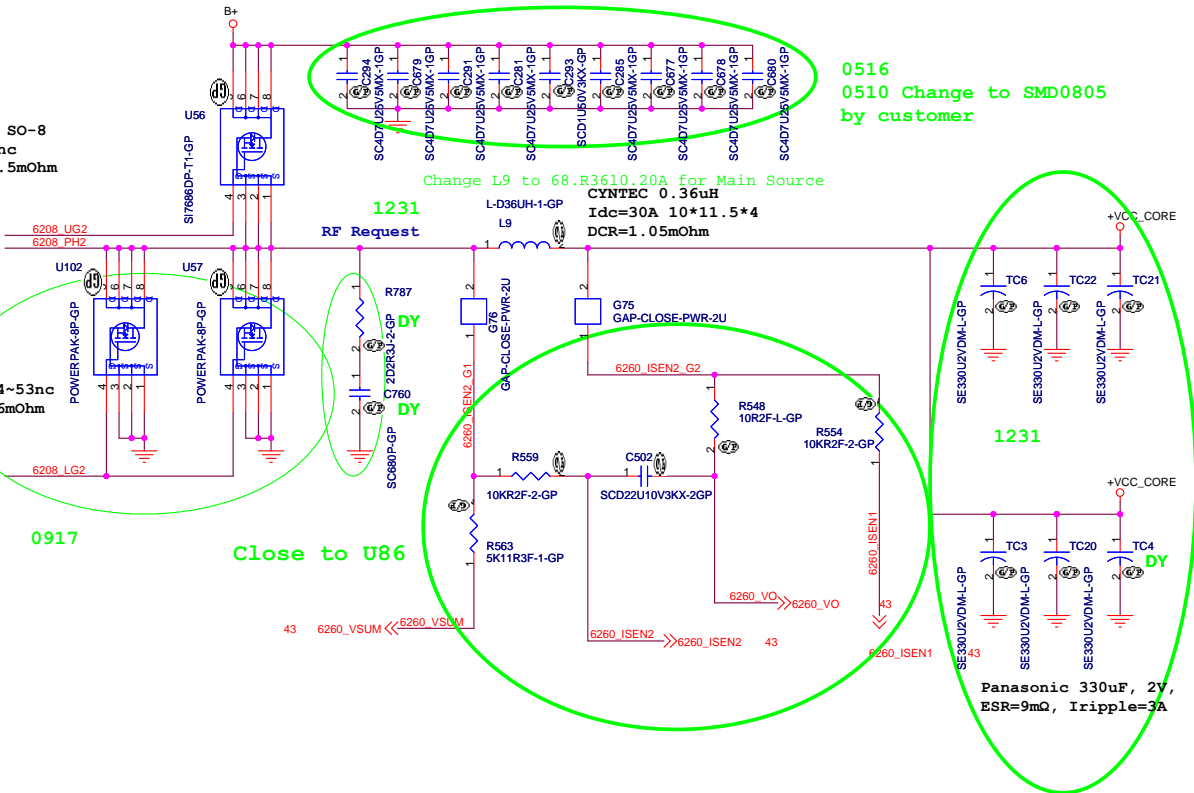


AOL1426 Ultra SO-8
 Id=46A, Qg=10nc
 Rdson=10.2~12.5mOhm

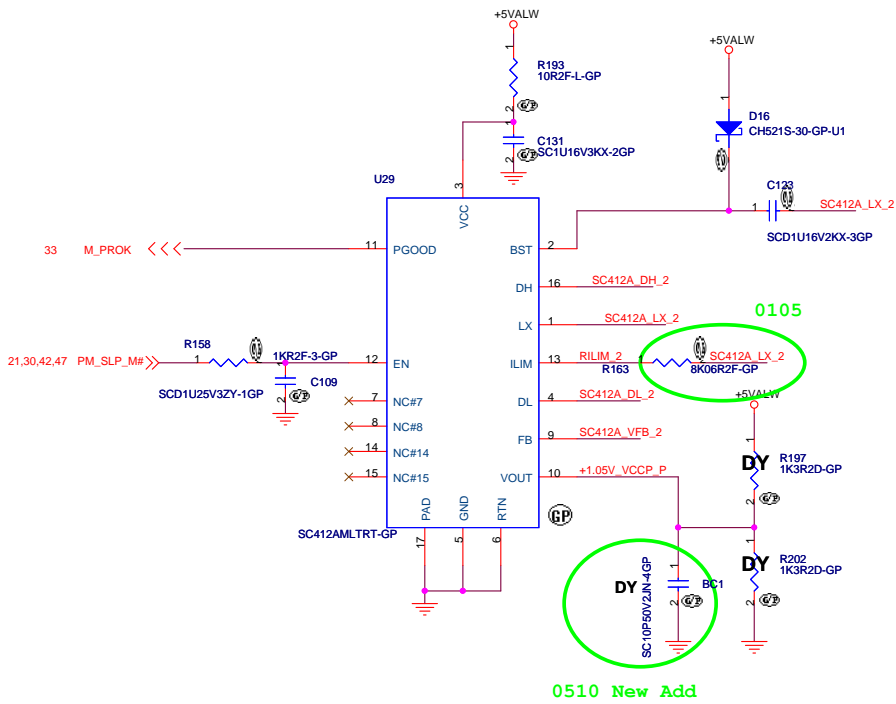
AO4456 SO-8
 Id=20A, Qg=44~53nc
 Rdson=4.5~5.6mOhm

0917

Close to U86

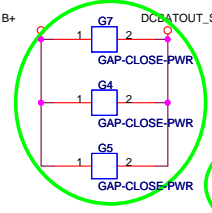


BOM1			
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
ISL6266A CPU CORE(2/2)			
Size	Document Number	Rev	
A3			SC
Date:	Friday, May 02, 2008	Sheet	44 of 53

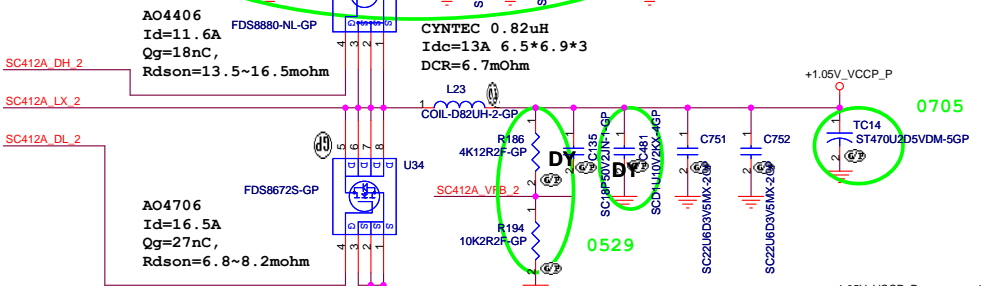


0510 New Add

0105



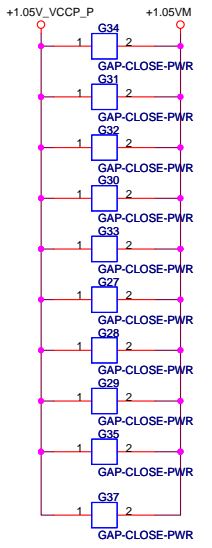
0510



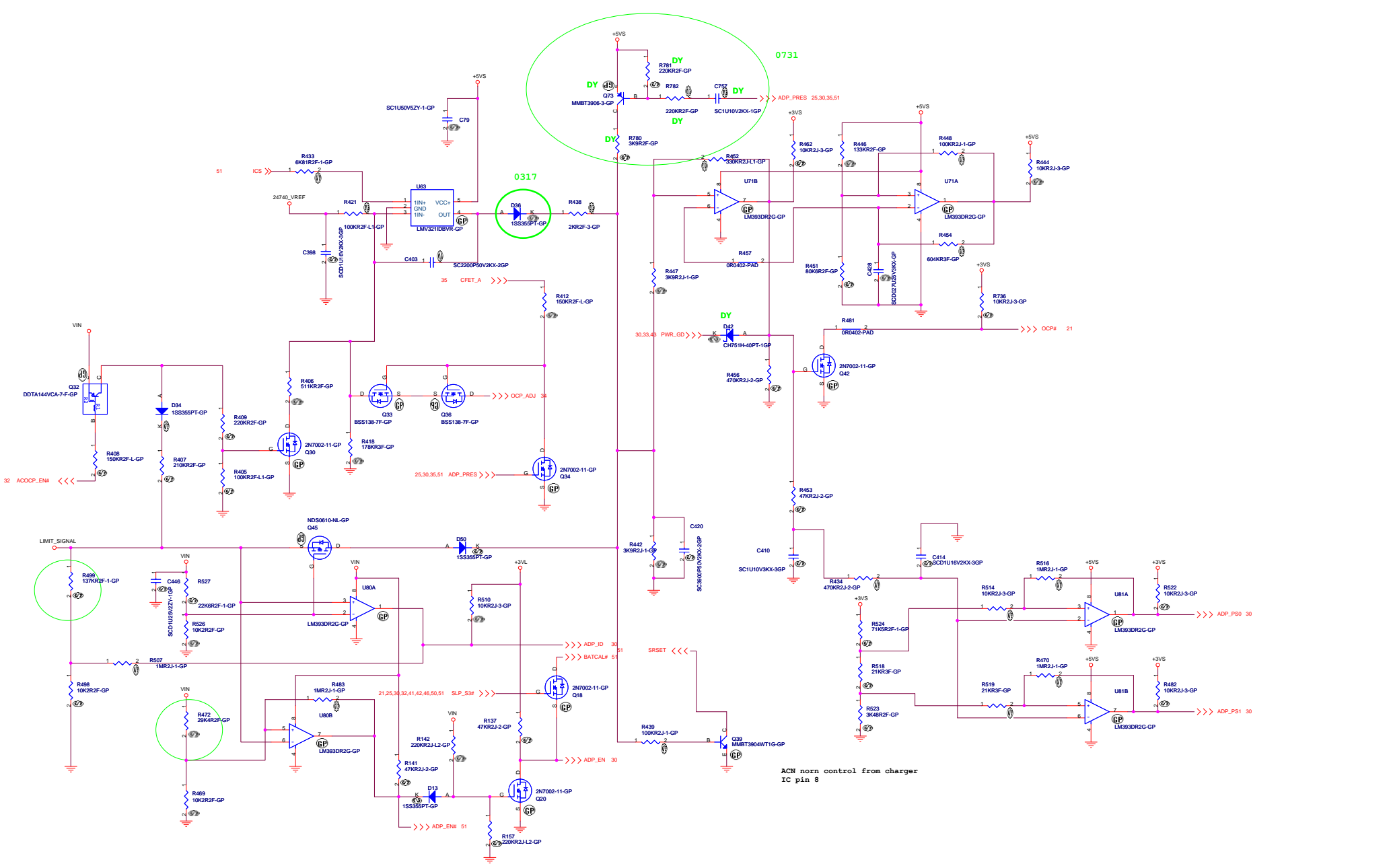
Close to U29 SC412A

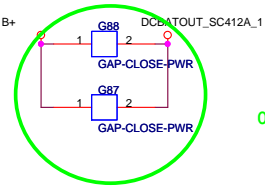
+1.05V_VCCP
I_{omax}=13A
OCP>20A

NEC 470uF 2.5V
ESR=9mOhm
Tripple=3.7A

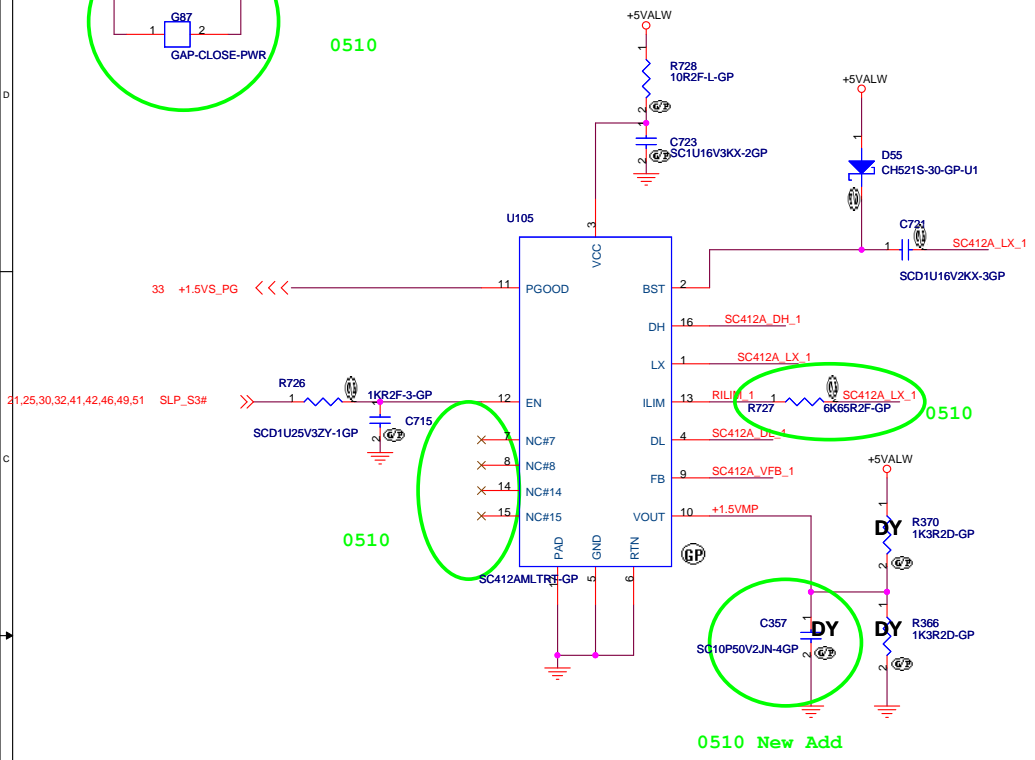


BOM1		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
SC412A +1.05VM		
Size	Document Number	Rev
A3	Karia	SC
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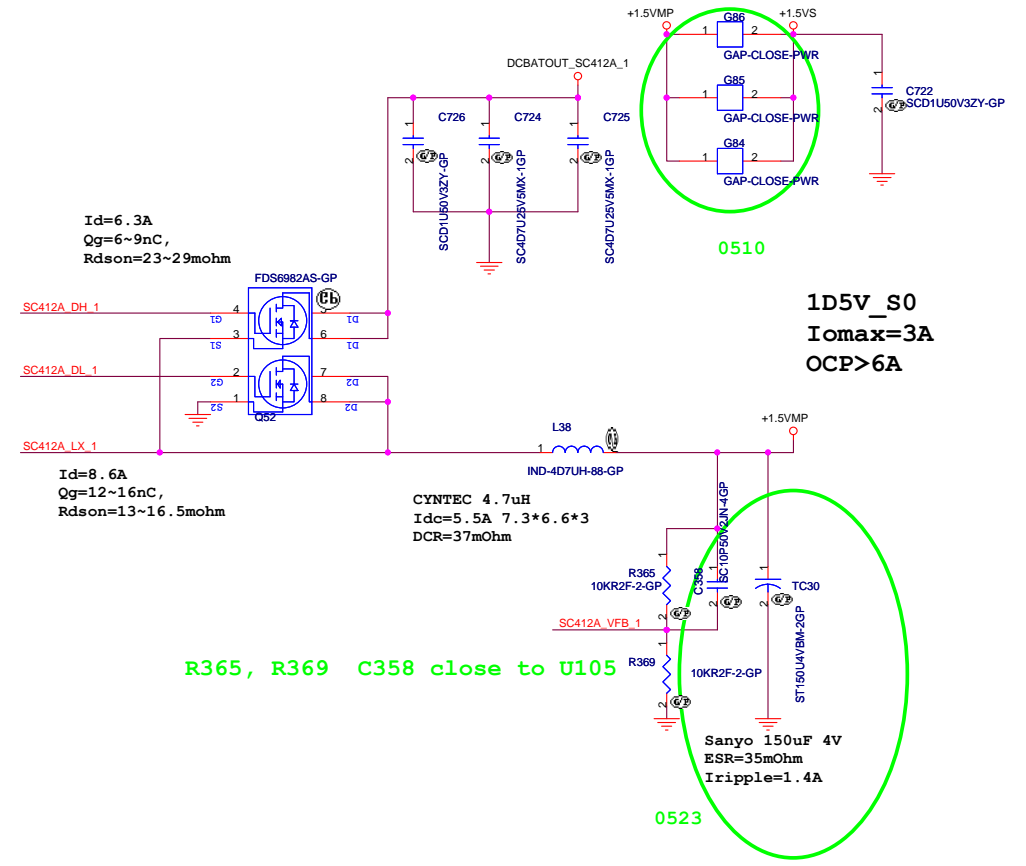


0510



0510

0510 New Add



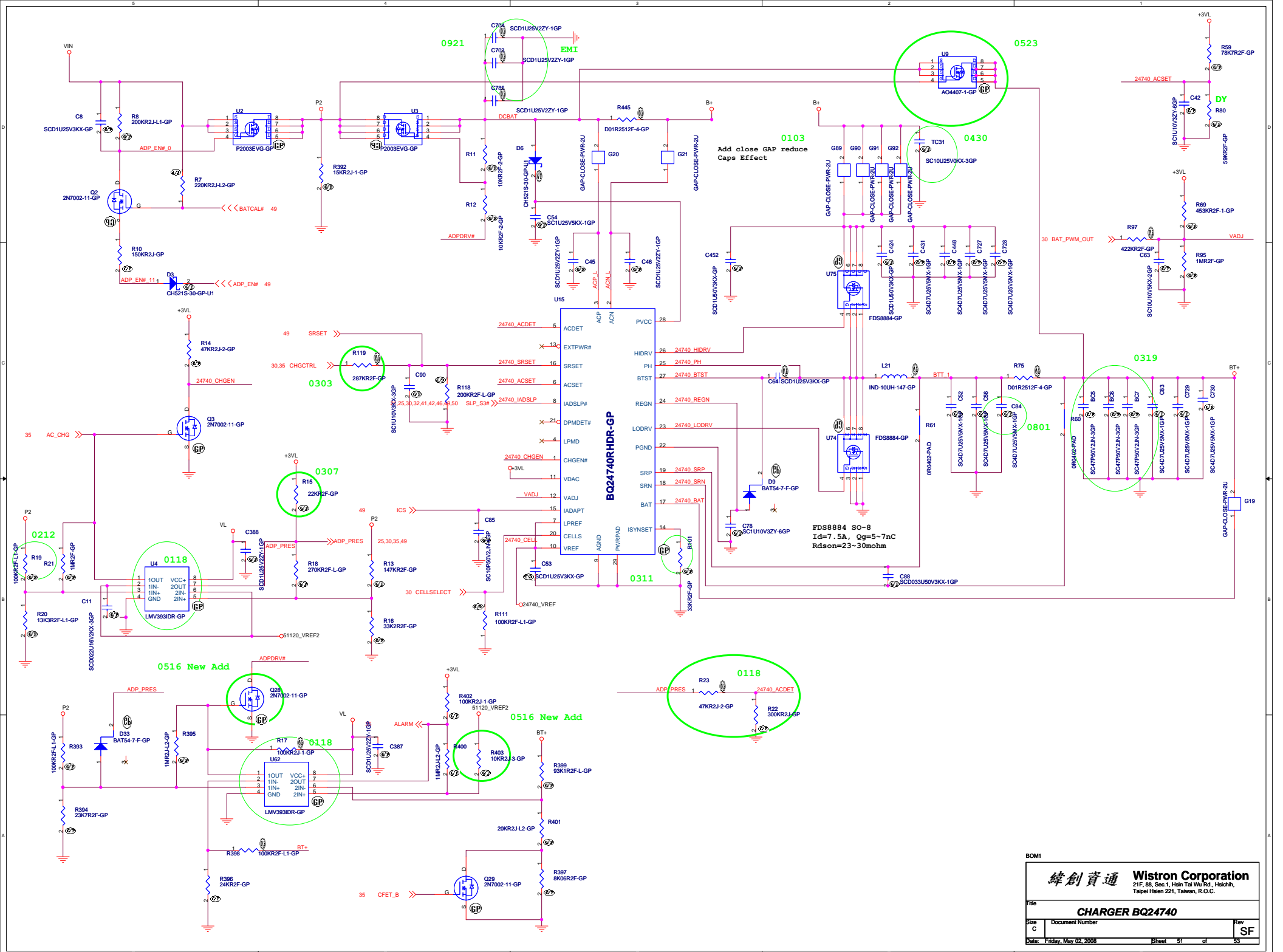
0510

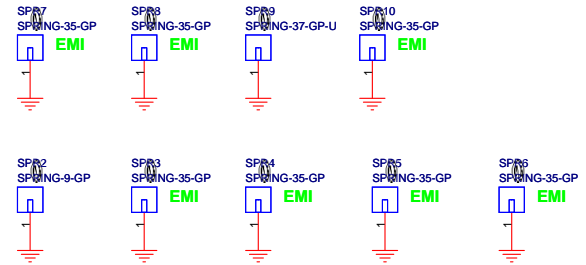
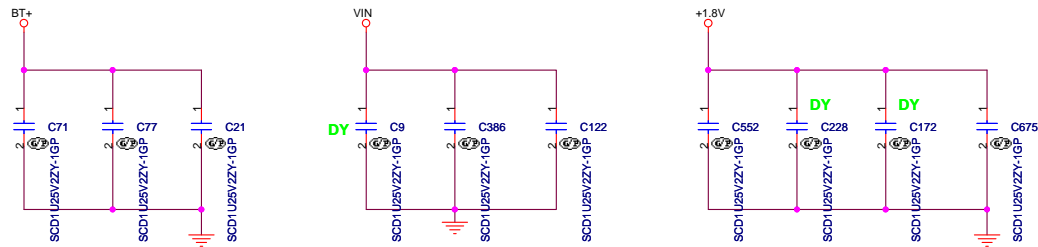
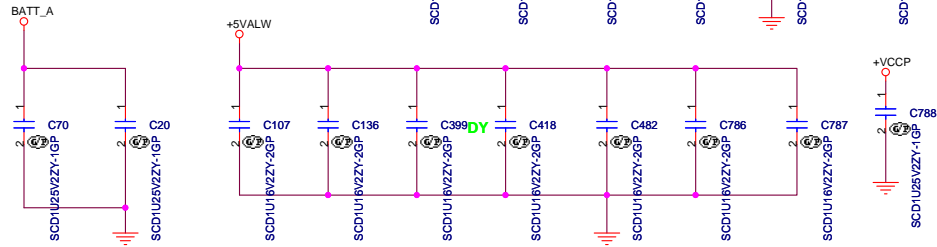
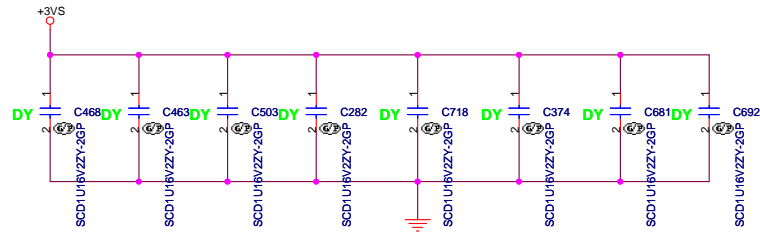
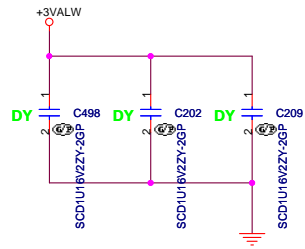
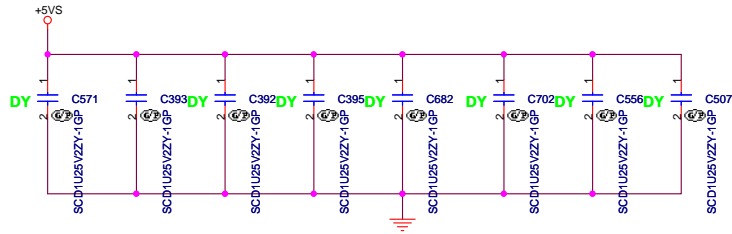
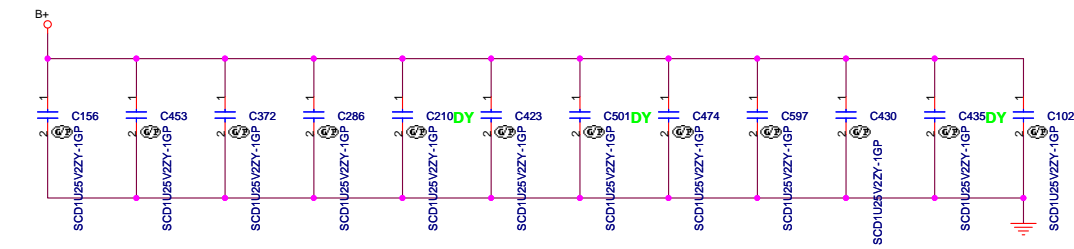
1D5V_S0
I_{omax}=3A
OCP>6A

R365, R369 C358 close to U105

0523

BOM1		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SC412A +1.5VS			
Size A3	Document Number	Rev	
	Karia	SC	
Date: Friday, May 02, 2008	Sheet 50	of	53

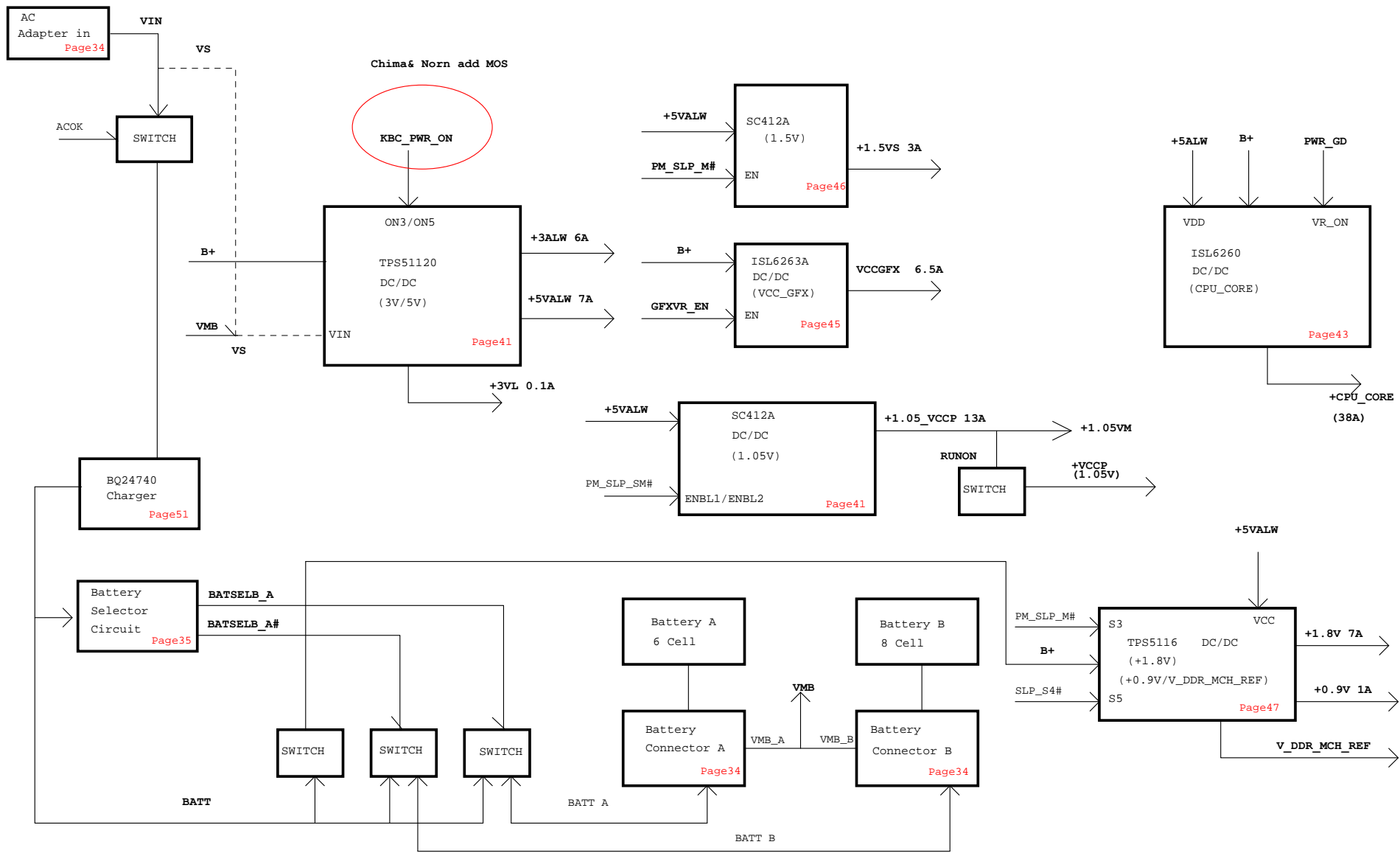




BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	EMI CAPS	
Size	Document Number	Rev
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BOM1

緯創資通		Wistron Corporation	
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>			
Title			
Power Block Diagram			
Size A3	Document Number KARIA		Rev SC
Date: Wednesday, January 02, 2008		Sheet 53	of 53