

IMG5 17" REV E

11/01/05

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
E		408158	PRODUCTION RELEASED	DATE	DATE
				11/01/05	?

D

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

PDF	CSA	CONTENTS	SYNC MASTER	DATE
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88	154	AUDIO: POWER SUPPLIES	FINO-SO	10/07/2005

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<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <p style="text-align: center;">  <small>THIRD ANGLE PROJECTION</small> </p>	<p>METRIC</p>	 Apple Computer Inc.
<p style="font-size: x-small;">DRAPTER <input type="checkbox"/> DESIGN CK <input type="checkbox"/></p> <p style="font-size: x-small;">ENG APPD <input type="checkbox"/> MFG APPD <input type="checkbox"/></p> <p style="font-size: x-small;">QA APPD <input type="checkbox"/> DESIGNER <input type="checkbox"/></p> <p style="font-size: x-small;">RELEASE <input type="checkbox"/> SCALE NONE <input type="checkbox"/></p> <p style="font-size: x-small;">MATERIAL/FINISH NOTED AS APPLICABLE</p>		<p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p>I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p>II. NOT TO REPRODUCE OR COPY IT</p> <p>III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p>
		<p>TITLE</p> <p style="font-size: large;">SCH, MLB, IMG5, 17</p>
		<p>DRAWING NUMBER 051-6790 REV. E</p> <p style="font-size: x-small; text-align: right;">SHT 1 OF 154</p>

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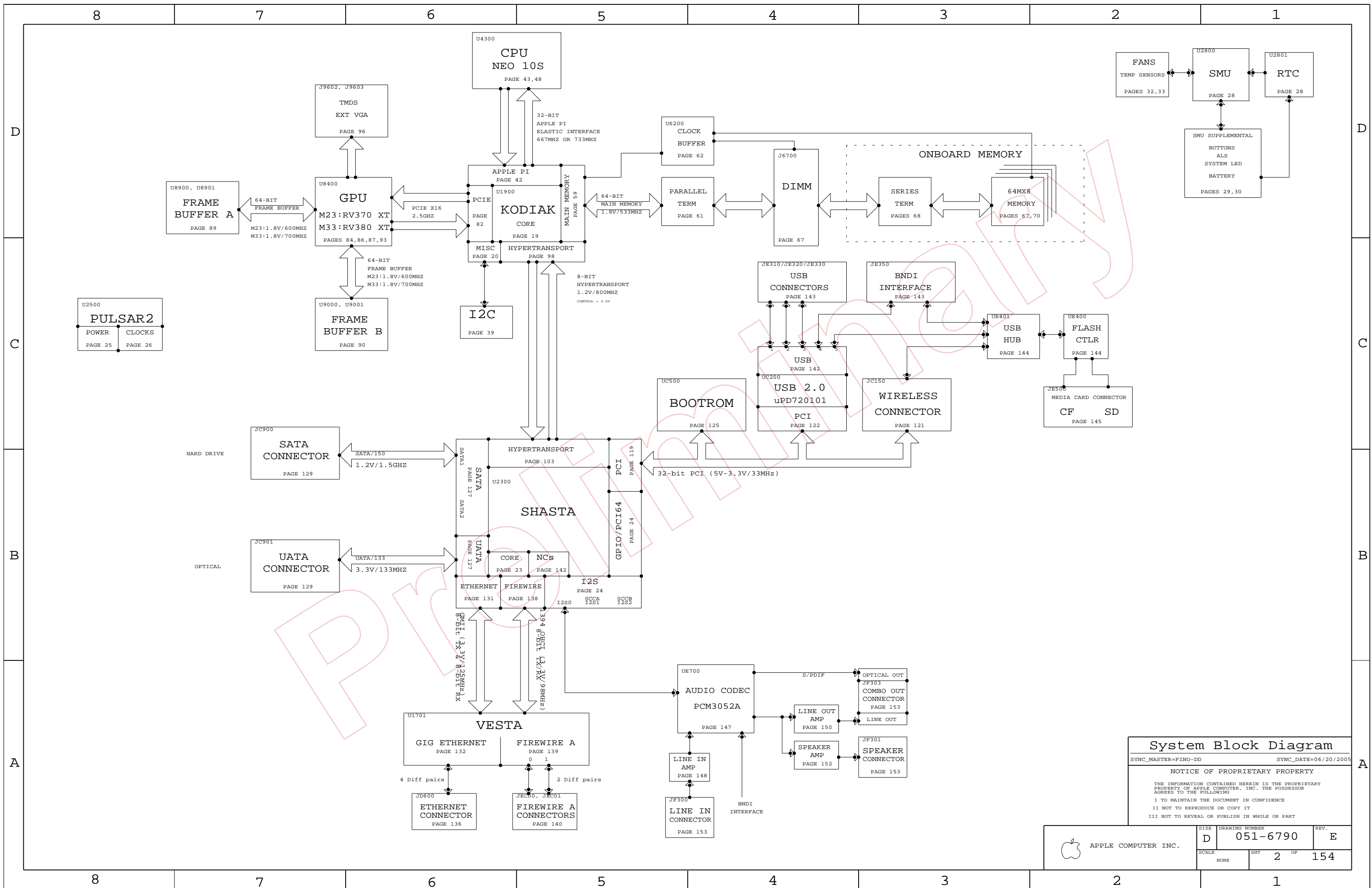
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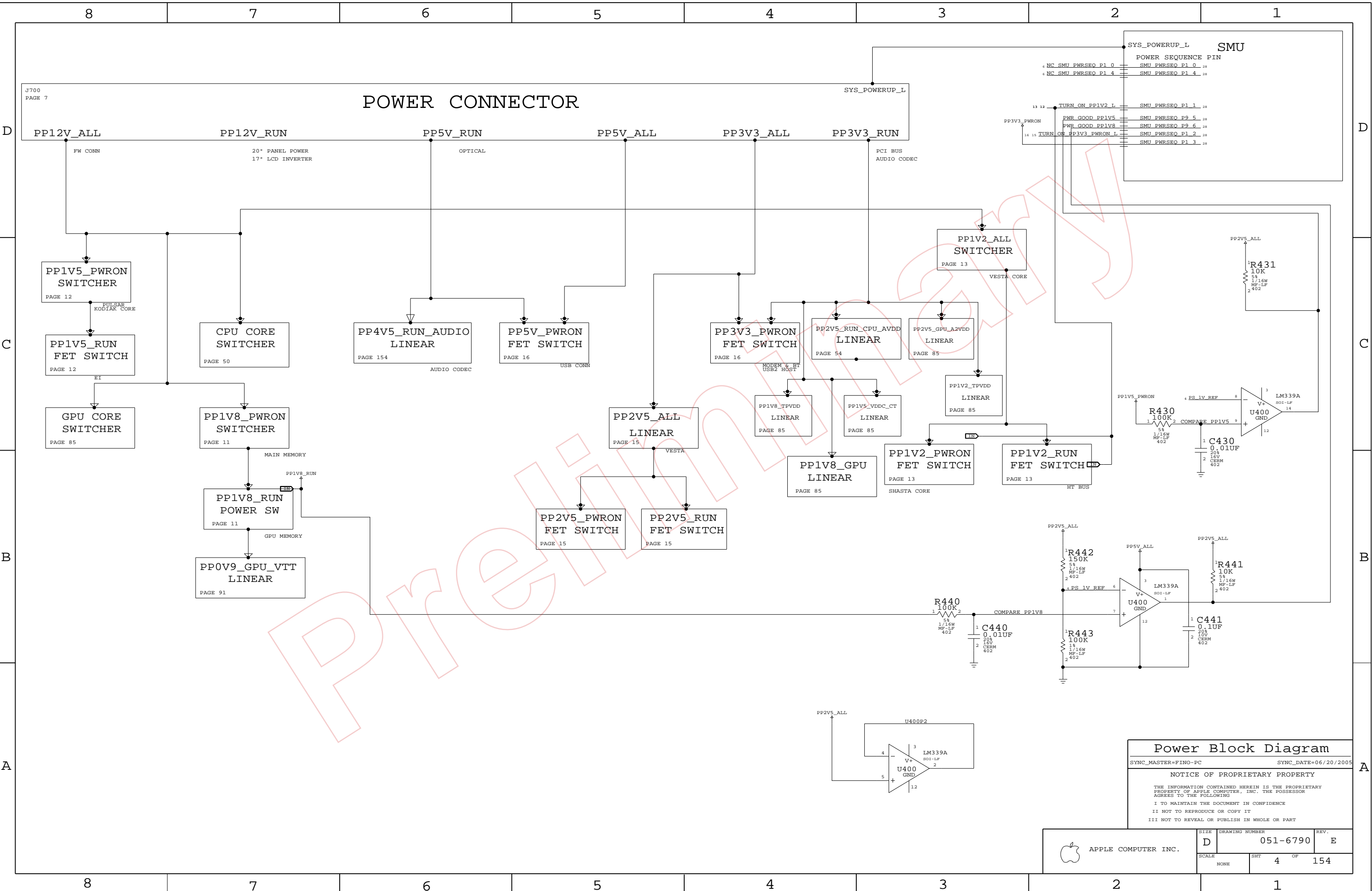
System Block Diagram

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

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NONE			



Power Block Diagram

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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NONE			

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PROCESSORS

NEED TO UPDATED BIN CODES AS NOTES

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION	
337S3224	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,1.9G,85C	1.9GHZ	1.10V	45W	50MV	U4300	17_INCH_LCD	CRITICAL
337S3220	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.1G,85C	2.1GHZ	1.10V	45W	50MV	U4300	20_INCH_LCD	CRITICAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3225	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.15V
337S3226	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.20V
337S3227	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.25V
337S3228	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.15V
337S3229	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.20V
337S3230	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.25V
337S3231	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.30V
337S3221	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.15V
337S3222	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.20V
337S3223	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
343S0379	1	IC,KODIAK,V1.2,PBGA,200MM	U1900		CRITICAL
343S0377	1	IC,ASIC,SHASTA,V1.1,PBGA,LF	U2300		CRITICAL
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U1701		CRITICAL
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500		CRITICAL

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
051-6790	1	PCB,SCHM,MLB,M23	SCH1	17_INCH_LCD	
051-6863	1	PCB,SCHM,MLB,M33	SCH1	20_INCH_LCD	
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD	CRITICAL
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD	CRITICAL
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VFP1		
825-6447	1	BARCODE LABEL, MLB	LBL1		
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500		CRITICAL
341T1752	1	PURCH ASSY, SMU BIG	U2800		CRITICAL
603-7318	1	M23 CPU HEATSINK	MECH1	OMIT	CRITICAL
603-7321	1	M33 CPU HEATSINK	MECH1	OMIT	CRITICAL
603-7319	1	M23 GPU HEATSINK	MECH2	OMIT	CRITICAL HEATSINKS ARE NOW ON THE PD BOM
603-7322	1	M33 GPU HEATSINK	MECH2	OMIT	CRITICAL
603-7320	1	M23 NB HEATSINK	MECH3	OMIT	CRITICAL
603-7323	1	M33 NB HEATSINK	MECH3	OMIT	CRITICAL
875-1905	1	CPU GAP FILLER	GAP1		
875-2429	1	LED COVER TAPE	TAPE1	17_INCH_LCD	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0140	378S0141		LED700,LED700	KINGBRIGHT LED
343S0388	343S0356		U1701	VESTA A4
126S0078	126S0086		C722	EL CAP
126S0068	126S0088		CF000	EL CAP
353S1321	353S1105		U400	LM339
138S0558	138S0547			10UF CAP ALL LOC.
124-0338	124-0333			PANASONIC CAPS

Preinitial

Table Items

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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NONE	5	154

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NO TEST XW NETS

Table of test nets for column 8, including items like GND U1100, GND U1200, GND U1300, etc.

Table of test nets for column 7, including items like GND GPU TPVSS, GND GPU TVSSR, GND GPU VSSDI, etc.

Table of test nets for column 6, including items like GND NEC AVSS R, GND AUDIO SPKRAMP PLANE, GND AUDIO CODEC, etc.

Table of test nets for column 5, including items like KOD H05 GND, KOD K07 GND, KOD G10 GND, etc.

Table of test nets for column 4, including items like TP FBBCS1 L, AUD 4V5 FB, ITS RUNNING, etc.

Table of test nets for column 3, including items like TP USB2 PWREN<0>, TP USB2 PWREN<1>, TP SB FSTEST, etc.

FUNC TEST NETS

NOTES FROM TOM FUSSELMAN
PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

Table of functional test nets for column 3, including items like FUNC_TEST=TRUE PPVCORE_CPU, FUNC_TEST=TRUE PP3V3_ALL_SMU, etc.

Table of functional test nets for column 3, including items like FUNC_TEST=TRUE SMU_BOOT_SCLK, FUNC_TEST=TRUE SMU_BOOT_RXD, etc.

EE IDENTIFIED NO TEST NETS

Table of EE identified test nets for column 8, including items like NC EI_NB_TO_CPU_B_CLK_P, NC EI_NB_TO_CPU_B_CLK_N, etc.

Table of EE identified test nets for column 7, including items like KPVDD2, KPGND2, CPU DIODE POS, etc.

Table of EE identified test nets for column 6, including items like RFBDC<126>, RFBDC<125>, RFBDC<124>, etc.

Table of EE identified test nets for column 5, including items like RFBDC<119>, RFBDC<118>, RFBDC<117>, etc.

Table of EE identified test nets for column 4, including items like RFBDC<16>, RFBDC<15>, RFBDC<14>, etc.

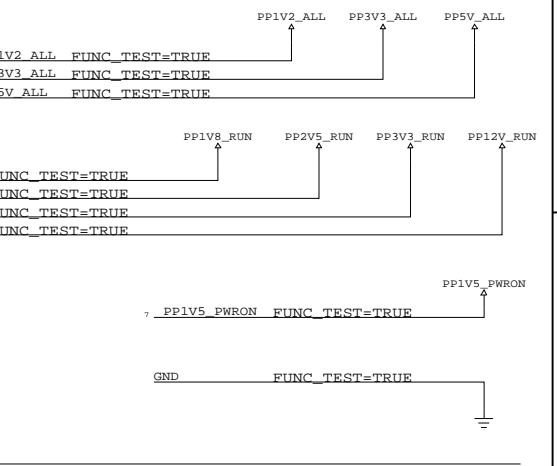


Table of EE identified test nets for column 8, including items like NC NB_CPU_A1_INT_L, NC NB_CPU_B0_INT_L, NC NB_CPU_B1_INT_L, etc.

Table of EE identified test nets for column 7, including items like NC I2S2_MCLK, NC SATA_RXD_N2_C, NC SATA_RXD_P2_C, etc.

Table of EE identified test nets for column 6, including items like RFBDC<110>, RFBDC<109>, RFBDC<108>, etc.

Table of EE identified test nets for column 5, including items like RFBDC<106>, RFBDC<105>, RFBDC<104>, etc.

Table of EE identified test nets for column 4, including items like RAM_DQ_R<60>, RAM_DQ_R<59>, RAM_DQ_R<58>, etc.

Table of EE identified test nets for column 8, including items like RFBDC<38>, RFBDC<37>, RFBDC<36>, etc.

Table of EE identified test nets for column 7, including items like RFBDC<54>, RFBDC<53>, RFBDC<52>, etc.

Table of EE identified test nets for column 6, including items like RFBDC<72>, RFBDC<71>, RFBDC<70>, etc.

Table of EE identified test nets for column 5, including items like RFBDC<67>, RFBDC<66>, RFBDC<65>, etc.

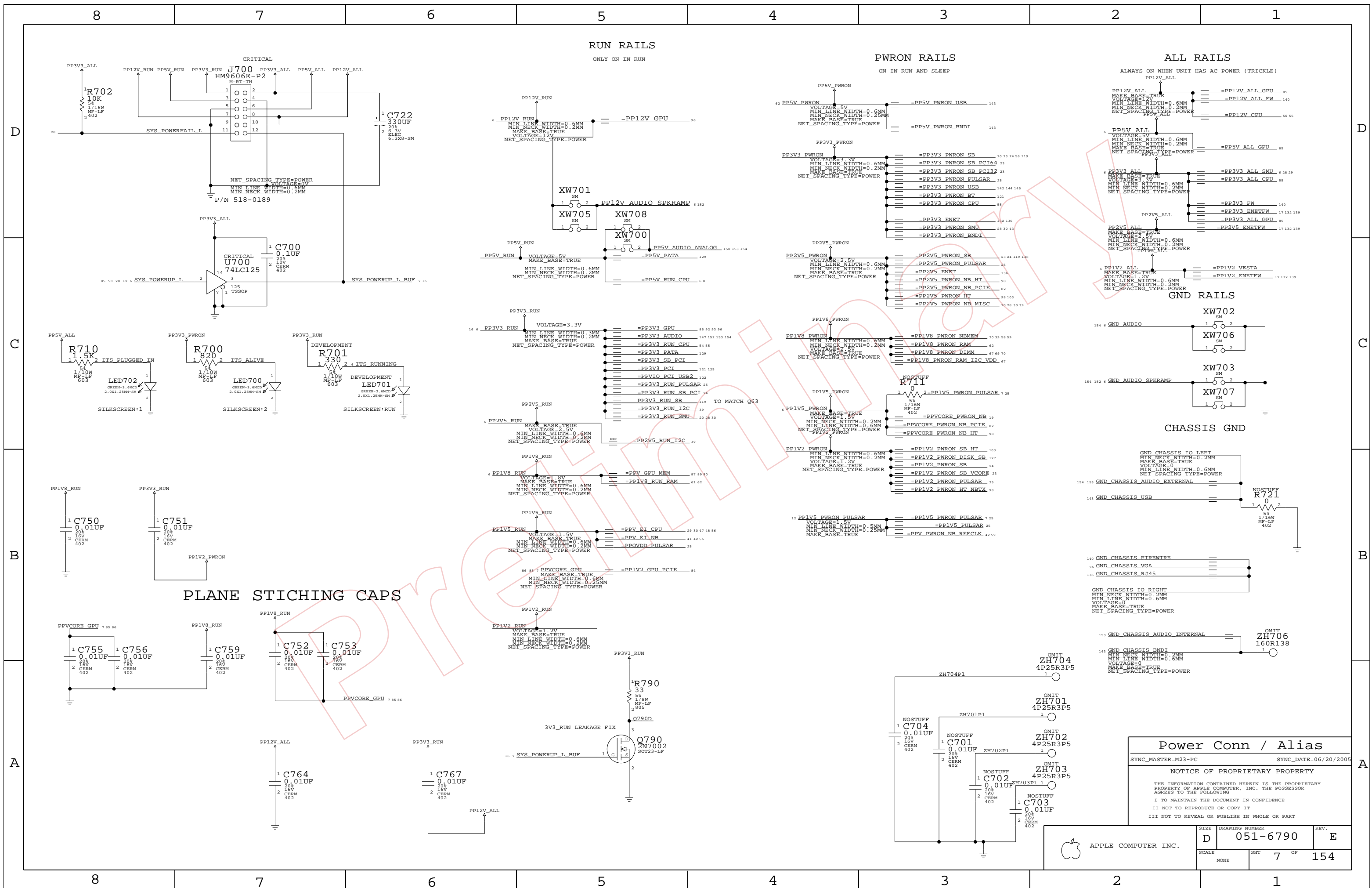
Table of EE identified test nets for column 4, including items like RAM_DQ_R<22>, RAM_DQ_R<21>, RAM_DQ_R<20>, etc.

FUNC TEST 1 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

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Power Conn / Alias

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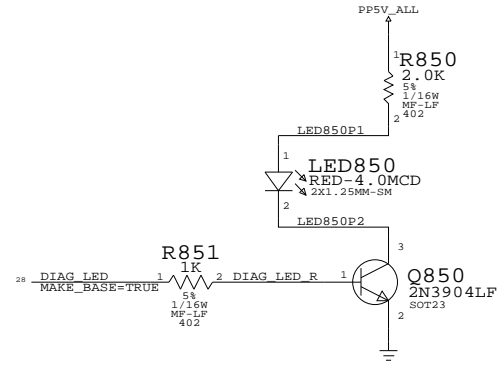
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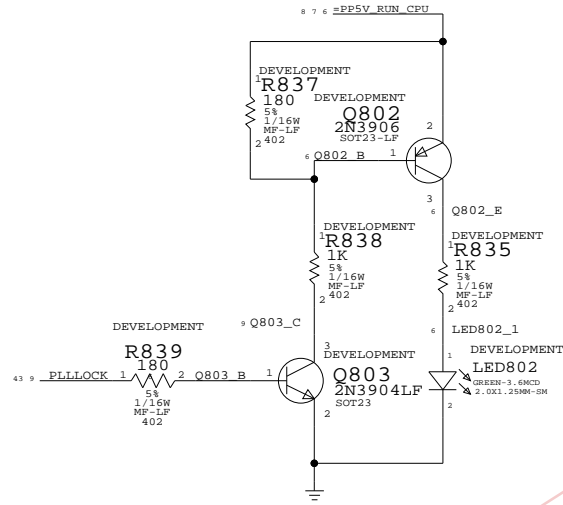
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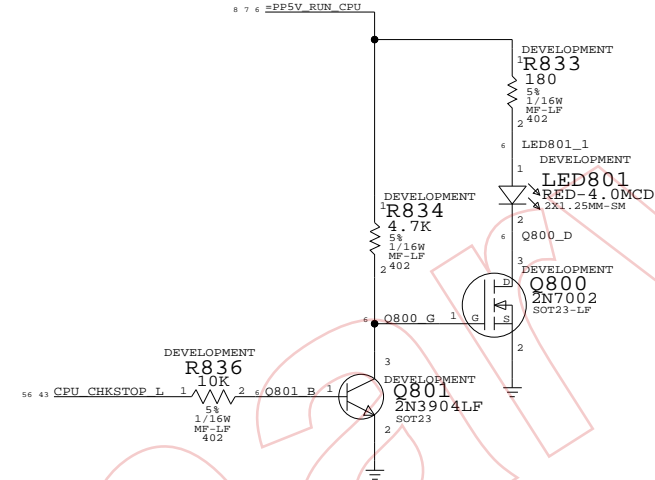
DIAG LED (OVERTEMP LED)



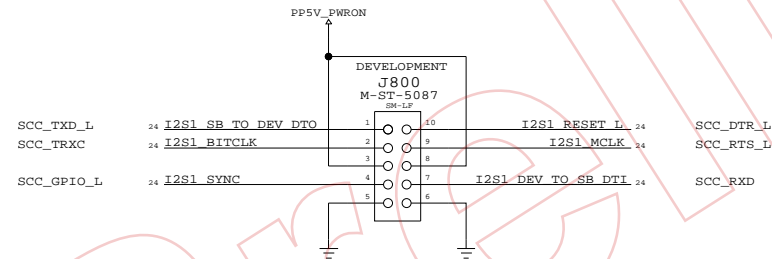
PLL LOCK LED



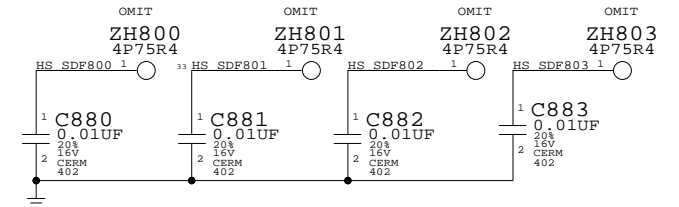
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

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THE FOLLOWING NETS ARE USED ONLY WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

THE FOLLOWING NETS DO NOT HAVE TEST POINT BECAUSE OF ROUTING DENSITY AND SIGNAL INTEGRITY. TEST COVERAGE WILL BE BY FCT NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

Table of test points and nets for column 8, including items like ENET_TXD_R<7>, TP_VESTA_TVCO_24, TP_VESTA_TXC_RXC_DELAY, etc.

Table of test points and nets for column 5, including items like Q803_C, PLLLOCK, LED_PPIV8_RUN_P, PULSAR_1V5_RUN_SWITCH, etc.

THE FOLLOWING PULSAR NETS WILL BE TESTED VIA TEST JET

Table of test points and nets for column 4, including items like CPU_A_TBN_CLK_R, CPU_B_TBN_CLK_R, CPU_A_APSYNC_R, etc.

Table of test points and nets for column 3, including items like 100M_N<0>, 100M_P<0>, CKA_N<0>, HT_NB_N<0>, HT_NB_P<0>, etc.

ADDING NO_TEST TO ALL PCIE NETS TO AVOID STUBS WILL GET COVERAGE IN FCT WITH A DIAG THAT CHECKS THAT THE BUS IS 16 LANES WIDE

Table of test points and nets for column 3, including items like PCIE_NB_TO_SLOTA_NF<0..15>, PCIE_NB_TO_SLOTA_P<0..15>, etc.

JTAG TEST POINTS NEED TO BE ON THE BOTTOM OF THE BOARD ADDING FUNC_TEST=TRUE TO THESE NETS

Table of test points and nets for column 2, including items like TP_JTAG_SB_TCK, TP_JTAG_SB_TDI, TP_JTAG_SB_TDO, etc.

Table of test points and nets for column 2, including items like JTAG_NB_TCK, JTAG_NB_TDI, JTAG_NB_TDO, etc.

Table of test points and nets for column 2, including items like TP_JTAG_VESTA_TDI, TP_JTAG_VESTA_TDO, TP_JTAG_VESTA_TCK, etc.

Table of test points and nets for column 2, including items like JTAG_CPU_TCK, JTAG_CPU_TDI, JTAG_CPU_TDO, etc.

FUNC TEST 2 OF 2

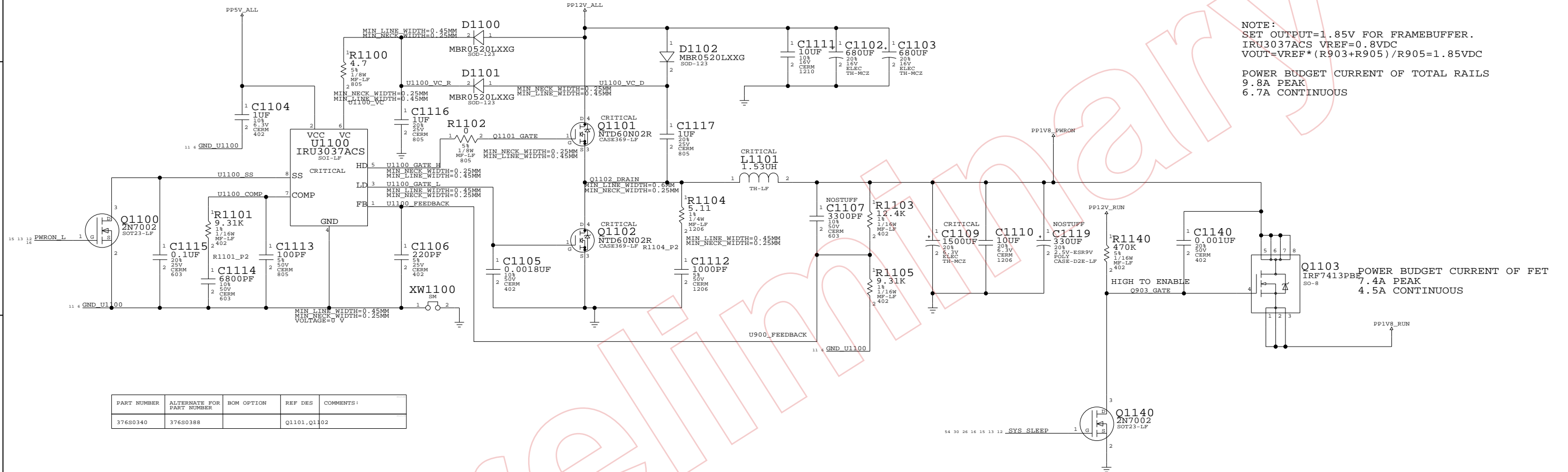
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1.8V VOLTAGE REGULATOR



NOTE:
 SET OUTPUT=1.85V FOR FRAMEBUFFER.
 IRU3037ACS VREF=0.8VDC
 $V_{OUT} = V_{REF} * (R_{903} + R_{905}) / R_{905} = 1.85VDC$
 POWER BUDGET CURRENT OF TOTAL RAILS
 9.8A PEAK
 6.7A CONTINUOUS

POWER BUDGET CURRENT OF FET
 7.4A PEAK
 4.5A CONTINUOUS

1.8V Vreg

SYNC_MASTER=M23-PC SYNC_DATE=06/20/2005

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	D	051-6790	E
SCALE	SHT	11 OF	154
NONE			

KODIAK CORE VOLTAGE REGULATOR

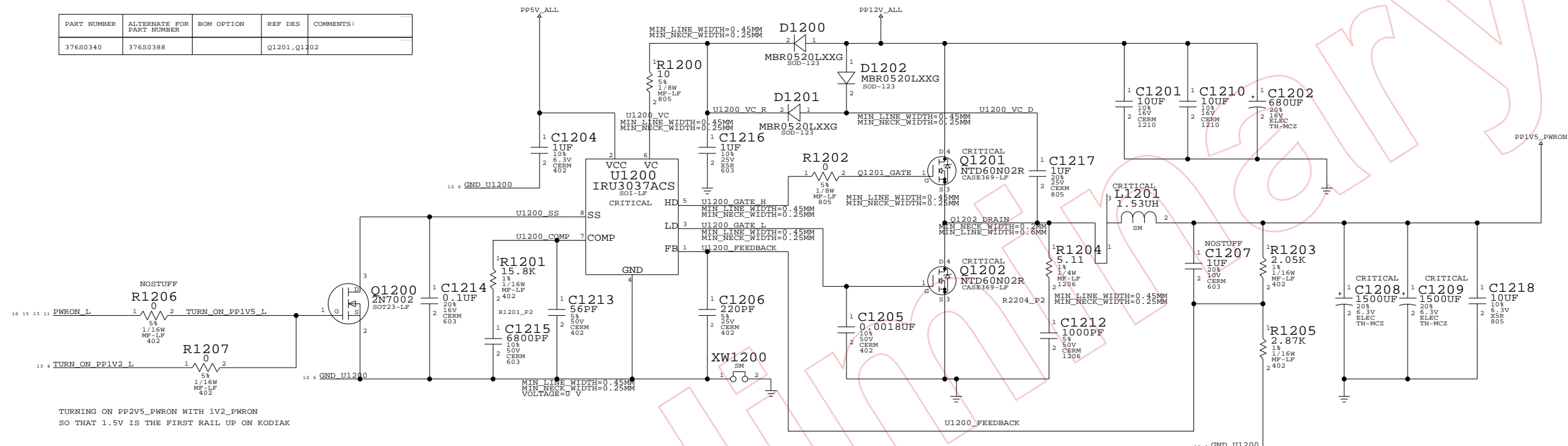
NOTE:

IRU3037ACS VREF=0.8VDC
 $V_{OUT} = V_{REF} * (R_{1203} + R_{1205}) / R_{1205} = 1.25VDC$

LOAD FROM POWER BUDGET
 8.5A PEAK CURRENT DRAW
 7.2A CONTINUOUS CURRENT DRAW

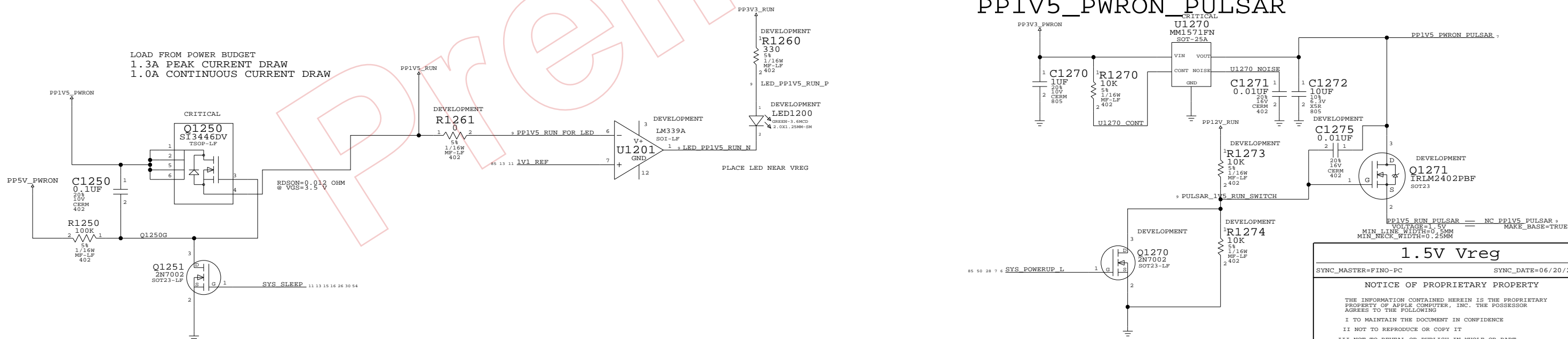
1.35V R1205=2.87K
 1.30V R1205=3.24K
 1.25V R1205=3.65K

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1201, Q1202	



TURNING ON PP2V5_PWRON WITH 1V2_PWRON
 SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

PP1V5_PWRON_PULSAR



LOAD FROM POWER BUDGET
 1.3A PEAK CURRENT DRAW
 1.0A CONTINUOUS CURRENT DRAW

1.5V Vreg

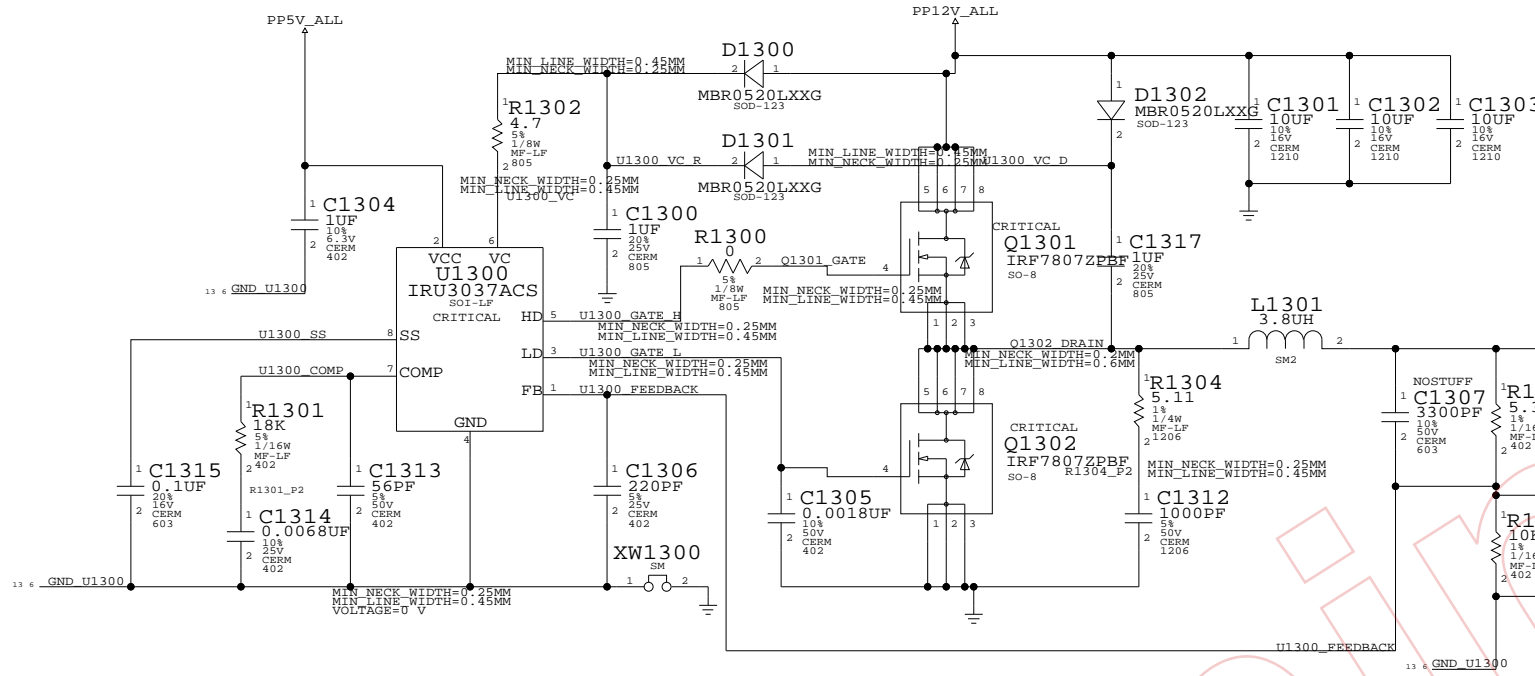
SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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SCALE	SHT	12 OF	154
NONE			

PP1V2_ALL VOLTAGE REGULATOR



NOTE:
 SET OUTPUT=1.22-1.23V
 IRU3037ACS VREF=0.8VDC
 $V_{OUT}=V_{REF} * (R1003+R1005)/R1005=1.22-1.23VDC$

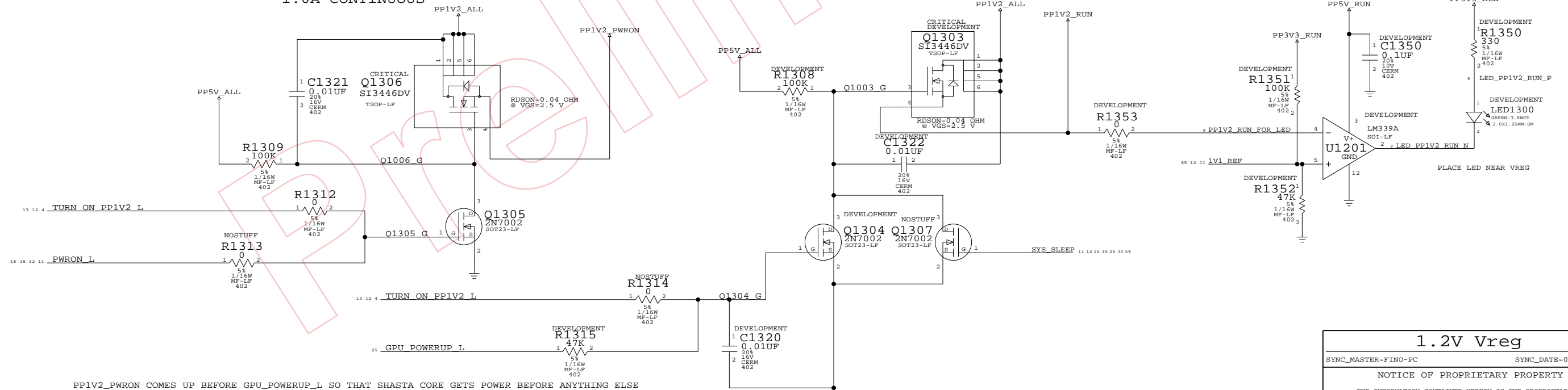
POWER BUDGET CURRENT OF TOTAL RAILS
 3.2A PEAK
 2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

PEAK CURRENT 1.3A
 1.0A CONTINUOUS

PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

1.2V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

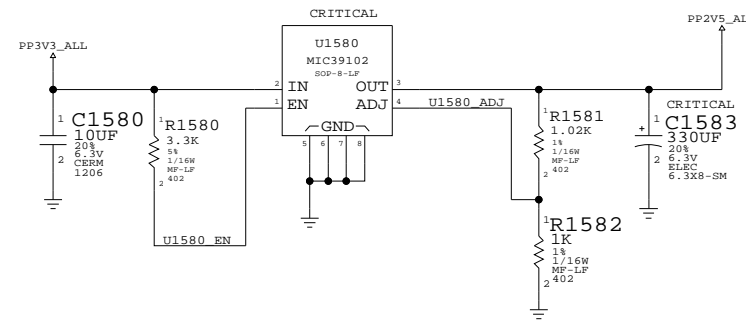
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NONE			

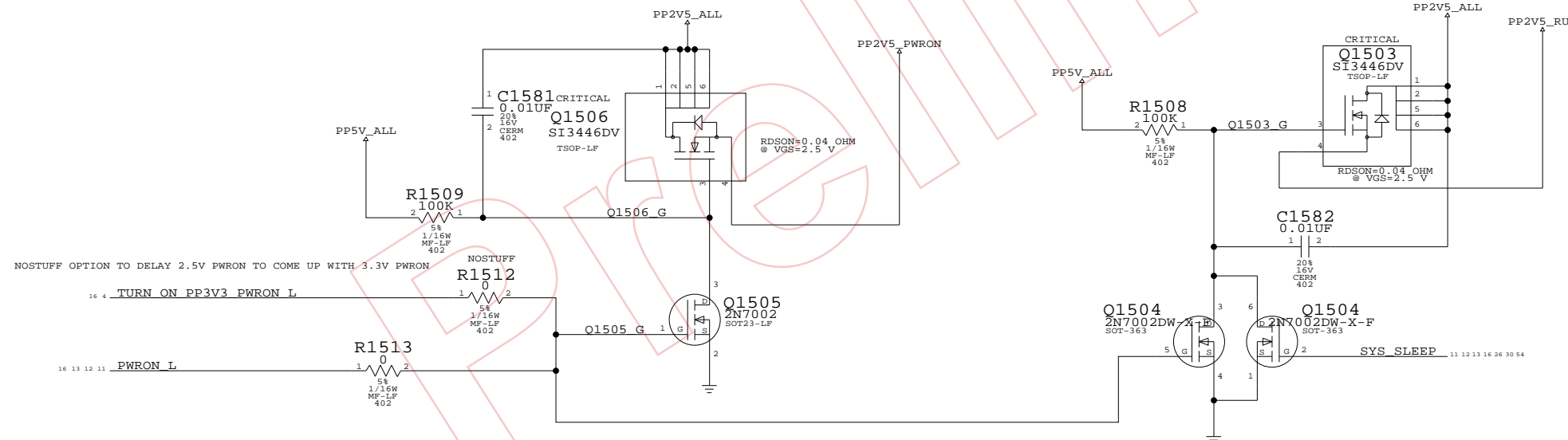
PP2V5_ALL VOLTAGE REGULATOR

NOTE:
 SET OUTPUT=2.5V
 IRU3037CS VREF=1.24VDC
 $V_{OUT} = V_{REF} * (R_{1581} + R_{1582}) + 1 = 5.505VDC$
 POWER BUDGET CURRENT OF TOTAL RAILS
 0.2A PEAK
 0.1A CONTINUOUS



PP2V5_PWRON FET SWITCH PEAK CURRENT 0.1A

PP2V5_RUN FET SWITCH PEAK CURRENT 0.1A



2.5V Vreg

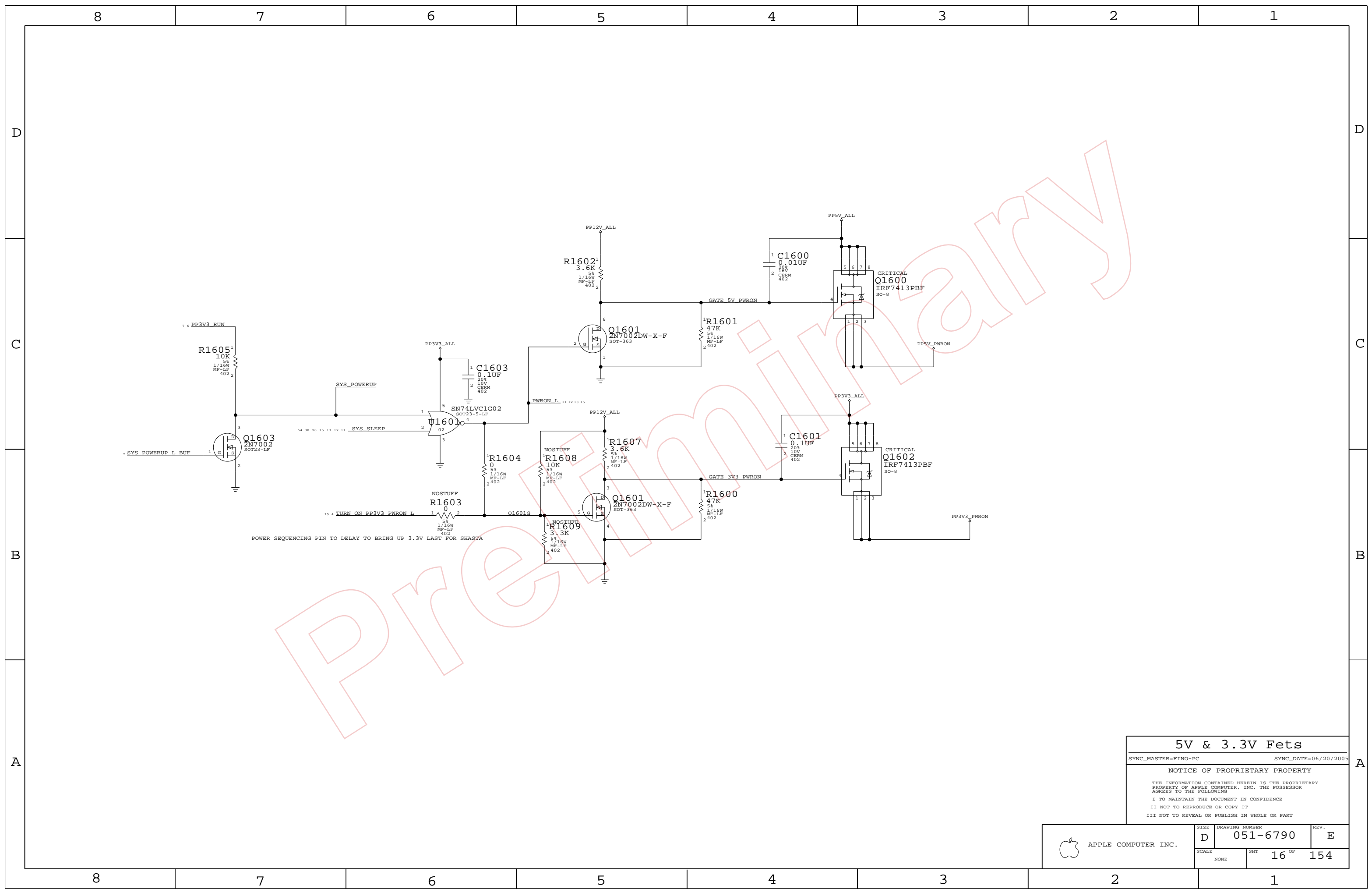
SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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NONE			




5V & 3.3V Fets

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NONE			

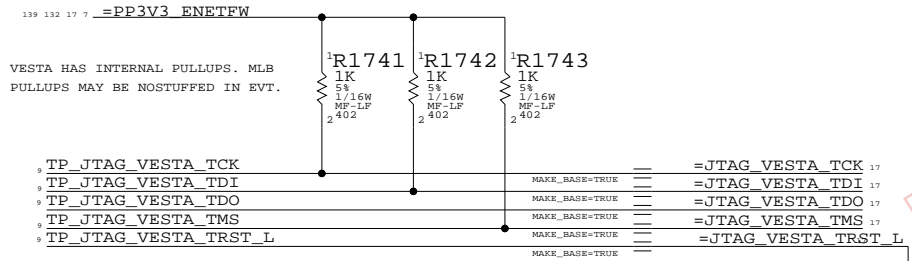
Page Notes

Power aliases required by this page:

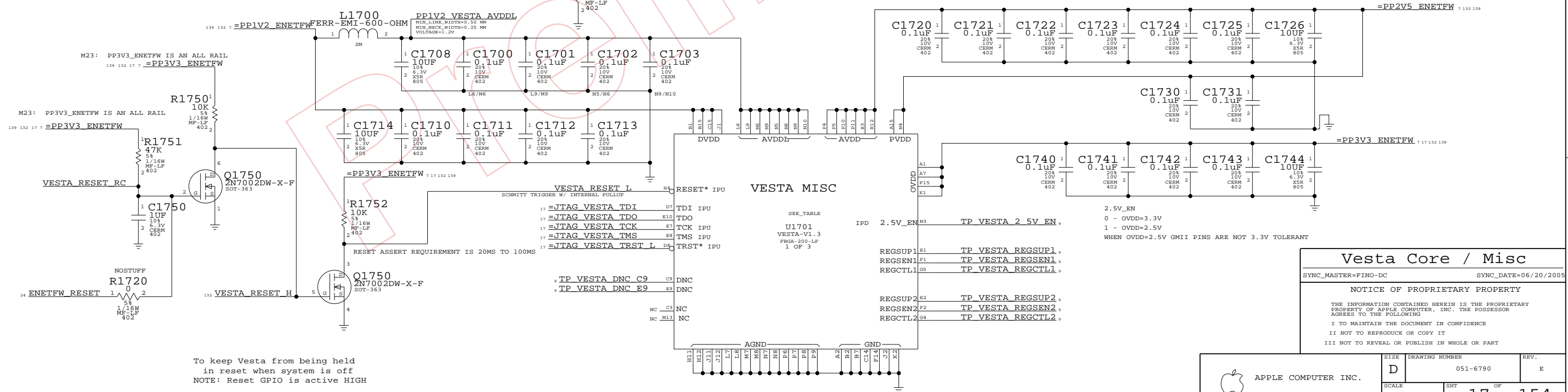
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG

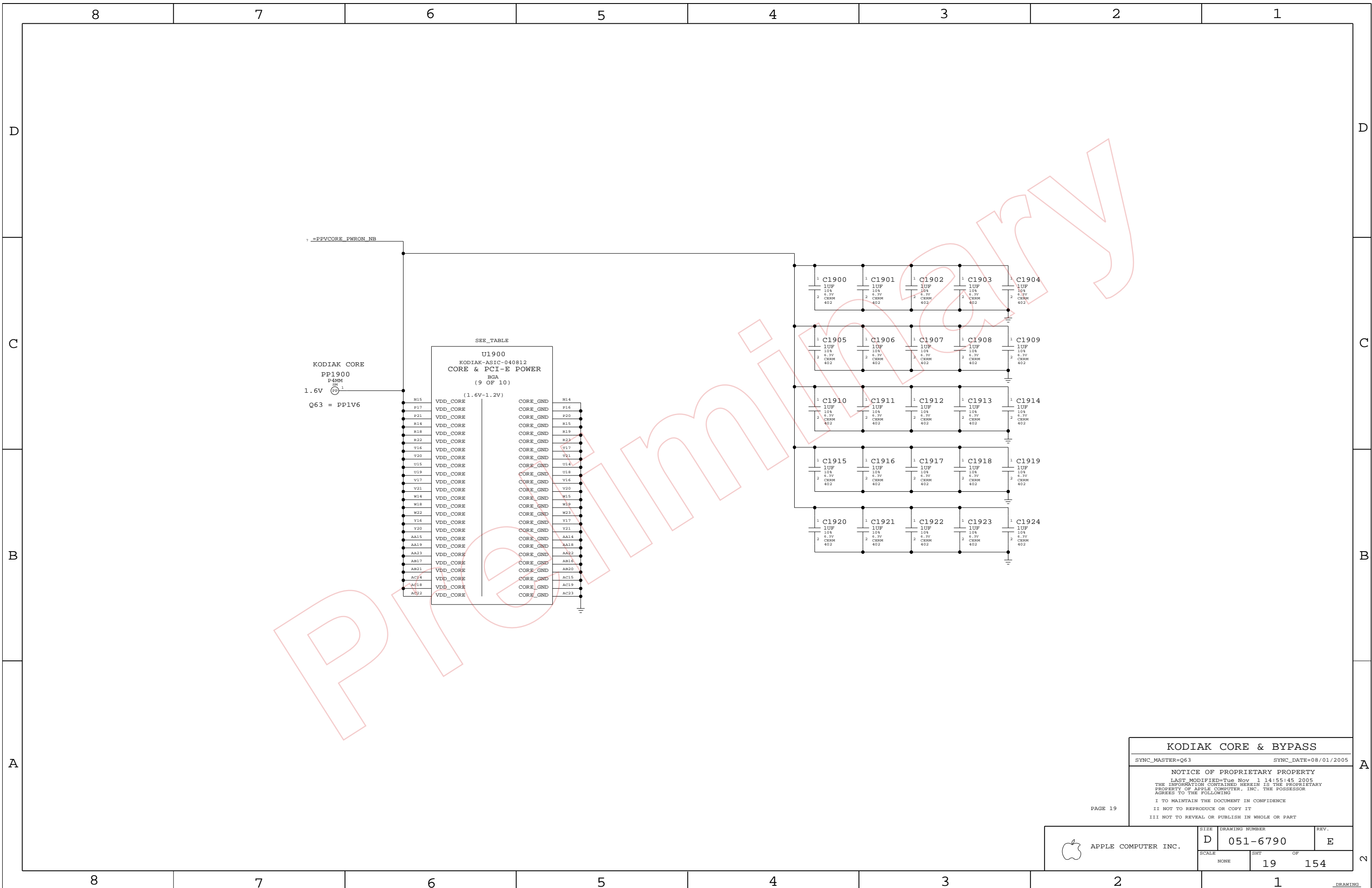


M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS



Vesta Core / Misc	
SYNC_MASTER=FINO-DC	SYNC_DATE=06/20/2005
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SCALE	SHT	OF	REV.
NONE	17	154	



KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

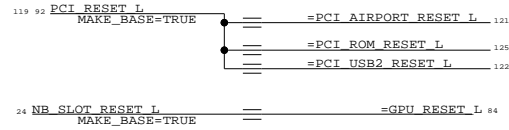
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PAGE 19

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	D	051-6790	E
SCALE	NONE	SHT OF	19 154

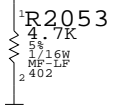
SHASTA ALIASES

PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB) AND SYS_IO_RESET_L (SMU)

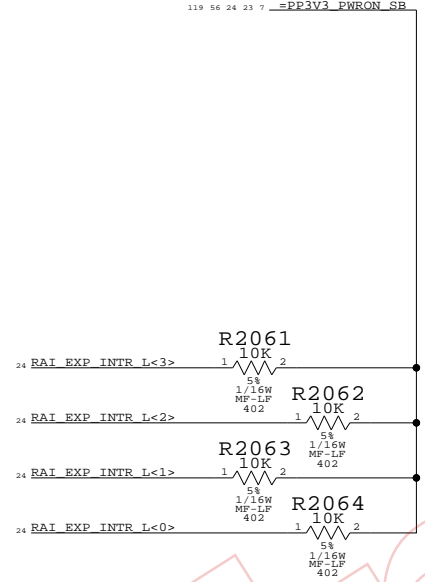


SHASTA JTAG

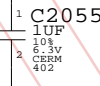
THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS. TP JTAG SB_TCK, TP JTAG SB_TDI, TP JTAG SB_TDO, TP JTAG SB_TMS.



SHASTA GPIO TERMINATIONS (SOME OF THESE ARE NOSTUFF ON PAGE 24)

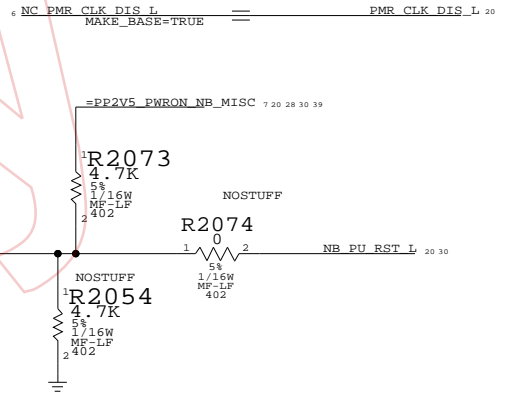


C2055 ADDED FOR KODIAK RAM DECOUPLING PAGE 58 IS SHORT ONE CAP

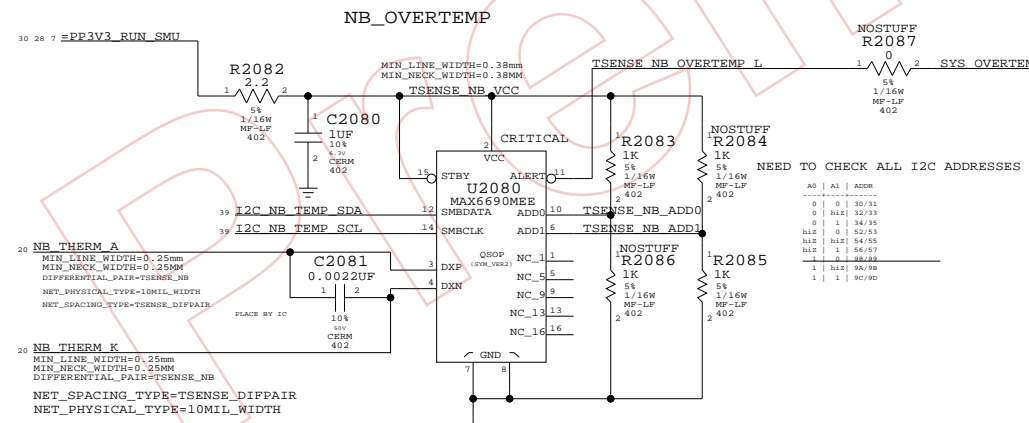
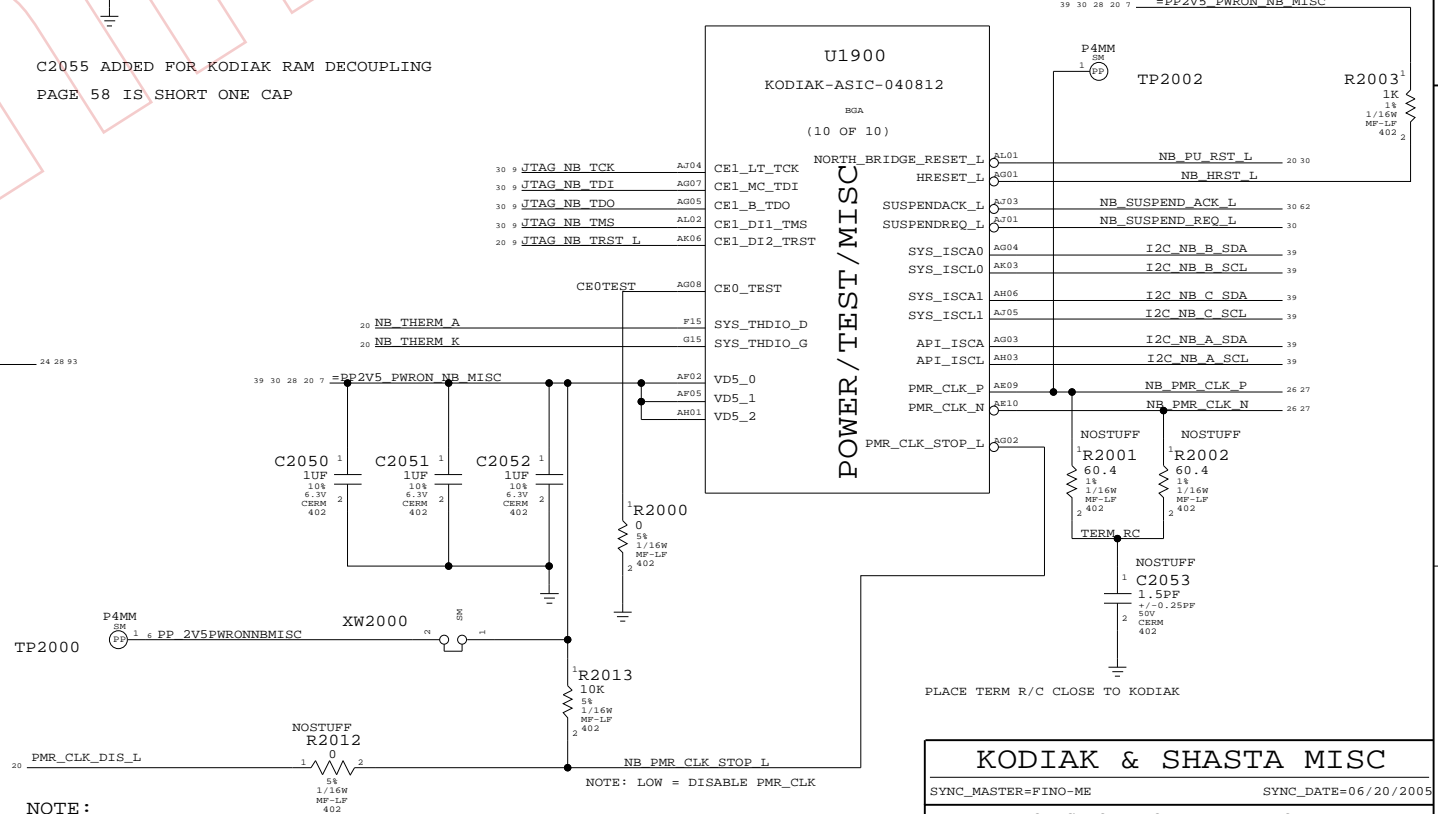


KODIAK ALIASES

KODIAK JTAG_TRST PULLED HIGH TO ALLOW SMU DEBUG ACCESS



POWER / TEST / MISC



NEED TO CHECK ALL I2C ADDRESSES

NOTE: PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK USED FOR DEBUG PLACE R2012 IN AN ACCESSIBLE LOCATION

KODIAK & SHASTA MISC. SYNC_MASTER=FINO-ME. SYNC_DATE=06/20/2005. NOTICE OF PROPRIETARY PROPERTY. THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.

Table with columns: SIZE (D), DRAWING NUMBER (051-6790), REV. (E), SCALE (NONE), SHEET (20 OF 154).

Page Notes

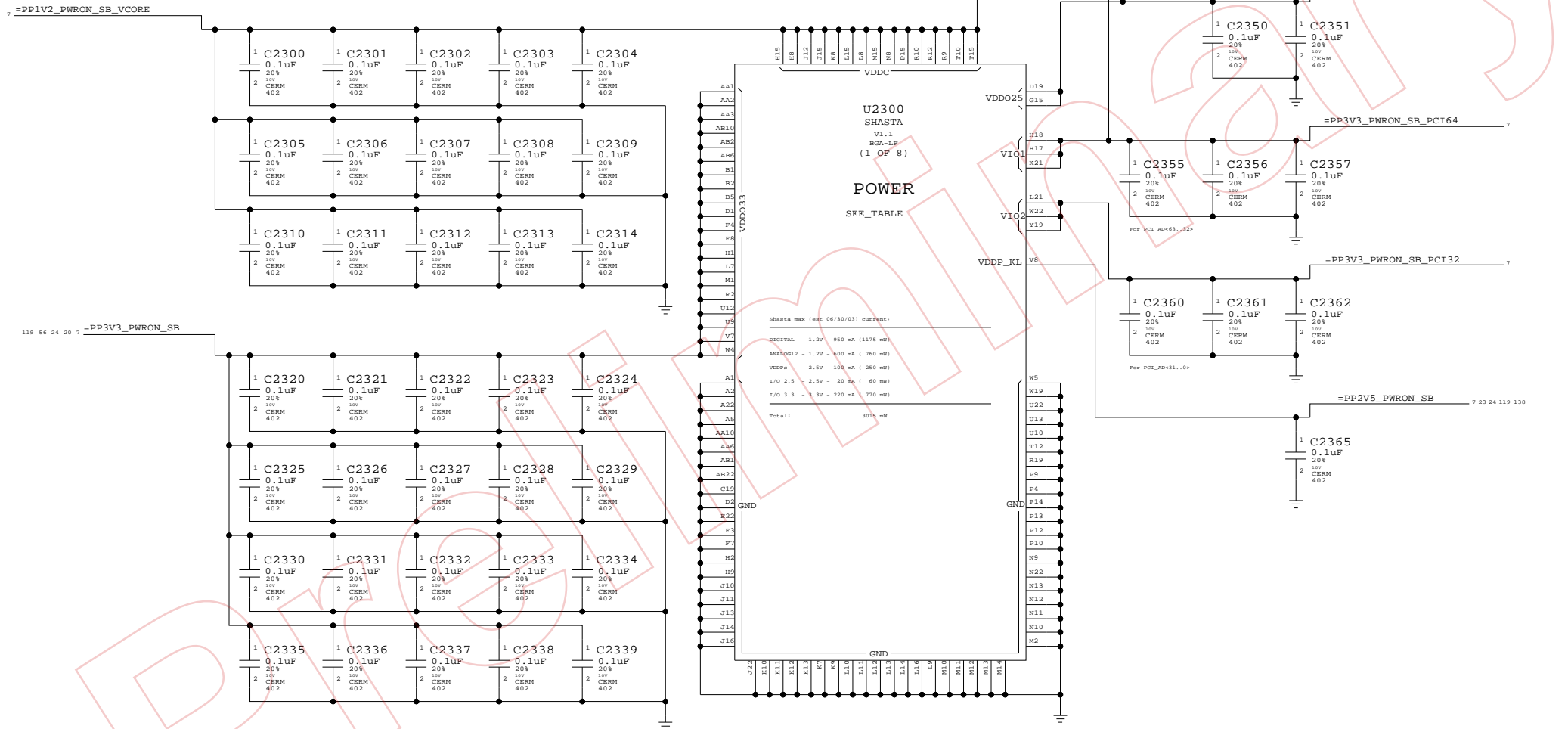
Power aliases required by this page:
 - =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
 - =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
 - =PP3V3_PWRON_SB
 - =PP2V5_PWRON_SB
 - =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
 (NONE)

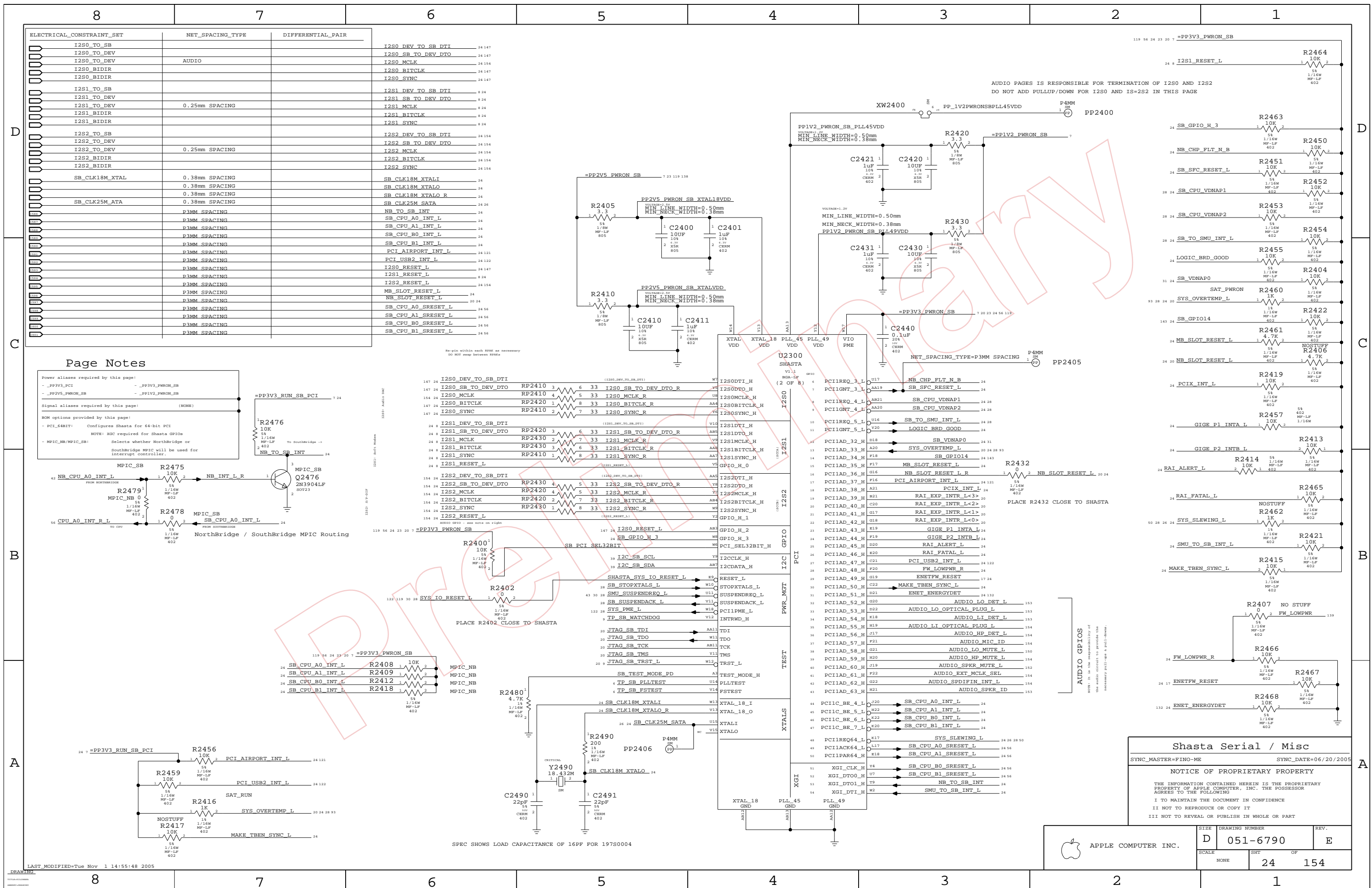
BOM options provided by this page:
 (NONE)

Power Sequencing:
 Must power Shasta VCore rail before any other Shasta supplies.



Shasta Core Power	
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NONE	23 OF 154		



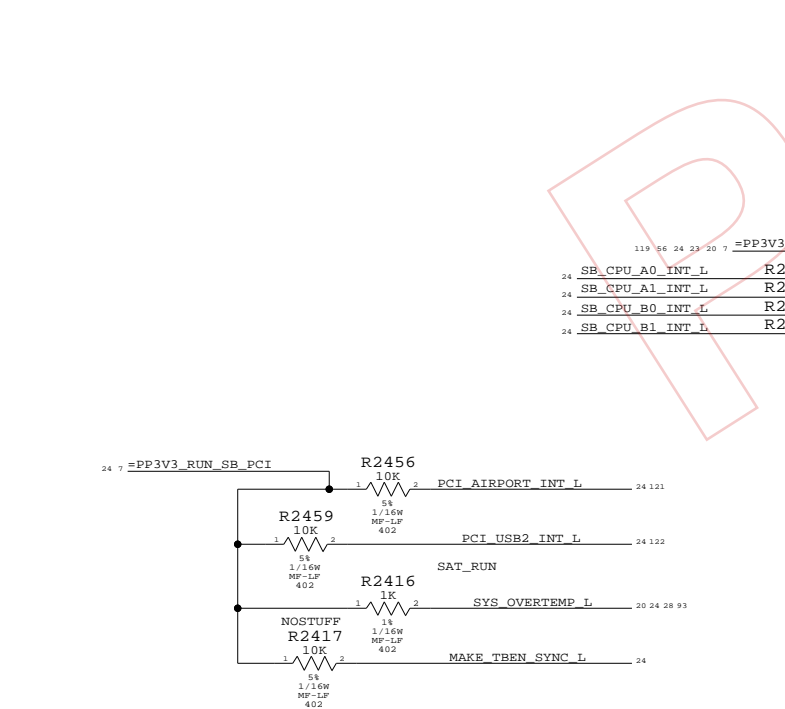
Page Notes

Power aliases required by this page:
 - _PP3V3_PCI - _PP3V3_PWRON_SB
 - _PP2V5_PWRON_SB - _PP2V5_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
 - PCI_64BIT: Configures Shasta for 64-bit PCI
 - NOTE: XDC required for Shasta GP10s
 - MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

NorthBridge / SouthBridge MPIC Routing

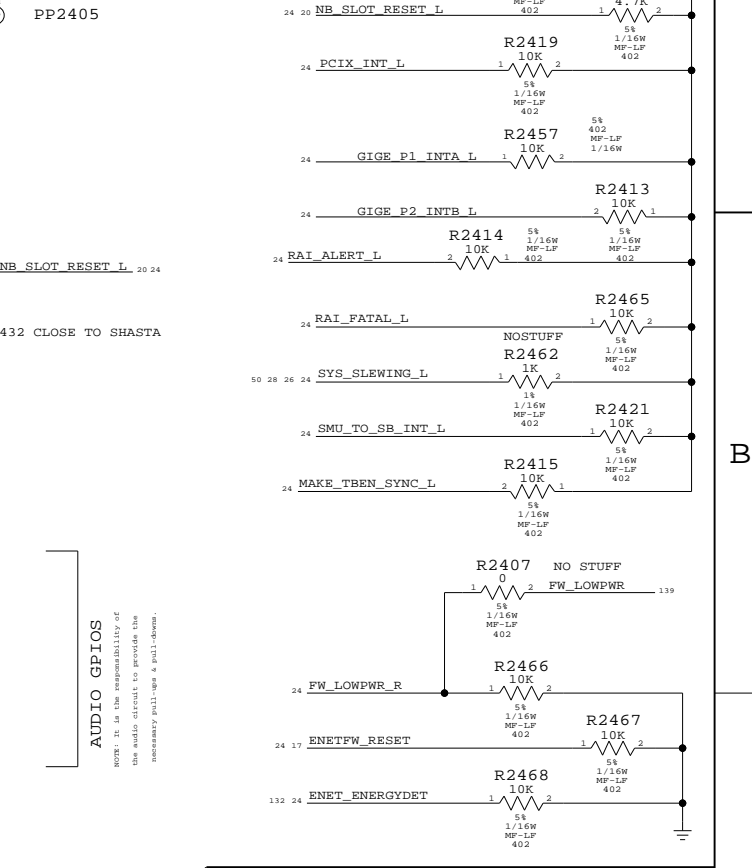


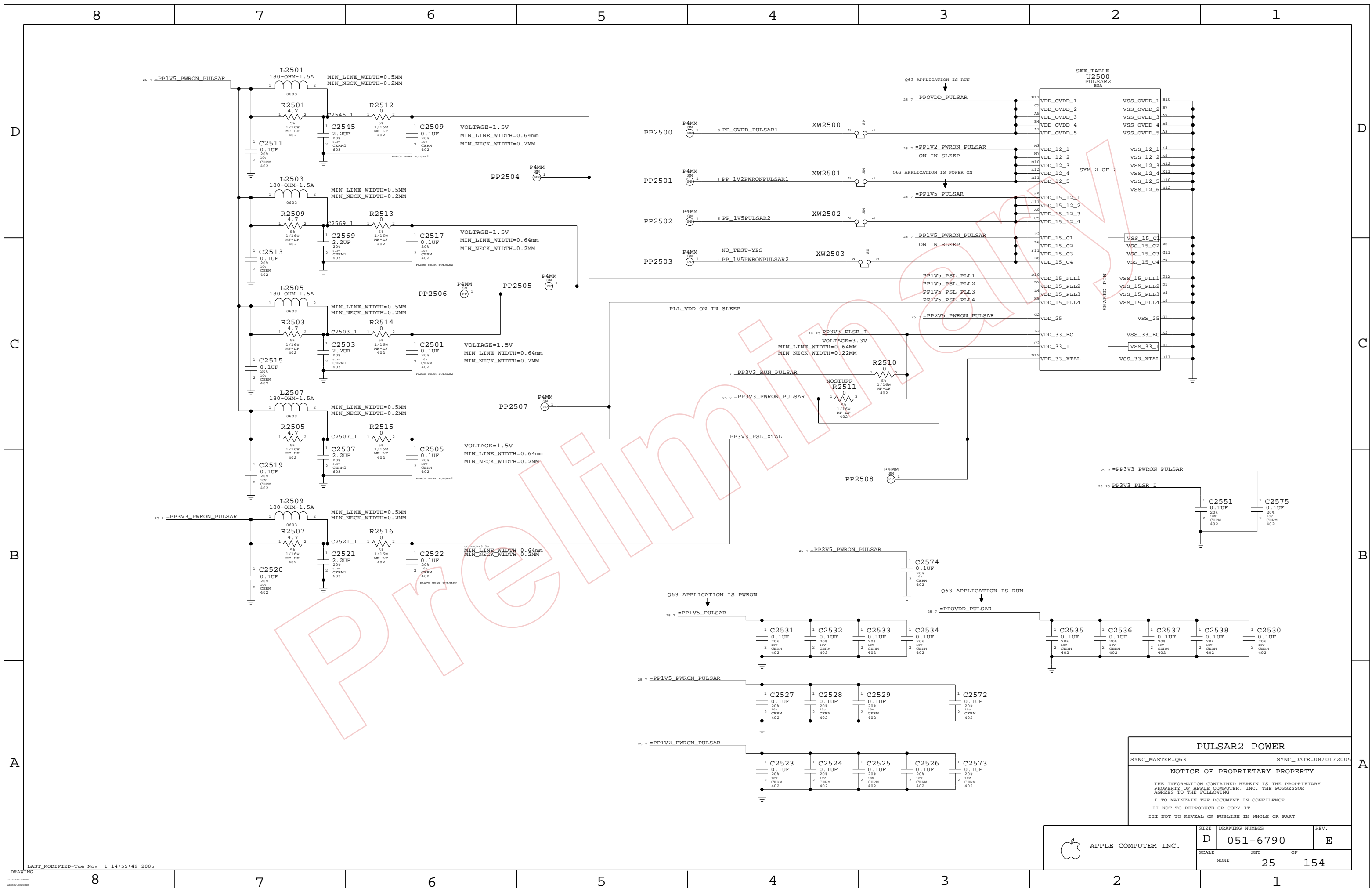
Place within each BOM as necessary
 so BOM map between pages

Net Name	Value	Pin	Component	Value
I2S0_DEV_TO_SB_DTI	10K	24	R2401	10K
I2S0_SB_TO_DEV_DTO	10K	24	R2402	10K
I2S0_MCLK	10K	24	R2403	10K
I2S0_BITCLK	10K	24	R2404	10K
I2S0_SYNC	10K	24	R2405	10K
I2S1_DEV_TO_SB_DTI	10K	24	R2406	10K
I2S1_SB_TO_DEV_DTO	10K	24	R2407	10K
I2S1_MCLK	10K	24	R2408	10K
I2S1_BITCLK	10K	24	R2409	10K
I2S1_SYNC	10K	24	R2410	10K
I2S2_DEV_TO_SB_DTI	10K	24	R2411	10K
I2S2_SB_TO_DEV_DTO	10K	24	R2412	10K
I2S2_MCLK	10K	24	R2413	10K
I2S2_BITCLK	10K	24	R2414	10K
I2S2_SYNC	10K	24	R2415	10K
I2S0_RESET_L	10K	24	R2416	10K
I2S1_RESET_L	10K	24	R2417	10K
I2S2_RESET_L	10K	24	R2418	10K
SB_CLK18M_XTAL	18.432M	24	Y2490	18.432M
SB_CLK18M_XTALO	18.432M	24	Y2490	18.432M
SB_CLK25M_SATA	25M	24	Y2490	25M
SB_CLK25M_SATL	25M	24	Y2490	25M
SB_CPU_A0_INT_L	10K	24	R2419	10K
SB_CPU_A1_INT_L	10K	24	R2420	10K
SB_CPU_B0_INT_L	10K	24	R2421	10K
SB_CPU_B1_INT_L	10K	24	R2422	10K

Shasta Serial / Misc

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PULSAR2 POWER

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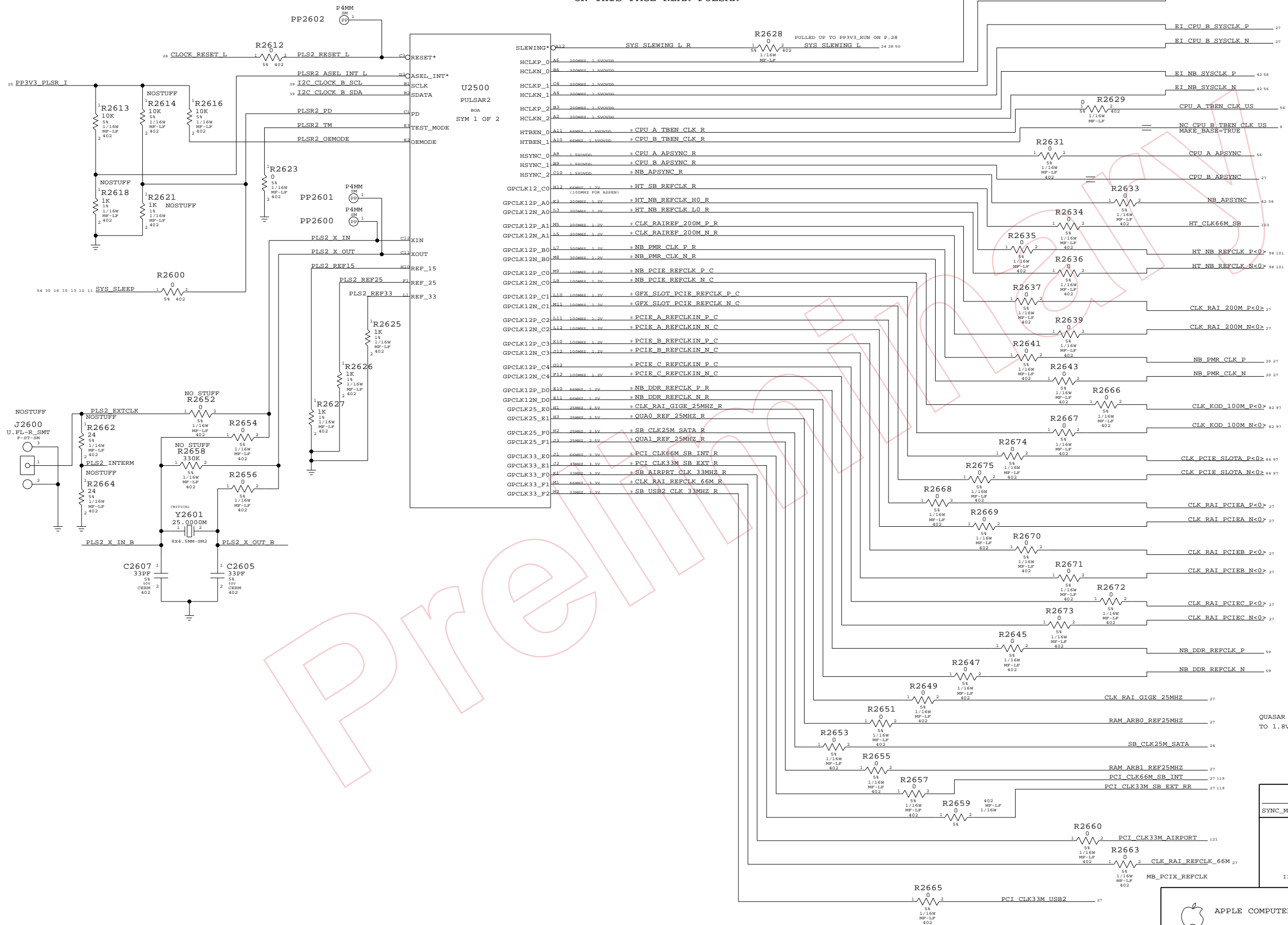
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PLACE ALL 0-OHM SERIES RESISTORS
ON THIS PAGE NEAR PULSAR



REMOVED R2632 AND R2630
FROM UNUSED CLOCKS FOR EMC

QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES
LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS
 SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

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		26	154

D

D

C

C

B

B

A

A

N/C ALIASES

N/C RAINIER CLOCKS

NC_CLK_RAI_REFCLK_66M == CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

NC_CLK_RAI_GIGE_25MHZ == CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

NC_CLK_RAI_200M_P<0> == CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_200M_N<0> == CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEA_P<0> == CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEA_N<0> == CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEB_P<0> == CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEB_N<0> == CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEC_P<0> == CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEC_N<0> == CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

NC_EI_CPU_B_SYSCLK_P == EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

NC_EI_CPU_B_SYSCLK_N == EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

NC_CPU_B_APSYNC == CPU_B_APSYNC 26
MAKE_BASE=TRUE

N/C QUASAR CLOCKS

NC_RAM_ARB0_REF25MHZ == RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

NC_RAM_ARB1_REF25MHZ == RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

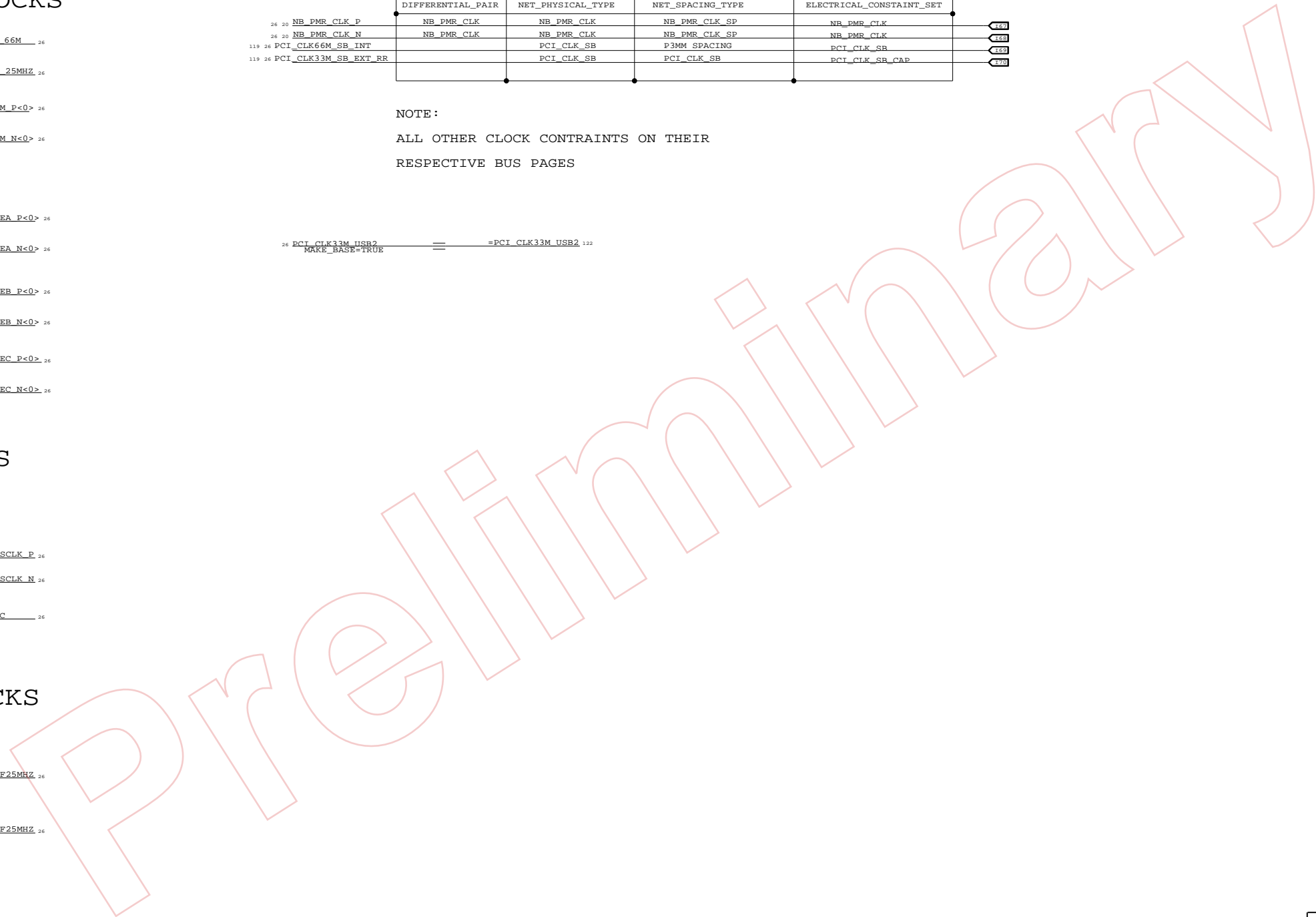
CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTRAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	479
26 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	481
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM_SPACING	PCI_CLK_SB	483
119 26 PCI_CLK33M_SB_EXT RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB_CAP	480

NOTE:

ALL OTHER CLOCK CONTRAINTS ON THEIR RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 == PCI_CLK33M_USB2 122
MAKE_BASE=TRUE



Pulsar Aliases

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

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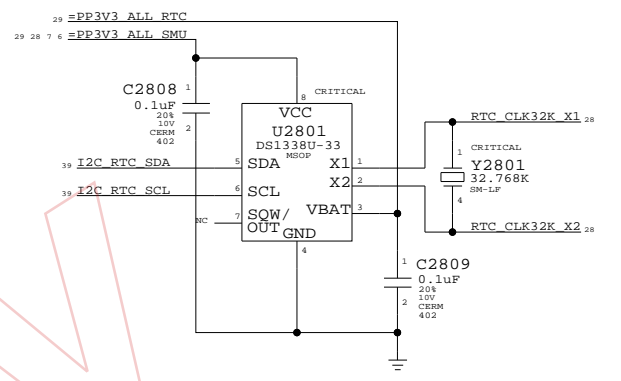
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_CLK10M_XTAL	0.38MM SPACING	
RTC_CLK32K_XTAL	0.38MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	

NET	NET	NET
SMU_CLK10M_XIN	SMU_CLK10M_XOUT	SMU_CLK10M_XOUT_R
RTC_CLK32K_X1	RTC_CLK32K_X2	SMU_IO_RESET_L
		SYS_NORTH_RESET_L

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_RESET	0.25MM SPACING	
SMU_RESET	0.25MM SPACING	
	0.25MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	
	0.38MM SPACING	

NET	NET	NET
SYS_NORTH_RESET_L	SYS_IO_RESET_L	CLOCK_RESET_L
		SYS_RESET_BUTTON_L

Real Time Clock



Page Notes

Power aliases required by this page:
 - =PP3V3_ALL_SMU
 - =PP3V3_ALL_RTC
 - =PP3V3_PWRON_SMU
 - =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

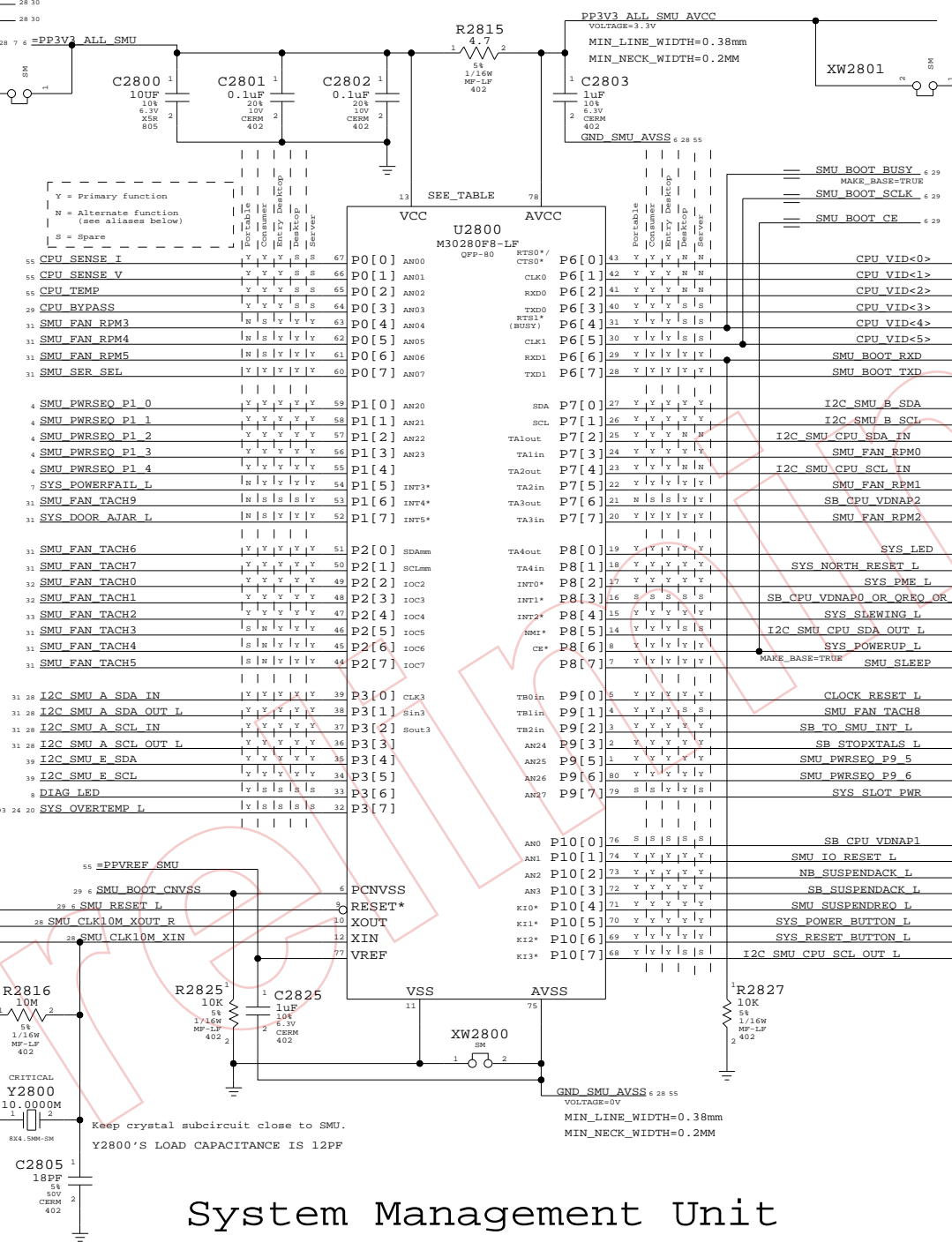
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

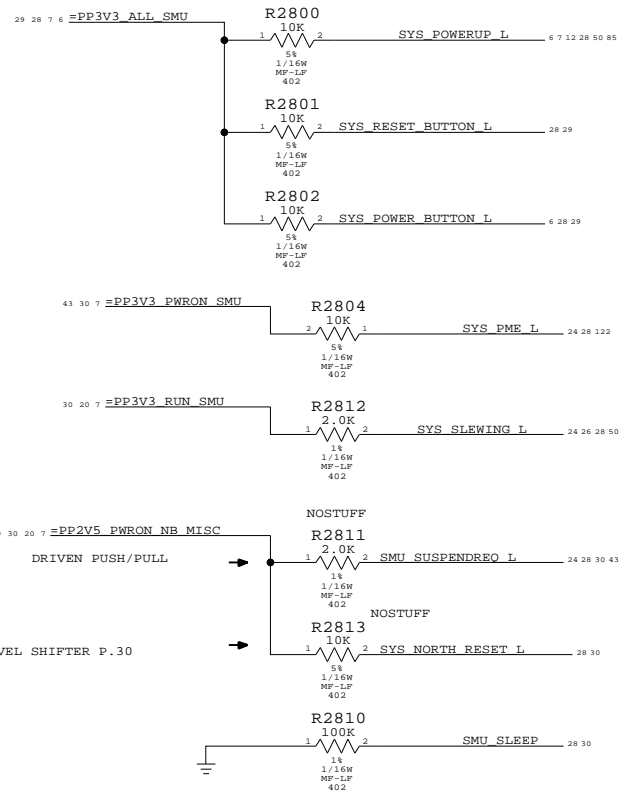
NOTE: Some primary and alternate functions require pull-ups that are not provided on this page. Please review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

P1[0] NOT USED --->



SMU Pull-ups / pull-down



System Management Unit

Alternate Functions

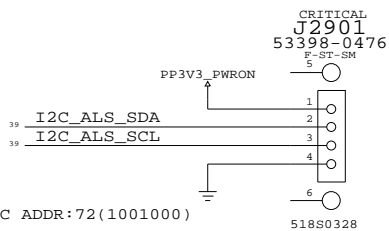
Port	Port	Port
31 28 CPU VID<0>	6.0	SAT MRESET L
31 28 CPU VID<1>	6.1	CPU A INSERTED L
31 28 CPU VID<2>	6.2	CPU B INSERTED L
31 28 I2C SMU CPU SDA IN	7.2	SMU FAN PWM8
31 28 I2C SMU CPU SCL IN	7.4	SMU FAN PWM9
31 28 I2C SMU A SDA IN	3.0	I2C SMU A SDA
31 28 I2C SMU A SDA OUT L	3.1	I2C SMU A SCL
31 28 CPU VID<3>	6.3	SMU FAN RPM6
31 28 CPU VID<4>	6.4	SMU FAN RPM7
31 28 I2C SMU A SCL IN	3.2	NB_TDI
31 28 I2C SMU A SCL OUT L	3.3	NB_TCK
31 28 I2C SMU CPU SDA OUT L	8.5	NB_TMS
31 28 I2C SMU CPU SCL OUT L	10.7	NB_TDO SMU

System Management Unit
 SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

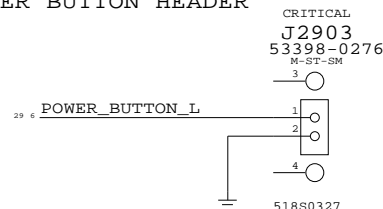
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NONE	28	154

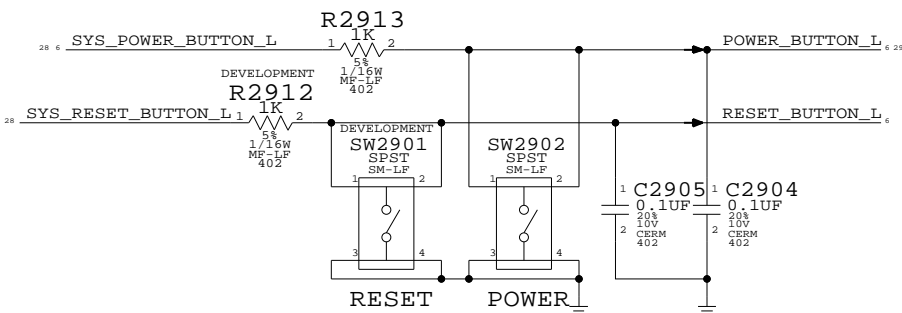
AMBIENT LIGHT SENSOR CONNECTOR



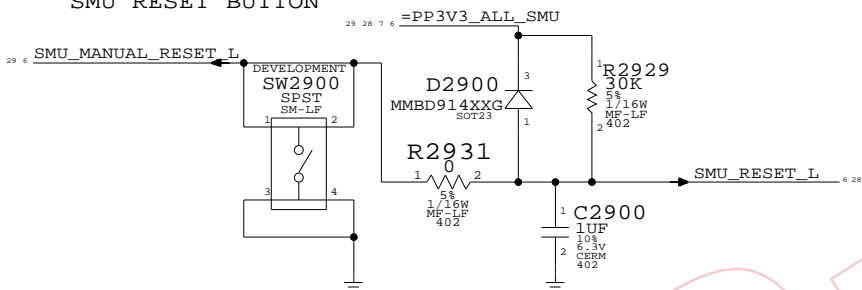
POWER BUTTON HEADER



SYS POWER AND RESET BUTTON

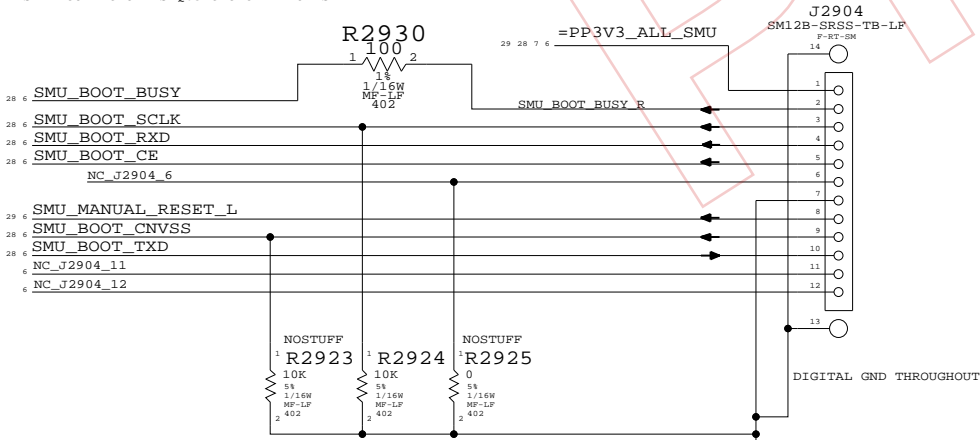


SMU RESET BUTTON



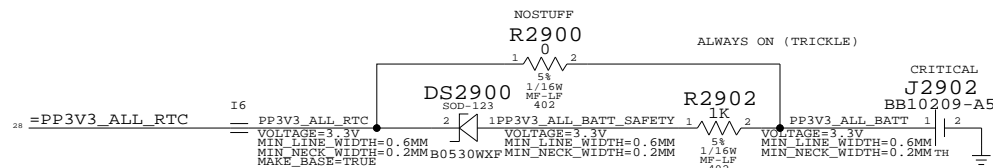
SMU DEBUG/DOWNLOAD CONNECTOR

SAME CONNECTOR AS Q63 CPU CARD FOR SAT

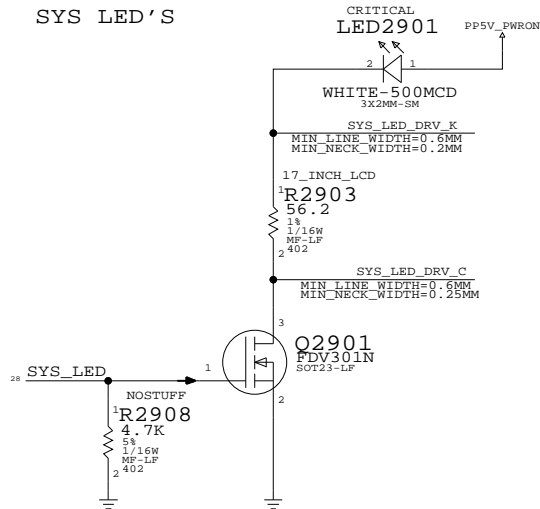


R2930, R2931, J2904 SHOULD BE MOVED BACK TO THE DEVELOPMENT BOM POST-RAMP

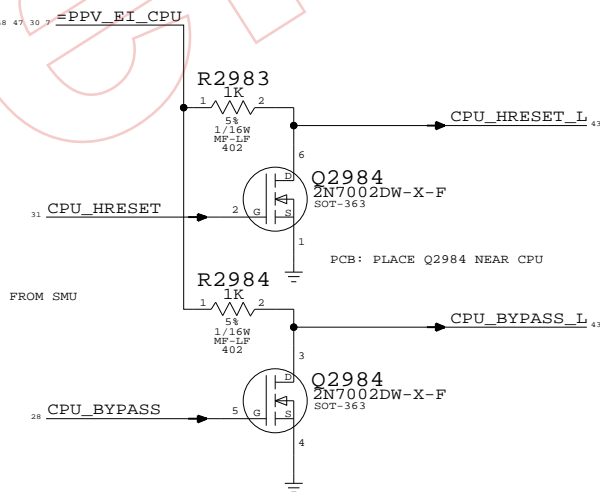
RTC BATTERY



SYS LED'S



DRIVE STRONG HRESET AND BYPASS TO CPU



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES, 39.2 OHM, 1%, 402, LF	R2903	20_INCH_LCD

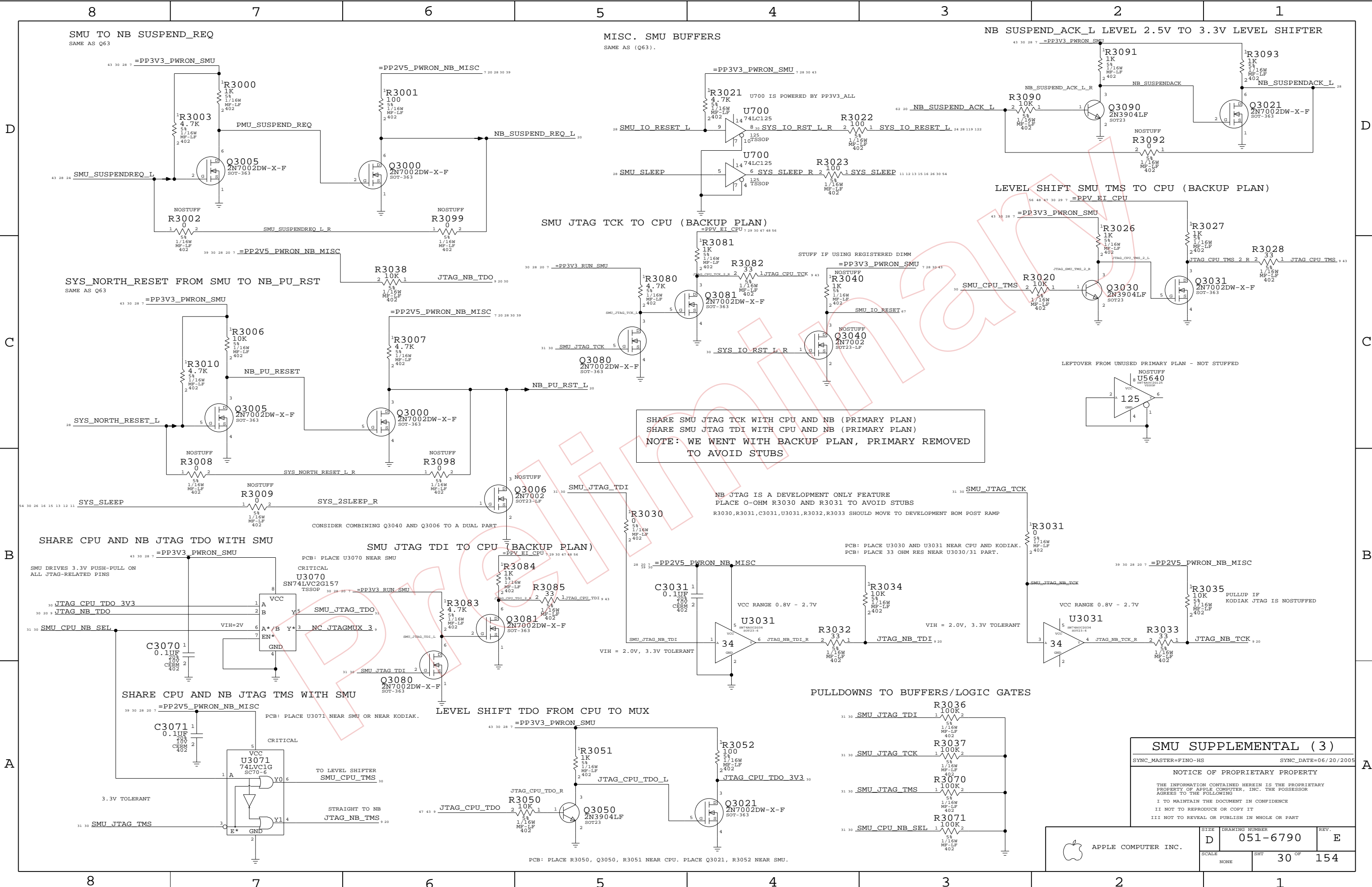
SMU SUPPLEMENTAL (2)

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		29	154



SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)
SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)
NOTE: WE WENT WITH BACKUP PLAN, PRIMARY REMOVED
TO AVOID STUBS

NB JTAG IS A DEVELOPMENT ONLY FEATURE
PLACE 0-OHM R3030 AND R3031 TO AVOID STUBS
R3030, R3031, C3031, U3031, R3032, R3033 SHOULD MOVE TO DEVELOPMENT BOM POST RAMP

PCB: PLACE U3070 NEAR SMU
CRITICAL

PCB: PLACE U3030 AND U3031 NEAR CPU AND KODIAK.
PCB: PLACE 33 OHM RES NEAR U3030/31 PART.

PCB: PLACE U3071 NEAR SMU OR NEAR KODIAK.
CRITICAL

PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.

SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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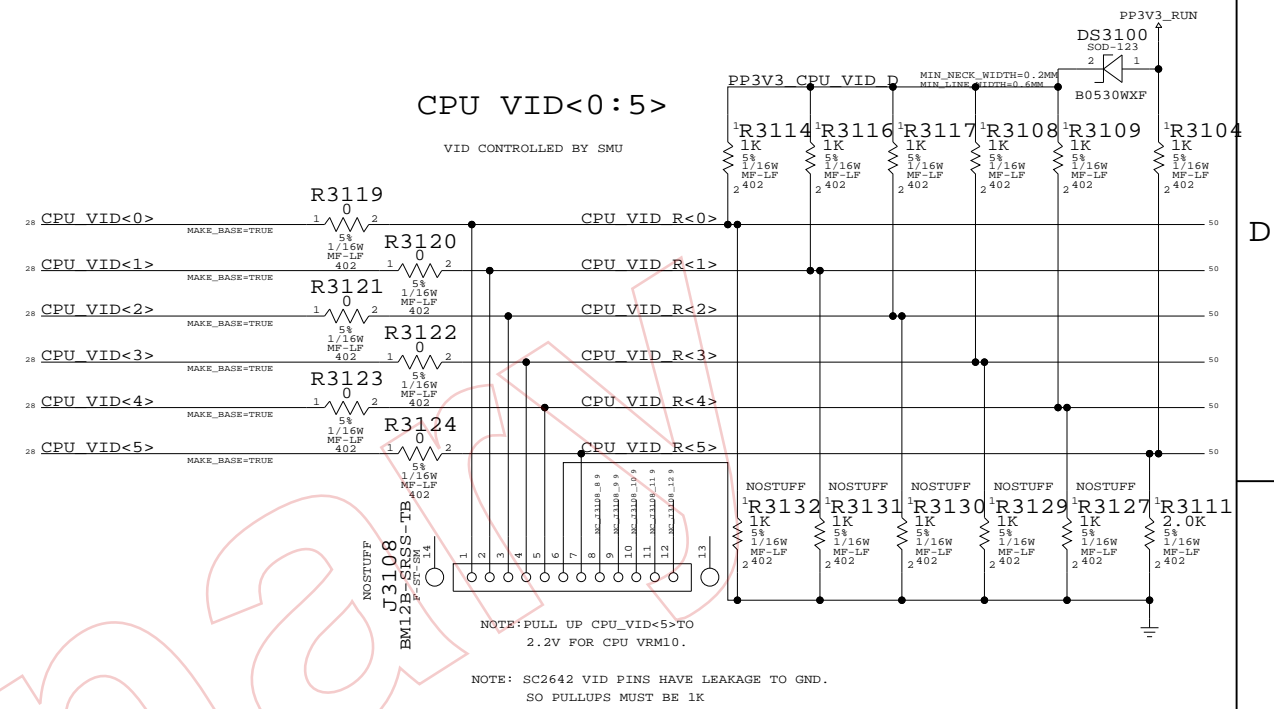
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NONE			

SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION	Q63 NET NAME (SHARED PAGE)
Q63 NC'S THESE AS IT USES A SAT.		CPU_SENSE_I0 P0.0	
		CPU_SENSE_V0 P0.1	
		CPU_TEMP0 P0.2	
		CPU_BYPASS P0.3	
M23/M33 DOESN'T HAVE THOSE FANS.	NC SMU FAN RPM3	FAN_CNTRL0_4 P0.4	SMU FAN RPM3
	NC SMU FAN RPM4	FAN_CNTRL0_5 P0.5	SMU FAN RPM4
	NC SMU FAN RPM5	FAN_CNTRL0_6 P0.6	SMU FAN RPM5
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE. M23/M33 DOESN'T USE. P1.0 NC ON PG 7.	NC SMU SER_SEL	SMU_SCCL_SEL P0.7	SMU SER_SEL
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_SENSE_I1 P1.1	
		CPU_SENSE_V1 P1.2	
		CPU_TEMP1 P1.3	
		PS1_3 P1.3	
		PS1_4 P1.4	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		POWERFAIL* P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE. CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	NC SMU CPU VID LE0	CPU_VID_LE0 P1.6	SMU FAN TACH9
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE. M23/M33 DOESN'T HAVE THIS FAN.	NC SYS DOOR AJAR L	DOOR_AJAR* P1.7	SYS DOOR AJAR L
	NC SMU CPU VID LE1	CPU_VID_LE1 P2.0	SMU FAN TACH6
	NC SMU FAN TACH7	FAN_TACH2_1 P2.1	SMU FAN TACH7
		FAN_TACH2_2 P2.2	
		FAN_TACH2_3 P2.3	
		FAN_TACH2_4 P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7. M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	NC SMU FAN TACH3	FAN_TACH2_5 P2.5	SMU FAN TACH3
	NC SMU FAN TACH4	FAN_TACH2_6 P2.6	SMU FAN TACH4
	NC SMU FAN TACH5	FAN_TACH2_7 P2.7	SMU FAN TACH5
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	I2C SMU A SDA	I2C_A_DAT P3.0	I2C SMU A SDA IN
	I2C SMU A SCL	I2C_A_CLK P3.1	I2C SMU A SDA OUT L
	SMU JTAG TDI	TDI P3.2	I2C SMU A SCL IN
	SMU JTAG TCK	TCK P3.3	I2C SMU A SCL OUT L
		IIC_E_DAT P3.4	
		IIC_E_CLK P3.5	
		DIAG_LED P3.6	
		OVERTEMP* P3.7	
		CPU_VID[0] P6.0	
		CPU_VID[1] P6.1	
		CPU_VID[2] P6.2	
		CPU_VID[3] P6.3	
		CPU_VID[4] P6.4	
		CPU_VID[5] P6.5	
		DEBUG_RXD P6.6	
		DEBUG_TXD P6.7	
		IIC_B_DAT P7.0	
		IIC_B_CLK P7.1	
Q63 USE OF P7.2 IS PWM FAN SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	SMU CPU NB SEL	CPU_TMS P7.2	I2C SMU CPU SDA IN
		FAN_CNTRL7_3 P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4) M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.	NC I2C SMU CPU SCL IN	FAN_CNTRL7_4 P7.4	I2C SMU CPU SCL IN
		FAN_CNTRL7_5 P7.5	
		VDNAP2 P7.6	
		FAN_CNTRL7_7 P7.7	
		SYSTEM_LED P8.0	
		NB_RESET* P8.1	
		PME* P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	SB VDNAP0	VDNAP0 P8.3	SB CPU VDNAP0 OR QREQ OR SPDIF
		SLEWING* P8.4	
	SMU JTAG TMS	DR_5 P8.5	I2C SMU CPU SDA OUT L
		POWERUP* P8.6	
		SLEEP P8.7	
		CLK_RESET* P9.0	
Q63 USE OF P9.1 IS TACH 8.	CPU HRESET	CPU_HRESET P9.1	SMU FAN TACH8
		SMU_DOORBELL* P9.2	
		STOP_XTAL* P9.3	
		PS9_5 P9.5	
		PS9_6 P9.6	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7. M23/M33 HAS NO SLOTS.	NC SLOT TOTAL PWR	SLOT_TOTAL_PWR P9.7	SYS SLOT PWR
		VDNAP1 P10.0	
		IO_RESET* P10.1	
		SUSPEND_ACK* P10.2	
		SUSPEND_IO_ACK* P10.3	
		SUSPEND_REQ* P10.4	
		PWR_BUTTON* P10.5	
		RST_BUTTON* P10.6	
	SMU JTAG TDO	TDO P10.7	I2C SMU CPU SCL OUT L



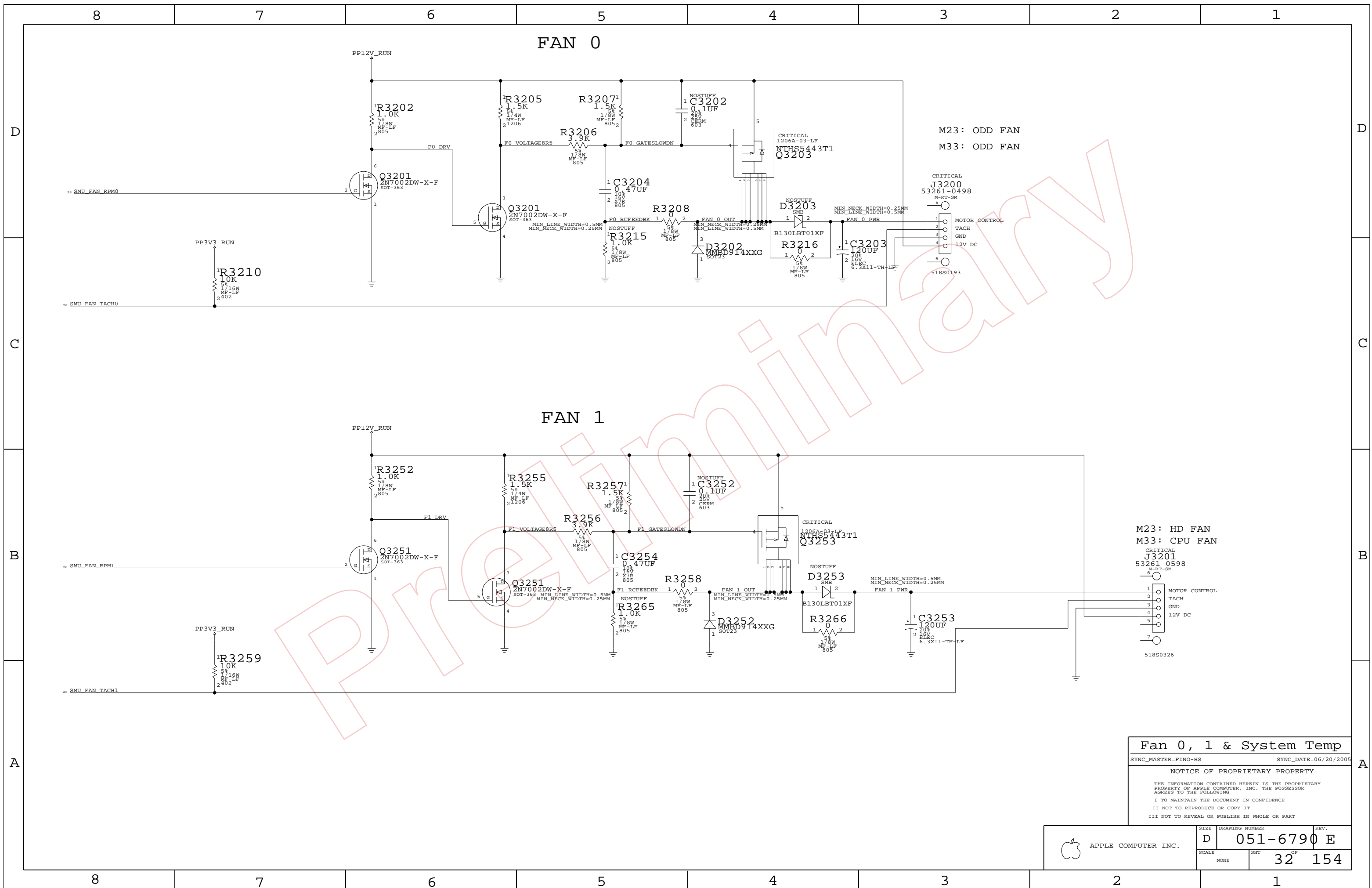
SMU SUPPLEMENTAL (4)

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Fan 0, 1 & System Temp

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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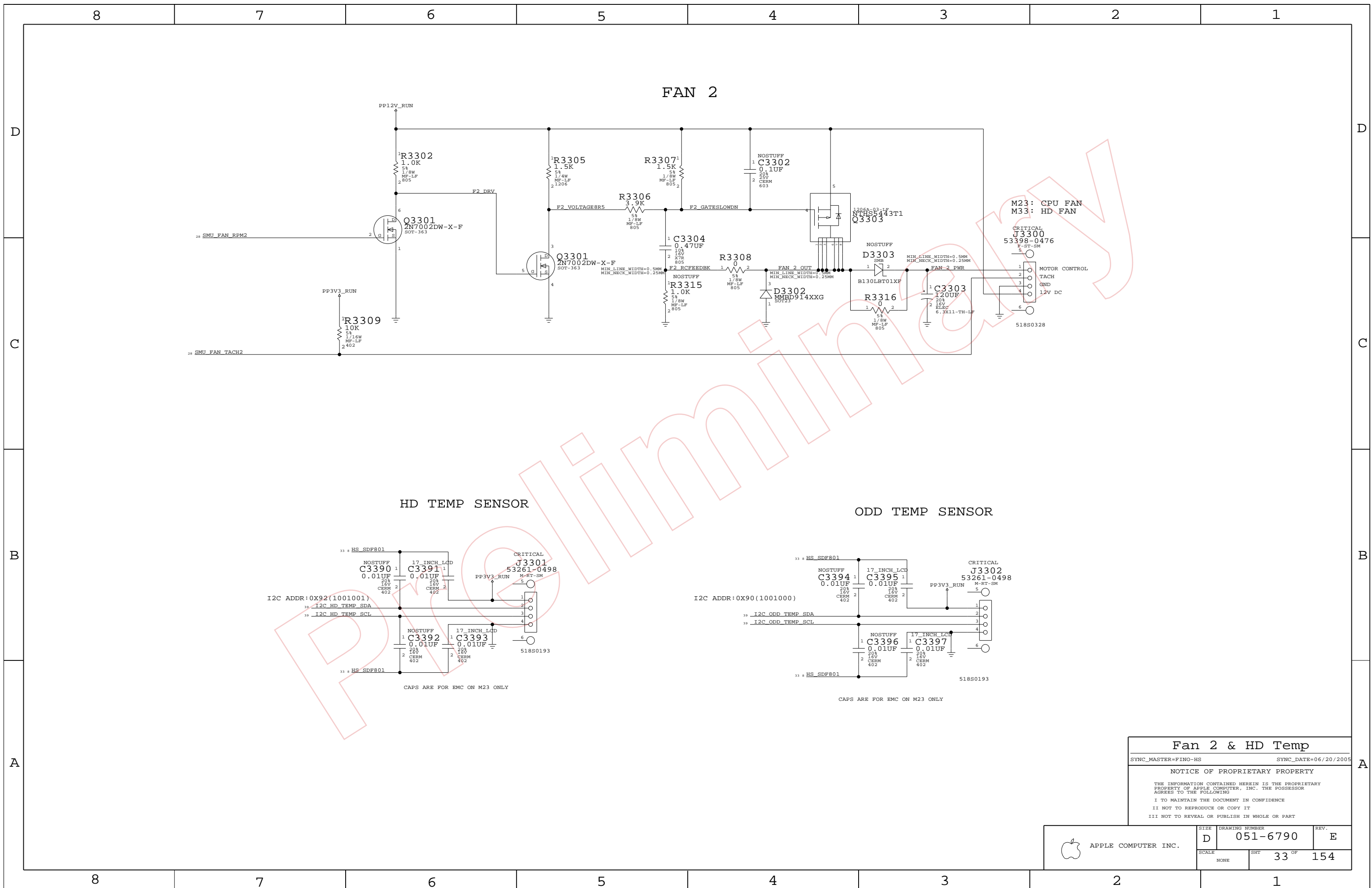
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Fan 2 & HD Temp

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NONE			

SMU AND NB I2C A BUS

SB I2C BUS

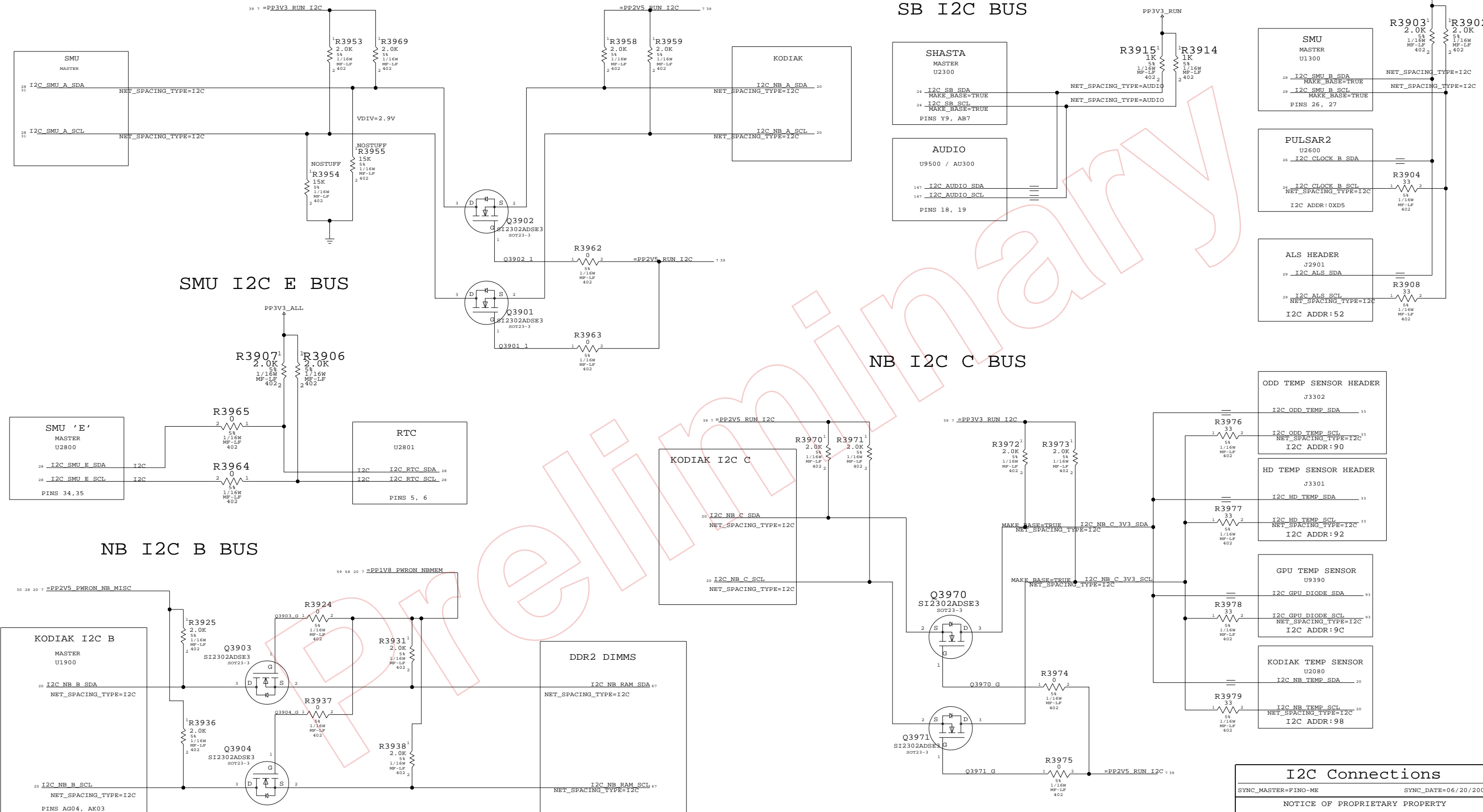
SMU I2C B BUS

SMU I2C E BUS

NB I2C C BUS

NB I2C B BUS

I2C Connections



SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

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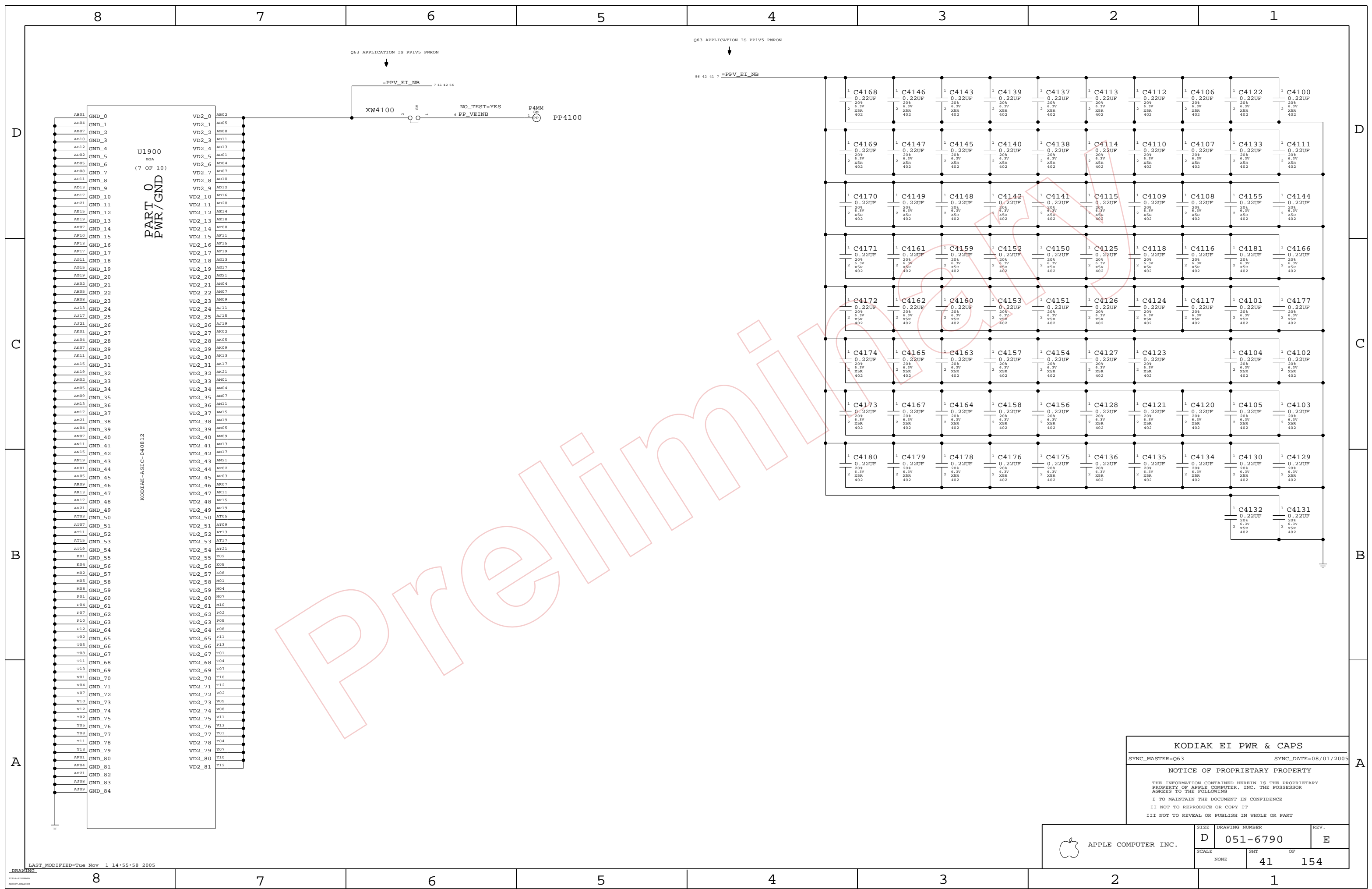
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NONE			



U1900
BGA
(7 OF 10)
PART 0
PWR/GND

KODIAK-ASTC-040812

KODIAK EI PWR & CAPS
 SYNC_MASTER=Q63 SYNC_DATE=08/01/2005
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SCALE	SHT OF		
NONE	41 OF		154

D

D

C

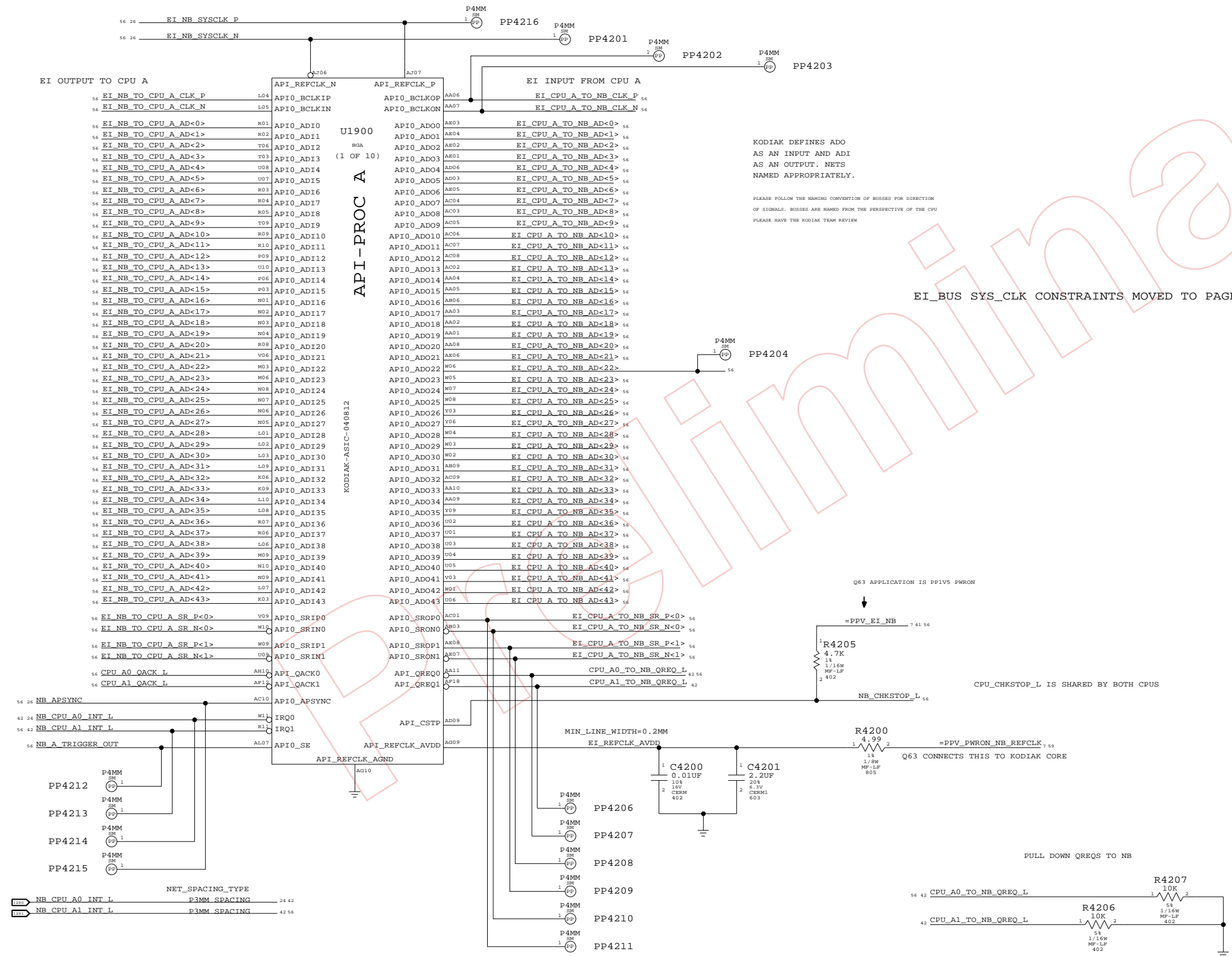
C

B

B

A

A



KODIAK DEFINES ADO AS AN INPUT AND ADI AS AN OUTPUT. NETS NAMED APPROPRIATELY.

PLEASE FOLLOW THE NAMING CONVENTION OF BUSES FOR DIRECTION OF SIGNALS. BUSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU PLEASE HAVE THE KODIAK TEAM REVIEW

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

Q63 APPLICATION IS PP1VS PWRON

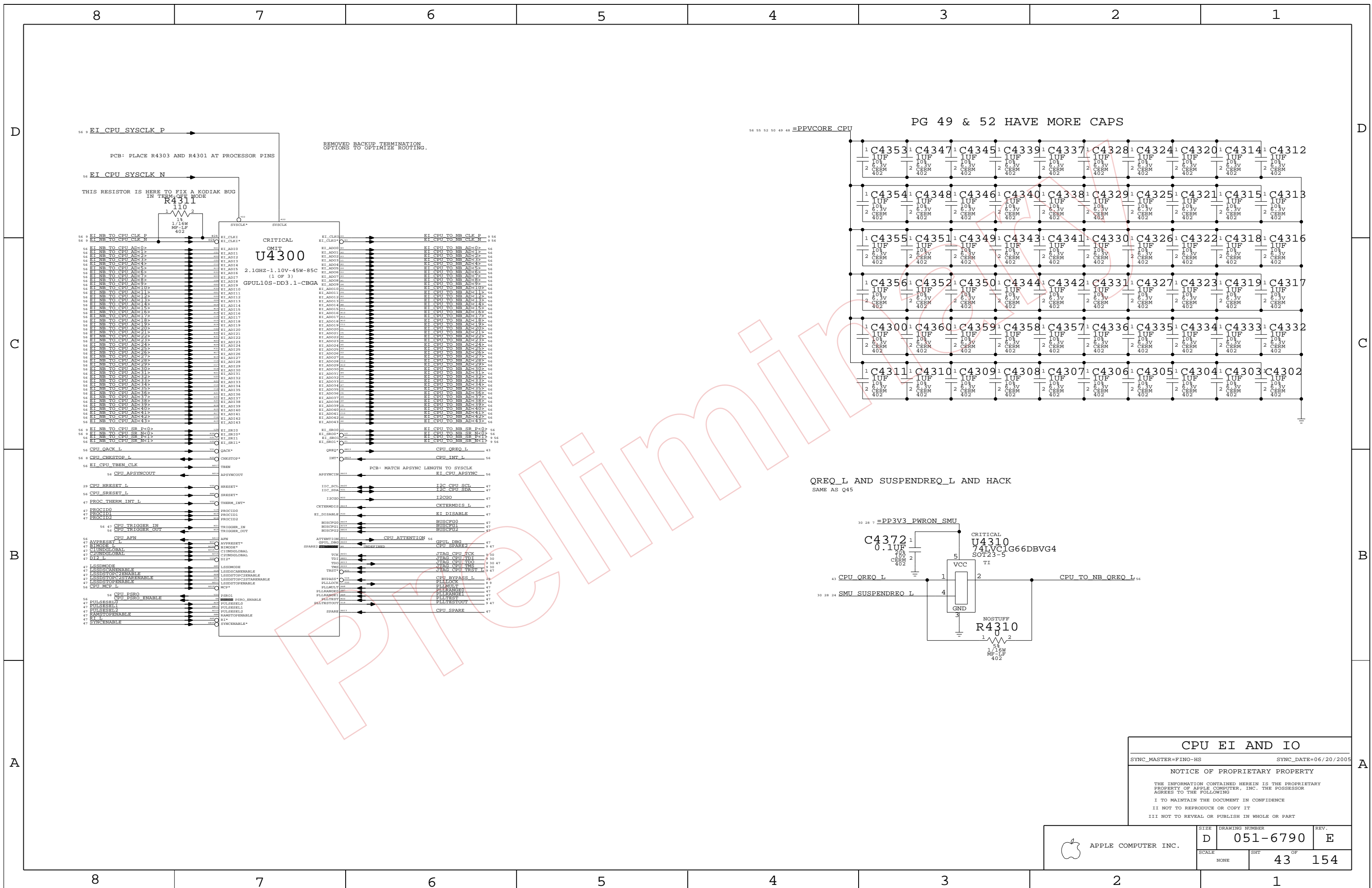
CPU_CHKSTOP_L IS SHARED BY BOTH CPUS

Q63 CONNECTS THIS TO KODIAK CORE

PULL DOWN QREQS TO NB

KODIAK EI A		
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005	
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CPU EI AND IO

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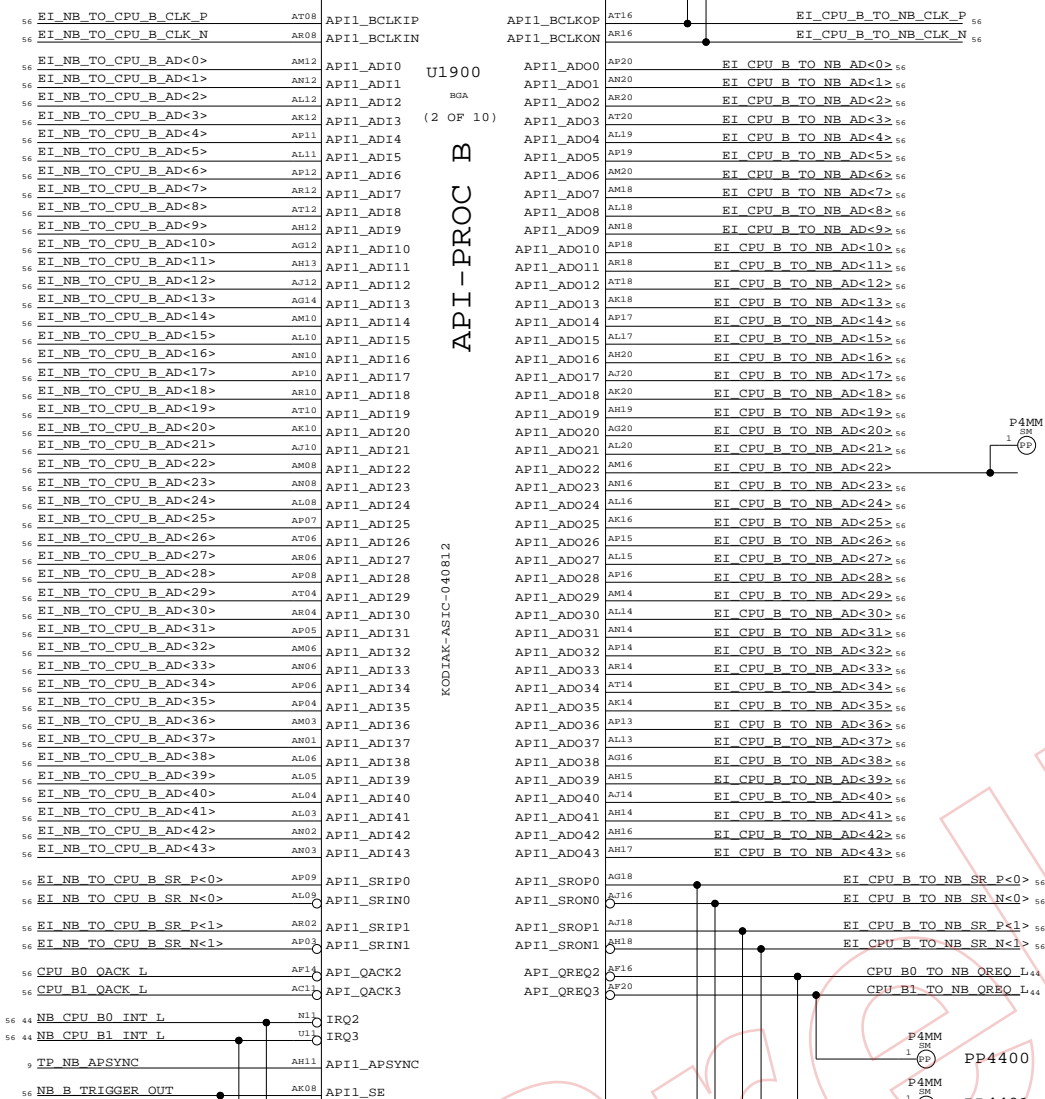
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		43	154

PLEASE FOLLOW THE NAMING CONVENTION OF BUSES FOR DIRECTION OF SIGNALS. BUSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

EI INPUT FROM CPU B



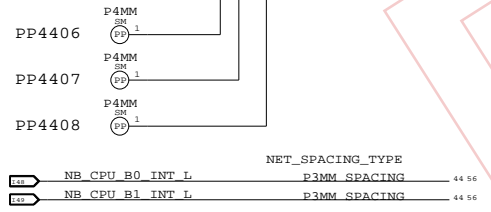
KODIAK DEFINES ADO AS AN INPUT AND ADI AS AN OUTPUT. NETS NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT ELECTRICAL_CONSTRAINT_SET FOR CPU_A AND CPU_B.

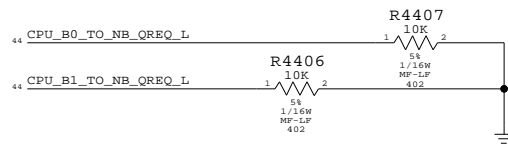
EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

API-PROC B
KODIAK-ASIC-040812

WIRE TP_NB_APSYNC TO A TEST POINT

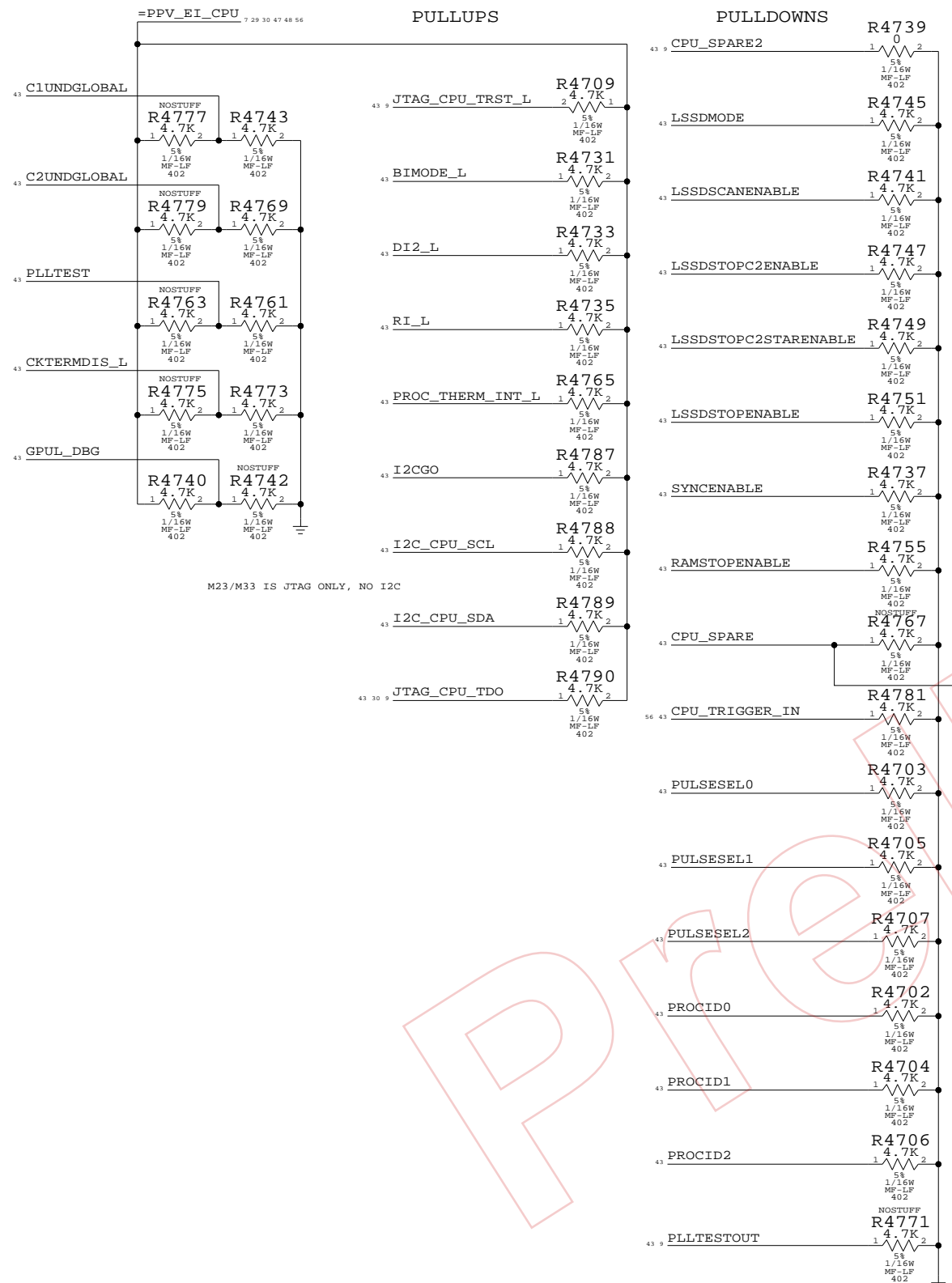


PULL DOWN QREQS TO NB



KODIAK EI B
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	D	051-6790	E
SCALE	NONE	SHT OF	44 154



NOTES

JTAG DRIVEN ON SMU PG 30
 QREQ PULLDOWNS ON Q63 SHARED PAGE
 SRESET DRIVEN ON PG 56
 INT DRIVEN BY KODIAK
 R4739 REQUIRED TO ACCESS THE RINGS

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
 1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

>= 1.8 GHZ *

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3T01
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2T01

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2T01
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF

SELECT ELASTIC MODE OR BYPASS.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736	
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF

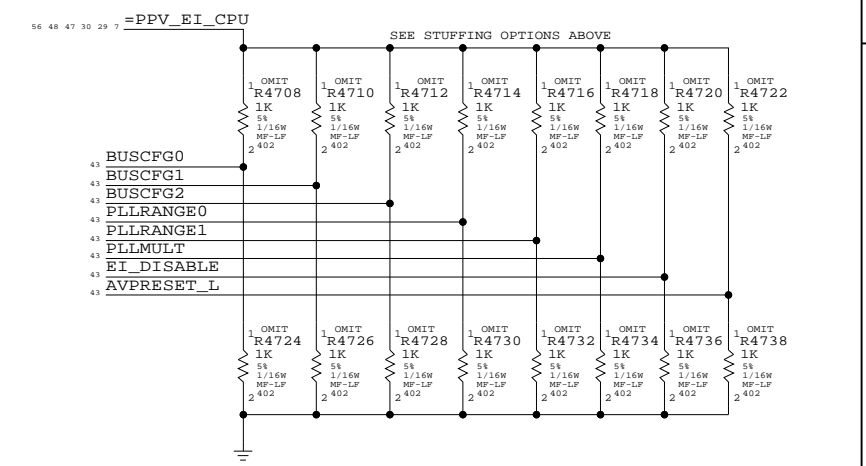
SELECT PLL FREQUENCY RANGE.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722	AVPRESET OFF
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION



CPU STRAPS

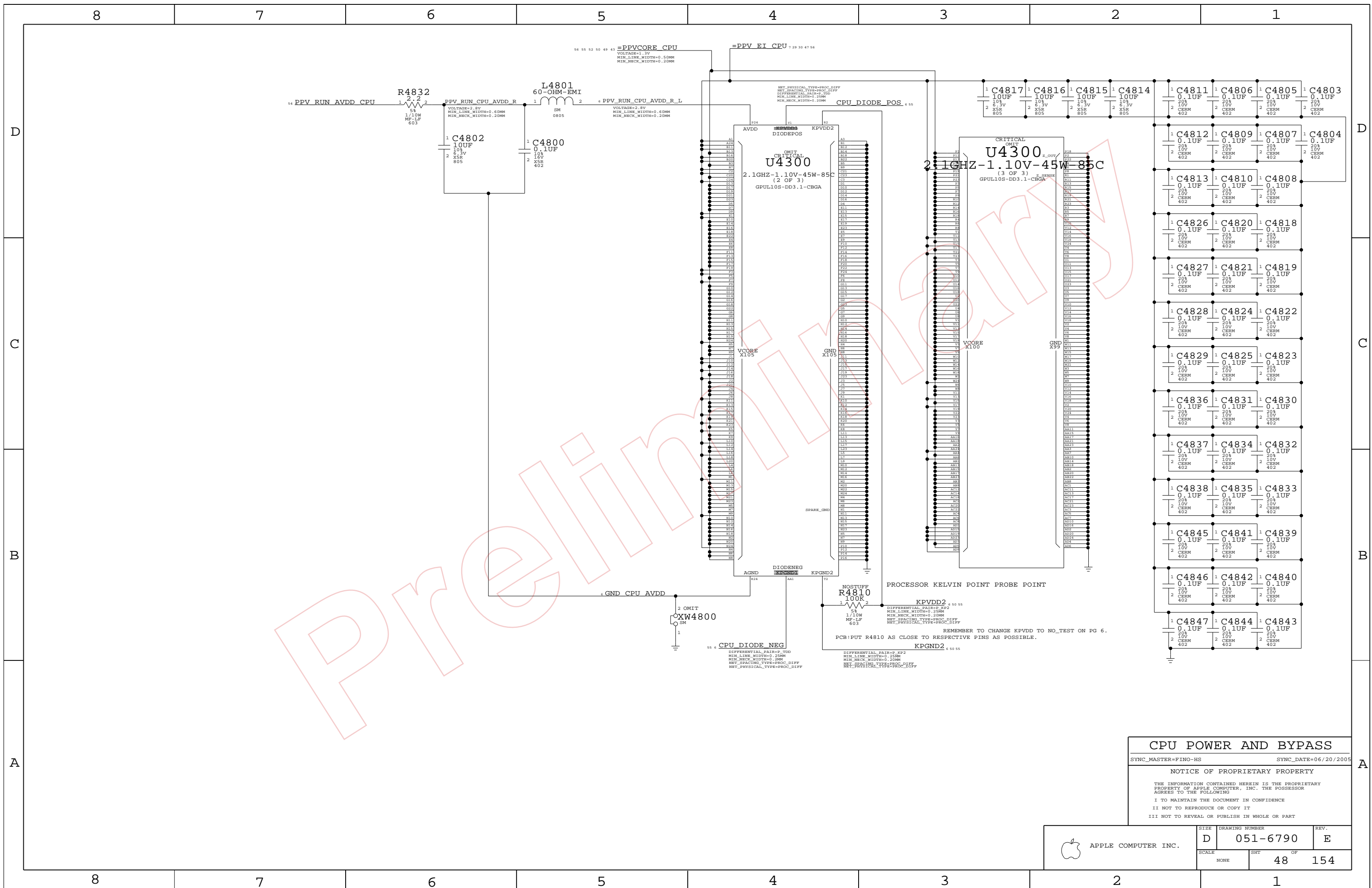
SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	NONE	SHT	OF
		47	154



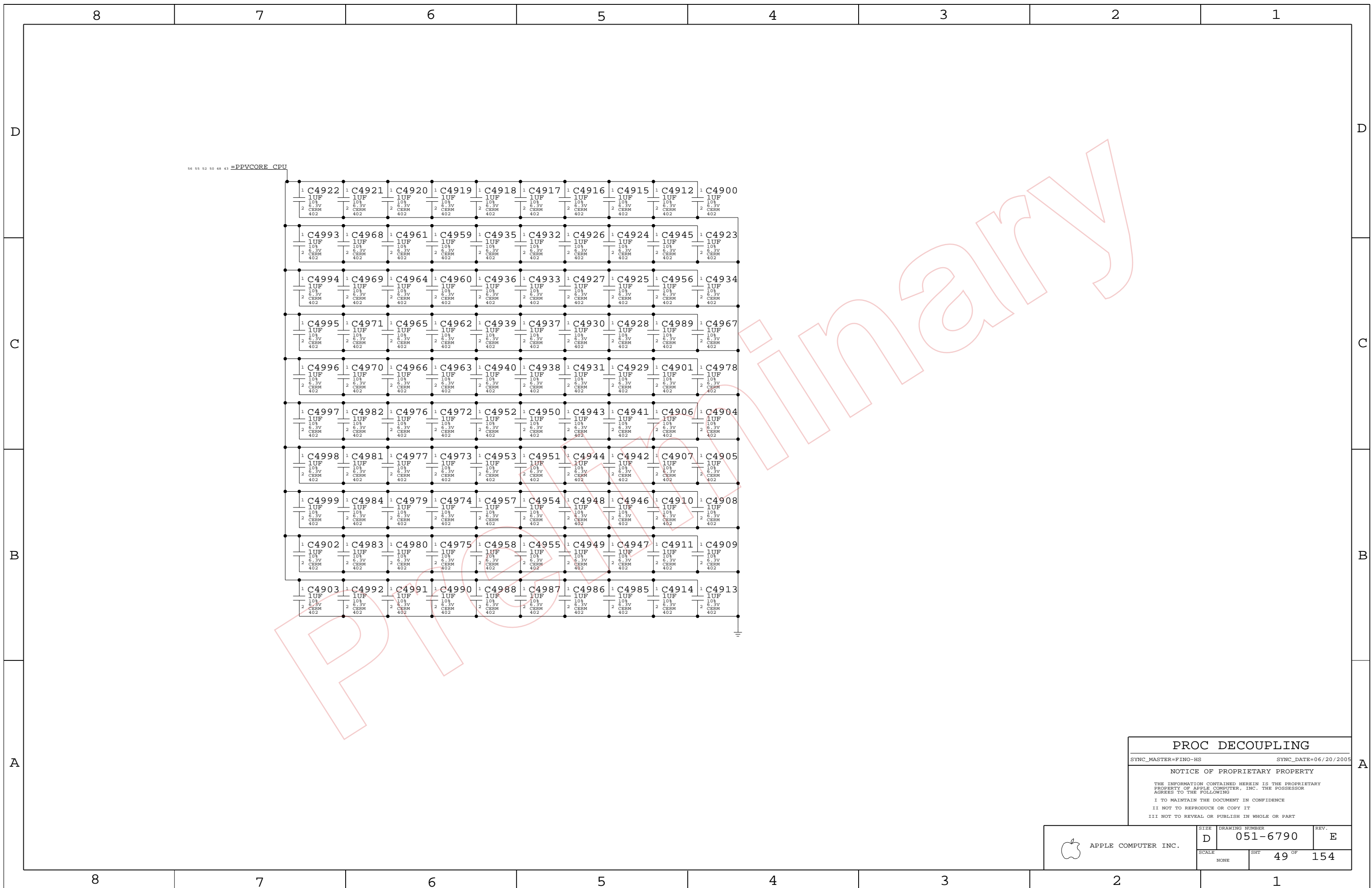
CPU POWER AND BYPASS

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	NONE	SHT	OF
		48	154



PROC DECOUPLING

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

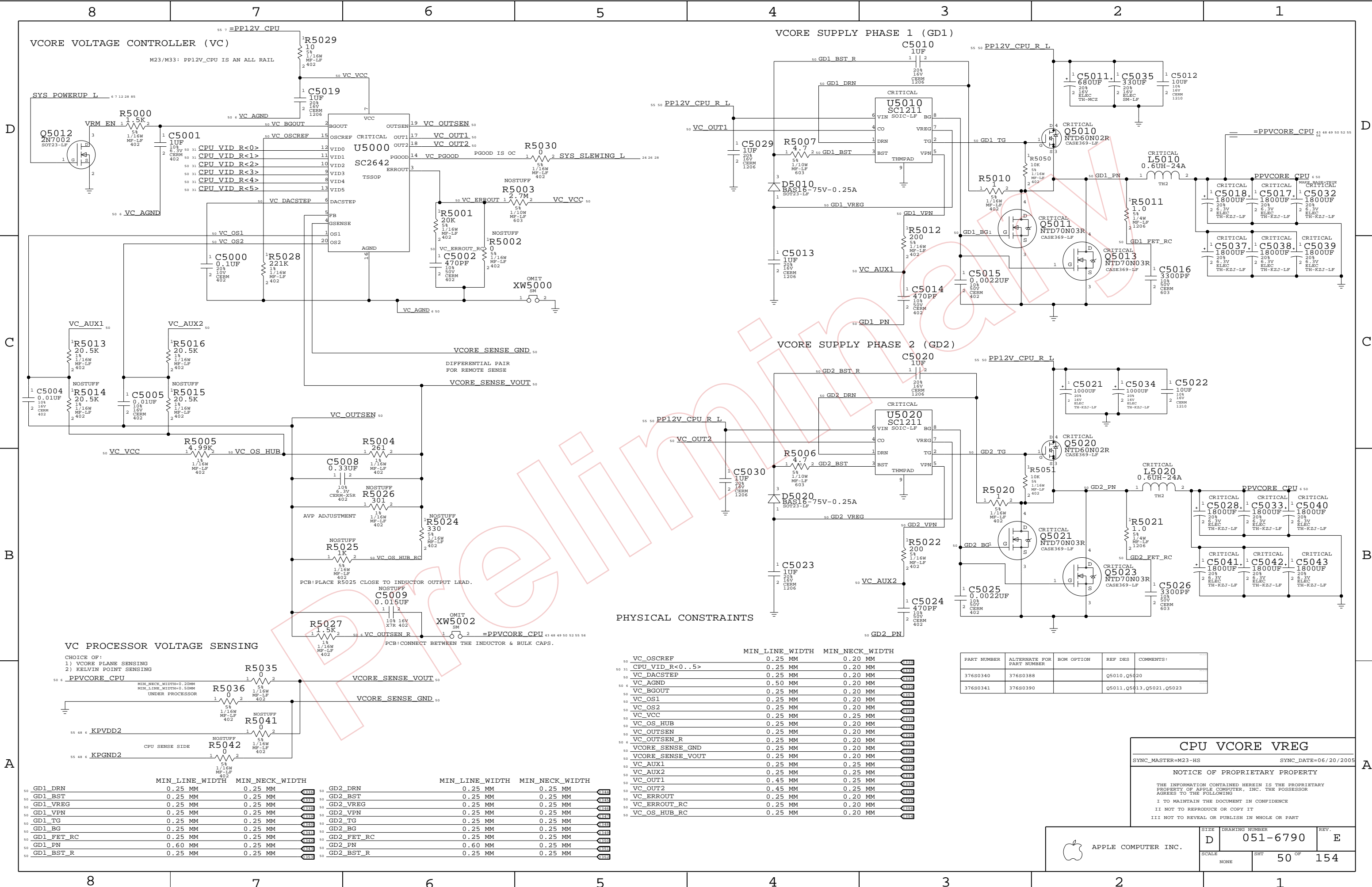
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHT 49 OF	154



VCORE VOLTAGE CONTROLLER (VC)

VCORE SUPPLY PHASE 1 (GD1)

VCORE SUPPLY PHASE 2 (GD2)

VC PROCESSOR VOLTAGE SENSING

PHYSICAL CONSTRAINTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0340	376S0388		Q5010, Q5020	
376S0341	376S0390		Q5011, Q5013, Q5021, Q5023	

MIN_LINE_WIDTH	MIN_NECK_WIDTH	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD1_DRN	0.25 MM	GD2_DRN	0.25 MM
GD1_BST	0.25 MM	GD2_BST	0.25 MM
GD1_VREG	0.25 MM	GD2_VREG	0.25 MM
GD1_VPN	0.25 MM	GD2_VPN	0.25 MM
GD1_TG	0.25 MM	GD2_TG	0.25 MM
GD1_BG	0.25 MM	GD2_BG	0.25 MM
GD1_FET_RC	0.25 MM	GD2_FET_RC	0.25 MM
GD1_PN	0.60 MM	GD2_PN	0.60 MM
GD1_BST_R	0.25 MM	GD2_BST_R	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
VC_OSCREF	0.25 MM	0.20 MM
CPU_VID_R<0..5>	0.25 MM	0.20 MM
VC_DACSTEP	0.25 MM	0.20 MM
VC_AGN2	0.50 MM	0.20 MM
VC_BGOUT	0.25 MM	0.20 MM
VC_OS1	0.25 MM	0.20 MM
VC_OS2	0.25 MM	0.20 MM
VC_VCC	0.25 MM	0.25 MM
VC_OS_HUB	0.25 MM	0.20 MM
VC_OUTSEN	0.25 MM	0.20 MM
VC_OUTSEN_R	0.25 MM	0.20 MM
VCORE_SENSE_GND	0.25 MM	0.20 MM
VCORE_SENSE_VOUT	0.25 MM	0.20 MM
VC_AUX1	0.25 MM	0.25 MM
VC_AUX2	0.25 MM	0.25 MM
VC_OUT1	0.45 MM	0.25 MM
VC_OUT2	0.45 MM	0.25 MM
VC_ERROUT	0.25 MM	0.20 MM
VC_ERROUT_RC	0.25 MM	0.20 MM
VC_OS_HUB_RC	0.25 MM	0.20 MM

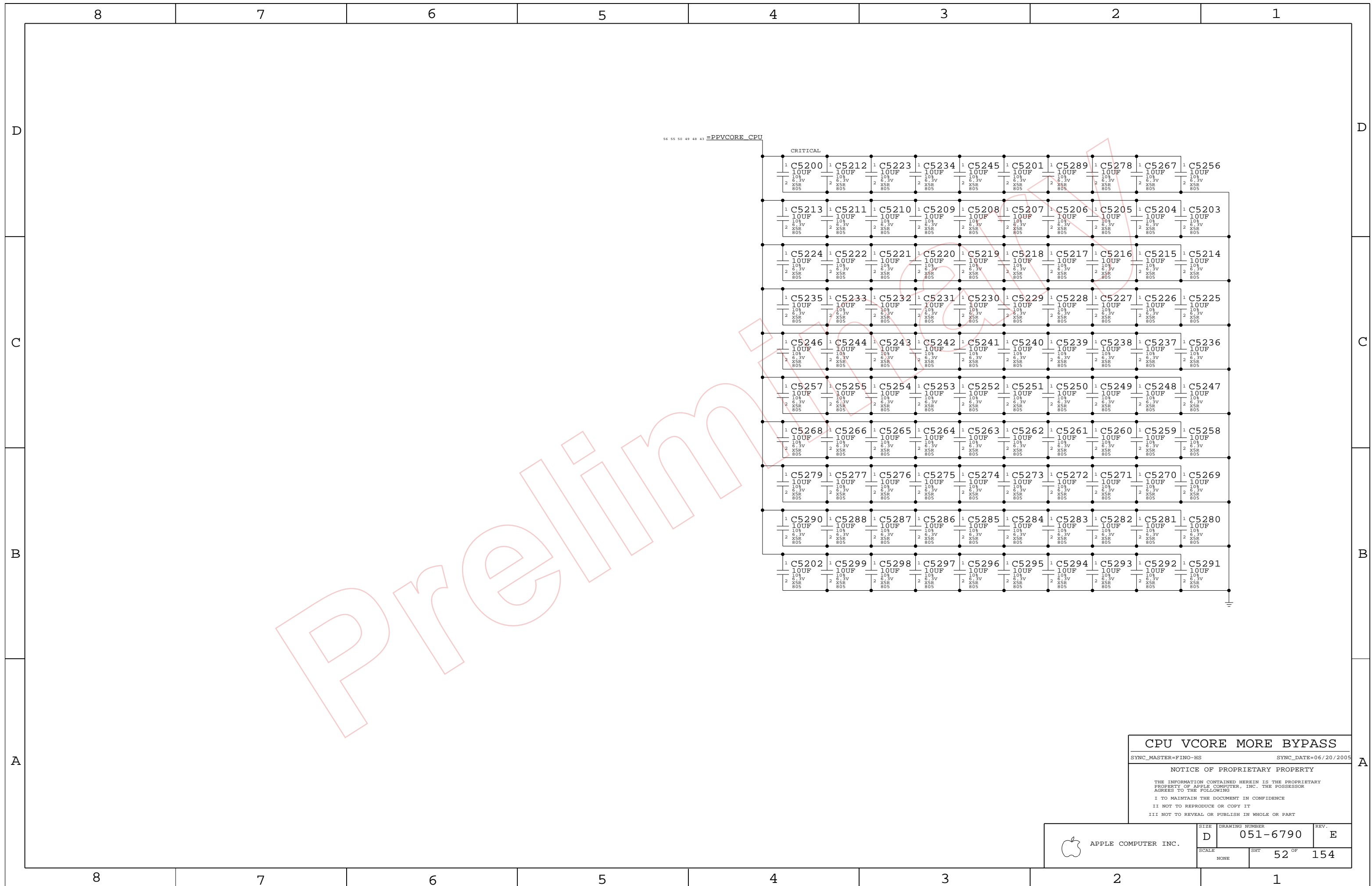
CPU VCORE VREG

SYNC_MASTER=M23-HS SYNC_DATE=06/20/2005

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	D	051-6790	E
SCALE	SHT	50 OF	154
NONE			




CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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	D	051-6790	E
SCALE	SHT		OF
NONE	52		154

8

7

6

5

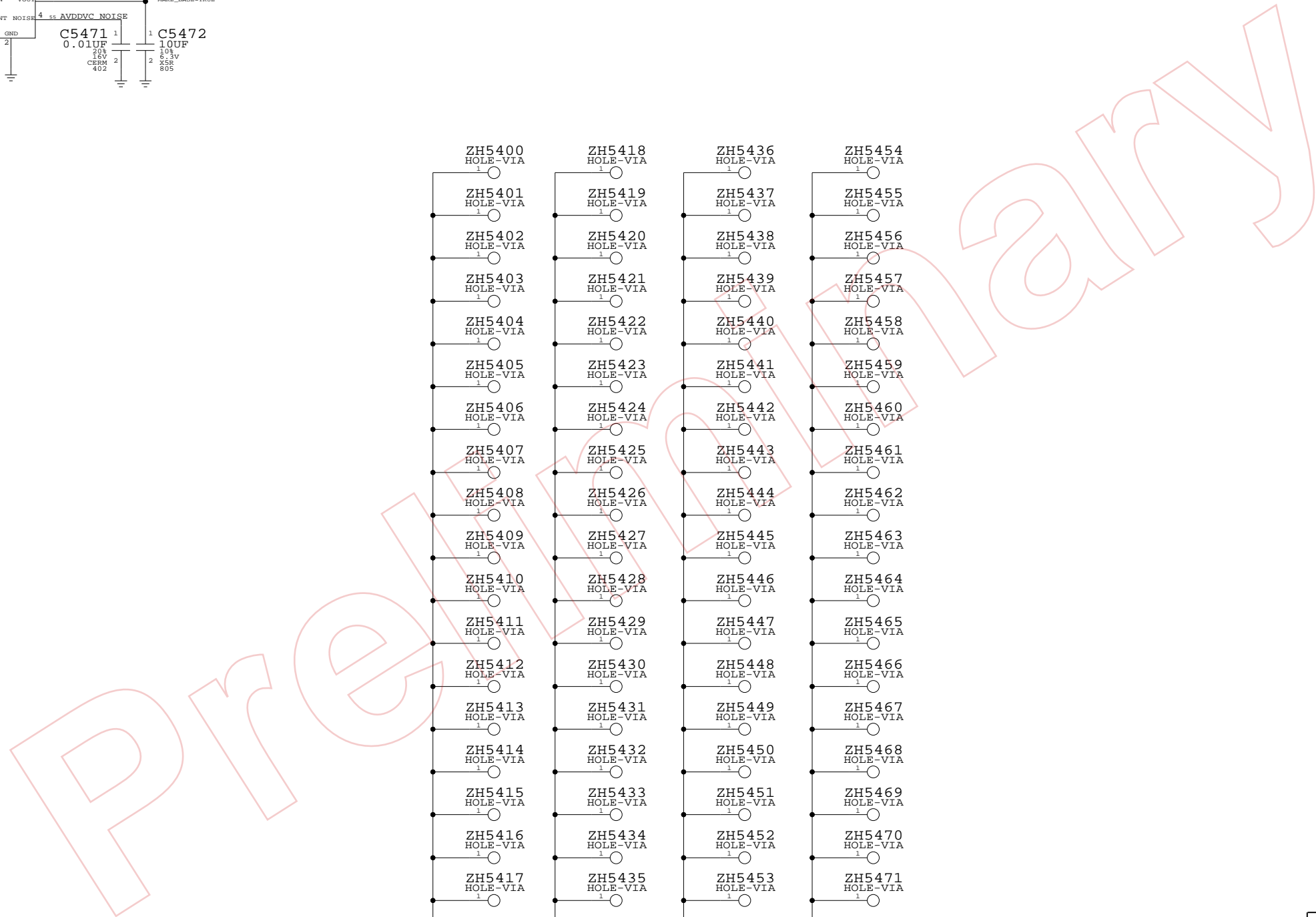
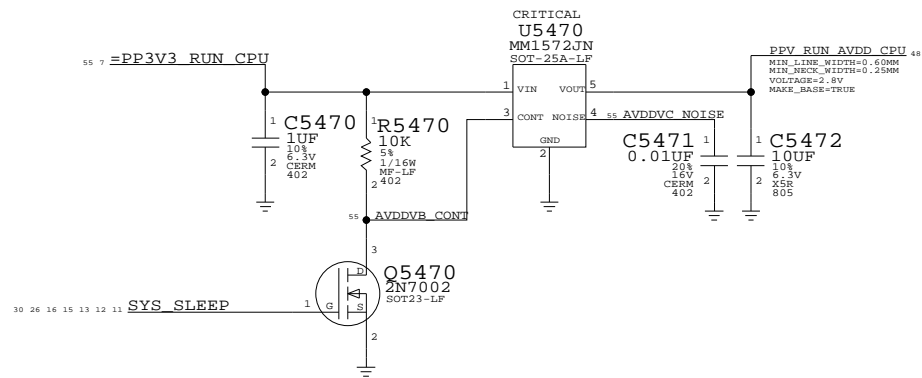
4

3

2

1

PROCESSOR AVDD VREG



CPU AVDD VREG

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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	D	051-6790	E
SCALE	SHT	OF	
NONE	54	154	

8

7

6

5

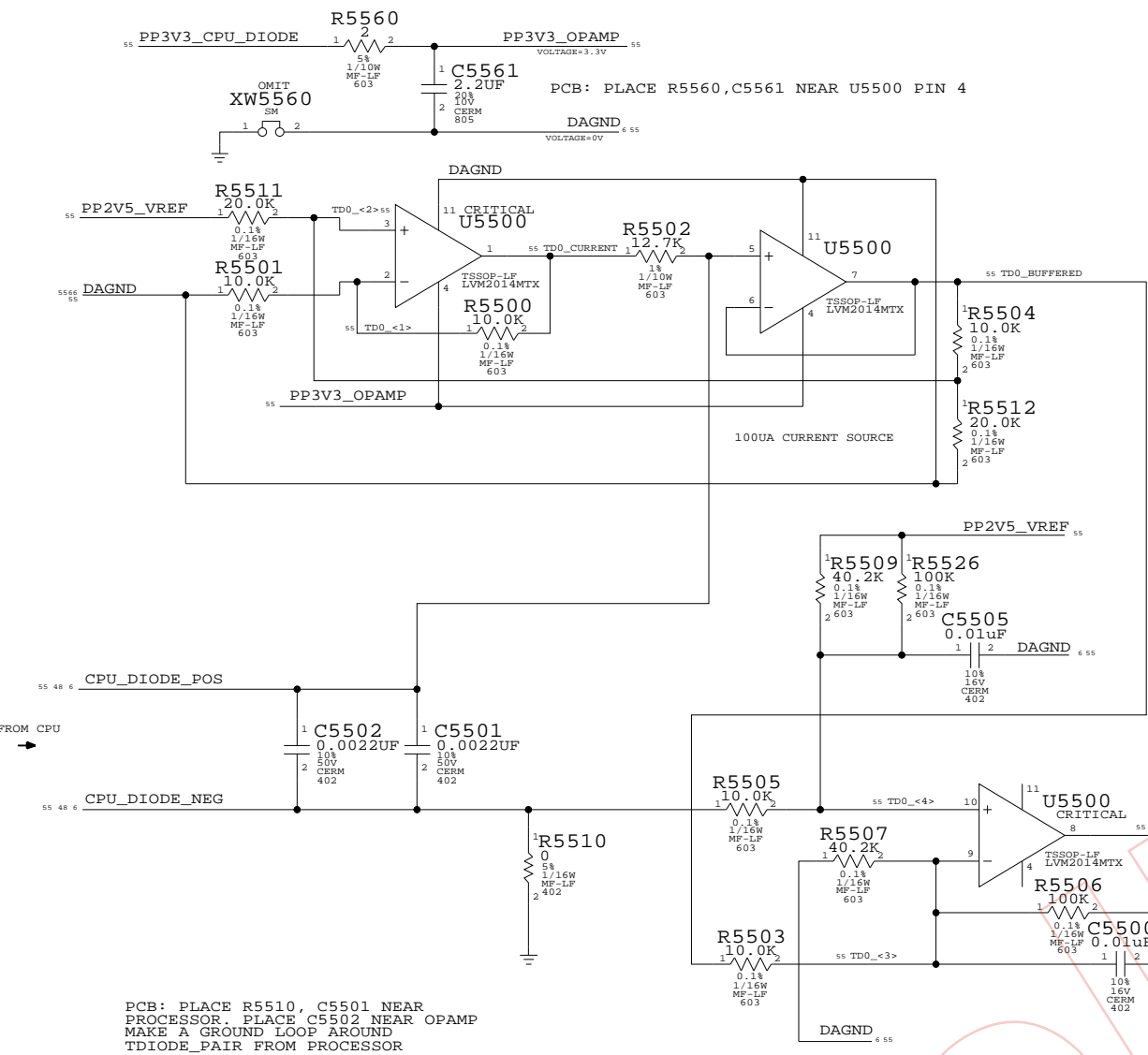
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3

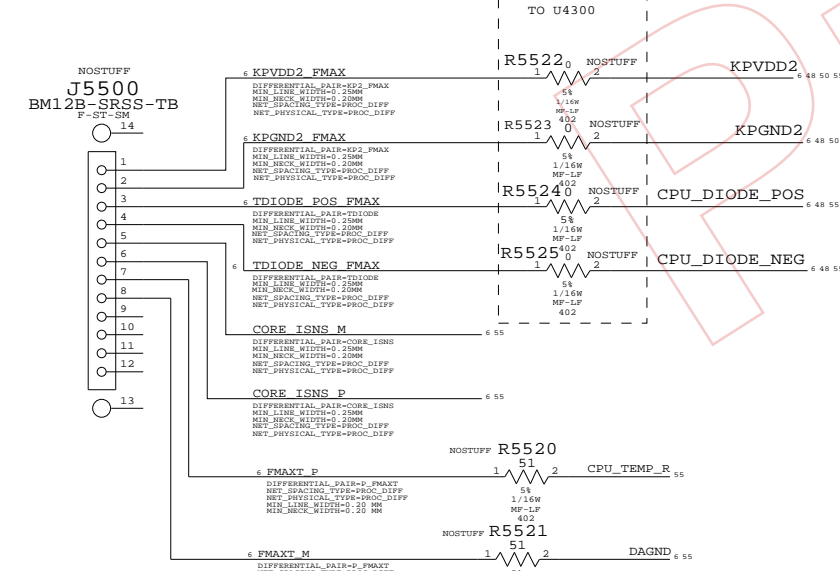
2

1

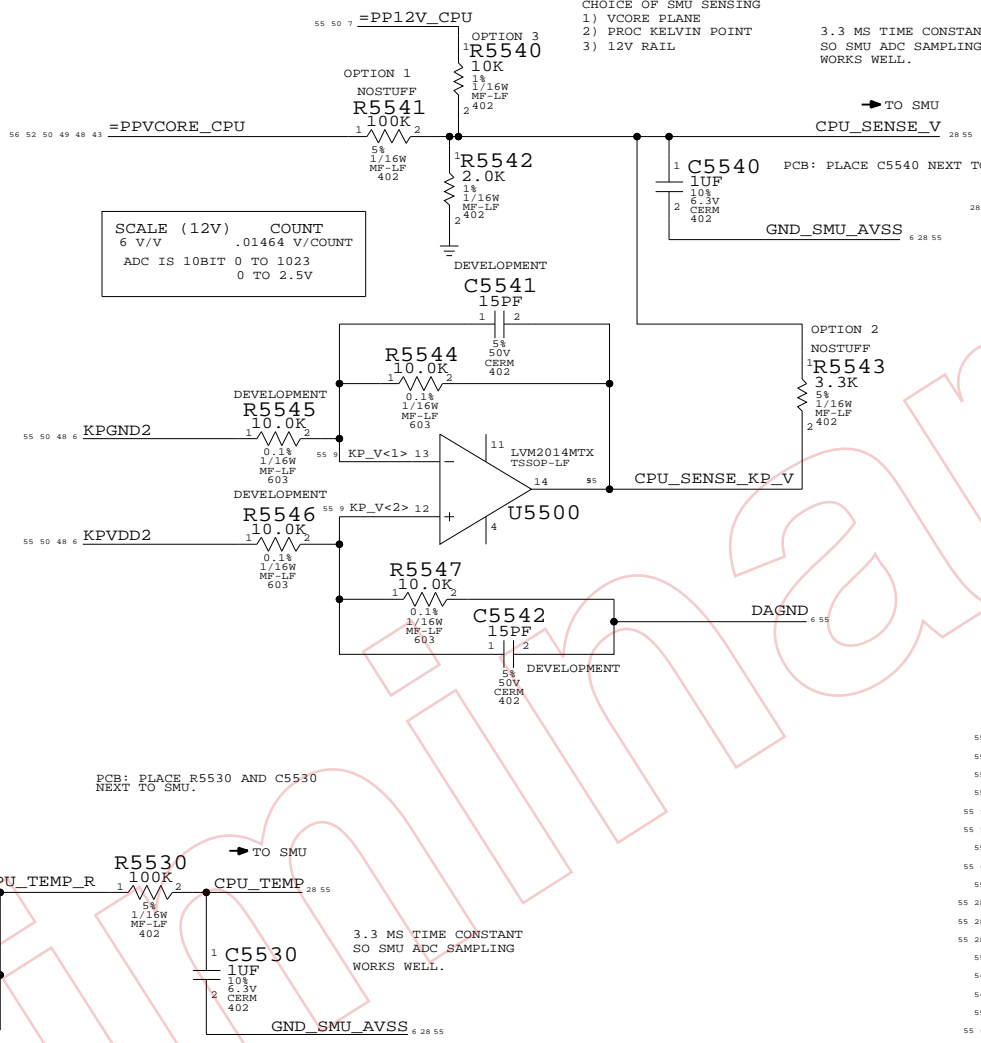
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



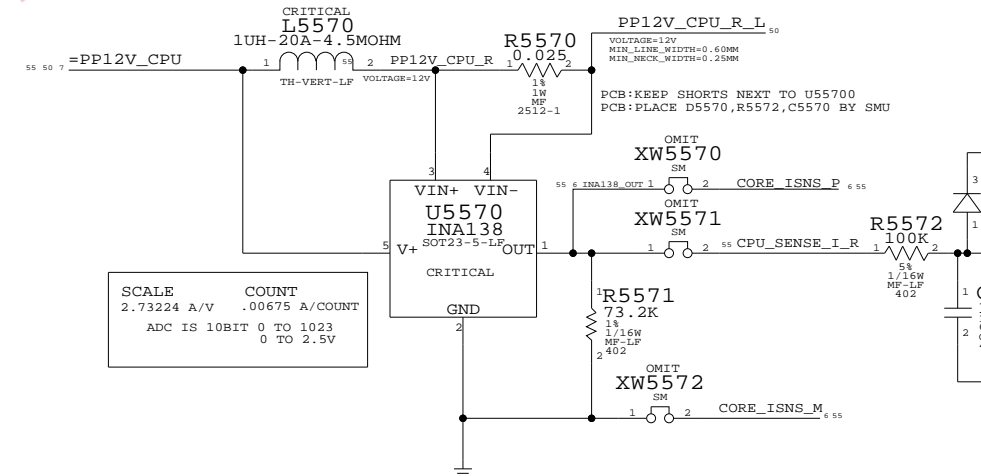
FMAX CONNECTOR



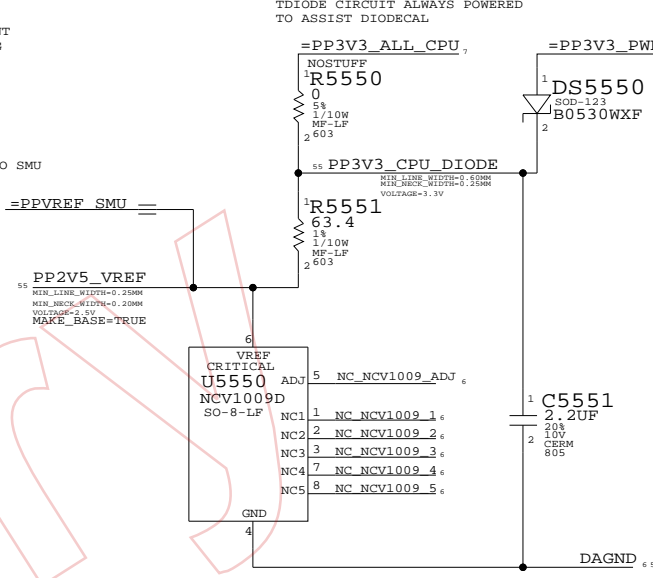
PROCESSOR VCORE VOLTAGE SENSE



PROCESSOR VCORE CURRENT SENSE (USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



2.5V PRECISION VOLTAGE REFERENCE SOURCE



PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
TD0_<1..4>	0.25 MM	0.25 MM
PP12V_CPU_R	0.60 MM	0.25 MM
TD0_CURRENT	0.25 MM	0.25 MM
TD0_BUFFERED	0.25 MM	0.25 MM
KP_V<1..2>	0.25 MM	0.25 MM
CPU_SENSE_KP_V	0.25 MM	0.25 MM
PP3V3_OPAMP	0.60 MM	0.25 MM
INA138_OUT	0.25 MM	0.25 MM
CPU_SENSE_I_R	0.25 MM	0.25 MM
CPU_SENSE_I	0.25 MM	0.25 MM
CPU_SENSE_V	0.25 MM	0.25 MM
CPU_TEMP	0.25 MM	0.20 MM
CPU_TEMP_R	0.25 MM	0.20 MM
AVDDVC_NOISE	0.25 MM	0.20 MM
AVDDVB_CONT	0.25 MM	0.20 MM
PP12V_CPU_R	0.60 MM	0.25 MM
DAGND	0.60 MM	0.25 MM

T, V, I SENSORS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

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	D	051-6790	E
SCALE	SHEET	OF	
NONE	55	154	

CONNECT PULSAR CLKS TO CPU/NB

Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include EI_CPU_SYSCLK_P, EI_CPU_SYSCLK_N, EI_CPU_APSYNC, EI_CPU_TREN_CLK, and EI_NB_APSYNC.

CONNECT KODIAK EI A TO/FROM CPU

Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include EI_NB_TO_CPU_CLK_P, EI_NB_TO_CPU_CLK_N, EI_NB_TO_CPU_AD<0..43>, EI_NB_TO_CPU_SR_P<0..1>, and EI_NB_TO_CPU_SR_N<0..1>.

Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include EI_CPU_TO_NB_CLK_P, EI_CPU_TO_NB_CLK_N, EI_CPU_TO_NB_AD<0..43>, EI_CPU_TO_NB_SR_P<0..1>, and EI_CPU_TO_NB_SR_N<0..1>.

CONNECT CPU TO KODIAK QREQ A0

Table with 4 columns: Pin, Signal Name, Component, and Pin. Row: CPU_TO_NB_QREQ_L, CPU_A0_TO_NB_QREQ_L.

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include CPU_QACK_L, NC_CPU_A1_QACK_L, NC_CPU_B0_QACK_L, and NC_CPU_B1_QACK_L.

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include CPU_INT_L, NC_NB_CPU_A1_INT_L, NC_NB_CPU_B0_INT_L, and NC_NB_CPU_B1_INT_L.

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

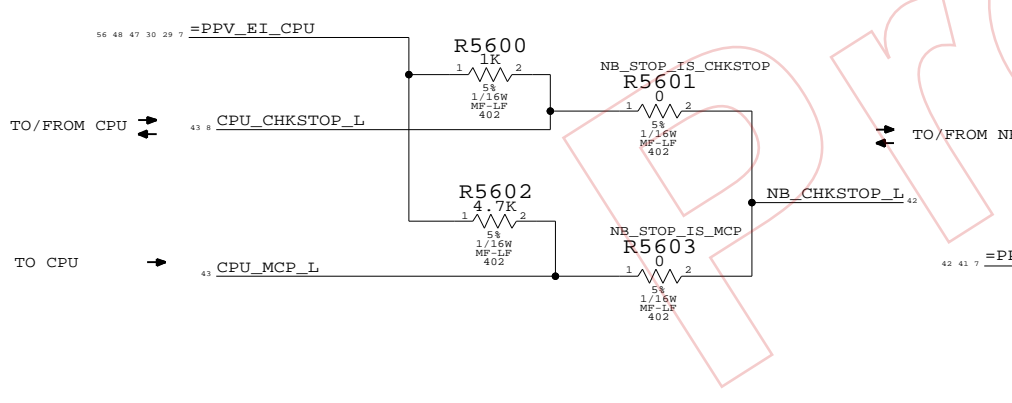
Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include CPU_SRESET_L_R, NOTUSED_CPU_A1_SRESET_L, NOTUSED_CPU_B0_SRESET_L, and NOTUSED_CPU_B1_SRESET_L.

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include TP_NB_B_TRIGGER_OUT, TP_NB_A_TRIGGER_OUT, TP_CPU_APSYNCOUT, TP_CPU_TRIGGER_IN, TP_CPU_TRIGGER_OUT, NC_PSR0, NC_PSR0_ENABLE, TP_CPU_ATTENTION, and NC_CPU_AFN.

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU_CHKSTOP OR MCP TO NB



EI BUS AND SYSCLK CONSTRAINT LABELS

Table with 5 columns: Signal Name, ELECTRICAL_CONSTRAINT_SET, NET_SPACING_TYPE, NET_PHYSICAL_TYPE, and DIFFERENTIAL_PAIR. Rows include EI_CPU_TO_NB_CLK_P, EI_CPU_TO_NB_CLK_N, EI_CPU_TO_NB_AD<0..21>, EI_CPU_TO_NB_SR_P<0..1>, EI_CPU_TO_NB_SR_N<0..1>, EI_NB_TO_CPU_CLK_P, EI_NB_TO_CPU_CLK_N, EI_NB_TO_CPU_AD<0..43>, EI_NB_TO_CPU_SR_P<0..1>, EI_NB_TO_CPU_SR_N<0..1>, EI_NB_APSYNC, EI_CPU_APSYNC, EI_CPU_SYSCLK_P, EI_CPU_SYSCLK_N, EI_NB_SYSCLK_P, EI_NB_SYSCLK_N, EI_CPU_TO_NB_AD<22>, and EI_CPU_TO_NB_AD<23..43>.

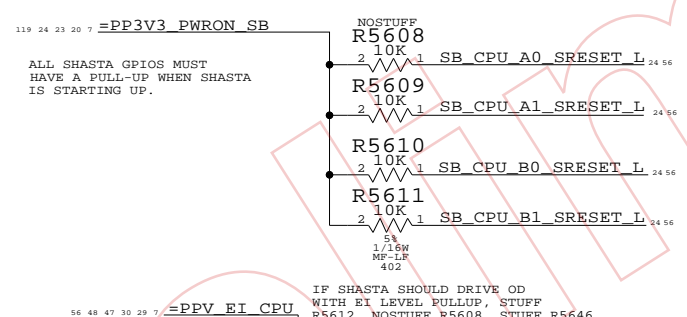
NC KODIAK EI B OUTPUT PORT

Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include NC_EI_NB_TO_CPU_B_CLK_P, NC_EI_NB_TO_CPU_B_CLK_N, NC_EI_NB_TO_CPU_B_AD<0..43>, NC_EI_NB_TO_CPU_B_SR_P<0..1>, and NC_EI_NB_TO_CPU_B_SR_N<0..1>.

NC KODIAK EI B INPUT PORT

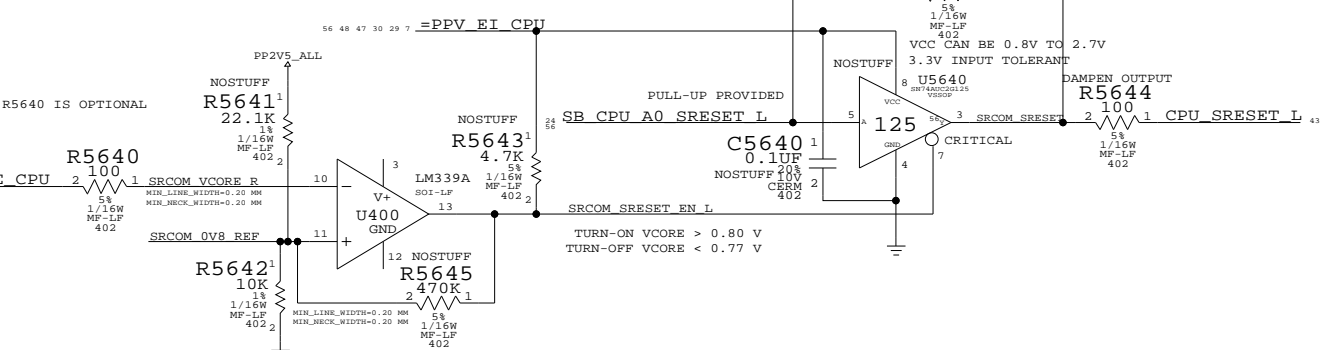
Table with 4 columns: Pin, Signal Name, Component, and Pin. Rows include NC_EI_CPU_B_TO_NB_CLK_P, NC_EI_CPU_B_TO_NB_CLK_N, NC_EI_CPU_B_TO_NB_AD<0..43>, NC_EI_CPU_B_TO_NB_SR_P<0..1>, and NC_EI_CPU_B_TO_NB_SR_N<0..1>.

PULLUPS FOR SRESET'S FROM SHASTA



SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVOID IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.



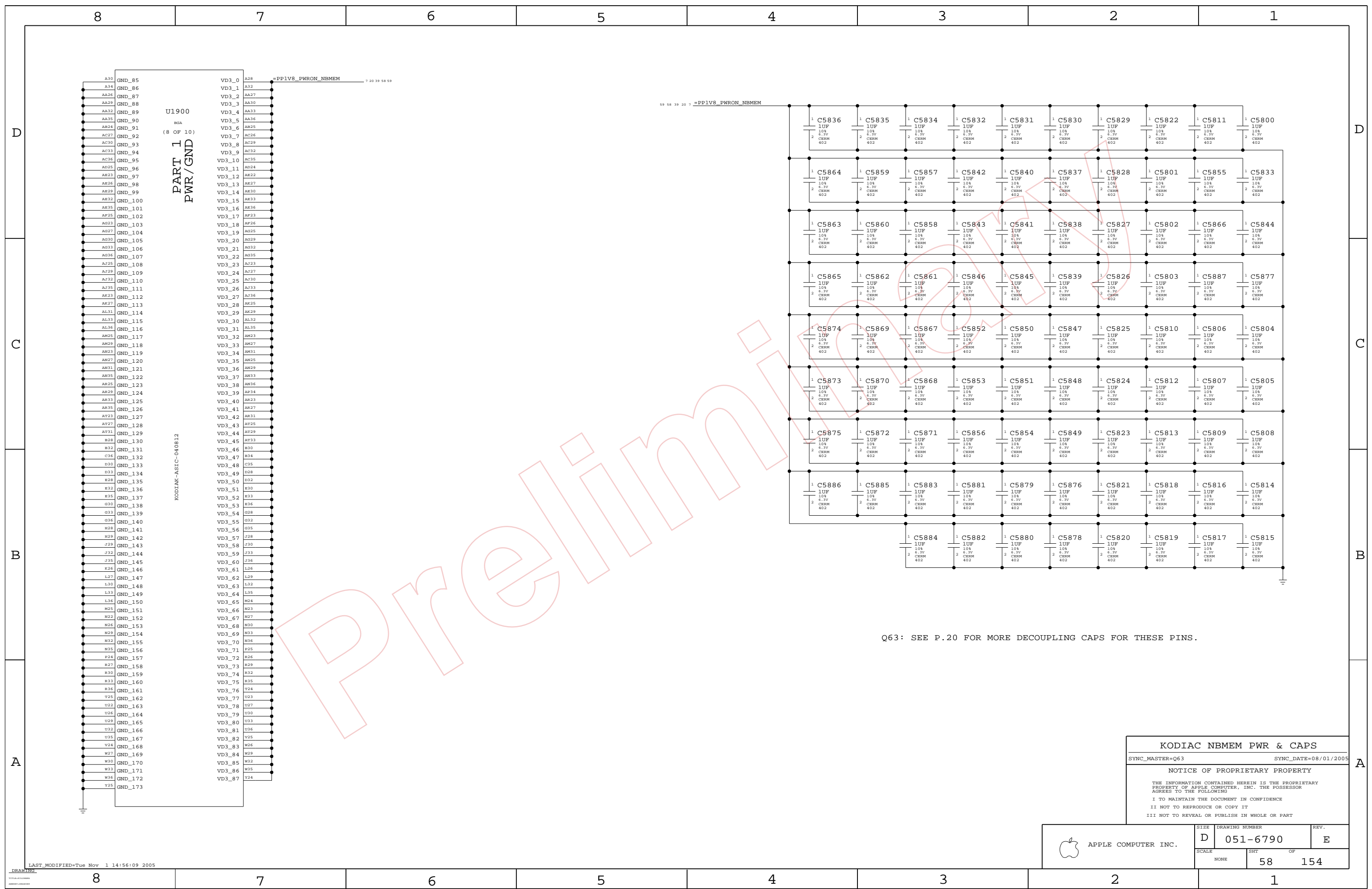
NOTE, NB UNUSED INTS DO NOT REQUIRE PULLUPS, ONLY SHASTA (SINCE ITS OUTPUTS ARE TEMPORARILY INPUTS ON BOOTUP).

INT PULLUP IS SO INT PIN IS NOT FLOATING TO PROCESSOR BUT WEAK TO ALLOW KODIAK TO DRIVE PUSH-PULL STRONGLY

CPU ALIASES & MISC

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Table with 3 columns: Apple Computer Inc. logo, Drawing Number (D 051-6790), and Revision (E). Below it is a table with 4 columns: SCALE (NONE), SHEET (56 OF), and PART (154).



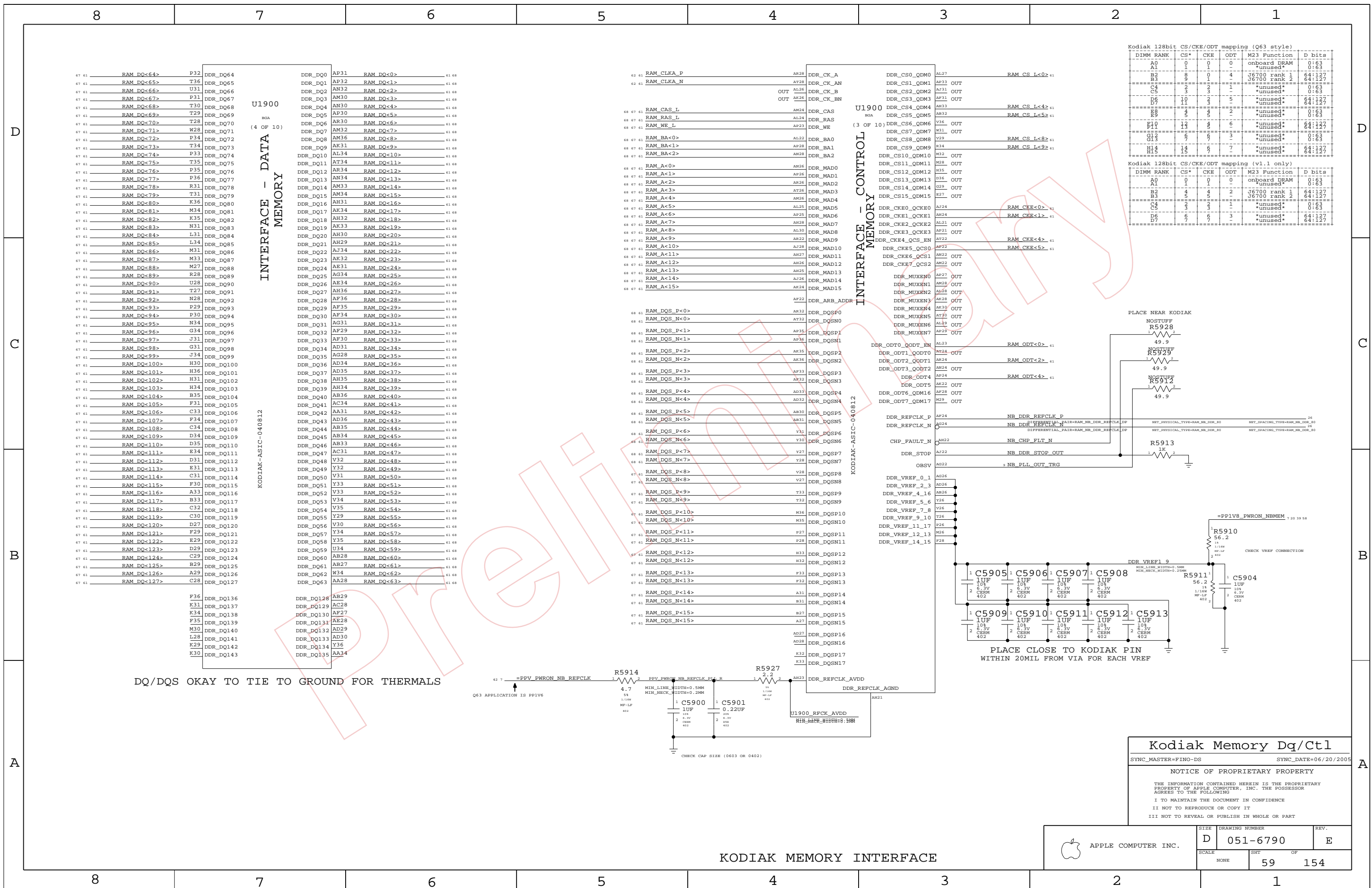
U1900
(8 OF 10)
PART 1 OF 10
PWR/GND

KODIAK-AS1C-040812

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAK NBMEM PWR & CAPS
 SYNC_MASTER=Q63 SYNC_DATE=08/01/2005
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	D	051-6790	E
SCALE	SHT OF		
NONE	58 OF		154



U1900
BGA
(4 OF 10)
INTERFACE - DATA
MEMORY

U1900
BGA
(3 OF 10)
INTERFACE - CONTROL
MEMORY

Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	1	0	onboard DRAM	0:63
A1	1	1	0	*unused*	0:63
B2	8	0	4	U6700 rank 1	64:127
B3	9	1	1	U6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	2	1	*unused*	0:63
D6	10	3	2	*unused*	0:63
D7	11	3	2	*unused*	0:63
E8	5	5	5	*unused*	64:127
E9	6	5	5	*unused*	64:127
F10	13	4	6	*unused*	64:127
F11	14	4	6	*unused*	64:127
G12	7	3	3	*unused*	0:63
G13	9	3	3	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	6	7	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	1	0	onboard DRAM	0:63
A1	1	1	0	*unused*	0:63
B2	4	4	2	U6700 rank 1	64:127
B3	5	5	5	U6700 rank 2	64:127
C4	3	3	1	*unused*	0:63
C5	3	3	1	*unused*	0:63
D6	6	7	7	*unused*	64:127
D7	7	7	7	*unused*	64:127

DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS

PLACE CLOSE TO KODIAK PIN
WITHIN 20MIL FROM VIA FOR EACH VREF

Kodiak Memory Dq/Ctl

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

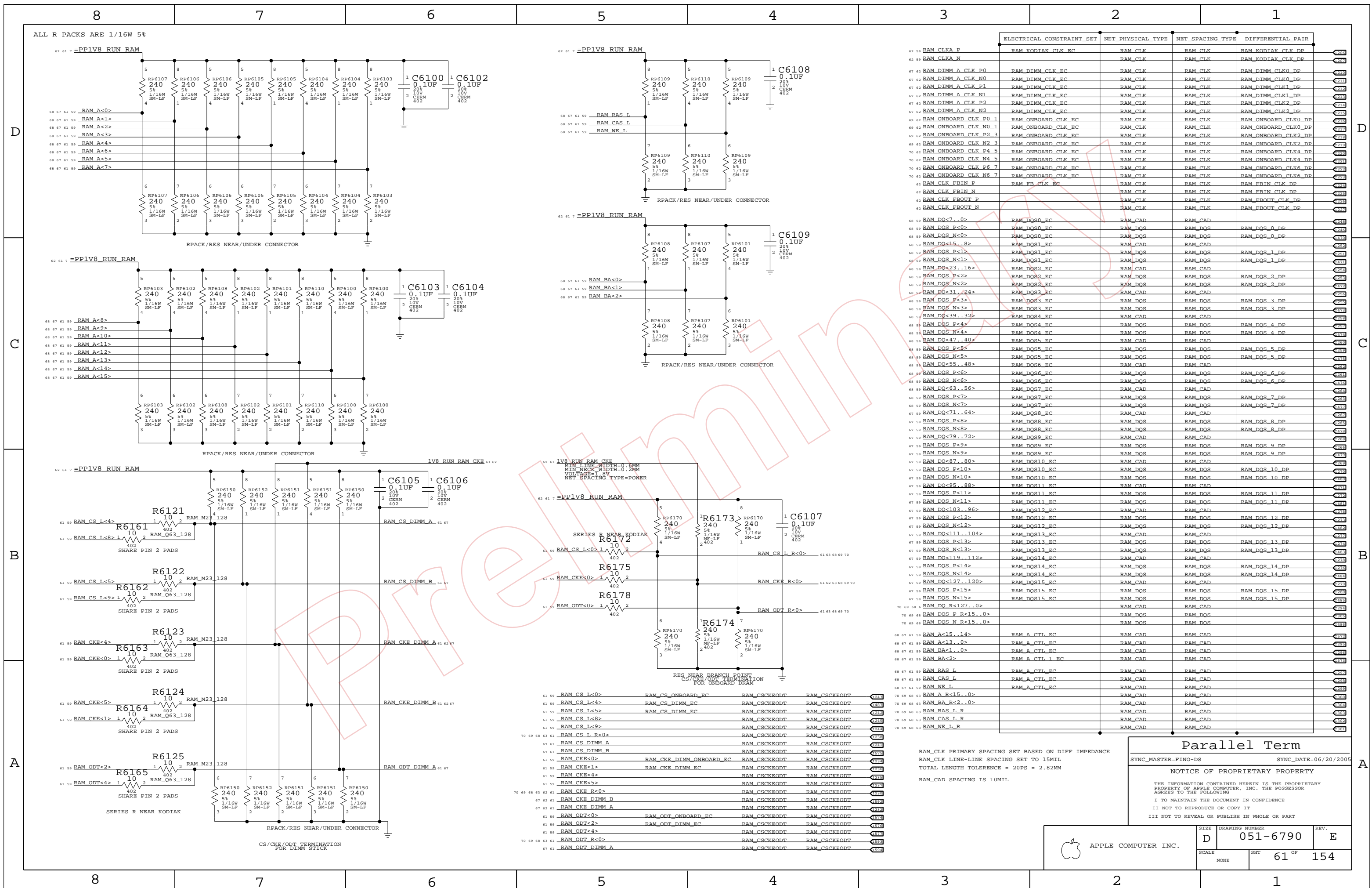
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SCALE NONE	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHEET 59	OF 154

KODIAK MEMORY INTERFACE



APPLE COMPUTER INC.

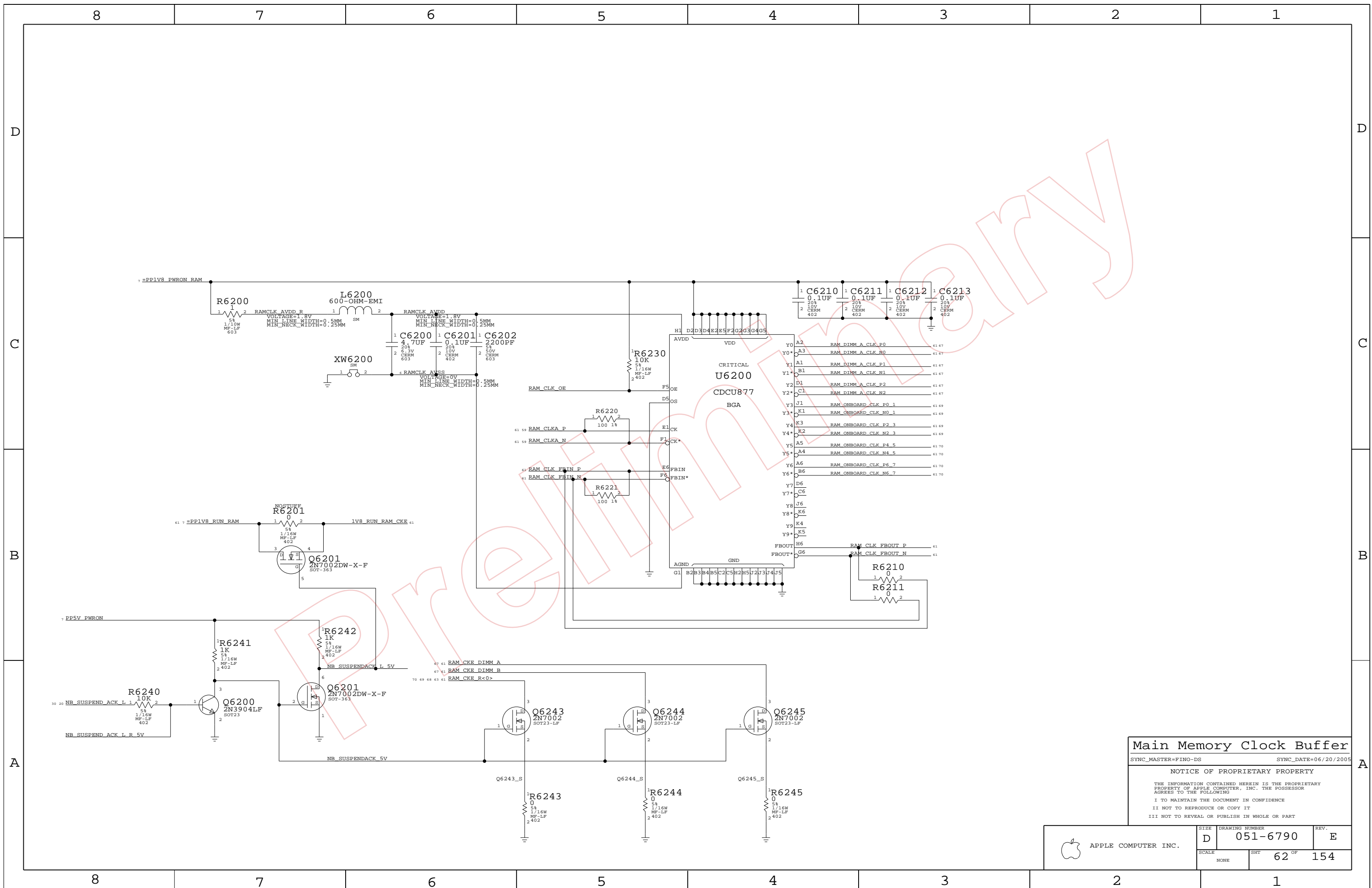


ALL R PACKS ARE 1/16W 5%

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
RAM_CLKA_P	RAM_CLK	RAM_CLK	RAM_CLKDIAK_CLK_DP
RAM_CLKA_N	RAM_CLK	RAM_CLK	RAM_CLKDIAK_CLK_DP
RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK0_DP
RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK0_DP
RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK1_DP
RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK1_DP
RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK2_DP
RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK2_DP
RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK0_DP
RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK0_DP
RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK2_DP
RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK2_DP
RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK4_DP
RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK4_DP
RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK6_DP
RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK6_DP
RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBIN_CLK_DP
RAM_CLK_FBIN_N	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBIN_CLK_DP
RAM_CLK_FBOUT_P	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBOUT_CLK_DP
RAM_CLK_FBOUT_N	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBOUT_CLK_DP
RAM_DS0<7..0>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<0>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<0>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<15..8>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<1>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<1>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<23..16>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<2>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<2>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<31..24>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<3>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<3>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<39..32>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<4>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<4>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<47..40>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<5>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<5>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<55..48>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<6>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<6>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<63..56>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<7>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<7>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<71..64>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<8>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<8>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<79..72>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<9>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<9>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<87..80>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<10>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<10>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<95..88>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<11>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<11>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<103..96>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<12>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<12>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<111..104>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<13>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<13>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<119..112>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<14>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<14>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<127..120>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<15>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<15>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<127..0>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P_R<15..0>	RAM_DS0	RAM_DS0	RAM_DS0_DP
RAM_DS0_N_R<15..0>	RAM_DS0	RAM_DS0	RAM_DS0_DP
RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_A_CTL_DP
RAM_BAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_A_R<15..0>	RAM_CAD	RAM_CAD	RAM_CAD
RAM_BA_R<2..0>	RAM_CAD	RAM_CAD	RAM_CAD
RAM_RAS_L_R	RAM_CAD	RAM_CAD	RAM_CAD
RAM_CAS_L_R	RAM_CAD	RAM_CAD	RAM_CAD
RAM_WE_L_R	RAM_CAD	RAM_CAD	RAM_CAD

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
 RAM_CLK LINE-LINE SPACING SET TO 15MIL
 TOTAL LENGTH TOLERANCE = 20PS = 2.82MM
 RAM_CAD SPACING IS 10MIL

Parallel Term
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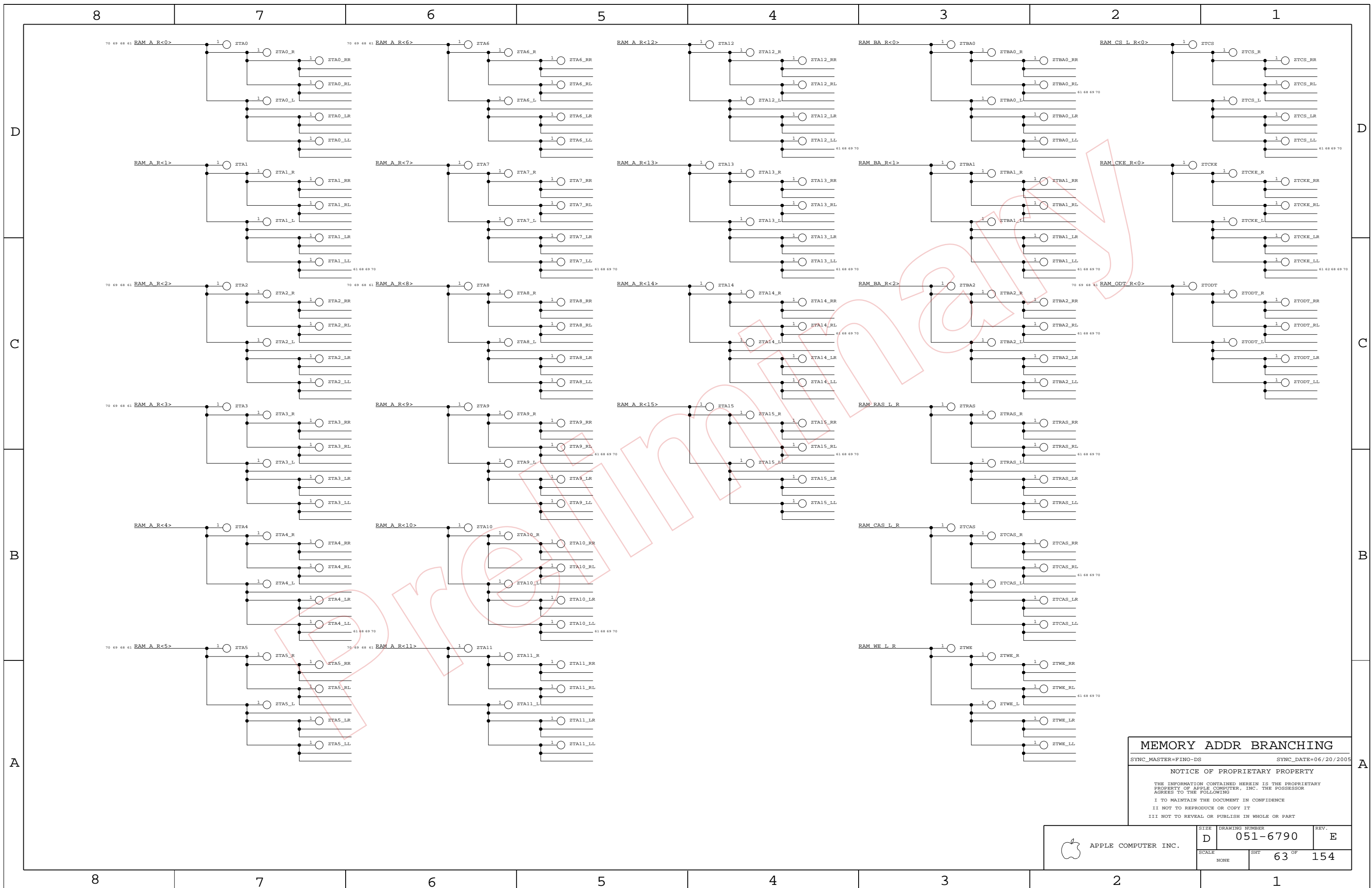
Main Memory Clock Buffer

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SCALE	SHT	OF	
NONE	62	154	




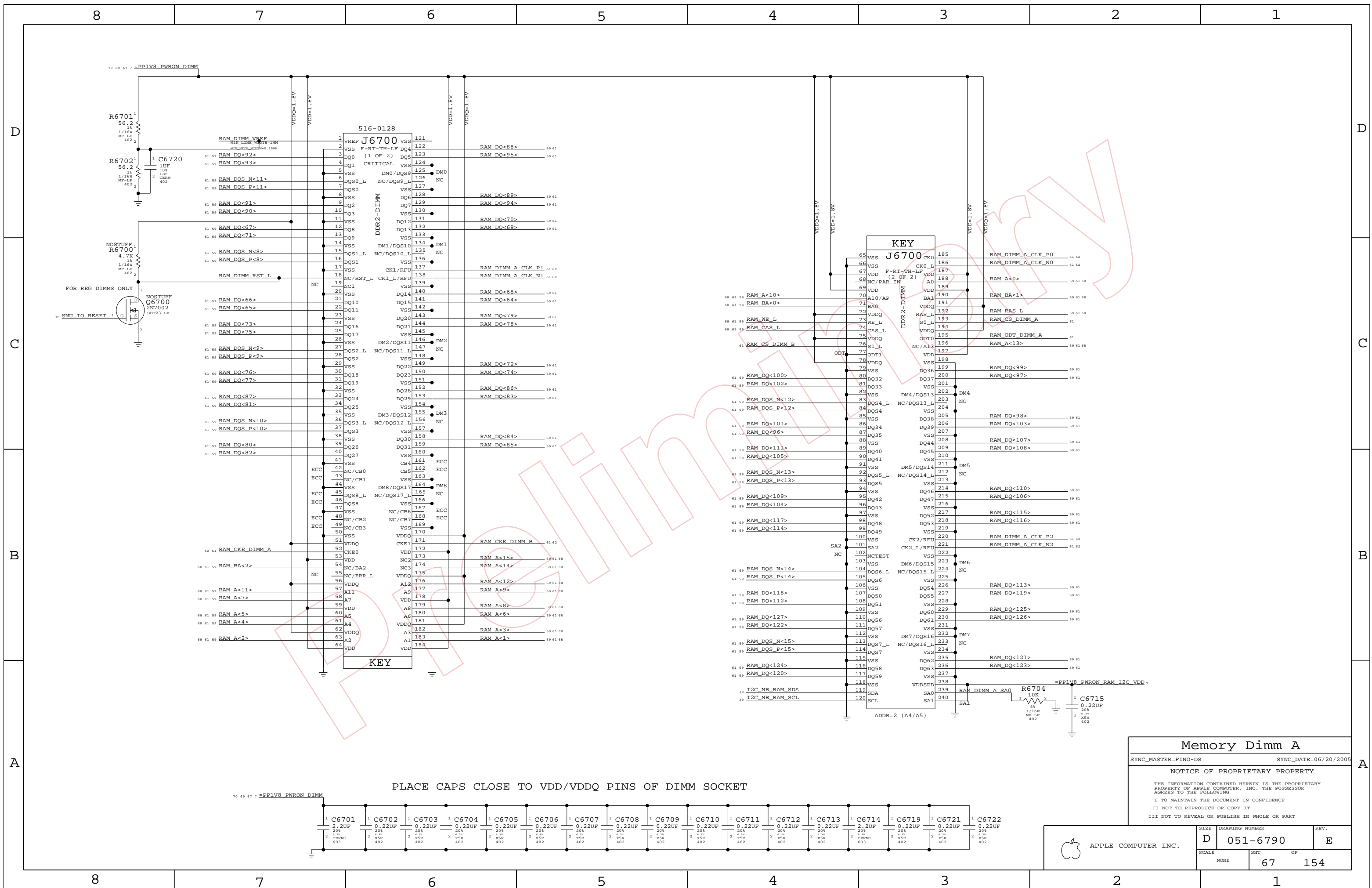
MEMORY ADDR BRANCHING

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

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SCALE	SHT	63 OF 154	
NONE			



PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET

1	C6701	2.2UF	20%	CSRM1	609	2	C6702	0.22UF	20%	X5R	402	3	C6703	0.22UF	20%	X5R	402	4	C6704	0.22UF	20%	X5R	402	5	C6705	0.22UF	20%	X5R	402	6	C6706	0.22UF	20%	X5R	402	7	C6707	0.22UF	20%	X5R	402	8	C6708	0.22UF	20%	X5R	402	9	C6709	0.22UF	20%	X5R	402	10	C6710	0.22UF	20%	X5R	402	11	C6711	0.22UF	20%	X5R	402	12	C6712	0.22UF	20%	X5R	402	13	C6713	0.22UF	20%	X5R	402	14	C6714	2.2UF	20%	CSRM1	609	15	C6719	0.22UF	20%	X5R	402	16	C6721	0.22UF	20%	X5R	402	17	C6722	0.22UF	20%	X5R	402
---	-------	-------	-----	-------	-----	---	-------	--------	-----	-----	-----	---	-------	--------	-----	-----	-----	---	-------	--------	-----	-----	-----	---	-------	--------	-----	-----	-----	---	-------	--------	-----	-----	-----	---	-------	--------	-----	-----	-----	---	-------	--------	-----	-----	-----	---	-------	--------	-----	-----	-----	----	-------	--------	-----	-----	-----	----	-------	--------	-----	-----	-----	----	-------	--------	-----	-----	-----	----	-------	--------	-----	-----	-----	----	-------	-------	-----	-------	-----	----	-------	--------	-----	-----	-----	----	-------	--------	-----	-----	-----	----	-------	--------	-----	-----	-----

KEY

65	VSS	185	RAM_DIMM_CLK_P0	61 62
66	VSS	186	RAM_DIMM_CLK_N0	61 62
67	VDD	187		
68	NC/PAR_IN	188	RAM_A<0>	59 61 68
69	VDD	189		
70	VDD	190	RAM_BA<1>	59 61 68
71	VDDQ	191		
72	RAS_L	192	RAM_RAS_L	59 61 68
73	WE_L	193	RAM_CS_DIMM_A	61
74	CAS_L	194		
75	VDDQ	195	RAM_ODT_DIMM_A	61
76	ODT0	196	RAM_A<13>	59 61 68
77	NC/A13	197		
78	ODT1	198		
79	VDDQ	199	RAM_DQ<99>	59 61
80	DQ32	200	RAM_DQ<97>	59 61
81	DQ33	201		
82	VSS	202	DM4	DM4
83	DQS4_L	203	NC	
84	DQS4	204		
85	VSS	205	RAM_DQ<98>	59 61
86	DQ34	206	RAM_DQ<103>	59 61
87	DQ35	207		
88	DQ44	208	RAM_DQ<107>	59 61
89	DQ45	209	RAM_DQ<108>	59 61
90	DQ41	210		
91	VSS	211	DM5	DM5
92	DM5/DQS14	212	NC	
93	DQS5_L	213		
94	DQS5	214	RAM_DQ<110>	59 61
95	DQ46	215	RAM_DQ<106>	59 61
96	DQ42	216		
97	DQ43	217	RAM_DQ<115>	59 61
98	DQ52	218	RAM_DQ<116>	59 61
99	DQ53	219		
100	VSS	220	RAM_DIMM_CLK_P2	61 62
101	CK2/RFU	221	RAM_DIMM_CLK_N2	61 62
102	SA2	222		
103	NC	223		
104	DM6/DQS15	224	DM6	DM6
105	NC/DQS15_L	225		
106	DQS6_L	226	RAM_DQ<113>	59 61
107	DQ54	227	RAM_DQ<119>	59 61
108	DQ55	228		
109	DQ51	229	RAM_DQ<125>	59 61
110	DQ60	230	RAM_DQ<126>	59 61
111	DQ57	231		
112	VSS	232	DM7	DM7
113	DM7/DQS16	233	NC	
114	DQS7_L	234		
115	DQS7	235	RAM_DQ<121>	59 61
116	DQ62	236	RAM_DQ<123>	59 61
117	DQ58	237		
118	DQ59	238		
119	VSS	239	RAM_DIMM_A_SA0	
120	SA0	240		
121	SCL			

Memory Dimm A

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

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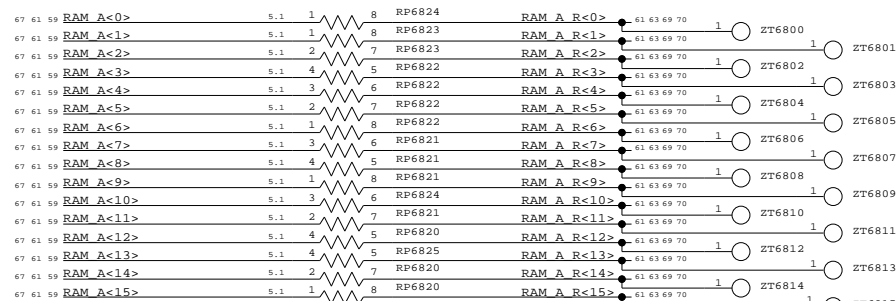
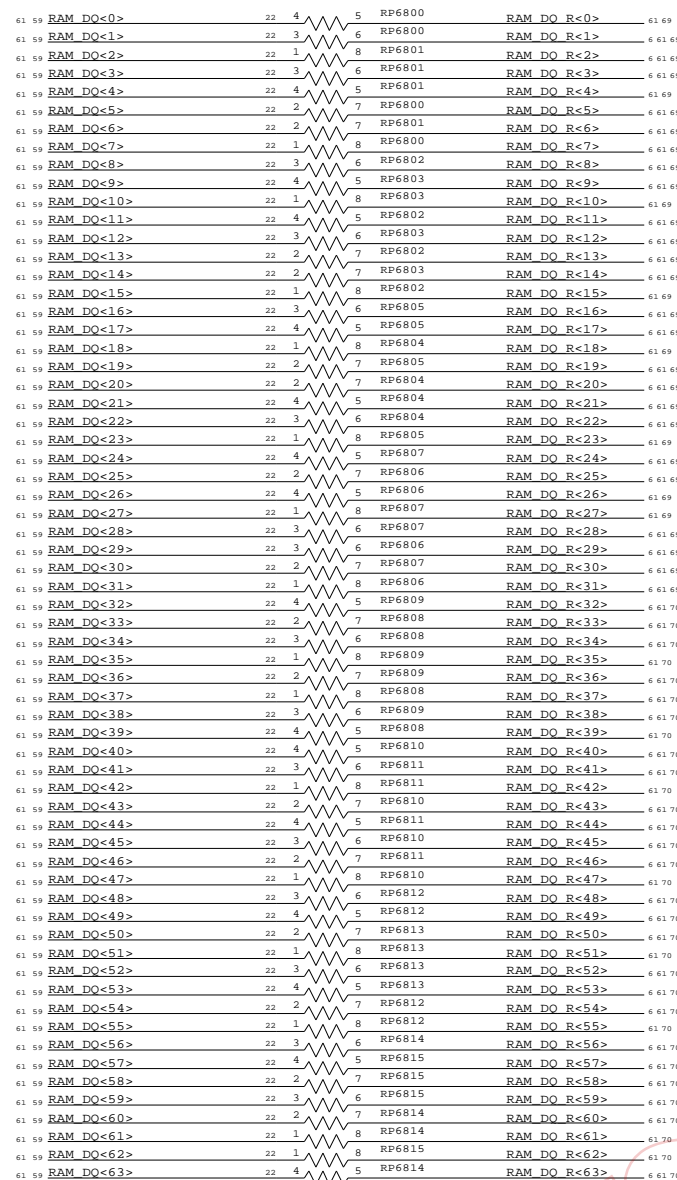
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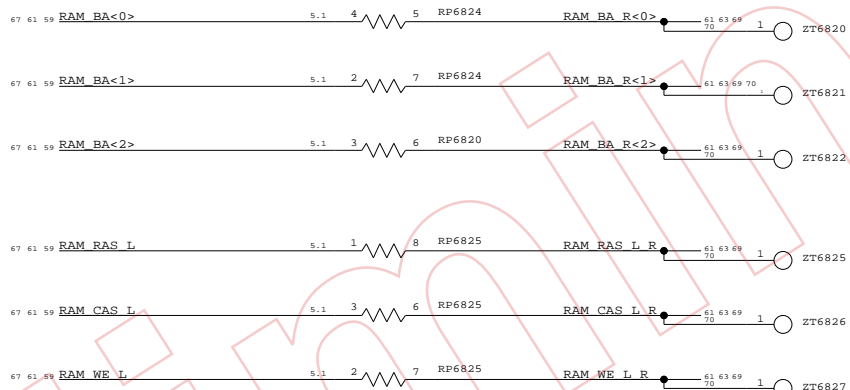
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	D	051-6790	E
SCALE	SHT	OF	
NONE	67	154	

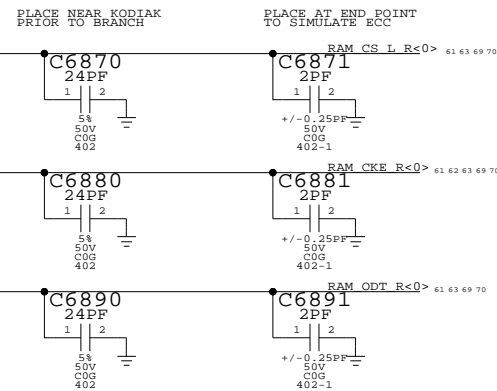
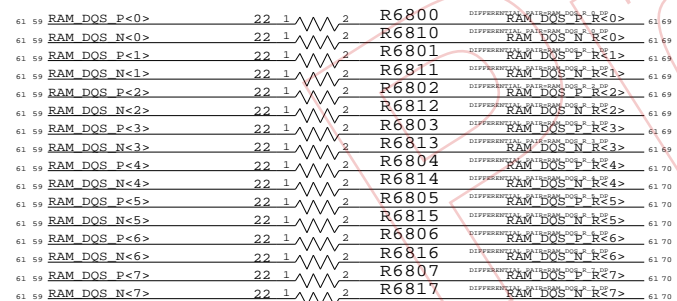
ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A



VIAS FOR ECC STUB



VIAS FOR ECC STUB



MLB Mem Series Term

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

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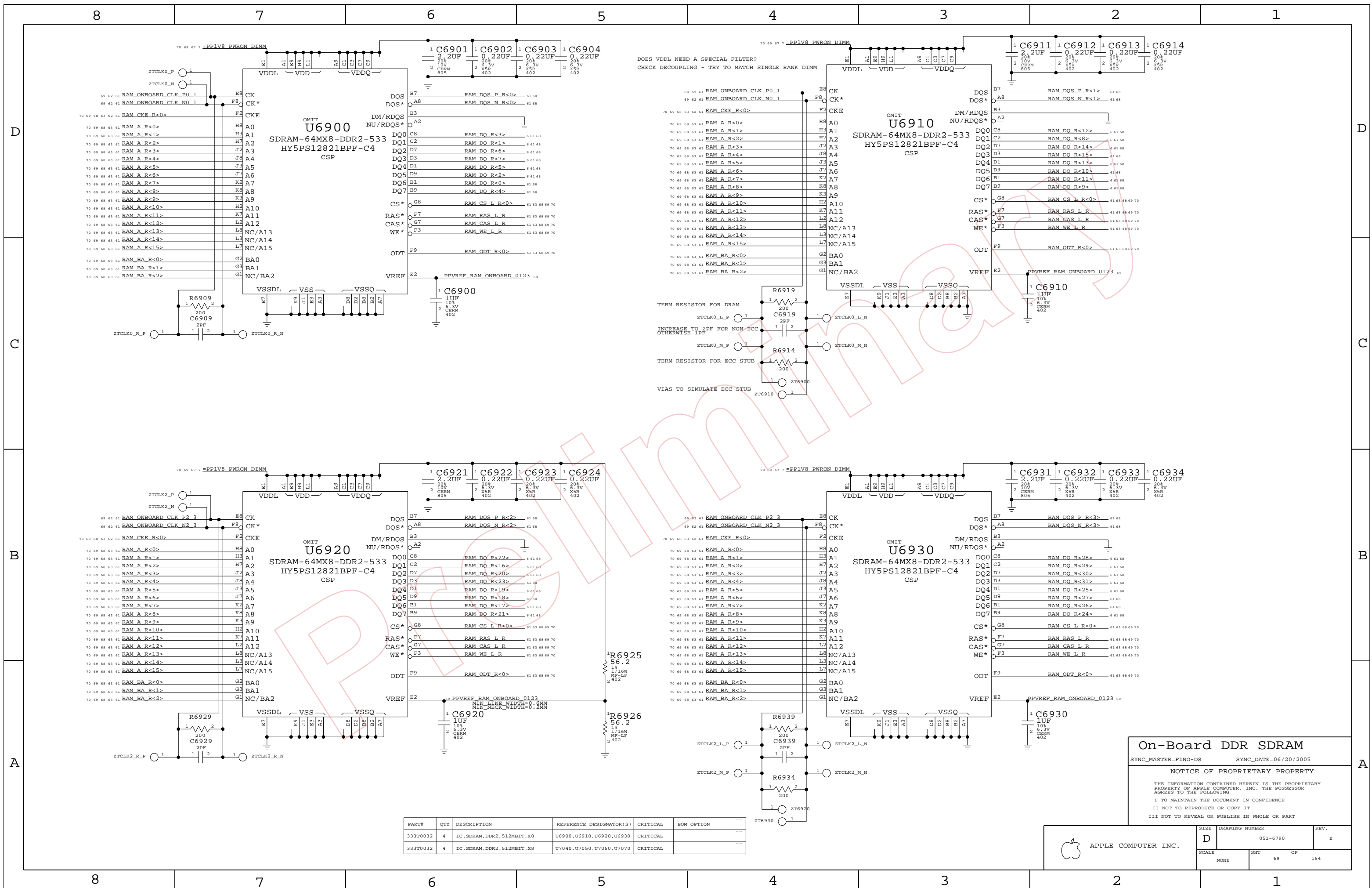


APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6790 E

SCALE NONE SHIT 68 OF 154



DOES VDDL NEED A SPECIAL FILTER?
CHECK DECOUPLING - TRY TO MATCH SINGLE RANK DIMM


On-Board DDR SDRAM

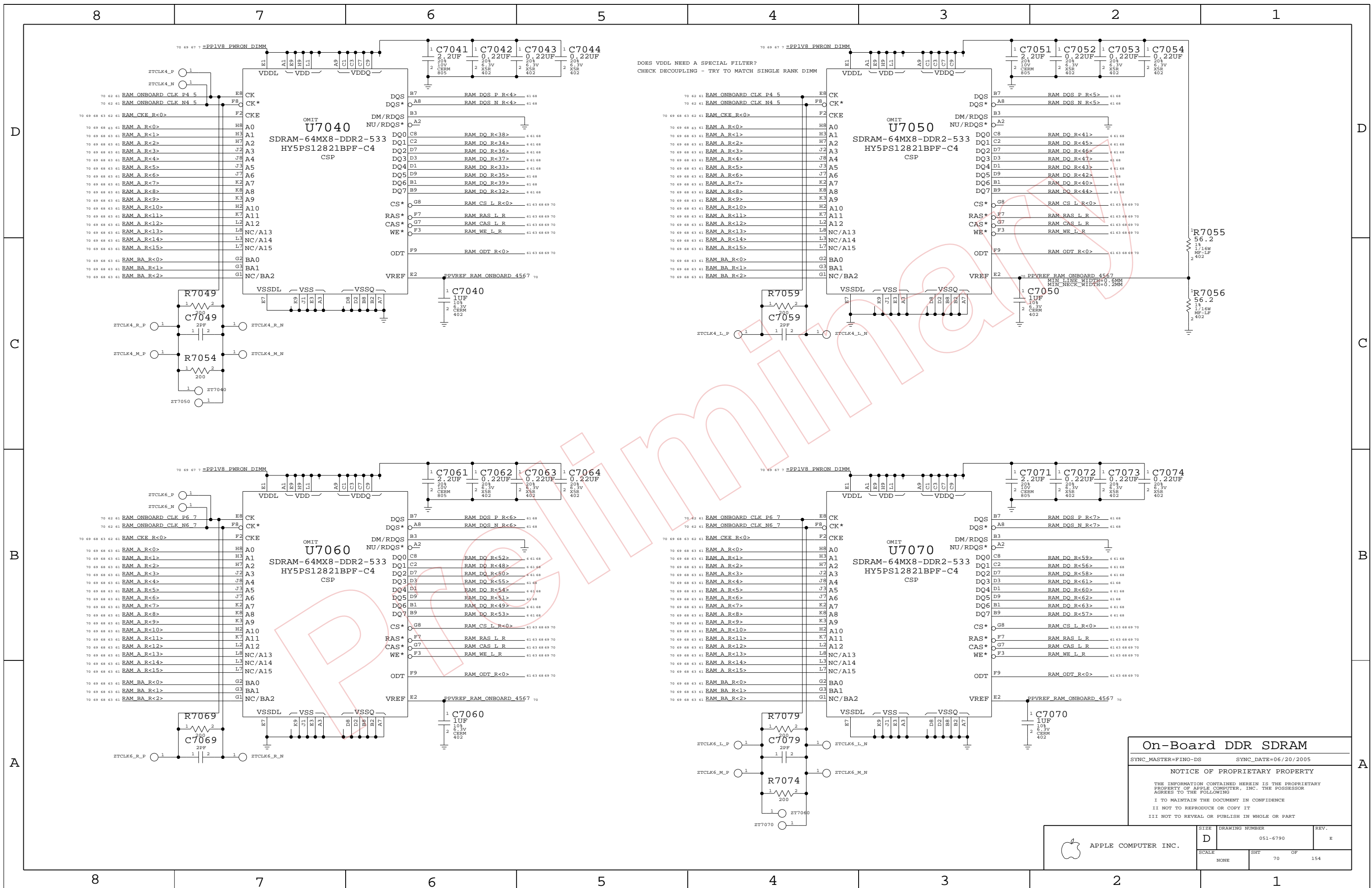
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333T0032	4	IC, SDRAM, DDR2, 512MBIT, X8	U6900, U6910, U6920, U6930	CRITICAL	
333T0032	4	IC, SDRAM, DDR2, 512MBIT, X8	U7040, U7050, U7060, U7070	CRITICAL	


APPLE COMPUTER INC.
 SCALE: NONE SHEET: 69 OF 154
 SIZE: D DRAWING NUMBER: 051-6790 REV: E



DOES VDDL NEED A SPECIAL FILTER?
CHECK DECOUPLING - TRY TO MATCH SINGLE RANK DIMM

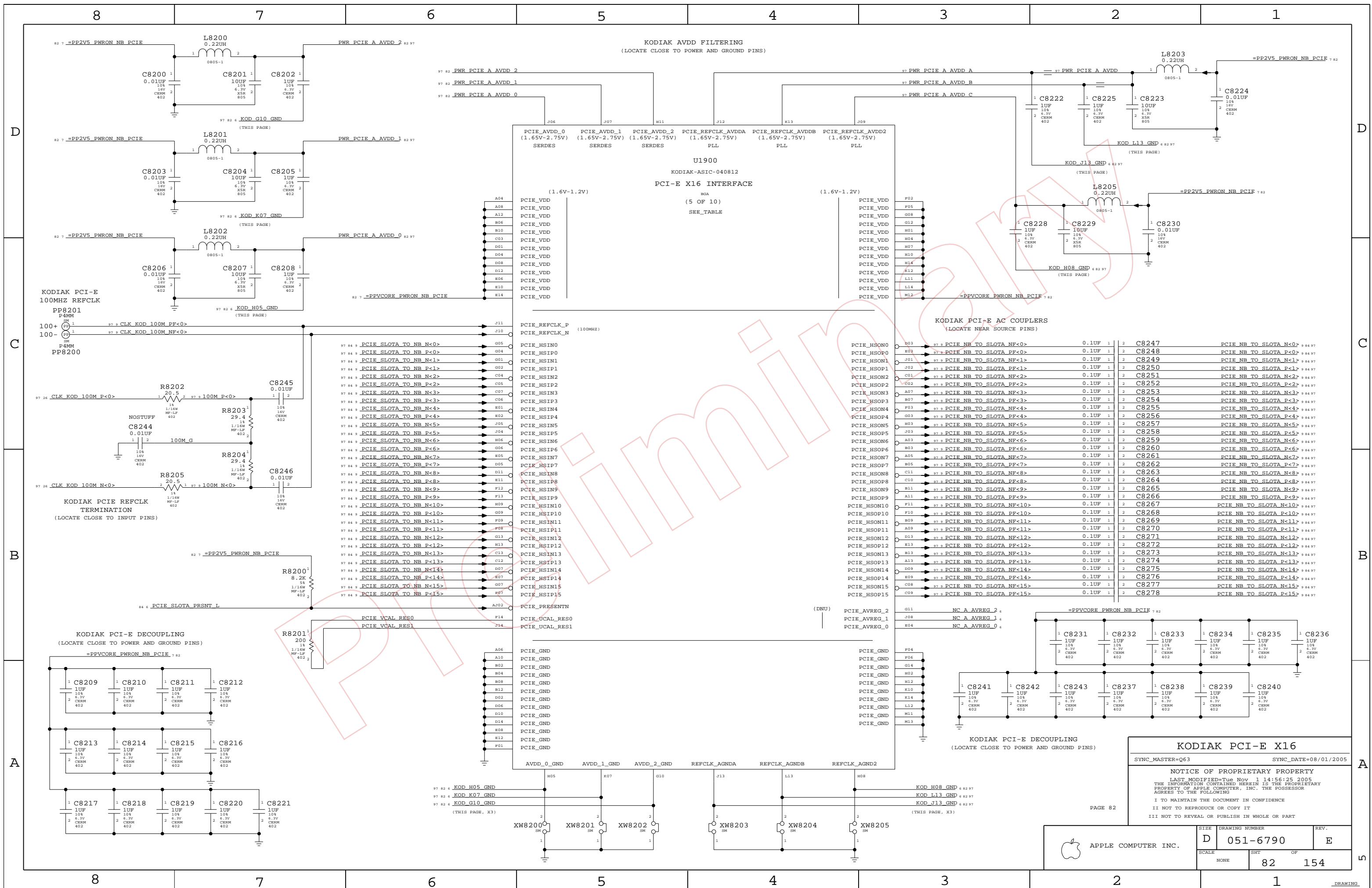
On-Board DDR SDRAM

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHEET 70	OF 154



KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)

U1900
KODIAK-ASIC-040812
PCI-E X16 INTERFACE
(5 OF 10)
SEE_TABLE

KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)

KODIAK PCI-E
100MHZ REFCLK

PP8201
P4MM

R8202
20.5

C8244
0.01UF

KODIAK PCI-E REFCLK
TERMINATION
(LOCATE CLOSE TO INPUT PINS)

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

R8201
200

KODIAK PCI-E X16

SYNC_MASTER=063 SYNC_DATE=08/01/2005

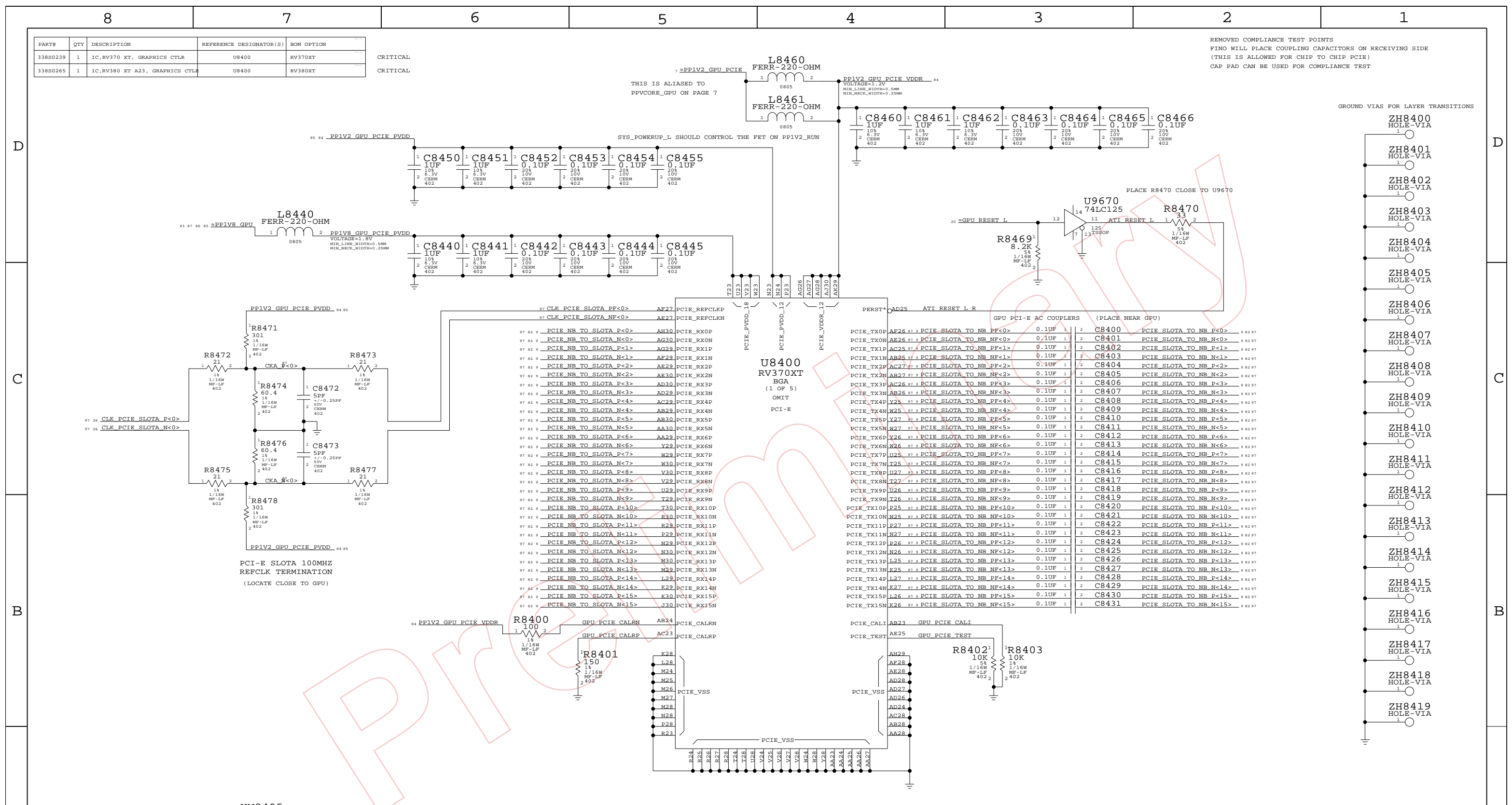
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT	OF	
NONE	82	154	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
33880239	1	IC,RV370 XT, GRAPHICS CTRL	U8400	RV370XT
33880265	1	IC,RV380 XT A23, GRAPHICS CTRL	U8400	RV380XT

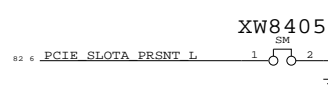
CRITICAL
CRITICAL

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST



GROUND VIAS FOR LAYER TRANSITIONS

- ZH8400 HOLE-VIA
- ZH8401 HOLE-VIA
- ZH8402 HOLE-VIA
- ZH8403 HOLE-VIA
- ZH8404 HOLE-VIA
- ZH8405 HOLE-VIA
- ZH8406 HOLE-VIA
- ZH8407 HOLE-VIA
- ZH8408 HOLE-VIA
- ZH8409 HOLE-VIA
- ZH8410 HOLE-VIA
- ZH8411 HOLE-VIA
- ZH8412 HOLE-VIA
- ZH8413 HOLE-VIA
- ZH8414 HOLE-VIA
- ZH8415 HOLE-VIA
- ZH8416 HOLE-VIA
- ZH8417 HOLE-VIA
- ZH8418 HOLE-VIA
- ZH8419 HOLE-VIA

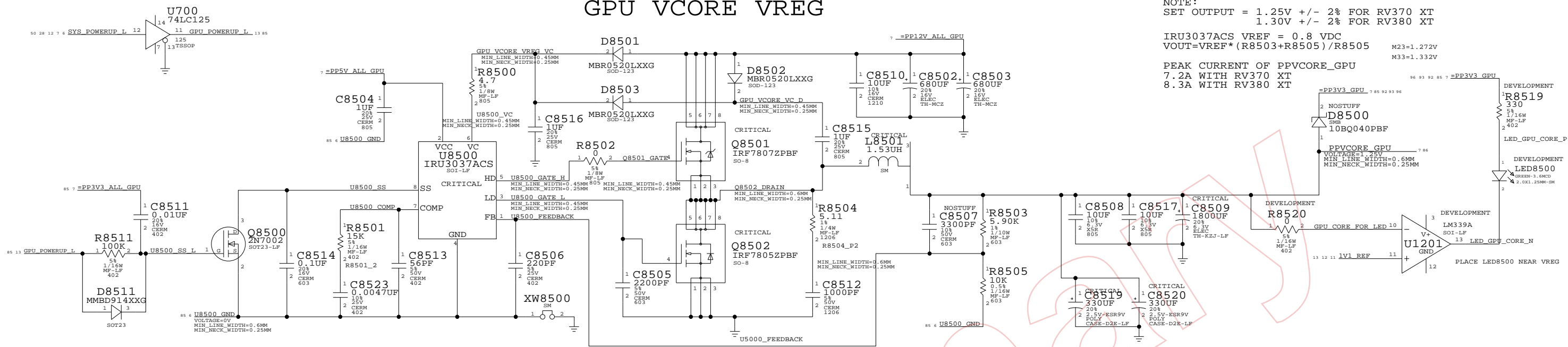


GPU PCIe		
SYNC_MASTER=M23-DD	SYNC_DATE=06/20/2005	
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SCALE	SHT	OF	
NONE	84	154	

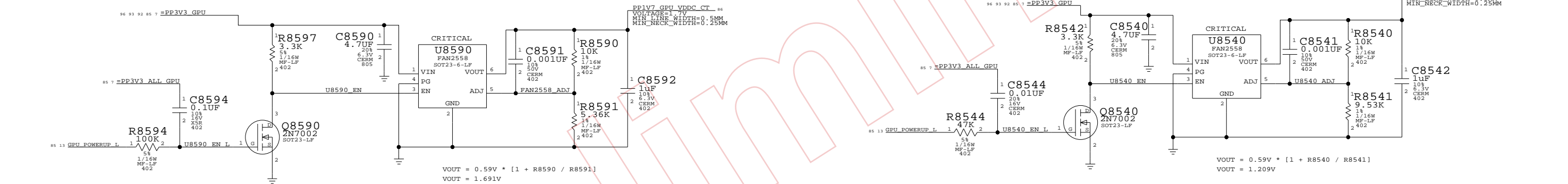
GPU VCORE VREG

NOTE:
 SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
 1.30V +/- 2% FOR RV380 XT
 IRU3037ACS VREF = 0.8 VDC
 $V_{OUT} = V_{REF} * (R8503 + R8505) / R8505$ M23=1.272V
 M33=1.332V
 PEAK CURRENT OF PPVCORE_GPU
 7.2A WITH RV370 XT
 8.3A WITH RV380 XT



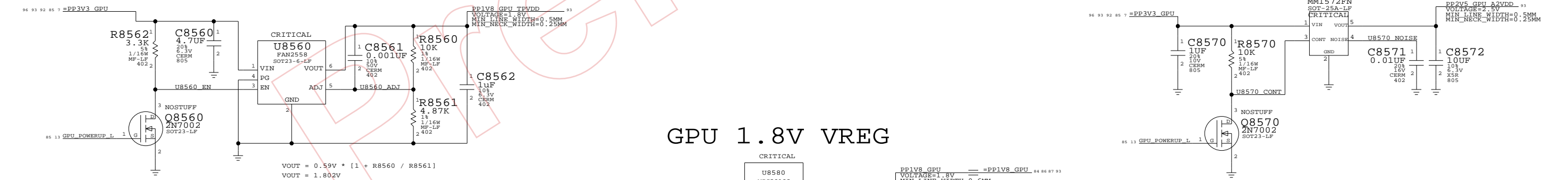
GPU 1.7V VDDC_CT

GPU 1.20V PCIE PVDD

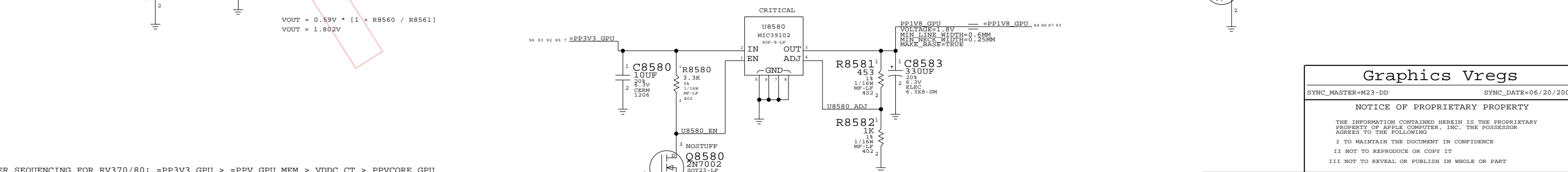


GPU 1.80V TPVDD

GPU 2.5V A2VDD



GPU 1.8V VREG



Graphics Vregs

SYNC_MASTER=M23-DD SYNC_DATE=06/20/2005

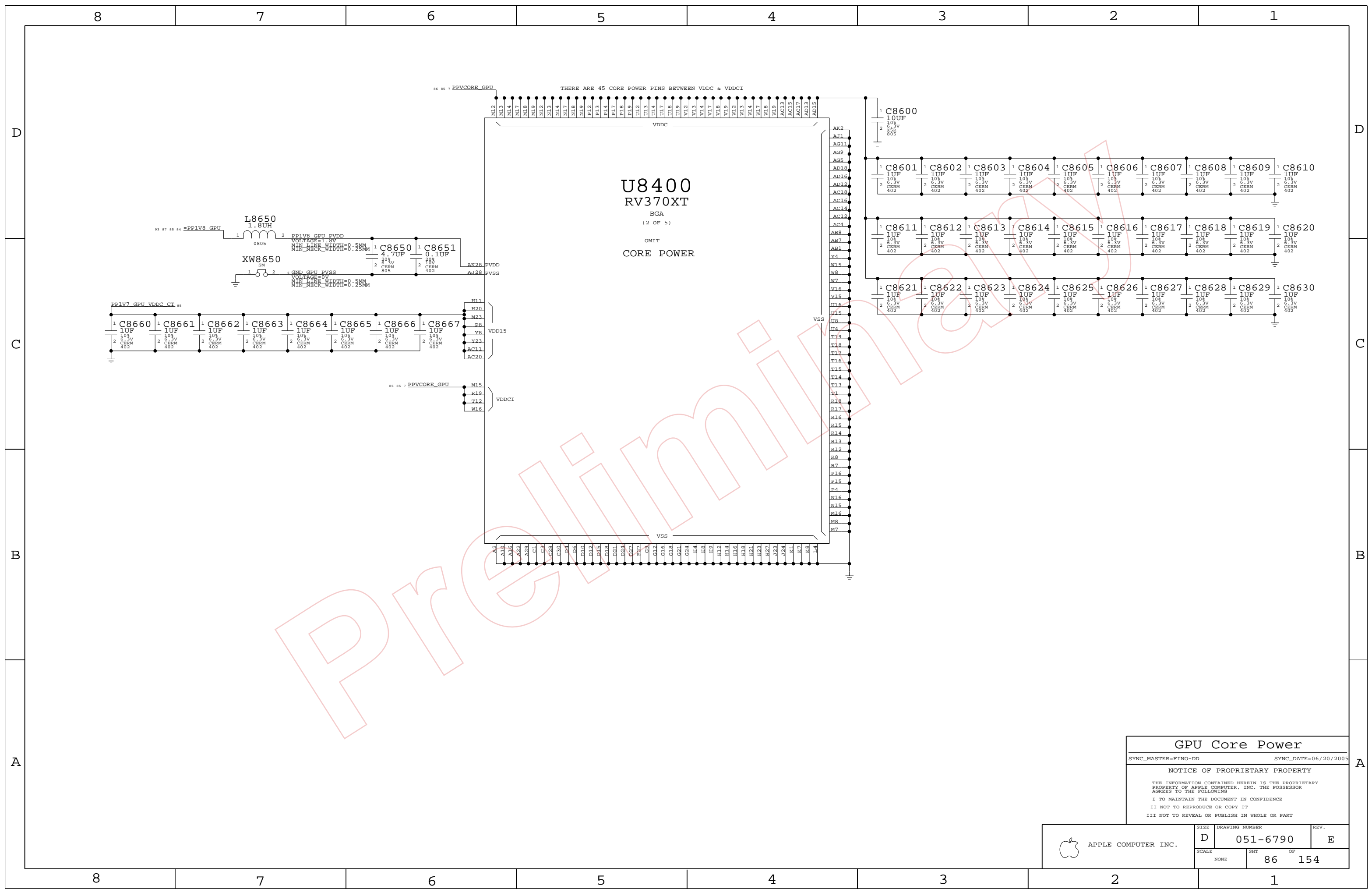
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POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
 PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
 HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
 POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

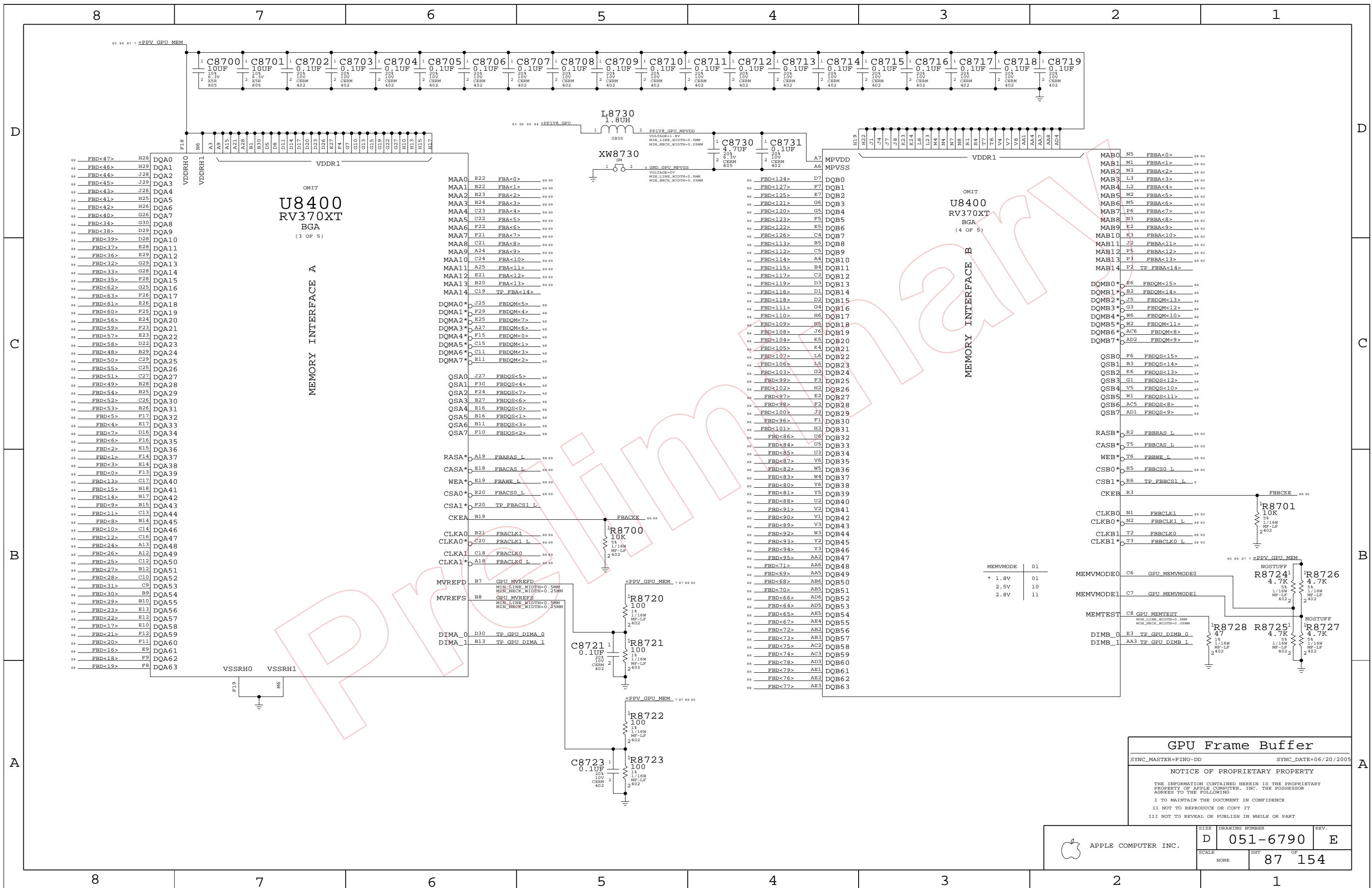
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	NONE	SHT	OF
		85	154



U8400
RV370XT
BGA
(2 OF 5)
OMIT
CORE POWER

GPU Core Power
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NONE	86 OF 154		



GPU Frame Buffer

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APPLE COMPUTER INC.	SCALE	SHT	REV.
	NONE	87 OF 154	E

FRAME BUFFER A TERMINATION

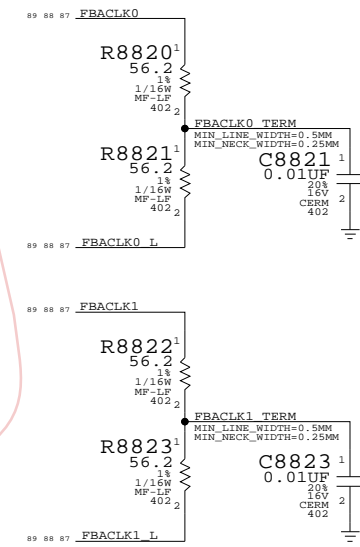
PLACE R'S CLOSE TO MEMORY

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

Table listing termination points for Frame Buffer A, including signals like FBD<31>, FBD<30>, FBD<29>, FBD<28>, FBD<27>, FBD<26>, FBD<25>, FBD<24>, FBD<0>, FBD<1>, FBD<2>, FBD<3>, FBD<17>, FBD<16>, FBD<18>, FBD<19>, FBD<15>, FBD<14>, FBD<13>, FBD<12>, FBD<10>, FBD<11>, FBD<9>, FBD<8>, FBD<5>, FBD<6>, FBD<4>, FBD<7>, FBD<20>, FBD<21>, FBD<22>, FBD<23>.

Table listing termination points for Frame Buffer A, including signals like FBD<32>, FBD<33>, FBD<34>, FBD<35>, FBD<36>, FBD<37>, FBD<38>, FBD<39>, FBD<40>, FBD<41>, FBD<42>, FBD<43>, FBD<44>, FBD<45>, FBD<46>, FBD<47>, FBD<48>, FBD<49>, FBD<50>, FBD<51>, FBD<52>, FBD<53>, FBD<54>, FBD<55>, FBD<56>, FBD<57>, FBD<58>, FBD<59>, FBD<60>, FBD<61>, FBD<62>, FBD<63>.

Table listing termination points for Frame Buffer A, including signals like FBDQS<0>, FBDQS<1>, FBDQS<2>, FBDQS<3>, FBDQS<4>, FBDQS<5>, FBDQS<6>, FBDQS<7>, FBDQM<0>, FBDQM<1>, FBDQM<2>, FBDQM<3>, FBDQM<4>, FBDQM<5>, FBDQM<6>, FBDQM<7>.



FRAME BUFFER B TERMINATION

Table listing termination points for Frame Buffer B, including signals like FBD<64>, FBD<65>, FBD<66>, FBD<67>, FBD<84>, FBD<85>, FBD<86>, FBD<87>, FBD<72>, FBD<73>, FBD<75>, FBD<74>, FBD<68>, FBD<70>, FBD<69>, FBD<71>, FBD<80>, FBD<81>, FBD<82>, FBD<83>, FBD<76>, FBD<77>, FBD<78>, FBD<79>, FBD<91>, FBD<90>, FBD<89>, FBD<88>, FBD<95>, FBD<94>, FBD<93>, FBD<92>.

Table listing termination points for Frame Buffer B, including signals like FBD<96>, FBD<97>, FBD<98>, FBD<99>, FBD<100>, FBD<101>, FBD<102>, FBD<103>, FBD<104>, FBD<105>, FBD<106>, FBD<107>, FBD<108>, FBD<109>, FBD<110>, FBD<111>, FBD<112>, FBD<113>, FBD<114>, FBD<115>, FBD<116>, FBD<117>, FBD<118>, FBD<119>, FBD<120>, FBD<121>, FBD<122>, FBD<123>, FBD<124>, FBD<125>, FBD<126>, FBD<127>.

Table listing termination points for Frame Buffer B, including signals like FBDQS<8>, FBDQS<9>, FBDQS<10>, FBDQS<11>, FBDQS<12>, FBDQS<13>, FBDQS<14>, FBDQS<15>, FBDQM<8>, FBDQM<9>, FBDQM<10>, FBDQM<11>, FBDQM<12>, FBDQM<13>, FBDQM<14>, FBDQM<15>.

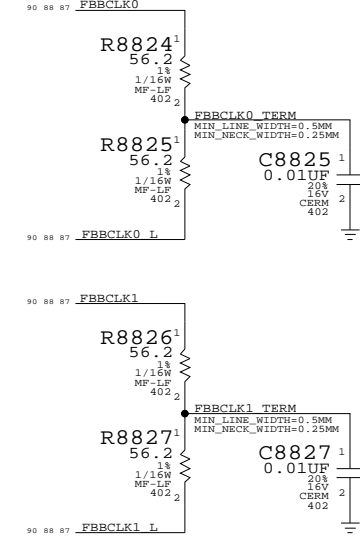
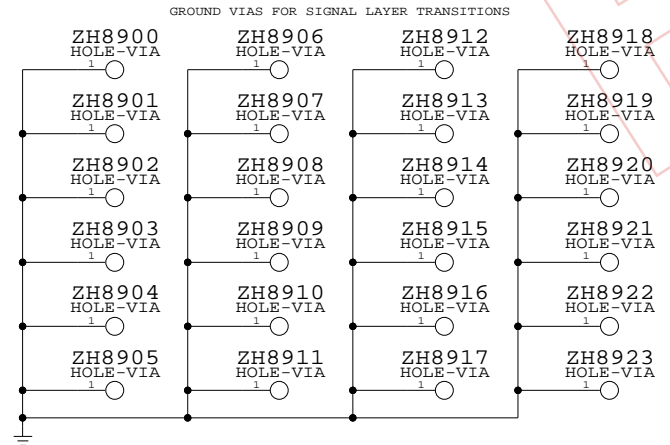
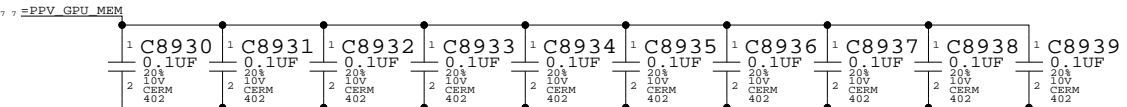
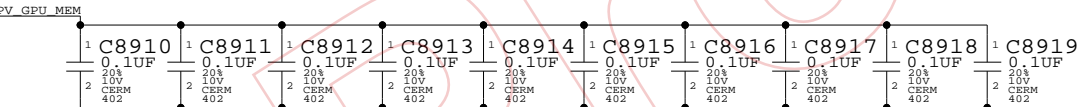
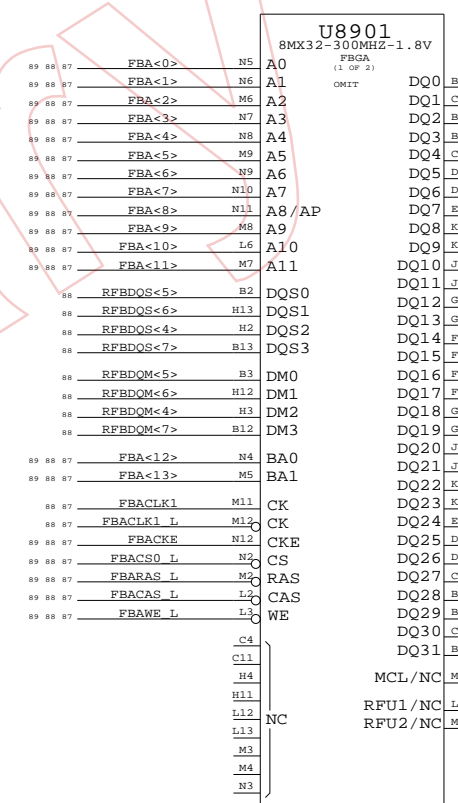
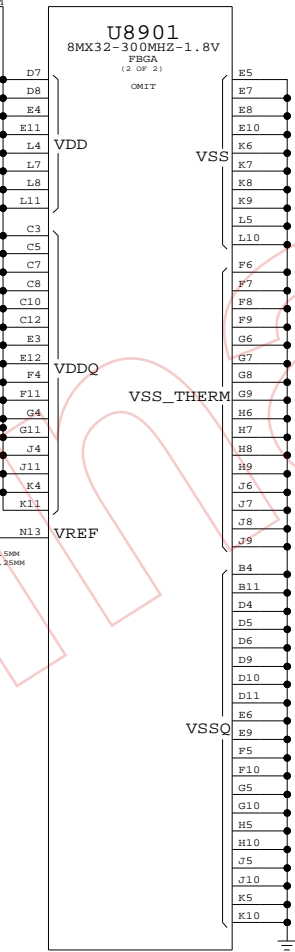
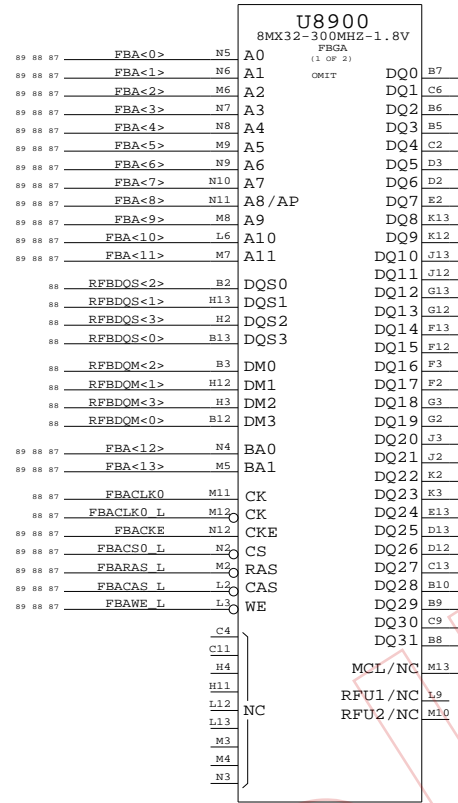
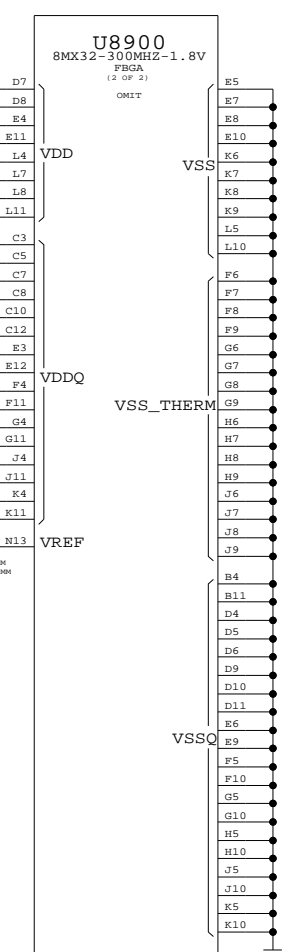
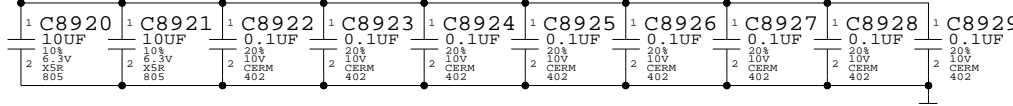
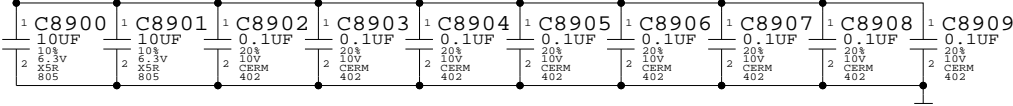
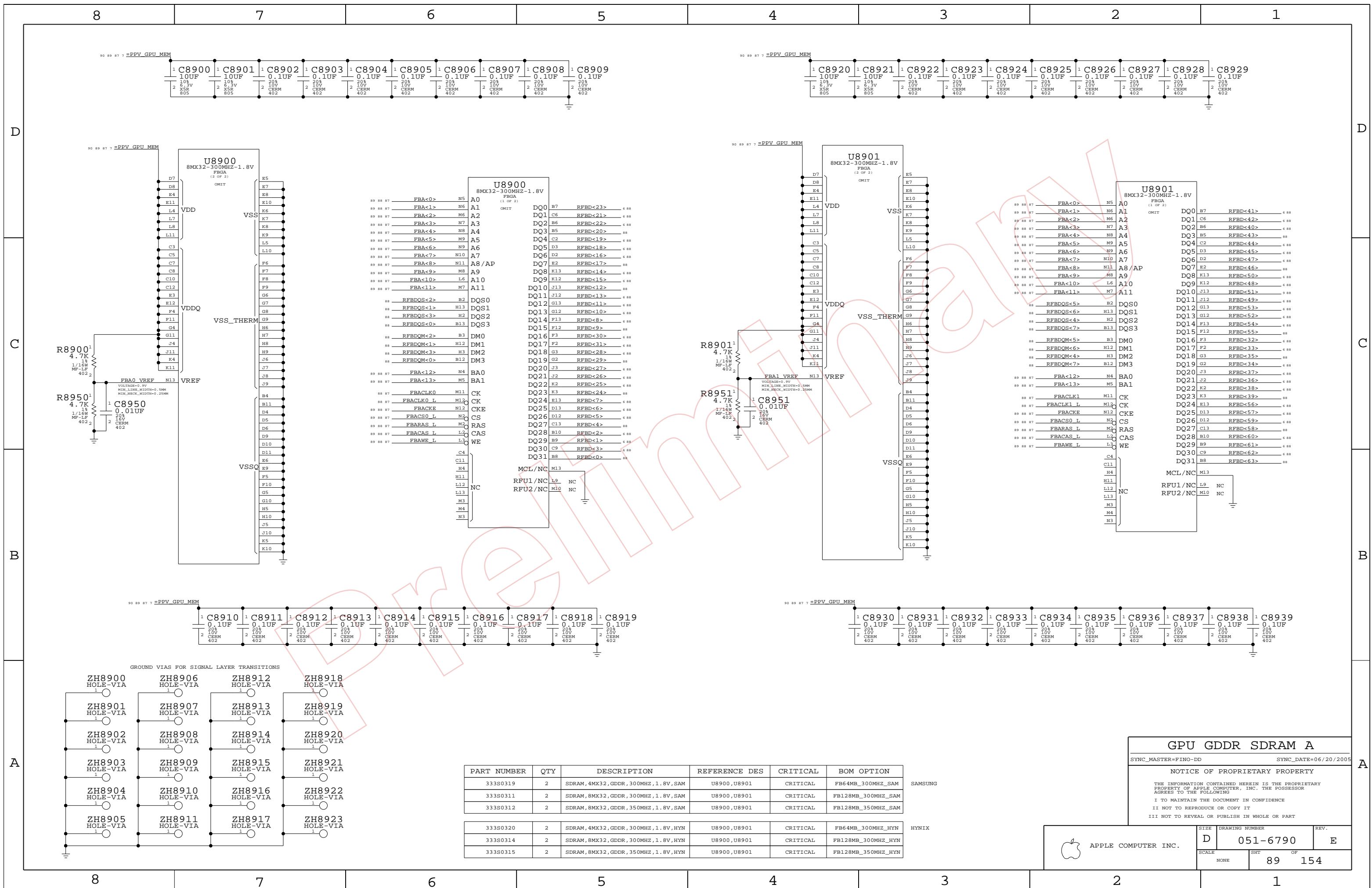


Table mapping electrical constraint sets to net physical types, net spacing types, and differential pairs for Frame Buffer A termination.

Table mapping electrical constraint sets to net physical types, net spacing types, and differential pairs for Frame Buffer B termination.

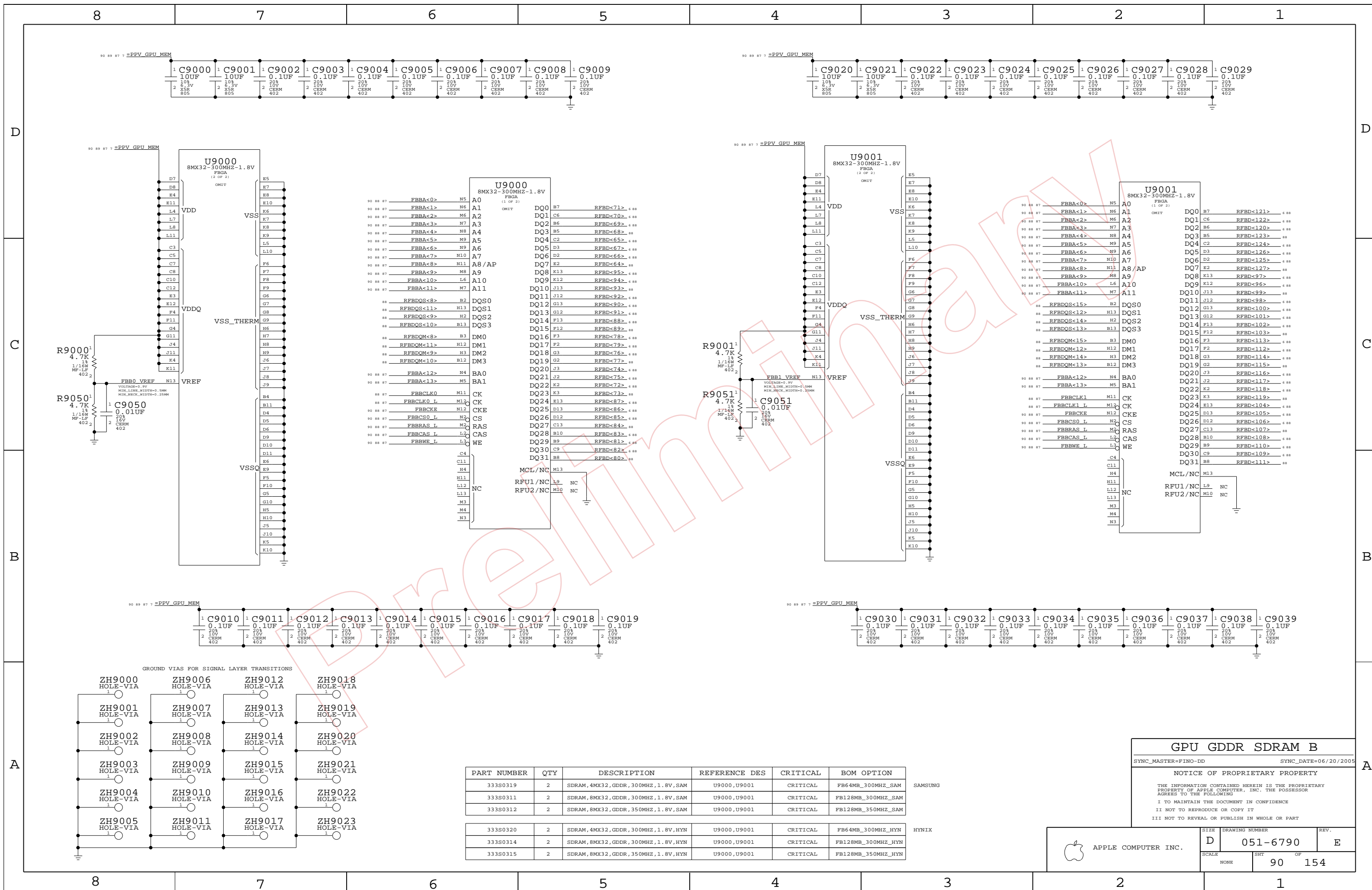
FB Series Termination
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0319	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB64MB_300MHZ_SAM
333S0311	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_300MHZ_SAM
333S0312	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_350MHZ_SAM
333S0320	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB64MB_300MHZ_HYN
333S0314	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_300MHZ_HYN
333S0315	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_350MHZ_HYN

GPU GDDR SDRAM A
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GPU GDDR SDRAM B
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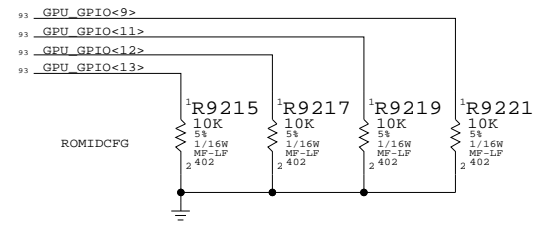
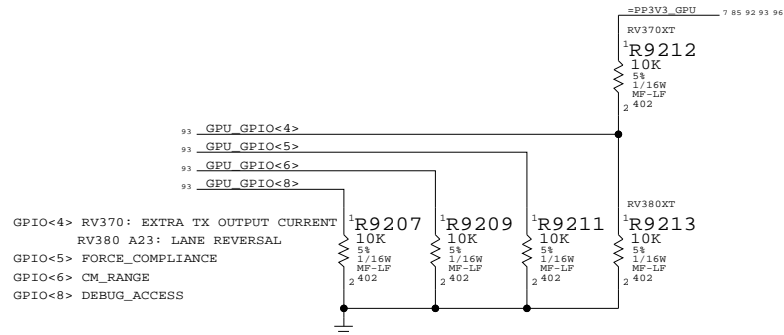
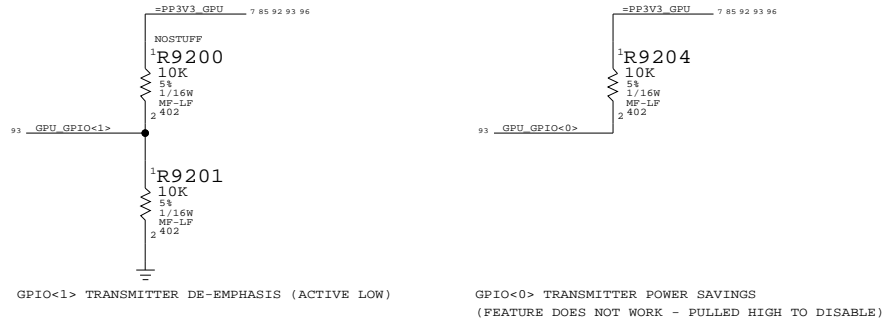
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0319	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB64MB_300MHZ_SAM
333S0311	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB128MB_300MHZ_SAM
333S0312	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB128MB_350MHZ_SAM
333S0320	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB64MB_300MHZ_HYN
333S0314	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB128MB_300MHZ_HYN
333S0315	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB128MB_350MHZ_HYN

APPLE COMPUTER INC.

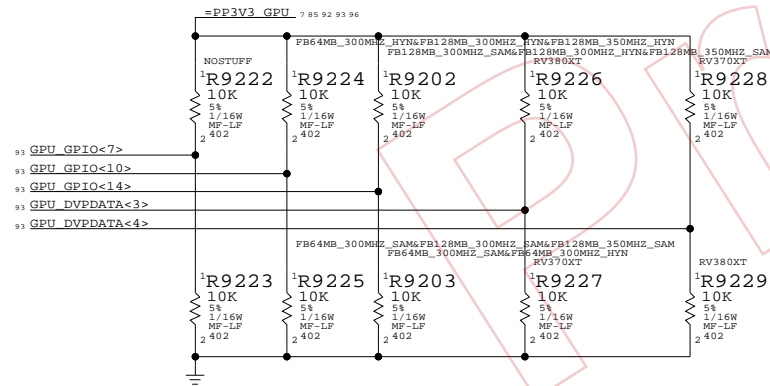
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SCALE	NONE	SHT	90	OF	154

ATI STRAPS

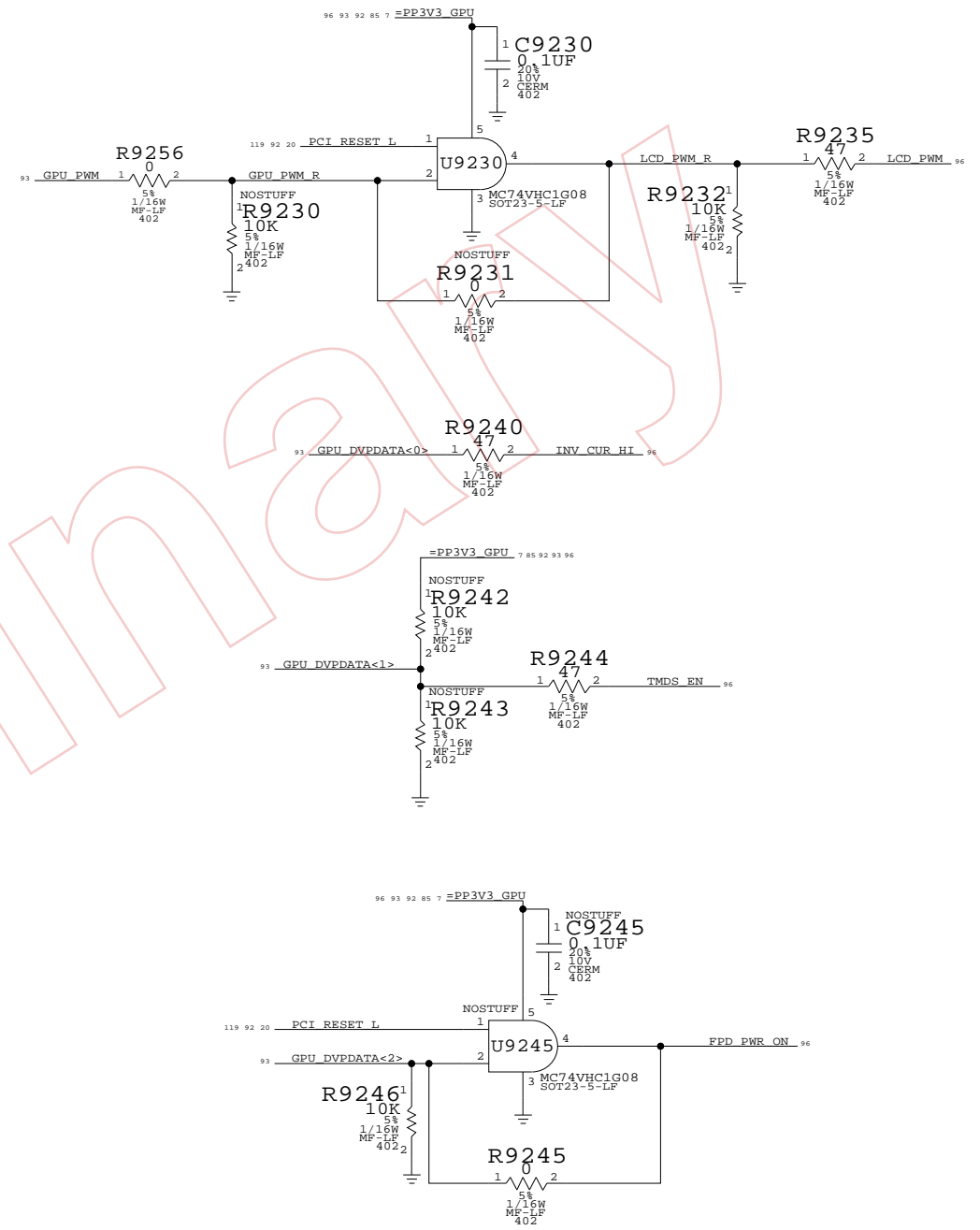
APPLE GPIOS



MEMORY STRAPS



GPIO<7> - MEMORY DIE REVISION
 0 - ORIGINAL DIE REVISION
 1 - NEW (FUTURE) DIE REV
 GPIO<10> - MEMORY VENDOR
 0 - SAMSUNG
 1 - HYNIX
 GPIO<14> - MEMORY DENSITY
 0 - 4MX32
 1 - 8MX32
 DVPDATA<3,4> - SPEED
 00 - 325E / 200M
 01 - 400E / 300M
 10 - 500E / 350M
 11 - RESERVED FOR FUTURE USE



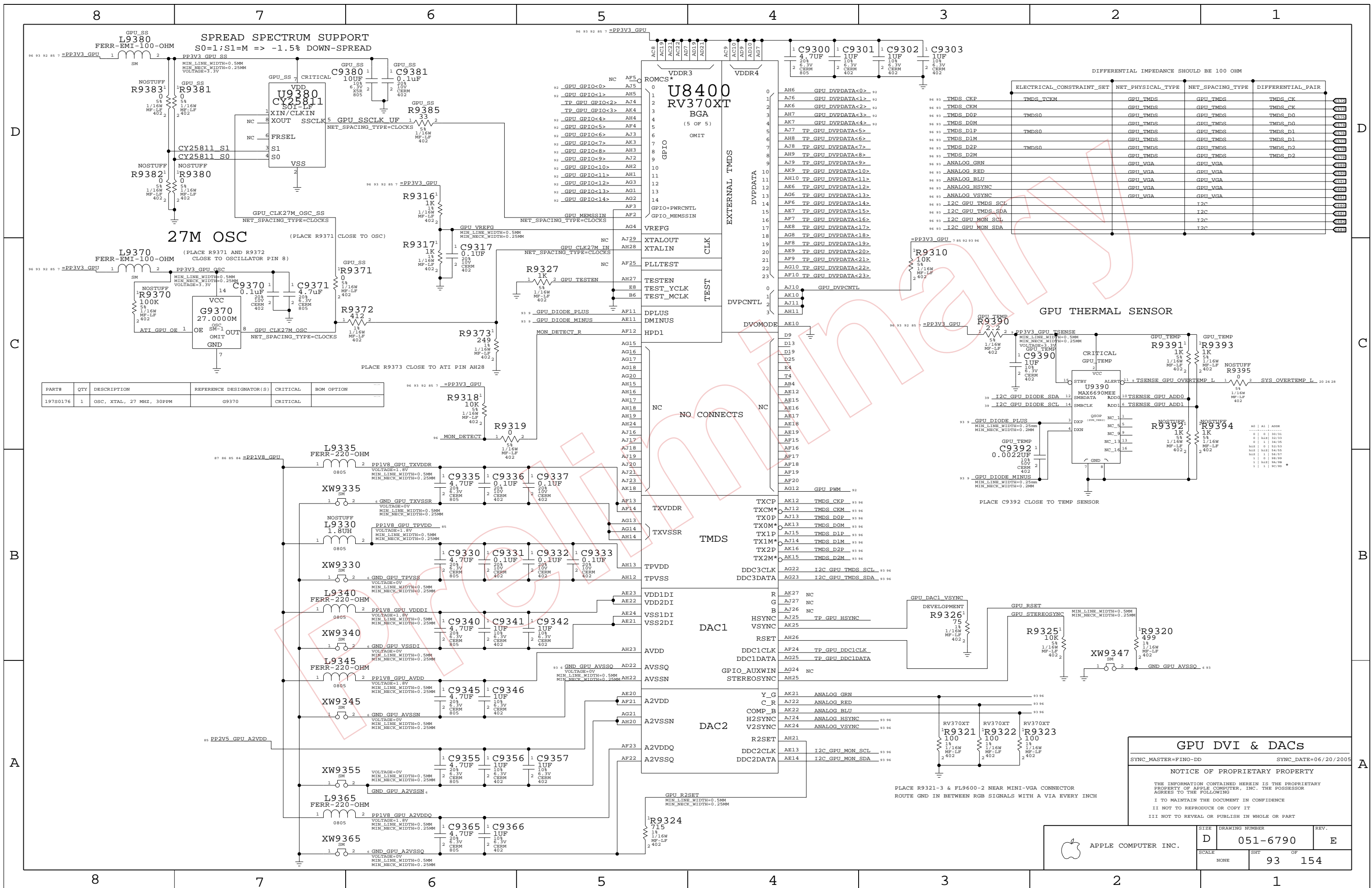
GPU Straps

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	D	051-6790	E
SCALE	NONE	SHT	OF
		92	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0176	1	OSC, XTAL, 27 MHz, 30PPM	G9370	CRITICAL	

GPU DVI & DACs

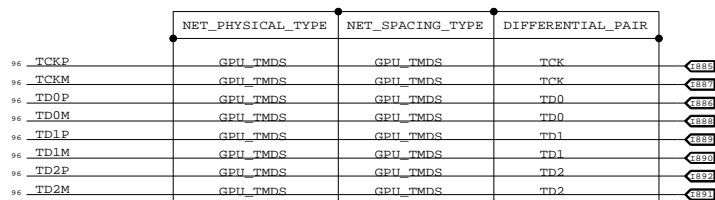
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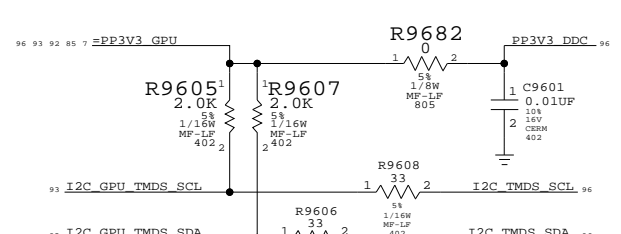
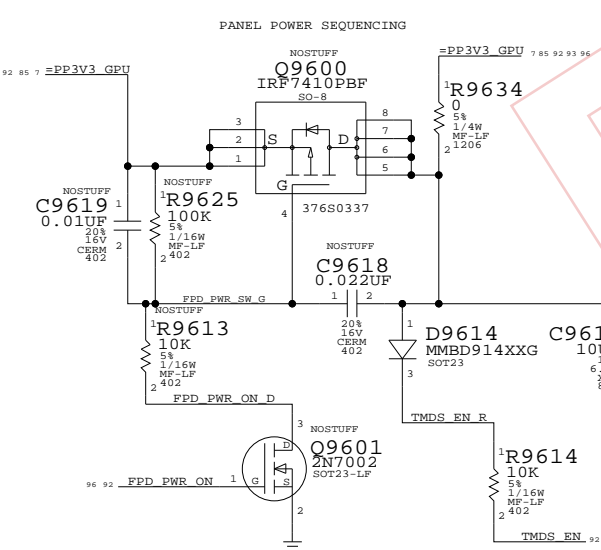
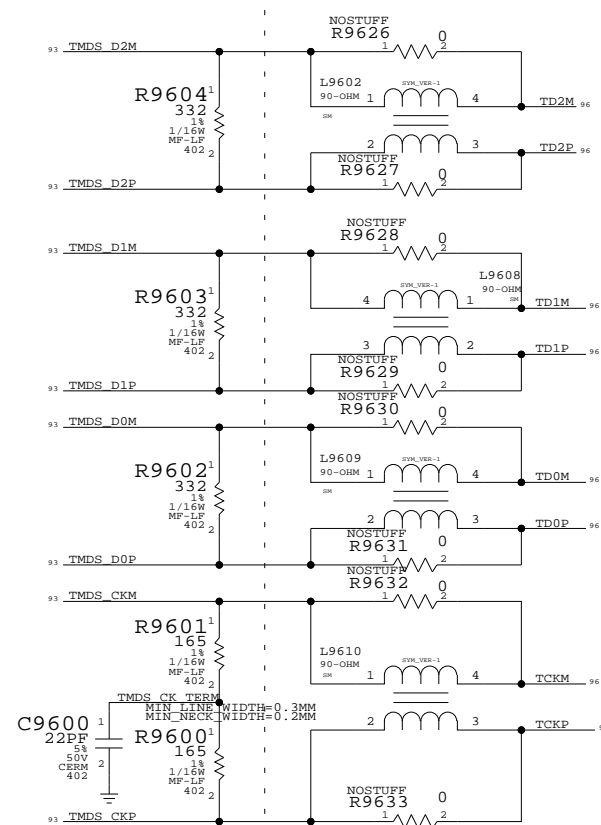
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHEET	OF	
NONE	93	154	

INTERNAL LCD

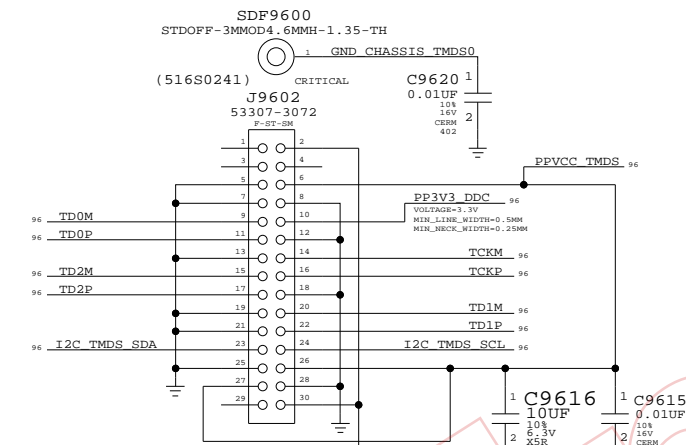


PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

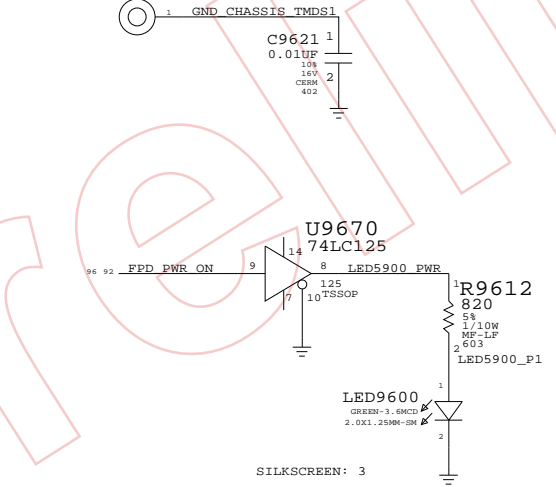
PLACE FILTER CLOSE TO TMD5 CONNECTOR



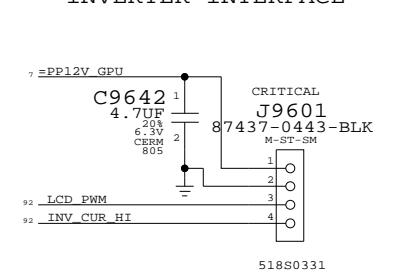
INTERNAL TMD5 CONNECTOR



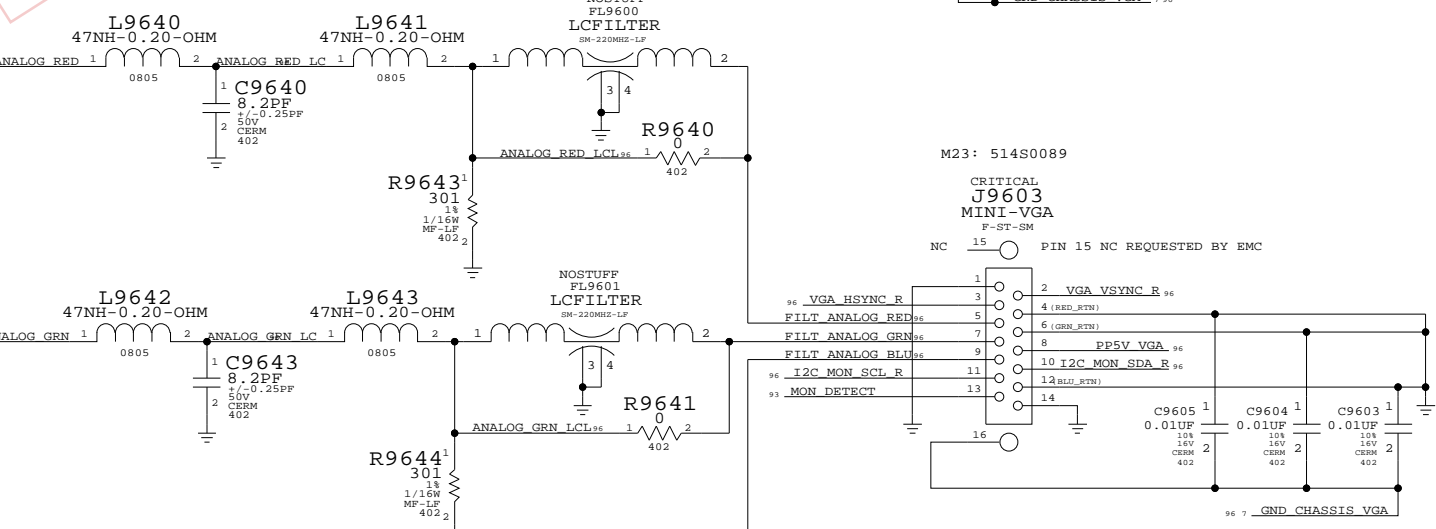
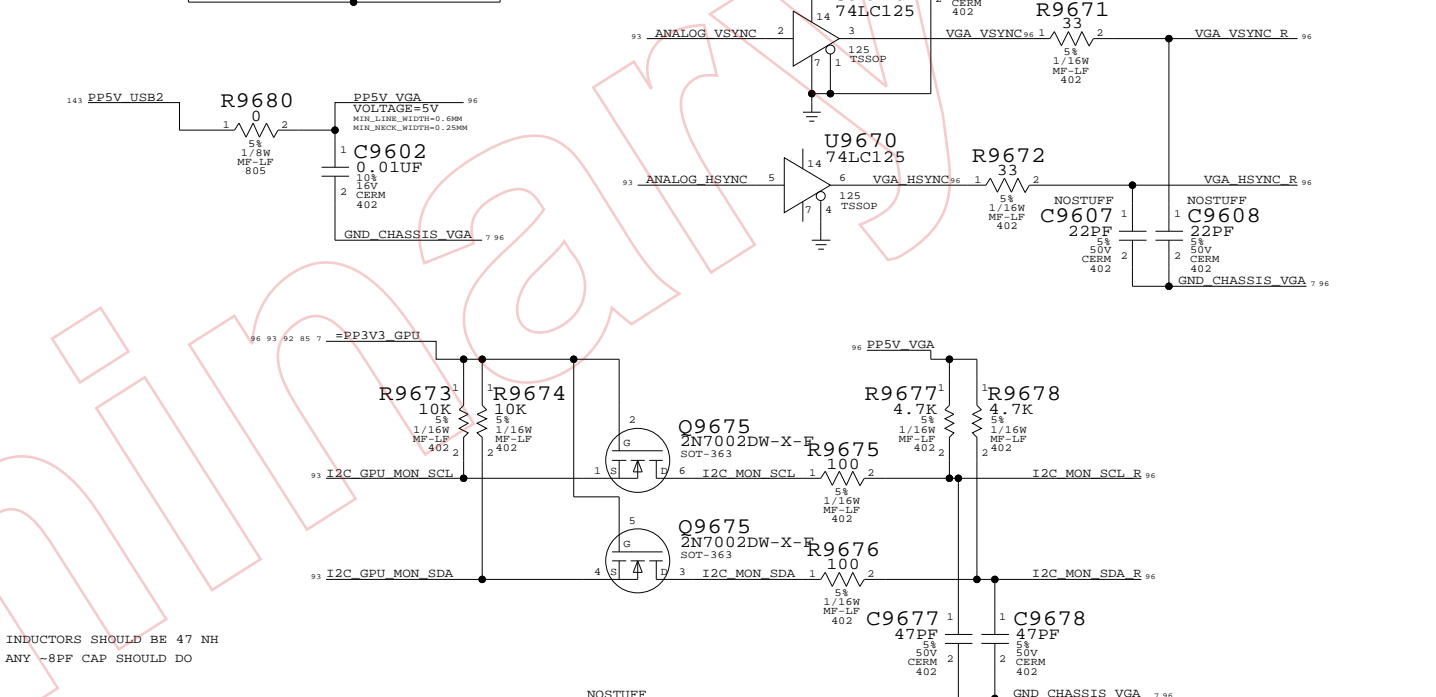
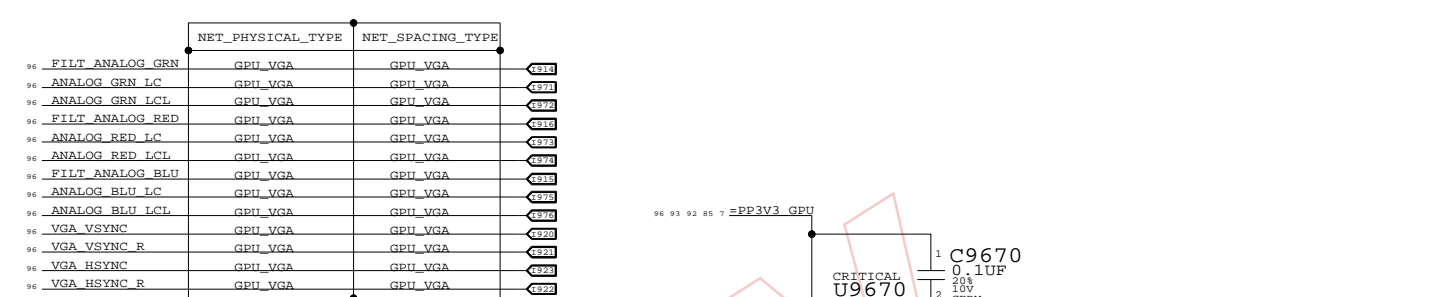
INDUCTORS SHOULD BE 47 NH ANY -8PF CAP SHOULD DO



INVERTER INTERFACE



EXTERNAL VGA CONNECTOR



TMD5/Inverter/ExtVGA

SYNC_MASTER=M23-DD SYNC_DATE=06/20/2005

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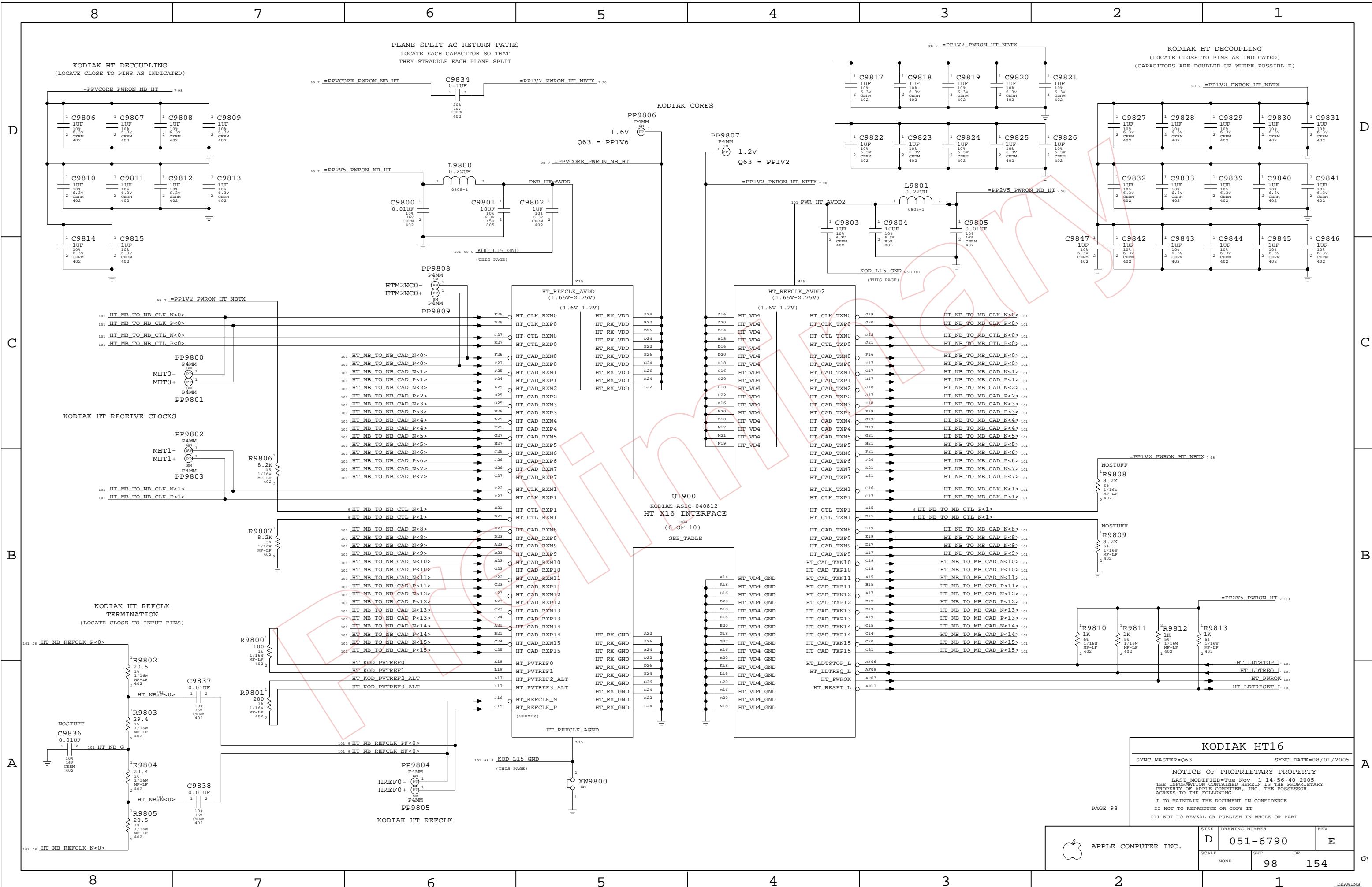
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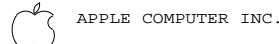
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHEET		OF
NONE	96		154



KODIAK HT16
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SCALE	SHT	OF
NONE	98	154



8

7

6

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2

1

D

D

C

C

B

B

A

A

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
HT NB TO MB CLK N<0>	HT NB TO SB CLK N<0>	TRUE	HT NB TO SB CLK	HT NB TO SB PP	HT CAD
HT NB TO MB CAD N<0>	HT NB TO SB CAD N<0>	TRUE	HT NB TO SB CAD0	HT NB TO SB PP	HT CAD
HT NB TO MB CAD N<1>	HT NB TO SB CAD N<1>	TRUE	HT NB TO SB CAD1	HT NB TO SB	HT CAD
HT NB TO MB CAD N<2>	HT NB TO SB CAD N<2>	TRUE	HT NB TO SB CAD2	HT NB TO SB	HT CAD
HT NB TO MB CAD N<3>	HT NB TO SB CAD N<3>	TRUE	HT NB TO SB CAD3	HT NB TO SB	HT CAD
HT NB TO MB CAD N<4>	HT NB TO SB CAD N<4>	TRUE	HT NB TO SB CAD4	HT NB TO SB	HT CAD
HT NB TO MB CAD N<5>	HT NB TO SB CAD N<5>	TRUE	HT NB TO SB CAD5	HT NB TO SB	HT CAD
HT NB TO MB CAD N<6>	HT NB TO SB CAD N<6>	TRUE	HT NB TO SB CAD6	HT NB TO SB	HT CAD
HT NB TO MB CAD N<7>	HT NB TO SB CAD N<7>	TRUE	HT NB TO SB CAD7	HT NB TO SB	HT CAD
HT NB TO MB CTL N<0>	HT NB TO SB CTL N<0>	TRUE	HT NB TO SB CTL0	HT NB TO SB	HT CAD
HT MB TO NB CLK N<0>	HT SB TO NB CLK N<0>	TRUE	HT SB TO NB CLK	HT SB TO NB PP	HT CAD
HT MB TO NB CAD N<0>	HT SB TO NB CAD N<0>	TRUE	HT SB TO NB CAD0	HT SB TO NB PP	HT CAD
HT MB TO NB CAD N<1>	HT SB TO NB CAD N<1>	TRUE	HT SB TO NB CAD1	HT SB TO NB	HT CAD
HT MB TO NB CAD N<2>	HT SB TO NB CAD N<2>	TRUE	HT SB TO NB CAD2	HT SB TO NB	HT CAD
HT MB TO NB CAD N<3>	HT SB TO NB CAD N<3>	TRUE	HT SB TO NB CAD3	HT SB TO NB	HT CAD
HT MB TO NB CAD N<4>	HT SB TO NB CAD N<4>	TRUE	HT SB TO NB CAD4	HT SB TO NB	HT CAD
HT MB TO NB CAD N<5>	HT SB TO NB CAD N<5>	TRUE	HT SB TO NB CAD5	HT SB TO NB	HT CAD
HT MB TO NB CAD N<6>	HT SB TO NB CAD N<6>	TRUE	HT SB TO NB CAD6	HT SB TO NB	HT CAD
HT MB TO NB CAD N<7>	HT SB TO NB CAD N<7>	TRUE	HT SB TO NB CAD7	HT SB TO NB	HT CAD
HT MB TO NB CTL N<0>	HT SB TO NB CTL N<0>	TRUE	HT SB TO NB CTL0	HT SB TO NB	HT CAD
NC HT MB TO NB CAD P<8..15>		TRUE			
NC HT MB TO NB CAD N<8..15>		TRUE			
TP HT MB TO NB CLK N<1>		TRUE			
TP HT MB TO NB CLK P<1>		TRUE			
NC HT NB TO MB CAD P<8..15>		TRUE			
NC HT NB TO MB CAD N<8..15>		TRUE			
NC HT NB TO MB CLK N<1>		TRUE			
NC HT NB TO MB CLK P<1>		TRUE			
HT NB REFCLK P<0>			HT NB REFCLK0	HT NB REFCLK	HT CLK
HT NB REFCLK N<0>			HT NB REFCLK0	HT CLK	HT CLK
HT NB P<0>			HT NBO	HT CLK	HT CLK
HT NB N<0>			HT NBO	HT CLK	HT CLK
HT NB REFCLK PF<0>			HT NB REFCLK F0	HT CLK	HT CLK
HT NB REFCLK NF<0>			HT NB REFCLK F0	HT CLK	HT CLK

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
PWR_HT_AVDD	0.4MM	0.2MM	2.5
PWR_HT_AVDD2	0.4MM	0.2MM	2.5
KOD_L15_GND	0.4MM	0.2MM	0
HT_NB_G	KEEP DIFF CLOCK FROM BEING A SINGLE XNET		0

HT ALIASES

FINO-ME 06/20/2005

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SCALE	SHT	101	154
NONE			

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
HT	0.38mm SPACING	
HT	0.38mm SPACING	
HT	2.54mm SPACING	

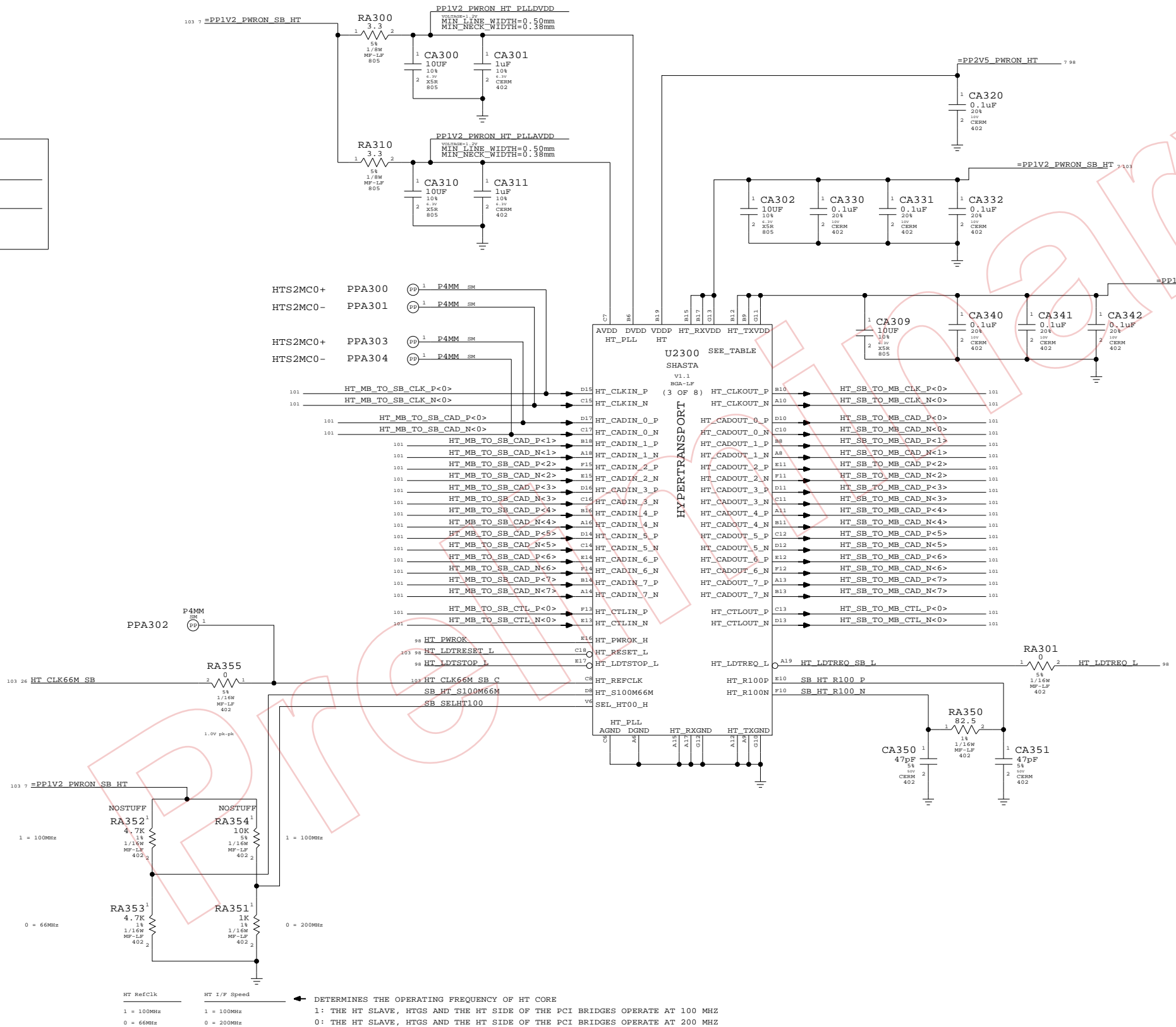
HT CLK66M_SB_C	103
HT CLK66M_SB	26 103
HT LDTRESET_L	98 103

Page Notes

Power aliases required by this page:
 =PP2V5_PWRON_HT
 =PP1V2_PWRON_HT

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - SB_HT_200M
 Stuffs resistor to select 200MHz HT 1/F.



Shasta HyperTransport

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SCALE	NONE	SHT	OF
		103	154

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

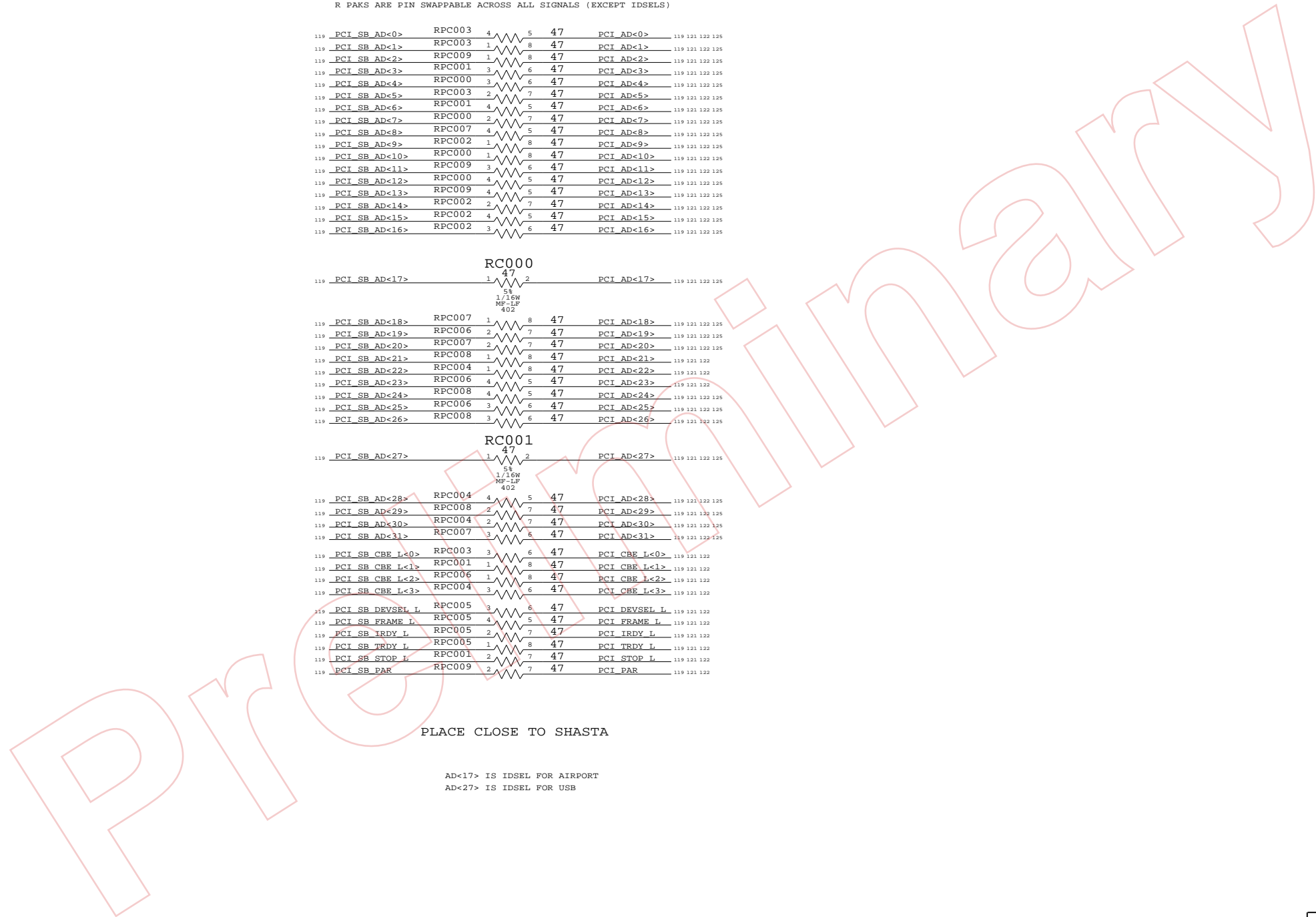
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119	PCI_SB_AD<1>	RPC003	1	8	47	PCI_AD<1>	119 121 122 125
119	PCI_SB_AD<2>	RPC009	1	8	47	PCI_AD<2>	119 121 122 125
119	PCI_SB_AD<3>	RPC001	3	6	47	PCI_AD<3>	119 121 122 125
119	PCI_SB_AD<4>	RPC000	3	6	47	PCI_AD<4>	119 121 122 125
119	PCI_SB_AD<5>	RPC003	2	7	47	PCI_AD<5>	119 121 122 125
119	PCI_SB_AD<6>	RPC001	4	5	47	PCI_AD<6>	119 121 122 125
119	PCI_SB_AD<7>	RPC000	2	7	47	PCI_AD<7>	119 121 122 125
119	PCI_SB_AD<8>	RPC007	4	5	47	PCI_AD<8>	119 121 122 125
119	PCI_SB_AD<9>	RPC002	1	8	47	PCI_AD<9>	119 121 122 125
119	PCI_SB_AD<10>	RPC000	1	8	47	PCI_AD<10>	119 121 122 125
119	PCI_SB_AD<11>	RPC009	3	6	47	PCI_AD<11>	119 121 122 125
119	PCI_SB_AD<12>	RPC000	4	5	47	PCI_AD<12>	119 121 122 125
119	PCI_SB_AD<13>	RPC009	4	5	47	PCI_AD<13>	119 121 122 125
119	PCI_SB_AD<14>	RPC002	2	7	47	PCI_AD<14>	119 121 122 125
119	PCI_SB_AD<15>	RPC002	4	5	47	PCI_AD<15>	119 121 122 125
119	PCI_SB_AD<16>	RPC002	3	6	47	PCI_AD<16>	119 121 122 125

119	PCI_SB_AD<17>	RC000	1	47	2	PCI_AD<17>	119 121 122 125
119	PCI_SB_AD<18>	RPC007	1	8	47	PCI_AD<18>	119 121 122 125
119	PCI_SB_AD<19>	RPC006	2	7	47	PCI_AD<19>	119 121 122 125
119	PCI_SB_AD<20>	RPC007	2	7	47	PCI_AD<20>	119 121 122 125
119	PCI_SB_AD<21>	RPC008	1	8	47	PCI_AD<21>	119 121 122
119	PCI_SB_AD<22>	RPC004	1	8	47	PCI_AD<22>	119 121 122
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119	PCI_SB_AD<24>	RPC008	4	5	47	PCI_AD<24>	119 121 122 125
119	PCI_SB_AD<25>	RPC006	3	6	47	PCI_AD<25>	119 121 122 125
119	PCI_SB_AD<26>	RPC008	3	6	47	PCI_AD<26>	119 121 122 125

119	PCI_SB_AD<27>	RC001	1	47	2	PCI_AD<27>	119 121 122 125
119	PCI_SB_AD<28>	RPC004	4	5	47	PCI_AD<28>	119 121 122 125
119	PCI_SB_AD<29>	RPC008	2	7	47	PCI_AD<29>	119 121 122 125
119	PCI_SB_AD<30>	RPC004	2	7	47	PCI_AD<30>	119 121 122 125
119	PCI_SB_AD<31>	RPC007	3	6	47	PCI_AD<31>	119 121 122 125
119	PCI_SB_CBE_L<0>	RPC003	3	6	47	PCI_CBE_L<0>	119 121 122
119	PCI_SB_CBE_L<1>	RPC001	1	8	47	PCI_CBE_L<1>	119 121 122
119	PCI_SB_CBE_L<2>	RPC006	1	8	47	PCI_CBE_L<2>	119 121 122
119	PCI_SB_CBE_L<3>	RPC004	3	6	47	PCI_CBE_L<3>	119 121 122
119	PCI_SB_DEVSEL_L	RPC005	3	6	47	PCI_DEVSEL_L	119 121 122
119	PCI_SB_FRAME_L	RPC005	4	5	47	PCI_FRAME_L	119 121 122
119	PCI_SB_IRDY_L	RPC005	2	7	47	PCI_IRDY_L	119 121 122
119	PCI_SB_TRDY_L	RPC005	1	8	47	PCI_TRDY_L	119 121 122
119	PCI_SB_STOP_L	RPC001	2	7	47	PCI_STOP_L	119 121 122
119	PCI_SB_PAR	RPC009	2	7	47	PCI_PAR	119 121 122

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB



PCI SERIES TERMINATION

SYNC_MASTER=FINO-MW SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT	OF	
NONE	120	154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
 - _PP3V3_PCI

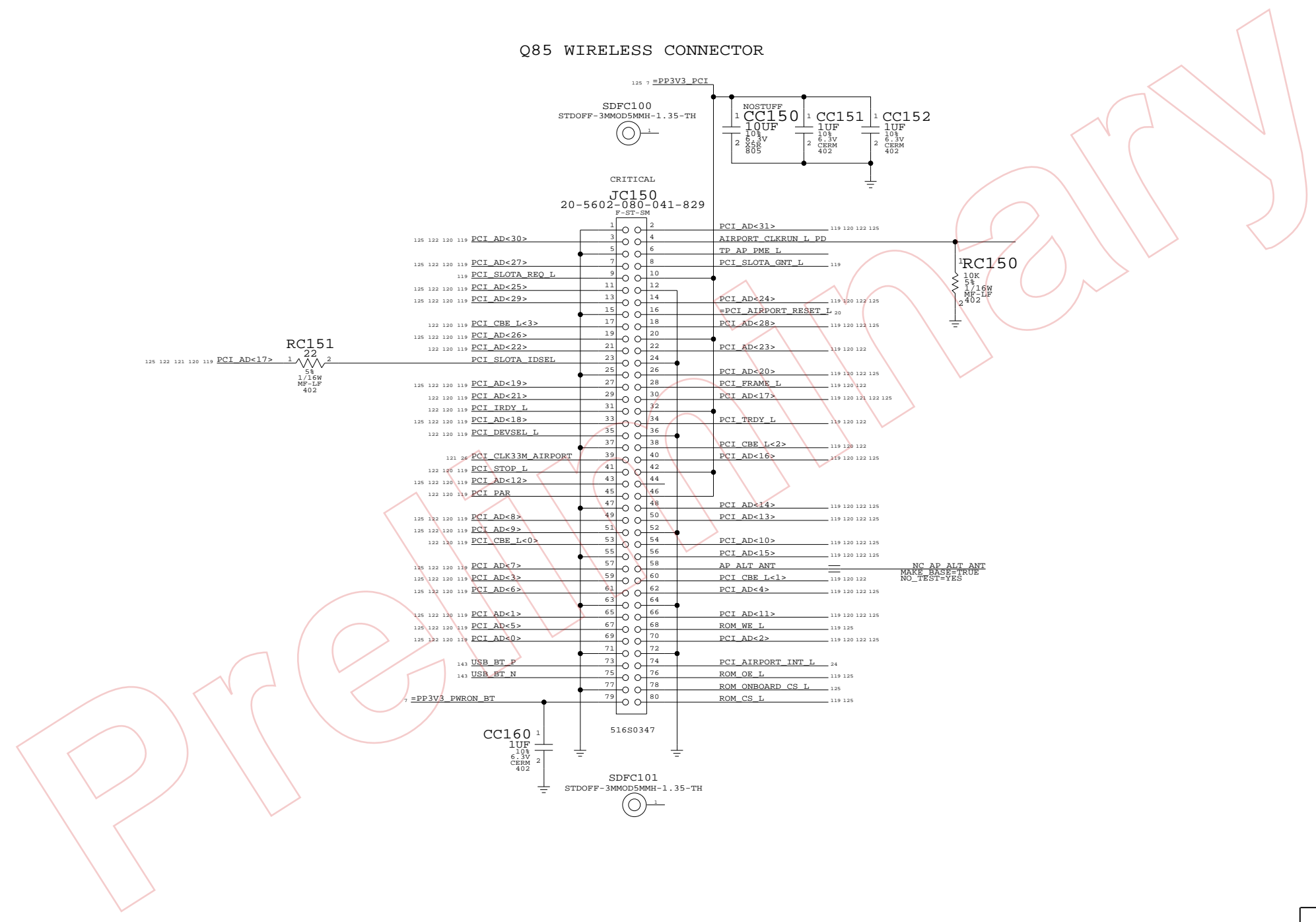
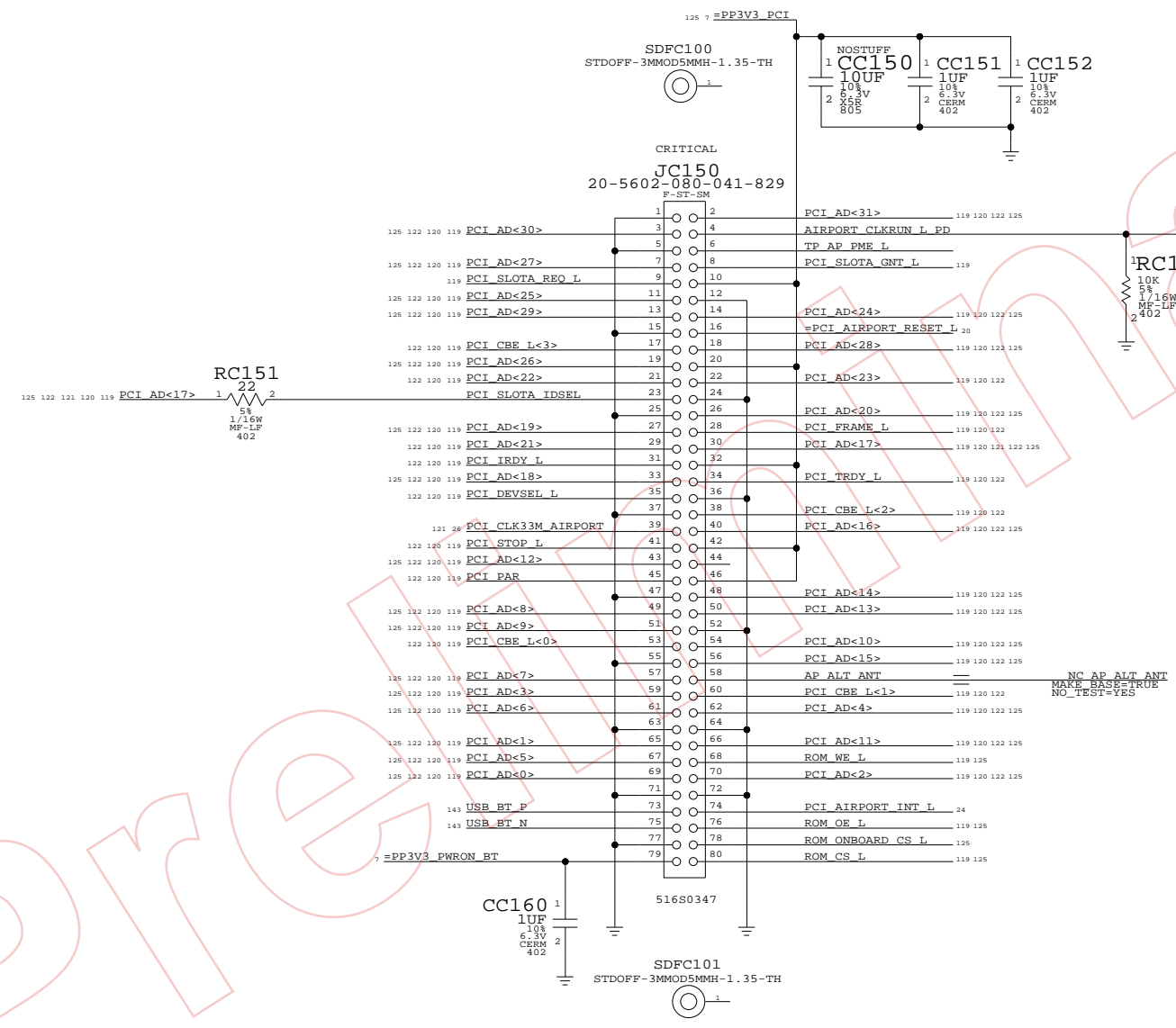
Signal aliases required by this page:
 - _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH
 SYNC_MASTER=FINO-MW SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	NONE	SHT OF	121 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	=PCI_CLK33M_USB2

Page Notes

Power aliases required by this page:
 - _PPVIO_PCI (to 3.3V or 5V)

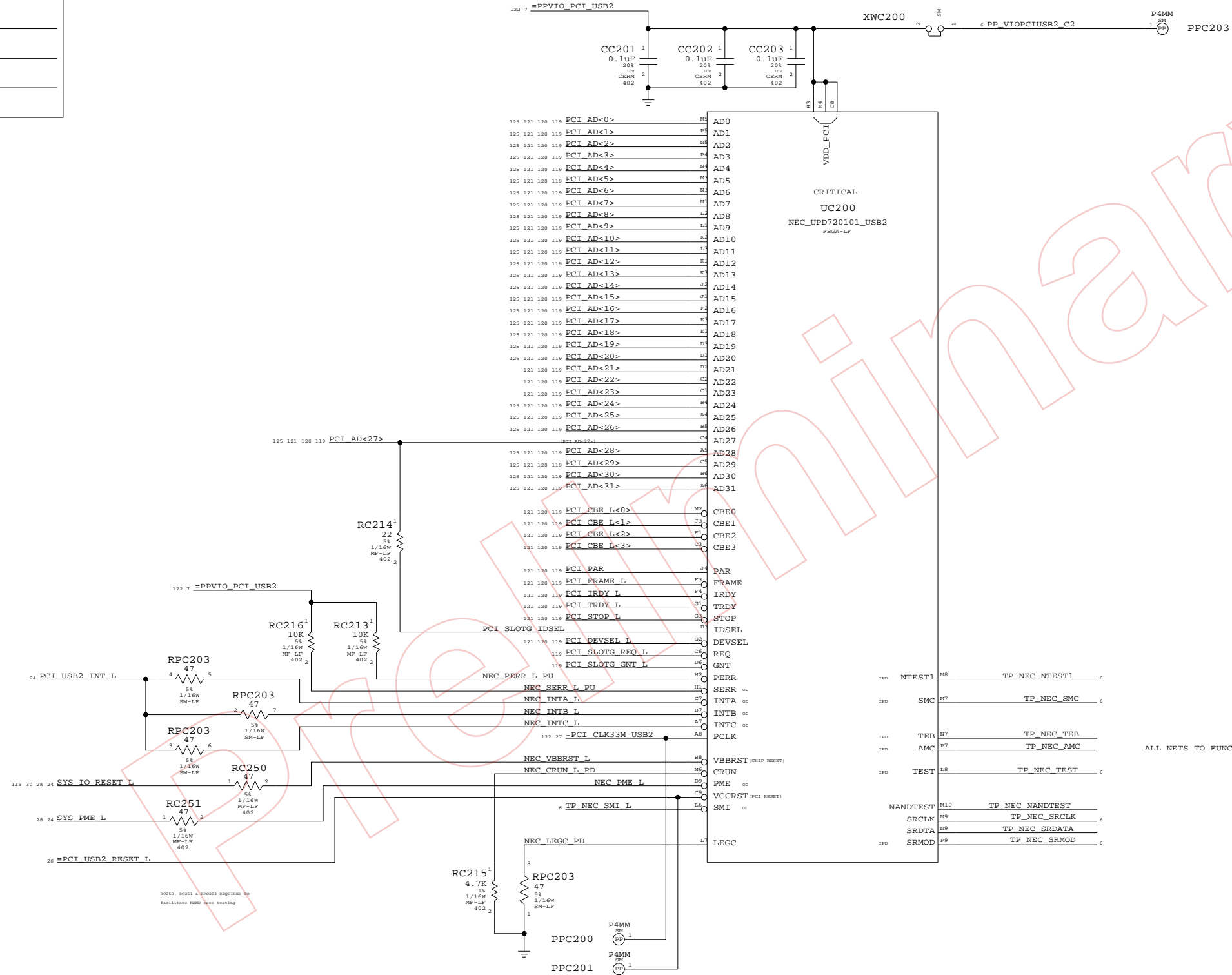
Signal aliases required by this page:
 - _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports Discold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN



USB 2.0 PCI Interface
 SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	NONE	SHT	OF
		122	154

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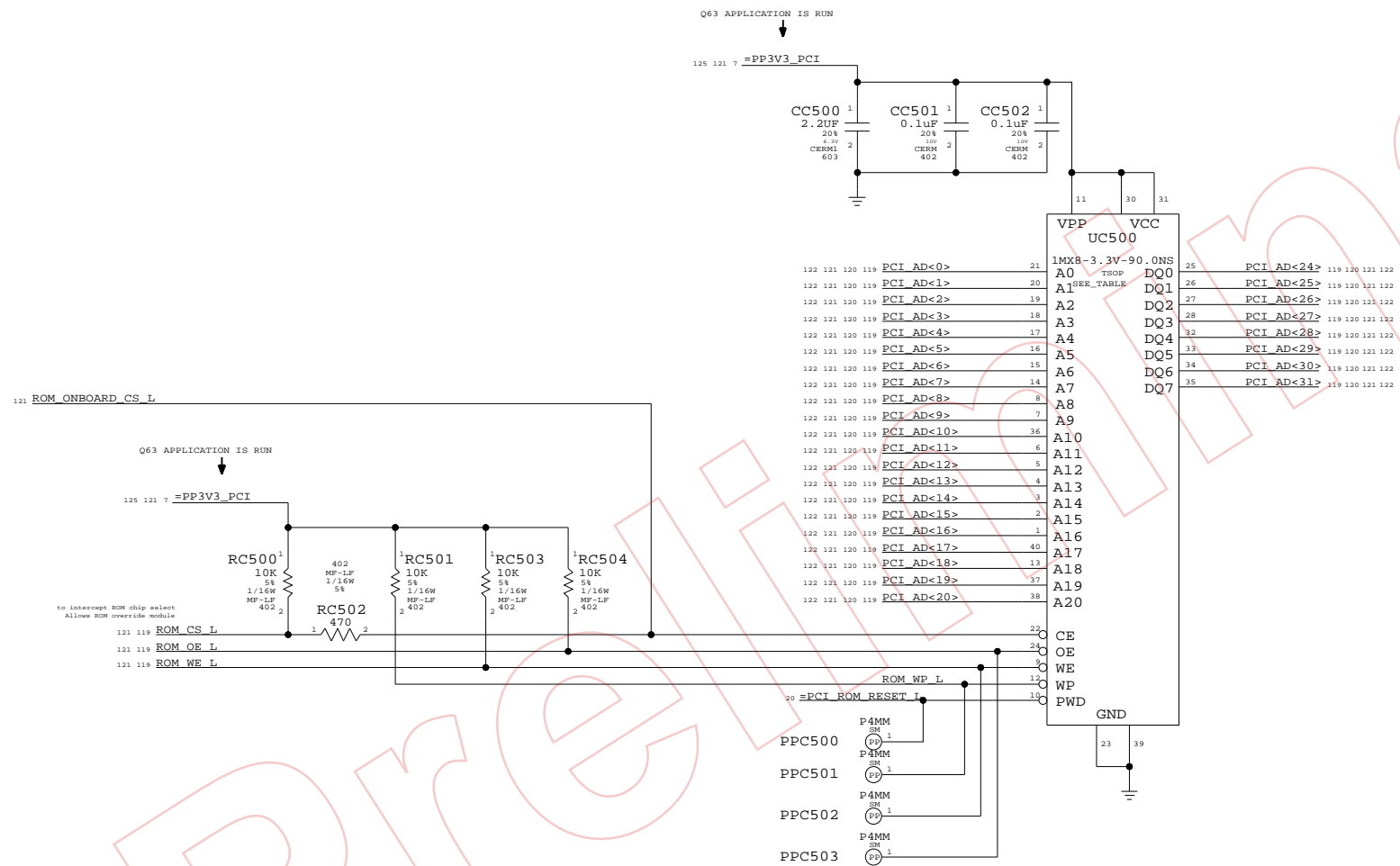
Page Notes

Power aliases required by this page:
 - #PP3V3_PCI

Signal aliases required by this page:
 (NONE)

BCM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

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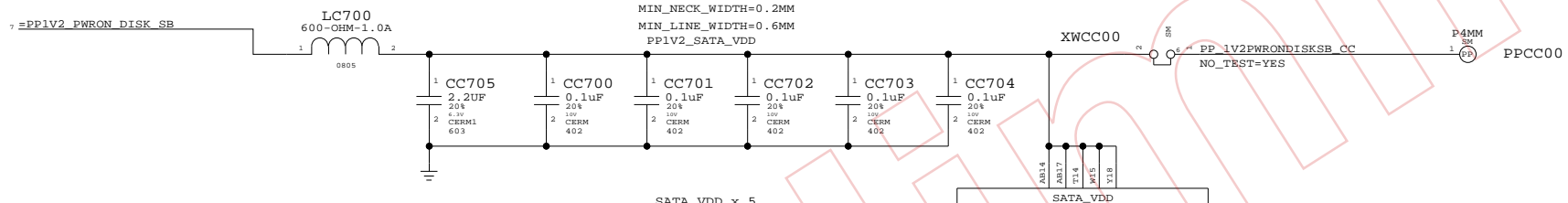
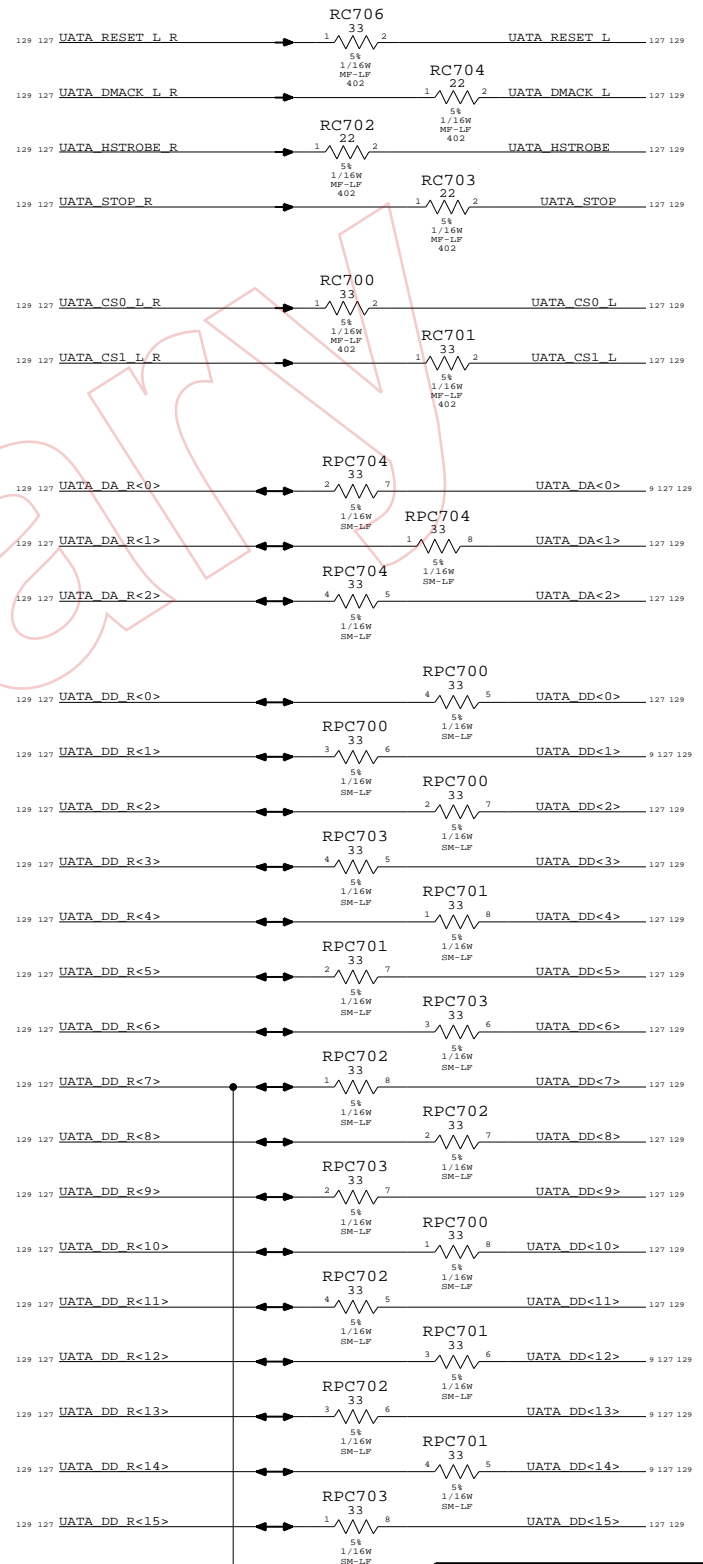
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT OF		
NONE	125 OF 154		

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	SATA	SATA	SATA_RXD1_C
	SATA	SATA	SATA_RXD1_C
	SATA	SATA	SATA_TXD1
	SATA	SATA	SATA_TXD1
	SATA	SATA	SATA_RXD2_C
	SATA	SATA	SATA_RXD2_C
	SATA	SATA	SATA_TXD2
	SATA	SATA	SATA_TXD2
			UATA_DD<15..8>
			UATA_DD<7>
			UATA_DD<6..0>
			UATA_DA<2..0>
			UATA_CS1_L
			UATA_CS1_L
			UATA_HSTROBE
			UATA_STOP
			UATA_DMACK_L
			UATA_RESET_L
			UATA_DSTROBE
			UATA_DMARQ
			UATA_INTRO
			UATA_DD_R<15..8>
			UATA_DD_R<7>
			UATA_DD_R<6..0>
			UATA_DA_R<2..0>
			UATA_CS0_L_R
			UATA_CS1_L_R
			UATA_DMACK_L_R
			UATA_HSTROBE_R
			UATA_STOP_R
			UATA_RESET_L_R

PLACE TERMINATION RESISTORS AT UATA CONNECTOR JC901



Page Notes

- Power aliases required by this page:
 - _PP1V2_PWRON_DISK
 - Signal aliases required by this page:
 - (NONE)
 - BOM options provided by this page:
 - (NONE)
- Net Spacing Type: SATA
- Line To Line: 0.38mm
 Length Tolerance: 1.27mm
 Primary Max Sep: 0.25mm outer
 Primary Max Sep: 0.23mm inner
 Secondary Max Sep: 2.54mm
 Secondary Length: 12.70mm
- NOTE: Target differential impedance for SATA data pairs is 100 ohms.

UATA	UATA	UATA
UD_IDEDD_0_H	U76	UATA_DD_R<0>
UD_IDEDD_1_H	H7	UATA_DD_R<1>
UD_IDEDD_2_H	H6	UATA_DD_R<2>
UD_IDEDD_3_H	E2	UATA_DD_R<3>
UD_IDEDD_4_H	C1	UATA_DD_R<4>
UD_IDEDD_5_H	C2	UATA_DD_R<5>
UD_IDEDD_6_H	E3	UATA_DD_R<6>
UD_IDEDD_7_H	O6	UATA_DD_R<7>
UD_IDEDD_8_H	O5	UATA_DD_R<8>
UD_IDEDD_9_H	D4	UATA_DD_R<9>
UD_IDEDD_10_H	O7	UATA_DD_R<10>
UD_IDEDD_11_H	F6	UATA_DD_R<11>
UD_IDEDD_12_H	C3	UATA_DD_R<12>
UD_IDEDD_13_H	F5	UATA_DD_R<13>
UD_IDEDD_14_H	E5	UATA_DD_R<14>
UD_IDEDD_15_H	O5	UATA_DD_R<15>
UD_IDEDA0_H	E6	UATA_DA_R<0>
UD_IDEDA1_H	C4	UATA_DA_R<1>
UD_IDEDA2_H	D6	UATA_DA_R<2>
UD_IDECS1FX_L	B3	UATA_CS0_L_R
UD_IDECS3FX_L	B4	UATA_CS1_L_R
UD_IDEDMACK_L	B8	UATA_DMACK_L_R
UD_IDEDMARQ_H	B4	UATA_DMARQ
UD_IDERD_L	B4	UATA_HSTROBE_R
UD_IDEWR_L	D3	UATA_STOP_R
UD_IDERST_L	B7	UATA_RESET_L_R
RXDP1	AA16	SATA_TXD_P1
RXDN1	AB16	SATA_TXD_N1
RXDP2	Y15	SATA_TXD_P2
RXDN2	Y14	SATA_TXD_N2

AC coupling required for any SATA pair used.
 Recommended 0.1uF cap placed close to Shasta.
 (Caps provided by device page)

Shasta Disk

SYNC_MASTER=M23-DC SYNC_DATE=06/20/2005

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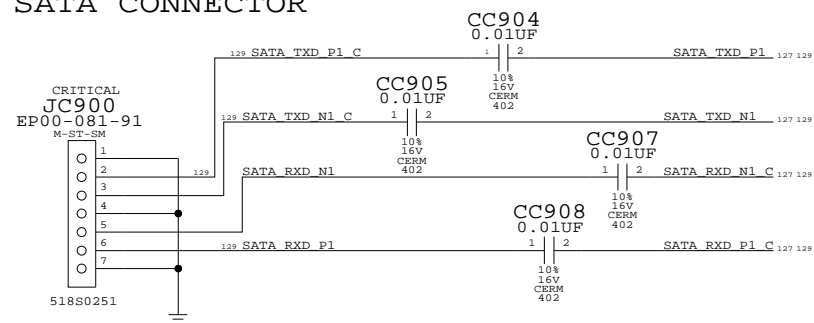
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHEET OF		
NONE	127 OF 154		

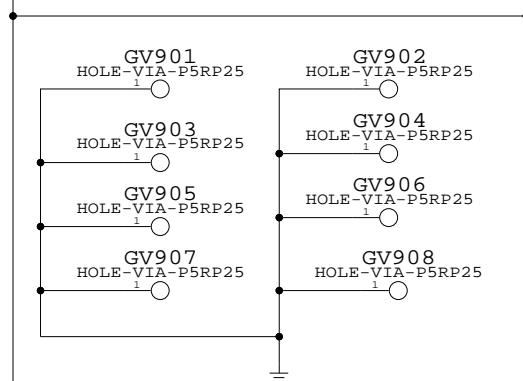
SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

- 127 SATA TXD P2 == NC_SATA_TXD_P2 6 MAKE_BASE=TRUE
- 127 SATA TXD N2 == NC_SATA_TXD_N2 6 MAKE_BASE=TRUE
- 127 SATA RXD N2 C == NC_SATA_RXD_N2_C 6 MAKE_BASE=TRUE
- 127 SATA RXD P2 C == NC_SATA_RXD_P2_C 6 MAKE_BASE=TRUE

SATA DIFF PAIR GND VIAS



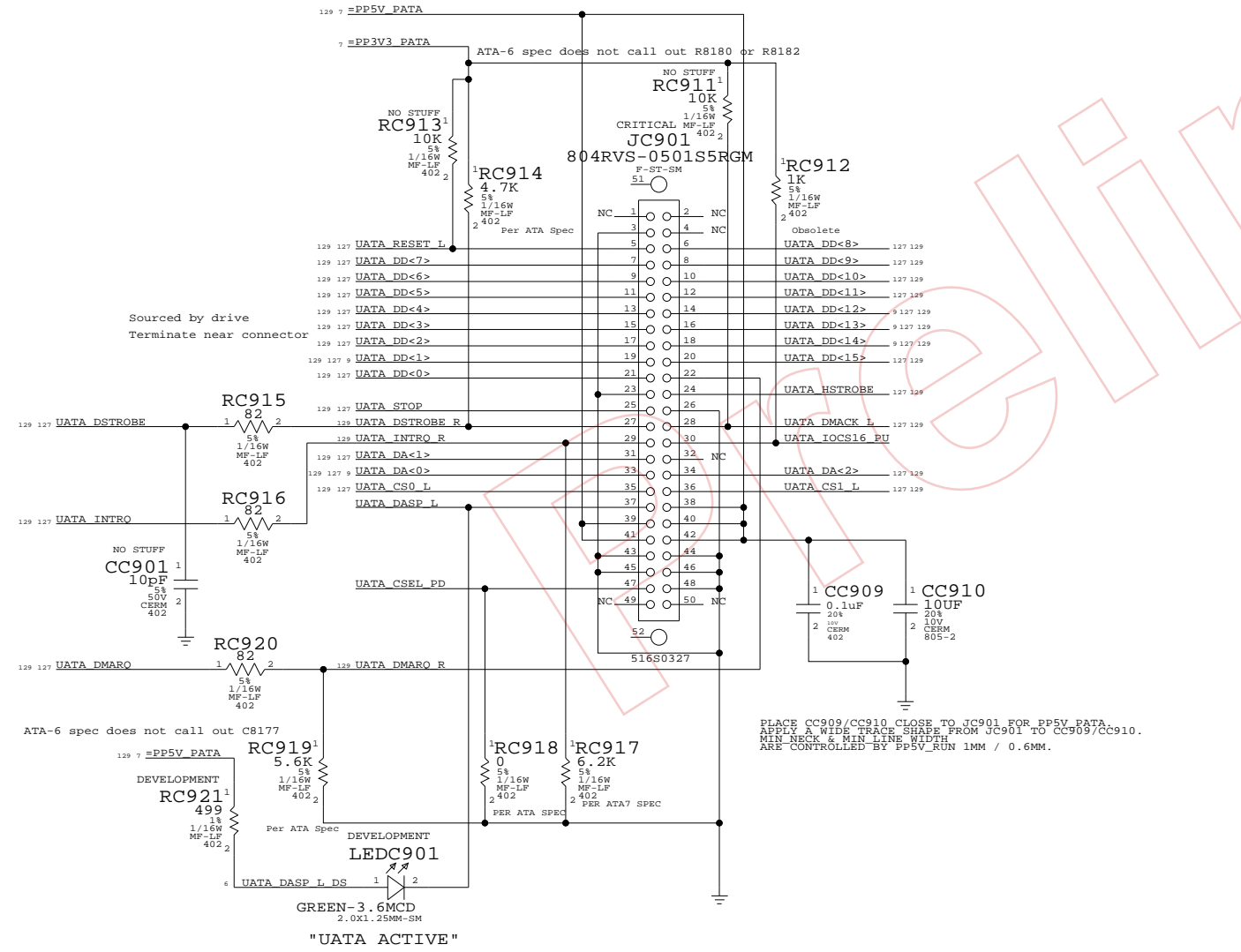
4-12-05
ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA NO CLOSER THAN 0.152MM TO SIGNAL VIA.

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
129 127 UATA_DD<15>_S>	UATA_DD	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DD<6>_0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DA<2>_0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_HSTROBE	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
129 127 UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DMARQ	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
129 127 UATA_INTRO_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DD_R<15>_S>	UATA_NETPH	UATA_NETSPA			
129 127 UATA_DD_R<7>	UATA_NETPH	UATA_NETSPA			
129 127 UATA_DD_R<6>_0>	UATA_NETPH	UATA_NETSPA			
129 127 UATA_DA_R<2>_0>	UATA_NETPH	UATA_NETSPA			
129 127 UATA_CS0_L_R	UATA_NETPH	UATA_NETSPA			
129 127 UATA_CS1_L_R	UATA_NETPH	UATA_NETSPA			
129 127 UATA_HSTROBE_R	UATA_NETPH	UATA_NETSPA			
129 127 UATA_STOP_R	UATA_NETPH	UATA_NETSPA			
129 127 UATA_DMACK_L_R	UATA_NETPH	UATA_NETSPA			
129 127 UATA_RESET_L_R	UATA_NETPH	UATA_NETSPA			
129 127 UATA_DSTROBE	UATA_NETPH	UATA_NETSPA			
129 127 UATA_DMARQ	UATA_NETPH	UATA_NETSPA			
129 127 UATA_INTRO	UATA_NETPH	UATA_NETSPA			
129 127 SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
129 127 SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
129 127 SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
129 127 SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
129 127 SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
129 127 SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
129 127 SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
129 127 SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

UATA FROM RPAKS TO JC901

UATA FROM SHASTA U2300 TO RPAKS

PATA CONNECTOR



4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.
UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE FOR PP1V2_SATA_VDD AND THEN NECK DOWN TO THE DEFAULT VALUE WHEN NECESSARY. THE WIDTH/NECK PROPERTIES ON PAGE 127 ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL HELP MITIGATE THE LOSS ACROSS THE Q1306 FET SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M23-DC SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.

SCALE: NONE

DRAWING NUMBER: D 051-6790

SIT: 129 OF 154

REV: E

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PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA₈ -> VESTA

131	9	ENET_TXD_R<0>	159	MAKE_BASE=TRUE	ENET_TXD<0>	9	131	132
131	9	ENET_TXD_R<1>	160	MAKE_BASE=TRUE	ENET_TXD<1>	9	131	132
131	9	ENET_TXD_R<2>	161	MAKE_BASE=TRUE	ENET_TXD<2>	9	131	132
131	9	ENET_TXD_R<3>	162	MAKE_BASE=TRUE	ENET_TXD<3>	9	131	132
131	9	ENET_TXD_R<4>	163	MAKE_BASE=TRUE	ENET_TXD<4>	9	131	132
131	9	ENET_TXD_R<5>	164	MAKE_BASE=TRUE	ENET_TXD<5>	9	131	132
131	9	ENET_TXD_R<6>	165	MAKE_BASE=TRUE	ENET_TXD<6>	9	131	132
131	9	ENET_TXD_R<7>		MAKE_BASE=TRUE	ENET_TXD<7>	9	131	132
			166					
131	9	ENET_TX_EN_R	167	MAKE_BASE=TRUE	ENET_TX_EN	9	131	132
131	9	ENET_TX_ER_R		MAKE_BASE=TRUE	ENET_TX_ER	9	131	132
			168					
131	9	ENET_CLK125M_GTX_R		MAKE_BASE=TRUE	ENET_CLK125M_GTX	131	132	
			169					
131	9	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131	132	

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

			184					
132	ENET_CLK125M_GBE_REF_R		MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	132			
			170					
132	ENET_CLK25M_TX_R		MAKE_BASE=TRUE	ENET_CLK25M_TX	131			
			171					
132	ENET_CLK125M_RX_R		MAKE_BASE=TRUE	ENET_CLK125M_RX	131			
			172					
132	9	ENET_RXD_R<0>	173	MAKE_BASE=TRUE	ENET_RXD<0>	9	131	
132	9	ENET_RXD_R<1>	174	MAKE_BASE=TRUE	ENET_RXD<1>	9	131	
132	9	ENET_RXD_R<2>	175	MAKE_BASE=TRUE	ENET_RXD<2>	9	131	
132	9	ENET_RXD_R<3>	176	MAKE_BASE=TRUE	ENET_RXD<3>	9	131	
132	9	ENET_RXD_R<4>	177	MAKE_BASE=TRUE	ENET_RXD<4>	9	131	
132	9	ENET_RXD_R<5>	178	MAKE_BASE=TRUE	ENET_RXD<5>	9	131	
132	9	ENET_RXD_R<6>	179	MAKE_BASE=TRUE	ENET_RXD<6>	9	131	
132	9	ENET_RXD_R<7>		MAKE_BASE=TRUE	ENET_RXD<7>	9	131	
			180					
132	9	ENET_RX_DV_R	181	MAKE_BASE=TRUE	ENET_RX_DV	131		
132	9	ENET_RX_ER_R		MAKE_BASE=TRUE	ENET_RX_ER	131		
			182					
132	9	ENET_COL_R	183	MAKE_BASE=TRUE	ENET_COL	131		
132	9	ENET_CR_S_R		MAKE_BASE=TRUE	ENET_CR_S	131		

Preliminary

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ENET SERIES TERM
 SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005
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	D	051-6790	E
SCALE	SHT	OF	
NONE	130	154	

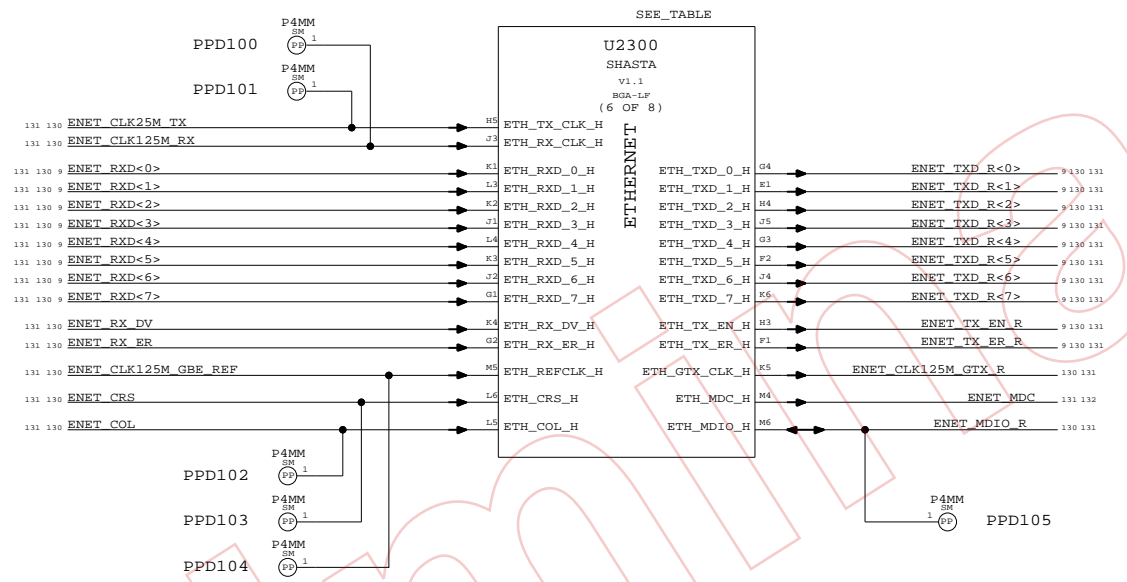
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET	0.38mm SPACING	ENET_CLK25M_TX 130 131
ENET	0.38mm SPACING	ENET_CLK125M_RX 130 131
ENET	0.38mm SPACING	ENET_CLK125M_GBR_REF 130 131
ENET	0.38mm SPACING	ENET_CLK125M_GTX 130 132
ENET	0.38mm SPACING	ENET_CLK125M_GTX_R 130 131
ENET	ENET_FW_2X	ENET_RXD_R<7..0> 9 130 132
ENET	ENET_FW_3X	ENET_RX_DV_R 130 132
ENET	ENET_FW_3X	ENET_RX_ER_R 130 132
ENET	ENET_FW_2X	ENET_RXD<7..0> 9 130 131
ENET	ENET_FW_3X	ENET_RX_DV 130 131
ENET	ENET_FW_3X	ENET_RX_ER 130 131
ENET	ENET_FW_2X	ENET_TXD_R<7..0> 9 130 131
ENET	ENET_FW_3X	ENET_TX_EN_R 9 130 131
ENET	ENET_FW_3X	ENET_TX_ER_R 9 130 131
ENET	ENET_FW_2X	ENET_TXD<7..0> 9 130 132
ENET	ENET_FW_3X	ENET_TX_EN 9 130 132
ENET	ENET_FW_3X	ENET_TX_ER 9 130 132
ENET	ENET_FW_3X	ENET_CR_S_R 130 132
ENET	ENET_FW_3X	ENET_COL_R 130 132
ENET	ENET_FW_3X	ENET_CR_S 130 131
ENET	ENET_FW_3X	ENET_COL 130 131
ENET	ENET_FW_3X	ENET_MDC 131 132
ENET	ENET_FW_3X	ENET_MDIO 130 131 132
ENET	ENET_FW_3X	ENET_MDIO_R 130 131
ENET	ENET_FW_3X	R8405_1 131
ENET	ENET_FW_3X	R8405_2 131
ENET	ENET_FW_3X	R8407_2 131

Page Notes

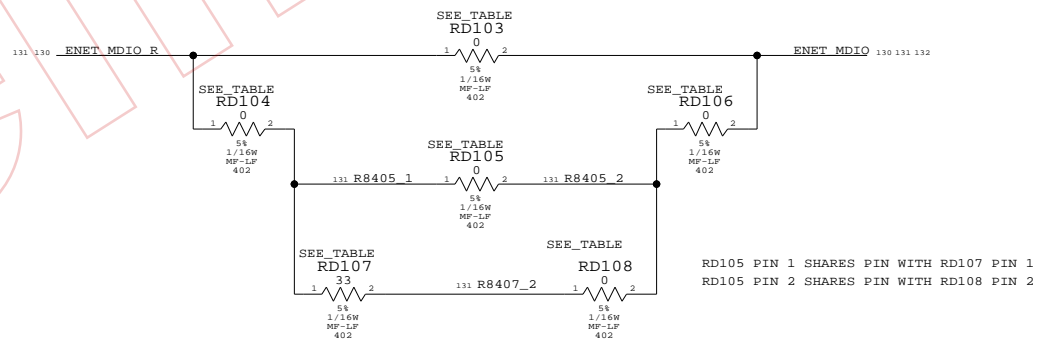
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES, 0-OHM, 402, 5%	RD103		ENET_MDIO_DELAY_0 *
116S0004	3	RES, 0-OHM, 402, 5%	RD104, RD105, RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES, 0-OHM, 402, 5%	RD104, RD108, RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES, 33-OHM, 402, 5%	RD107		ENET_MDIO_DELAY_4NS

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	NONE	SHT	OF
		131	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET	0.38mm SPACING	ENET_CLK125M_GBE_REF_R 130 132
ENET	0.38mm SPACING	ENET_CLK125M_RX_R 130 132
ENET	0.38mm SPACING	ENET_CLK25M_TX_R 130 132
ENET	ENET	ENET_MDI0 132 136
ENET	ENET	ENET_MDI0 132 136
ENET	ENET	ENET_MDI1 132 136
ENET	ENET	ENET_MDI1 132 136
ENET	ENET	ENET_MDI2 132 136
ENET	ENET	ENET_MDI2 132 136
ENET	ENET	ENET_MDI3 132 136
ENET	ENET	ENET_MDI3 132 136
ENET	0.38mm SPACING	VESTA_CLK25M_XTALI 132
ENET	0.38mm SPACING	VESTA_CLK25M_XTALO 132
ENET	0.38mm SPACING	VESTA_CLK25M_XTALO_R 132

Page Notes

Power aliases required by this page:
 - =PP3V3_ENET
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

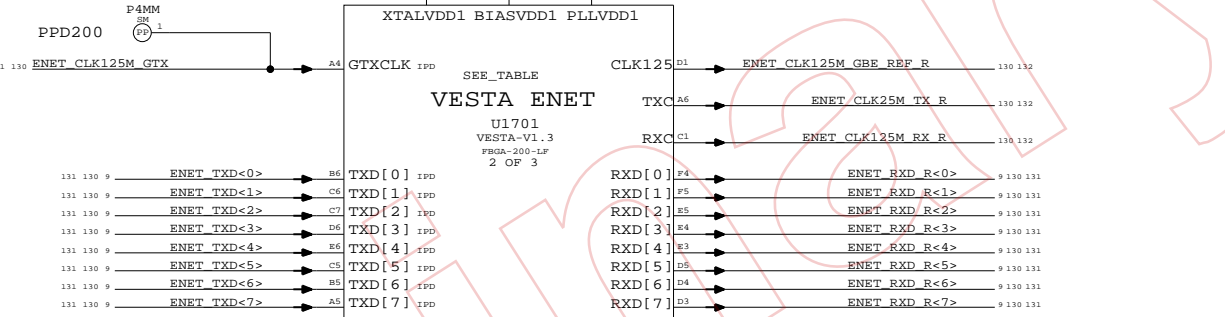
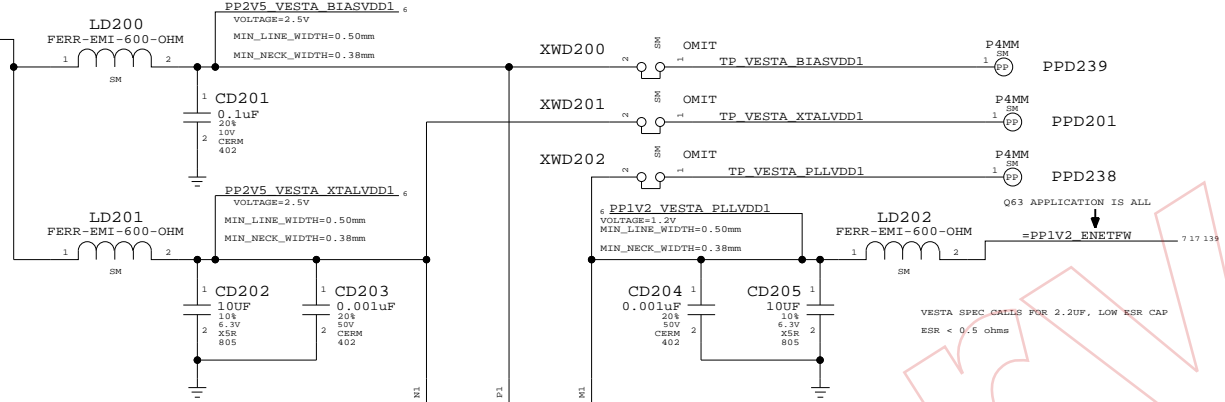
Net Spacing Type: ENET

Line To Line: 0.38mm
 Length Tolerance: 1.27mm
 Primary Max Sep: 0.13mm
 Secondary Max Sep: 2.54mm
 Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

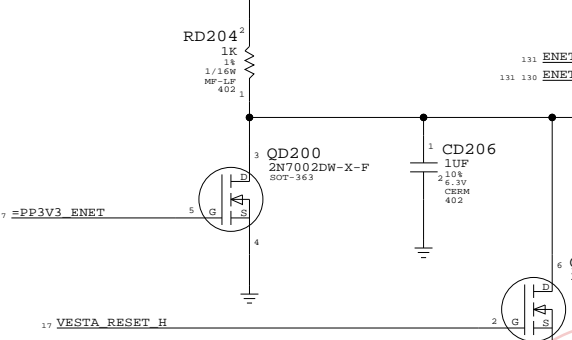
Q63 APPLICATION IS ALL

139 17 7 =PP2V5_ENETFW



Q63 APPLICATION IS ALL

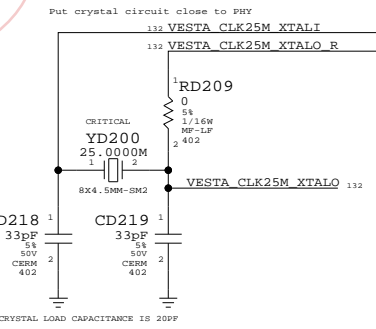
139 17 7 =PP3V3_ENETFW



Vesta Config Straps:

PHYA<4..0> - PHY Address Select (Internal Pull-downs)	MANMS - Manual Master/Slave Configuration Select (Internal Pull-down)
EN_10B - TBI Interface Select (Internal Pull-down)	HUB - Repeater Select (Internal Pull-down)
RGMIEN - RGMI Enable (Internal Pull-down)	ER - Edge Rate Select (Internal Pull-down)
FDX - Full-Duplex Select (Internal Pull-up)	AM_EN - Auto-Negotiation Select (Internal Pull-down)
F1000 - Speed Select (Internal Pull-up)	TXC_RXC_DELAY (Internal Pull-up)
SPD0 - Speed Select (Internal Pull-down)	

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T



INTR*/ENERGYDET ENET_ENERGYDET 24 TERMINATION OFF PAGE

Vesta Ethernet PHY
 SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	NONE	SHT	OF
		132	154

8

7

6

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4

3

2

1

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET	NET PHYSICAL TYPE	VALUE	REF
ENET	ENET MDI P<0>	132 136	
ENET	ENET MDI N<0>	132 136	
ENET	ENET MDI P<1>	132 136	
ENET	ENET MDI N<1>	132 136	
ENET	ENET MDI P<2>	132 136	
ENET	ENET MDI N<2>	132 136	
ENET	ENET MDI P<3>	132 136	
ENET	ENET MDI N<3>	132 136	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDES ON TOP SIDE OF BOARD

D

D

C

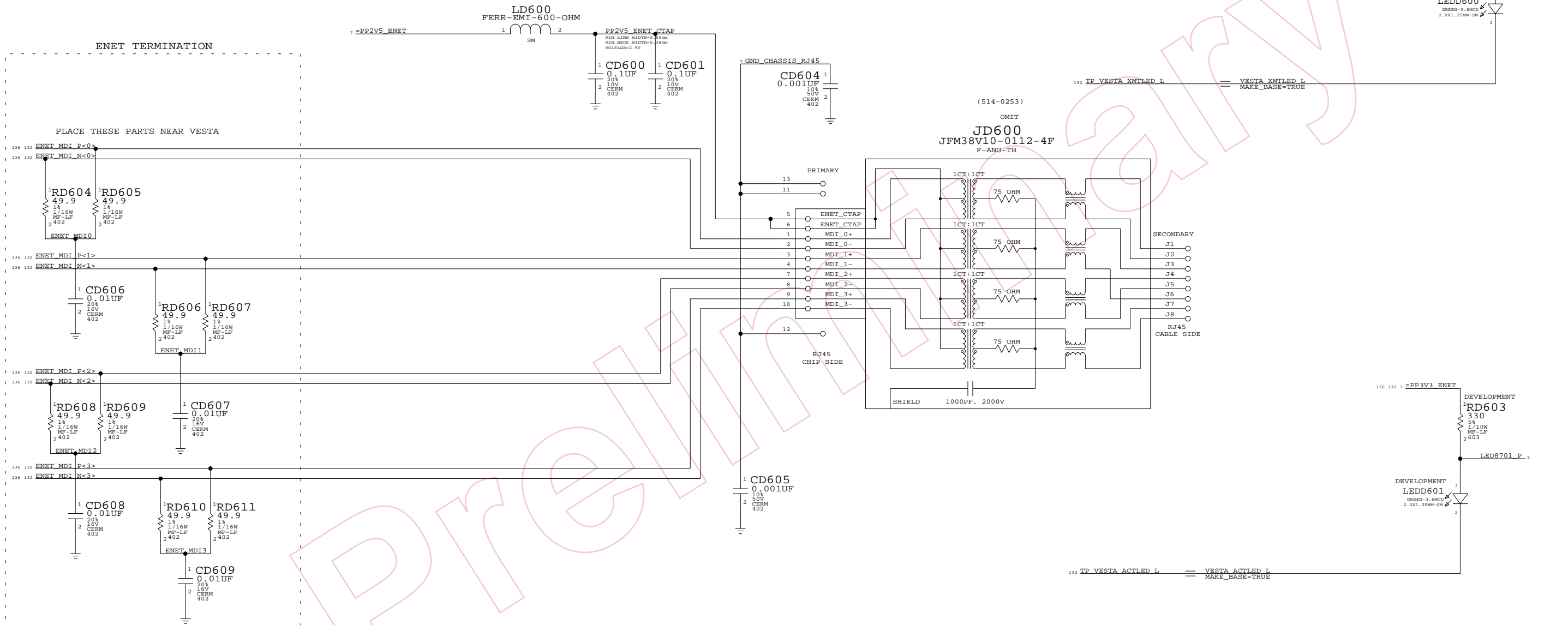
C

B

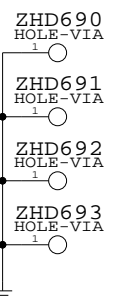
B

A

A



SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING



ETHERNET CONNECTOR
 SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT OF		
NONE	136 OF 154		

8

7

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2

1

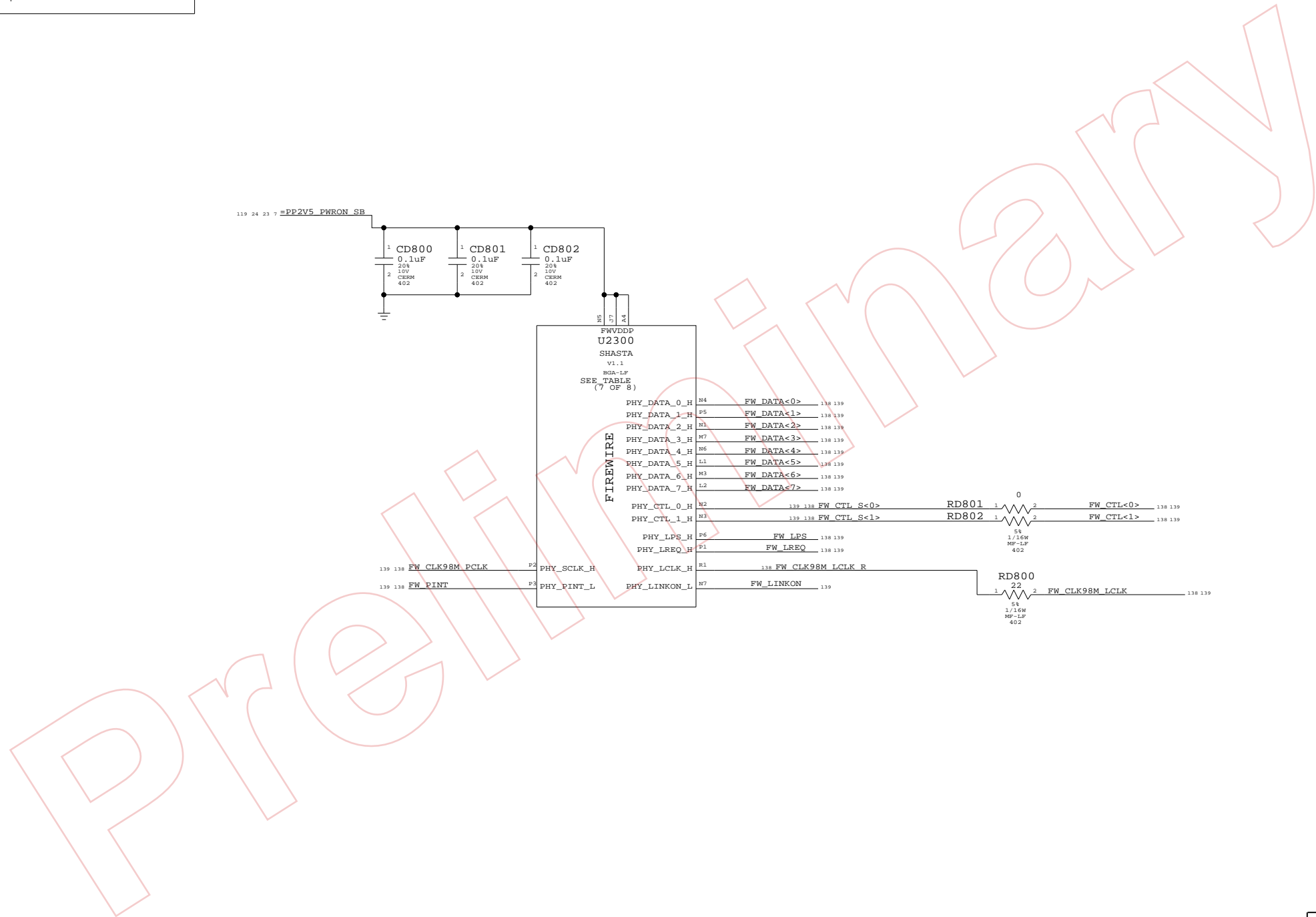
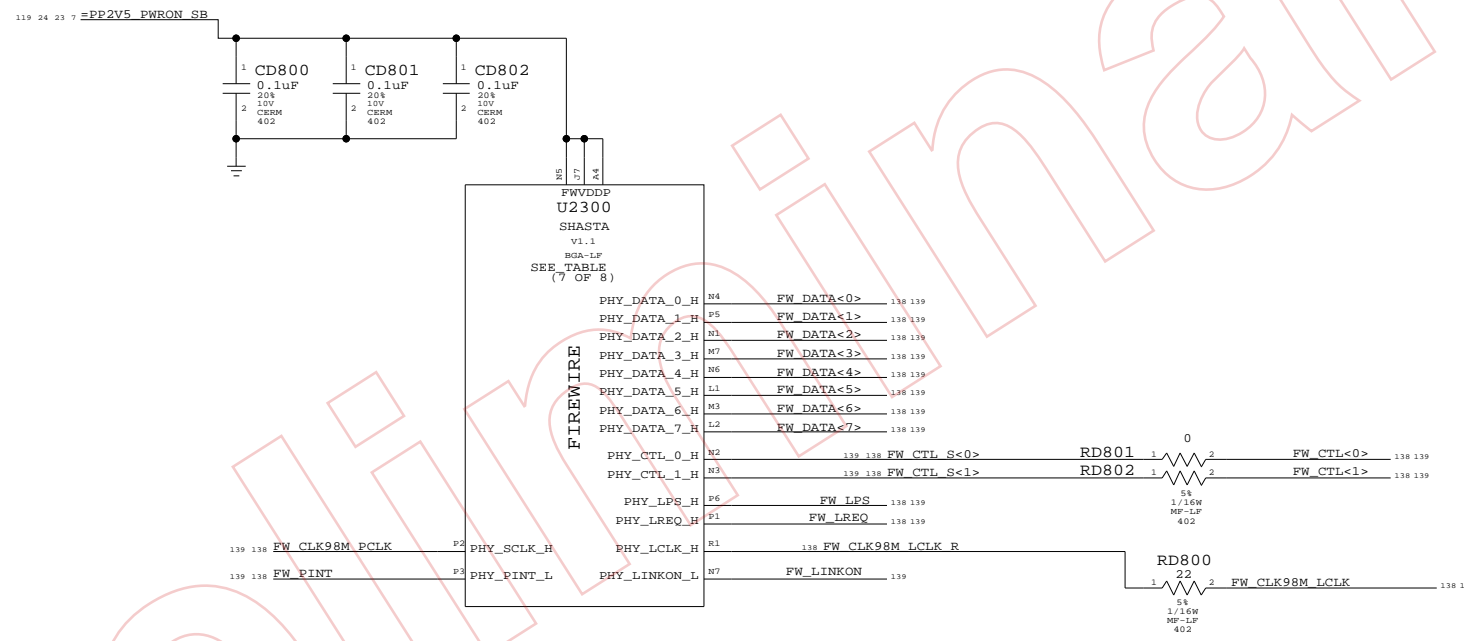
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW	ENET_FW_2X	FW_DATA<7..0>
FW	ENET_FW_3X	FW_CTL_S<1..0>
FW	ENET_FW_3X	FW_CTL<1..0>
FW	ENET_FW_2X	FW_DATA_R<7..0>
FW	ENET_FW_3X	FW_CTL_R<1..0>
FW	ENET_FW_3X	FW_LPS
FW	ENET_FW_3X	FW_LREQ
FW	ENET_FW_3X	FW_PINT
FW	0.38mm SPACING	FW_CLK98M_LCLK
FW	0.38mm SPACING	FW_CLK98M_PCLK
FW	0.38mm SPACING	FW_CLK98M_LCLK_R

Page Notes

Power aliases required by this page:
 - _PP2V5_PWRON_SB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT OF		
NONE	138	154	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
(PROVIDED BY LINK PAGE)		0.38mm SPACING	
	FW	FW	FW_TPA0
	FW	FW	FW_TPA P<0>
	FW	FW	FW_TPB0
	FW	FW	FW_TPB P<0>
	FW	FW	FW_TPA1
	FW	FW	FW_TPA P<1>
	FW	FW	FW_TPB1
	FW	FW	FW_TPB P<1>
	FW	FW	FW_TPA2
	FW	FW	FW_TPA P<2>
	FW	FW	FW_TPB2
	FW	FW	FW_TPB P<2>
		0.38mm SPACING	VESTA_CLK24M_XTALI
		0.38mm SPACING	VESTA_CLK24M_XTALO
		0.38mm SPACING	VESTA_CLK24M_XTALO_R
	FW_CTL		FW_CTL_S<1..0>
	FW_CTL		FW_CTL<1..0>
	FW_CTL		FW_CTL_R<1..0>

Page Notes

Power aliases required by this page:
 - =PPFW_PHY
 - =PP3V3_FW
 - =PP3V3_ENETFW
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - VESTA_DS_ONLY_EN0
 If stuffed, adds external pull-up to counter internal pull-down in Vesta.
 See straps table for more information.
 - VESTA_PWR_CLASS_0
 If stuffed, adds external pull-down to counter internal pull-up in Vesta.
 See straps table for more information.

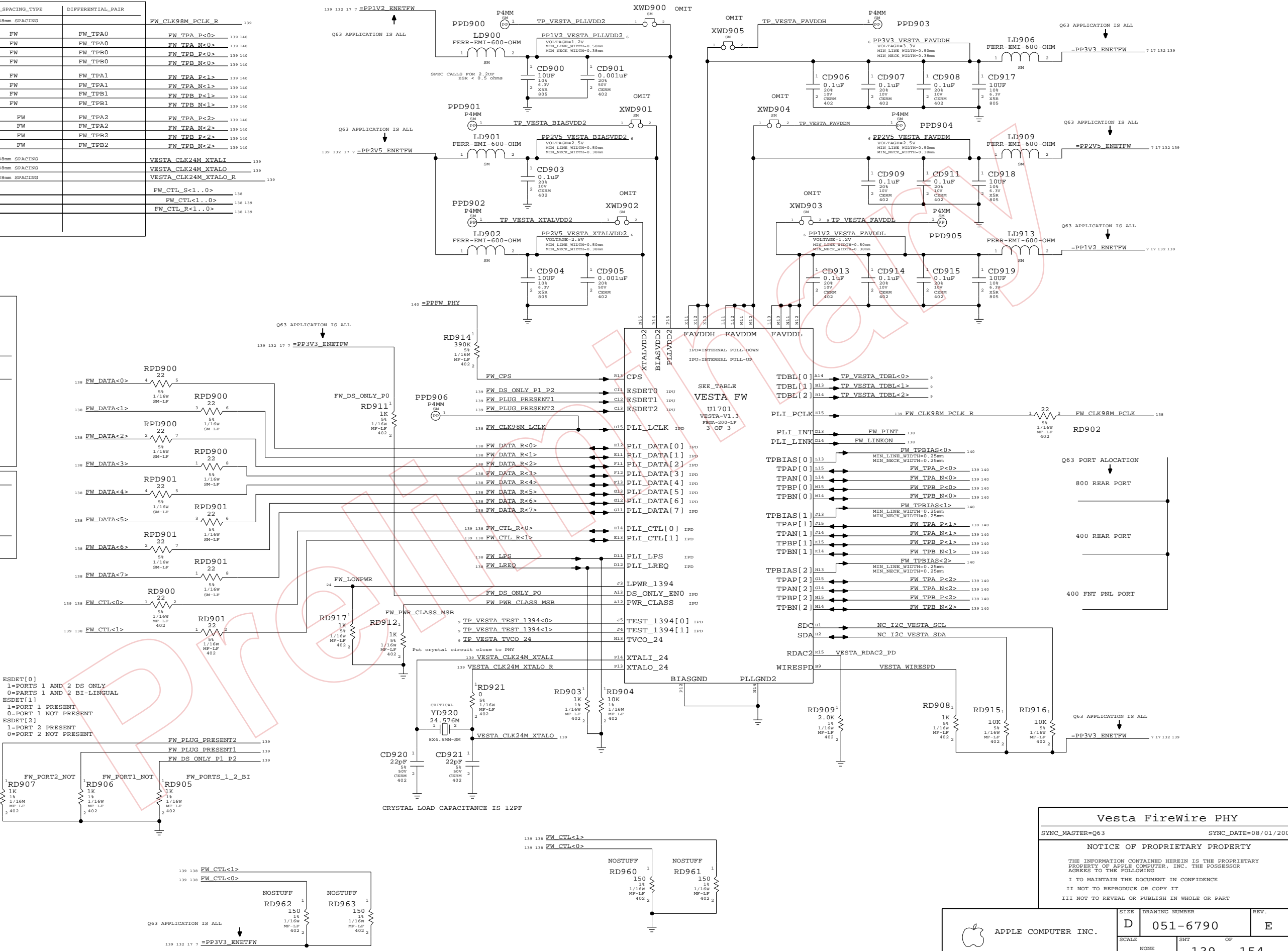
Net Spacing Type: FW

NOTE: Target differential impedance for FW data pairs is 110 ohms.

VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
 1 - Sets Power Class to 0x4
 0 - Sets Power Class to 0x0
 (Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE
 1 - Port 0 Data/Strobe mode only
 0 - Port 0 Billingual mode
 (Internal Pull-down)



Vesta FireWire PHY
 SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

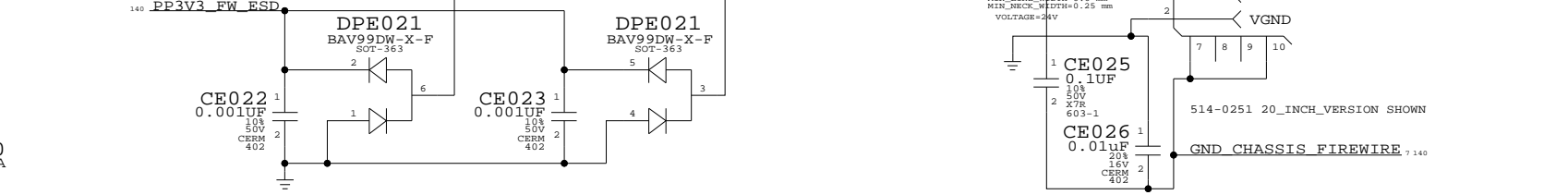
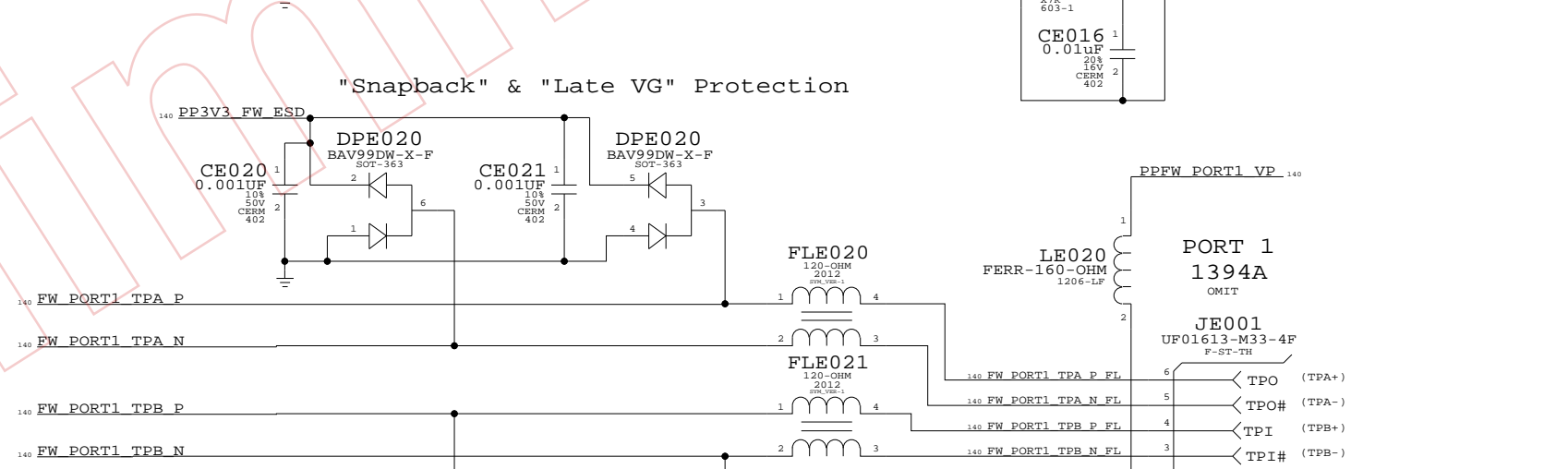
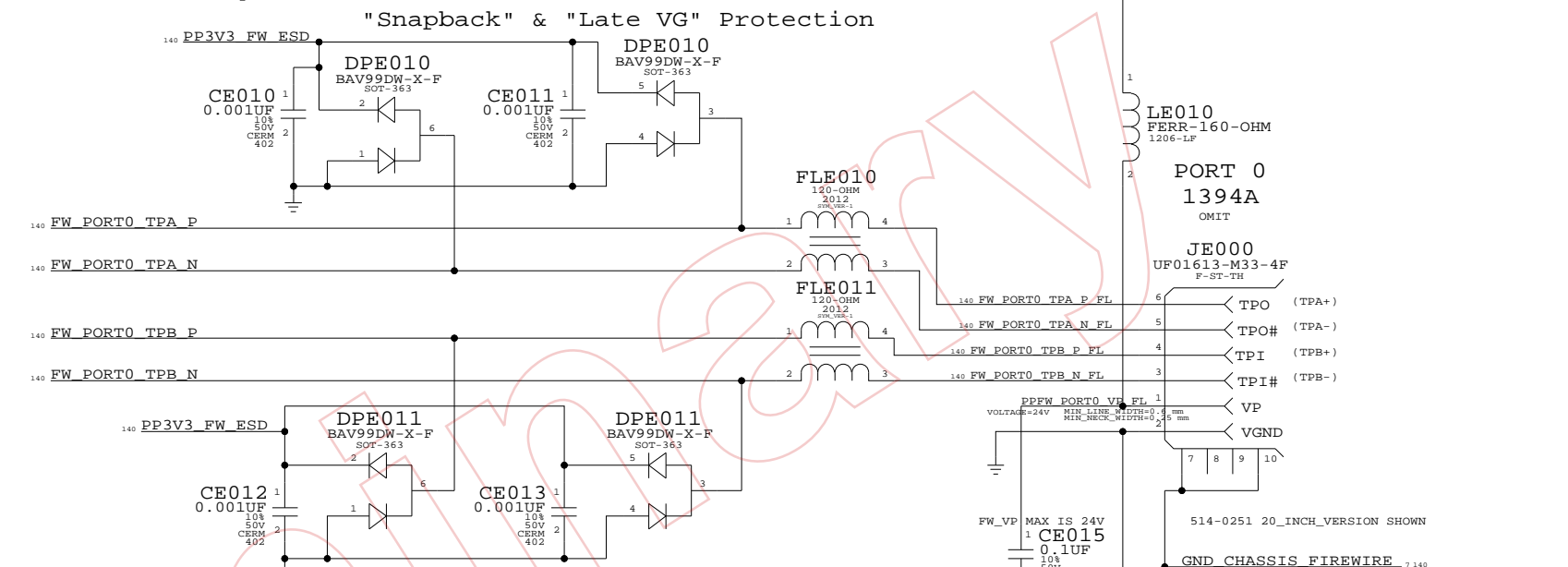
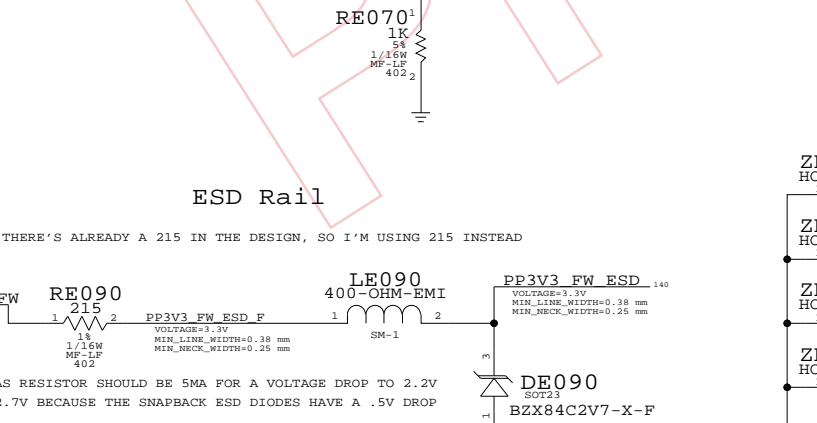
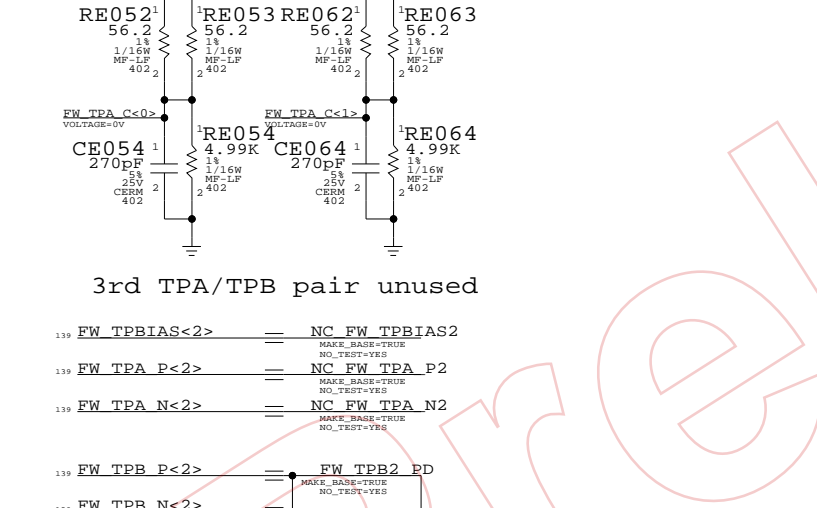
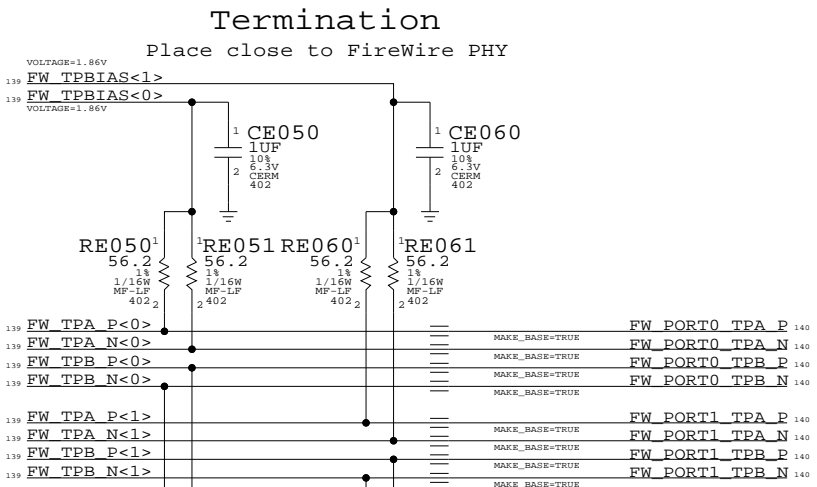
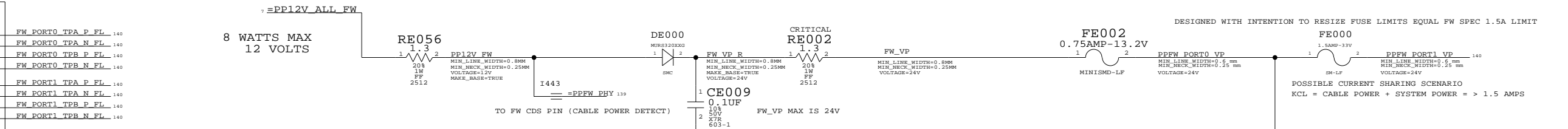
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	SCALE	DRAWING NUMBER		REV.
	NONE	D	051-6790	E
SHEET		OF		
139		154		

NET_TYPE		
SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FW	FW	FW_TPA0_FL
FW	FW	FW_TPA0_FL
FW	FW	FW_TPA0_FL
FW	FW	FW_TPA0_FL
FW	FW	FW_TPA1_FL
FW	FW	FW_TPA1_FL
FW	FW	FW_TPA1_FL
FW	FW	FW_TPA1_FL
FW	FW	FW_TPB0_FL
FW	FW	FW_TPB0_FL
FW	FW	FW_TPB0_FL
FW	FW	FW_TPB0_FL
FW	FW	FW_TPB1_FL
FW	FW	FW_TPB1_FL
FW	FW	FW_TPB1_FL
FW	FW	FW_TPB1_FL



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT	OF	154
NONE	140		

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_2
	USB2	USB2_S	USB2_3
	USB2	USB2_S	USB2_4
	0.38mm SPACING		NEC_CLK30M_XT1
	0.38mm SPACING		NEC_CLK30M_XT2
	0.38mm SPACING		NEC_CLK30M_XT2_R

USB2_P<0>	142 143
USB2_N<0>	142 143
USB2_P<1>	142 143
USB2_N<1>	142 143
USB2_P<2>	142 143
USB2_N<2>	142 143
USB2_P<3>	142 143
USB2_N<3>	142 143
USB2_P<4>	142 143
USB2_N<4>	142 143

Q63 USB PORT ALLOCATION
 REAR USB (PORT #0)
 FRONT PANEL USB (PORT #1)
 REAR USB (PORT #2)
 REAR USB (PORT #3)

Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_USB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

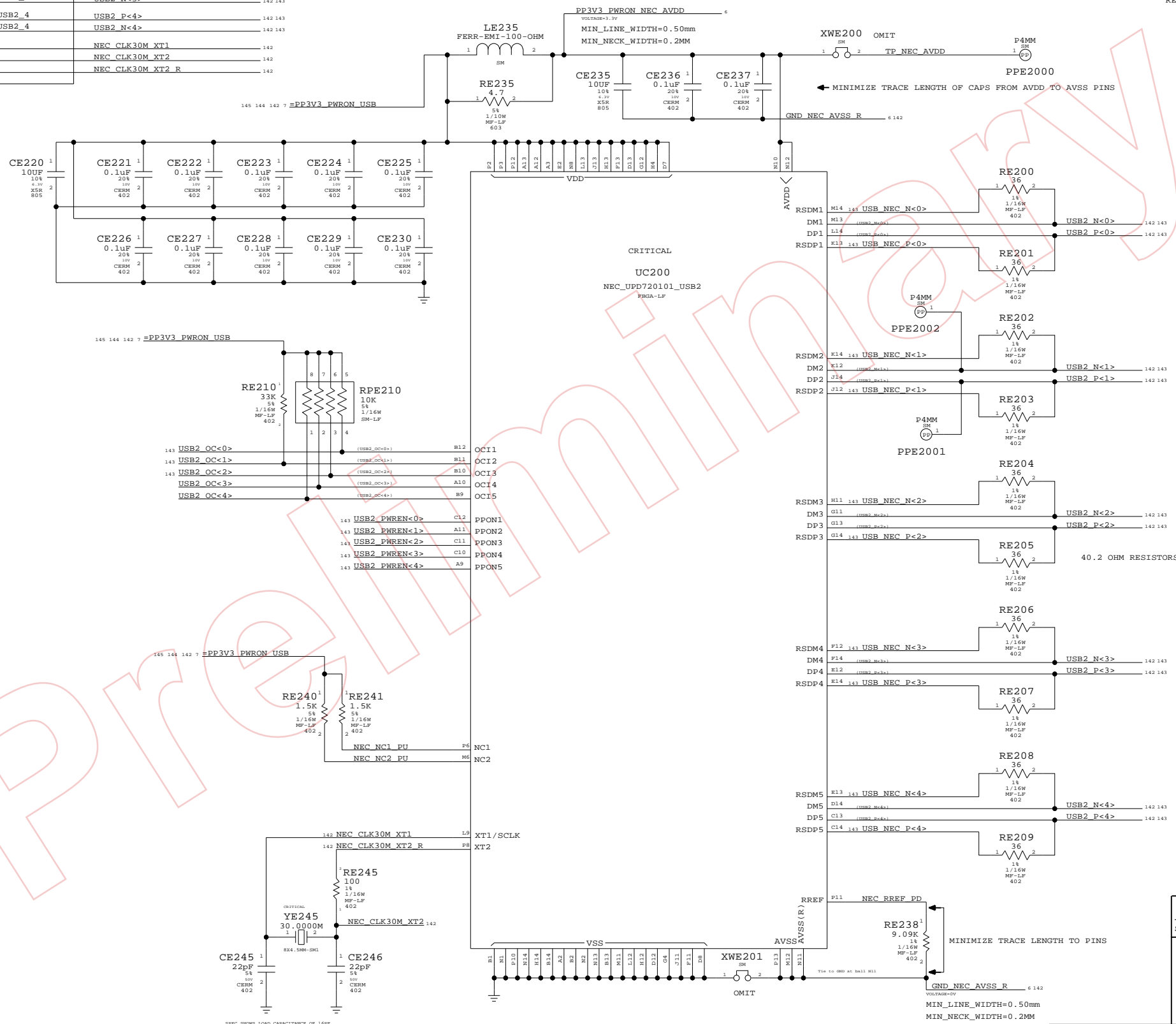
Net Spacing Type: USB2

Line To Line: 0.50mm
 Length Tolerance: 1.27mm
 Primary Max Sep: 0.19mm
 Secondary Max Sep: 2.54mm
 Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300 SHASTA V1.1 BGA-LF (8 OF 8)

NC0	P7	TP_SB<0>	6
NC1	P8	TP_SB<1>	6
NC2	P3	TP_SB<2>	6
NC3	P4	TP_SB<3>	6
NC4	P5	TP_SB<4>	6
NC5	P6	TP_SB<5>	6
NC6	P7	TP_SB<6>	6
NC7	P8	TP_SB<7>	6
NC8	T1	TP_SB<8>	6
NC9	T2	TP_SB<9>	6
NC10	T3	TP_SB<10>	6
NC11	T4	TP_SB<11>	6
NC12	T5	TP_SB<12>	6
NC13	T6	TP_SB<13>	6
NC14	T7	TP_SB<14>	6
NC15	T8	TP_SB<15>	6
NC16	U1	TP_SB<16>	6
NC17	U2	TP_SB<17>	6
NC18	U3	TP_SB<18>	6
NC19	U4	TP_SB<19>	6
NC20	U5	TP_SB<20>	6
NC21	U6	TP_SB<21>	6
NC22	V1	TP_SB<22>	6
NC23	V2	TP_SB<23>	6
NC24	V3	TP_SB<24>	6
NC25	V4	TP_SB<25>	6
NC26	W1	TP_SB<26>	6
NC27	W3	TP_SB<27>	6
NC28	Y1	TP_SB<28>	6
NC29	Y3	TP_SB<29>	6



APPLE COMPUTER INC.

SCALE	SHEET	OF
NONE	142	154

USB Host Interfaces

SYNC_MASTER=FINO-PC SYNC_DATE=07/05/2005

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Page Notes

Power aliases required by this page:

- PP5V_PWRON_USB
- PP5V_PWRON_UDASH
- PP3V3_PWRON_UDASH
- PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

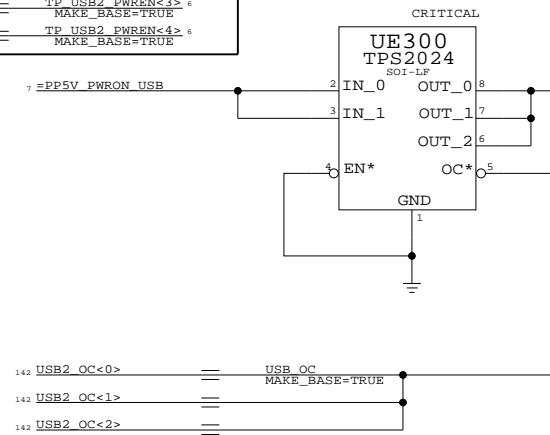
BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

- 142 USB2_PWREN<0> == TP_USB2_PWREN<0> 6 MAKE_BASE=TRUE
- 142 USB2_PWREN<1> == TP_USB2_PWREN<1> 6 MAKE_BASE=TRUE
- 142 USB2_PWREN<2> == TP_USB2_PWREN<2> 6 MAKE_BASE=TRUE
- 142 USB2_PWREN<3> == TP_USB2_PWREN<3> 6 MAKE_BASE=TRUE
- 142 USB2_PWREN<4> == TP_USB2_PWREN<4> 6 MAKE_BASE=TRUE

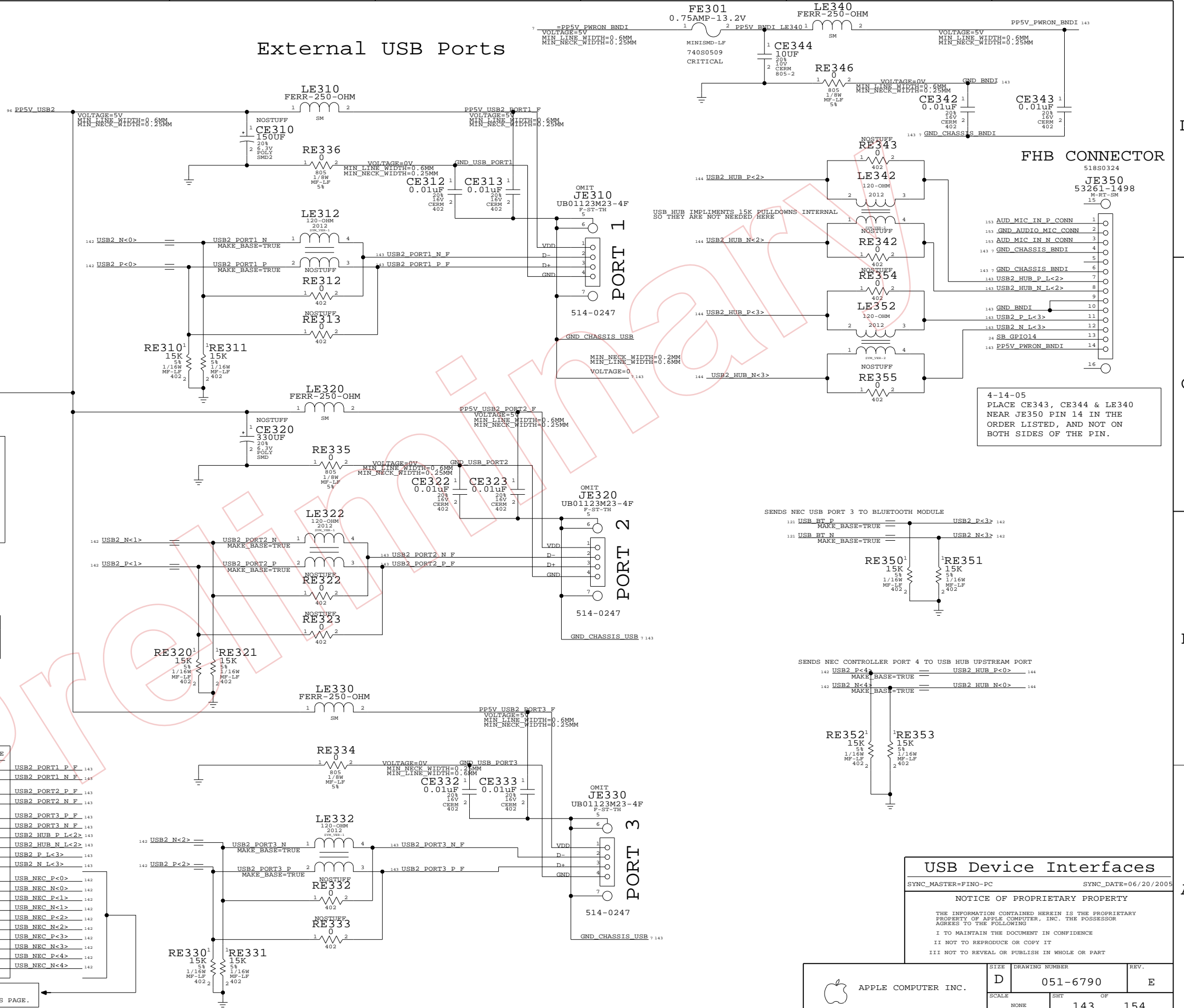


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23B-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33B-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

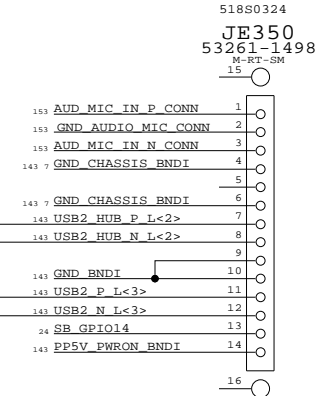
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE
PROVIDED	USB2	USB2_PORT1_P_F	USB2 USB2_PORT1_P_F 143
BY	USB2	USB2_PORT1_F	USB2 USB2_PORT1_N_F 144
USB CONTROLLER	USB2	USB2_PORT2_F	USB2 USB2_PORT2_P_F 143
	USB2	USB2_PORT2_F	USB2 USB2_PORT2_N_F 143
	USB2	USB2_PORT3_F	USB2 USB2_PORT3_P_F 143
	USB2	USB2_PORT3_F	USB2 USB2_PORT3_N_F 143
	USB2	USB2_HUB_F	USB2 USB2_HUB_P_L<2> 143
	USB2	USB2_HUB_F	USB2 USB2_HUB_N_L<2> 143
	USB2	USB2_BNDI_F	USB2 USB2_P_L<3> 143
	USB2	USB2_BNDI_F	USB2 USB2_N_L<3> 143
	USB2	USB2_0_IC	USB2 USB_NEC_P<0> 142
	USB2	USB2_0_IC	USB2 USB_NEC_N<0> 142
	USB2	USB2_1_IC	USB2 USB_NEC_P<1> 142
	USB2	USB2_1_IC	USB2 USB_NEC_N<1> 142
	USB2	USB2_2_IC	USB2 USB_NEC_P<2> 142
	USB2	USB2_2_IC	USB2 USB_NEC_N<2> 142
	USB2	USB2_3_IC	USB2 USB_NEC_P<3> 142
	USB2	USB2_3_IC	USB2 USB_NEC_N<3> 142
	USB2	USB2_4_IC	USB2 USB_NEC_P<4> 142
	USB2	USB2_4_IC	USB2 USB_NEC_N<4> 142

DUE TO THESE NETS ARE ON A Q63 SHARED PAGE 124, THESE PROPERTIES FOR M23/M33 WERE PLACED ON THIS PAGE.

External USB Ports



FHB CONNECTOR



4-14-05
PLACE CE343, CE344 & LE340 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.

USB Device Interfaces

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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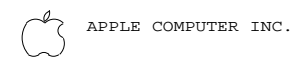
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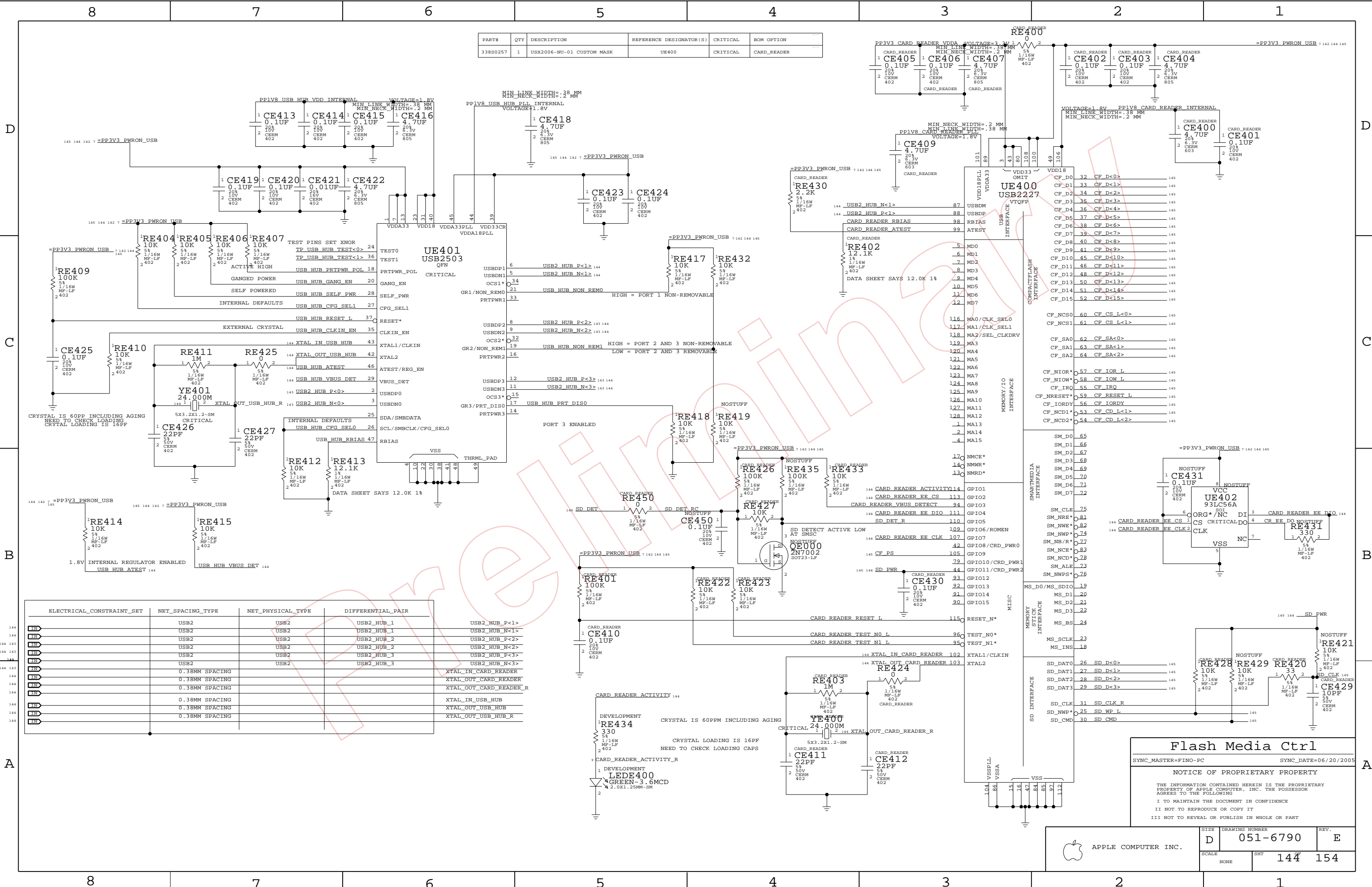
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

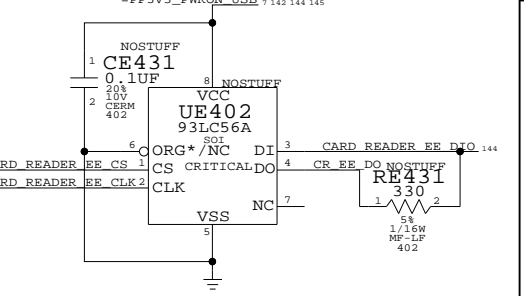
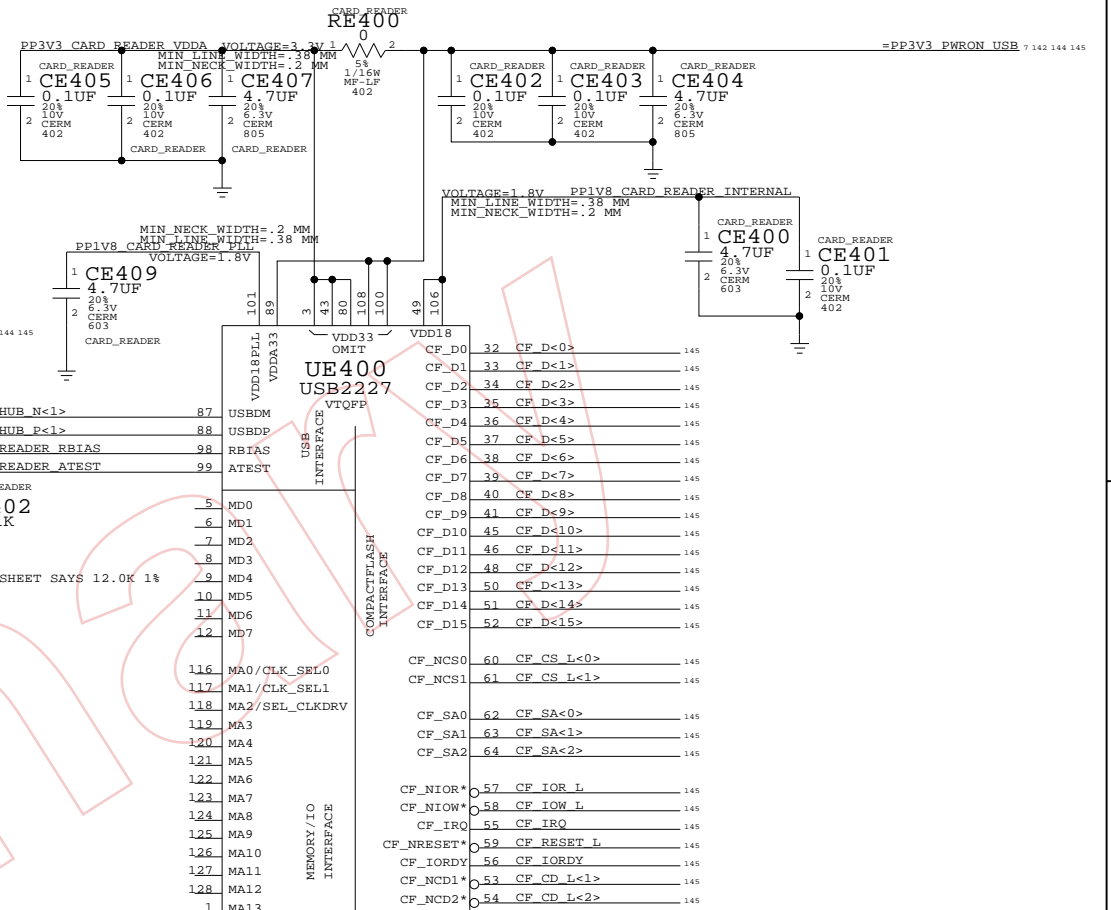
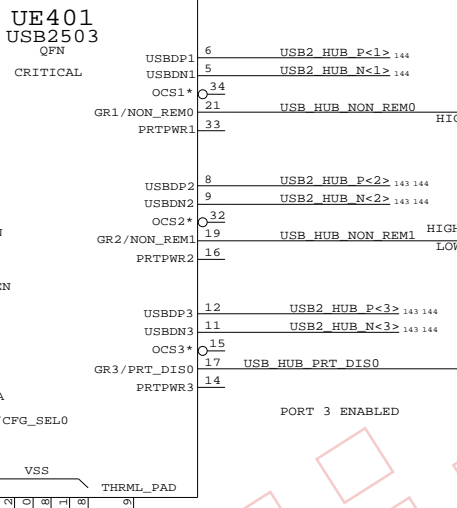
SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHEET	OF
NONE	143	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0257	1	USX2006-NU-01 CUSTOM MASK	UE400	CRITICAL	CARD_READER



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
MIN	USB2	USB2	USB2_HUB_1
MIN	USB2	USB2	USB2_HUB_1
MIN	USB2	USB2	USB2_HUB_2
MIN	USB2	USB2	USB2_HUB_2
MIN	USB2	USB2	USB2_HUB_3
MIN	USB2	USB2	USB2_HUB_3
MIN	0.38MM SPACING		XTAL_IN_CARD_READER
MIN	0.38MM SPACING		XTAL_OUT_CARD_READER
MIN	0.38MM SPACING		XTAL_IN_USB_HUB
MIN	0.38MM SPACING		XTAL_OUT_USB_HUB
MIN	0.38MM SPACING		XTAL_OUT_USB_HUB_R



Flash Media Ctrl

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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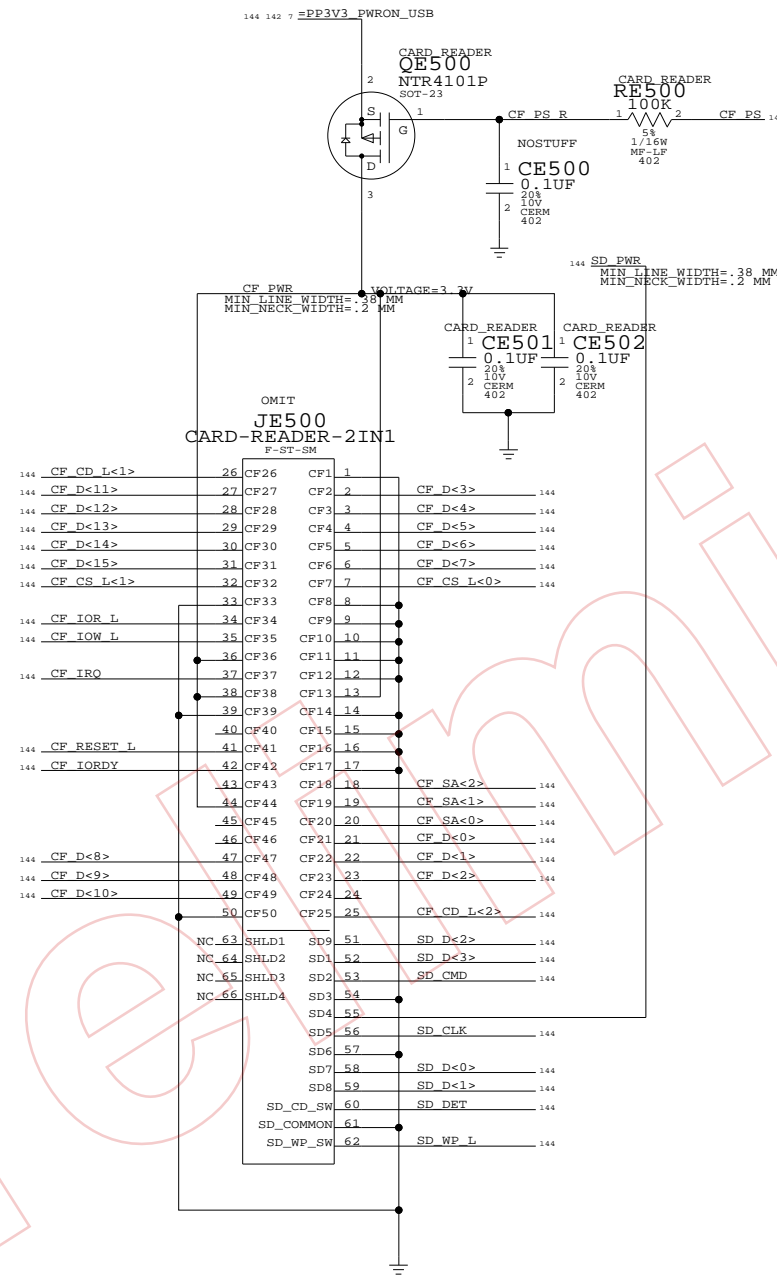
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT	144	154
NONE			

IF USING THE CARD READER, MUST CHANGE THESE BOM OPTIONS TO:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51280010	1	CONN, MEDIA CARD M23	JE500	CRITICAL	CARD_READER 17_INCH_LCD
51280012	1	CONN, MEDIA CARD M33	JE500	CRITICAL	CARD_READER 20_INCH_LCD



WRITE PROTECT AND CARD DETECT SWITCHES

CARD STATUS	WRITE PROTECT	WRITE ENABLE	CARD DETECT
NOT INSERTED	OPEN	OPEN	OPEN
FULLY INSERTED	OPEN	CLOSE	CLOSE

Flash Connector

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

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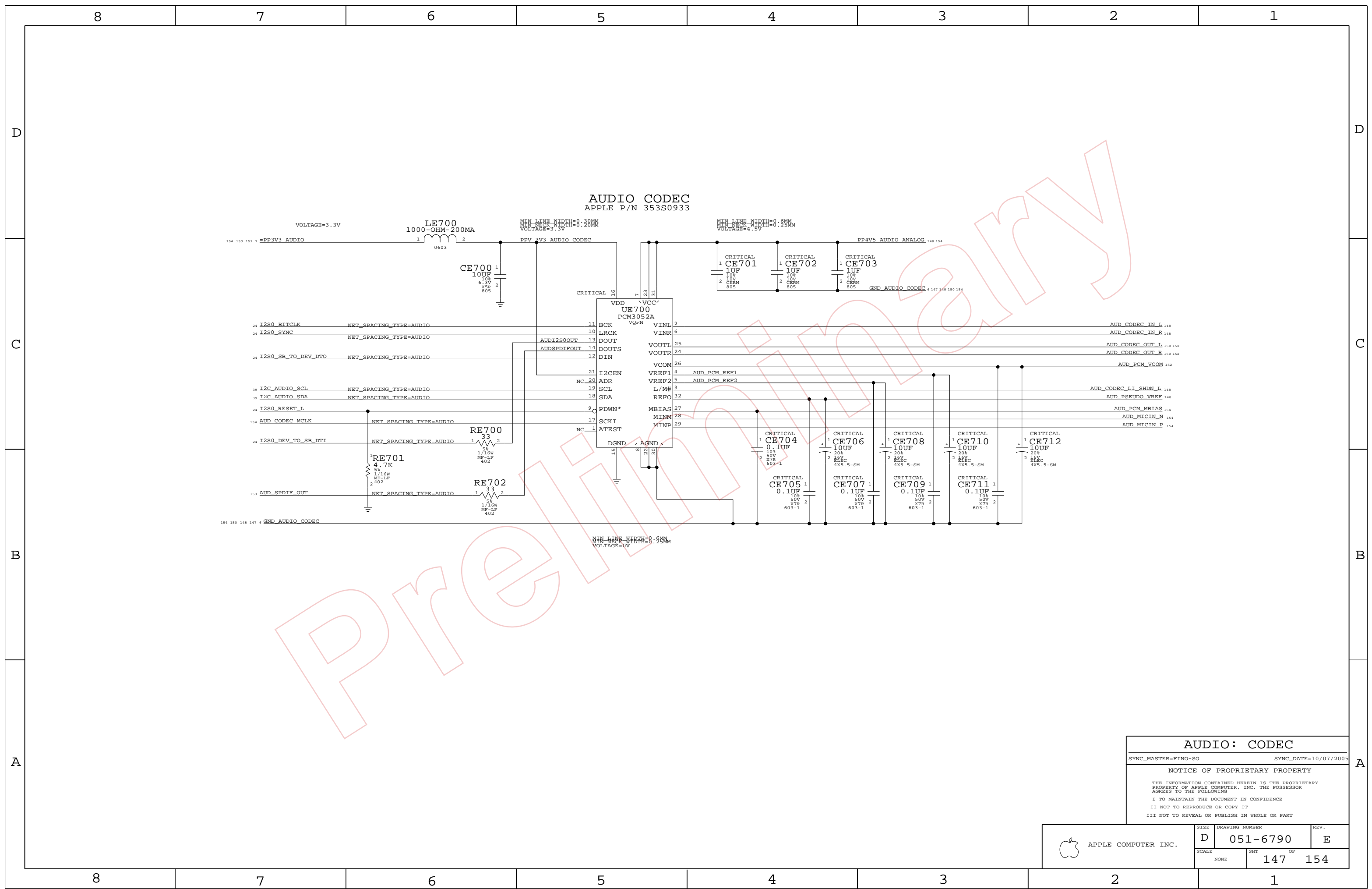
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT	REV.	
NONE	145	154	



AUDIO CODEC
APPLE P/N 353S0933

AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

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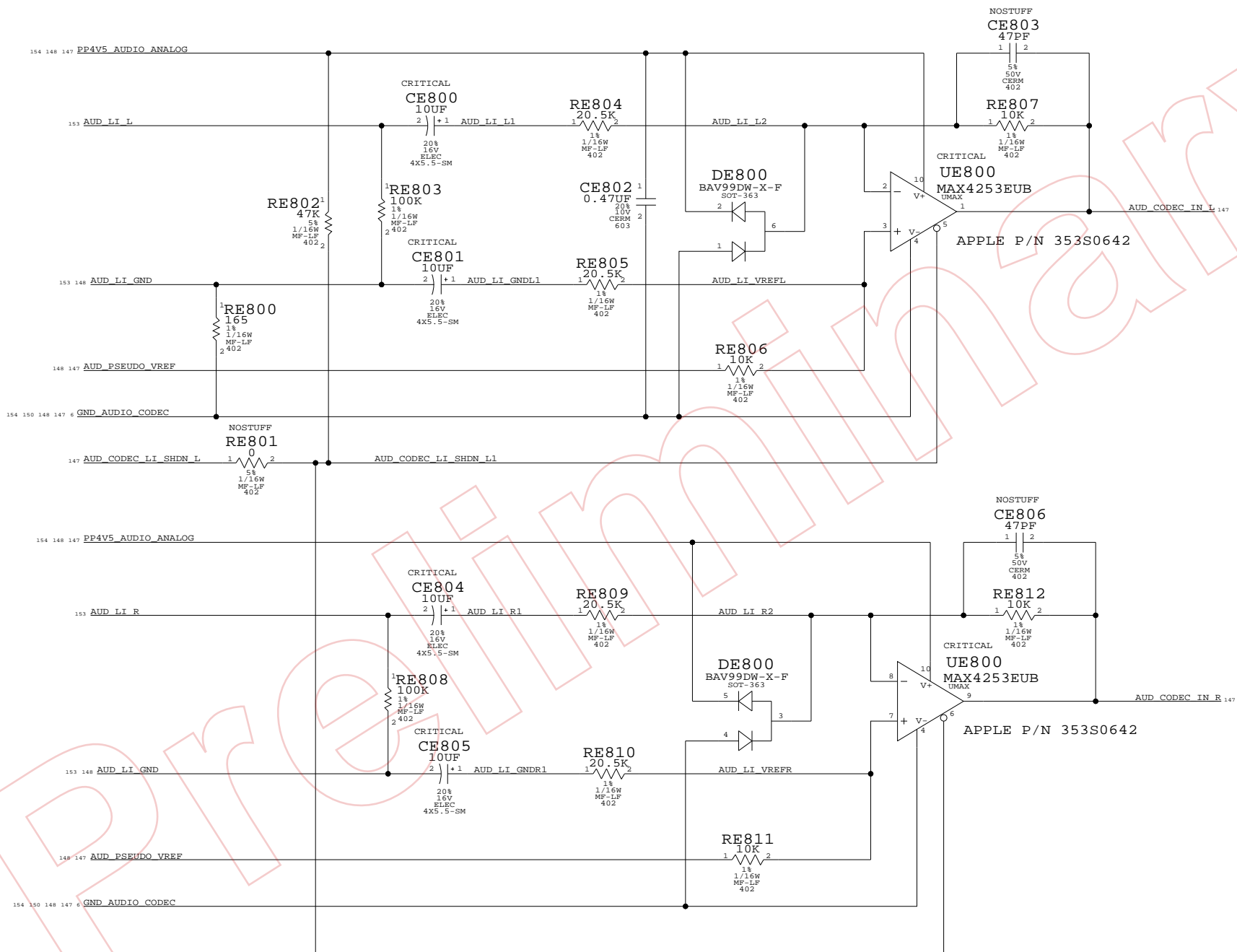
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT OF		
NONE	147 OF 154		

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49




AUDIO: LINE INPUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

NOTICE OF PROPRIETARY PROPERTY

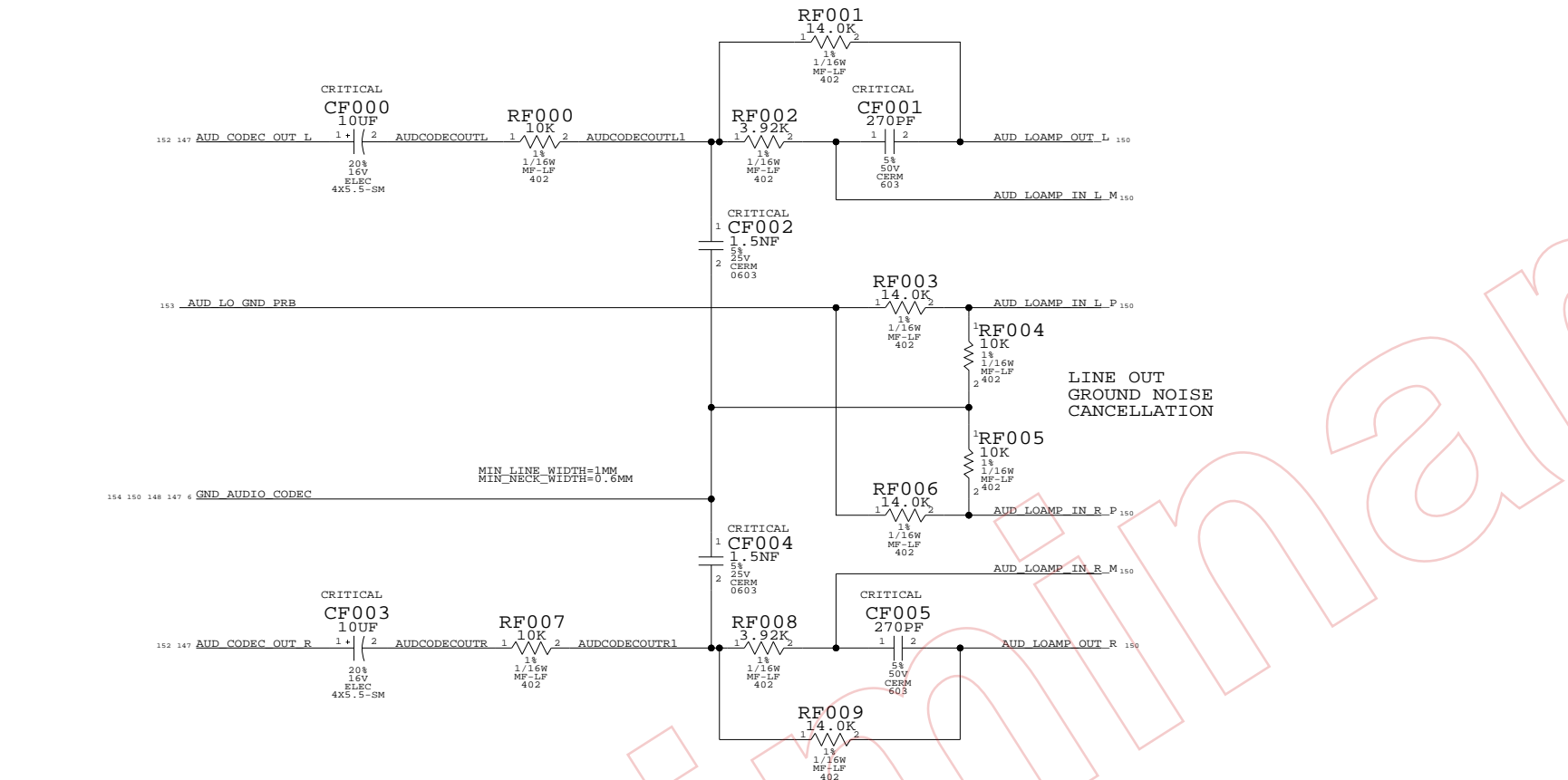
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	NONE	SHT OF	148 154

LINE OUT LOW-PASS FILTER

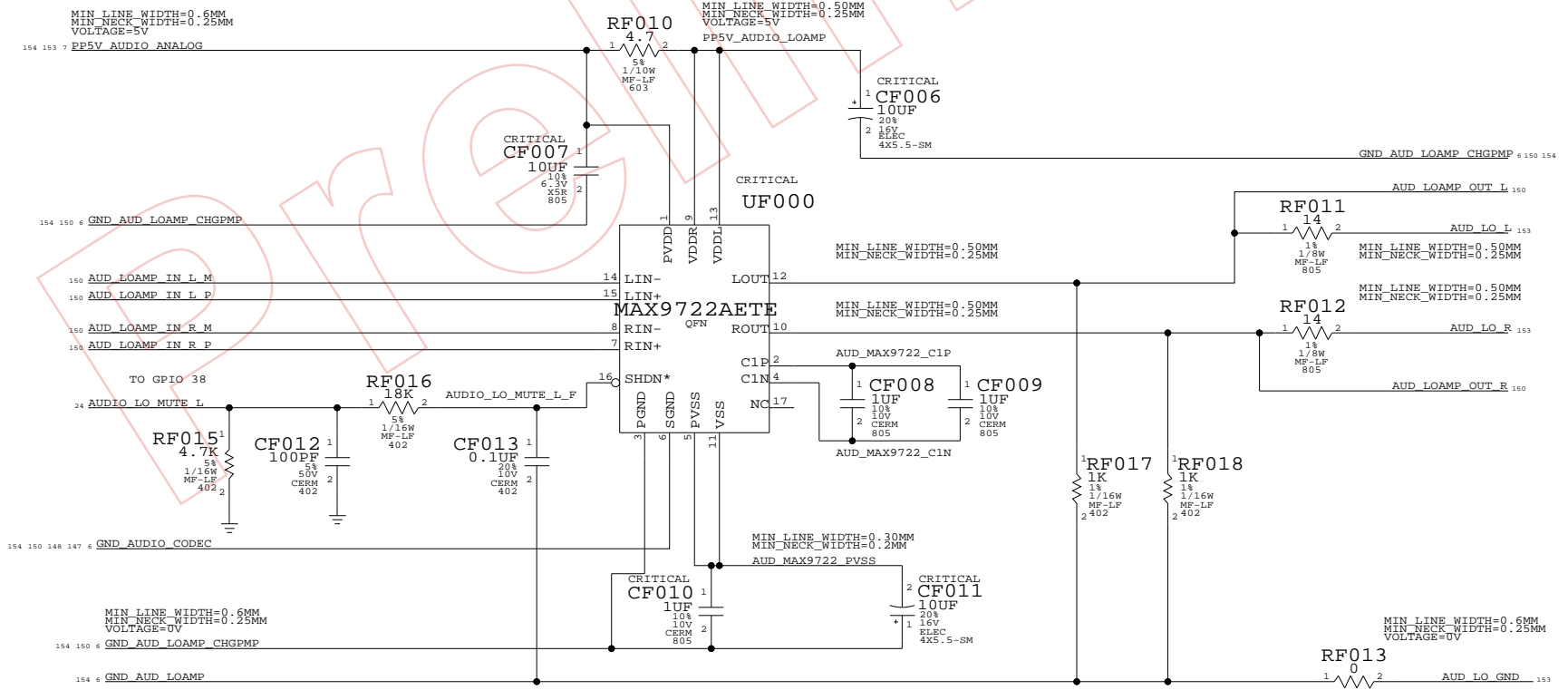
FC = 37 KHZ, HO = -1.4



LINE OUT
GROUND NOISE
CANCELLATION

LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

NOTICE OF PROPRIETARY PROPERTY

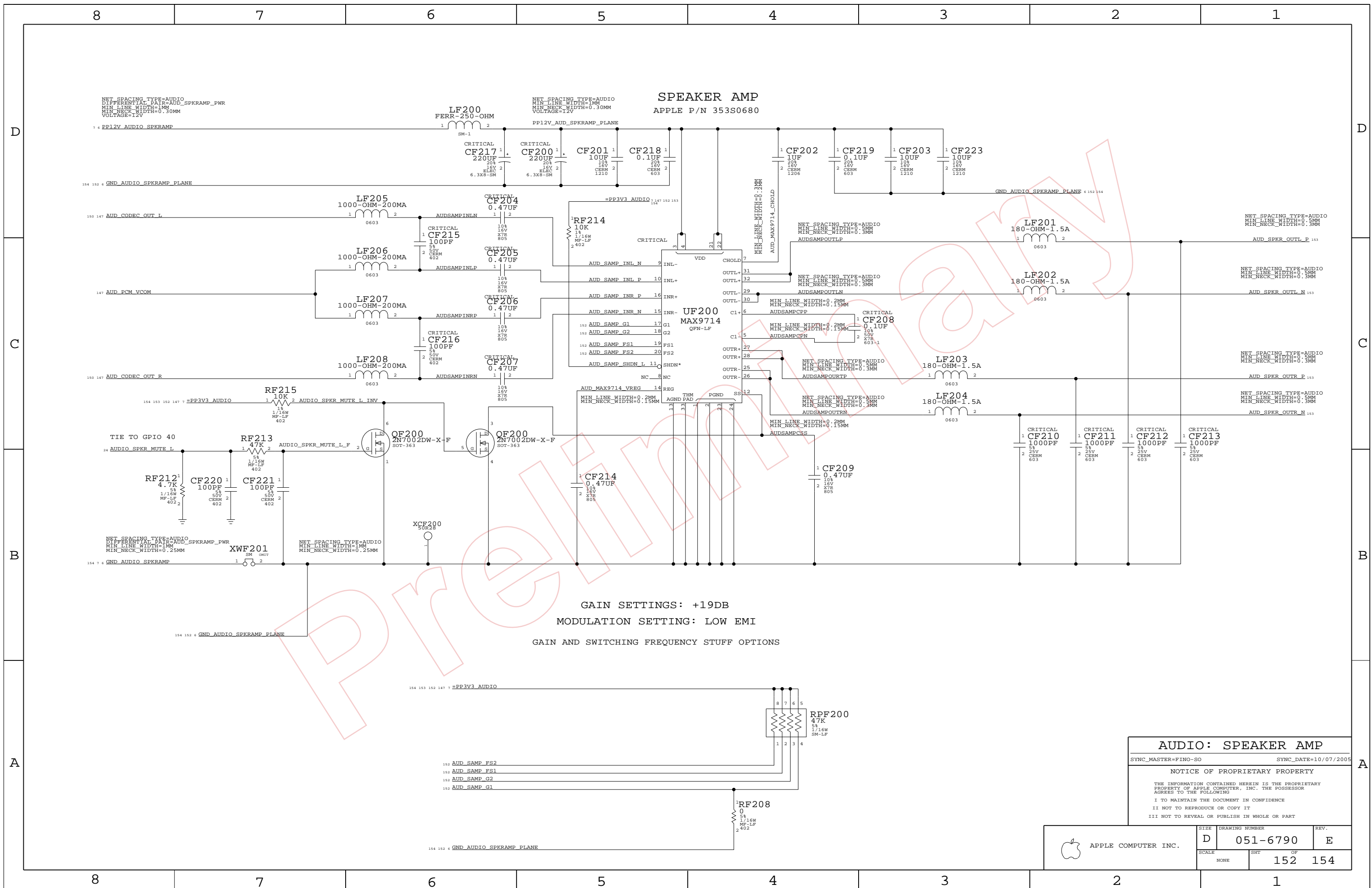
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SCALE	NONE	SHT	OF
		150	154

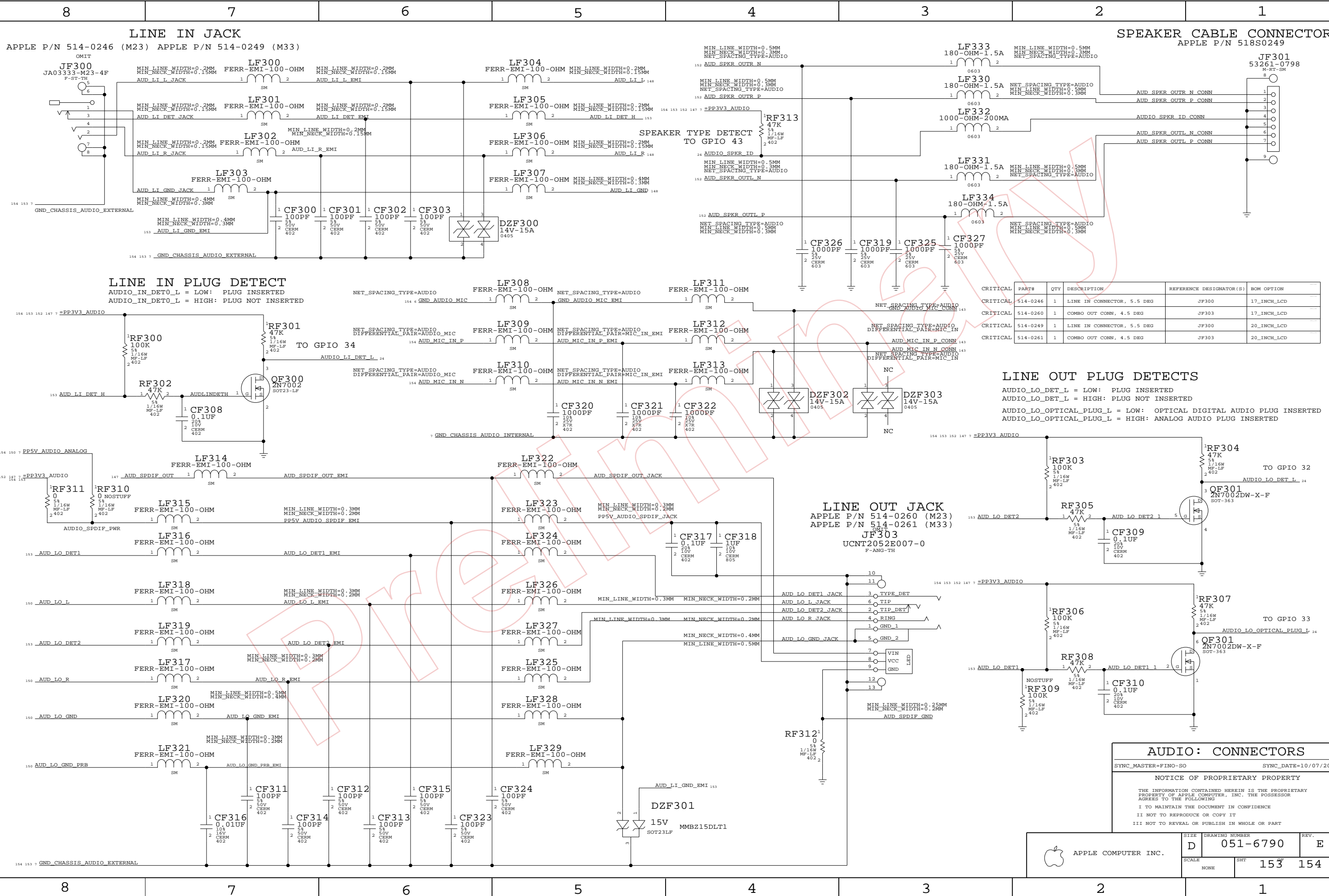


SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

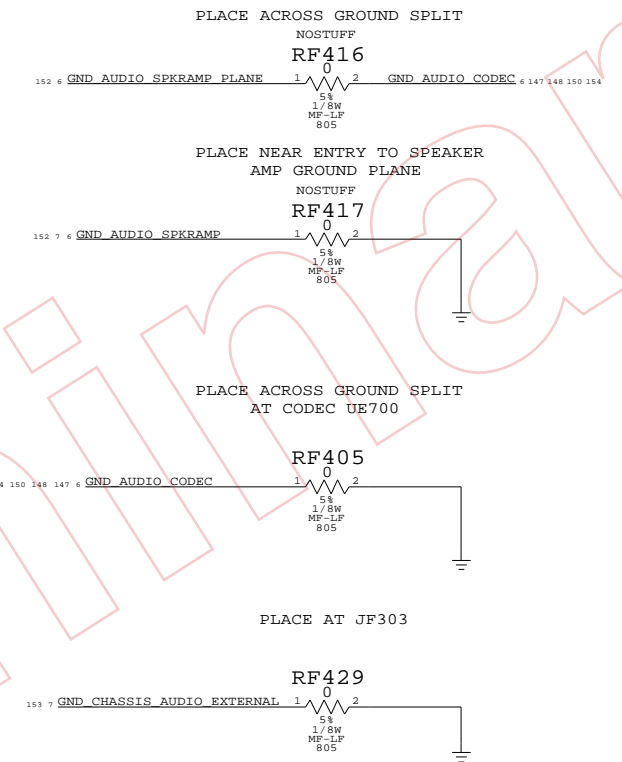
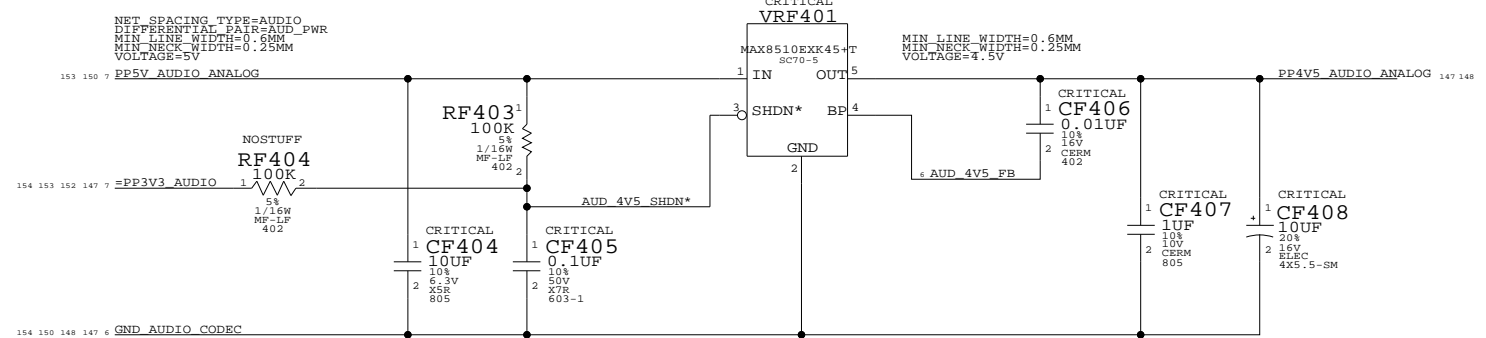
AUDIO: SPEAKER AMP
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005
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	D	051-6790	E
SCALE	NONE	SHT	OF
		152	154



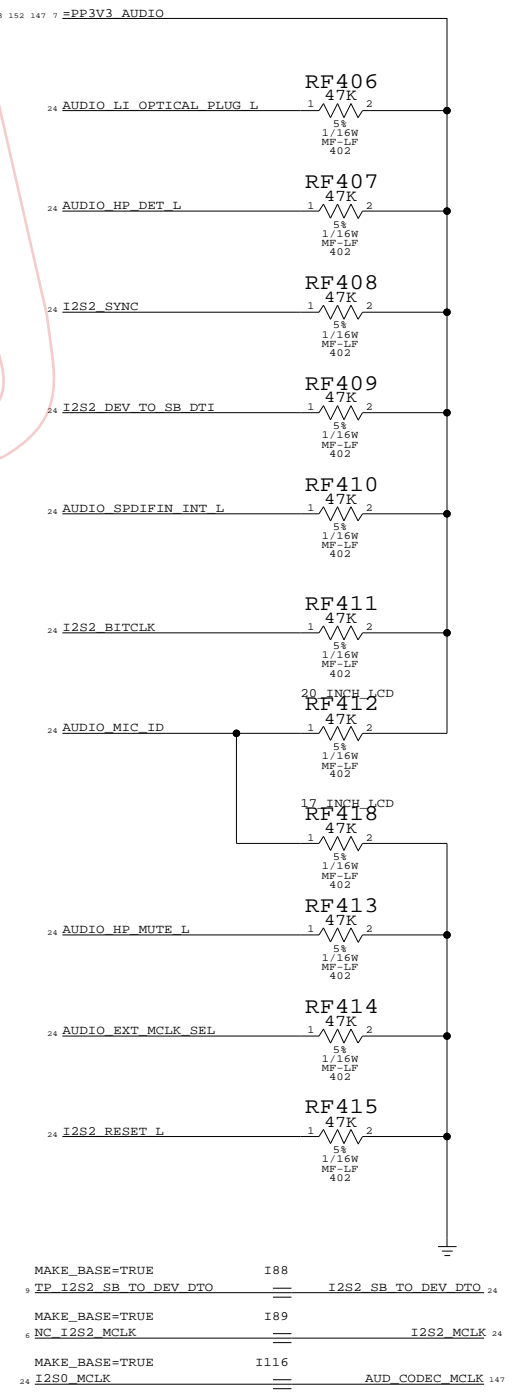
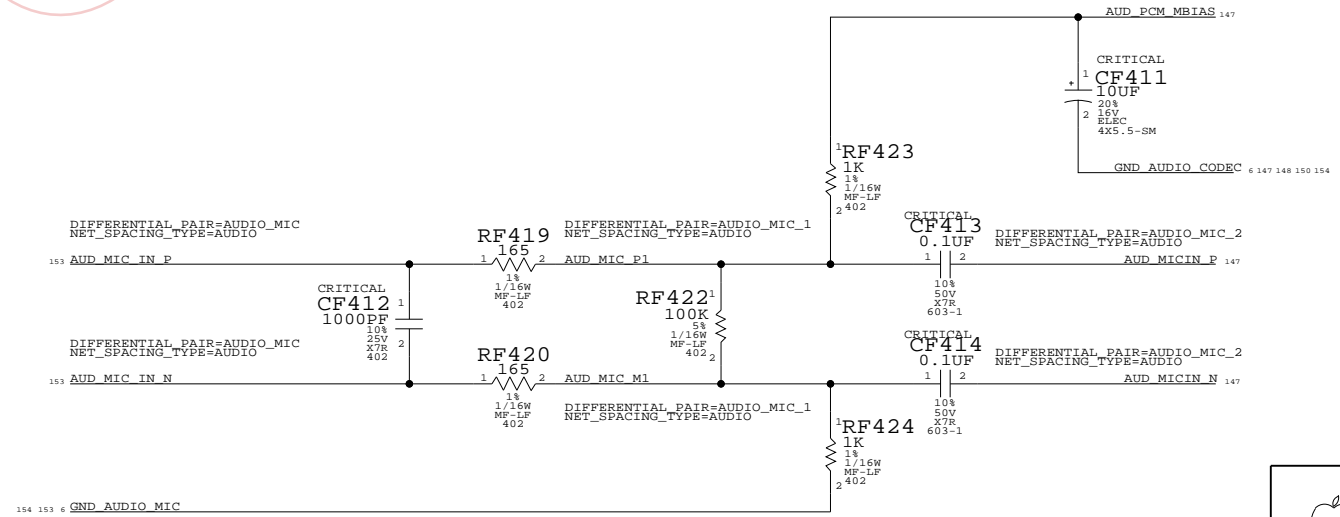
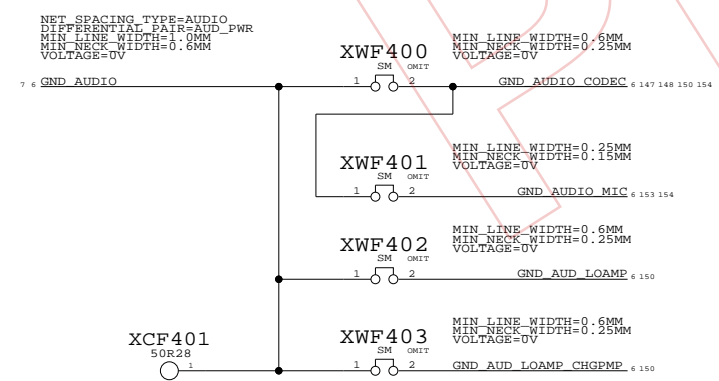
UNUSED GPIO TERMINATIONS

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APPLE P/N 353S0733



MICROPHONE IMPEDANCE MATCHING CIRCUIT

AUDIO GROUND RETURNS



AUDIO: POWER SUPPLIES

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	D	051-6790	E
SCALE	NONE	SHT OF	154 OF 154