Data Sheet, V1.2, May 2002

TC1775

32-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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TC1775 Data Sheet
Preliminary
Revision History: 2002-05 V1.2

Previous Versions: V1.1, 2001-08; V1.0, 2001-08;

Page	Subjects (major changes since last revision)
Changes from V1.1, 2001-08 to V1.2, 2002-05	
–	Status of data sheet changed from “Advance Information” into “Preliminary”
36	ADC features: example of 10-bit ADC conversion time added
54	Note below Figure 16 added
59	Column “Jitter” in Table 8 removed; the jitter is now defined in “PLL Parameters” on Page 82 and Figure 31; 2nd footnote for Table 8 added
60	Note on bottom extended “… specified by the crystal suppliers:”
66	Section “Package Parameters” added
68, 69, 70	Definition and values for pull-up/pull-down currents changed
71	Curves for pull-up/pull-down characteristics added
73	Formulas for conversion time t_C corrected; f_{ANA} min./max. specification added
73	Definition of I_{AOV} and k_A improved
76	Note 1) for I_{OZ} added
77	I_{DD} max corrected; I_{DD} active for V_{DDSB} added; note for I_{ID} and I_{SL} added
78	t_{RFAnom} (typ.) added
80	Figure 29 corrected
81	Figure 30 corrected
82, 83	PLL specification and parameters completed
84, 87, 89, 92, 94, 95	Several AC timing parameter values added or corrected: t_{10}, t_{11}, t_{15}, t_{20}, t_{21}, t_{25}, t_{45}, t_{46}, t_{47}, t_{55}, t_{61}, t_{62}
95	Definition of t_{61} and t_{62} changed
several	Formal changes
Changes from V1.0, 2001-08 to V1.1, 2001-08	
84	Reference for t_{31} and t_{32} to Page 90 added
89	t_{50} and t_{51} changed into TBD; note changed into “Will be guaranteed …”
90	t_{31} and t_{32} (Data setup/hold to CLKIN ↓ in burst mode timing) changed; note 1) added
95	t_{61} and t_{62} changed into TBD; note changed into “Will be guaranteed …”

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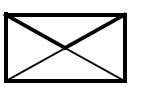

Preliminary

32-Bit Single-Chip Microcontroller TC1775
TriCore Family

- High Performance 32-bit TriCore CPU with 4-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock
- Dual Issue super-scalar implementation
  - Instruction triple issue
- Circular Buffer and bit-reverse addressing modes for DSP algorithms
- Flexible multi-master interrupt system
- Very fast interrupt response time
- Hardware controlled context switch for task switch and interrupts
- 72 Kbytes of on-chip SRAM for data and time critical code
- Independent Peripheral Control Processor (PCP) for low level driver support with 20 Kbytes code/parameter memory
- Built-in calibration support
- On-chip Flexible Peripheral Interface Bus (FPI Bus) for interconnections of functional units
- Flexible External Bus Interface Unit (EBU) used for
  - Communication with external data memories and peripheral units
  - Instruction fetches from external Burst Flash program memories
- On-Chip Peripheral Units
  - General Purpose Timer Array (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex I/O management
  - Multifunctional General Purpose Timer Unit (GPTU) with three 32-bit timer/counters
  - Two Asynchronous/Synchronous Serial Channels (ASC0, ASC1) with baud rate generator, parity, framing and overrun error detection
  - Two High Speed Synchronous Serial Channels (SSC0, SSC1) with programmable data length and shift direction
  - TwinCAN module with two interconnected CAN nodes for high efficiency data handling via FIFO buffering and gateway data transfer
  - Serial Data Link module (SDLM) compliant to SAE Class B J1850 specification
  - Two Analog-to-Digital Converter Units (ADC0, ADC1) with 8-bit, 10-bit, or 12-bit resolution and 16 analog inputs each
  - Watchdog Timer and System Timer
  - Real Time Clock
- Eleven 16-bit digital I/O ports and two 16-bit analog ports
- On-chip Debug Support
- Power Management System
- Clock Generation Unit with PLL
- Ambient temperature under bias: -40 °C to +125 °C
- P-BGA-329 package

Preliminary

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies: the derivative itself, i.e. its function set, the temperature range, and the package and the type of delivery.

The TC1775 is available with the following ordering code:

Type	Ordering Code	Package	Description
SAK-TC1775-L40E	Q67121-C2285-A701	P-BGA-329	32-Bit Single-Chip Microcontroller 40 MHz -40 °C to +125 °C

Preliminary

Block Diagram

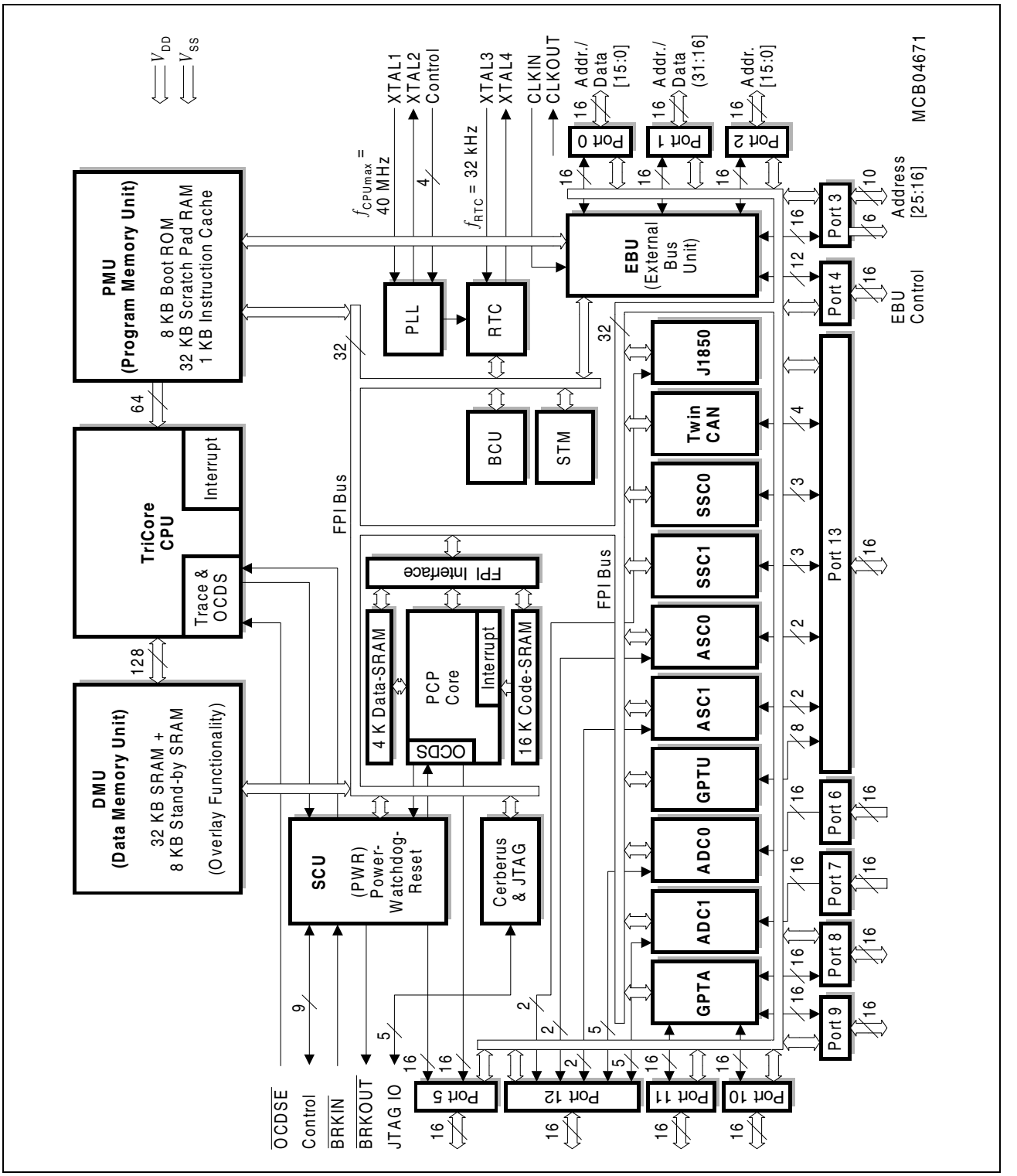

Figure 1 TC1775 Block Diagram

Preliminary

Logic Symbol

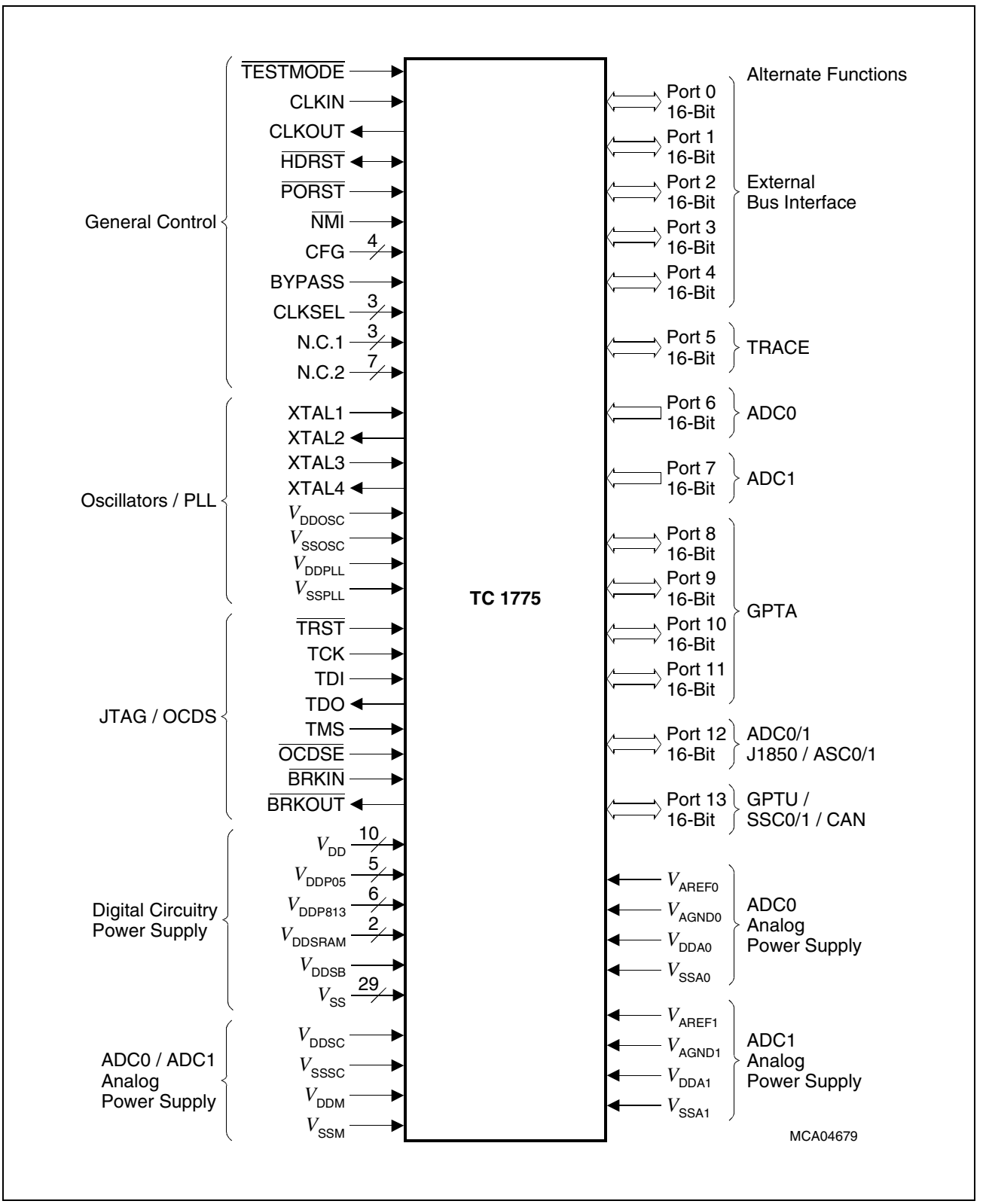

Figure 2 TC1775 Logic Symbol

Preliminary

Pin Configuration

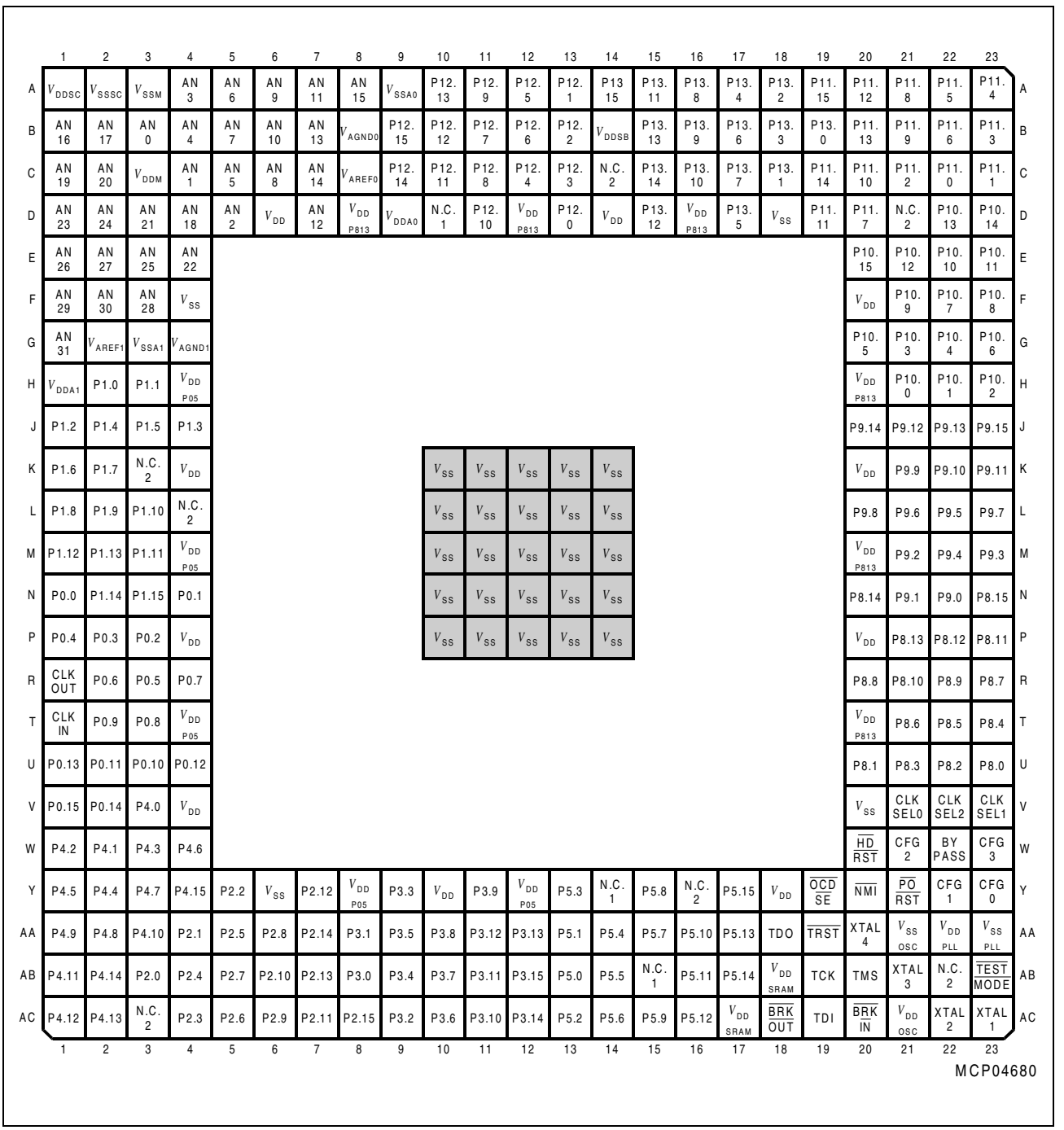

Figure 3 TC1775 Pinning: P-BGA-329 Package (top view)

Table 1 Pin Definitions and Functions

Symbol	Pin	In Out	Functions
P0		I/O	**Port 0** Port 0 serves as 16-bit general purpose I/O port or as lower external address/data bus AD[15:0] (multiplexed bus mode) or data bus D[15:0] (demultiplexed bus mode) for the EBU. Port 0 is used as data input by an external bus master when accessing modules on the internal FPI Bus.
P0.0	N1	I/O	AD0 / D0 Address/data bus line 0 / Data bus line 0
P0.1	N4	I/O	AD1 / D1 Address/data bus line 1 / Data bus line 1
P0.2	P3	I/O	AD2 / D2 Address/data bus line 2 / Data bus line 2
P0.3	P2	I/O	AD3 / D3 Address/data bus line 3 / Data bus line 3
P0.4	P1	I/O	AD4 / D4 Address/data bus line 4 / Data bus line 4
P0.5	R3	I/O	AD5 / D5 Address/data bus line 5 / Data bus line 5
P0.6	R2	I/O	AD6 / D6 Address/data bus line 6 / Data bus line 6
P0.7	R4	I/O	AD7 / D7 Address/data bus line 7 / Data bus line 7
P0.8	T3	I/O	AD8 / D8 Address/data bus line 8 / Data bus line 8
P0.9	T2	I/O	AD9 / D9 Address/data bus line 9 / Data bus line 9
P0.10	U3	I/O	AD10 / D10 Address/data bus line 10 / Data bus line 10
P0.11	U2	I/O	AD11 / D11 Address/data bus line 11 / Data bus line 11
P0.12	U4	I/O	AD12 / D12 Address/data bus line 12 / Data bus line 12
P0.13	U1	I/O	AD13 / D13 Address/data bus line 13 / Data bus line 13
P0.14	V2	I/O	AD14 / D14 Address/data bus line 14 / Data bus line 14
P0.15	V1	I/O	AD15 / D15 Address/data bus line 15 / Data bus line 15

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P1		I/O	**Port 1** Port 1 serves as 16-bit general purpose I/O port or as upper external address/data bus AD[31:16] (multiplexed bus mode) or data bus D[31:16] (demultiplexed bus mode) for the EBU. Port 1 is used as data input by an external bus master when accessing modules on the internal FPI Bus.
P1.0	H2	I/O	AD16 / D16 Address/data bus line 16 / Data bus line 16
P1.1	H3	I/O	AD17 / D17 Address/data bus line 17/ Data bus line 17
P1.2	J1	I/O	AD18 / D18 Address/data bus line 18 / Data bus line 18
P1.3	J4	I/O	AD19 / D19 Address/data bus line 19 / Data bus line 19
P1.4	J2	I/O	AD20 / D20 Address/data bus line 20 / Data bus line 20
P1.5	J3	I/O	AD21 / D21 Address/data bus line 21 / Data bus line 21
P1.6	K1	I/O	AD22 / D22 Address/data bus line 22 / Data bus line 22
P1.7	K2	I/O	AD23 / D23 Address/data bus line 23 / Data bus line 23
P1.8	L1	I/O	AD24 / D24 Address/data bus line 24 / Data bus line 24
P1.9	L2	I/O	AD25 / D25 Address/data bus line 25 / Data bus line 25
P1.10	L3	I/O	AD26 / D26 Address/data bus line 26 / Data bus line 26
P1.11	M3	I/O	AD27 / D27 Address/data bus line 27 / Data bus line 27
P1.12	M1	I/O	AD28 / D28 Address/data bus line 28 / Data bus line 28
P1.13	M2	I/O	AD29 / D29 Address/data bus line 29 / Data bus line 29
P1.14	N2	I/O	AD30 / D30 Address/data bus line 30 / Data bus line 30
P1.15	N3	I/O	AD31 / D31 Address/data bus line 31 / Data bus line 31

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P2		I/O	**Port 2** Port 2 serves as 16-bit general purpose I/O port or as lower external address bus for the EBU. When used as address bus, it outputs the addresses A[15:0] of an external access in demultiplexed bus mode. Port 2 is used as address input by an external bus master when accessing modules on the internal FPI Bus.	
P2.0	AB3	I/O	A0	Address bus line 0
P2.1	AA4	I/O	A1	Address bus line 1
P2.2	Y5	I/O	A2	Address bus line 2
P2.3	AC4	I/O	A3	Address bus line 3
P2.4	AB4	I/O	A4	Address bus line 4
P2.5	AA5	I/O	A5	Address bus line 5
P2.6	AC5	I/O	A6	Address bus line 6
P2.7	AB5	I/O	A7	Address bus line 7
P2.8	AA6	I/O	A8	Address bus line 8
P2.9	AC6	I/O	A9	Address bus line 9
P2.10	AB6	I/O	A10	Address bus line 10
P2.11	AC7	I/O	A11	Address bus line 11
P2.12	Y7	I/O	A12	Address bus line 12
P2.13	AB7	I/O	A13	Address bus line 13
P2.14	AA7	I/O	A14	Address bus line 14
P2.15	AC8	I/O	A15	Address bus line 15

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P3		I/O	**Port 3** Port 3 serves as 16-bit general purpose I/O port or as upper external address bus for the EBU. When used as address bus, it outputs the addresses A[25:16] of an external access in demultiplexed bus mode. P3[9:0] is used as address input by an external bus master when accessing modules on the internal FPI Bus. Port 3 also provides chip select output lines $\overline{CS0}$ - $\overline{CS3}$, $\overline{CSEMU}$, and $\overline{CSOVL}$.	
P3.0	AB8	I/O	A16	Address bus line 16
P3.1	AA8	I/O	A17	Address bus line 17
P3.2	AC9	I/O	A18	Address bus line 18
P3.3	Y9	I/O	A19	Address bus line 19
P3.4	AB9	I/O	A20	Address bus line 20
P3.5	AA9	I/O	A21	Address bus line 21
P3.6	AC10	I/O	A22	Address bus line 22
P3.7	AB10	I/O	A23	Address bus line 23
P3.8	AA10	I/O	A24	Address bus line 24
P3.9	Y11	I/O	A25	Address bus line 25
P3.10[1)]	AC11	O	$\overline{CS3}$	Chip select output line 3
P3.11[1)]	AB11	O	$\overline{CS2}$	Chip select output line 2
P3.12[1)]	AA11	O	$\overline{CS1}$	Chip select output line 1
P3.13[1)]	AA12	O	$\overline{CS0}$	Chip select output line 0
P3.14[1)]	AC12	O	$\overline{CSEMU}$	Chip select output for emulator region
P3.15[1)]	AB12	O	$\overline{CSOVL}$	Chip select output for emulator overlay memory

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P4		I/O	**Port 4** Port 4 is used as general purpose I/O port but also serves as control bus for the EBU control lines.
P4.0[1)]	V3	I/O	$\overline{RD}$ Read control line
P4.1[1)]	W2	I/O	RD/$\overline{WR}$ Write control line
P4.2[2)]	W1	O	ALE Address latch enable output
P4.3[1)]	W3	O	$\overline{ADV}$ Address valid output
P4.4[1)]	Y2	I/O	$\overline{BC0}$ Byte control line 0
P4.5[1)]	Y1	I/O	$\overline{BC1}$ Byte control line 1
P4.6[1)]	W4	I/O	$\overline{BC2}$ Byte control line 2
P4.7[1)]	Y3	I/O	$\overline{BC3}$ Byte control line 3
P4.8[1)]	AA2	I	$\overline{WAIT}$/$\overline{IND}$ Wait input / End of burst input
P4.9[1)]	AA1	O	$\overline{BAA}$ Burst address advance output
P4.10[1)]	AA3	I	$\overline{CSFPI}$ Chip select FPI input
P4.11[1)]	AB1	I	$\overline{HOLD}$ Hold request input
P4.12[1)]	AC1	I/O	$\overline{HLDA}$ Hold acknowledge input/output
P4.13[1)]	AC2	O	$\overline{BREQ}$ Bus request output
P4.14[1)]	AB2	O	$\overline{CODE}$ Code fetch status output
P4.15[1)]	Y4	I/O	SVM Supervisor mode input/output The $\overline{CODE}$ signal has the same timing as the $\overline{CSx}$ signals which are located at Port 3.

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P5		I/O	**Port 5** Port 5 serves as 16-bit general purpose I/O port or as CPU or PCP trace output port for the OCDS logic.	
P5.0	AB13	O	TRACE0	CPU or PCP trace output 0
P5.1	AA13	O	TRACE1	CPU or PCP trace output 1
P5.2	AC13	O	TRACE2	CPU or PCP trace output 2
P5.3	Y13	O	TRACE3	CPU or PCP trace output 3
P5.4	AA14	O	TRACE4	CPU or PCP trace output 4
P5.5	AB14	O	TRACE5	CPU or PCP trace output 5
P5.6	AC14	O	TRACE6	CPU or PCP trace output 6
P5.7	AA15	O	TRACE7	CPU or PCP trace output 7
P5.8	Y15	O	TRACE8	CPU or PCP trace output 8
P5.9	AC15	O	TRACE9	CPU or PCP trace output 9
P5.10	AA16	O	TRACE10	CPU or PCP trace output 10
P5.11	AB16	O	TRACE11	CPU or PCP trace output 11
P5.12	AC16	O	TRACE12	CPU or PCP trace output 12
P5.13	AA17	O	TRACE13	CPU or PCP trace output 13
P5.14	AB17	O	TRACE14	CPU or PCP trace output 14
P5.15	Y17	O	TRACE15	CPU or PCP trace output 15

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P6		I	**Port 6** Port 6 provides the analog input lines for the AD Converter 0 (ADC0).	
P6.0	B3	I	AN0	Analog input 0 / V_{AREF}[1] input for ADC0
P6.1	C4	I	AN1	Analog input 1 / V_{AREF}[2] input for ADC0
P6.2	D5	I	AN2	Analog input 2 / V_{AREF}[3] input for ADC0
P6.3	A4	I	AN3	Analog input 3
P6.4	B4	I	AN4	Analog input 4
P6.5	C5	I	AN5	Analog input 5
P6.6	A5	I	AN6	Analog input 6
P6.7	B5	I	AN7	Analog input 7
P6.8	C6	I	AN8	Analog input 8
P6.9	A6	I	AN9	Analog input 9
P6.10	B6	I	AN10	Analog input 10
P6.11	A7	I	AN11	Analog input 11
P6.12	D7	I	AN12	Analog input 12
P6.13	B7	I	AN13	Analog input 13
P6.14	C7	I	AN14	Analog input 14
P6.15	A8	I	AN15	Analog input 15
P7		I	**Port 7** Port 7 provides the analog input lines for the AD Converter 1 (ADC1).	
P7.0	B1	I	AN16	Analog input 16 / V_{AREF}[1] input for ADC1
P7.1	B2	I	AN17	Analog input 17 / V_{AREF}[2] input for ADC1
P7.2	D4	I	AN18	Analog input 18 / V_{AREF}[3] input for ADC1
P7.3	C1	I	AN19	Analog input 19
P7.4	C2	I	AN20	Analog input 20
P7.5	D3	I	AN21	Analog input 21
P7.6	E4	I	AN22	Analog input 22
P7.7	D1	I	AN23	Analog input 23
P7.8	D2	I	AN24	Analog input 24
P7.9	E3	I	AN25	Analog input 25
P7.10	E1	I	AN26	Analog input 26
P7.11	E2	I	AN27	Analog input 27
P7.12	F3	I	AN28	Analog input 28
P7.13	F1	I	AN29	Analog input 29
P7.14	F2	I	AN30	Analog input 30
P7.15	G1	I	AN31	Analog input 31

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P8		I/O	**Port 8** Port 8 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P8.0	U23	I/O	IN0 / OUT0 line of GPTA
P8.1	U20	I/O	IN1 / OUT1 line of GPTA
P8.2	U22	I/O	IN2 / OUT2 line of GPTA
P8.3	U21	I/O	IN3 / OUT3 line of GPTA
P8.4	T23	I/O	IN4 / OUT4 line of GPTA
P8.5	T22	I/O	IN5 / OUT5 line of GPTA
P8.6	T21	I/O	IN6 / OUT6 line of GPTA
P8.7	R23	I/O	IN7 / OUT7 line of GPTA
P8.8	R20	I/O	IN8 / OUT8 line of GPTA
P8.9	R22	I/O	IN9 / OUT9 line of GPTA
P8.10	R21	I/O	IN10 / OUT10 line of GPTA
P8.11	P23	I/O	IN11 / OUT11 line of GPTA
P8.12	P22	I/O	IN12 / OUT12 line of GPTA
P8.13	P21	I/O	IN13 / OUT13 line of GPTA
P8.14	N20	I/O	IN14 / OUT14 line of GPTA
P8.15	N23	I/O	IN15 / OUT15 line of GPTA
P9		I/O	**Port 9** Port 9 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P9.0	N22	I/O	IN16 / OUT16 line of GPTA
P9.1	N21	I/O	IN17 / OUT17 line of GPTA
P9.2	M21	I/O	IN18 / OUT18 line of GPTA
P9.3	M23	I/O	IN19 / OUT19 line of GPTA
P9.4	M22	I/O	IN20 / OUT20 line of GPTA
P9.5	L22	I/O	IN21 / OUT21 line of GPTA
P9.6	L21	I/O	IN22 / OUT22 line of GPTA
P9.7	L23	I/O	IN23 / OUT23 line of GPTA
P9.8	L20	I/O	IN24 / OUT24 line of GPTA
P9.9	K21	I/O	IN25 / OUT25 line of GPTA
P9.10	K22	I/O	IN26 / OUT26 line of GPTA
P9.11	K23	I/O	IN27 / OUT27 line of GPTA
P9.12	J21	I/O	IN28 / OUT28 line of GPTA
P9.13	J22	I/O	IN29 / OUT29 line of GPTA
P9.14	J20	I/O	IN30 / OUT30 line of GPTA
P9.15	J23	I/O	IN31 / OUT31 line of GPTA

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
P10		I/O	**Port 10** Port 10 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P10.0	H21	I/O	IN32 / OUT32 line of GPTA
P10.1	H22	I/O	IN33 / OUT33 line of GPTA
P10.2	H23	I/O	IN34 / OUT34 line of GPTA
P10.3	G21	I/O	IN35 / OUT35 line of GPTA
P10.4	G22	I/O	IN36 / OUT36 line of GPTA
P10.5	G20	I/O	IN37 / OUT37 line of GPTA
P10.6	G23	I/O	IN38 / OUT38 line of GPTA
P10.7	F22	I/O	IN39 / OUT39 line of GPTA
P10.8	F23	I/O	IN40 / OUT40 line of GPTA
P10.9	F21	I/O	IN41 / OUT41 line of GPTA
P10.10	E22	I/O	IN42 / OUT42 line of GPTA
P10.11	E23	I/O	IN43 / OUT43 line of GPTA
P10.12	E21	I/O	IN44 / OUT44 line of GPTA
P10.13	D22	I/O	IN45 / OUT45 line of GPTA
P10.14	D23	I/O	IN46 / OUT46 line of GPTA
P10.15	E20	I/O	IN47 / OUT47 line of GPTA
P11		I/O	**Port 11** Port 11 is a 16-bit bidirectional general purpose I/O port which also serves as input or output for the GPTA.
P11.0	C22	I/O	IN48 / OUT48 line of GPTA
P11.1	C23	I/O	IN49 / OUT49 line of GPTA
P11.2	C21	I/O	IN50 / OUT50 line of GPTA
P11.3	B23	I/O	IN51 / OUT51 line of GPTA
P11.4	A23	I/O	IN52 / OUT52 line of GPTA
P11.5	A22	I/O	IN53 / OUT53 line of GPTA
P11.6	B22	I/O	IN54 / OUT54 line of GPTA
P11.7	D20	I/O	IN55 / OUT55 line of GPTA
P11.8	A21	I/O	IN56 / OUT56 line of GPTA
P11.9	B21	I/O	IN57 / OUT57 line of GPTA
P11.10	C20	I/O	IN58 / OUT58 line of GPTA
P11.11	D19	I/O	IN59 / OUT59 line of GPTA
P11.12	A20	I/O	IN60 / OUT60 line of GPTA
P11.13	B20	I/O	IN61 / OUT61 line of GPTA
P11.14	C19	I/O	IN62 / OUT62 line of GPTA
P11.15	A19	I/O	IN63 / OUT63 line of GPTA

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P12		I/O	**Port 12** Port 12 is a 16-bit bidirectional general purpose I/O port or serves as ADC control port and SDLM/ASC I/O port.	
P12.0	D13	O	AD0EMUX0	ADC0 external multiplexer control 0
P12.1	A13	O	AD0EMUX1	ADC0 external multiplexer control 1
P12.2	B13	O	AD0EMUX2	ADC0 external multiplexer control 2
P12.3	C13	O	AD1EMUX0	ADC1 external multiplexer control 0
P12.4	C12	O	AD1EMUX1	ADC1 external multiplexer control 1
P12.5	A12	O	AD1EMUX2	ADC1 external multiplexer control 2
P12.6	B12	I	AD1EXTIN0	ADC1 external trigger input 0
P12.7	B11	I	AD1EXTIN1	ADC1 external trigger input 1
P12.8	C11	I	AD0EXTIN0	ADC0 external trigger input 0
P12.9	A11	I	AD0EXTIN1	ADC0 external trigger input 1
P12.10	D11	I	RXJ1850	SDLM receiver input
P12.11	C10	O	TXJ1850	SDLM transmitter output
P12.12	B10	I/O	RXD0A	ASC0 receiver input/output A
P12.13	A10	O	TXD0A	ASC0 transmitter output A
P12.14	C9	I/O	RXD1A	ASC1 receiver input/output A
P12.15	B9	O	TXD1A	ASC1 transmitter output A

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions	
P13		I/O	**Port 13** Port 13 is a 16-bit bidirectional general purpose I/O port that is also used as input/output for the serial interfaces (ASC, SSC, CAN) and timers (GPTU).	
P13.0	B19	I/O	GPT0	GPTU I/O line 0
P13.1	C18	I/O	GPT1	GPTU I/O line 1
P13.2	A18	I/O	GPT2	GPTU I/O line 2
		I/O	RXD0B	ASC0 receiver input/output B
P13.3	B18	I/O	GPT3	GPTU I/O line 3
		O	TXD0B	ASC0 transmitter output B
P13.4	A17	I/O	GPT4	GPTU I/O line 4
		I/O	RXD1B	ASC1 receiver input/output B
P13.5	D17	I/O	GPT5	GPTU I/O line 5
		O	TXD1B	ASC1 transmitter output B
P13.6	B17	I/O	GPT6	GPTU I/O line 6
		I/O	SCLK0	SSC0 clock input/output
P13.7	C17	I/O	GPT7	GPTU I/O line 7
		I/O	MRST0	SSC0 master receive / slave transmit input/output
P13.8	A16	I/O	MTSR0	SSC0 master transmit / slave receive output/input
P13.9	B16	I/O	SCLK1	SSC1 clock input/output
P13.10	C16	I/O	MRST1	SSC1 master receive / slave transmit input/output
P13.11	A15	I/O	MTSR1	SSC1 master transmit / slave receive output/input
P13.12	D15	I	RXDCAN0	CAN receiver input 0
P13.13	B15	O	TXDCAN0	CAN transmitter output 0
P13.14	C15	I	RXDCAN1	CAN receiver input 1
P13.15	A14	O	TXDCAN1	CAN transmitter output 1
CLKSEL0 **CLKSEL1** **CLKSEL2**	V21 V23 V22	I I I	**PLL Clock Selection Inputs** These pins are sampled during power-on reset ($\overline{\text{PORST}}$ = low); they determine the division rate in the feedback path of the PLL (N-Factor). The latched values of these input pins are available in the PLL Clock Control Register PLL_CLC. The combination BYPASS = 1 and CLKSEL[2:0] = 000_B during power-on reset is reserved.	

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
BYPASS	W22	I	**PLL Bypass Control Input** BYPASS is used for direct drive mode operation of the clock circuitry. This pin is sampled during power-on reset ($\overline{\text{PORST}}$ = low). Its level is latched into the PLL Clock Control Register PLL_CLC. The combination BYPASS = 1 and CLKSEL[2:0] = 000_B during power-on reset is reserved.
CFG0 **CFG1** **CFG2** **CFG3**	Y23 Y22 W21 W23	I I I I	**Operation Configuration Inputs** The configuration inputs define the boot options of the TC1775 after a hardware reset operation.
$\overline{\text{TRST}}$[3]	AA19	I	**JTAG Module Reset/Enable Input** A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.
TCK[3]	AB19	I	**JTAG Module Clock Input**
TDI[4]	AC19	I	**JTAG Module Serial Data Input**
TDO	AA18	O	**JTAG Module Serial Data Output**
TMS[4]	AB20	I	**JTAG Module State Machine Control Input**
$\overline{\text{OCDSE}}$[4]	Y19	I	**OCDS Enable Input** A low level on this pin during power-on reset ($\overline{\text{PORST}}$ = low) enables the on-chip debug support (OCDS). In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{BRKIN}}$[4]	AC20	I	**OCDS Break Input** A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.
$\overline{\text{BRKOUT}}$	AC18	O	**OCDS Break Output** A low level on this pin indicates that a programmable OCDS event has occurred.
$\overline{\text{NMI}}$[4]	Y20	I	**Non-Maskable Interrupt Input** A high-to-low transition on this pin causes a NMI-Trap request to the CPU.

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
$\overline{\text{HDRST}}$[4]	W20	I/O	**Hardware Reset Input/Reset Indication Output** Assertion of this bidirectional open-drain pin causes a synchronous reset of the chip through external circuitry. This pin must be driven for a minimum duration. The internal reset circuitry drives this pin in response to a power-on, hardware, watchdog and power-down wake-up reset for a specific period of time. For a software reset, activation of this pin is programmable.
$\overline{\text{PORST}}$[5]	Y21	I	**Power-on Reset Input** A low level on $\overline{\text{PORST}}$ causes an asynchronous reset of the entire chip. $\overline{\text{PORST}}$ is a fully asynchronous level sensitive signal.
CLKIN	T1	I	**EBU Clock Input** CLKIN must be connected externally with CLKOUT. For fine-tuning of the external bus interface timing, this external connection can be an external delay circuit.
CLKOUT	R1	O	**Clock Output**
$\overline{\text{TEST}}$ **MODE**[4]	AB23	I	**Test Mode Select Input** For normal operation of the TC1775, this pin should be connected to V_{DDP05}.
XTAL1 **XTAL2**	AC23 AC22	I O	**Oscillator/PLL/Clock Generator Input/Output Pins** XTAL1 is the input to the main oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the main oscillator amplifier circuit. For clocking the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
XTAL3 **XTAL4**	AB21 AA20	I O	**Real Time Clock Oscillator Input/Output** XTAL3 and XTAL4 are the input and the output of the 32 kHz oscillator that is used for the Real Time Clock.

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
V_{DDOSC}	AC21	–	**Main Oscillator Power Supply (2.5 V)**[6)7)]
V_{SSOSC}	AA21	–	**Main Oscillator Ground**
V_{DDPLL}	AA22	–	**PLL Power Supply (2.5 V)**[6)7)]
V_{SSPLL}	AA23	–	**PLL Ground**
V_{SS}	F4, Y6, V20, D18, K10 to K14, L10 to L14, M10 to M14, N10 to N14, P10 to P14	–	**Ground**
V_{DD}	K4, P4 V4, D6 Y10 D14 Y18 F20 K20 P20	–	**Core Power Supply (2.5 V)**[6)7)]

Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
V_{DDP05}	H4 M4 T4 Y8 Y12	–	**Ports 0 to 5 Power Supply (2.5 V)**[6)7)]
V_{DDP813}	D8 D12 D16 H20 M20 T20	–	**Port 8-13 and Dedicated Pins Power Supply (3.3 to 5 V)**[8)]
V_{DDSRAM}	AC17, AB18	–	**SRAM (RAMs of DMU, PMU, and PCP) Power Supply (2.5 V)**[7)]
V_{DDSB}	B14	–	**Stand-by Power Supply of 8 Kbyte SBSRAM (2.5 V)**[7)]
V_{DDSC}	A1	–	**ADC Short Circuit/Broken Wire Logic Power Supply (5 V)**[8)]
V_{SSSC}	A2	–	**ADC Short Circuit/Broken Wire Logic Ground**
V_{DDM}	C3	–	**ADC Analog Part Power Supply (5 V)**[8)]
V_{SSM}	A3	–	**ADC Analog Part Ground**
V_{DDA0}	D9	–	**ADC0 Analog Part Power Supply (2.5 V)**[6)7)]
V_{SSA0}	A9	–	**ADC0 Analog Part Ground for V_{DDA0}**
V_{DDA1}	H1	–	**ADC1 Analog Part Power Supply (2.5 V)**[6)7)]
V_{SSA1}	G3	–	**ADC1 Analog Part Ground for V_{DDA1}**
V_{AREF0}	C8	–	**ADC0 Reference Voltage**[8)]
V_{AGND0}	B8	–	**ADC0 Reference Ground**
V_{AREF1}	G2	–	**ADC1 Reference Voltage**[8)]
V_{AGND1}	G4	–	**ADC1 Reference Ground**

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Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	Functions
N.C.1	AB15, D10, Y14	–	**Not Connected 1** These pins must not be connected.
N.C.2	AB22, C14, K3, AC3, L4, D21, Y16	–	**Not Connected 2** For compatibility reasons, these pins should not be connected. Any connection to 5 V does not harm the device.

1) After reset, an internal pull-up device is enabled for this pin.

2) After reset, an internal pull-down device is enabled for this pin.

3) These pins have an internal pull-down device connected.

4) These pins have an internal pull-up device connected.

5) The TC1775 BA11 step has an internal pull-up device connected to this pin.

6) The voltage on power supply pins marked with 8) has to be raised earlier or at least at the same time as on power supply pins marked with 6) (details see power supply section on **Page 62**).

7) In order to minimize the danger of latch-up conditions, these 2.5 V V_{DD} power supply pins should be kept at the same voltage level during normal operating mode. This condition is best achieved by generating the 2.5 V power supplies from a single voltage source. The condition is also valid in normal operating mode if a separate stand-by power supply V_{DDSB} is used.

8) The voltage on power supply pins marked with 8) has to be raised earlier or at least at the same time as on power supply pins marked with 6) (details see power supply section on **Page 62**).

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Parallel Ports

The TC1775 has 196 digital input/output port lines, which are organized into twelve parallel 16-bit ports, Port 0 to Port 5 with 2.5 V nominal voltage (pin class B), and Port 8 to Port 13 with 3.0 to 5.25 V voltage (pin class A). Additionally, 32 analog input port lines are available, which are organized into two parallel 16-bit ports, Port 6 and Port 7.

The digital parallel ports can be all used as general purpose I/O lines or they can perform input/output functions for the on-chip peripheral units.

Port 0 to Port 5 are especially dedicated for the on-chip External Bus Interface Unit to communicate with external memories, external peripherals, or external debugging devices via an external bus interface. Port 8 to Port 13 can be assigned to the on-chip peripheral units for their specific I/O operations. An overview on the port-to-peripheral unit assignment is shown in **Figure 4**.

*Note: For further details on the three pin classes of the TC1775 I/O pins see also **Table 10** on **Page 64**:*

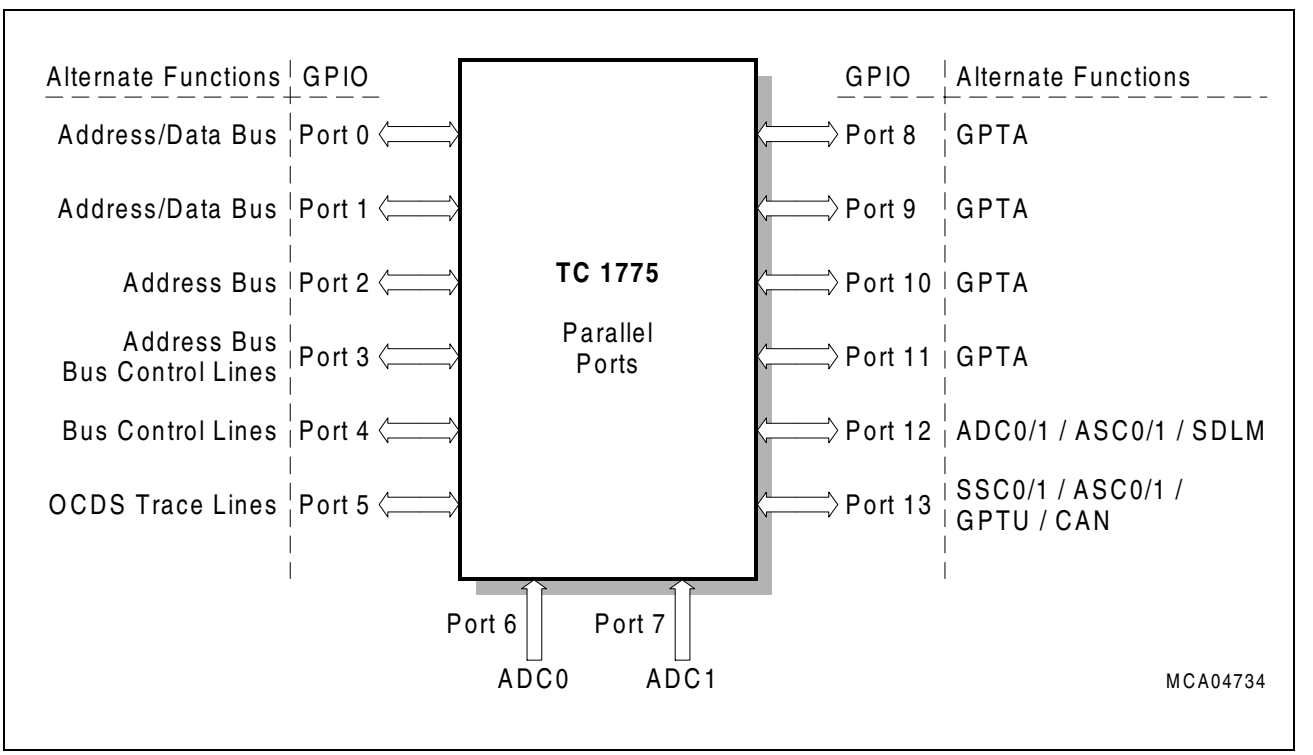

Figure 4 Parallel Ports of the TC1775

Preliminary

Serial Interfaces

The TC1775 includes six serial peripheral interface units:

- Two Asynchronous/Synchronous Serial Interfaces (ASC0 and ASC1)
- Two High-Speed Synchronous Serial Interfaces (SSC0 and SSC1)
- One TwinCAN Interface
- One J1850 Serial Data Link Interface (SDLM)

Asynchronous/Synchronous Serial Interfaces

Figure 5 shows a global view of the functional blocks of the two Asynchronous/ Synchronous Serial interfaces ASC0 and ASC1.

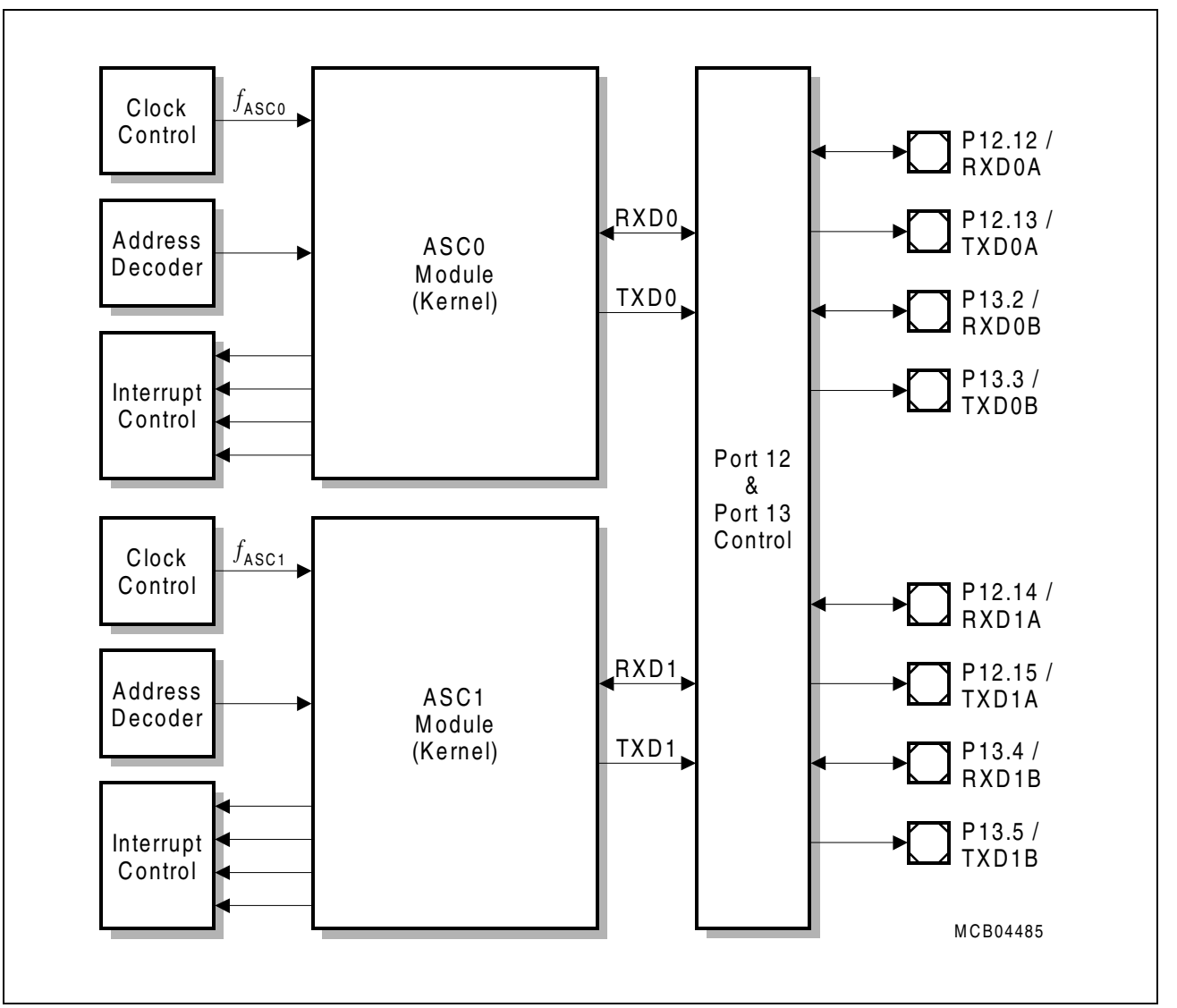

Figure 5 General Block Diagram of the ASC Interfaces

Preliminary

Each ASC module, ASC0 and ASC1, communicates with the external world via two pairs of two I/O lines each. The RXD line is the receive data input signal (in Synchronous Mode also output). TXD is the transmit output signal. Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

The Asynchronous/Synchronous Serial Interfaces provide serial communication between the TC1775 and other microcontrollers, microprocessors or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock which is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data are double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal that can be very accurately adjusted by a prescaler implemented as a fractional divider.

Features:

- Full duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baud rate from 2.5 Mbit/s to 0.6 Bit/s (@ 40 MHz clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 5 Mbit/s to 406.9 Bit/s (@ 40 MHz clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmitter buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receiver buffer full condition
  - On an error condition (frame, parity, overrun error)
- Two pin pairs RXD/TXD for each ASC available at Port 12 or Port 13

High-Speed Synchronous Serial Interfaces

Figure 6 shows a global view of the functional blocks of the two High-Speed Synchronous Serial interfaces SSC0 and SSC1.

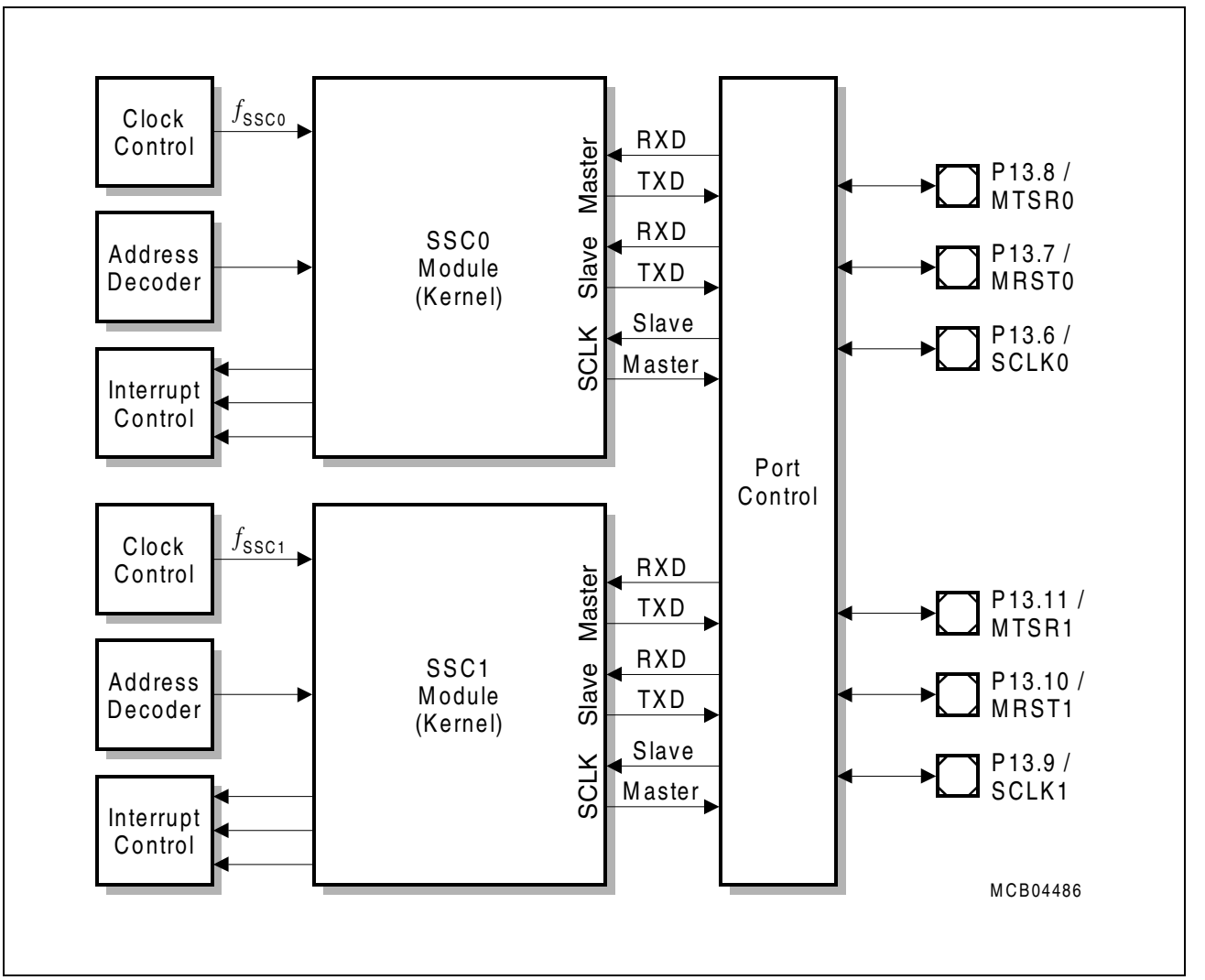

Figure 6 General Block Diagram of the SSC Interfaces

Each of the SSC modules has three I/O lines, located at Port 13. Each of the SSC modules is further supplied by separate clock control, interrupt control, address decoding, and port control logic.

The SSC supports full-duplex and half-duplex serial synchronous communication up to 20 Mbit/s (@ 40 MHz module clock). The serial clock signal can be generated by the SSC itself (master mode) or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A 16-bit baud rate generator provides the SSC with a separate serial clock signal.

Preliminary

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Flexible data format
  - Programmable number of data bits: 2 to 16 bit
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation from 20 Mbit/s to 305.18 Bit/s (@ 40 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Three-pin interface
  - Flexible SSC pin configuration

Preliminary

TwinCAN Interface

Figure 7 shows a global view of the functional blocks of the TwinCAN module.

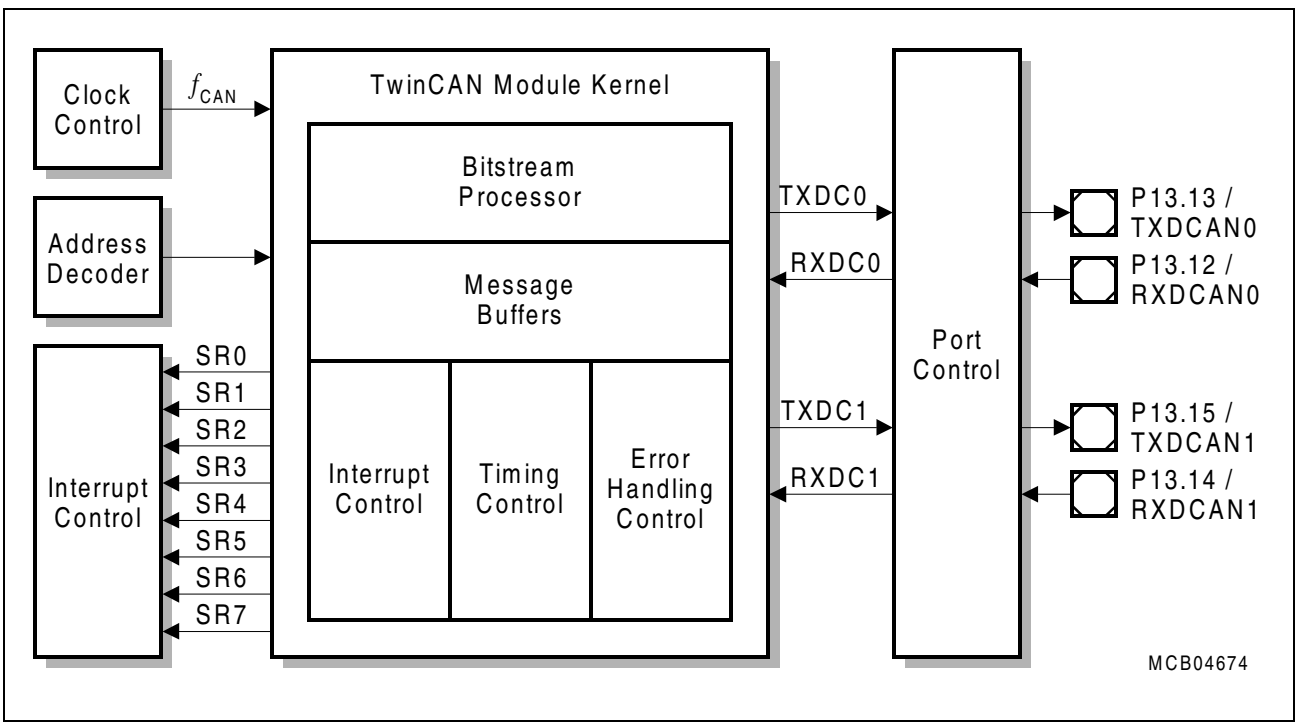

Figure 7 General Block Diagram of the TwinCAN Module

The TwinCAN module has four I/O lines located at Port 13. The TwinCAN module is further supplied by a clock control, interrupt control, address decoding, and port control logic.

The TwinCAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames are handled in accordance to CAN specification V2.0 part B (active). Each of the two Full-CAN interfaces can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share the TwinCAN module's resources to optimize the CAN bus traffic handling and to minimize the CPU load. The flexible combination of Full-CAN functionality and the FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the increased number of message objects permit precise and convenient CAN bus traffic handling.

Depending on the application, each of the thirty-two message objects can be individually assigned to one of the two CAN nodes. Gateway functionality allows automatic data exchange between two separate CAN bus systems to reduce CPU load and improve the real time behavior of the entire system.

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The bit timings for both CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 Mbit/s. A pair of receive and transmit pins connect each CAN node to a bus transceiver.

Features:

- Full CAN functionality conforms to CAN specification V2.0 B active
- Dedicated control registers are provided for each CAN node
- A data transfer rate up to 1 Mbit/s is supported
- Flexible and powerful message transfer control and error handling capabilities are implemented
- Full-CAN functionality: 32 message objects can be individually
  - Assigned to one of the two CAN nodes
  - Configured as transmit or receive objects
  - Participate in a 2, 4, 8, 16 or 32 message buffer with FIFO algorithm
  - Setup to handle frames with 11-bit or 29-bit identifiers
  - Provided with programmable acceptance mask register for filtering
  - Monitored via a frame counter
  - Configured to Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used
- CAN Analyzer Mode for bus monitoring is implemented

Serial Data Link Interface

Figure 8 shows a global view of the functional blocks of the Serial Data Link Interface (SDLM).

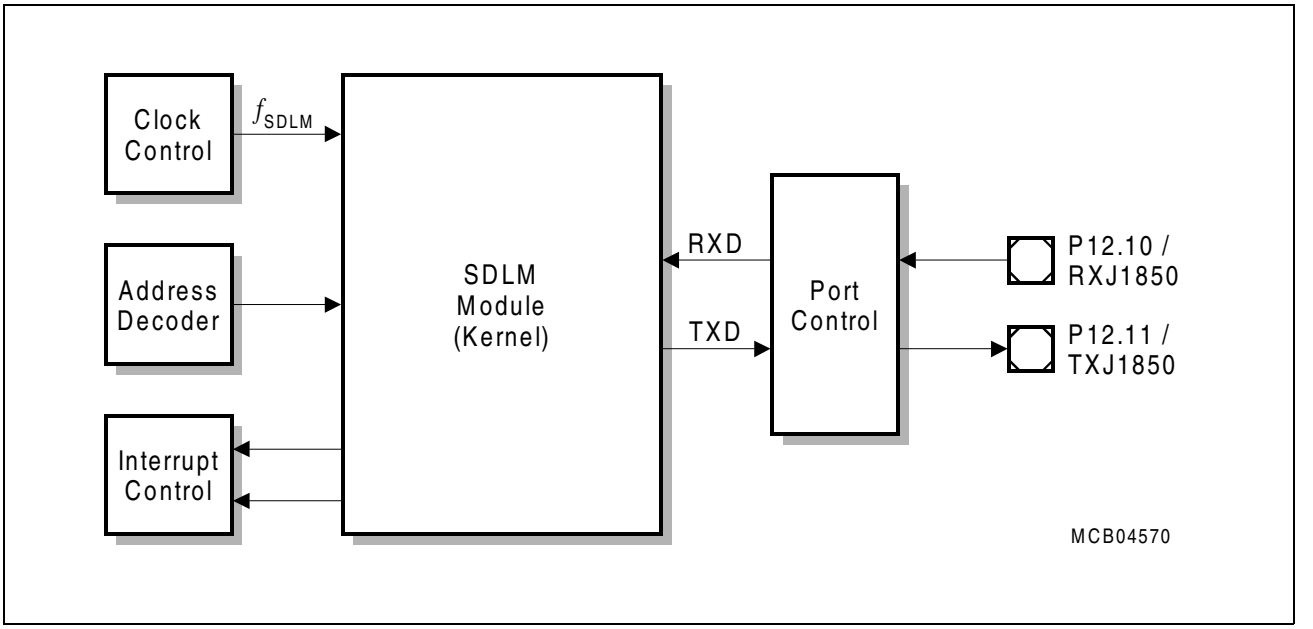

Figure 8 General Block Diagram of the SDLM Interface

The SDLM module communicates with the external world via two I/O lines located at Port 12, the J1850 bus. The RXD line is the receive data input signal and TXD is the transmit data output signal.

The Serial Data Link module (SDLM) provides serial communication to a J1850 based serial bus. J1850 bus transceivers must be implemented externally in a system. The SDLM module conforms to the SAE Class B J1850 Specification and is compatible to Class 2 protocol.

General SDLM Features:

- Compliant to SAE Class B J1850 Specification
- Full support of GM Class 2 protocol
- Variable Pulse Width (VPW) format with 10.4 kbit/s
- High speed receive/transmit 4x mode with 41.6 kbit/s
- Digital noise filter
- Support of single byte headers or consolidated headers
- CRC generation and check
- Support of Block Mode for receive and transmit

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Data Link Operation Features:

- 11-byte transmit buffer
- Double buffered 11-byte receive buffer
- Support of In-Frame Response (IFR) types 1, 2, 3
- Advanced interrupt handling for RX, TX, and error conditions
- All interrupt sources can be enabled/disabled individually
- Support of automatic IFR Transmission for IFR types 1 and 2 for 3-byte consolidated headers

Note: The SDLM module does not support the Pulse Width Modulation (PWM) data format.

Preliminary

Timer Units

The TC1775 includes two timer units:

- General Purpose Timer Unit (GPTU)
- General Purpose Timer Array (GPTA)

General Purpose Timer Unit

Figure 9 shows a global view of all functional blocks of the General Purpose Timer Unit (GPTU) module.

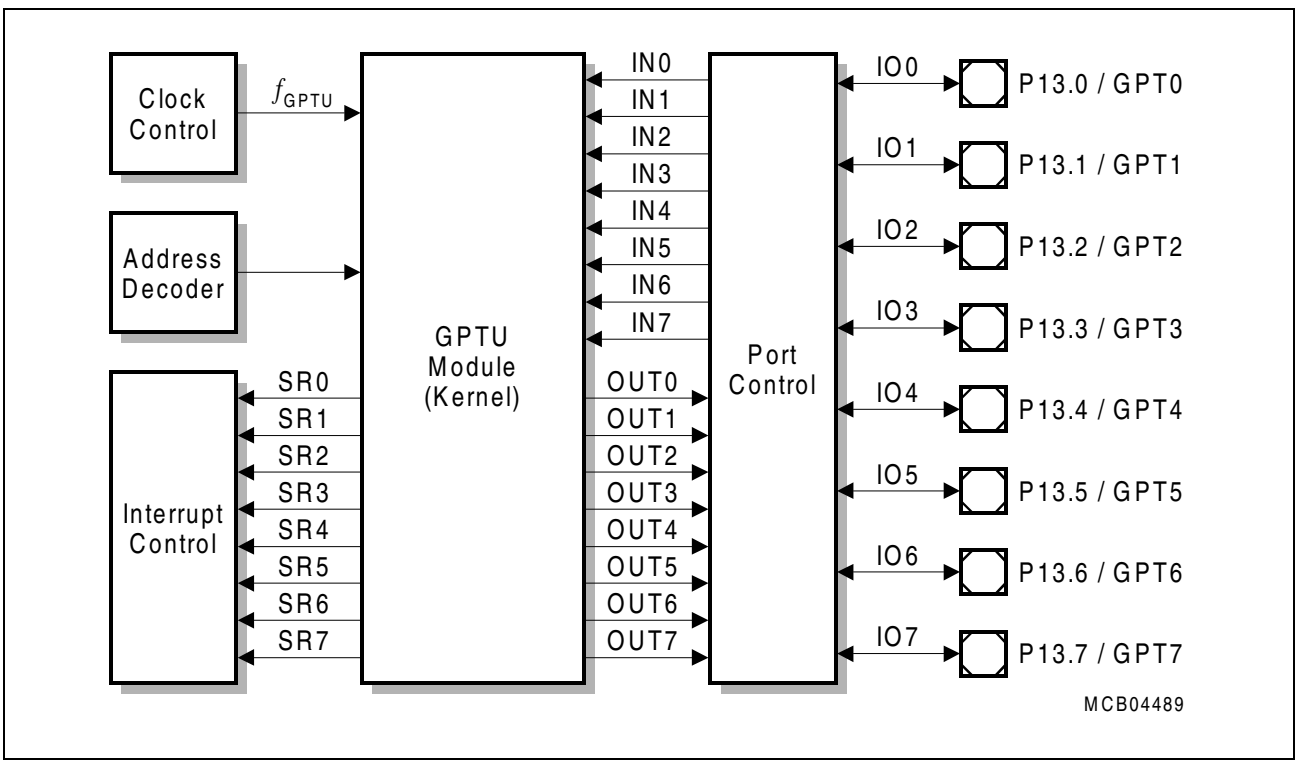

Figure 9 General Block Diagram of the GPTU Interface

The GPTU consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. The GPTU communicates with the external world via eight inputs and eight outputs located at Port 13.

The three timers of the GPTU module (T0, T1, and T2) can operate independently from each other, or can be combined:

General Features:

- All timers are 32-bit precision timers with a maximum input frequency of f_{GPTU}
- Events generated in T0 or T1 can be used to trigger actions in T2
- Timer overflow or underflow in T2 can be used to clock either T0 or T1
- T0 and T1 can be concatenated to form one 64-bit timer

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Features of T0 and T1:

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers
- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Two input pins can define a count option

Features of T2:

- Count up or down is selectable
- Operating modes:
  - Timer
  - Counter
  - Quadrature counter (incremental/phase encoded counter interface)
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins
- T2 events are freely assignable to the service request nodes

General Purpose Timer Array

Figure 10 shows a global block diagram of the General Purpose Timer Array (GPTA) implementation.

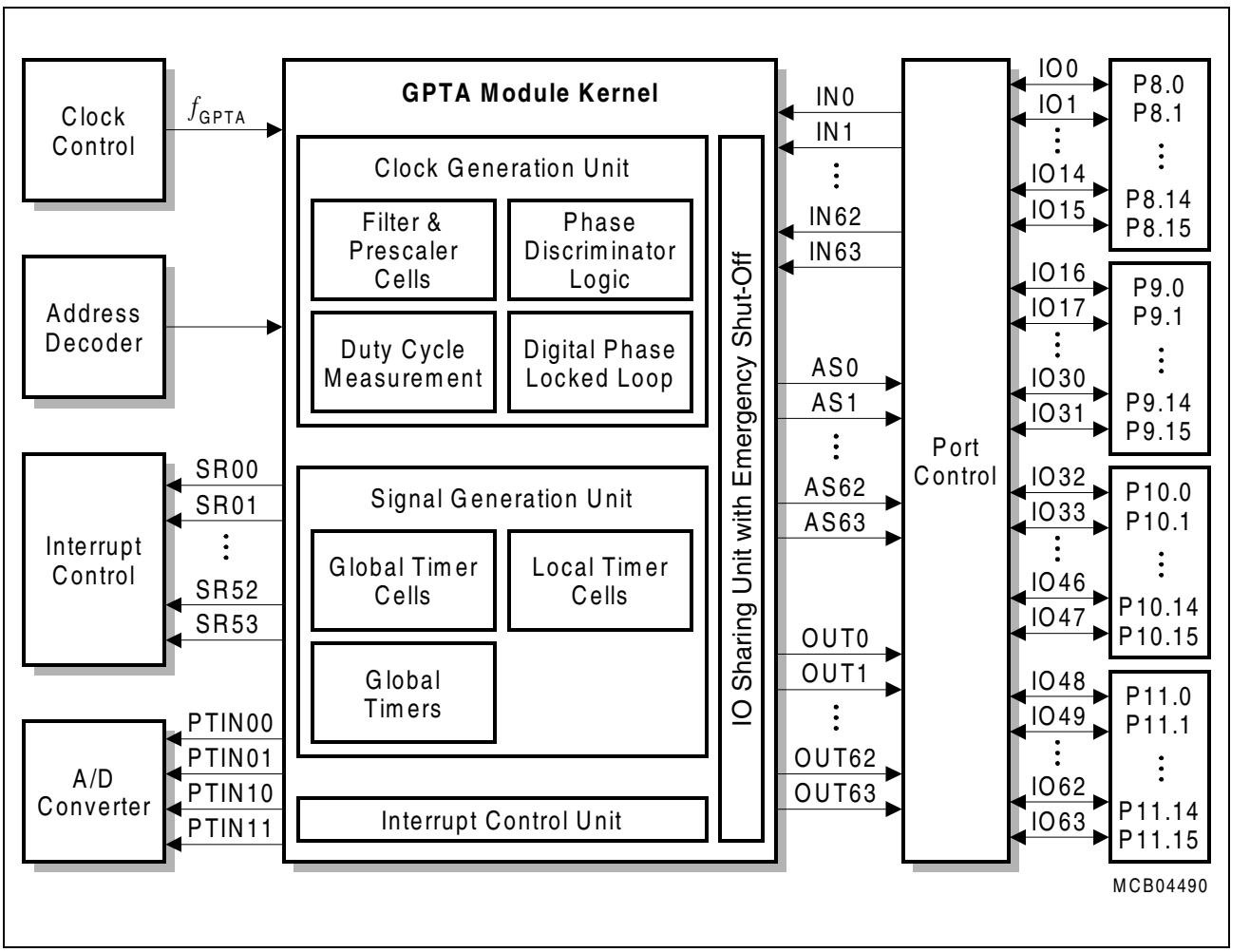

Figure 10 GPTA Module Block Diagram

The GPTA module has 64 input lines and 64 output lines, which are connected with Port 8, Port 9, Port 10, and Port 11.

The General Purpose Timer Array (GPTA) provides important digital signal filtering and timer support whose combination enables autonomous and complex functionalities. This architecture allows easy implementation and easy validation of any kind of timer functions.

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The General Purpose Timer Array (GPTA) provides a set of hardware modules required for high speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated "Global Timer Cells".
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an event that occurred at an external port pin or at an internal FPC output. A GTC may be also used to control an external port pin with the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may be also logically tied together to drive a common external port pin with a complex signal waveform. LTCs — enabled in Timer Mode or Capture Mode — can be clocked or triggered by
  - A prescaled GPTA module clock,
  - An FPC, PDL, DCM, PLL, or GTC output signal line,
  - An external port pin.

Some input lines driven by processor I/O pads may be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following list summarizes all blocks supported:

Clock Generation Unit (GPTA)

- Filter and Prescaler Cell (FPC):
  - Six independent units
  - Three operating modes (Prescaler, Delayed Debounce Filter, Immediate Debounce Filter)
  - f_{GPTA} down-scaling capability
  - $f_{GPTA}/2$ maximum input signal frequency in Filter Mode
- Phase Discriminator Logic (PDL):
  - Two independent units
  - Two operating modes (2 and 3 sensor signals)
  - $f_{GPTA}/4$ maximum input signal frequency in 2-sensor mode, $f_{GPTA}/6$ maximum input signal frequency in 3-sensor mode
- Duty Cycle Measurement (DCM):
  - Four independent units
  - 0 to 100% margin and time-out handling

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  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL):
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

GPTA Signal Generation Unit

- Global Timers (GT):
  - Two independent units
  - Two operating modes (Free Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC):
  - 32 independent units
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC):
  - 64 independent units
  - Three operating modes (Timer, Capture and Compare)
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Control Unit

- 111 interrupt sources generating 54 service requests

I/O Sharing Unit

- Able to process lines from FPC, GTC, and LTC
- Emergency function

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Analog Digital Converters

The two on-chip Analog-to-Digital Converter (ADC) modules of the TC1775 offer 8-bit, 10-bit, or 12-bit resolution including sample-and-hold functionality. The A/D converters operate using the method of the successive approximation. A multiplexer selects among up to 16 analog input channels for each ADC. Conversion requests are generated either under software control or by hardware. An automatic self-calibration adjusts the ADC modules to changing temperatures or process variations.

Features:

- 8-bit, 10-bit, 12-bit A/D conversion
- Successive approximation conversion method
- Fast conversion times: e.g. 10-bit conversion (without sample time): 5.05 µs
- Total Unadjusted Error (TUE) of ±2 LSB @ 10-bit resolution
- Integrated sample-and-hold functionality
- Sixteen analog input channels
- Dedicated control and status registers for each analog channel
- Powerful conversion request sources
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Broken wire – short circuit detection
- Flexible service request generation
- Synchronization of the two on-chip A/D Converters
- Automatic control of external analog multiplexer
- Equidistant samples initiated by timer
- External trigger inputs for conversion requests
- Two external trigger inputs, connected with the General Purpose Timer Array (GPTA)
- Power reduction and clock control

Figure 11 shows a global view of the ADC module kernels with the module specific interface connections.

Each of the ADC modules communicates with the external world via five digital I/O lines and sixteen analog inputs. Clock control, address decoding, and interrupt service request control are managed outside the ADC module kernel. Two trigger inputs and a synchronization bridge are used for internal control purposes.

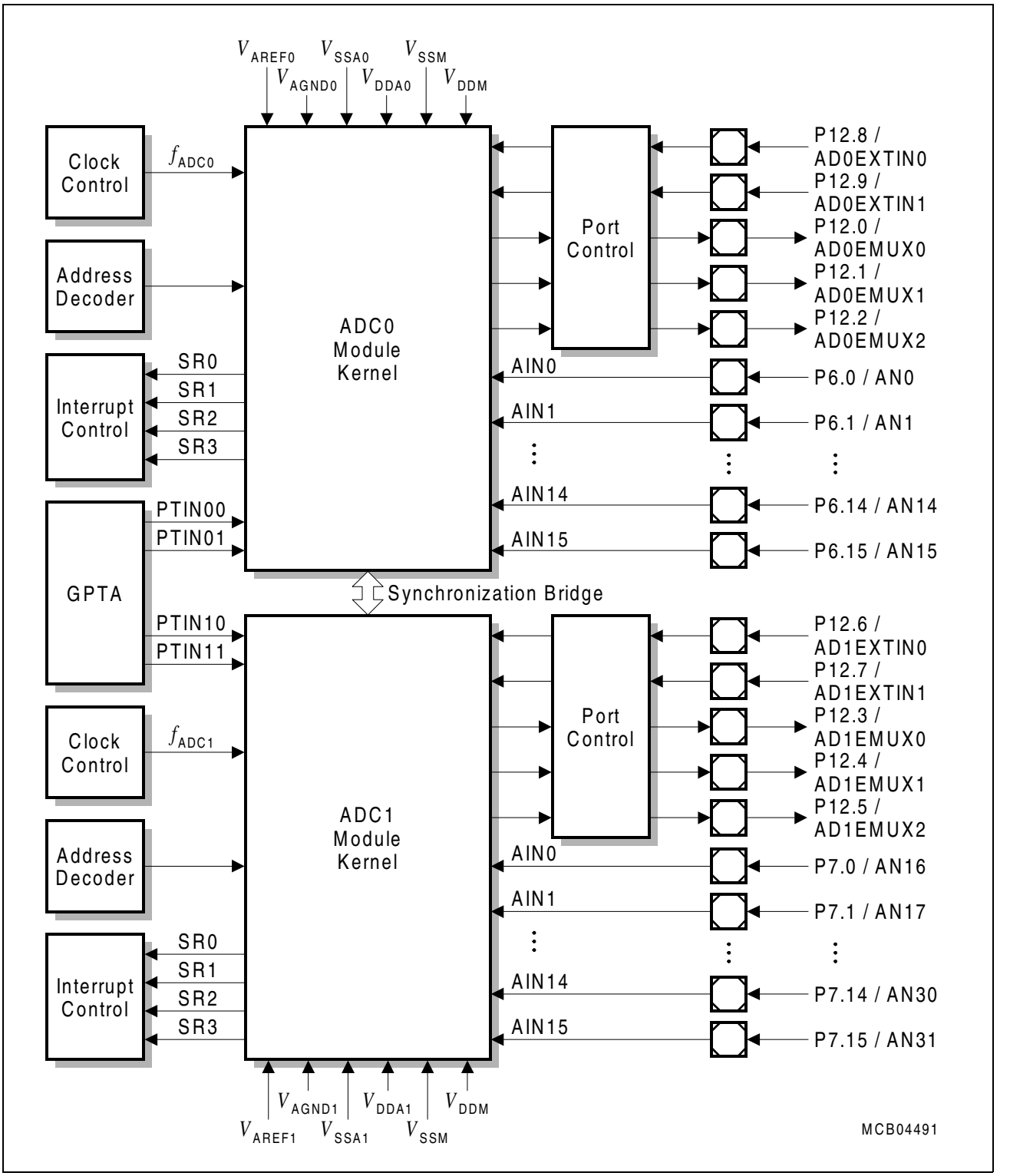


Figure 11 ADC0/ADC1 Modules with Interconnections

Preliminary

On-Chip Memories

The memory system of the TC1775 provides the following memories:

- Program Memory Unit (PMU) with
  - 8 Kbytes Boot ROM (BROM)
  - 32 Kbytes Code Scratch-Pad RAM (SPRAM)
  - 1 Kbyte Instruction Cache (ICACHE)
- Data Memory Unit (DMU) with
  - 40 Kbytes Data Memory (SRAM)
  - Includes 8 Kbytes static RAM (SBSRAM) for standby operation using a battery
- Peripheral Control Processor (PCP) with
  - 16 Kbytes Data Memory (PCODE)
  - 4 Kbytes Parameter RAM (PRAM)

Preliminary

Address Map

Table 2 defines the specific segment oriented address blocks of the TC1775 with its address range, size, and PMU/DMU access view. Table 3 shows the block address map of memory segment 15 which includes the on-chip peripheral units.

Table 2 TC1775 Block Address Map

Segment	Address Range	Size	Description	DMU Acc.	PMU Acc.[1]	
0 to 7	$0000\ 0000_H$ – $7FFF\ FFFF_H$	2 GB	Reserved	–	–	
8	$8000\ 0000_H$ – $8FFF\ FFFF_H$	256 MB	Reserved	via FPI	PMU local	cached
9	$9000\ 0000_H$ – $9FFF\ FFFF_H$	256 MB	Reserved	DMU local	via FPI	
10	$A000\ 0000_H$ – $AFFF\ FFFF_H$	256 MB	External Memory Space	via FPI	via EBU or FPI	
11	$B000\ 0000_H$ – $BDFF\ FFFF_H$	224 MB	External Memory Space mappable into segment 10	via FPI	via EBU	non-cached
	$BE00\ 0000_H$ – $BEFF\ FFFF_H$	16 MB	External Emulator Space		via FPI	
	$BF00\ 0000_H$ – $BFFF\ DFFF_H$	–	Reserved		PMU local	
	$BFFF\ E000_H$ – $BFFF\ FFFF_H$	8 KB	Boot ROM 4 Kbytes general purpose 4 Kbytes factory test support			
12	$C000\ 0000_H$ – $C000\ 7FFF_H$	32 KB	Local Code Scratch-Pad RAM (SPRAM)	via FPI	PMU local	
	$C000\ 8000_H$ – $C7FF\ FEFF_H$	–	Reserved			
	$C7FF\ FF00_H$ – $C7FF\ FFFF_H$	256 B	PMU Control Registers			
	$C800\ 0000_H$ – $CFFF\ FFFF_H$	128 MB	Reserved			

Table 2 TC1775 Block Address Map (cont'd)

Segment	Address Range	Size	Description	DMU Acc.	PMU Acc.[1)]	
13	D000 0000$_H$ – D000 7FFF$_H$	32 KB	Local Data Memory (SRAM)	DMU local	via FPI	non-cached
	D000 8000$_H$ – D000 9FFF$_H$	8 KB	Local Data Memory for standby operation (SBSRAM)			
	D000 A000$_H$ – D000 BFFF$_H$	8 KB	SBSRAM mirrored			
	D000 C000$_H$ – D000 DFFF$_H$	8 KB	SBSRAM mirrored			
	D000 E000$_H$ – D000 FFFF$_H$	8 KB	SBSRAM mirrored			
	D000 A000$_H$ – D7FF FEFF$_H$	–	Reserved			
	D7FF FF00$_H$ – D7FF FFFF$_H$	256 B	DMU Registers			
	D800 0000$_H$ – DFFF FFFF$_H$	256 MB	Reserved			
14	E000 0000$_H$ – EFFF FFFF$_H$	256 MB	External Peripheral and Data Memory Space	via FPI	not possible	

Table 2 TC1775 Block Address Map (cont'd)

Segment	Address Range	Size	Description	DMU Acc.	PMU Acc.[1]	
15	$F000\ 0000_H$ – $F000\ 3EFF_H$	16 KB	On-Chip Peripherals & Ports	via FPI	not possible	non-cached
	$F000\ 3F00_H$ – $F000\ 3FFF_H$	256 B	PCP Registers			
	$F000\ 4000_H$ – $F000\ FFFF_H$	–	Reserved			
	$F001\ 0000_H$ – $F001\ 0FFF_H$	4 KB	PCP Parameter Memory (PRAM)			
	$F001\ 1000_H$ – $F001\ FFFF_H$	–	Reserved			
	$F002\ 0000_H$ – $F002\ 3FFF_H$	16 KB	PCP Code Memory (PCODE)			
	$F002\ 4000_H$ – $F00F\ FFFF_H$	–	Reserved			
	$F010\ 0000_H$ – $F010\ 0BFF_H$	12 × 256 B	CAN Module			
	$F010\ 0C00_H$ – $FFFE\ FEFF_H$	–	Reserved			
	$FFFE\ FF00_H$ – $FFFE\ FFFF_H$	256 B	CPU Slave Interface Registers (CPS)			
	$FFFF\ 0000_H$ – $FFFF\ FFFF_H$	64 KB	Core SFRs + GPRs			

[1] The PMU can access external memory directly ("via EBU", only instruction accesses) or via the FPI Bus ("via FPI").

Table 3 Block Address Map of Segment 15

Symbol	Description	Address Range	Size
SCU	System Control Unit	F000 0000$_H$ – F000 00FF$_H$	256 Bytes
RTC	Real Time Clock	F000 0100$_H$ – F000 01FF$_H$	256 Bytes
BCU	Bus Control Unit	F000 0200$_H$ – F000 02FF$_H$	256 Bytes
STM	System Timer	F000 0300$_H$ – F000 03FF$_H$	256 Bytes
OCDS	On-Chip Debug Support	F000 0400$_H$ – F000 04FF$_H$	256 Bytes
EBU	External Bus Unit	F000 0500$_H$ – F000 05FF$_H$	256 Bytes
–	Reserved	F000 0600$_H$ – F000 06FF$_H$	–
GPTU	General Purpose Timer Unit	F000 0700$_H$ – F000 07FF$_H$	256 Bytes
ASC0	Async./Sync. Serial Interface 0	F000 0800$_H$ – F000 08FF$_H$	256 Bytes
ASC1	Async./Sync. Serial Interface 1	F000 0900$_H$ – F000 09FF$_H$	256 Bytes
SSC0	High-Speed Synchronous Serial Interface 0	F000 0A00$_H$ – F000 0AFF$_H$	256 Bytes
SSC1	High-Speed Synchronous Serial Interface 1	F000 0B00$_H$ – F000 0BFF$_H$	256 Bytes
–	Reserved	F000 0C00$_H$ – F000 17FF$_H$	–
GPTA	General Purpose Timer Array	F000 1800$_H$ – F000 1FFF$_H$	8 × 256 Bytes
–	Reserved	F000 2000$_H$ – F000 21FF$_H$	–
ADC0	Analog-to-Digital Converter 0	F000 2200$_H$ – F000 23FF$_H$	512 Bytes
ADC1	Analog-to-Digital Converter 1	F000 2400$_H$ – F000 25FF$_H$	512 Bytes
SDLM	Serial Data Link Module	F000 2600$_H$ – F000 26FF$_H$	256 Bytes
–	Reserved	F000 2700$_H$ – F000 27FF$_H$	–
P0	Port 0	F000 2800$_H$ – F000 28FF$_H$	256 Bytes
P1	Port 1	F000 2900$_H$ – F000 29FF$_H$	256 Bytes
P2	Port 2	F000 2A00$_H$ – F000 2AFF$_H$	256 Bytes
P3	Port 3	F000 2B00$_H$ – F000 2BFF$_H$	256 Bytes
P4	Port 4	F000 2C00$_H$ – F000 2CFF$_H$	256 Bytes
P5	Port 5	F000 2D00$_H$ – F000 2DFF$_H$	256 Bytes
P6	Port 6 (no registers available)	F000 2E00$_H$ – F000 2EFF$_H$	256 Bytes
P7	Port 7 (no registers available)	F000 2F00$_H$ – F000 2FFF$_H$	256 Bytes
P8	Port 8	F000 3000$_H$ – F000 30FF$_H$	256 Bytes
P9	Port 9	F000 3100$_H$ – F000 31FF$_H$	256 Bytes

Table 3 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
P10	Port 10	F000 3200$_H$ – F000 32FF$_H$	256 Bytes
P11	Port 11	F000 3300$_H$ – F000 33FF$_H$	256 Bytes
P12	Port 12	F000 3400$_H$ – F000 34FF$_H$	256 Bytes
P13	Port 13	F000 3500$_H$ – F000 35FF$_H$	256 Bytes
–	Reserved	F000 3600$_H$ – F000 3EFF$_H$	–
PCP	PCP Registers	F000 3F00$_H$ – F000 3FFF$_H$	256 Bytes
	Reserved	F000 4000$_H$ – F000 FFFF$_H$	–
	PCP Data Memory (PRAM)	F001 0000$_H$ – F001 0FFF$_H$	4 Kbytes
	Reserved	F001 1000$_H$ – F001 FFFF$_H$	–
	PCP Code Memory (PCODE)	F002 0000$_H$ – F002 3FFF$_H$	16 Kbytes
–	Reserved	F002 4000$_H$ – F00F FFFF$_H$	–
CAN[1)]	Controller Area Network Module	F010 0000$_H$ – F010 0BFF$_H$	12 × 256 Bytes
–	Reserved	F010 0C00$_H$ – FFFE FEFF$_H$	–
CPU	Slave Interface Registers (CPS)	FFFE FF00$_H$ – FFFE FFFF$_H$	256 Bytes
	Reserved	FFFF 0000$_H$ – FFFF BFFF$_H$	–
	Memory Protection Registers	FFFF C000$_H$ – FFFF EFFF$_H$	12 Kbytes
	Reserved	FFFF F000$_H$ – FFFF FCFF$_H$	–
	Core Debug Register (OCDS)	FFFF FD00$_H$ – FFFF FDFF$_H$	256 Bytes
	Core Special Function Registers (CSFRs)	FFFF FE00$_H$ – FFFF FEFF$_H$	256 Bytes
	General Purpose Register (GPRs)	FFFF FF00$_H$ – FFFF FFFF$_H$	256 Bytes

1) Access to unused address regions within this peripheral unit don't generate a bus error.

Preliminary

Memory Protection System

The TC1775 memory protection system specifies the addressable range and read/write permissions of memory segments available to the currently executing task. The memory protection system controls the position and range of addressable segments in memory. It also controls the kinds of read and write operations allowed within addressable memory segments. Any illegal memory access is detected by the memory protection hardware, which then invokes the appropriate Trap Service Routine (TSR) to handle the error. Thus, the memory protection system protects critical system functions against both software and hardware errors. The memory protection hardware can also generate signals to the Debug Unit to facilitate tracing illegal memory accesses.

There are two Memory Protection Register Sets in the TC1775, numbered 0 and 1, which specify memory protection ranges and permissions for code and data. The PSW.PRS bit field determines which of these is the set currently in use by the CPU. Because the TC1775 uses a Harvard-style memory architecture, each Memory Protection Register Set is broken down into a Data Protection Register Set and a Code Protection Register Set. Each Data Protection Register Set can specify up to four address ranges to receive particular protection modes. Each Code Protection Register Set can specify up to two address ranges to receive particular protection modes.

Each of the Data Protection Register Sets and Code Protection Register Sets determines the range and protection modes for a separate memory area. Each contains register pairs which determine the address range (the Data Segment Protection Registers and Code Segment Protection Registers) and one register (Data Protection Mode Register) which determines the memory access modes which apply to the specified range.

Preliminary

On-Chip FPI Bus

The FPI Bus interconnects the functional units of the TC1775, such as the CPU and on-chip peripheral components. The FPI Bus also interconnects the TC1775 to external components by way of the External Bus Controller Unit (EBU). The FPI Bus is designed to be quick to acquire by on-chip functional units, and quick to transfer data. The low setup overhead of the FPI Bus access protocol guarantees fast FPI Bus acquisition, which is required for time-critical applications. The FPI Bus is designed to sustain high transfer rates. For example, a peak transfer rate of up to 160 Mbyte/s can be achieved with a 40 MHz bus clock and 32-bit data bus. Multiple data transfers per bus arbitration cycle allow the FPI Bus to operate at close to its peak bandwidth.

Features:

- Supports multiple bus masters
- Supports demultiplexed address/data operation
- Address and data buses are 32 bits wide
- Data transfer types include 8-, 16-, and 32-bit sizes
- Single- and multiple-data transfers per bus acquisition cycle
- Designed to minimize EMI and power consumption

External Bus Unit

The External Bus Unit (EBU) of the TC1775 is the interface between external memories and peripheral units and the internal memories and peripheral units. The basic structure of the EBU is shown in **Figure 12**.

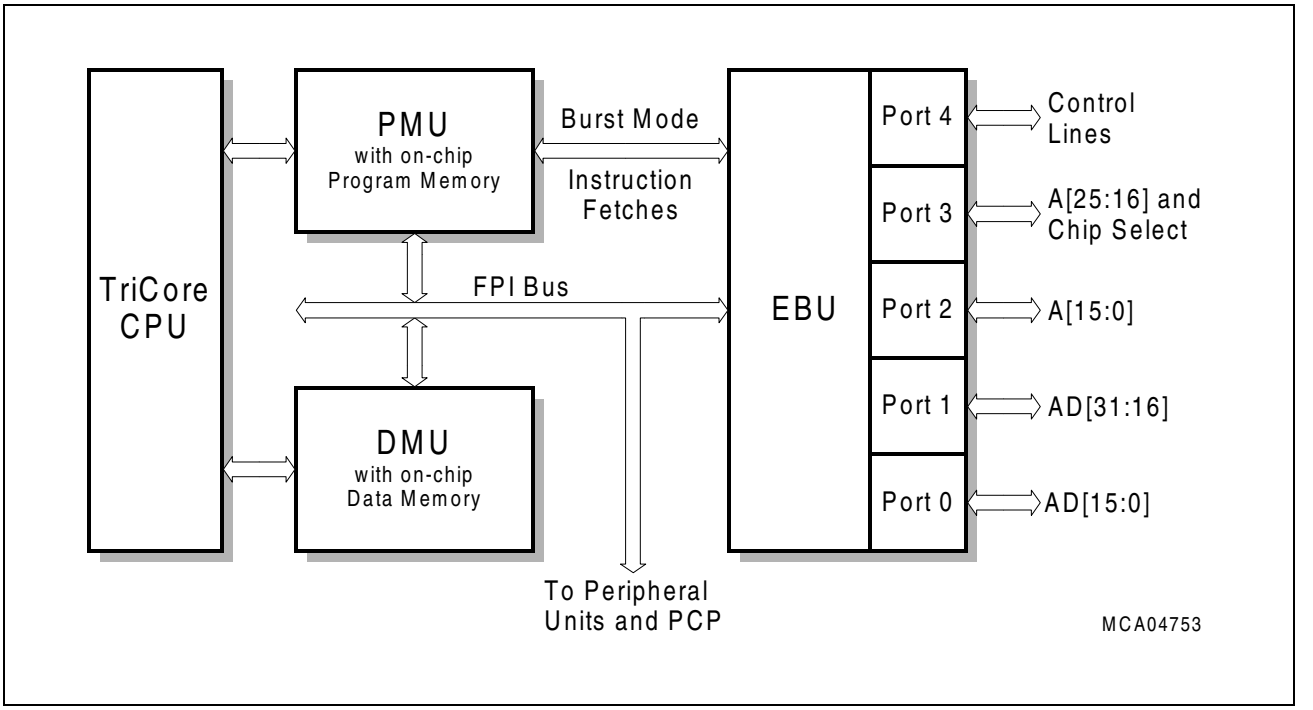


Figure 12 EBU Structure and Interfaces

The EBU is primarily used for the following two operations:

- Communication with external memories or peripheral units via the FPI Bus
- Instruction fetches from the PMU to external Burst Flash program memories

The EBU controls all transactions required for these two operations and in particular handles the arbitration between these two tasks.

The types of external devices/bus modes controlled by the EBU are:

- INTEL style peripherals (separate $\overline{RD}$ and $\overline{WR}$ signals)
- ROMs, EPROMs
- Static RAMs
- Demultiplexed A/D bus
- Multiplexed A/D bus

The PMU controls accesses to external code memories. It especially supports:

  – Burst Mode Flash Memories (ROM)

Note: Instruction fetches of the PMU from external Burst Flash program memories are only possible with 32-bit data bus width.

Preliminary

Peripheral Control Processor

The Peripheral Control Processor (PCP) performs tasks that would normally be performed by the combination of a DMA controller and its supporting CPU interrupt service routines in a traditional computer system. It could easily be considered as the host processor's first line of defense as an interrupt-handling engine. The PCP can off-load the CPU from having to service time-critical interrupts. This provides many benefits, including:

- Avoiding large interrupt-driven task context-switching latencies in the host processor
- Lessening the cost of interrupts in terms of processor register and memory overhead
- Improving the responsiveness of interrupt service routines to data-capture and data-transfer operations
- Easing the implementation of multitasking operating systems.

The PCP has an architecture that efficiently supports DMA type transactions to and from arbitrary devices and memory addresses within the TC1775 and also has reasonable stand alone computational capabilities.

The PCP is made up of several modular blocks as follows:

- PCP Processor Core
- Code Memory (PCODE)
- Parameter Memory (PRAM)
- PCP Interrupt Control Unit (PICU)
- PCP Service Request Nodes (PSRN)
- System bus interface to the FPI Bus

The PCP is fully interrupt-driven, meaning it is only activated through service requests; there is no main program running in the background as with a conventional processor.

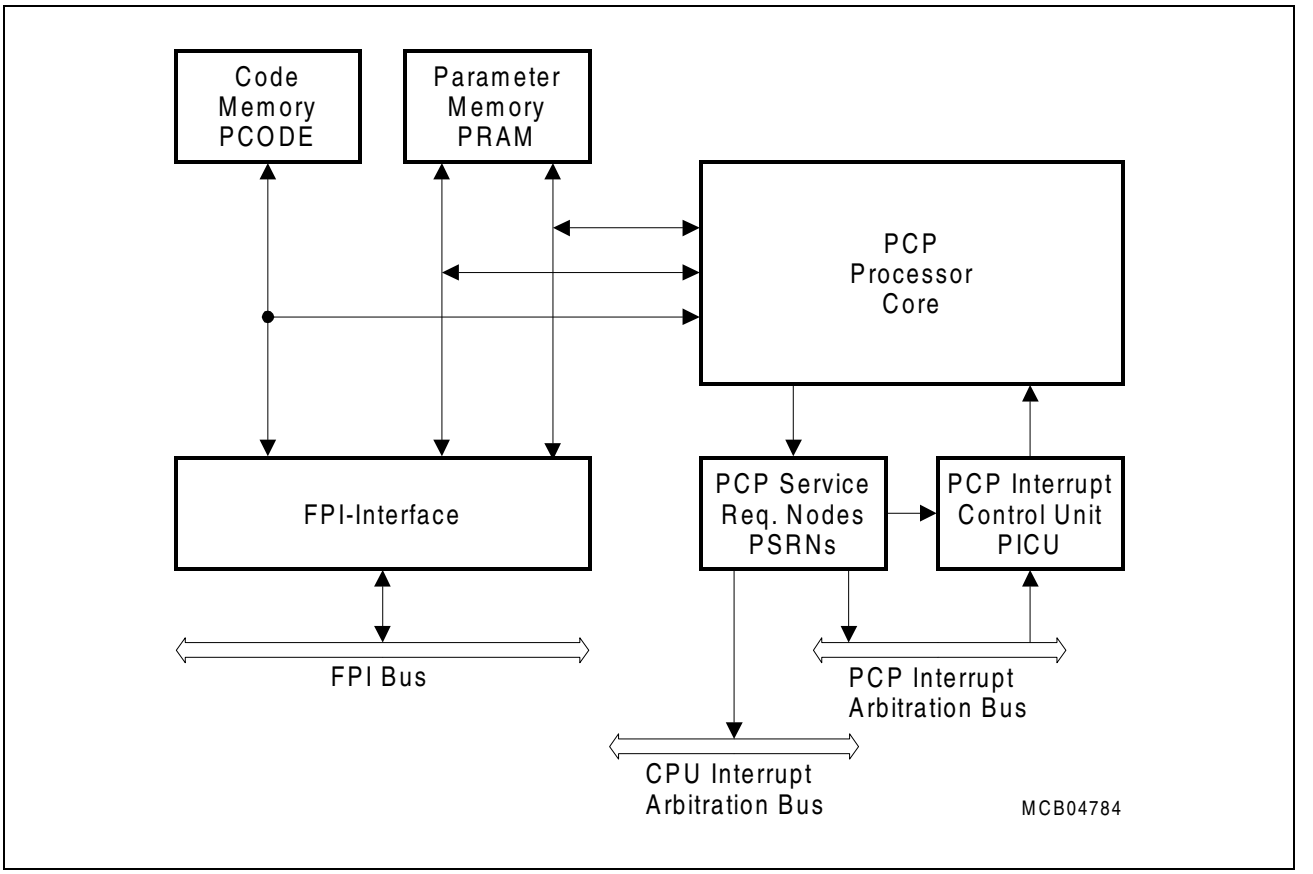


Figure 13 PCP Block Diagram

Table 4 PCP Instruction Set Overview

Instruction Group	Description
DMA primitives	Efficient DMA channel implementation
Load/Store	Transfer data between PRAM or FPI memory and the general purpose registers, as well as move or exchange values between registers
Arithmetic	Add, subtract, compare and complement
Divide/Multiply	Divide and multiply
Logical	And, Or, Exclusive Or, Negate
Shift	Shift right or left, rotate right or left, prioritize
Bit Manipulation	Set, clear, insert and test bits
Flow Control	Jump conditionally, jump long, exit
Miscellaneous	No operation, Debug

Preliminary

System Timer

The STM within the TC1775 is designed for global system timing applications requiring both high precision and long range. The STM provides the following features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Driven by clock f_{STM} (identical with the system clock f_{SYS})
- Counting begins at power-on reset
- Continuous operation is not affected by any reset condition except power-on reset

The STM is an upward counter, running with the system clock frequency f_{SYS}. It is enabled per default after reset, and immediately starts counting up. Other than via reset, it is not possible to affect the contents of the timer during normal operation of the application, it can only be read, but not written to. Depending on the implementation of the clock control of the STM, the timer can optionally be disabled or suspended for power-saving and debugging purposes via a clock control register.

The maximum clock period is $2^{56} \times 1/f_{STM}$. At f_{STM} = 40 MHz, for example, the STM counts 57.1 years before overflowing. Thus, it is capable of continuously timing the entire expected product life-time of a system without overflowing.

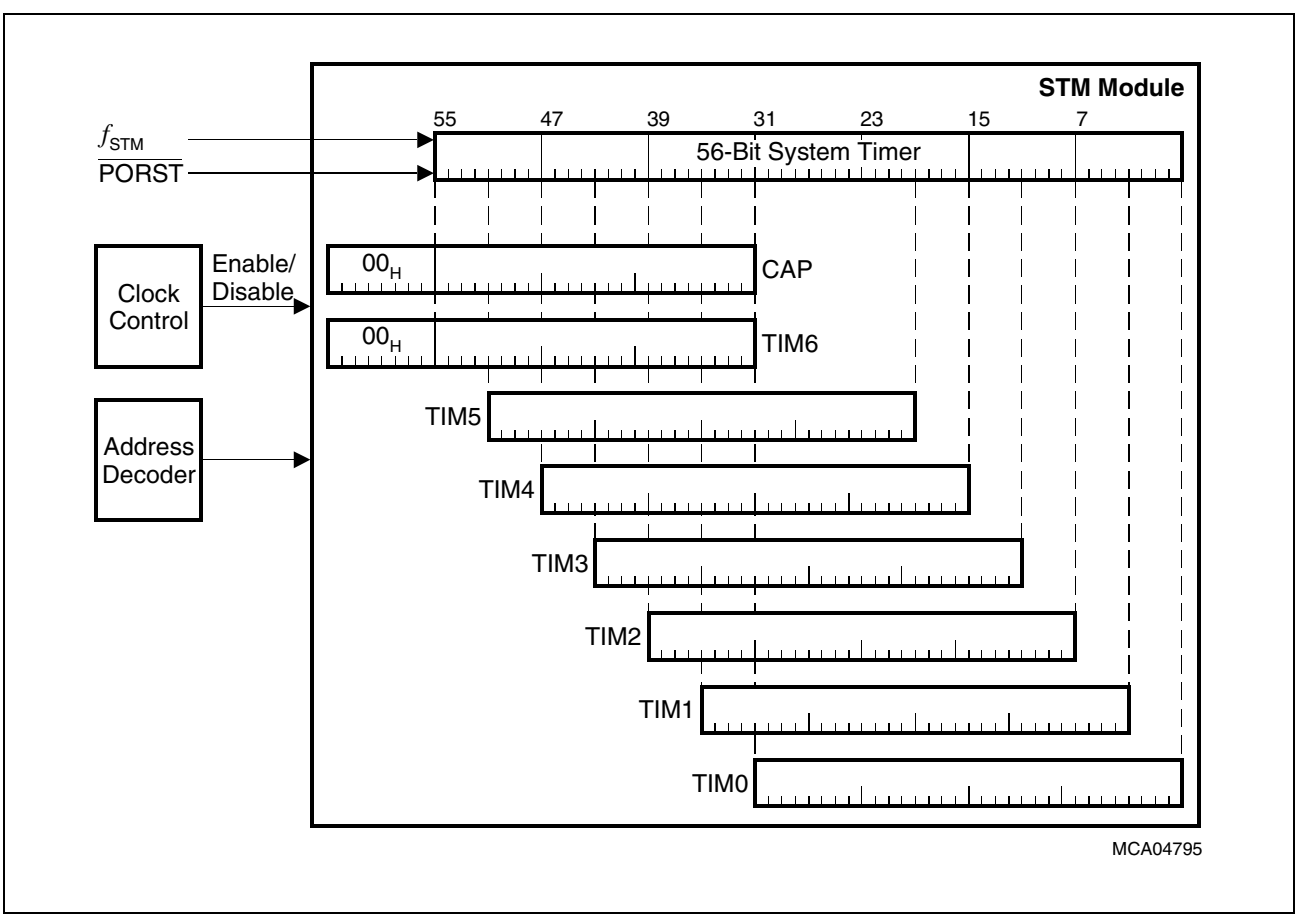


Figure 14 Block Diagram of the STM Module

Preliminary

Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1775 in a user-specified time period. When enabled, the WDT will cause the TC1775 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1775 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the EndInit feature and monitors its modifications. A system-wide line is connected to the ENDINIT bit implemented in a WDT control register, serving as an additional write-protection for critical registers (besides Supervisor Mode protection).

A further enhancement in the TC1775’s Watchdog Timer is its reset prewarning operation. Instead of immediately resetting the device on the detection of an error, as known from standard Watchdogs, the WDT first issues an Non-maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, an important aid in debugging.

Features:

- 16-bit Watchdog counter
- Selectable input frequency: $f_{SYS}/256$ or $f_{SYS}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT and limited.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation.
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation.
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a Watchdog induced reset occurs twice without a proper access to its control register in between, a severe system malfunction is assumed and the TC1775 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.

- Important debugging support is provided through the reset prewarning operation by first issuing an NMI to the CPU before finally resetting the device after a certain period of time.

Real Time Clock

Figure 15 shows a global view of all functional blocks oft he RTC interface.

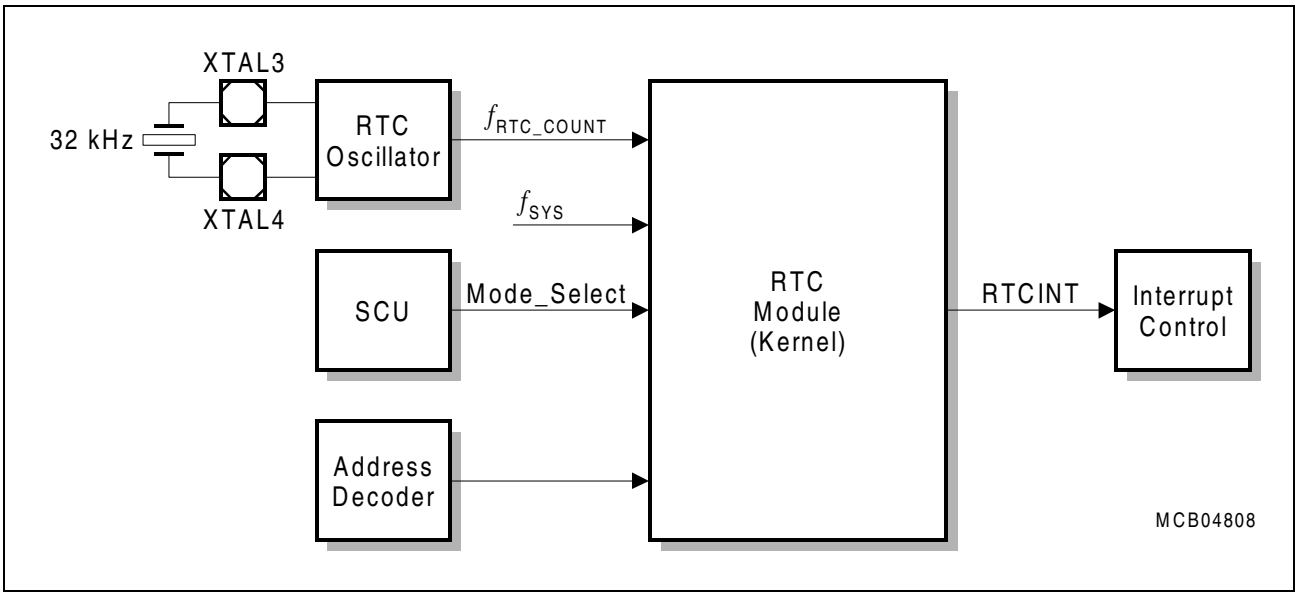


Figure 15 Block Diagram of the RTC Interface

The Real Time Clock (RTC) module is an independent timer chain that counts time ticks. The base frequency of the RTC can be programmed via a reload counter. The RTC can work asynchronously with the system frequency, and is optimized on low power consumption.

Features:

- On-chip 32.768 kHz oscillator for counting current time and date
- Cyclic time-based interrupts
- Alarm interrupt for wake-up on a defined time
- 48-bit timer for long-term measurements

Preliminary

System Control Unit

The System Control Unit (SCU) of the TC1775 handles the system control tasks. All these system functions are tightly coupled, thus, they are conveniently handled by one unit, the SCU. The system tasks of the SCU are:

- Reset Control
  - Generation of all internal reset signals
  - Generation of external $\overline{\text{HDRST}}$ reset signal
- PLL Control
  - PLL_CLC Clock Control Register
- Power Management Control
  - Enabling of several power-down modes
  - Control of the PLL in power-down modes
- Watchdog Timer
- Port 5 Trace Control
- Device Identification

Preliminary

Interrupt System

An interrupt request can be serviced either by the CPU or by the Peripheral Control Processor (PCP). These units are called “Service Providers”. Interrupt requests are called “Service Requests” rather than “Interrupt Requests” in this document because they can be serviced by either of the Service Providers.

Each peripheral in the TC1775 can generate service requests. Additionally, the Bus Control Unit, the Debug Unit, the PCP, and even the CPU itself can generate service requests to either of the two Service Providers. As shown in **Figure 16**, each TC1775 unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRCx, where “mod” is the identifier of the service requesting unit and “x” an optional index. Two buses connect the SRNs with two Interrupt Control Units, which handle interrupt arbitration among competing interrupt service requests, as follows:

- The Interrupt Control Unit (ICU) arbitrates service requests for the CPU and administers the CPU Interrupt Arbitration Bus.
- The Peripheral Interrupt Control Unit (PICU) arbitrates service requests for the PCP and administers the PCP Interrupt Arbitration Bus.

Units, which can generate service requests are:

- General Purpose Timer Unit (GPTU) with 8 SRNs
- General Purpose Timer Array (GPTA) with 54 SRNs
- Two High-Speed Synchronous Serial Interfaces (SSC0/SSC1) with 3 SRNs each
- Two Asynchronous/Synchronous Serial Interfaces (ASC0/ASC1) with 4 SRNs each
- TwinCAN controller with 8 SRNs
- Serial Data Link Module (SDLM) with 2 SRNs
- Two Analog/Digital Converters (ADC0/ADC1) with 4 SRNs each
- Real Time Clock (RTC) with 1 SRN
- Bus Control Unit (BCU) with 1 SRN
- Peripheral Control Processor (PCP) with 4 SRNs
- Central Processing Unit (CPU) with 4 SRNs
- Debug Unit (OCDS) with 1 SRN

The PCP can make service requests directly to itself (via the PICU), or it can make service requests to the CPU. The Debug Unit can generate service requests to the PCP or the CPU. The CPU can make service requests directly to itself (via the ICU), or it can make service requests to the PCP. The CPU Service Request Nodes are activated through software.

External interrupt inputs in TC1775 are available using the input pins connected to the General-Purpose Timer Unit (GPTU). Each of the eight GPTU I/O pins can be used as an external interrupt input, using the Service Request Nodes of the GPTU module. In addition, such an external interrupt input can also trigger a timer function.

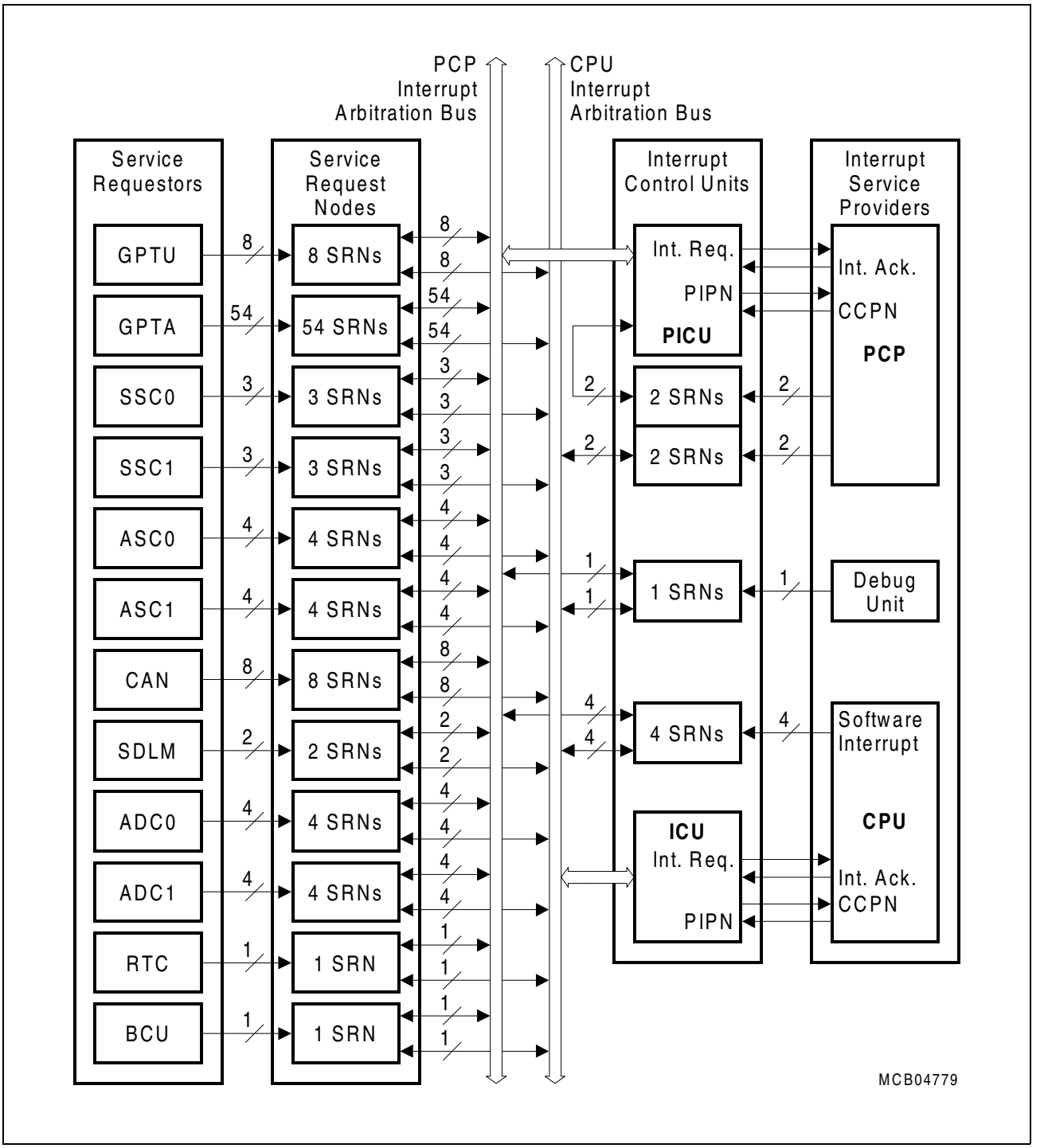


Figure 16 Block Diagram of the TC1775 Interrupt System

Note: Depending on the selected system frequency f_{SYS}, the number of clocks for interrupt arbitration cycles must be selected as follows:
$f_{SYS} \leq 30$ MHz: ICR.CONECYC = 1
$f_{SYS} > 30$ MHz: ICR.CONECYC = 0

Boot Options

The TC1775 booting schemes provides a number of different boot options for the start of code execution. **Table 5** shows the boot options available in the TC1775.

Table 5 Boot Selections

$\overline{\text{OCDSE}}$	$\overline{\text{BRKIN}}$	CFG [3]	CFG [2:0]	Type of Boot	Boot Source	Initial PC Value
1	1	X	000_B	Start from Boot ROM	Boot ROM	BFFF FFFC$_H$
			001_B			
			010_B			
		0	100_B	External memory as slave directly via EBU	External Memory (cached)	A000 0000$_H$
		1	100_B	External memory as master directly via EBU		
		0	101_B	External memory as slave via FPI Bus		
		1	101_B	External memory as master via FPI Bus		
		X	011_B 110_B 111_B	Reserved; don't use these combinations;		
0	1	0	100_B or 101_B	Go to halt with EBU enabled as slave	–	–
		1		Go to halt with EBU enabled as master		
		all other combina-tions		Go to halt with EBU disabled		
0	0	don't care		Go to external emulator space	–	BE00 0000$_H$
1	0	don't care		Tri-state chip (deep sleep)	–	–

Preliminary

Power Management System

The TC1775 power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application.

There are four power management modes:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Table 6 describes these features of the power management modes.

Table 6 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the $\overline{\text{NMI}}$ pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock continues to be distributed only to those peripherals programmed to operate in Sleep Mode. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the $\overline{\text{NMI}}$ pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.
Deep Sleep	The system clock is shut off; only an external signal will restart the system. Entering this state requires an orderly shut-down controlled by the Power Management State Machine (PMSM).

Preliminary

On-Chip Debug Support

The On-Chip Debug Support of the TC1775 consists of four building blocks:

- OCDS module in the TriCore CPU
  - On-chip breakpoint hardware
  - Support of an external break signal
- OCDS module in the PCP
  - Special DEBUG instruction for program execution tracing
- Trace module of the TriCore
  - Outputs 16 bits per cycle with pipeline status information, PC bus information, and breakpoint qualification information
- Debugger Interface (Cerberus)
  - Provided for debug purposes of emulation tool vendors
  - Accessible through a JTAG standard interface with dedicated JTAG port pins

Figure 17 shows a basic block diagram of the building blocks.

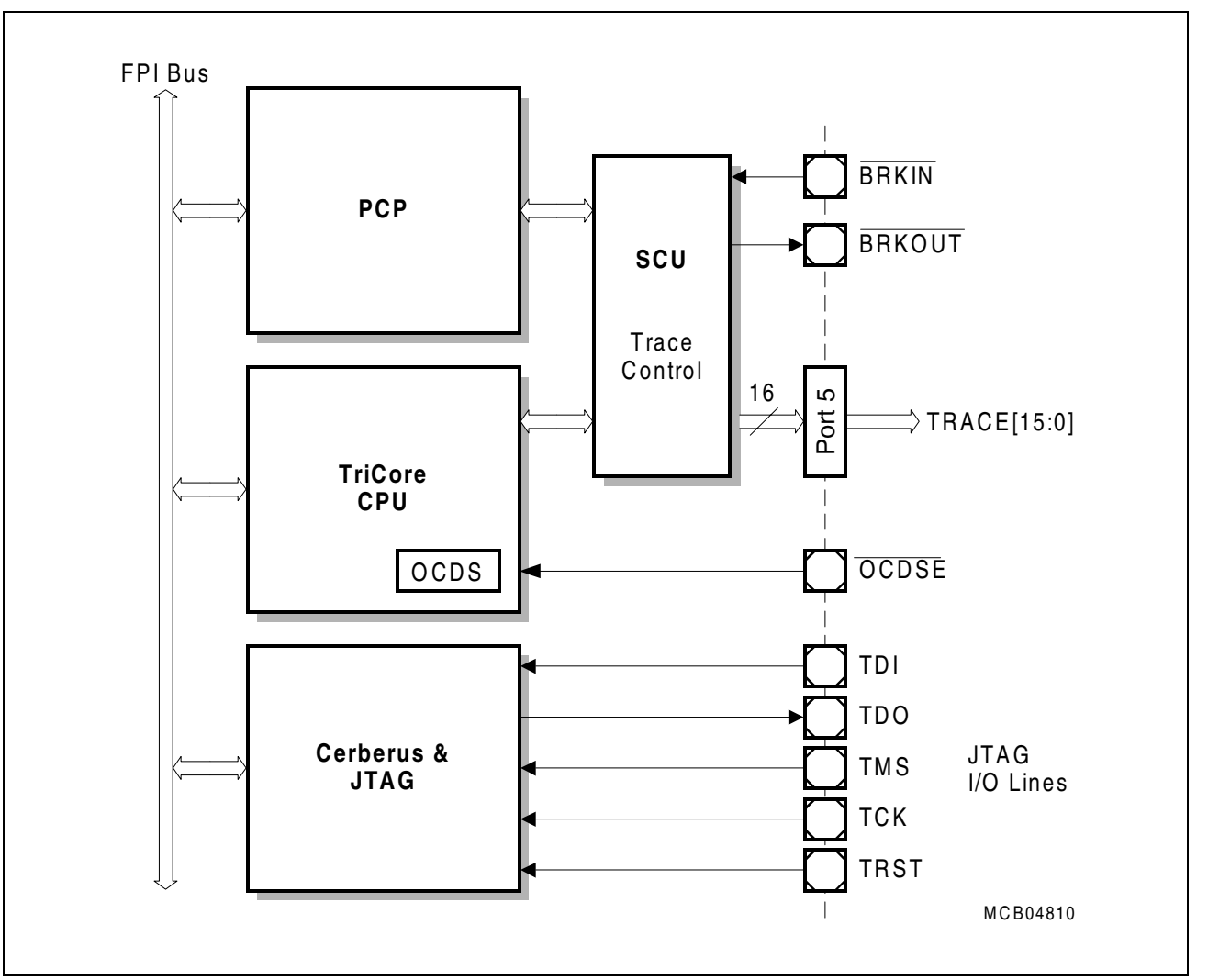


Figure 17 OCDS Support Basic Block Diagram

Clock Generation Unit

The Clock Generation Unit (CGU) in the TC1775, shown in **Figure 18**, consists of an oscillator circuit and a Phase-Locked Loop (PLL). The PLL can convert a low-frequency external clock signal to a high-speed internal clock for maximum performance. The PLL also has fail-safe logic that detects degenerate external clock behavior such as abnormal frequency deviations or a total loss of the external clock. It can execute emergency actions if it looses its lock on the external clock.

In general, the CGU is controlled through the System Control Unit (SCU) module of the TC1775.

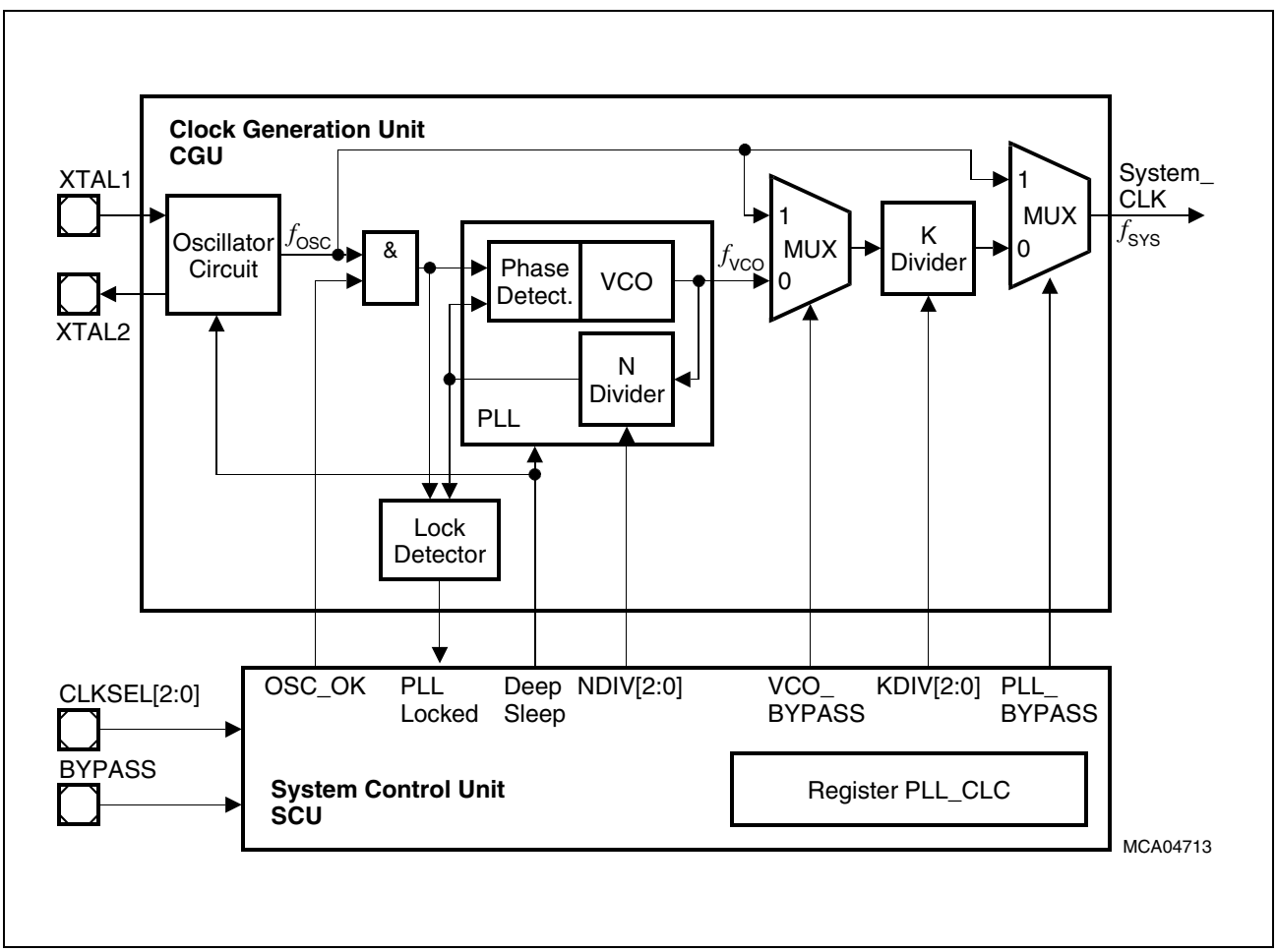


Figure 18 Clock Generation Unit Block Diagram

Besides the two XTAL pins for the oscillator, input pins CLKSEL[2:0] and BYPASS are used for configuration of the clock generation unit. These inputs are checked by the SCU which generates the appropriate control signals and latches the state of these signals into register PLL_CLC.

PLL Operation

The f_{VCO} clock of the PLL has a frequency which is a multiple of the externally applied clock f_{OSC}. The factor for this is controlled through the value N applied to the divider in the feedback path. N is defined through three PLL configuration inputs CLKSEL[2:0].

Table 7 Input Frequencies and N Factor for f_{VCO}

CLKSEL[2:0]	N-Factor	f_{VCO} = 150 MHz	f_{VCO} = 160 MHz	f_{VCO} = 200 MHz
000_B	8	18.75	20	25
001_B	9	16.67	17.76	22.22
010_B	10	15	16	20
011_B	11	13.64	14.55	18.18
100_B	12	12.5	13.33	16.67
101_B	13	11.54	12.31	15.38
110_B	14	10.71	11.43	14.29
111_B	15	10	10.67	13.33

Shaded combinations should not be used because the maximum oscillator frequency of 16 MHz is exceeded.

The K-Divider is a software controlled divider. **Table 8** lists the possible values for K and the resulting division factor.

Table 8 Output Frequencies f_{SYS} Derived from Various Output Factors

K-Factor		f_{SYS} [1]			Duty Cycle [%]
Selected Factor	KDIV	f_{VCO} = 150 MHz	f_{VCO} = 160 MHz	f_{VCO} = 200 MHz	
2	000_B	75	80	100	50
4	010_B	37.5	40	50	50
5[2]	011_B	30	32	40	40
6	100_B	24.5	26.67	33.33	50
8	101_B	18.75	20	25	50
9[2]	110_B	16.67	17.78	22.22	44
10	111_B	15	16	20	50
16	001_B	9.38	10	12.5	50

Shaded combinations cannot not be used because the maximum system clock frequency of 40 MHz is exceeded.

1) Depending on the selected system frequency f_{SYS}, the number of clocks for interrupt arbitration cycles must be selected as follows: $f_{SYS} \leq 30$ MHz: ICR.CONECYC = 1, $f_{SYS} > 30$ MHz: ICR.CONECYC = 0.

2) These odd K-Factors should not be used (not tested because of the unsymmetrical duty cycle).

Recommended Oscillator Circuits

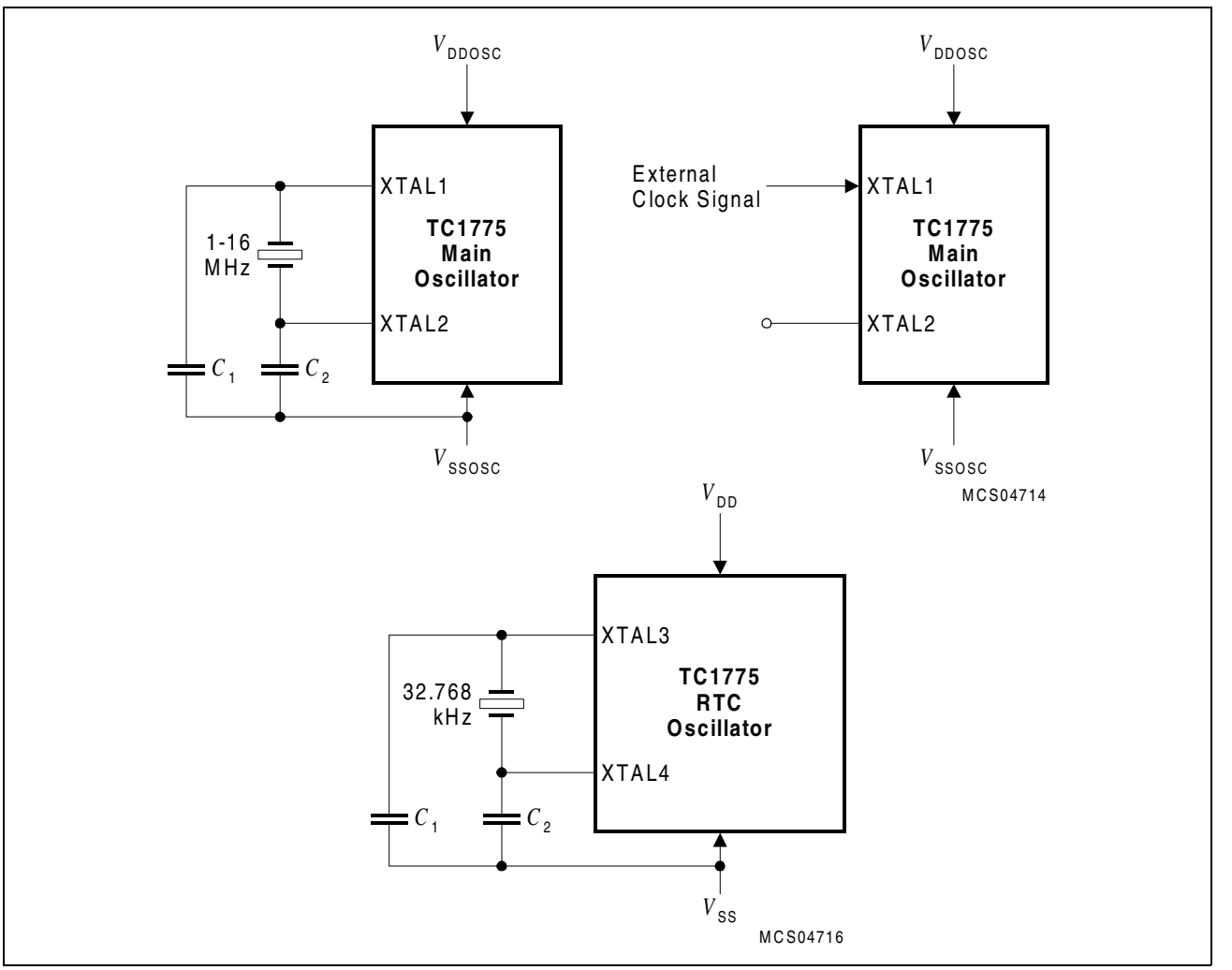


Figure 19 Oscillator Circuitries

For the main oscillator of the TC1775 the following external passive components are recommended:

- Crystal: max. 16 MHz
- C_1, C_2: 10 pF

A block capacitor between V_{DDOSC} and V_{SSOSC} is recommended, too.

For the RTC oscillator of the TC1775 the following external passive components are recommended:

- Crystal: 32.768 kHz
- C_1, C_2: 12 pF

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

Preliminary

Power Supply

Figure 20 shows the TC1775's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling. Also the operation margin is improved in sensitive modules like the A/D converter by noise reduction.

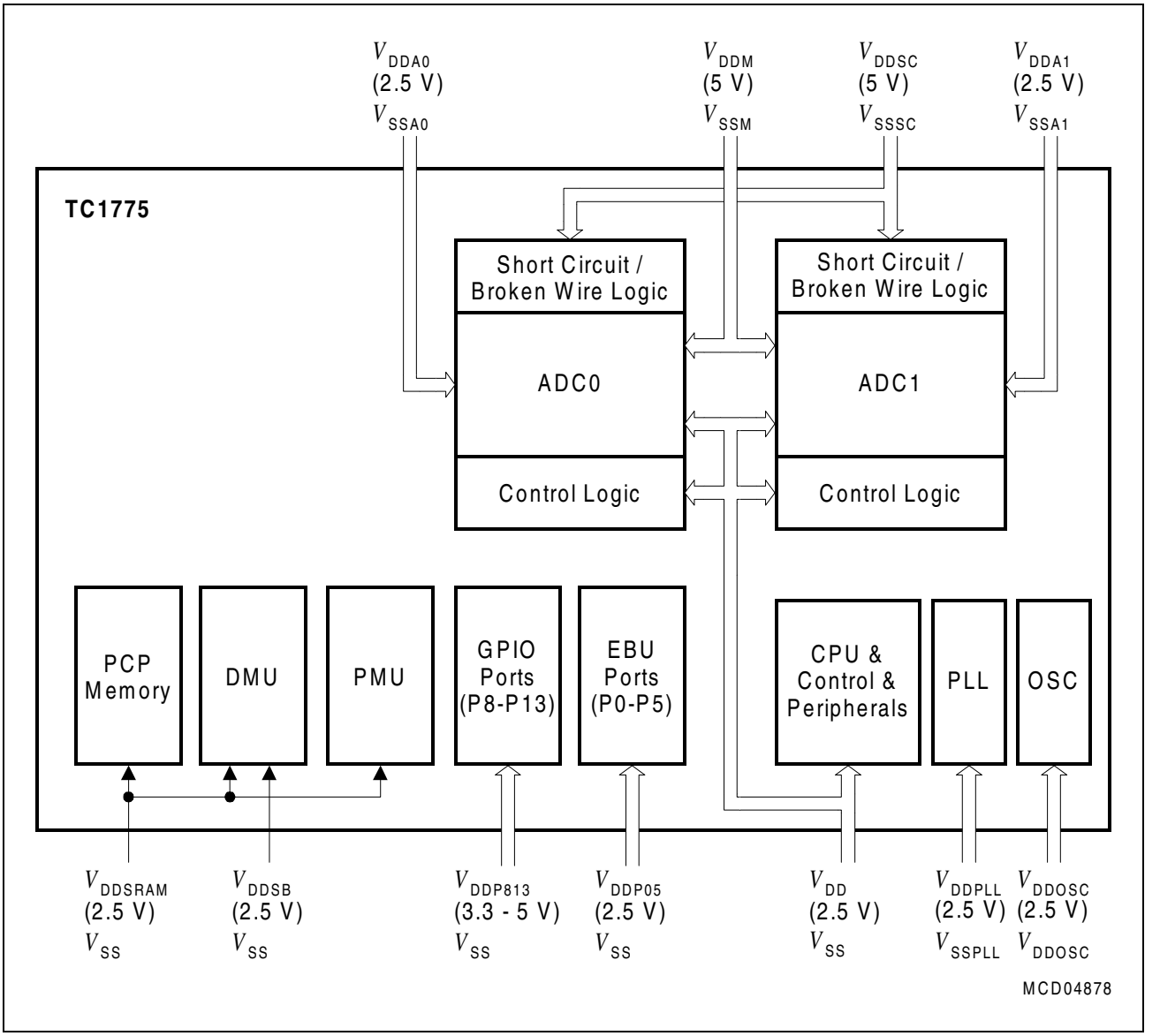


Figure 20 TC1775 Power Supply Concept

Preliminary

Ports Power Supply

The TC1775's port power supply concept is shown in **Figure 21**. The ports assigned with the External Bus Unit (EBU) are in a separate power supply group for 2.5 V nominal operating voltage. The general purpose input/outputs (GPIOs) except the EBU provide 3.3 to 5 V input/output acceptance and drive characteristics.

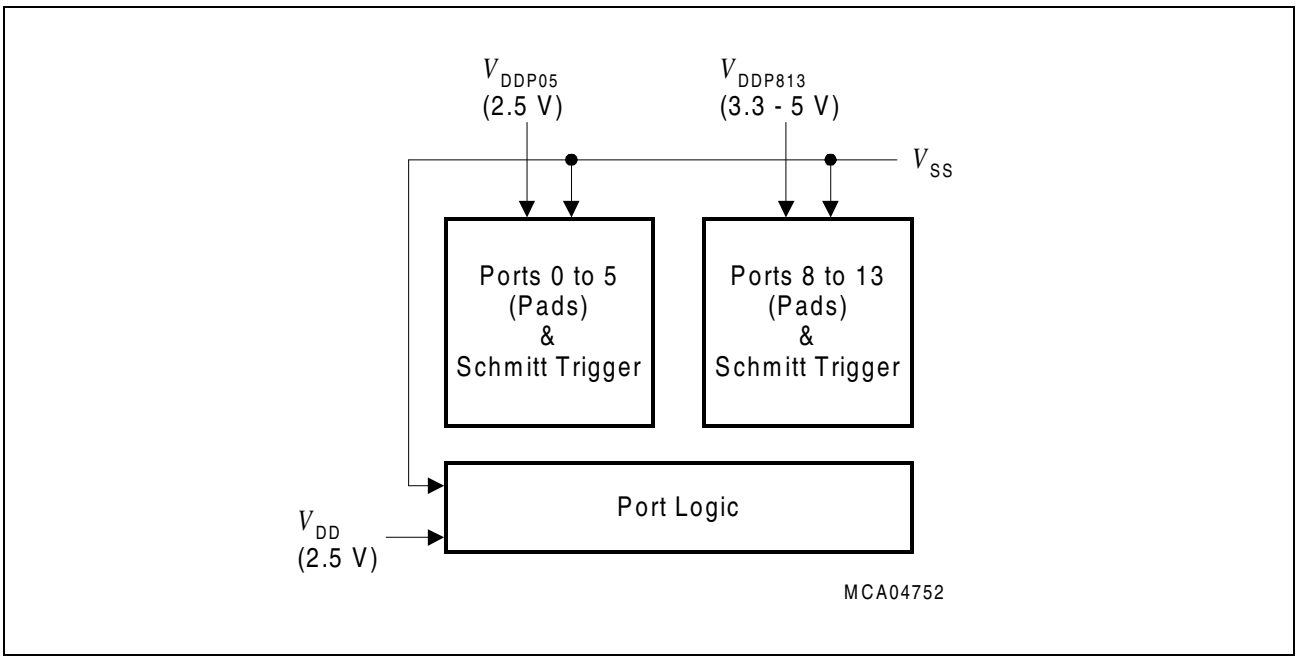


Figure 21 Ports Power Supply Concept

Power-up Sequence

During Power-up the reset pin $\overline{\text{PORST}}$ has to be held active until both power supply voltages have reached at least their minimum values.

During the Power-up time (rising of the supply voltages from 0 to their regular operating values) it has to be ensured, that the difference between V_{DDP813} and V_{DDI} (i.e. V_{DDP813} - V_{DDI}) never drops below -0.3 V (V_{DDI} = V_{DD} and V_{DDP05}).

Power Loss

If V_{DDP813} is dropping below V_{DDI}, external circuitry in the power supply has to ensure, that V_{DDI} is also limited to the same level.

If V_{DDI} is dropping below the operating range, V_{DDP813} may stay active.

Powering Down

During powering down (falling of the supply voltages from their regular operating values to zero), it has to be ensured, that the difference between V_{DDP813} and V_{DDI} (V_{DDP813} - V_{DDI}) never drops below -0.3 V.

Preliminary

Identification Register Values

Table 9 TC1775 Identification Registers

Short Name	Address	Value
PMU_ID	C7FF FF08$_H$	0006 C002$_H$
DMU_ID	D7FF FF08$_H$	0007 C002$_H$
SCU_ID	F000 0008$_H$	0003 C002$_H$
MANID	F000 0070$_H$	0000 1820$_H$
CHIPID	F000 0074$_H$	0000 8002$_H$
RTID	F000 0078$_H$	0000 0000$_H$
RTC_ID	F000 0108$_H$	0000 5A01$_H$
BCU_ID	F000 0208$_H$	0000 6A05$_H$
STM_ID	F000 0308$_H$	0000 C002$_H$
JPD_ID	F000 0408$_H$	0000 6301$_H$
EBU_ID	F000 0508$_H$	0005 C002$_H$ (BA11-Step)
		0005 C003$_H$ (BA21-Step)
GPTU_ID	F000 0708$_H$	0001 C002$_H$
ASC0_ID	F000 0808$_H$	0000 4401$_H$
ASC1_ID	F000 0908$_H$	0000 4401$_H$
SSC0_ID	F000 0A08$_H$	0000 4503$_H$
SSC1_ID	F000 0B08$_H$	0000 4503$_H$
GPTA_ID	F000 1808$_H$	0002 C001$_H$
ADC0_ID	F000 2208$_H$	0000 3101$_H$
ADC1_ID	F000 2408$_H$	0000 3101$_H$
SDLM_ID	F000 2608$_H$	0000 4202$_H$
PCP_ID	F000 3F08$_H$	000D C001$_H$
CAN_ID	F010 0008$_H$	0000 4110$_H$
CPU_ID	FFFE FF08$_H$	0000 0202$_H$

Preliminary

Parameter Interpretation

The parameters listed on the following pages partly represent the characteristics of the TC1775 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):

The logic of the TC1775 will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):

The external system must provide signals with the respective timing characteristics to the TC1775.

Pin Classes

The TC1775 has three classes of digital I/O pins:

- **Class A** pins, which are 3.3 V to 5 V nominal voltage pins
- **Class B** pins, which are 2.5 V nominal voltage pins (input tolerant for 3.3 V)
- **Class C** pins, which are 2.5 V nominal voltage pins only

Table 10 shows the assignments of all digital I/O pins to pin classes and to V_{DD} power supply pins.

Table 10 Assignments of Digital Pins to Pin Classes and Power Supply Pins

Pins	Pin Classes	Power Supply	
Port 8 to Port 13 CLKSEL[2:0], BYPASS, CFG[3:0], $\overline{\text{HDRST}}$	Class A (nominal 3.0 to 5.25 V)	V_{DDP813}	V_{SS}
Port 0 to 5 $\overline{\text{TRST}}$, TCK, TDI, TDO, TMS, $\overline{\text{ODCSE}}$, $\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$, $\overline{\text{NMI}}$, $\overline{\text{PORST}}$, CLKOUT, CLKIN $\overline{\text{TESTMODE}}$	Class B (nominal 2.5 V, 3.3 V tolerant)	V_{DDP05}	
Core supply, no pins assigned	(nominal 2.5 V)	V_{DD}, V_{DDSRAM}, V_{DDSB}	
		V_{DDPLL}	V_{SSPLL}
XTAL1, XTAL2, XTAL3, XTAL4	Class C (nominal 2.5 V)	V_{DDOSC}	V_{SSOSC}

Preliminary

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_A	-65	150	°C	–
Junction temperature	T_J	–	150	°C	under bias
Voltage on Class A power supply pins with respect to V_{SS}	V_{DD}	-0.5	6.2	V	see Table 10
Voltage on Class B and C power supply pins with respect to V_{SS}	V_{DD}	-0.5	3.25	V	–
Voltage on power supply pins “no pins assigned” with respect to V_{SS}	V_{DD}	-0.5	3.25	V	–
Voltage on any Class A input pin with respect to V_{SS}	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Voltage on any Class B input pin with respect to V_{SS}	V_{IN}	-0.5	3.7	V	–
Voltage on any Class C input pin with respect to V_{SS}	V_{IN}	-0.5	V_{DDOSC} + 0.5	V	–
Input current on any pin during overload condition	I_{IN}	-10	10	mA	–
Absolute sum of all input currents during overload condition	ΣI_{IN}	–	|100|	mA	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Preliminary

Package Parameters (P-BGA-329)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Power dissipation	P_{DISS}	–	1	W	–
Thermal resistance	R_{THA}	–	23	K/W	Chip to ambient

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1775. All parameters specified in the following table refer to these operating conditions, unless otherwise noticed.

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage[1]	V_{DDP813}	3.0	5.25	V	Class A pins
	V_{DD}[2]	2.3	2.75	V	CPU Core and Class B pins
	V_{DDOSC}	2.3	2.75	V	Class C pins
	V_{DDSB}[3]	2.25	2.75	V	–
Digital ground voltage	V_{SS}	0		V	–
Ambient temperature under bias	T_A	-40	+125	°C	–
Analog supply voltages	V_{DDA}	2.25	2.75	V	–
	V_{DDM}	4.5	5.25	V	–
Analog reference voltage	V_{AREF}	4	V_{DDM} + 0.05	V	4)
Analog ground voltage	V_{AGND}	V_{SSA} - 0.05	V_{SSA} + 0.05	V	5)
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	–
CPU clock	f_{SYS}	–	40	MHz	–
Overload current	I_{OV}	-10	10	mA	6)7)8)
Short circuit current	I_{SC}	-10	10	mA	3)4)9)
Absolute sum of overload + short circuit currents	$\Sigma\|I_{OV}\| + \|I_{SC}\|$	–	|50|	mA	7)
External load capacitance	C_L	–	50	pF	–

1) Digital supply voltages applied to the TC1775 must be static regulated voltages which allow a typical voltage swing of ±10%.

2) This V_{DD} specification is applicable for the power supply pins: V_{DD}, V_{DDOSC}, V_{DDPLL}, V_{DDSRAM}, V_{DDP05}, and V_{DDSB}. In order to minimize the danger of latch-up conditions, these 2.5 V V_{DD} power supply pins should be kept at the same voltage level during normal operating mode. This condition is typically achieved by generating the 2.5 V power supplies from a single voltage source. The condition is also valid in normal operating mode if a separate stand-by power supply V_{DDSB} is used.

3) The minimum voltage at pin V_{DDSB} during TC1775 power down mode is 1.8 V in order to keep the contents of SBRAM valid. The core power supply V_{DD} must be below the standby power supply $V_{DD} < V_{DDSB} + 0.3$ V.

4) The value of V_{AREF} is permitted to be within the range of $V_{SSA} - 0.05$ V < V_{AREF} < $V_{DDM} + 0.05$ V. The value specified for the total unadjusted error (TUE) is not guaranteed while the V_{AREF} is out of the specified range.

5) The value of V_{AGND} is permitted to be within the range of $V_{SSA} - 0.05$ V < V_{AGND} < $V_{DDM} + 0.05$ V. The value specified for the total unadjusted error (TUE) is not guaranteed while the V_{AGND} is out of the specified range.

6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD} + 0.5$ V or $V_{OV} < V_{SS} - 0.5$ V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

7) Not 100% tested, guaranteed by design and characterization.

8) Applicable for analog inputs.

9) Applicable for digital inputs.

Preliminary

DC Characteristics

Input/Output DC-Characteristics

V_{SS} = 0 V; T_A = -40 °C to +125 °C;

Parameter[1]	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Class A Pins (V_{DDP813} = 3.0 to 5.25 V)						
Output low voltage[2]	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA[3] I_{OL} = 600 µA[4] V_{DDP813} = 4.5 to 5.25 V
				0.2 × V_{DDP813}	V	I_{OL} = 2.4 mA I_{OL} = 600 µA[4] V_{DDP813} = 3.0 to 4.49 V
Output high voltage[2]	V_{OH}	CC	0.7 × V_{DDP813}	–	V	I_{OH} = -2.4 mA I_{OH} = -600 µA[4] V_{DDP813} = 4.5 to 5.25 V
					V	I_{OH} = -2.4 mA I_{OH} = -600 µA[4] V_{DDP813} = 3.0 to 4.49 V
Input low voltage[5]	V_{IL}	SR	-0.5	0.8	V	V_{DDP813} = 4.5 to 5.25 V (TTL)
				0.43 × V_{DDP813}	V	V_{DDP813} = 4.5 to 5.25 V (CMOS)
				0.2 × V_{DDP813}	V	V_{DDP813} = 3.0 to 4.49 V (CMOS)
Input high voltage[5]	V_{IH}	SR	2.0	V_{DDP813} + 0.5	V	V_{DDP813} = 4.5 to 5.25 V (TTL)
			0.73 × V_{DDP813}		V	V_{DDP813} = 3.0 to 5.25 V (CMOS)
Pull-up current[6]	I_{PUH}	CC	–	10	µA	V_{OUT} = V_{DDP813} - 0.02 V
	I_{PUL}	CC	-120	–	µA	V_{OUT} = 0.5 × V_{DDP813}
Pull-down current[7]	I_{PDL}	CC	10	–	µA	V_{OUT} = 0.02 V
	I_{PDH}	CC	–	120	µA	V_{OUT} = 0.5 × V_{DDP813}

Preliminary

Input/Output DC-Characteristics (cont'd)
V_{SS} = 0 V; T_A = -40 °C to +125 °C;

Parameter[1]	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Class B Pins (V_{DDP05} = 2.30 to 2.75 V)						
Output low voltage	V_{OL}	CC	–	0.2 × V_{DDP05}	V	I_{OL} = 2.4 mA
				0.45		I_{OL} = 600 µA
Output high voltage	V_{OH}	CC	0.7 × V_{DDP05}	–	V	I_{OH} = -2.4 mA
			0.9 × V_{DDP05}	–	V	I_{OH} = -600 µA
Input high voltage	V_{IH}	SR	0.7 × V_{DDP05}	3.7	V	–
Input low voltage	V_{IL}	SR	-0.5	0.2 × V_{DDP05}	V	–
Pull-up current[6]	I_{PUH}	CC	–	10	µA	V_{OUT} = V_{DDP05} - 0.02 V
	I_{PUL}	CC	-60	–	µA	V_{OUT} = 0.5 × V_{DDP05}
Pull-down current[7]	I_{PDL}	CC	10	–	µA	V_{OUT} = 0.02 V
	I_{PDH}	CC	–	60	µA	V_{OUT} = 0.5 × V_{DDP05}
Class A and B Pins						
Input Hysteresis	HYS	CC	0.065 × V_{DDPx}[8]	–	V	TTL and CMOS[9]
Input leakage current (Digital I/O)	I_{OZ2}	CC	–	±500	nA	0 V < V_{IN} < V_{DDPx}[8]
Peak short-circuit current Peak back-drive current (per digital pin) Peak time & period time[10][11]	$I_{SCBDpeak}$	SR	–	±20	mA	[12][9]

Preliminary

Input/Output DC-Characteristics (cont'd)

V_{SS} = 0 V; T_A = -40 °C to +125 °C;

Parameter[1)]	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Constant short-circuit current Constant back-drive current (per digital pin)	$I_{SCBDcons}$	SR	–	±10	mA	12)9)
Pin capacitance[9)] (Digital I/O)	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C

Class C Pins (V_{DDOSC} = 2.30 to 2.75 V), see Page 76

1) All Class A pins of the TC1775 are equipped with Low-Noise output drivers, which significantly improve the device's EMI performance. These Low-Noise drivers deliver their maximum current only until the respective target output level is reached. After that the output current is reduced. This results in an increased impedance of the driver, which attenuates electrical noise from the connected PCB tracks. The current, which is specified in column "Test Conditions", is delivered in any case.

2) This specification is not valid for outputs of GPIO lines, which are switched to open drain mode. In open drain mode the output will float and the voltage results from the external circuitry.

3) Output drivers in high current mode.

4) Condition for output driver in dynamic current mode & low current mode – guaranteed by design characterization.

5) Input characteristics can be switched between TTL and CMOS via register Px_PICON except for dedicated pins which have CMOS input characteristics.

6) The maximum current can be drawn while the respective signal line remains inactive.

7) The minimum current must be drawn in order to drive the respective signal line active.

8) In case of Class B pins $V_{DDx} = V_{DDP05}$. In case of Class A pins $V_{DDx} = V_{DDP813}$.

9) Guaranteed by design characterization.

10) The max. peak-short-circuit current resp. max. peak-back-drive current is limited by max. 20 mA and the peak period equivalent of 10 mA constant-short-circuit current resp. 10 mA constant-back-drive current. The integral of $I_{SCBDpeak}$ over the peak period is thus limited to 10 mA (provided: $I_{SCBDpeak} \leq 20$ mA).

11) To be defined for Class B pads.

12) Short-circuit or back-drive conditions during operation occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{SCBD} > V_{DDPx}$ **+ 0.5 V or** $V_{SCBD} < V_{SS}$ **- 0.5 V**) or a short circuit condition occurs on the respective pin. The absolute sum of input I_{SCBD} and I_{OV} currents on all port pins must not exceed **100 mA** at any time. The supply voltage (V_{DDPx} and V_{SS}) must remain within the specified limits. Under short-circuit conditions the corresponding pin is not ready for use. In case of Class B pins $V_{DDx} = V_{DDP05}$. In case of Class A pins $V_{DDx} = V_{DDP813}$.

Preliminary

Pull-Up/Pull-Down Characteristics

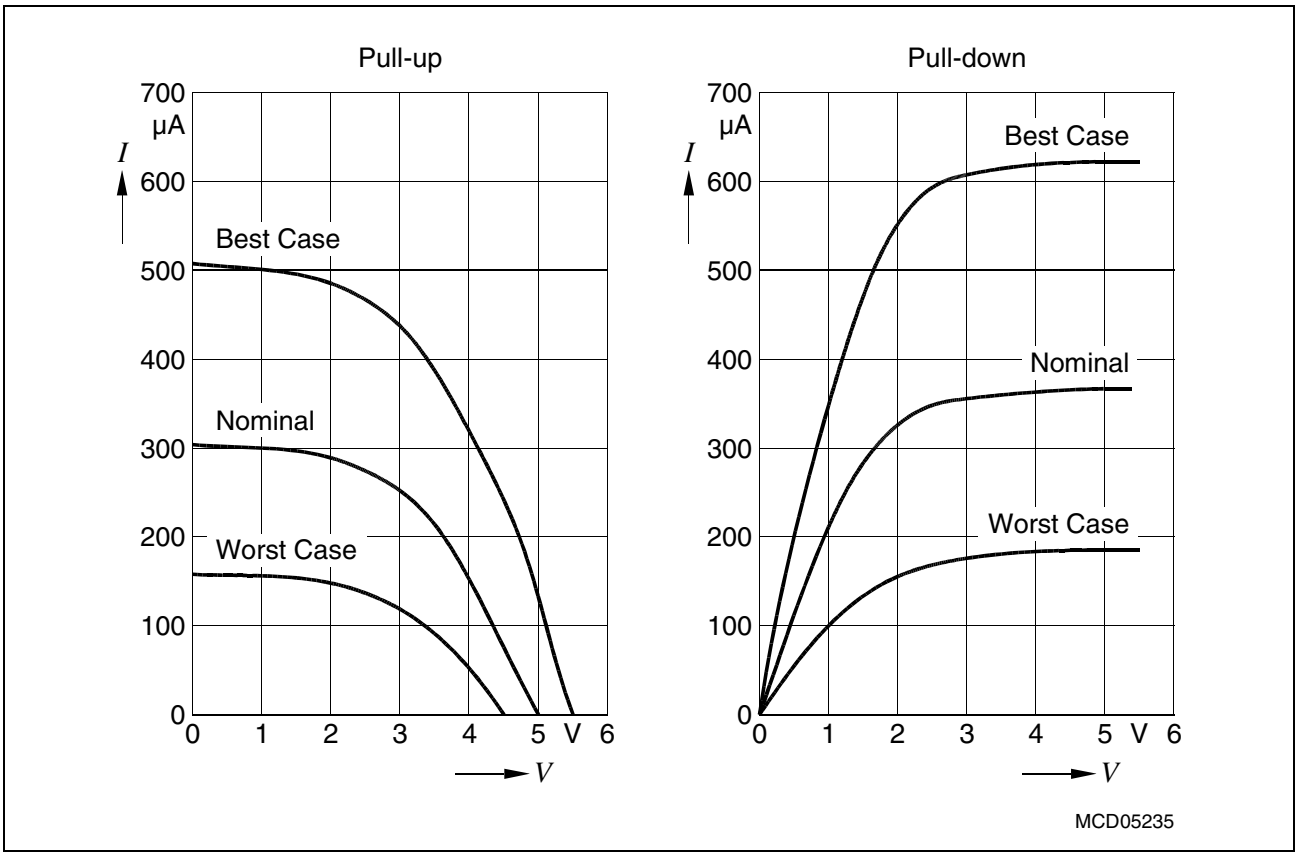


Figure 22 Pull-Up/Pull-Down Characteristics of Class A Pins

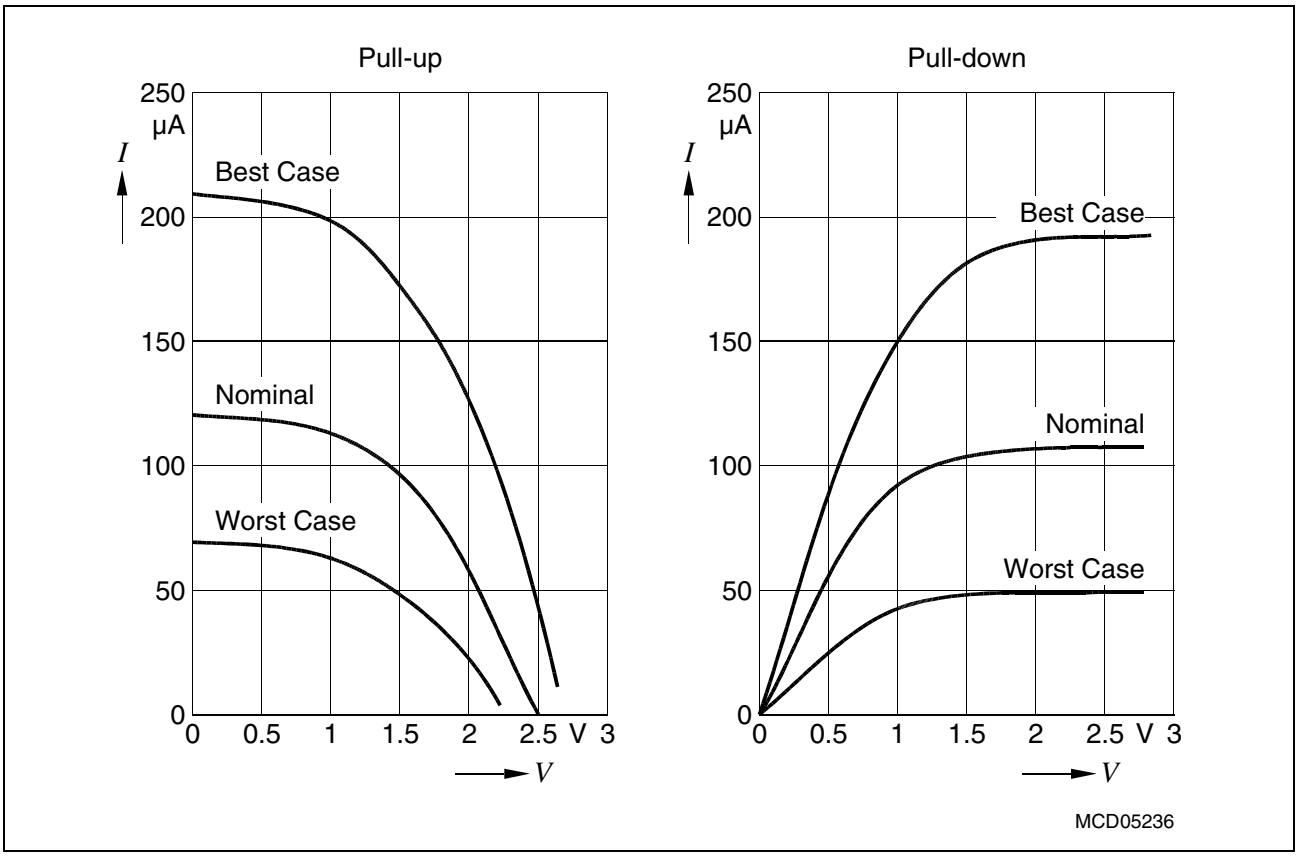


Figure 23 Pull-Up/Pull-Down Characteristics of Class B Pins

*Note: The pull-up/pull-down characteristics as shown in **Figure 22** and **Figure 23** are guaranteed by design characterization.*

Preliminary

AD Converter Characteristics

T_A = -40 °C to +125 °C; V_{SS} = 0 V;

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Analog supply voltages	V_{DDAx}	SR	2.25	2.5	2.75	V	1)
	V_{DDM}	SR	4.5	5	5.25	V	–
	V_{DDSC}	SR	V_{DDM} - 0.05	–	V_{DDM} + 0.05	V	–
Analog ground voltage	V_{SSAx}	SR	-0.1	–	0.1	V	2)
Analog reference voltage	V_{AREFx}	SR	4	–	V_{DDM} + 0.05	V	3)
Analog reference ground	V_{AGNDx}	SR	V_{SSAx} - 0.05	–	V_{SSAx} + 0.05	V	4)
Analog input voltage range	V_{AIN}	SR	V_{AGNDx}	–	V_{AREFx}	V	–
Internal ADC clock	f_{ANA}		0.5	–	2	MHz	–
Power-up calibration time	t_{PUC}		–	–	3328 × (3 + CON.CPS) × t_{BC}	µs	–
Sample time	t_S	CC	(3 + CON.CPS) × (CHCONn.STC + 2) × t_{BC}			µs	5)
			6 × t_{BC}	–	–	µs	
Conversion time	t_C	CC	t_S + (30 + CON.CPS × 4) × t_{BC} + 2 × t_{DIV}			µs	for 8-bit conv.5)
			t_S + (36 + CON.CPS × 4) × t_{BC} + 2 × t_{DIV}			µs	for 10-bit conv.5)
			t_s + (42 + CON.CPS × 4) × t_{BC} + 2 × t_{DIV}			µs	for 12-bit conv.5)
Total unadjusted error	TUE6)	CC	–	–	±1	LSB	for 8-bit conv.
			–	–	±2	LSB	for 10-bit conv.
			–	–	±6	LSB	for 12-bit conv.
Overload current7)	I_{AOV1}8)	CC	-2	–	+5	mA	–
			-2		0	mA	$k_A = 1.0 \times 10^{-3}$
			0		+5	mA	$k_A = 1.0 \times 10^{-4}$
	I_{AOV2}9)	CC	-4	–	+10	mA	–
			-4		0	mA	$k_A = 1.0 \times 10^{-3}$
			0		+10	mA	$k_A = 1.0 \times 10^{-4}$

Preliminary

AD Converter Characteristics (cont'd)

T_A = -40 °C to +125 °C; V_{SS} = 0 V;

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Overload coupling factor[10]	k_A	CC	–	–	1.0×10^{-3}	–	see I_{AOV1} and I_{AOV2}
					1.0×10^{-4}	–	
Input leakage current at analog inputs	I_{OZ1}	CC	–	–	±200	nA	0 V < V_{IN} < V_{DDA}[1]
Input leakage current at V_{AGND} and V_{AREF}	I_{OZ2}	CC	–	–	±500	nA	0 V < V_{IN} < V_{DDA}[1]
Switched cap. at the positive reference voltage input	C_{AREFSW}	CC	–	15	20	pF	[11]
Switched cap. at the negative reference voltage input	C_{AGNDS}	CC	–	15	20	pF	[11]
Total cap. at the analog voltage input	C_{AINTOT}	CC	–	12	15	pF	–
Switched cap. at the analog voltage input	C_{AINSW}	CC	–	–	10	pF	[12]
ON resistance of the transmission gates in the analog voltage path	R_{AIN}	CC	–	–	0.7	kΩ	–

1) V_{DDAx} = V_{DDA0} for A/D Converter ADC0 and V_{DDAx} = V_{DDA1} for A/D Converter ADC1.

2) V_{SSAx} = V_{SSA0} for A/D Converter ADC0 and V_{SSAx} = V_{SSA1} for A/D Converter ADC1.

3) The value of V_{AREF} is permitted to be within the range of V_{SSA} - 0.05 V < V_{AREF} < V_{DDM} + 0.05 V. The value specified for the total unadjusted error (TUE) is not guaranteed while the V_{AREF} is out of the specified range.

4) The value of V_{AGND} is permitted to be within the range of V_{SSA} - 0.05 V < V_{AGND} < V_{DDM} + 0.05 V. The value specified for the total unadjusted error (TUE) is not guaranteed while the V_{AGND} is out of the specified range.

5) Definitions for CPS, STC, t_{BC} and t_{DIV} see **Figure 25**.

6) TUE is tested at V_{AREF} = 5 V, V_{AGND} = 0 V and V_{DDM} = 4.9 V.

7) Analog overload conditions during operation occur if the voltage on the respective ADC pin exceeds the specified operating range (i.e. V_{AOV} > V_{DDM} **+ 0.5 V or** V_{AOV} < V_{SSM} **- 0.5 V**) or a short circuit condition occurs on the respective ADC pin. The absolute sum of input currents on all port pins must not exceed **10 mA** at any time. The supply voltage (V_{DD}, V_{DDA0}, V_{DDA1} and V_{SS}, V_{SSA0}, V_{SSA1}) must remain within the specified limits. Under short-circuit conditions the corresponding pin is not ready for use.

8) Applies for one analog input pin.

9) Applies for two adjacent analog input pins.

10) The overload coupling factor (k_A) defines the worst case relation of an overload condition (I_{OV}) at one pin to the resulting leakage current (I_{leak}) into an adjacent pin: $|I_{leak}| = k_A \times |I_{OV}|$.
Thus under overload conditions an additional error leakage voltage (U_{AEL}) will be induced onto an adjacent analog input pin due to the resistance of the analog input source (R_{AIN}). That means $U_{AEL} = R_{AIN} \times |I_{leak}|$.
See also section 7.1.6 “Error Through Overload Conditions” in the TC1775 Peripheral Units User’s Manual for further explanations.

11) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage. Alternatively, the redistributed charge could be specified.

12) The switched capacitance at the analog voltage input must be charged within the sampling time. Alternatively, the redistributed charge could be specified.

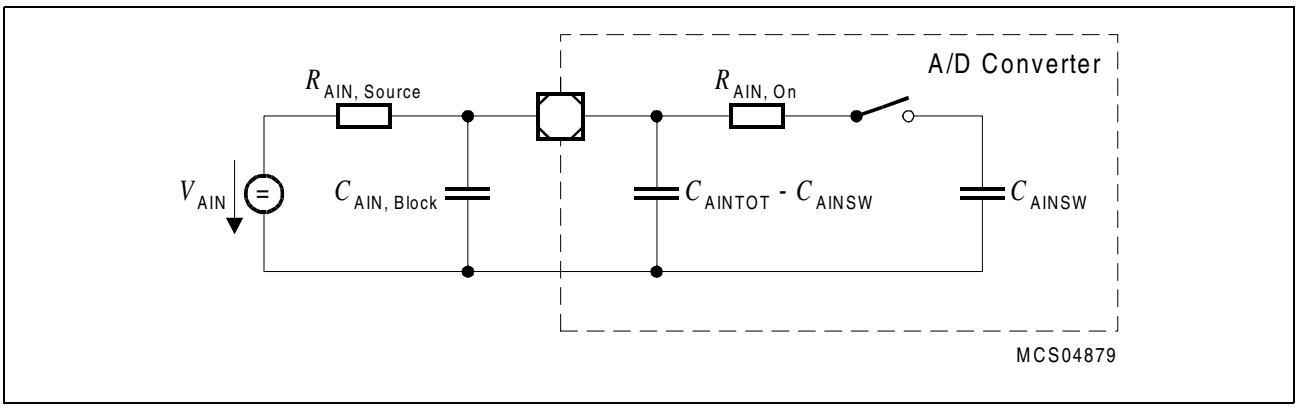


Figure 24 Equivalent Circuitry of Analog Input

Note: This equivalent circuitry for an analog input is also valid for the reference inputs V_{AREF} and V_{AGND}.

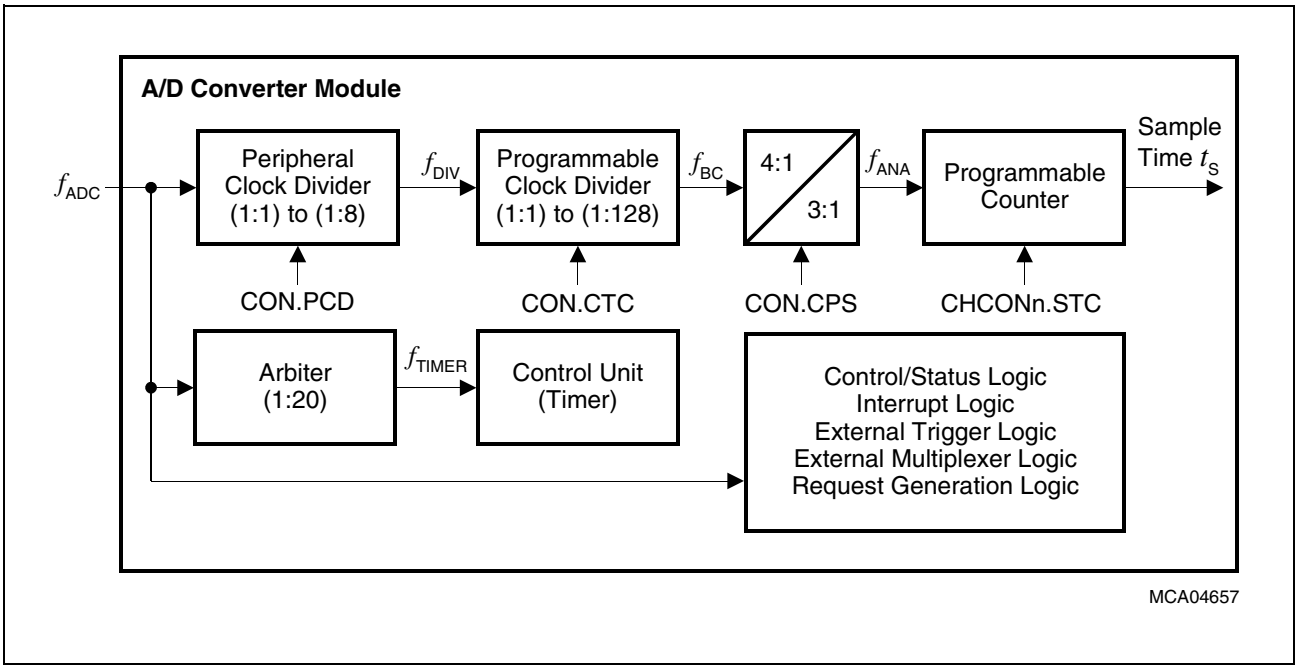


Figure 25 ADC Clock Circuit

Note: The frequency of f_{ADC} is the system clock frequency (f_{SYS}) divided by the value of bit field ADCx_CLC.RMC.

Oscillator Pins (Class C Pins)

T_A = -40 °C to +125 °C; V_{DDOSC} = 2.30 to 2.75 V; V_{SSOSC} = 0 V;

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Input low voltage at XTAL1, XTAL3	V_{ILX}	SR	-0.5	0.3 × V_{DDOSC}	V	–
Input high voltage at XTAL1, XTAL3	V_{IHX}	SR	0.7 × V_{DDOSC}	V_{DDOSC} + 0.5	V	–
Input current at XTAL1	I_{IX1}	CC	–	±20	µA	0 V < V_{IN} < V_{DDOSC}
Input current at XTAL3	I_{IX3}	CC	–	±0.5	µA	0 V < V_{IN} < V_{DDOSC}
Input leakage current XTAL1, XTAL3[1)]	I_{OZ}	CC	–	±200	nA	0 V< V_{IN} < V_{DDOSC}

1) Only applicable in deep sleep mode.

Preliminary

Power Supply Current

T_A = -40 °C to +125 °C;

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.[1]	max.		
Active mode supply current	I_{DD}	CC	–	–	250	mA	$\overline{PORST}$ = V_{IL}[2)3)]
			–	266	320	mA	Sum of I_{DDS}[4)]
			–	36	–	mA	I_{DD} at V_{DDP05}[4)]
			–	4	–	mA	I_{DD} at V_{DDP813}[4)]
			–	219	–	mA	I_{DD} at V_{DD} and V_{DDSRAM}[4)]
			–	3[4)]	80[5)]	mA	I_{DD} at V_{DDSB}
			–	4	–	mA	I_{DD} at V_{DDSC} and V_{DDAx}[4)]
Idle mode supply current	I_{ID}	CC	–	80	200	mA	$\overline{PORST}$ = V_{IH}[1)2)6)7)]
Sleep mode supply current	I_{SL}	CC	–	50	160	mA	$\overline{PORST}$ = V_{IH}[1)2)7)]
Deep sleep mode supply current	I_{DS}	CC	–	4	1000	µA	$\overline{PORST}$ = V_{IH}[8)]
Stand-by pin power supply current	I_{SB}	CC	–	1	200	µA	I_{DD} at V_{DDSB}[9)]
			–	1	120	µA	[10)]

1) Parameters in this column are tested at 25 °C, 40 MHz system clock (if applicable) and nominal V_{DD} voltages.

2) These parameters are tested at V_{DDmax} and 40 MHz system clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

3) These power supply currents are defined as the sum of all currents at the V_{DD} power supply lines: V_{DD} + V_{DDP05} + V_{DDP813} + V_{DDSRAM} + V_{DDSB} + V_{DDPLL} + V_{DDOSC} + V_{DDSC} + V_{DDM} + V_{DDA0} + V_{DDA1}

4) These power consumption characteristics are measured while running a typical application pattern. The power consumption of modules can increase or decrease using other application programs. The PLL is inactive during this measurement.

5) This parameter has been evaluated at design characterization using an untypical test pattern that makes extensive usage of the SBSRAM.

6) All peripherals are enabled and in idle state.

7) Guaranteed by design characterization.

8) I_{DS} is the sum of all power supply currents except V_{DDSB}.

9) TC1775 in deep sleep mode.

10) All other V_{DD} pins are at 0V; T_J = 150 °C; V_{DDSB} = 2.0 V.

Preliminary

AC Characteristics

Output Rise/Fall Times

Class A drivers (GPIO/peripheral ports 8 to 13): V_{DDP813} = 4.5 to 5.25 V; V_{SS} = 0 V

Class B drivers (Bus interface ports 0 to 5): V_{DDP05} = 2.30 to 2.75 V; V_{SS} = 0 V

T_A = -40 °C to +125 °C, unless otherwise noted; f_{SYS} = 40 MHz

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Class A Pins						
Nominal output rise/ fall time[1)]	t_{RFAnom} CC	–	5	–	ns	T_A = 25 °C, C_L = 50 pF, V_{DDP813} = 5.0 V Px_POCON.PEC = 00_B Px_POCON.PDC = $0X_B$
Maximal output rise/ fall time[1)]	t_{RFAmax} CC	–	–	12	ns	C_L = 50 pF Px_POCON.PEC = 00_B Px_POCON.PDC = $0X_B$
Slow output rise/fall time[1)]	$t_{RFAslow}$ CC	–	–	55	ns	C_L = 100 pF Px_POCON.PEC = 01_B Px_POCON.PDC = $0X_B$
Class B Pins						
Output rise/fall time[1)]	t_{RFBmax} CC	–	–	4	ns	for CLKOUT C_L = 50 pF
		–	–	7	ns	for all Class B pins except CLKOUT C_L = 50 pF

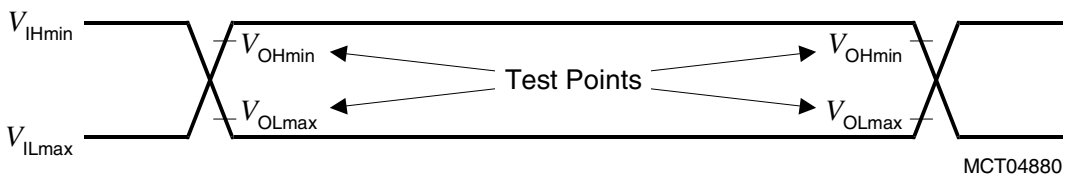
1) Measured from 10% output level to 90% output level and vice versa.

Preliminary

Testing Waveforms

T_A = -40 °C to +125 °C; Frequency: max. 40 MHz;

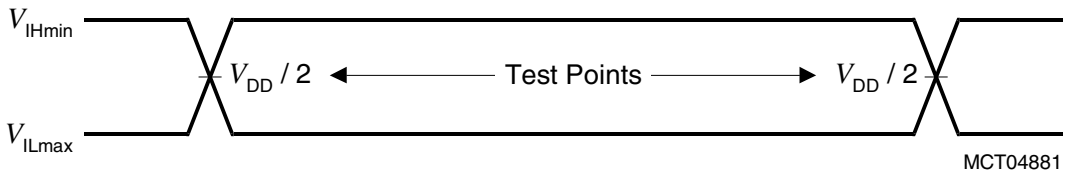
Class A Pins: V_{DDP813} = 3.0 to 5.25 V; V_{SS} = 0 V;



AC inputs during testing are driven with V_{IHmin} for a logic 1 and V_{ILmax} for a logic 0. Timing measurements are made at V_{OHmin} for a logic 1 and V_{OLmax} for a logic 0. Input and Output Low/High max./min. voltages are defined at **Page 68**.

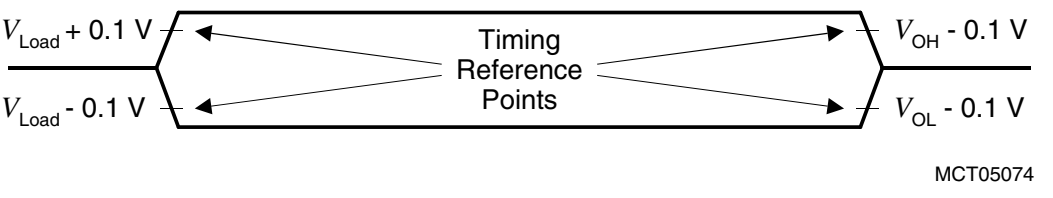
Figure 26 Testing Waveforms for Class A Pins

Class B and Class C Pins: V_{DD} = 2.30 to 2.75 V; V_{SS} = 0 V;
V_{DDOSC} = 2.30 to 2.75 V; V_{SSOSC} = 0 V;



AC inputs during testing are driven with V_{IHmin} for a logic 1 and V_{ILmax} for a logic 0. Timing measurements are made at V_{DD}/2 for a logic 1 and for a logic 0. Input Low/High max./min. voltages are defined at **Page 69** and **Page 76**.

Figure 27 Testing Waveforms for Class B and Class C Pins



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 15 mA).

Figure 28 Tri-State Testing Waveforms for Class B Pins

Preliminary

Input Clock Timing

V_{DDOSC} = 2.30 to 2.75 V; V_{SSOSC} = 0 V; T_A = -40 °C to +125 °C;

Parameter		Symbol	Limit Values		Unit
			min.	max.	
Oscillator clock frequency	direct drive	f_{OSC} SR (= $1/t_{OSC}$)	1	16	MHz
	with PLL		10	16	MHz
Input clock frequency driving at XTAL1	direct drive	$1/t_{OSCDD}$ SR	–	40	MHz
	with PLL		10	30	MHz
Input clock high time		t_1 SR	7	–	ns
Input clock low time		t_2 SR	7	–	ns
Input clock rise time		t_3 SR	–	4	ns
Input clock fall time		t_4 SR	–	4	ns

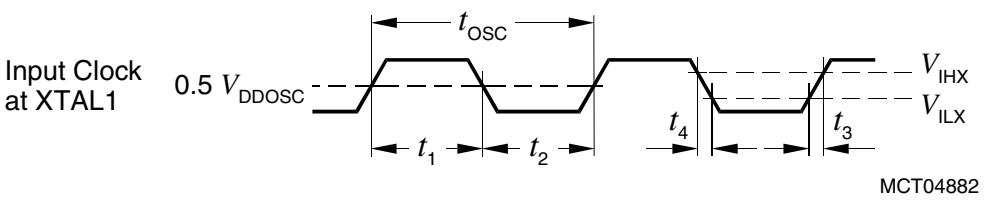


Figure 29 Input Clock Timing

Preliminary

CLKOUT Timing

V_{SS} = 0 V; V_{DDP05} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values			Unit
			min.	typ.	max.	
Clock period	t_{CLKOUT}	CC	25	–	–	ns
Clock high time	t_5	CC	7.5	–	–	ns
Clock low time	t_6	CC	7.5	–	–	ns
Clock rise time	t_7	CC	–	–	4	ns
Clock fall time	t_8	CC	–	–	4	ns
Clock duty cycle $t_5/(t_5 + t_6)$	DC	CC	45	50	55	%

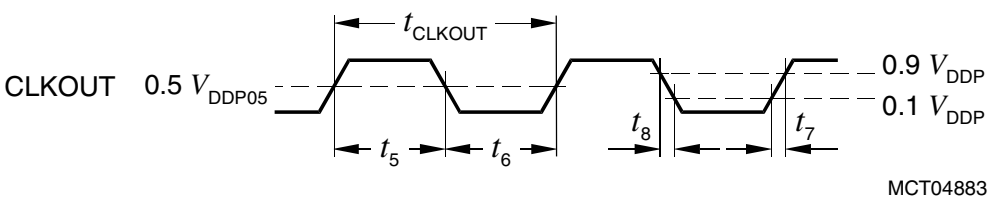


Figure 30 CLKOUT Output Clock Timing

Preliminary

PLL Parameters

Note: All PLL characteristics defined on this and the next page are guaranteed by design characterization.

V_{SS} = 0 V; V_{DD} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C;

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Accumulated jitter	D_N	see Figure 31		–
VCO frequency range	f_{VCO}	150	200	MHz
PLL base frequency	$f_{PLLBASE}$	40	130	MHz
PLL lock-in time	t_L	–	200	µs

Phase Locked Loop Operation

When PLL operation is enabled and configured (see Figure 18 and Page 59), the PLL clock f_{VCO} (and with it the system clock f_{SYS}) is constantly adjusted to the selected frequency. The relation between f_{VCO} and f_{SYS} is defined by: $f_{VCO} = K \times f_{SYS}$. The PLL causes a jitter of f_{SYS} and also of CLKOUT, which is directly derived from f_{SYS} and which has its frequency.

The following two formulas define the (absolute) approximate maximum value of jitter D_N in ns dependent on the K-factor, the system clock frequency f_{SYS} in MHz, and the number P of consecutive f_{SYS} periods.

$$\text{for } P < \frac{23.5}{K} \qquad D_N\,[\text{ns}] = \pm \frac{3.9}{f_{SYS}\,[\text{MHz}]} \times P + 1.2 \qquad [1]$$

$$\text{for } P \geq \frac{23.5}{K} \qquad D_N\,[\text{ns}] = \pm \frac{91.7}{f_{SYS}\,[\text{MHz}] \times K} + 1.2 \qquad [2]$$

With rising number P of clock cycles the maximum jitter increases linearly up to a value of P that is defined by the K-factor of the PLL. Beyond this value of P the maximum accumulated jitter remains at a constant value. Further, a lower system clock frequency f_{SYS} results in a higher maximum jitter.

Figure 31 gives an example for the jitter curves with K = 8.

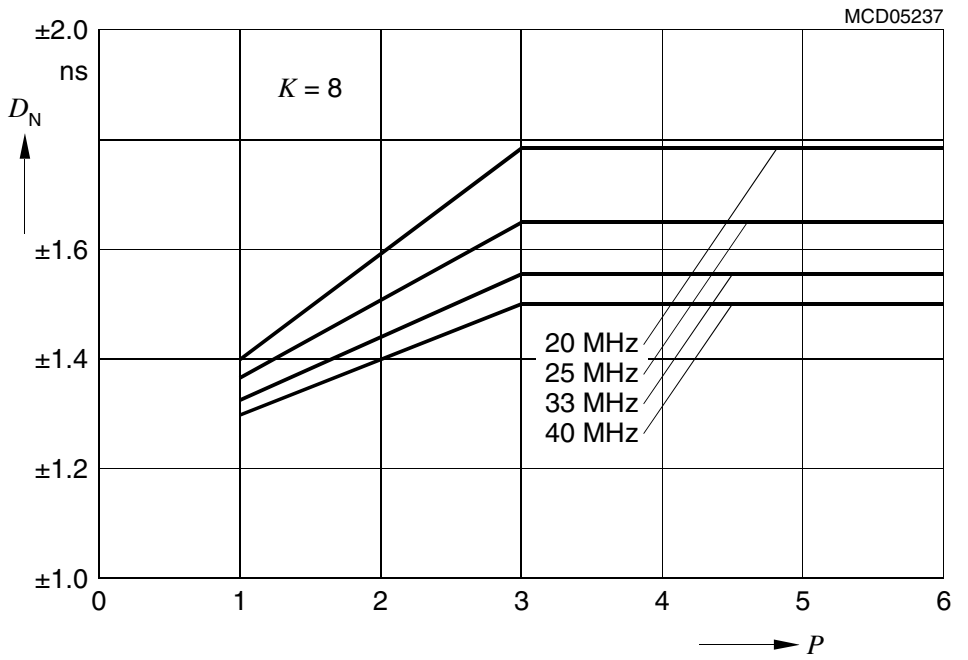


Figure 31 Approximated Maximum Accumulated PLL Jitter (for K = 8)

*Note: For safe clock generation and PLL operation the definitions and restrictions as defined at pages **58**, **59**, and **80** must be regarded.*

Preliminary

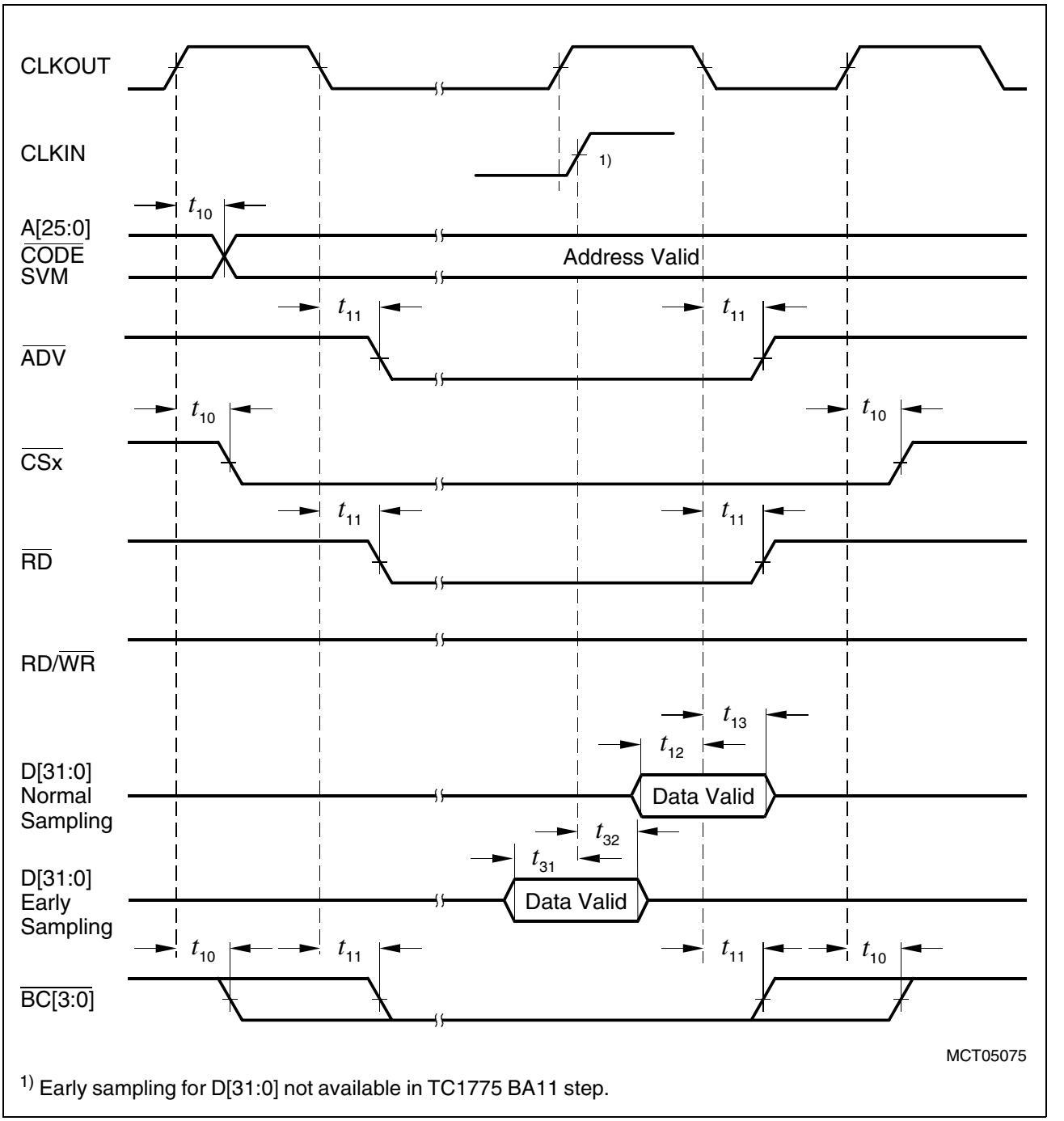
EBU Demultiplexed Timing

V_{SS} = 0 V; V_{DDP05} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
Output delay from CLKOUT ↑	t_{10}	CC	0	9	ns
Output delay from CLKOUT ↓	t_{11}	CC	-2	4	ns
Data setup to CLKOUT ↓	t_{12}	SR	9	–	ns
Data hold from CLKOUT ↓ [1]	t_{13}	SR	1	–	ns
Data valid after CLKOUT ↑ [1]	t_{15}	CC	2	–	ns
Data setup to CLKIN ↑ [2]	t_{31}	SR	see Page 90	–	ns
Data hold from CLKIN ↑ [2]	t_{32}	SR	see Page 90	–	ns

[1] Valid for EBU_BUSCONx.26 = 0.

[2] Valid for EBU_BUSCONx.26 = 1 (early sample feature). Not applicable for TC1775 BA11 step.



1) Early sampling for D[31:0] not available in TC1775 BA11 step.

Figure 32 EBU Demultiplexed Read Timing

*Note: $\overline{WAIT}$ timing see **Figure 36**.*

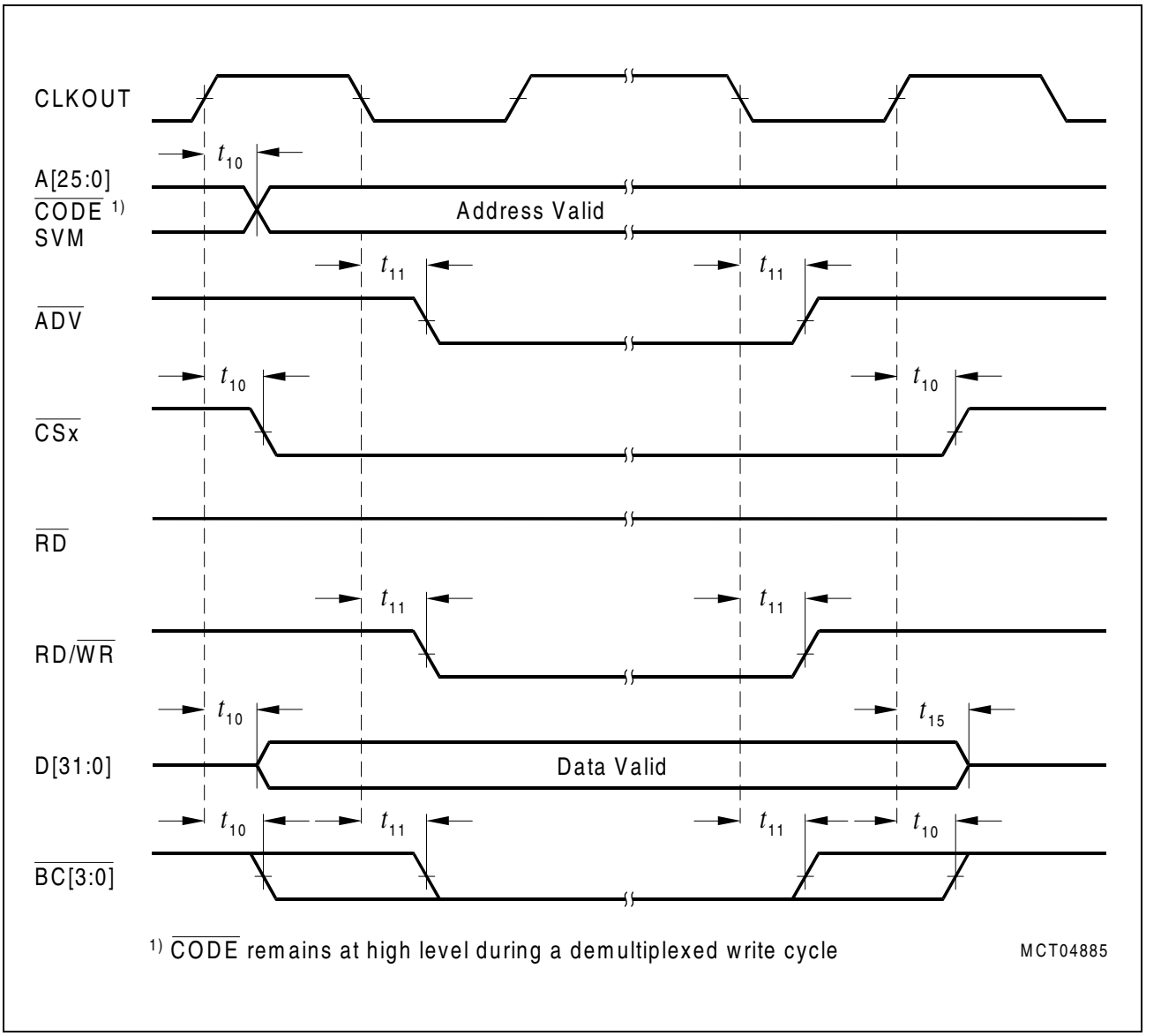


Figure 33 EBU Demultiplexed Write Timing

Preliminary

EBU Multiplexed Timing

V_{SS} = 0 V, V_{DDP05} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
Output delay from CLKOUT ↗ [1]	t_{20}	CC	-2	10	ns
Output delay from CLKOUT ↘	t_{21}	CC	-2	4	ns
Data setup to CLKOUT ↘	t_{22}	SR	9	–	ns
Data hold from CLKOUT ↘	t_{23}	SR	1	–	ns
Address and data valid after CLKOUT ↗ [1]	t_{25}	CC	2	–	ns

[1] The following condition is always valid: $t_{25} < t_{20}$

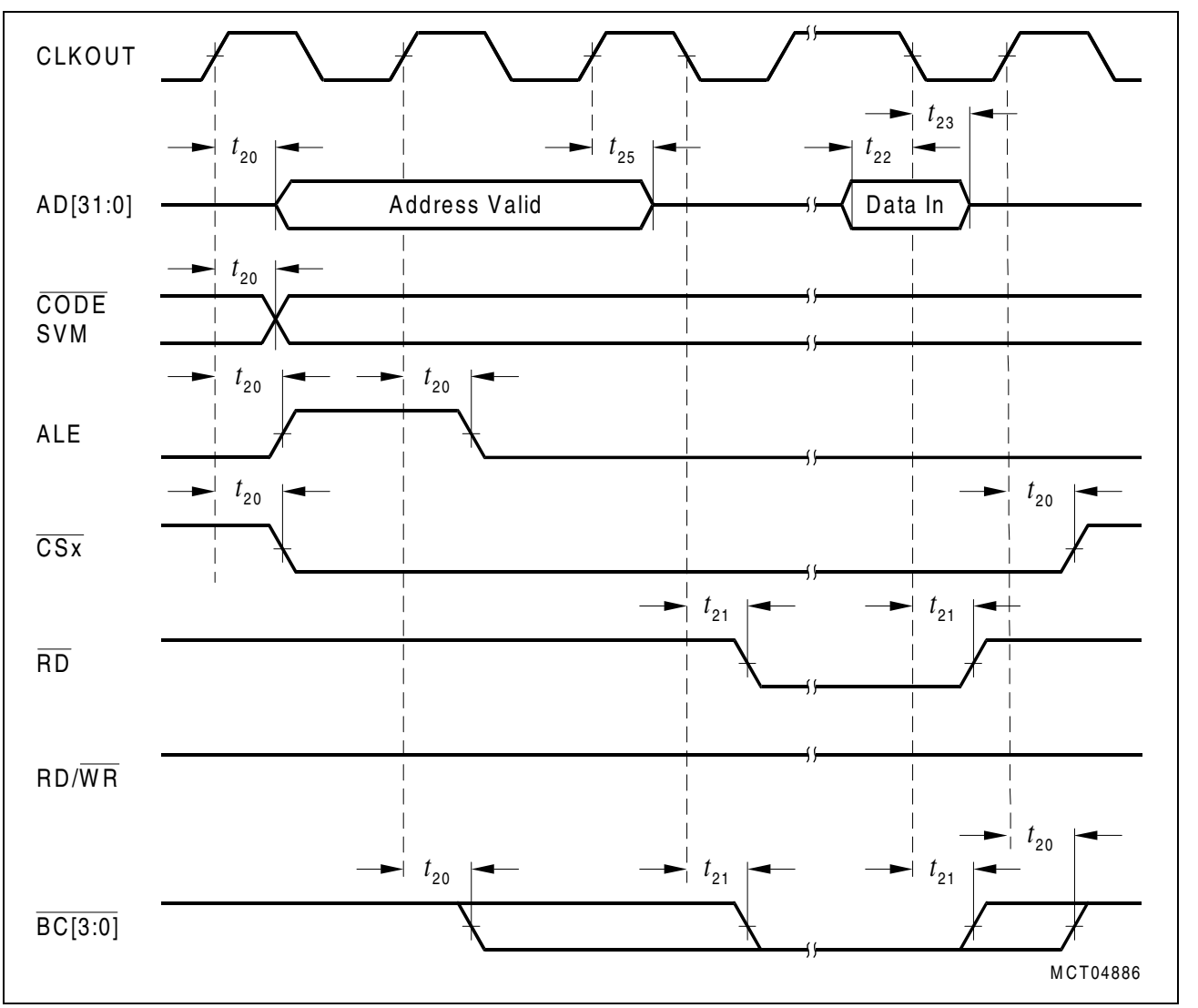


Figure 34 EBU Multiplexed Read Timing

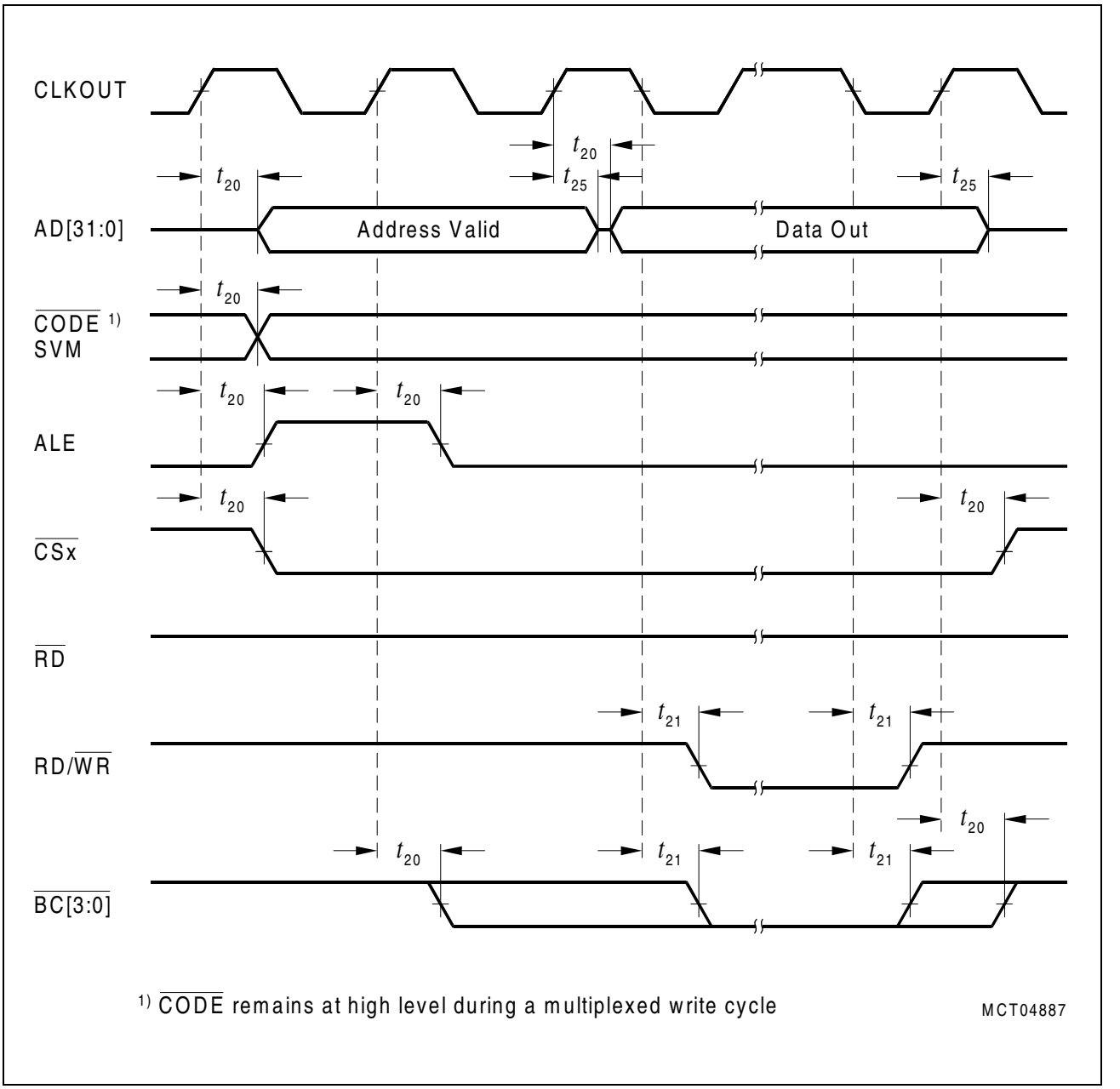


Figure 35 EBU Multiplexed Write Timing

Preliminary

$\overline{\text{WAIT}}$ Timing (FPI Bus to external Memory)

V_{SS} = 0 V; V_{DDP05} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
$\overline{\text{WAIT}}$ setup to CLKOUT ↓	t_{50}	SR	14[1)]	–	ns
$\overline{\text{WAIT}}$ hold from CLKOUT ↓	t_{51}	SR	14[1)]	–	ns
$\overline{\text{WAIT}}$ setup to CLKOUT ↑	t_{52}	SR	7	–	ns
$\overline{\text{WAIT}}$ hold from CLKOUT ↑	t_{53}	SR	2	–	ns

1) Guaranteed by design characterization.

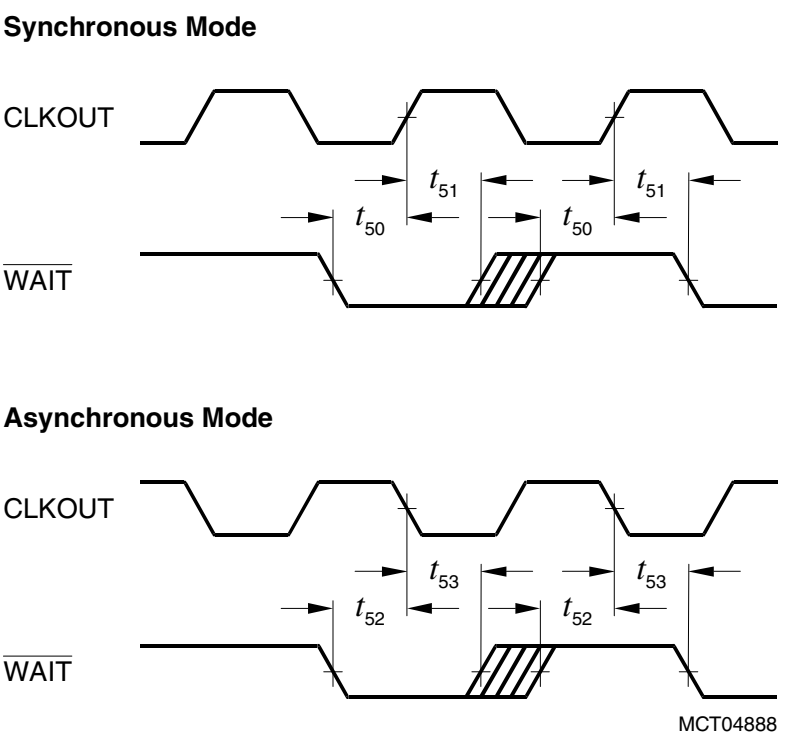


Figure 36 $\overline{\text{WAIT}}$ Timing (from FPI Bus to external Memory)

Preliminary

EBU Burst Mode Timing

V_{SS} = 0 V, V_{DDP05} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
Output delay from CLKIN ↓	t_{30}	CC	0	14	ns
Data setup to CLKIN ↓	t_{31}	SR	2[1)]	–	ns
Data hold from CLKIN ↓	t_{32}	SR	3[1)]	–	ns

1) Guaranteed by design characterization.

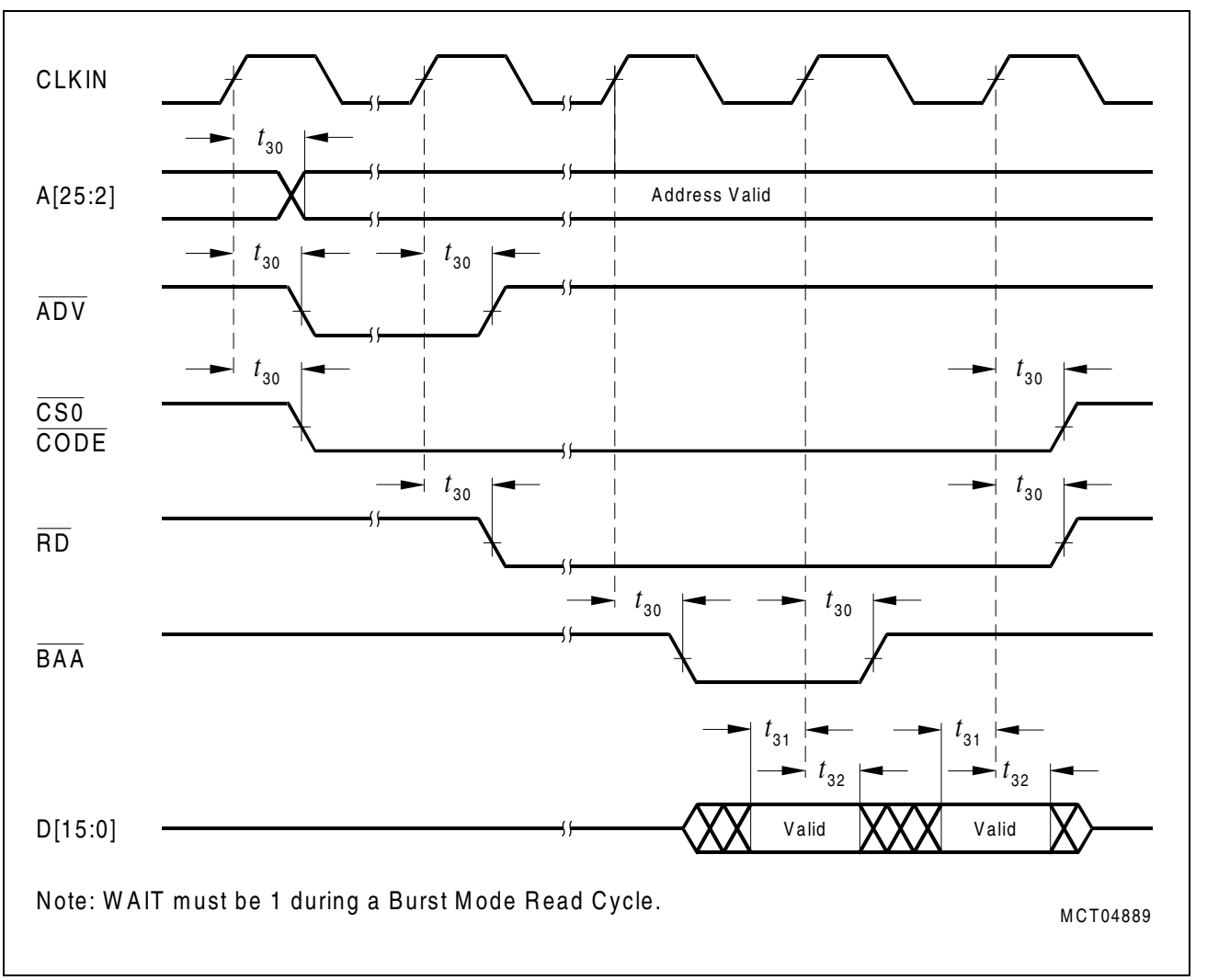


Figure 37 Burst Mode Timing (Instruction Read)

Note: Burst mode and external Flash related application hints are described in a separate application note.

Preliminary

EBU Arbitration Signal Timing

V_{SS} = 0 V, V_{DDP05} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
Output delay from CLKOUT ↓	t_{40}	CC	–	3	ns
Data setup to CLKOUT ↓	t_{41}	SR	8	–	ns
Data hold from CLKOUT ↓	t_{42}	SR	2	–	ns

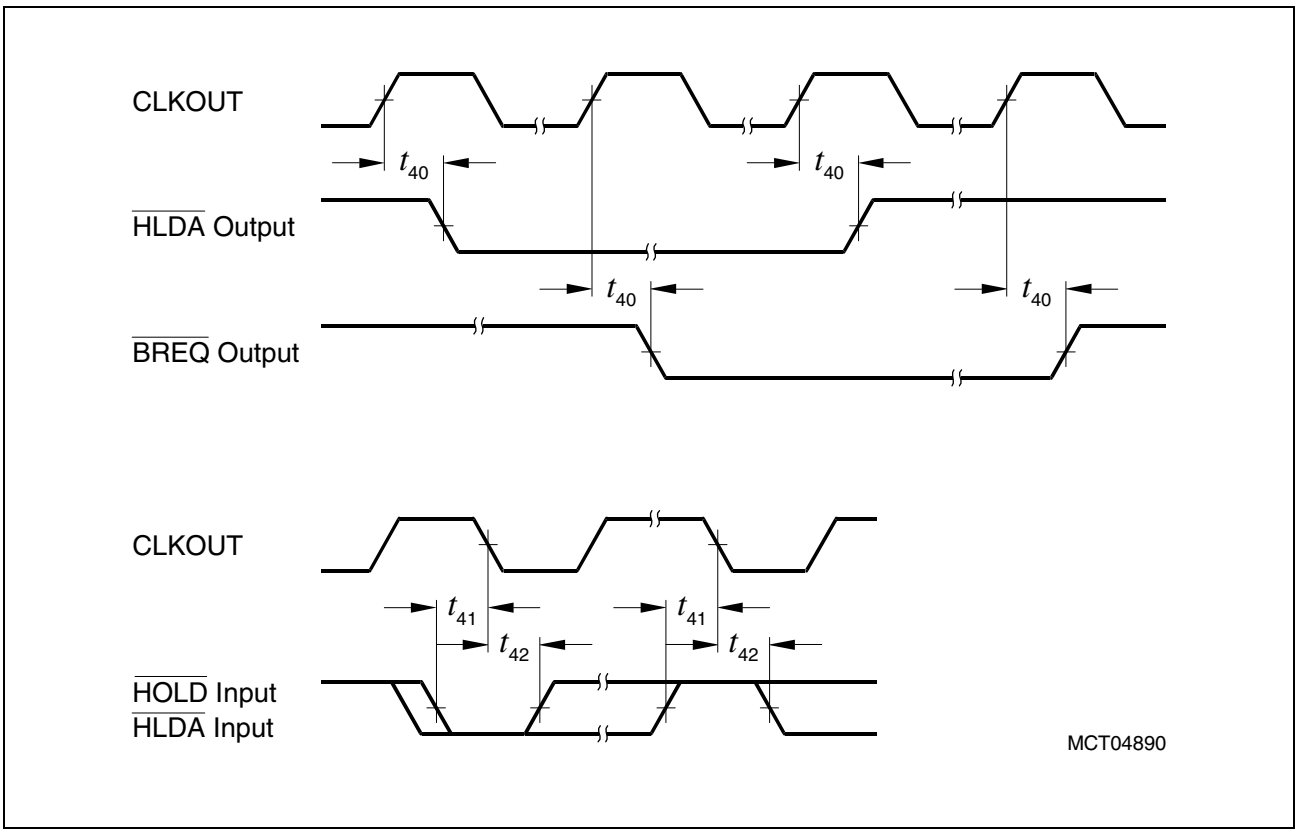


Figure 38 EBU Arbitration Signal Timing

Preliminary

EBU External Access Timing

V_{SS} = 0 V, V_{DDP05} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
$\overline{CSFPI}$, $\overline{BC}$[3:0], A[23:2] setup before $\overline{RD}$ ↘ or RD/$\overline{WR}$ ↘	t_{43}	SR	3	–	ns
Data valid after $\overline{RD}$ ↘	t_{44}	CC	$2 \times t_{CLKOUT}$	–	ns
$\overline{WAIT}$ active after $\overline{RD}$ ↘ or RD/$\overline{WR}$ ↘	t_{45}	CC	–	11	ns
RD/$\overline{WAIT}$ float after $\overline{RD}$ ↗ or RD/$\overline{WR}$ ↗	t_{46}	CC	–	20	ns
Data setup to RD/$\overline{WR}$ ↗	t_{47}	SR	3	–	ns
Data hold from RD/$\overline{WR}$ ↗	t_{48}	SR	3	–	ns

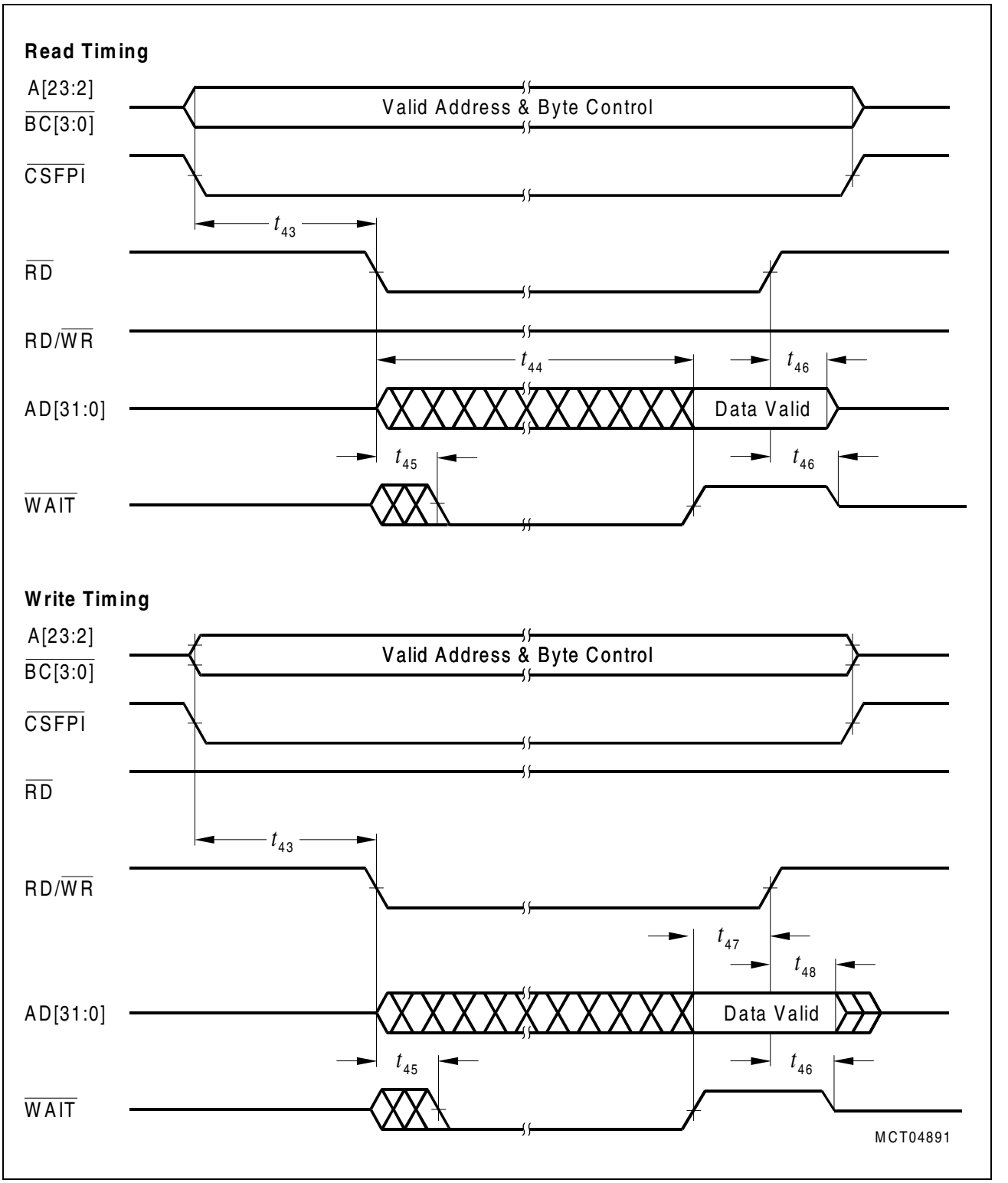


Figure 39 EBU External Access Timing (external Master to FPI Bus)

Preliminary

Port 5 (Trace Port) Timing

This timing is applicable for Port 5 when CPU or PCP trace mode is enabled (SCU_CON.ETEN = 1).

V_{SS} = 0 V; V_{DDP05} = 2.30 to 2.75 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
Port 5 lines high/low from CLKOUT ↓	t_{55}	CC	-4	5	ns

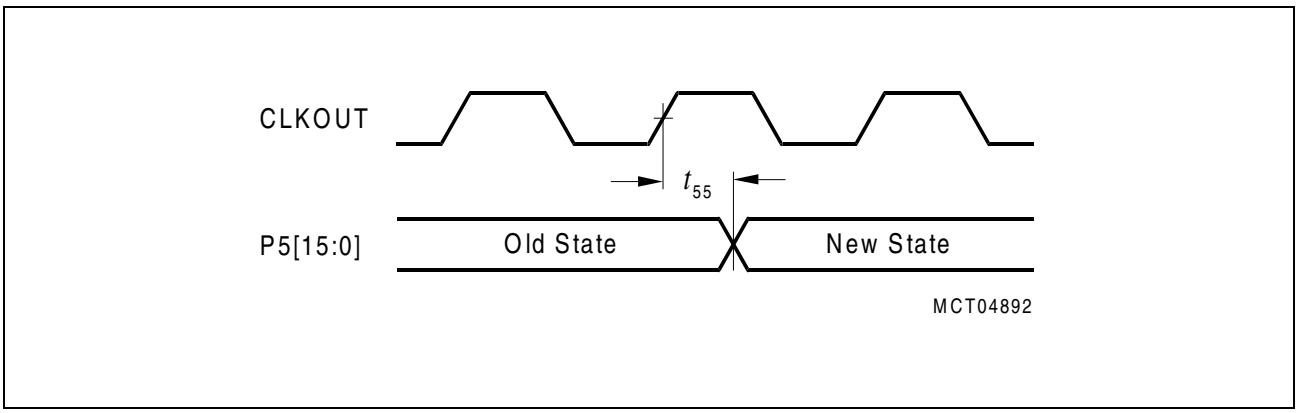


Figure 40 Port 5 Timing

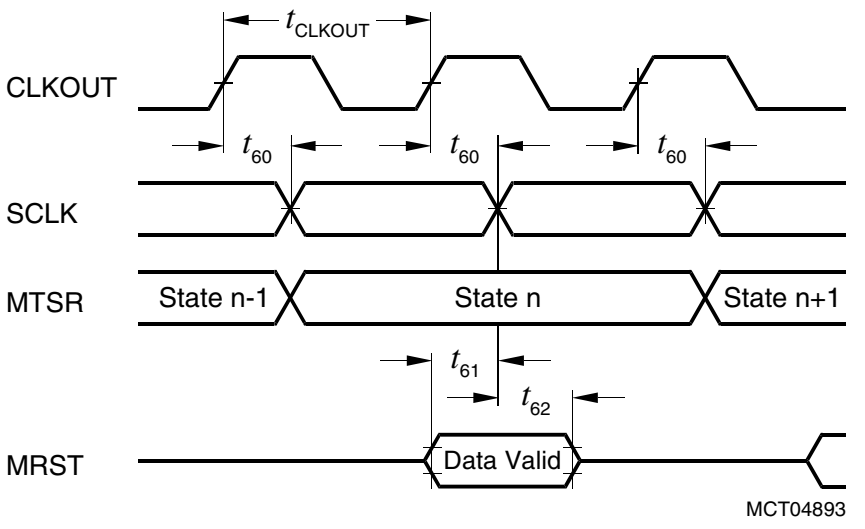
SSC Master Mode Timing

V_{SS} = 0 V; V_{DDP813} = 4.5 to 5.25 V; T_A = -40 °C to +125 °C; C_L = 50 pF;

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK/$\overline{\text{MTSR}}$ low/high from CLKOUT ↘ [1]	t_{60}	CC	–	7	ns
MRST setup to SLCK rising/falling edge	t_{61}	SR	14[2]	–	ns
MRST hold from SLCK rising/falling edge	t_{62}	SR	14[2]	–	ns

1) This parameter is valid for high current mode output driver characteristic and normal timing edge characteristic (P13_POCON.PECx = 00_B and P13_POCON.PDCx = 00_B).

2) Guaranteed by design characterization.



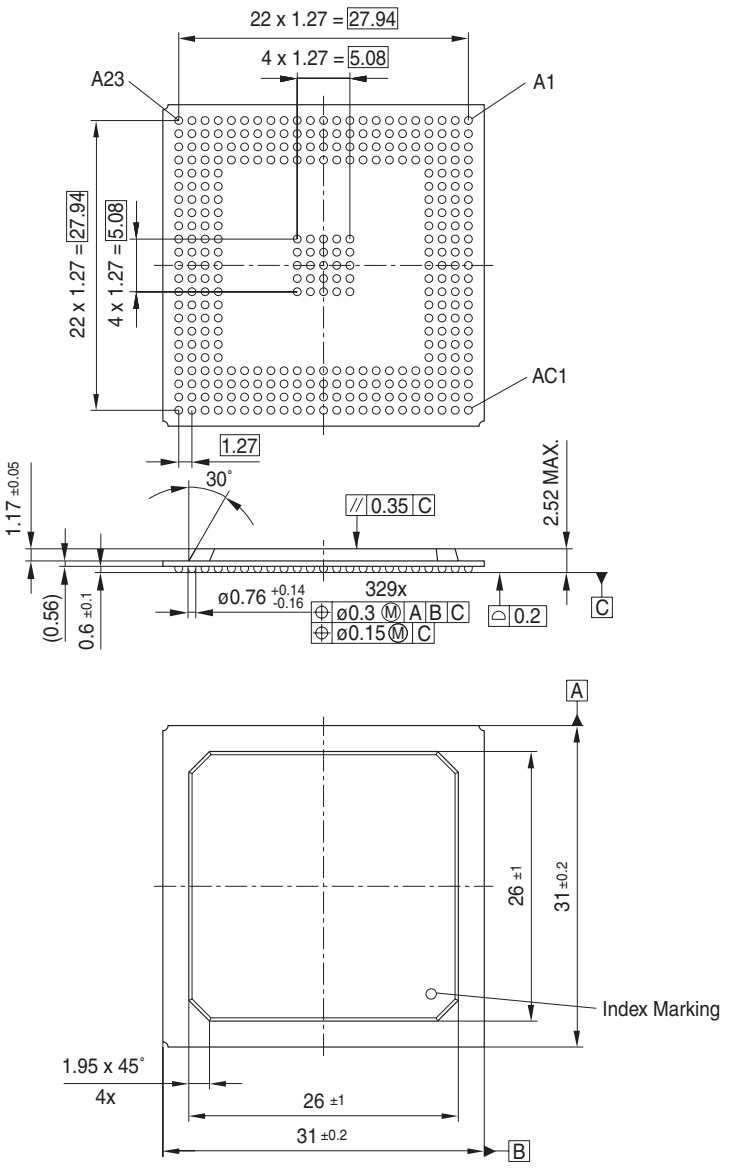
Note: The timing diagram assumes the highest possible baud rate operation.
($f_{SSC} = f_{CLKOUT}$, SSCx_CLC.RMC = 1, SSCx_BR.BR_VALUE = 0000_H)

Figure 41 SSC Master Mode Timing

Preliminary

Package Outlines

P-BGA-329
(Plastic Ball Grid Array Package)



You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

http://www.infineon.com

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