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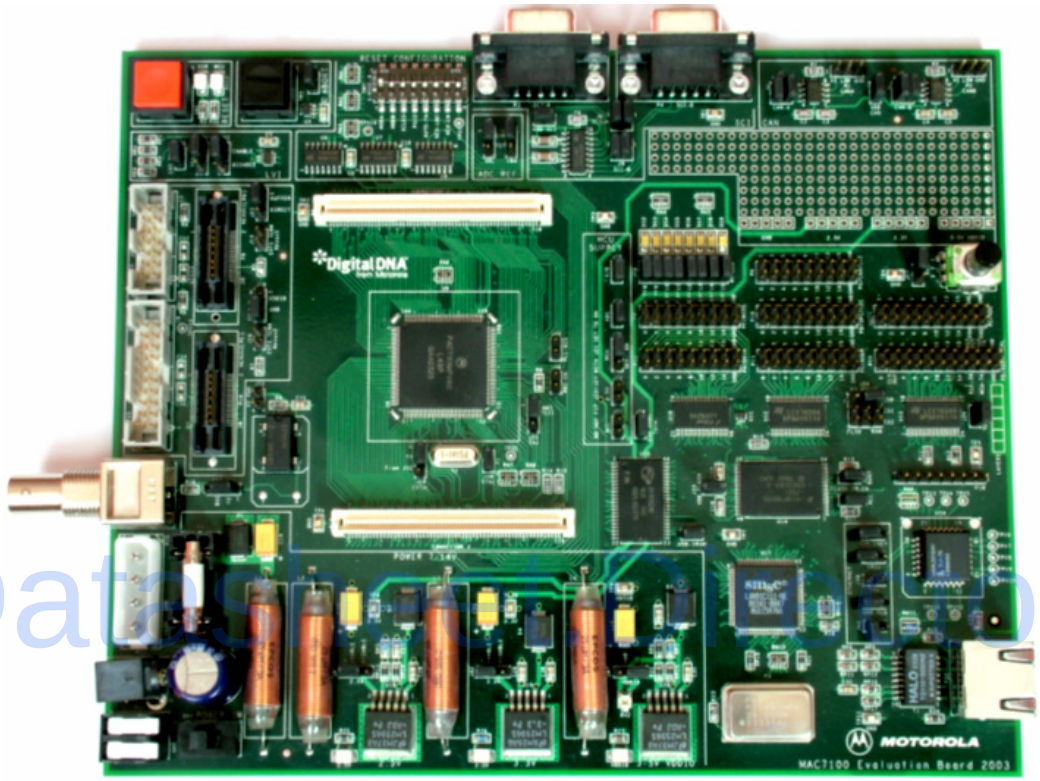

MAC7100EVB Users Manual

Revision 1.1

November 2004

Note – This users manual is for RE11505F Rev O PCBs

Revision History:

Revision	Date	Author	Comment
0.2	27 June 2003	A. Robertson	Initial Release – Prototype PCB Only
1.0	18 Sept 2003	A. Robertson	Changes for RE11505F Rev O Production PCB
1.1	12 Nov 2004	A. Robertson	Changed to Freescale. Updated MAC family table

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1. Introduction

This document details the setup and configuration of the Freescale MAC7100 evaluation board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the MAC7100 family of microprocessors and to facilitate hardware and software development.

The table below shows the MAC7100 family portfolio (correct at time of writing this document).

Table 1-1 MAC7100 Product Family

Part Number	Flash Size	RAM Size	Expanded Bus
MAC71x6	1MB	48KB	Optional
MAC71x5	768KB	40KB	Optional
MAC71x1	512KB	32KB	Optional
MAC71x4	384KB	20KB	Contact Freescale
MAC71x2	256KB	16KB	Contact Freescale

The "**x**" in the part number field defines the package type and pinout options of the MCU. For information purposes, the package types are detailed below.

Table 1-2 MAC7100 Package Options

Package Designator	Package Type	ADC Channels	External Bus
0	144 LQFP	32	No
1	144 LQFP	16	Yes
2	112 LQFP	16	No
3	208 MAP BGA	32	Yes
4	100 LQFP	16	No

Note that not all packages are available for all devices. The information detailed in the tables above is subject to change. For the latest product information, please consult the MAC7100 website at www.freescale.com/mac7100, or speak to your Freescale representative.

The MAC7100 EVB is populated with the MAC7111 MCU. As can be seen from the tables above, this is a 144QFP device with 512Kbytes of Flash and 32Kbytes of SRAM. Should you wish to develop using any of the lower specification devices, this can be achieved by emulating the feature set with the MAC7111 on the EVB. If you are developing with a higher specification device, EVB adapter boards are available for this purpose. For important information on the use of adapter board, please see section 6.1.

All of the MAC7100 family members in the same package are pin compatible (eg the MAC711**1** is pin compatible to the MAC711**5**).

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

Throughout this document, active low MCU signals are denoted with an "*x*" added onto the signal name, eg XCLKS*x*.

1.1 EVB Feature List

The EVB provides the following features:

- MAC7111 MCU device soldered directly onto the EVB with sufficient room to fit a surface mount Yamaichi IC149-144 series socket if required (solder tabs and polarisation pins are supported).
- Single external power supply input (7-14V), regulated on board to provide all the necessary EVB voltages. Power may be supplied via a 2.1mm barrel power jack, 2-way Lever style connector or standard PC (Molex style) power supply connector.
- Flexible on board power supply selection, including the ability to bypass the internal 2.5V MCU regulator if desired.
- Master power switch.
- User Reset and Abort pushbutton switches.
- Configurable Low Voltage Inhibit (LVI) control circuitry to monitor all of the voltages from the EVB regulators.
- Full reset mode configuration switches.
- Flexible MCU clock source options allowing clock to be selected from on board crystal circuit, on board oscillator module or external clock source (via BNC connector). Both traditional and loop controlled (amplitude limited) Pierce oscillator configurations are supported for the local crystal circuit.
- 14 and 20-way JTAG connectors.
- 38 pin MICTOR (Matched Impedance Connector) NEXUS connectors.
- Two 120-way expansion connectors to allow connection of a daughter card supporting different MCU variants or additional application specific circuitry.
- Array of 0.1 inch pitch user connectors, providing direct access to all of the MCU port signals.
- Up to 128K Bytes of asynchronous SRAM supported on the EVB. Can be configured for use with any MCU chip select.
- Up to 2M Bytes of asynchronous FLASH supported on the EVB with hardware write protection jumpers. As with the SRAM, this can also be configured for use with any MCU chip select.
- Two SCI (RS232) physical interface circuits connected to standard PC style DB9 female connectors allowing direct connection to a PC serial port using a standard serial cable.
- Two Philips PCA82C250T high-speed CAN interface transceivers connected to the MCU CAN channels A and B.
- Memory mapped full duplex 10/100 Megabit Ethernet controller and RJ45 connector.
- Small prototyping area consisting of a grid of 0.1 inch spaced through holes with easy access to ground and power supply points.

IMPORTANT

Before the EVB is used or power is applied, please fully read the following sections on how to correctly configure the board.

Failure to correctly configure the board may cause device or EVB damage.

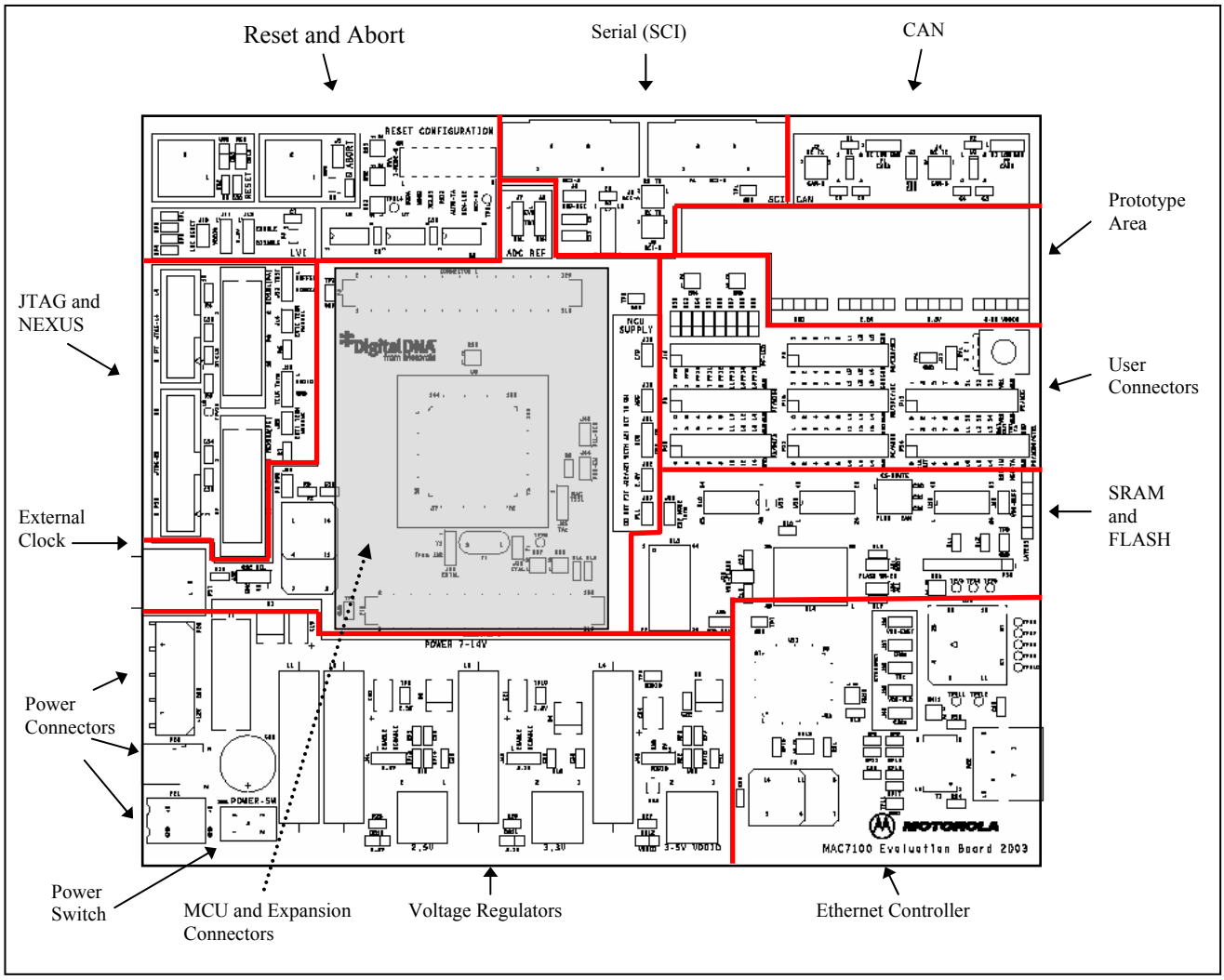
2. Configuration

This section details the configuration of each of the EVB functional blocks.

Throughout this document, all default jumper and switch settings are clearly marked with "**(D)**" and are shown in blue text. This should allow a more rapid return to the default state of the EVB if required. Note that the default configuration for all 3-pin jumpers is a header fitted between pins 1 and 2.

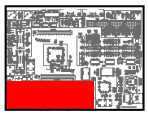
The EVB has been designed with ease of use in mind and, where possible, has been segmented into functional blocks as shown below. Detailed silkscreen legend has been used throughout the board on all switches, jumpers and user connectors.

Figure 2-1 EVB Functional Blocks



2.1 Power Supply Configuration

The Power supply section is located in the bottom left area of the EVB



The EVB requires an external supply voltage of 7-14V DC, minimum 1Amp. This is regulated on board using three switching voltage regulators to provide the necessary EVB voltages of 5V, 3.3V and 2.5V. There are three different power supply input connectors on the EVB as described in the following section.

2.1.1 Power Supply Input Connectors

2.1mm Barrel Connector – P23:

This connector should be used to connect the supplied wall-plug mains adapter. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1mm plug uses the correct polarisation as shown below:

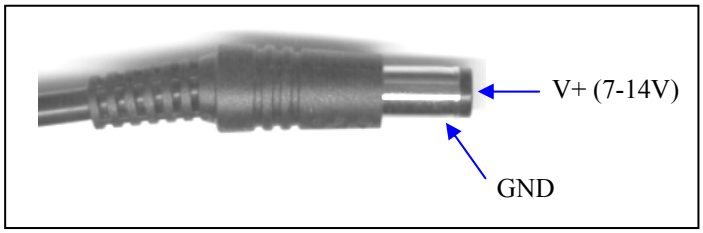


Figure 2-2 2.1mm Power Connector

2-Way Lever Connector – P21:

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarisation of the connectors is clearly marked on the EVB and care must be taken to ensure this is connected correctly.

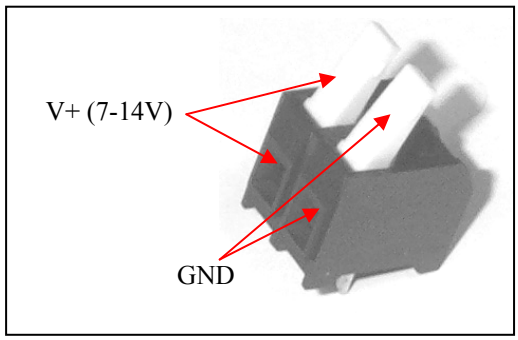


Figure 2-3 2-Lever Power Connector

PC Style Power Connector – P20:

PC Power supplies offer an in-expensive source of stable, high current DC power. The EVB is designed to support direct connection of a PC power supply 4-way connector (Molex Style plug that would normally be connected to a PC hard disk or other internal PC hardware). Only the +12V line is used on the EVB and the +5V line is not connected to any EVB circuitry. Typically, the +12V line will be coloured yellow (as shown in the figure below), however the connectors are polarised and can therefore only be connected in the correct orientation.

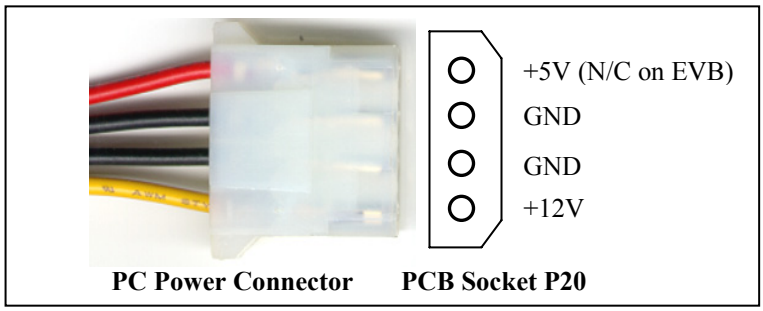


Figure 2-4 PC Power Connector

Notes:

- *PC power supplies are designed to be used with a load connected to both the 5V and 12V lines. Without this, the power supply may shut down or not regulate correctly. The load of the EVB is generally sufficient for the +12V line but supplemental loading may be required on the +5V line in order for the 12V line to regulate correctly or indeed for the power supply to power on.*
- *If an ATX style power supply is used, there is an additional requirement in that the "PS_ON" line on the motherboard connector must be grounded in order for the power supply to start. Please see the associated power supply documentation for details.*

2.1.2 Power Supply Configuration Jumpers (J41, J42 and J43)

The Power supply control jumpers are located adjacent to the respective regulators.

As mentioned above, the EVB has three voltage regulators on board:

- 2.5V regulator (U18) to supply the MCU Core voltage when the MCU on-chip regulator is disabled.
- 3.3V regulator (U19) for the EVB peripherals (For example Ethernet Controller).
- VDDIO regulator (U20) for the MCU I/O supply and EVB peripherals.

The 2.5V and 3.3V regulators can be disabled if they are not required. The VDDIO regulator has the option of being used in either a fixed 5V mode configuration or in a variable 3-5V mode. This is intended to support the MAC7100 specification where the peripheral voltage can be varied.

Table 2-1 Regulator Configuration Jumpers

Jumper	Position	PCB Legend	Description
J41 (2.5V)	1-2 **(D)** 2-3	ENABLE DISABLE	2.5V regulator output is Enabled 2.5V regulator output is Disabled
J42 (3.3V)	1-2 **(D)** 2-3	ENABLE DISABLE	3.3V regulator output is Enabled 3.3V regulator output is Disabled
J43 (VDDIO)	1-2 **(D)** 2-3	5V VAR	VDDIO regulator is configured as 5.0V fixed mode. VDDIO regulator is configured as 3-5V variable mode controlled by RV2

When the VDDIO regulator is set to variable mode, the output can be varied from approximately 3V to 5V by moving trimming resistor RV2. The following graph gives an indication of the expected VDDIO regulator output voltage against resistor value when used in variable mode.

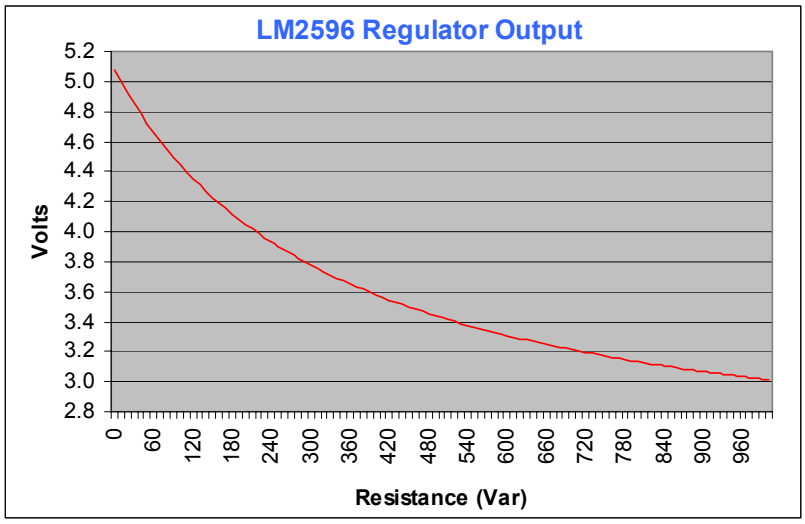


Figure 2-5 VDDIO Regulator Variable Output

Before changing any of the regulator configurations, it is worthwhile carefully considering if any of the EVB components you require will be affected. Table 2-2 details a list of the various EVB components and peripherals affected by each regulator.

Table 2-2 Power Supply Distribution

Regulator	Used On	Comments
VDDIO (3-5V)	MCU VDDA, VDDX and VDDR pins External FLASH and SRAM CAN / RS232 physical interface drivers Expansion and prototype area connectors Reset control and Abort switch circuits Nexus and JTAG connectors Pullup resistors LED's and variable resistor on user connectors	 5V mode only. Disable if VDDIO < 4.75V * 5V mode only. Disable if VDDIO < 4.75V *
2.5V	MCU 2.5V and VDDPLL pins (When VDDR = 0V) External Oscillator Module LVI circuit main power and reset switch Expansion and prototype area connectors	Only when MCU on-chip regulator disabled
3.3V	Address Data-Bus and control buffers Ethernet Controller Ethernet circuit PLD (also controls TGT-TA signal) Expansion and prototype area connectors	

** If the VDDIO regulator is set to variable mode, these blocks must be disabled if VDDIO < 4.75V*

2.1.3 Power Switch (SW4)

Slide switch SW4 can be used to isolate the power supply input from the EVB voltage regulators if required.

Moving the slide switch to the **right** (away from connector P21) will turn the EVB **on**.
Moving the slide switch to the **left** (towards connector P21) will turn the EVB **off**.

2.1.4 Power Status LED's and Fuse

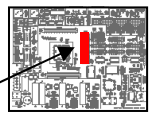
When power is applied to the EVB, green power LED's adjacent to the voltage regulators show the presence of the supply voltages as follows:

LED DS10 – Indicates that the 2.5V regulator is enabled and working correctly
LED DS11 – Indicates that the 3.3V regulator is enabled and working correctly
LED DS12 – Indicates that the VDDIO (3-5V) regulator is working correctly

If no LED's are illuminated when power is applied to the EVB and the Regulator jumpers are set to "enable", it is possible that either power switch SW4 is in the "OFF" position or that the fuse F1 has blown. This can occur if power is applied to the EVB in reverse-bias where a protection diode ensures that the fuse blows rather than causing damage to the EVB. Replace F1 with a 20mm 1A fast blow fuse.

2.2 MCU Power Supply Jumpers (J15, J19, J21, J22 and J27)

The MCU Power supply jumpers are located to the right of the MCU in a box titled "MCU Supply"



The MCU power supply lines are grouped together according to function (eg VDDX, VDDA). Each grouping is jumpered to allow isolation from the power supply in order to facilitate current measurement. In addition, these jumpers are used to disable the MCU on-chip 2.5V regulator if required and allow the EVB 2.5V regulator to be used to power the MCU core and PLL circuitry.

Table 2-3 MCU Power Supply Jumpers

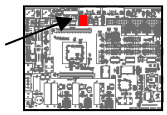
Jumper	Position	Description
J19 (ADC)	FITTED **(D)** REMOVED	Connects EVB VDDIO regulator output to MCU VDDA pins MCU VDDA logic is not powered
J15 (I/O)	FITTED **(D)** REMOVED	Connects EVB VDDIO regulator output to MCU VDDX pins MCU VDDX logic is not powered
J21 (REG) *	1-2 **(D)** 2-3	Connects EVB VDDIO regulator output to MCU VDDR pins Connects MCU VDDR to GND (required if J22 / J27 fitted)
J22 (2.5V) *	FITTED REMOVED **(D)**	Connects EVB 2.5V regulator output to MCU VDD2.5 pins MCU On Chip regulator powers VDD2.5
J27 (PLL) *	FITTED REMOVED **(D)**	Connects EVB 2.5V regulator output to MCU VDDPLL pins MCU On Chip regulator powers VDDPLL

CAUTION: * When jumper J21 (REG) is set to position 1-2 (ON), enabling the built in 2.5V MCU regulator, jumpers J22 (2.5V) and J27 (PLL) MUST be removed.

The jumper configuration shown in Table 2-3 shows the default state of the EVB where the EVB is configured to use the MCU on-chip 2.5V regulator. In this case, jumpers J22 and J27 are removed and no external 2.5V power is supplied to the MCU. The EVB can be re-configured with the EVB 2.5V regulator powering the MCU core and PLL circuitry in preference to the MCU on-chip regulator. In this configuration, jumper J21 (REG) is moved to position 2-3 (OFF) and jumpers J22 (2.5V) and J27 (PLL) are fitted.

2.3 ADC Reference Voltage Select (J7, J8)

The ADC reference voltage jumpers are located at the top of the EVB in a box titled "ADC REF".



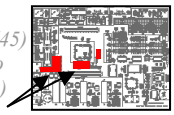
The Analogue to digital converter reference voltages, VRH and VRL can be connected directly to the EVB supply lines (where VRH is connected to VDDIO and VRL to GND) or can be routed to user connector P11, allowing user defined reference voltages to be supplied.

Figure 2-6 ADC Reference Voltage Selection

Jumper	Position	PCB Legend	Description
J8 (VRH)	1-2 **(D)**	EVB	MCU VRH is connected to EVB VDDIO
	2-3	TGT	MCU VRH is connected to user connector P11
J7 (VRL)	1-2 **(D)**	EVB	MCU VRL is connected to EVB analogue GND
	2-3	TGT	MCU VRL is connected to user connector P11

2.4 MCU Clock Control (Jumpers J23, J29, J30 and J32)

The MCU clock control jumpers are located around the MCU (J29, J30, J45) and above and in the area adjacent to the BNC connector P17 (J32 and J23)



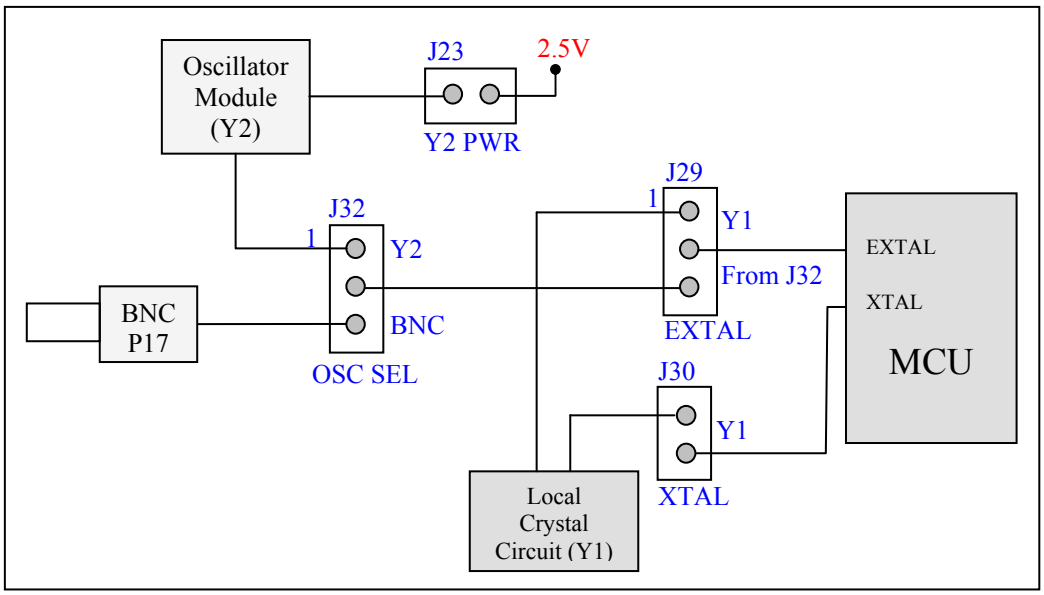
2.4.1 Clock Selection

The EVB supports three possible MCU clock sources:

(1) The local Pierce clock oscillator circuit Y1 (which can be configured in traditional or low power modes).
(2) An oscillator module Y2, driving the MCU EXTAL signal.
(3) An external clock input to the EVB via BNC connector P17, again driving the MCU EXTAL signal.

The selection between these options is controlled using jumpers as shown below:

Figure 2-7 EVB Clock Selection



Jumper	Position	PCB Legend	Description
J23 (Y2 PWR)	FITTED REMOVED **(D)**		Oscillator Module Y2 is powered (enabled) Oscillator Module Y2 is not powered (disabled)
J32 (OSC SEL)	1-2 **(D)** 2-3	Y2 BNC	External EXTAL routed from Oscillator Module Y2 External EXTAL routed from BNC Connector P17
J29 (EXTAL)	1-2 **(D)** 2-3	Y1 From J32	MCU EXTAL connected to local oscillator circuit MCU EXTAL routed to source defined by J32
J30 (XTAL)	FITTED **(D)** REMOVED		MCU XTAL connected to local oscillator circuit XTAL disconnected (External Oscillator configuration)

Table 2-4 Clock Source Jumper Selection

The default configuration connects the MCU EXTAL and XTAL pins to the local clock oscillator circuit containing Y1. This can be configured as either loop controlled (ALC) Pierce (default) or full swing Pierce, as detailed in Figure 2-8. The reset state of the XCLKS*x* (External Clock Source) pin determines the type of local oscillator circuit that will be used (see section 2.8).

In order to configure the EVB to use an external oscillator source, jumper J29 (EXTAL) is moved to position 2-3 and jumper J30 (XTAL) must be removed. Jumper J32 (OSC SEL) is then used to select the external clock source from either the oscillator module Y2 (J32 in position 1-2) or BNC connector P17 (J32 in position 2-3). If the oscillator module Y2 is to be used, jumper J23 (Y2 PWR) must be fitted.

Caution - When an external oscillator source is used, XCLKSx must be set LOW (as configured for normal Pierce configuration) - see section 2.8.

Notes:

- *The power for oscillator module Y2 is sourced from the EVB 2.5V regulator so this regulator must be enabled if oscillator module Y2 is used. See section 2.1.2 for details*
- *When an external oscillator source is used (Y2 or BNC), only the MCU EXTAL pin is driven. The MCU XTAL pin must be left open circuit by removing jumper J30. When using the BNC connector, care must be taken to ensure the signal amplitude does not exceed 2.5V.*

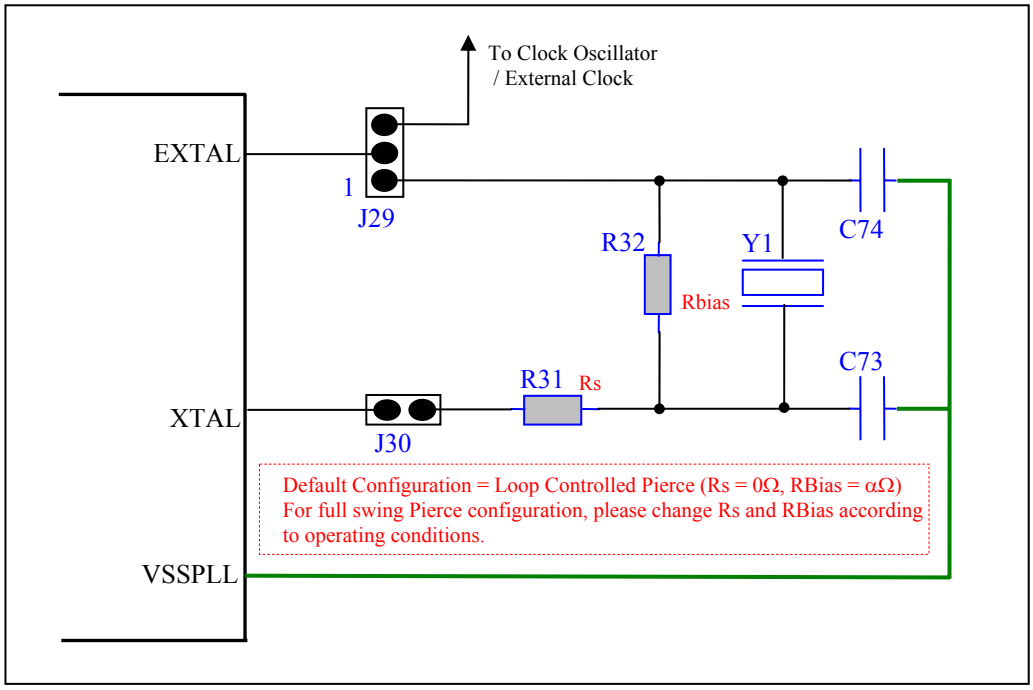


Figure 2-8 Pierce Oscillator Configuration

2.4.2 PLL Control (J45)

If the PLL circuitry is not required, this can be disabled by tying the MCU XFC pin to VDDPLL. Jumper J45 provides this functionality. The table below shows the default configuration with jumper J45 removed, thus enabling the PLL.

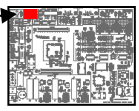
Table 2-5 PLL Disable Jumper

Jumper	Position	Description
J45 (PLL-DIS)	FITTED	MCU PLL Circuitry is disabled (XFC = VDDPLL)
	REMOVED **(D)**	MCU PLL Circuitry is enabled

Note – If the PLL is disabled, the clock circuitry should be configured to use either the full swing Pierce oscillator configuration or an external clock source.

2.5 Abort Switch and Control (J1, SW3)

The Abort Switch is located at the top left of the EVB in a box titled "ABORT".



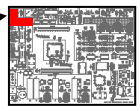
An active low, push button ABORT switch (SW3) is provided on the EVB. This is connected to the MCU XIRQ*x* pin via jumper J1 and when pressed, drives the MCU XIRQ*x* signal low, causing an interrupt. Active de-bounce circuitry ensures that a press of the switch issues a clean signal to the MCU, avoiding multiple interrupts.

Table 2-6 Abort Enable Jumper

Jumper	Position	Description
J1 (ABORT)	FITTED **(D)**	ABORT switch is connected to MCU XIRQ*x* line (abort switch enabled)
	REMOVED	ABORT switch is disconnected from MCU XIRQ*x* line (disabled)

2.6 Reset Switch, LEDs and LVI Control (Jumpers J10, J11, J12, SW2)

The Reset and LVI circuitry is located at the top left corner of the EVB in areas titled "RESET" and "LVI



The EVB incorporates an LVI (Low Voltage Inhibit) device to provide under-voltage protection for all of the EVB voltage regulators. When the regulator voltage(s) drop below a certain threshold level, the LVI will automatically assert the MCU reset line in order to prevent incorrect operation of the MCU or EVB circuitry.

The table below shows the LVI reset threshold levels for each power supply line on the EVB.

Table 2-7 LVI Resistor Ladder Values

Regulator	Minimum Voltage Before MCU reset
2.5V	2.33V
3.3V	2.9V
VDDIO	4.75V

The LVI device is powered from the 2.5V regulator output with additional monitor inputs providing the protection for the 3.3V and VDDIO regulator outputs. Jumpers provide the possibility to disable the LVI protection for the 3.3V or VDDIO regulators if desired. In addition, a jumper is provided to disconnect the LVI reset output so it will NOT assert the MCU reset line. This allows the 2.5V regulator to be disabled without causing an MCU reset.

The LVI device also provides a de-bounced input for the EVB reset switch, SW2.

Table 2-8 LVI Control Jumpers

Jumper	Position	PCB Legend	Description
J10 (LVI Reset)	FITTED **(D)**		RESET signal from LVI drives the MCU RESET*x* line
	REMOVED		LVI is disconnected from MCU RESET*x* line (disabled)
J11 (VDDIO)	1-2 **(D)**	ENABLE	VDDIO regulator output is monitored by LVI
	2-3	DISABLE	VDDIO regulator output is NOT monitored by LVI
J12 (3.3V)	1-2 **(D)**	ENABLE	3.3V regulator output is monitored by LVI
	2-3	DISABLE	VDDIO regulator output is NOT monitored by LVI

Notes:

- *Failing to set jumper J11 to disabled when using the VDDIO regulator in variable voltage mode will cause the LVI to issue a reset when VDDIO drops below approximately 4.75V*
- *If it is required to disable the 2.5V regulator on the EVB, jumper J10 must be removed to disconnect the LVI and MCU reset lines or the LVI will continually drive the MCU reset line. Note that if the LVI device is de-powered or jumper J10 is removed, the reset switch will no longer function.*

2.6.1 Reset LEDs

There are two reset LED's, DS1 (AMBER) and DS13 (RED), placed adjacent to the EVB RESET switch to indicate the RESET status of the EVB and MCU.

LED DS13, titled "MCU", will illuminate if the MCU itself issues a reset. In this condition, LED DS1 will NOT illuminate.

LED DS1, titled "USR", will illuminate when one of the following external hardware devices issues a reset to the MCU:

- LVI circuitry (either an under-voltage detection or the reset switch is being pressed)
- There is a reset being asserted from the user connectors or from the daughter card (if fitted)
- There is a reset being driven from the Nexus or JTAG debug probe.
- *Note that LED DS13 (MCU) will also illuminate during an external (user) reset!*

2.7 Reset Buffering Scheme

The MAC7100 family has a single RESET*x* pin. This pin functions as a dual purpose input / output MCU reset signal.

To reduce loading on the MCU reset pin and also allow direct connection of non open-drain reset signals (for example connected to the user or daughter card connectors), a reset-in and reset-out buffering scheme was created as shown in Figure 2-9. There are three possible external sources of reset:

- JTAG / NEXUS MCU Reset
- Daughter card connector or user connector
- LVI Reset circuitry (including reset switch)

These are gated together independently of each other and then converted into an open-drain reset output which is directly connected to the MCU reset pin.

Similarly, the MCU Reset pin is buffered to provide a Reset-Out signal which is used to control all devices on the EVB that require a reset input.

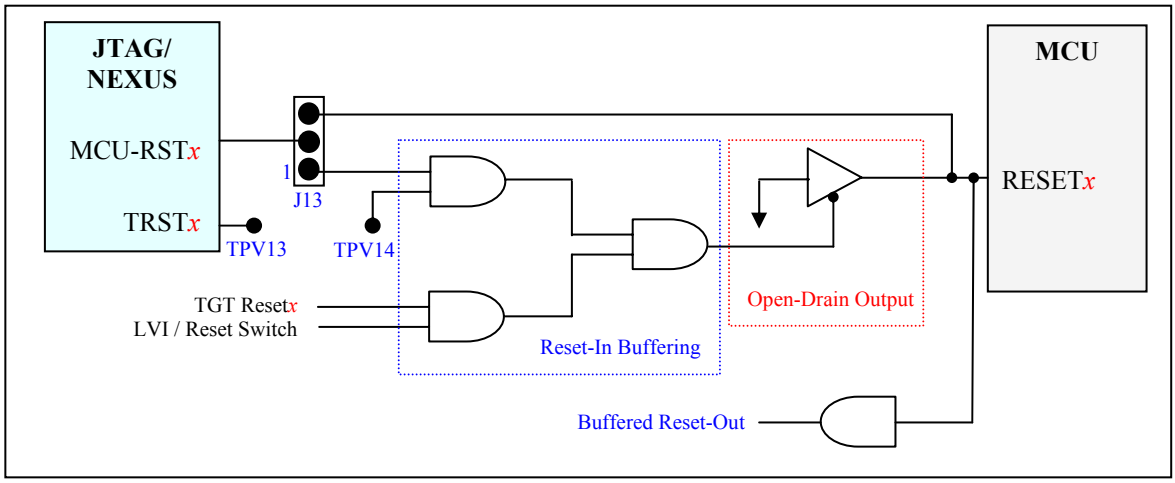


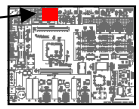
Figure 2-9 EVB Reset Buffering Scheme

Notes

- *As can be seen from the figure, there is a jumper J13 on the MCU-Resetx line from the JTAG / NEXUS connectors. For more information on this jumper, please refer to section 2.9.*
- *The MCU TRSTx signal cannot be asserted via the external MCU Reset pin so the debug interface TRSTx signal is not routed to the MCU reset circuitry.*

2.8 Reset Mode Configuration (SW1)

The Reset Mode Switch is located on the top edge of the EVB in an area titled "RESET CONFIGURATION".



The MAC7100 has 7 external mode pins that are used to configure the operating mode of the device based on their state at MCU reset.

The EVB uses a DIP switch (SW1) to set the value of these mode pins which is then actively driven onto the respective MCU pins whilst the MCU reset signal is low. Table 2-9 shows the reset function and MCU pin related to each DIP switch position

Table 2-9 MAC7100 Reset Configuration

Switch Position	Switch Legend	MCU Pin	Value	Setting	Function
1	MODA	PD1	0 (D) 1	ON OFF	Boot Vector taken from normal reset vector (Only if ModeB=0) PBL mode (Data Flash re-mapped to 0x0 and boot vector becomes 1st address of data flash. (Only if ModeB=0)
2	MODB	PD0	0 1 (D)	ON OFF	Single Chip Mode Expanded Mode (EIM relocated to 0x0, Boot From EIM)
3	XCLKS*x*	PD2	0 1 (D)	ON OFF	Standard Pierce Oscillator Mode / External Clock Mode Low Power (ALC) Pierce Oscillator Mode (ALC Circuit rqd)
4	PSIZ	PA14	0 1 (D)	ON OFF	EBI is configured with 8-bit Port Size out of reset EBI is configured with 16-bit Port Size out of reset
5	AUTO-TA	PA15	0 1 (D)	ON OFF	AutoACK is disabled – TA signal MUST be supplied externally AutoACK is enabled – EBI will supply TA signal automatically
6	NEX_LOC	PF0	0 1 (D)	ON OFF	The Nexus port is mapped to the primary port (PA0..PA6) The Nexus port is mapped to the secondary port (PE0..PE6) *
7	NEX-EN	PF1	0 1 (D)	ON OFF	The Nexus module is not present and cannot be enabled The Nexus module is present and debug interface can enable it
8		--- ---	0 1		Spare Spare

** See notes in section 2.9 if using this connector.*

Note – It is important that the MCU pins shown in Table 2-9 are NOT directly tied to ground or VCC at the user connectors as this will conflict with and invalidate the reset configuration data.

Switch SW1 is clearly labeled on the EVB with the switch function and also with the position of the switch required to drive logic 1 or 0. When the switches are in the ON position, this corresponds to logic 0.

The figure below shows the default configuration of the switch.

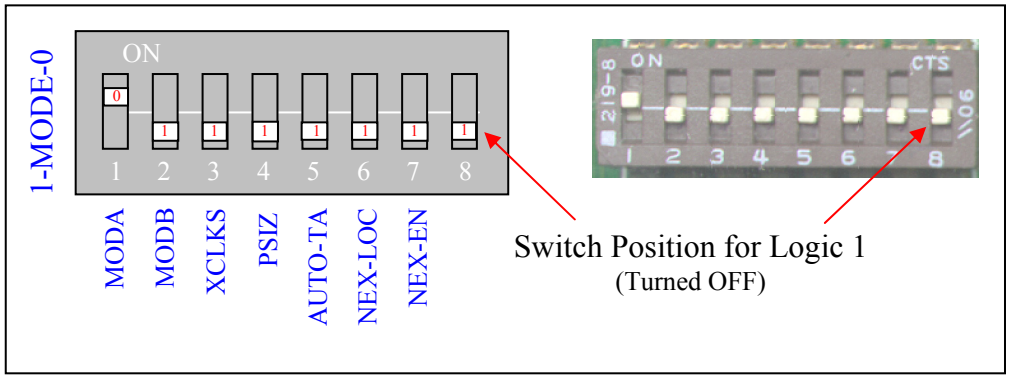
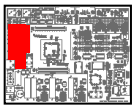


Figure 2-10 Reset Configuration (Mode) Switch

2.9 JTAG and Nexus Configuration (J13, J18)

The JTAG and NEXUS connectors are located on the left hand edge of the EVB.



The EVB has two JTAG connectors supporting both the 14 and 20 pin configurations. There are also two Nexus "mictor" connector footprints, allowing a Nexus probe to be connected to either of the possible multiplexed pin locations for Nexus on the MAC7100 family.

There are two generic jumpers associated with both JTAG and Nexus as shown in the tables below.

Table 2-10 JTAG / NEXUS Target Reset Routing Jumper J13

Jumper	Position	PCB Legend	Description
J13 (TRST)	1-2 **(D)**	BUFFER	TARGET reset signal is buffered to MCU RESET pin
	2-3	DIRECT	TARGET reset signal is connected directly to MCU RESET pin

Some JTAG and NEXUS probes have the ability to assert and also monitor the state of the MCU Reset line. This is not possible when the reset lines are buffered so jumper J13 is included to route the JTAG / NEXUS target reset signal directly to the MCU bi-directional reset pin. In order to use this feature, jumper J13 should be moved to position 2-3.

Table 2-11 JTAG / NEXUS TCLK Termination J18

Jumper	Position	PCB Legend	Description
J18 (TCLK Term)	1-2 **(D)**	VDDIO	JTAG / NEXUS TCLK signal is pulled to VDDIO via 10KΩ
	2-3	GND	JTAG / NEXUS TCLK signal is pulled to GND via 10KΩ

Some JTAG / NEXUS debug manufacturers require that the TCLK signal is pulled high and other require it is pulled low. Jumper J18 allows the user to select between the TCLK signal being pulled high (J18 position 1-2) or Low (J18 position 2-3). Please consult your debug probe manufacturer for details on the correct configuration.

2.9.1 JTAG Configuration

As mentioned above, the EVB supports both 14 and 20-way JTAG connectors. Either connector can be used without having to make any EVB jumper configuration changes.

When connecting or removing the JTAG debug interface, power must be removed from both the EVB and the JTAG debug interface.

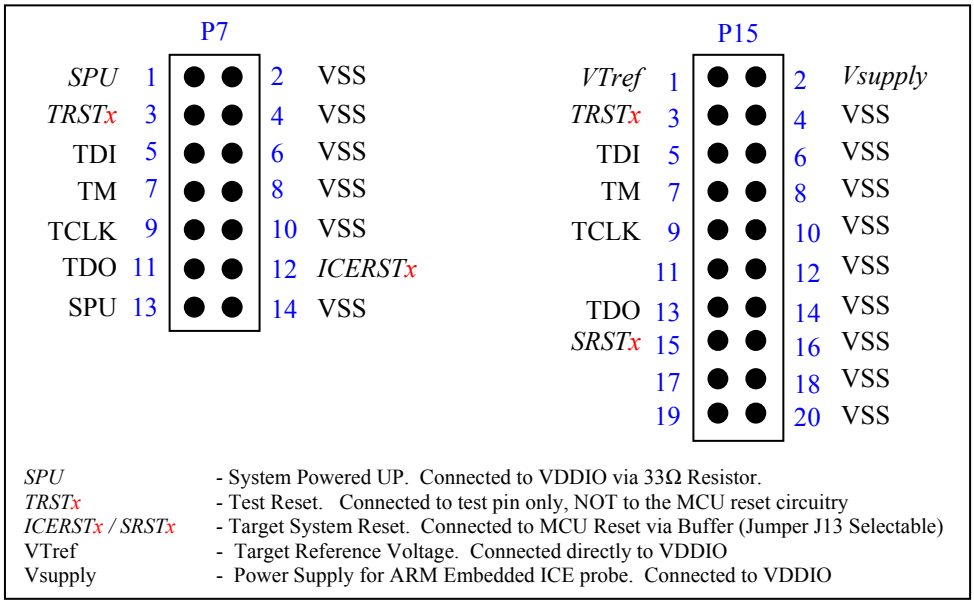


Figure 2-11 JTAG Connectors

2.9.2 Nexus Configuration (J14, J20)

The MAC7100 has a single Nexus 2+ debug module that is multiplexed between two physical locations, PortA and PortE. The EVB also has a connector fitted in both of these port positions. This allows the user to select which port pins may be used in order to support Nexus. Whatever port is configured for Nexus, it is important that you do NOT attempt to use the respective pins for any other purpose!

The following table shows the pins used for each Nexus configuration and details the EVB setup.

Table 2-12 Nexus Connectors

Nexus Port	Pins Used by Nexus	Functionality Lost	SW1 "NEX-LOC"	EVB Connector Used
PortA	PA[0..6]	PortA / Databus [0..6]	LOW (Switch = ON)	P6 – "NEXUS1(PA)"
PortE	PE[0..6]	PortE / ADC [0..6]	HIGH (Switch = OFF)	P16 – "NEXUS2(PE)"

The Nexus module must be made available for use by ensuring that the reset configuration switch (SW7), position 7 "NEX-EN" is high (switch is in OFF position). See section 2.8 for details.

Important Configuration Notes:

PortA Config When the EVB / MCU is configured to use the primary Nexus port (PortA), the upper byte of the Data bus, Data[8..15], is available for use. On the EVB however, all of the external memories are configured for 16-bit port width and will not function correctly when accessed by an 8-bit port. Therefore, **the external memory must be disabled if Nexus is used in the PortA configuration** (see section 2.10 for details). PortA[0..6] should not be connected to any other hardware whilst using this port for Nexus.

PortE Config When the MCU is configured to use the secondary Nexus port (PortE / ADC), **jumper J17 (RV1) must be removed** in order to prevent any contention between resistor RV1 and PortE[0]. PortE[0..6] should NOT be connected to any other hardware whilst using this port for Nexus.

When the NEXUS port is enabled, the EVTI*x* signal must be pulled high to prevent Nexus mode being inadvertently entered. As the Nexus pins are shared with other MCU port functions, these pull-ups must be selectable so they can be disabled when the respective port is not being used for Nexus. Jumpers are provided to enable the EVTI*x* pullup resistor for each port.

Table 2-13 EVTI Termination Enable Jumpers J14, J20

Jumper	Position	Description
J14 (EVTI Term Nexus 1)	FITTED	EVTI*x* Signal for Primary Nexus port (PA) is pulled high
	REMOVED **(D)**	EVTI*x* Signal for Primary Nexus port is not terminated
J20 (EVTI Term Nexus 2)	FITTED	EVTI*x* Signal for Secondary Nexus port (PA) is pulled high
	REMOVED **(D)**	EVTI*x* Signal for Secondary Nexus port is not terminated

The default configuration is NO pullup resistor is enabled. It is up to the user to determine what Nexus port will be used.

*Note – whenever a Nexus port is not going to be used, the respective EVTI*x *pullup resistor should be disabled by removing the relevant jumper.*

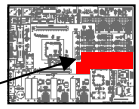
The following table details the pinout of the Nexus connector. (UBatt is connected to the main EVB power supply line via a resistor).

Table 2-14. NEXUS Debug Connector Pinout

Pin No	Function	Pin No	Function
1	Reserved	2	Reserved
3	Reserved	4	Reserved
5	Vendor I/O-0	6	CLKOUT
7	Vendor I/O-2	8	Vendor I/O-3
9	MCU Reset*x*	10	EVTI*x*
11	TDO	12	VREF (VDD Core)
13	Vendor I/O-4	14	RDY
15	TCLK	16	*N/C (MD0[7])*
17	TMS	18	*N/C (MDO[6])*
19	TDI	20	*N/C (MDO[5])*
21	MCU TRST*x*	22	*N/C (MDO[4])*
23	Vendor I/O-1	24	*N/C (MDO[3])*
25	*N/C (MDI[3])*	26	*N/C (MDO[2])*
27	*N/C (MDI[2])*	28	MDO[1]
29	*N/C (MDI[1])*	30	MDO[0]
31	UBATT (VDD IN, 7-12V)	32	EVTO*x*
33	UBATT (VDD IN, 7-12V)	34	MCK0
35	Tool I/O-0	36	*N/C (MSEO1)*
37	VSTBY (VDD Core)	38	MSEO

2.10 External Memory Configuration

The External Memory section is located in the lower right quarter of the EVB, below the bank of user connectors.



The following diagram shows the external memory implementation on the EVB.

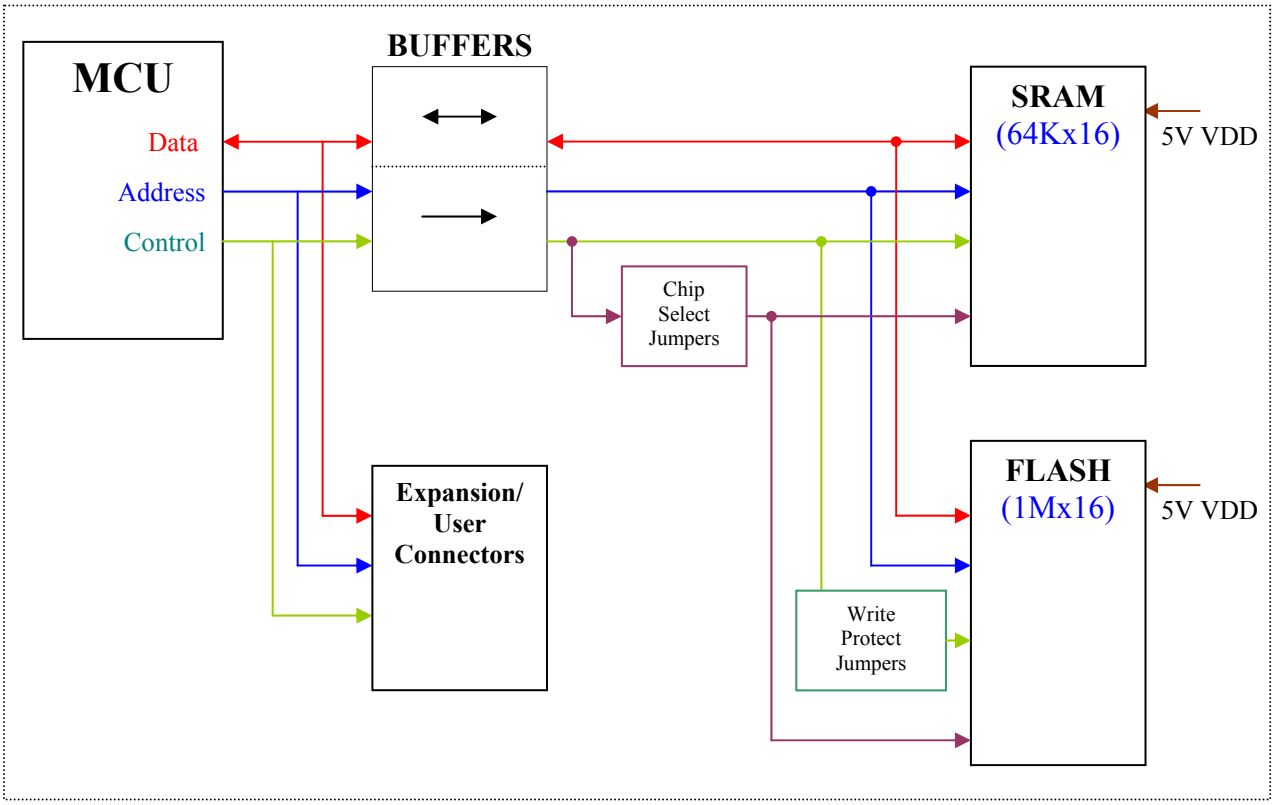


Figure 2-12 External Memory Scheme

2.10.1 Buffer Control (J26)

The MAC7111 MCU has a maximum output load capacitance of between 25 and 30pF on the external bus interface signals. In order not to exceed this loading specification on the EVB, all of the EBI signals to the external SRAM and FLASH (and Ethernet controller) are buffered. Note that the signals to the expansion connectors and user connectors remain un-buffered for two reasons:

(1) The EBI signals are multiplexed with bi-directional single chip mode peripherals
(2) The un-buffered interface provides a "true" MCU interface to the user.

Note – If you are interfacing to the EBI via the expansion or user connectors, you must ensure that the loading capacitance on each of the EBI signals does not exceed the specification, bearing in mind that the EVB buffers used on the EBI signals already have an input capacitance of approximately 8pF.

When the EVB is used in Single chip mode, the buffers must be disabled otherwise conflicts will occur between single chip functionality and the buffers. This can be achieved by REMOVING jumper J26 as shown in the table below. The default configuration enables the buffers, assuming the board will be used in expanded mode.

Table 2-15 EBI Buffer Control Jumper J26

Jumper	Position	Description
J26 (VDD-BUFF)	FITTED **(D)**	EBI External Memory Buffers are ENABLED
	REMOVED	EBI Buffers are DISABLED (Required in Single Chip Mode)

2.10.2 Chip Select Control (J24)

The EVB incorporates a flexible chip select routing scheme as shown below, allowing any of the three MAC7111 chip selects to be routed to either the RAM or the FLASH. The way the jumper is configured automatically prevents the same MCU chip select, inadvertently being assigned to both memories. The default configuration is shown. Chip select CS0*x* is routed to the external EVB FLASH and Chip select CS1*x* is routed to the external EVB SRAM. To re-configure the chip select mapping, please refer to the table below.

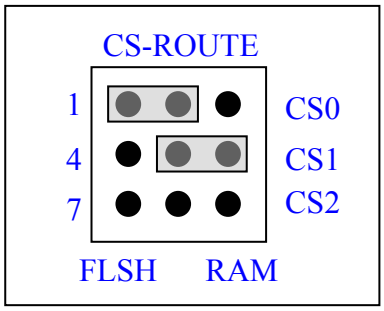


Figure 2-13 Chip Select Routing

Table 2-16 Chip Select Jumper J24

Jumper	Position	Chip Select	Routing	Description
J24 (CS-Route)	1-2 **(D)**	CS0*x*	FLASH	Chip Select CS0*x* is routed to the EVB FLASH
	2-3		RAM	Chip Select CS0*x* is routed to the EVB SRAM
	4-5	CS1*x*	FLASH	Chip Select CS1*x* is routed to the EVB FLASH
	5-6 **(D)**		RAM	Chip Select CS1*x* is routed to the EVB SRAM
	7-8	CS2*x*	FLASH	Chip Select CS2*x* is routed to the EVB FLASH
	8-9		RAM	Chip Select CS2*x* is routed to the EVB SRAM

Note – Care should be taken that the MCU Chip selects chosen for FLASH and RAM are not used elsewhere on any external hardware. The Ethernet controller uses CS2x if enabled (see section 2.11)

2.10.3 External SRAM Configuration (J35)

The EVB is fitted with a single 64Kx16 asynchronous SRAM giving a total memory space of 128Kbytes. This is configured as a 16-bit port and as such**, the MCU chip select being used for the SRAM must also be configured as a 16-bit port**. The SRAM circuitry supports both 8-bit and 16-bit accesses within the 16-bit port. See section 2.10.2 for details on how to select the desired chip select for SRAM on the EVB.

As this EVB provides a reference design platform, 5V SRAM devices were chosen which, in a standalone design, could directly interface to the MCU without the requirement for any buffering. In practice, a 3.3V SRAM device could have been used on the EVB as the buffers provide sufficient drive levels.

If the VDDIO regulator voltage drops below 5V when used in variable voltage mode, the SRAM devices MUST be disabled or unpredictable operation will occur. Similarly the SRAM must be disabled when the EVB is used in single chip mode. Jumper J35 provides a mechanism for disabling the SRAM.

Table 2-17 SRAM Power Supply Jumper J35

Jumper	Position	Description
J35 (VDD-SRAM)	FITTED **(D)**	EVB External SRAM is powered (enabled)
	REMOVED	SRAM is disabled. Requirement if S/C mode or VDDIO Variable Mode

Note- The SRAM MUST be disabled if VDDIO is less than 5V or the EVB is used in single chip mode.

Table 2-20 details pin compatible 5V asynchronous SRAM devices that may be used on the EVB.

Table 2-18 SRAM Pin Compatible Devices

Manufacturer	32K x 16	64K x 16
Cypress	CYC1020B	CYC1021B
IDT	N/A	IDT71016

2.10.4 External FLASH Configuration (J31, J33, J34)

The EVB is fitted with a single 1Mx16 asynchronous FLASH memory giving a total memory space of 2Mbytes. This is configured as a 16-bit port and, like the SRAM, **the MCU chip select assigned for the FLASH must also be configured as a 16-bit port. The FLASH circuitry is only designed to support 16-bit aligned accesses.** Any other access types must be avoided as these will result in incorrect data being read or written to the FLASH memory.

As with the SRAM, a 5V FLASH device has been chosen for use on the EVB. If the VDDIO regulator voltage drops below 5V when used in variable mode, the FLASH devices MUST be disabled or unpredictable operation will occur. The FLASH must also be disabled when the EVB is used in single chip mode using jumper J33.

Two additional jumpers provide a hardware mechanism for write protection. J34 controls read / write for the complete FLASH and J31 provides additional boot block protection (AM29F400B Flash only). By default, the complete FLASH memory block is un-protected.

Table 2-19 FLASH Control Jumpers

Jumper	Position	Description
J33 (VDD-FLASH)	FITTED **(D)** REMOVED	EVB External FLASH is powered (enabled) FLASH is disabled. Requirement if S/C mode or VDDIO Variable Mode
Flash Write Enable		
J31 (BOOT)	FITTED **(D)** REMOVED	FLASH Boot Block (AM29F400B) is set to read / write FLASH Boot Block (AM29F400B) can only be read
J34 (ALL)	FITTED **(D)** REMOVED	Complete FLASH is set to read / write (Boot Block Controlled By J31) Complete FLASH is set to read only

Note – In order for the flash boot block to be written on the AM28F400B device, BOTH jumpers J31 and J34 must be fitted.

Table 2-20 details pin compatible AMD 5V asynchronous FLASH devices that may be used on the EVB.

Table 2-20 AMD Flash Pin Compatible Devices

Part Number	Flash Size
AM29F160D*	16MBit (2M Bytes)
AM29F800B	8M Bit (1M Bytes)
AM29F400B	4M Bit (512K Bytes)

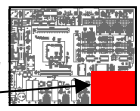
* Fitted by default

The AMD flash devices provide an easy in-system programming mechanism allowing the flash to be programmed and erased using commands sent to the flash via the MAC7100 external bus. Many debugger manufacturers provide automated external flash programming functionality, allowing the user to program the flash without having to manually control the programming command sequence. Please consult your debugger manufacturer for details.

No additional programming voltage is require to program the external flash however the write enable jumpers J34 (and if applicable J31) must be fitted before programming can take place.

2.11 Ethernet Controller Configuration (Jumpers J36, J37, J38, J39, J40)

The Ethernet controller circuitry is located in the bottom right area of the EVB. The Control jumpers are located in a box titled "ETHERNET"



There is a memory mapped Ethernet controller on the EVB, configured as shown in the block diagram below.

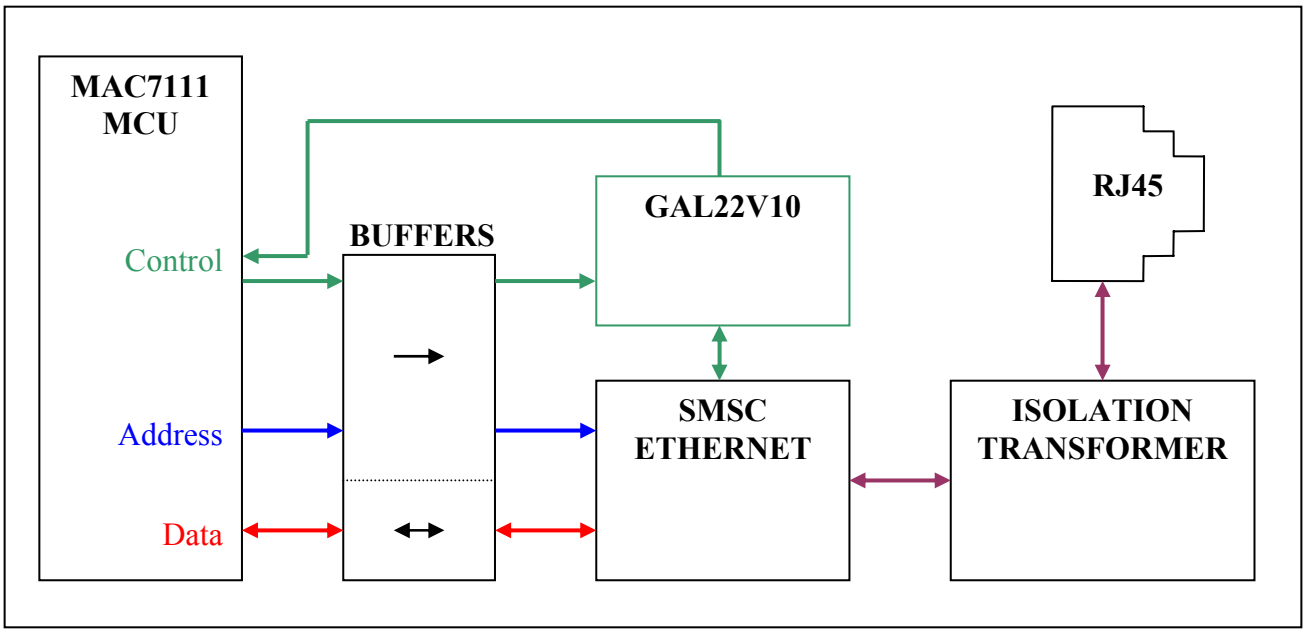


Figure 2-14 Ethernet Controller Block Diagram

The Ethernet controller used on the EVB is an SMSC LAN91C111-NE (Full Duplex, 10/100Mbit) device, configured for asynchronous bus mode in order to be compatible with the MAC7111 external bus. The MAC7111 cannot interface directly to the Ethernet controller as the control signals are generally active high on the Ethernet controller but active low on the MCU. In addition, some of the Ethernet controller signals are generated from multiple MCU signals. The GAL22V10 PLD (programmable logic device) is used to provide this MCU / Ethernet controller interface. The PLD also provides an input from the Target TA*x* signal, asserting the MCU TA*x* line whenever the Target TA or Ethernet TA signals are asserted.

Note - the Address / Data and Control signals to the Ethernet controller (and PLD) are buffered using the same set of buffers used for the external SRAM and FLASH detailed in section 2.10.1. These buffers must therefore be enabled (and the MCU running in expanded mode) before the Ethernet controller can be used.

The Ethernet controller and PLD are powered from the 3.3V EVB supply and as such, the 3.3V regulator must be enabled for the Ethernet controller circuitry to work.

There are 5 jumpers associated with the Ethernet circuitry as shown in Table 2-21 below. Jumper J36 is used to apply power to the Ethernet controller. When the MCU is used in single chip mode, or the Ethernet controller is not required, this jumper should be removed. Jumper J37 and J38 are used to connect the MCU IRQ*x* and MCU TA*x* signals to the PLD. Again, if the Ethernet controller is required, these jumpers must be fitted. Note that the PLD has these pins configured as open-drain output. Jumper J39 is used to apply power to the PLD and jumper J40 is used to connect the MCU chip select CS2 to the PLD which in turn is used to control the Ethernet Controller (as before, both these jumpers must be fitted for the Ethernet controller to function).

Table 2-21 Ethernet Circuit Control Jumpers

Jumper	Position	Description
J36 (VDD-ENET)	FITTED **(D)**	Ethernet Controller is powered (enabled)
	REMOVED	Ethernet Controller is disabled – Requirement in Single Chip mode
J37 (IRQx)	FITTED **(D)**	Ethernet Controller IRQ signal is connected to MCU IRQ*x* line
	REMOVED	Ethernet Controller IRQ signal is NOT connected to MCU IRQ*x* line
J38 (TAx)	FITTED **(D)**	Ethernet Controller and Target TA signals connected to MCU TA*x* line
	REMOVED	Ethernet Controller and Target TA signals NOT connected to MCU TA*x* line
J39 (VDD-PLD)	FITTED **(D)**	GAL22V10 is enabled (required if Ethernet controller or target TA required)
	REMOVED	GAL22V10 is disabled (Target TA or Ethernet controller will not function)
J40 (CS2x)	FITTED **(D)**	MCU Chip Select CS2*x* is routed to the Ethernet Controller via the GAL22V10
	REMOVED	MCU Chip Select CS2*x* is NOT connected to the Ethernet controller.

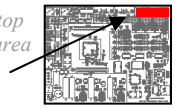
By default, the Ethernet controller circuit is fully enabled with all the jumpers shown in Table 2-21 fitted.

Notes:

- *Care should be taken to ensure that MCU Chip Select CS2x is not used for any other purpose if the Ethernet controller is used.*
- *The EVB buffers must be enabled in order to use the Ethernet controller.*
- *If the MCU is used in single chip mode, the Ethernet controller should be disabled.*

2.12 CAN Configuration (J2, J3, J4)

The CAN section is located at the top right hand edge of the EVB in an area marked "CAN".



The EVB has a Philips PCA82C250T high speed physical CAN interface driver on the MCU CAN-A and CAN-B channels. These are pre-configured for high speed operation by tying Pin8 of each CAN transceiver to ground via a zero ohm resistor. If required, these resistors can be changed to provide slope control mode of operation. See the EVB schematics for details.

Each CAN transceiver circuit has its CAN bus signals routed to a standard 0.1" connector at the top edge of the EVB. Connector P1 provides the CAN bus level signal interface for CAN-A and connector P2 for CAN-B. The pinout of these connectors is detailed below. Care should be taken NOT to confuse these connectors with jumper headers!

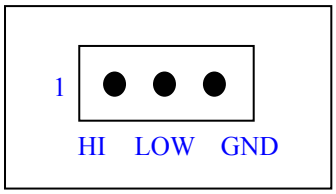


Figure 2-15 CAN Physical Interface Connector

Each of the MCU signals to the CAN transceivers is jumpered, allowing the CAN transceiver to be isolated if that MCU port is not configured or used for CAN operation. There is a 2x2 jumper for each CAN channel as shown in the table below. In addition, there is a global CAN power jumper (J3) which is used to completely remove power from both CAN transceivers.

Table 2-22 CAN Control Jumpers

Jumper	Legend	Position	Description
J2 (CAN-A) ***Posn 1-2***	**TX**	FITTED **(D)** REMOVED	MCU CNTX-A is connected to CAN controller A MCU CNTX-A is NOT routed to CAN controller .
J2 (CAN-A) ***Posn 3-4***	**RX**	FITTED **(D)** REMOVED	MCU CNRX-A is connected to CAN controller A MCU CNRX-A is NOT routed to CAN controller.
J4 (CAN-B) ***Posn 1-2***	**TX**	FITTED **(D)** REMOVED	MCU CNTX-B is connected to CAN controller B MCU CNTX-B is NOT routed to CAN controller .
J4 (CAN-B) ***Posn 3-4***	**RX**	FITTED **(D)** REMOVED	MCU CNRX-B is connected to CAN controller B MCU CNRX-B is NOT routed to CAN controller.
J3 (VDD-CAN)		FITTED **(D)** REMOVED	Power is applied to both CAN transceivers No power is applied to CAN transceivers

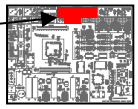
The default position is all jumpers fitted, connecting the MCU CAN A and CAN B signals to the CAN physical interface. If the MCU is configured such that a CAN channel is configured as a normal I/O port (eg PortG 4,5 for CAN-A), the respective jumpers must be removed or conflicts will occur. If neither CAN channel is being used, Jumper J3 should be removed to disable both CAN transceivers.

Notes:

- *The Philips CAN devices fitted to the EVB will only function with VDDIO connected to 5V. If the EVB is used in variable VDDIO mode, the CAN devices MUST be disabled using jumper J3.*
- *Care should be taken when fitting jumpers to the 2x2 headers as they can easily be fitted in the incorrect orientation. Jumper headers on J2 and J4 are fitted vertically.*

2.13 RS232 Configuration (J5, J6, J9)

The RS232 circuitry is located in the top centre edge of the EVB in an area titled "SCI".



The EVB has a single MAX232CSE RS232 transceiver device, providing RS232 signal translation for the MCU SCI channels A and B.

Each of the two RS232 outputs from the MAX232 device is connected to a 9-way female D-Type connector, allowing a direct RS232 connection to a PC or terminal. Connector P3 provides the RS232 level interface for MCU SCI-A and P4 for MCU SCI-B. The pinout of these connectors is detailed below. Note that hardware flow control is not supported on this implementation.

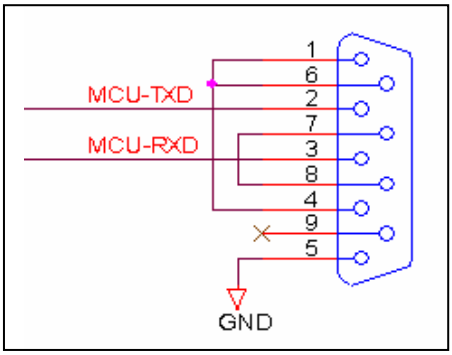


Figure 2-16 RS232 Physical Interface Connector

As with the CAN circuitry, each of the MCU signals to the RS232 transceiver is jumpered to allow individual isolation if required. There is also a global power jumper J5 controlling the power supply to the RS232 transceiver. This is shown in Table 2-23 below.

Table 2-23 RS232 Control Jumpers

Jumper	Legend	Position	Description
J6 (SCI-A) ***Posn 1-2***	**TX**	FITTED **(D)** REMOVED	MCU TXD-A is routed via MAX232 to P3 MCU TXD-A signal is not connected to MAX232
J6 (SCI-A) ***Posn 3-4***	**RX**	FITTED **(D)** REMOVED	MCU RXD-A is routed via MAX232 to P3 MCU RXD-A signal is not connected to MAX232
J9 (SCI-B) ***Posn 1-2***	**TX**	FITTED **(D)** REMOVED	MCU TXD-B is routed via MAX232 to P4 MCU TXD-B signal is not connected to MAX232
J9 (SCI-B) ***Posn 3-4***	**RX**	FITTED **(D)** REMOVED	MCU RXD-B is routed via MAX232 to P4 MCU RXD-B signal is not connected to MAX232
J5 (VDD-SCI)		FITTED **(D)** REMOVED	Power is applied to the MAX232 transceiver No power is applied to the MAX232 transceiver

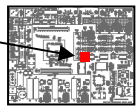
The default configuration is all jumpers fitted, connecting the MCU SCI- A and SCI-B signals to the physical RS232 connectors via the MAX232 device. If the MCU is configured such that SCI channel A or B is set as a normal I/O port, the respective jumpers must be removed from J6 or J9 or conflicts will occur. If neither channel is being used as an SCI, jumper J5 should be removed to disable the MAX232 transceiver device.

Notes:

- *The MAC232 device fitted to the EVB will only function with VDDIO connected to 5V. If the EVB is used in variable VDDIO mode, the MAX232 device MUST be disabled using jumper J5.*
- *Care should be taken when fitting jumpers to the 2x2 headers as they can easily be fitted in the incorrect orientation. Jumper headers on J6 and J9 are fitted vertically.*

2.14 Termination Resistor Control (J28)

The Termination control jumper is located to the bottom right of the MCU and MCU SUPPLY jumpers.



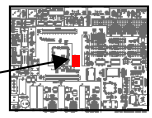
In expanded mode, the MCU EBI control signals must be pulled high. When the EVB is used in single chip mode however, you may require the respective port pins to be left floating with the external pullup resistors disabled. Jumper J28 controls the power to these pullup resistors. When the jumper is removed, the pullup resistors are no longer activated.

Table 2-24 EBI Pullup Resistor Control (J29)

Jumper	Position	Description
J28 (Exp-Mode Term)	FITTED **(D)** REMOVED	EVB EBI signals are pulled high (Expanded Mode) EBI signals are not pulled high (single Chip Mode)

2.15 MCU TA Jumper (J25)

The MCU TA jumper is located close to the bottom right hand corner of the MCU.



Jumper J25 is used for test purposes only and should remain in position 1-2 for normal operation. Moving this jumper will cause operational issues with the MCU in expanded mode.

Table 2-25 Jumper J25

Jumper	Position	PCB Legend	Description
J25 (TAx)	1-2 **(D)** 2-3	MAC 711	MCU TA*x* signal is connected TEST PURPOSES ONLY – DO NOT USE

3. Default Jumper Summary Table

The following table details the DEFAULT jumper configuration of the EVB as explained in detail in section 2.

Table 3-1 Default Jumper Positions

Jumper	Position	PCB Legend	Description
J1 (ABORT)	FITTED **(D)**		ABORT switch is connected to MCU XIRQ line
J2 (CAN-A) ***Posn 1-2***	FITTED **(D)**	TX	MCU CNTX-A is connected to CAN controller A
Posn 3-4	FITTED **(D)**	RX	MCU CNRX-A is connected to CAN controller A
J3 (VDD-CAN)	FITTED **(D)**		Power is applied to both CAN transceivers
J4 (CAN-B) ***Posn 1-2***	FITTED **(D)**	TX	MCU CNTX-B is connected to CAN controller B
Posn 3-4	FITTED **(D)**	RX	MCU CNRX-B is connected to CAN controller B
J5 (VDD-SCI)	FITTED **(D)**		Power is applied to the MAX232 transceiver
J6 (SCI-A) ***Posn 1-2***	FITTED **(D)**	TX	MCU TXD-A is routed via MAX232 to P3
Posn 3-4	FITTED **(D)**	RX	MCU RXD-A is routed via MAX232 to P3
J7 (VRL)	1-2 **(D)**	EVB	MCU VRL is connected to EVB analogue GND
J8 (VRH)	1-2 **(D)**	EVB	MCU VRH is connected to EVB VDDIO
J9 (SCI-B) ***Posn 1-2***	FITTED **(D)**	TX	MCU TXD-B is routed via MAX232 to P4
Posn 3-4	FITTED **(D)**	RX	MCU RXD-B is routed via MAX232 to P4
J10 (LVI Reset)	FITTED **(D)**		RESET signal from LVI drives the MCU RESET line
J11 (VDDIO)	1-2 **(D)**	ENABLE	VDDIO regulator output is monitored by LVI
J12 (3.3V)	1-2 **(D)**	ENABLE	3.3V regulator output is monitored by LVI
J13 (TRST)	1-2 **(D)**	BUFFER	JTAG Target Reset signal is buffered to MCU RESET pin
J14 (EVTI Term Nex1)	REMOVED **(D)**		EVTI Signal for Primary Nexus port is not terminated
J15 (I/O)	FITTED **(D)**		Connects EVB VDDIO regulator output to MCU VDDX pins
J16 (PF-LED)	ALL FITTED (D)		Connects PF[8..15] to LED's DS[2..9]
J17 (RV1)	FITTED **(D)**		Output from RV1 is applied to MCU PE0 / AN00 pin
J18 (TCLK Term)	1-2 **(D)**	VDDIO	JTAG / NEXUS TCLK signal is pulled to VDDIO via 10KΩ
J19 (ADC)	FITTED **(D)**		Connects EVB VDDIO regulator output to MCU VDDA pins
J20 (EVTI Term Nex2)	REMOVED **(D)**		EVTI Signal for Secondary Nexus port is not terminated
J21 (REG)	1-2 **(D)**		Connects EVB VDDIO regulator output to MCU VDDR pins
J22 (2.5V)	REMOVED **(D)**		MCU On Chip regulator powers VDD2.5
J23 (Y2 PWR)	REMOVED **(D)**		Oscillator Module Y1 is not powered (disabled)
J24 (CS-Route)	1-2 **(D)**	CS0 / FLSH	Chip Select CS0*x* is routed to the EVB FLASH
	5-6 **(D)**	CS1 / RAM	Chip Select CS1*x* is routed to the EVB SRAM
J25 (TAx)	1-2 **(D)**	MAC 711	MCU TA*x* signal is connected *(Do not move this jumper)*
J26 (VDD-BUFF)	FITTED **(D)**		EBI External Memory Buffers are ENABLED
J27 (PLL)	REMOVED **(D)**		MCU On Chip regulator powers VDDPLL
J28 (Exp-Mode Term)	FITTED **(D)**		EVB EBI signals are pulled high (Expanded Mode)
J29 (EXTAL)	1-2 **(D)**	Y1	MCU EXTAL connected to local oscillator circuit
J30 (XTAL)	FITTED **(D)**		MCU XTAL connected to local oscillator circuit
J31 (BOOT)	FITTED **(D)**		External FLASH Boot Block (AM29F400B) set to read / write
J32 (OSC SEL)	1-2 **(D)**	Y2	External EXTAL routed from Oscillator Module
J33 (VDD-FLASH)	FITTED **(D)**		EVB External FLASH is powered (enabled)
J34 (ALL)	FITTED **(D)**		Complete External FLASH is set to read / write
J35 (VDD-SRAM)	FITTED **(D)**		EVB External SRAM is powered (enabled)
J36 (VDD-ENET)	FITTED **(D)**		Ethernet Controller is powered (enabled)
J37 (IRQx)	FITTED **(D)**		Ethernet Controller IRQ signal is connected to MCU IRQ*x* line
J38 (TAx)	FITTED **(D)**		Ethernet Controller and Target TA signals connected to MCU TA*x*
J39 (VDD-PLD)	FITTED **(D)**		GAL22V10 PLD is enabled
J40 (CS2x)	FITTED **(D)**		MCU Chip Select CS2*x* is connected to the Ethernet Controller
J41 (2.5V)	1-2 **(D)**	ENABLE	2.5V regulator output is Enabled
J42 (3.3V)	1-2 **(D)**	ENABLE	3.3V regulator output is Enabled
J43 (VDDIO)	1-2 **(D)**	5V	VDDIO regulator is configured as 5.0V fixed mode.
J44 (PD2-EN)	REMOVED **(D)**		CLKOUT Impedance matching resistor is active
J45 (PLL-DIS)	REMOVED **(D)**		MCU PLL Circuitry is enabled

4. Jumper Configurations for EVB Operating Mode

This table details specific jumper positioning requirements for various EVB operating configurations / modes.

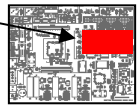
Note - Where "Any" is written in the table, this means the jumper can be configured as required by the user. It does NOT infer that the EVB will function correctly with the jumper in any position.

Table 4-1 Critical Jumper Positions

Jumper	Single Chip	Expanded	VDDIO=5v	VDDIO<5v
J1 (ABORT)	Any	Any	Any	Any
J2 (CAN-A)	Any	Any	Any	**REMOVED**
J3 (VDD-CAN)	Any	Any	Any	**REMOVED**
J4 (CAN-B)	Any	Any	Any	**REMOVED**
J5 (VDD-SCI)	Any	Any	Any	**REMOVED**
J6 (SCI-A)	Any	Any	Any	**REMOVED**
J7 (VRL)	Any	Any	Any	Any
J8 (VRH)	Any	Any	Any	Any
J9 (SCI-B)	Any	Any	Any	**REMOVED**
J10 (LVI Reset)	Any	Any	Any	Any
J11 (VDDIO)	Any	Any	Any	**2-3**
J12 (3.3V)	Any	Any	Any	Any
J13 (TRST)	Any	Any	Any	Any
J14 (EVTI Term Nex1)	Any	Any	Any	Any
J15 (I/O)	Any	Any	Any	Any
J16 (PF-LED)	Any	Any	Any	Any
J17 (RV1)	Any	Any	Any	Any
J18 (TCLK Term)	Any	Any	Any	Any
J19 (ADC)	Any	Any	Any	Any
J20 (EVTI Term Nex2)	Any	Any	Any	Any
J21 (REG)	Any	Any	Any	Any
J22 (2.5V)	Any	Any	Any	Any
J23 (Y2 PWR)	Any	Any	Any	Any
J24 (CS-Route)	**REMOVED**	Any	Any	**REMOVED**
J25 (TAx)	**1-2**	**1-2**	**1-2**	**1-2**
J26 (VDD-BUFF)	**REMOVED**	Any	Any	Any
J27 (PLL)	Any	Any	Any	Any
J28 (Exp-Mode Term)	**REMOVED**	Any	Any	Any
J29 (EXTAL)	Any	Any	Any	Any
J30 (XTAL)	Any	Any	Any	Any
J31 (BOOT)	Any	Any	Any	Any
J32 (OSC SEL)	Any	Any	Any	Any
J33 (VDD-FLASH)	**REMOVED**	Any	Any	**REMOVED**
J34 (ALL)	Any	Any	Any	Any
J35 (VDD-SRAM)	**REMOVED**	Any	Any	**REMOVED**
J36 (VDD-ENET)	**REMOVED**	Any	Any	Any
J37 (IRQx)	**REMOVED**	Any	Any	Any
J38 (TAx)	**REMOVED**	Any	Any	Any
J39 (VDD-PLD)	**REMOVED**	Any	Any	Any
J40 (CS2x)	**REMOVED**	Any	Any	Any
J41 (2.5V)	Any	Any	Any	Any
J42 (3.3V)	Any	Any	Any	Any
J43 (VDDIO)	Any	Any	Any	Any
J44 (PD2-EN)	Any	Any	Any	Any
J45 (PLL-DIS)	Any	Any	Any	Any

5. User Connector Descriptions

The User connectors are grouped together in the right hand middle section of the EVB.



This section details the pinout for the user connectors on the EVB. All of the user connectors are located to the right of the MCU and are all 0.1 inch pitch headers. Pins are grouped by Port functionality and the PCB legend clearly shows the single chip port number adjacent to each header pin.

5.1 Port A / DataBus (P12)

Table 5-1 Connector P12 – PortA / Databus

Pin No	PCB Legend	Pin Function	Pin No	PCB Legend	Pin Function
1 *	0	PA0 / DATA0 *	2 *	1	PA1 / DATA1 *
3 *	2	PA2 / DATA2 *	4 *	3	PA3 / DATA3 *
5 *	4	PA4 / DATA4 *	6 *	5	PA5 / DATA5 *
7 *	6	PA6 / DATA6 *	8	7	PA7 / DATA7
9	8	PA8 / DATA8	10	9	PA9 / DATA9
11	10	PA10 / DATA10	12	11	PA11 / DATA11
13	12	PA12 / DATA12	14	13	PA13 / DATA13
15	14	PA14 / DATA14 / EIMPS	16	15	PA15 / DATA15 / EIMACK
17	GND	GND	18	GND	GND

Notes:

- *If the EVB is used in expanded mode, the only connection to these pins should be for test / measurement equipment or for external bus interface purposes.*
- ** Indicates pin shared with Primary Nexus location. If this Nexus option is used, this pin must NOT be loaded. Nexus tools should ONLY be connected at the appropriate NEXUS Mictor connector, not at this header.*
- *Pins 14 and 15 (MCU Pins PA14, PA15) are used by the EVB reset configuration logic to determine the MCU EIM reset configuration. These pins must NOT be tied to power or ground OR pulled high or low using aggressive pullup / pulldown resistors.*

5.2 Port B / I^2C / SPI (P10)

Table 5-2 Connector P10 – PortB / I^2C / SPI

Pin No	PCB Legend	Pin Function	Pin No	PCB Legend	Pin Function
1	0	PB0 / SDA	2	1	PB1 / SCK
3	2	PB2 / SIN-A	4	3	PB3 / SOUT-A
5	4	PB4 / SCK-A	6	5	PB5 / SS-A
7	6	PB6 / PCS1-A	8	7	PB7 / PCS2-A
9	8	PB8 / PCSS-A	10	9	PB9 / SS-B
11	10	PB10 / PCSS-B	12	11	PB11 / PCS2-B
13	12	PB12 / PCS1-B	14	13	PB13 / SCK-B
15	14	PB14 / SOUT-B	16	15	PB15 / SIN-B
17	GND	GND	18	GND	GND

5.3 Port C / Address [0..15] (P13)

Table 5-3 Connector P13 – Port C / Address

Pin No	PCB Legend	Pin Function	Pin No	PCB Legend	Pin Function
1	0	PC0 / ADDR0	2	1	PC1 / ADDR1
3	2	PC2 / ADDR2	4	3	PC3 / ADDR3
5	4	PC4 / ADDR4	6	5	PC5 / ADDR5
7	6	PC6 / ADDR6	8	7	PC7 / ADDR7
9	8	PC8 / ADDR8	10	9	PC9 / ADDR9
11	10	PC10 / ADDR10	12	11	PC11 / ADDR11
13	12	PC12 / ADDR12	14	13	PC13 / ADDR13
15	14	PC14 / ADDR14	16	15	PC15 / ADDR15
17	GND	GND	18	GND	GND

Note – If the EVB is used in expanded mode, the only connection to these pins should be for test / measurement equipment or for external bus interface purposes

5.4 Port D / Address [16..21] / Control (P14 and J44)

Table 5-4 Connector P14 – Port D / Address / Control

Pin No	PCB Legend	Pin Function	Pin No	PCB Legend	Pin Function
1	0	PD0 / BS0*x* / MODB	2	1	PD1 / BS1*x* / MODA
3	CLKOUT	CLKOUT / XCLKS*x*	4	3	PD3 / XIRQ*x*
5	4	PD4 / IRQ*x*	6	5	PD5 / ADDR16
7	6	PD6 / ADDR17	8	7	PD7 / ADDR18
9	8	PD8 / ADDR19	10	9	PD9 / ADDR20
11	10	PD10 / ADDR21	12	11	PD11 / OE*x*
13	12	PD12 / CS2*x*	14	13	PD13 / CS1*x*
15	14	PD14 / CS0*x*	16	15	PD15 / RW*x*
17	RST-IN	Target RESET-IN*x* *	18	RST-OUT	MCU Reset-OUT*x* *[2]
19	MCU-TA	MCU TA*x* **	20	TGT-TA	Target TA*x* **
21	GND	GND	22	GND	GND

Notes:

- *If the EVB is used in expanded mode, the only connection to the ADDRESS / Control pins should be for test / measurement equipment or for external bus interface purposes.*
- *Pins 1,2 and 3 (MCU Pins PD0, PD1 and PD2) are used by the EVB reset configuration logic to determine the operating mode of the MCU. These pins must NOT be tied to power or ground OR pulled high or low using aggressive pullup / pulldown resistors.*
- ** **RST-INx** (pin 17) is connected to the Reset Buffering Input. **RST-OUTx** (Pin 18) is the buffered MCU reset signal. See section 2.7 for details.*
- *** **MCU-TAx** (Pin 19) is connected directly to the MCU TAx pin. This must be driven with an open-drain output only. **TGT-TAx** (Pin 20) is connected to the GAL22V10 and provides a non-open drain TA input. For **TGT-TAx** to function, the GAL22V10 must be configured as described in section 2.11.*

5.4.1 PD2 / CLKOUT impedance matching control (J44)

The MCU PD2/CLKOUT line has a series 33Ω resistor close to the MCU for CLKOUT impedance matching. If required, this resistor can be bypassed using jumper J44. The default position of this jumper is shown in the table below, with the jumper removed allowing impedance matching.

Table 5-5 PD2 / CLKOUT Termination Bypass Jumper

Jumper	Position	Description
J44 (PD2-EN)	FITTED	CLKOUT Impedance matching resistor is bypassed
	REMOVED **(D)**	CLKOUT Impedance matching resistor is active

5.5 Port E / ADC and Analogue Reference (P11 and J17)

Table 5-6 Connector P11 – Port E / ADC

Pin No	PCB Legend	Pin Function	Pin No	PCB Legend	Pin Function
1	0	PE0 / AN000 *	2	1	PE1 / AN001 *
3	2	PE2 / AN002 *	4	3	PE3 / AN003 *
5	4	PE4 / AN004 *	6	5	PE5 / AN005 *
7	6	PE6 /AN006 *	8	7	PE7 / AN007
9	8	PE8 /AN008	10	9	PE9 / AN009
11	10	PE10 / AN010	12	11	PE11 / AN011
13	12	PE12 / AN012	14	13	PE13 / AN013
15	14	PE14 / AN014	16	15	PE15 / AN015
17	VRH	USR-VRH **	18	VRL	USR-VRL **
19	GND	GND	20	GND	GND

Notes

- ** Pin shared with Secondary Nexus Location. If this Nexus option is used, this pin must NOT be loaded.* Nexus tools should ONLY be connected at the appropriate NEXUS Mictor connector, not at this header.
- ***** Pin 17 (VRH) and Pin 18 (VRL) provide a convenient point for the user to input high and low reference voltages for the ADC assuming that the ADC control jumpers are configured appropriately. See section 2.3 for details.***

To allow easy user evaluation of the ADC and to perform some simple tests, a 2K Ohm variable resistor (RV1) is provided which provides a voltage of between 0V and VDDIO onto ADC channel 0 (PE0). Jumper J17 can be used to disconnect this variable resistor if it is not required (or if PortE is to be used as a normal I/O Port). J11 and RV1 are located adjacent to connector P11.

Table 5-7 RV1 Connection Jumper J17

Jumper	Position	Description
J17 (RV1)	FITTED **(D)**	Output from variable resistor RV1 is applied to MCU PE0 / AN00 pin
	REMOVED	Output from RV1 is not connected to MCU (disabled)

5.6 Port F / EMIOS And User LED'S (P9, J16)

Table 5-8 Connector P9 – Port F / EMIOS

Pin No	PCB Legend	Pin Function	Pin No	PCB Legend	Pin Function
1	0	PF0 / EMIOS0 / NEX-PS	2	1	PF1 / EMIOS 1 / NEX-EN
3	2	PF2 / EMIOS 2	4	3	PF3 / EMIOS 3
5	4	PF4 / EMIOS 4	6	5	PF5 / EMIOS 5
7	6	PF6 / EMIOS 6	8	7	PF7 / EMIOS 7
9	8	PF8 / EMIOS 8	10	9	PF9 / EMIOS 9
11	10	PF10 / EMIOS 10	12	11	PF11 / EMIOS 11
13	12	PF12 / EMIOS 12	14	13	PF13 / EMIOS 13
15	14	PF14 / EMIOS 14	16	15	PF15 / EMIOS 15
17	GND	GND	18	GND	GND

Note - Pins 1 and 2 (MCU Pins PF0 and PF1) are used by the EVB reset configuration logic to determine the operating mode of the MCU. These pins must NOT be tied to power or ground OR pulled high or low using aggressive pullup / pulldown resistors.

8 LED's are provided to allow test and evaluation. These are connected to the upper byte of Port F (bits [8..15]). A jumper header (J16) is supplied to allow disconnection of these LED's if not required as shown in the diagram below. By default, all the jumpers are fitted.

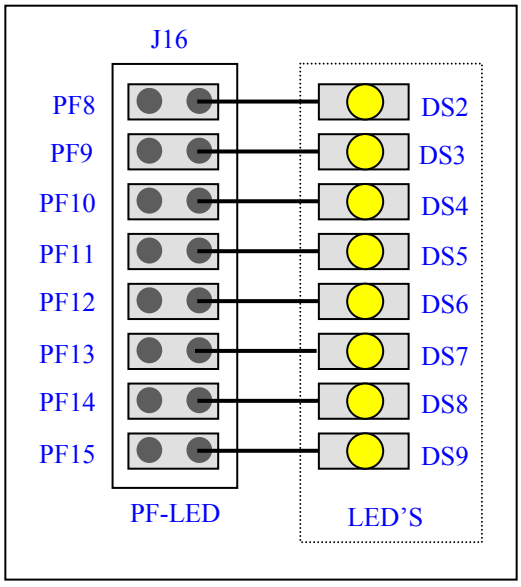


Figure 5-1 J16 and User LED control

Note – These LED's are ACTIVE low. A logic 0 must be driven out of the relevant port in order to illuminate the LED. They are connected via a resistor to VDDIO so if VDDIO is lowered (in variable voltage mode), the LED's will also get correspondingly dimmer.

5.7 Port G / CAN / SCI (P8)

Table 5-9 Connector P8 – Port G / CAN / SCI

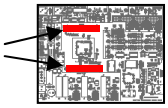
Pin No	PCB Legend	Pin Function	Pin No	PCB Legend	Pin Function
1	0	PG0 / RXD-B	2	1	PG1 / TXD-B
3	2	PG2 / RXD-A	4	3	PG3 / TXD-A
5	4	PG4 / CNTX-A	6	5	PG5 / CNRX-A
7	6	PG6 / CNTX-B	8	7	PG7 / CNRX-B
9	8	PG8 / CNTX-C	10	9	PG9 / CNRX-C
11	10	PG10 / CNTX-D	12	11	PG11 / CNRX-D
13	12	PG12 / RXD-D	14	13	PG13 / TXD-D
15	14	PG14 / RXD-C	16	15	PG15 / TXD-C
17	GND	GND	18	GND	GND

Notes:

- *The signals at connector P8 are MCU-LEVEL. For physical interface for SCI or CAN, please see sections 2.12 and 2.13*
- *When the Can or SCI physical interfaces are being used, the corresponding MCU level signal on connector P8 MUST be left unconnected or conflicts will occur.*

6. Expansion Connectors

The Expansion connectors are located above and below the MCU.



Two 120-way expansion connectors are fitted to the EVB, allowing connection of an MCU daughter-card or other board providing functionality enhancement. The pinout of these connectors is detailed below for reference.

All of the MCU power signals are routed to the expansion connectors after they have passed through the MCU supply isolation jumpers, thus allowing isolation of power supply lines to the daughter-card if required. Note the output from the 3.3V regulator is not jumpered.

The part numbers of possible connectors are detailed in Table 6-1 below.

Table 6-1 Expansion Connector Part Numbers

Connector Location	Height	Pitch	AMP Part Number
EVB	8mm	0.8mm	179031-5
Daughter Card	9mm	0.8mm	5-179009-5
	13mm	0.8mm	5-179010-5

Table 6-2 Expansion Connector 1 (P5)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	VDD3.3	2	VDDI/O	61	PD7 / ADD18	62	PD6 / ADD17
3	PC3 / ADDR3	4	GND	63	PE15 / AN15	64	GND
5	PC2 / ADDR2	6	PC1 / ADDR1	65	PE14 / AN14	66	
7		8	PC0 / ADDR0	67	PE13 / AN13	68	PE12 / AN12
9	GND	10	VDDI/O	69	GND	70	VDD2.5
11	PG7 / CNRX-B	12	PG6 / CNTX-B	71	PE11 / AN11	72	PE10 / AN10
13		14	PG11 / CNRX-D	73	MCU-VRL	74	MCU-VRH
15	VDD3.3	16	GND	75	USR-VRH	76	GND
17	PG10 / CNTX-D	18	PG9 / CNRX-C	77	USR-VRL	78	VDDA
19		20	PG8 / CNTX-C	79	VDDA	80	VDDA
21	GND	22	VDDI/O	81	GND	82	VDD2.5
23	PG5 / CNRX-A	24	PG4 / CNTX-A	83	PE9 / AN09	84	PE8 / AN08
25	PG3 / TXD-A	26		85	PE7 / AN07	86	PE6 / AN06
27	PG2 / RXD-A	28	GND	87	VDD3.3	88	GND
29	PG1 / TXD-B	30	PG0 / RXD-B	89	PE5 / AN05	90	PE4 / AN04
31		32	PG15 / TXD-C	91	PE3 / AN03	92	PE2 / AN02
33	GND	34	VDDI/O	93	GND	94	VDD2.5
35	PG14 / RXD-C	36	PA0 / DATA0	95		96	PE1 / AN01
37		38	PA1 / DATA1	97	PE0 / AN00	98	PA7 / DATA7
39	VDD3.3	40	GND	99		100	GND
41	PA2 / DATA2	42	PA3 / DATA3	101	PA8 / DATA8	102	PA9 / DATA9
43	PA4 / DATA4	44	PA5 / DATA5	103	PA10 / DATA10	104	PA11 / DATA11
45	GND	46	VDDI/O	105	GND	106	VDD2.5
47		48	PA6 / DATA6	107		108	PA12 / DATA12
49	TM	50	TCLK	109	PD5 / ADDR16	110	PC15 / ADDR15
51	TDO	52	GND	111	VDD3.3	112	GND
53		54	TDI	113		114	PC14 / ADDR14
55	PD10 / ADD21	56	PD9 / ADD20	115	PC13 / ADDR13	116	PC12 / ADDR12
57	GND	58	VDD2.5	117	GND	118	GND
59	PD8 / ADD19	60		119	GND	120	GND

Note: MCU-VRH and MCU-VRL are connected directly to the respective MCU pins. USR-VRH and USR-VRL are routed to pin 3 of the ADC selection jumpers J7 and J8.

Table 6-3 Expansion Connector 2 (P19)

Pin	Signal Name	Pin	Signal Name
1	VDD3.3	2	VDD2.5
3	PB0 / SDA	4	GND
5	PB1 / SCL	6	PB2 / SIN-A
7	PB3 / SOUT-A	8	
9	GND	10	VDD2.5
11	PB4 / SCK-A	12	PB5 / PCS0-A
13	PB6 / PCS1-A	14	PB7 / PCS2-A
15		16	GND
17	PB8 / PCS5-A	18	PF15 / EMIOS15
19	PF14 / EMIOS14	20	PF13 / EMIOS13
21	GND	22	VDD2.5
23		24	MTS12/PF12
25	PC4 / ADDR4	26	PC5 / ADDR5
27	VDD3.3	28	GND
29	PC6 / ADDR6	30	
31	PC7 / ADDR7	32	PF11 / EMIOS11
33	GND	34	VDD2.5
35	PF10 / EMIOS10	36	PF9 / EMIOS9
37		38	PF8 / EMIOS8
39	PF7 / EMIOS7	40	GND
41	PF6 / EMIOS6	42	PF5 / EMIOS5
43		44	PF4 / EMIOS4
45	GND	46	VDD2.5
47	PF3 / EMIOS3	48	PF2 / EMIOS2
49	PF1 / EMIOS1	50	PF0 / EMIOS0
51	VDD3.3	52	GND
53	PC8 / ADDR8	54	PC9 / ADDR9
55	PC10 / ADDR10	56	TGT-RESET*x*
57	GND	58	VDDI/O
59	PC11 / ADDR11	60	MCU-RESET*x*

Pin	Signal Name	Pin	Signal Name
61	PG12 / RXD-D	62	PG13 / TXD-D
63		64	GND
65	VDDR	66	VDDR
67	VDDR	68	VDDR
69	GND	70	VDDI/O
71		72	RESET-OUT*x*
73	VDDPLL	74	VDDPLL
75	VDDPLL	76	GND
77	EXT-EXTAL	78	
79	PA15 / DATA15	80	
81	GND	82	VDDI/O
83	PA14 / DATA14	84	PA13 / DATA13
85	PD11 / OE*x*	86	PD12 / CS2*x*
87		88	GND
89		90	PD0 / BS0*x*
91	PD1 / BS1*x*	92	PB9 / PCS0-B
93	GND	94	VDDI/O
95	PB10 / PCS5-B	96	
97	PB11 / PCS2-B	98	PB12 / PCS1-B
99	VDD3.3	100	GND
101	PB13 / SCK-B	102	PB14 / SOUT-B
103		104	PB15 / SIN-B
105	GND	106	VDDI/O
107	TA	108	CLKOUT
109	PD3 / XIRQ*x*	110	TGT-TA*x*
111	VDD3.3	112	GND
113	PD4 / IRQ*x*	114	PD13 / CS1*x*
115	PD14 / CS0*x*	116	PD15 / RW
117	GND	118	GND
119	GND	120	GND

6.1 Use of MCU adapter boards

If the EVB is to be used with an MCU adapter board, in order to provide support for packages other than 144QFP, there are a few points that you need to bear in mind when using the EVB in this configuration.

(1) The 144 QFP MCU on the EVB must not be fitted if an MCU adapter board is to be used. Otherwise, both MCU's will be addressing the same peripherals and external bus (if used). This will result in probable damage to the EVB and MCUs.

(2) The local clock circuitry on the EVB will not be used by the MCU adapter board (Pierce crystal oscillator circuit and PLL loop filter) as this will be implemented on the adapter board. Therefore, EVB jumpers J2, J3 and J4 will have no function.

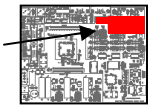
(3) Jumper J44 on the EVB is unused as Clkout impedance matching must be carried out as close to the MCU pin as possible.

All other jumpers and EVB configuration / features remain unchanged.

Note – The exact functionality of the EVB when used with an MCU adapter board will also depend on the functionality available on the MCU fitted to the adapter board. Many of these devices will not have an external bus for example.

7. Prototype Area

The prototype area is located in the top right section of the EVB.



A small prototyping area is included on the EVB, consisting of a 0.1” grid array. Power from all three regulators and ground pins are available at the bottom of the prototype area and are clearly marked.

Note the power supply lines to the prototype area are connected directly to the regulator outputs and not connected to the jumpered MCU supply.

Appendix A - Bill Of Materials

Item	Qty	Ref Des	Value	Function	Part Number
0	1	N/A	PCB RE11505F Rev O	Bare Printed Circuit Board, Revision O	RE11505F Rev O
1	1	C33	1000uF	Aluminium electrolytic Capacitor, 50V	Panasonic ECA-1VM102
2	5	C8 C11 C34 C35 C36	1.0uF	SMD Capacitor, 10V 1206 X7R	AVX CM316X7R105K16AT
3	3	C44 C58 C60	0.22uF X7R	SMD Capacitor, 16V 0805 X7R	C0805X7R160-224KNE
4	1	C19	68uF TANT	SMD Capacitor, 25V	AVX TAJE686K025R
5	1	C32	0.01uF	SMD Capacitor, 25V 0805	BC 0805B103K500BT
6	40	C1 C4 C5 C7 C9 C10 C15 C17 C22 C25 C27 C28 C29 C30 C31 C37 C38 C78 C79 C89 C40 C42 C45 C50 C67 C68 C71C55 C56 C62 C65 C66 C69 C70 C82 C84 C86 C88 C91 C92	0.1uF / 0.1uF X7R	SMD Capacitor, 25V 0805 X7R	AVX 08055C104KAT2A
7	1	C73 C74	10pf	SMD Capacitor, 25V COG 0805	C0805COG500-100JNE
8	6	C39 C41 C46 C47 C61 C49	470pF	SMD Capacitor, 50V 0805 COG	C0805COG500-471KNE
9	1	C48	4.7nF	SMD Capacitor, 50V 0805 COG	C0805X7R160-472KNE
10	24	C2 C3 C6 C18 C26 C43 C57 C72 C75 C76 C77 C23 C51 C52 C53 C54 C63 C64 C80 C81 C83 C85 C87 C90	1nF	SMD Capacitor, 50V COG 0805	AVX 08051C102KAT2A
11	1	C59	1nF X7R	SMD Capacitor, 50V X7R 0805	
12	3	C20 C21 C24	330uF AVX SMD	SMD Capacitor, AVX Tant, Low ESR	AVX TPSE337K010R0100
13	4	C12 C13 C14 C16	47pF - NO_FIT		DO NOT INSTALL
14	4	D1 D2 D3 D4	MBRS340T3	SMD Diode, Schottky Power	On Semi MBRS340T3
15	1	DS1	SMD YELLOW LED	SMD LED	Kingbright AA3528SYC
16	1	DS13	SMD RED LED	SMD LED	Kingbright AA3528EC
17	8	DS2 DS3 DS4 DS5 DS6 DS7 DS8 DS9	SMD YELLOW LED	SMD LED	Infineon HSMY-C650
18	3	DS10 DS11 DS12	SMD GREEN LED	SMD LED	Kingbright AA3528SGC
19	1	F1	Fuse, 1a, 250v,	Fuse, 5 x 20 mm, glass	Little Fuse 0216005.H
20	1	F1	Bussmann HTC-15M	Through Hole Fusemount (5mm Fuse)	Keystone 4527
21	1	FB1	FERRITE BEAD	SMD Ferrite Bead	Murata BLM31AJ601SN1L
22	19	J1 J3 J5 J10 J15 J17 J19 J26 J28 J30 J31 J33 J34 J35 J36 J37 J38 J39 J40	JUMPER 2 (Default FITTED)	Through Hole, 0.1 inch header (1x2)	Sullins PZC02SAAN
23	7	J14 J20 J22 J23 J27 J44 J45	JUMPER 2 (Default REMOVED)	Through Hole, 0.1 inch header (1x2)	Sullins PZC02SAAN
24	13	J7 J8 J11 J12 J13 J18 J21 J25 J29 J32 J41 J42 J43	JUMPER 3	Through Hole, 0.1 inch header (1x3)	Sullins PZC03SAAN
25	4	J2 J4 J6 J9	JUMPER 2x2	Through Hole, 0.1 inch header (2x2)	Sullins PZC02DAAN

26	1	J24	JUMPER 3x3	Through Hole, 0.1 inch header (3x3)	Sullins PZC0 Series
27	1	J16	JUMPER 8x2	Through Hole, 0.1 inch header (8x2)	Sullins PZC08DAAN
28	4	L1 L2 L3 L4	25uH	Through hole Inductor, 500V ferrite core	Seimens EPCOS B82111-B-C024
29	1	P11	HEADER 10x2	Through Hole, 0.1 inch header (10x2)	Sullins PZC10DAAN
30	1	P14	HEADER 11x2	Through Hole, 0.1 inch header (11x2)	Sullins PZC11DAAN
31	1	P15	Walled HEADER 10x2	Through Hole walled, 0.1 inch header (10x2)	3M 2520-6002UB
32	1	P17	CONNECTOR BNC-RA	Through Hole Pwr Connector, BNC 50 OHM	AMP 415046-1
33	1	P20	AMP PC PWR Connector	Through Hole Pwr Connector, PC Style	AMP 350211-1
34	1	P21	PWR 2SV-02	Through Hole Pwr Connector, 2-way Lever	Buchanan 2SV-02
35	1	P22	RJ45_LED	Through Hole, RJ45 Ethernet Connector	Amphenol RJHS-5381
36	1	P23	PWR Switchcraft RAPC722	Through Hole Pwr Connector, 2.1mm Jack	Switchcraft RAPC722
37	2	P3 P4	CONNECTOR DB9	Through Hole Connector, DB9 RS232 female	AMP 788796-1
38	2	P5 P19	AMP 120-way SMT Connector	SMD Connector, 120-way 0.8mm pitch plug	AMP 179031-5
39	2	P6 P16	HEADER 19x2 MICTOR	SMT Connector, MICTOR Style (M38C)	AMP 767054-1
40	1	P7	Walled HEADER 7x2	Through Hole walled, 0.1 inch header (7x2)	3M 2514-6002UB
41	5	P8 P9 P10 P12 P13	HEADER 9x2	Through Hole, 0.1 inch header (9x2)	Sullins PZC09DAAN
42	2	P1 P2	HEADER 3x1	Through Hole, 0.1 inch header (3x1)	Sullins PZC03SAAN
43	1	P18	HEADER 8x1	Through Hole, 0.1 inch header (8x1)	Sullins PZC08SAAN
44	1	R22	1K2	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
45	1	R25	150R	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
46	1	R26	270R	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
47	1	R28	5K	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
48	3	R3 R27 R35	560R	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
49	4	R4 R6 R8 R12	33R	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
50	14	R5 R7 R10 R11 R14 R15 R18 R34 R9 R13 R17 R23 R30 R33	10K	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
51	3	R1 R2 R29 R31	0R	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
52	2	R16 R20	100R	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
53	3	R21 R19 R24	1K	SMD Resistor, 0805 5%	Panasonic, Philips or AVX
54	1	R32	NO Fit	SMD Resistor, 0805 5%	
55	8	RN1 RN2 RN3 RN6 RN7 RN8 RN10 RN12	10K Net	SMD Resistor Network (x4), 1206 5%	Panasonic, Philips or AVX
56	1	RN11	75R Net	SMD Resistor Network (x4), 1206 5%	Panasonic, Philips or AVX
57	2	RN4 RN5	560R Net	SMD Resistor Network (x4), 1206 5%	Panasonic, Philips or AVX
58	1	RN9	4K7 Net	SMD Resistor Network (x4), 1206 5%	Panasonic, Philips or AVX
59	1	RP1	330R 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX

60	1	RP10	11K 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX
61	2	RP16 RP17	49.9R 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX
62	3	RP2 RP3 RP15	1K2 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX
63	1	RP4	180R 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX
64	1	RP5	15R 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX
65	3	RP6 RP13 RP14	470R 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX
66	1	RP7	270R 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX
67	4	RP8 RP9 RP11 RP12	24.9R 1%	SMD Precision Resistor, 0805 1%	Panasonic, Philips or AVX
68	1	RV1	2K Var	Through Hole trimmer, XICON 9mm snap-in	Alpha/Xicon 317-2090-2K
69	1	RV2	1K Var Trimmer SMD	SMD Trimmer, 3mm cermet type	CTS 303UC102E
70	1	SW1	SWITCH SPST, 8 Posn	SMD Switch, SPST Series 219 DIP	CTS Corp 219-8LPST
71	1	SW2	SWITCH C&K PUSH RED	SMD Switch, Momentary push button RED	C&K KS11R23CQD
72	1	SW3	SWITCH C&K PUSH BLK	SMD Switch, Momentary push button BLACK	C&K KS11R22CQD
73	1	SW4	SWITCH SPDT SLIDE	Through Hole Switch, SPDT Slide	CW Industries G107-0513
74	1	T1	HALO TG110-S050N5	SMD Filter, Ethernet isolation transformer	Halo TG110-S050N2
75	11	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11	HEADER 1-TP	SMD Test point	Keystone 5015
76	2	U1 U2	PCA82C250T	SMD IC, Can Transceiver, S08 Package	Philips PCA82C250TD
77	2	U12 U13	MC74LCX16244	SMD IC, 16 bit buffer driver	On Semi MC74LCX16244DT
78	2	U18 U20	LM2596S-ADJ	SMD Switching Voltage Regulator (Variable Output)	National Semi LM2596S-ADJ
79	1	U19	LM2596S-3.3	SMD Switching Voltage Regulator (3.3V Output)	National Semi LM2596S-3.3
80	1	U4	MAX232CSE	SMD IC, Maxim RS232 Level Shifter	Maxim MAX232CSE
81	1	U10	MC74LCX16245	SMD IC, 16 bit bi-directional buffer	On Semi MC74LCX16245DT
82	1	U11	NC7SZ57	SMD IC, TinyLogic Configurable 2-Input Logic Gate	Fairchild NC7SZ57P6X
83	1	U14	AM29F160D FLASH	SMD FLASH, 2MByte Standard pinout, 5V	AMD Am29F160D B75EC
84	1	U15	(64Kx16) SRAM	SMD SRAM, 128KByte 5V	Cypress CY7C1021B-12ZC
85	1	U16	ispGAL22V10AV-5LJC	PLCC IC, PAL22V10 3.3V GAL, ISP	Lattice ispGAL22V10AV-5LJC
86	1	XU16-1	940-99-028-17-400000	SMD Socket, 28-ld PLCC	Mil-Max 940-99-028-17-400000
87	1	U17	SMSC LAN91C111-NE	SMD IC, Ethernet transceiver, 10/100	SMSC LAN91C111-NE
88	1	U9	MAC7111 144QFP	Freescale MAC7111 QFP MCU	
89	1	U3	MAX6343-S	SMD IC,Low Voltage Monitor (Active Sw Debounce)	Maxim MAX6343SUT-T
90	1	U5	MAX6703-Z	SMD IC,Low Voltage Monitor Device	Maxim MAX6703ZKA-T
91	1	U6	MC74AC08-D	SMD IC, Quad 2-Input AND gates	Micrel MC74AC08-D

92	1	U7, U8	MC74AC125-D	SMD IC, Quad Buffer with 3-State Outputs	Micrel MC74AC125-D
93	1	Y1	8MHz XTAL, HC-49S	Through Hole Crystal Oscillator, HC-49 Low Profile	Fox FOXS080-20
94	1	Y2	8MHZ OSC Module	Through Hole Oscillator Module, DIP14	Epson SG-8002DC-PCB-ND
95	1	Y3	25MHz OSC Module	Through Hole Oscillator Module, DIP14	Pletronics P1145-HCV-25MHZ
Misc Items					
96	8		SJ-5518	Black self adhesive rubber feet	3M SJ5518-9-ND
97	50	All default jumper headers fitted	STC02SYAN	Jumper Shunts, 2 pin	Sullins STC02SYAN

Appendix B - EVB Schematics

MAC7100 Evaluation Board

Table Of Contents:

Revision Information

Rev	Date	Designer	Comments
0.1	28 March 03	A. Robertson	Provisional release
0.2	04 April 03	A. Robertson	Incorporates review changes - Release to PCB layout
0.3	22 April 03	A. Robertson	Mod's to incorporate changes to MCU reset config
0.4	30 April 03	A. Robertson	Remove PD2 Jumper and pull VSSTest to ground
1.0	25 July 03	A. Robertson	Changes for PCB RevB
1.1	12 Sept 03	A. Robertson	Changes to Productionise EVB (PCB RevO)
1.2	12 Nov 04	A. Robertson	Name Change to Freescale Semiconductor

Notes:

- Resistor networks are donated RNx. All resistor networks are SMD 1206 style package.
- High precision resistors (1%) are denoted RPx and are SMD 0805
- Variable resistors are denoted RVx
- All other resistors are SMD 0805 style unless otherwise stated
- All decoupling caps less than 0.1uF are COG SMD 0805 unless otherwise stated
- All decoupling caps greater than 0.1uF are X7R SMD 0805 unless otherwise stated
- All connectors are denoted Px
- All jumpers are denoted Jx
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2
- All Switches are denoted SWx
- All test points are denoted TPx
- All unpopulated test points (vias) are denoted as TPVx

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

Note:

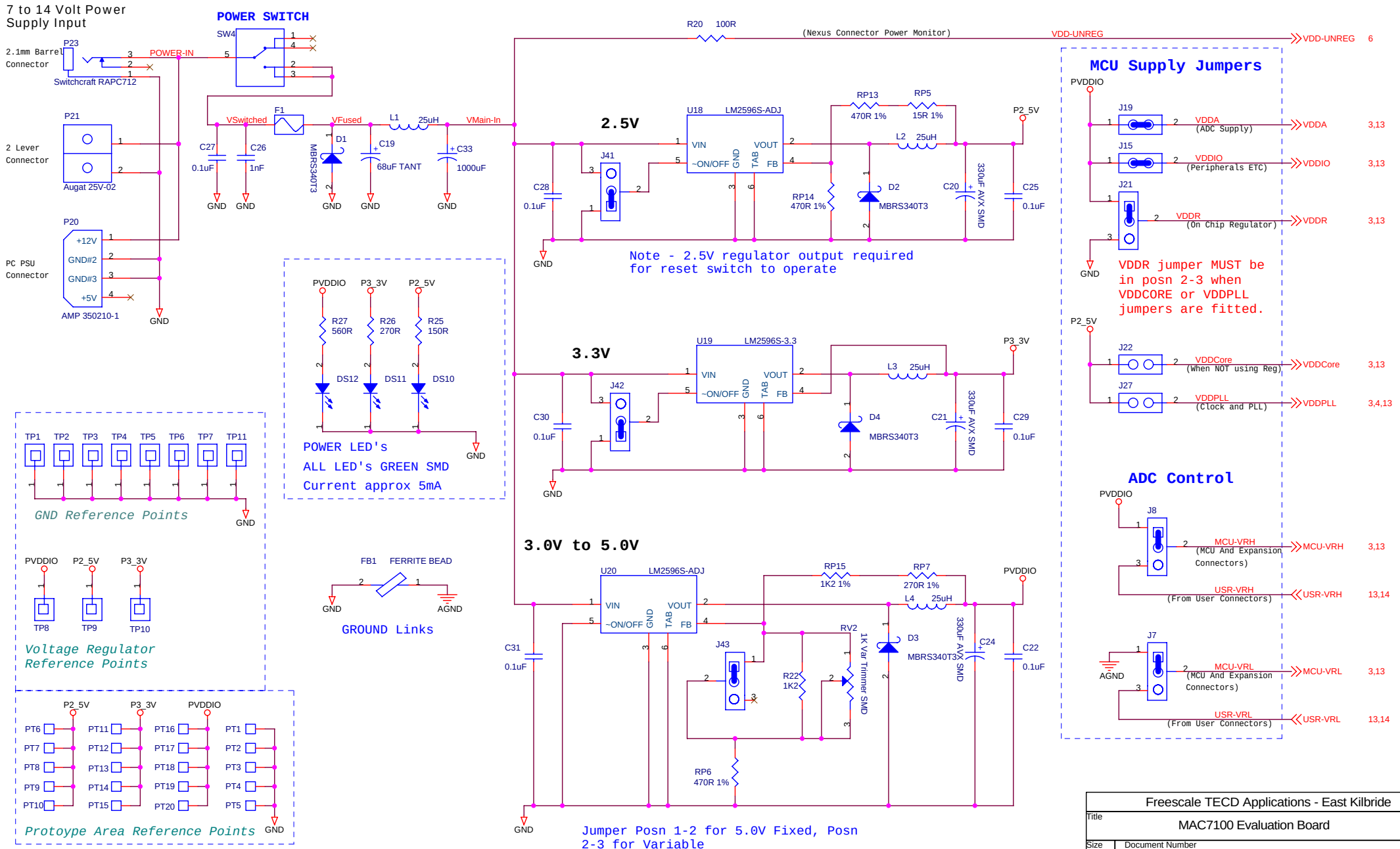
Freescale TECD Applications - East Kilbride

Title: MAC7100 Evaluation Board

Size: B | Document Number: Drawing 63A11505S (MAC7100 EVB) | Rev: 1.2

Date: Friday, November 12, 2004 | Sheet 1 of 15

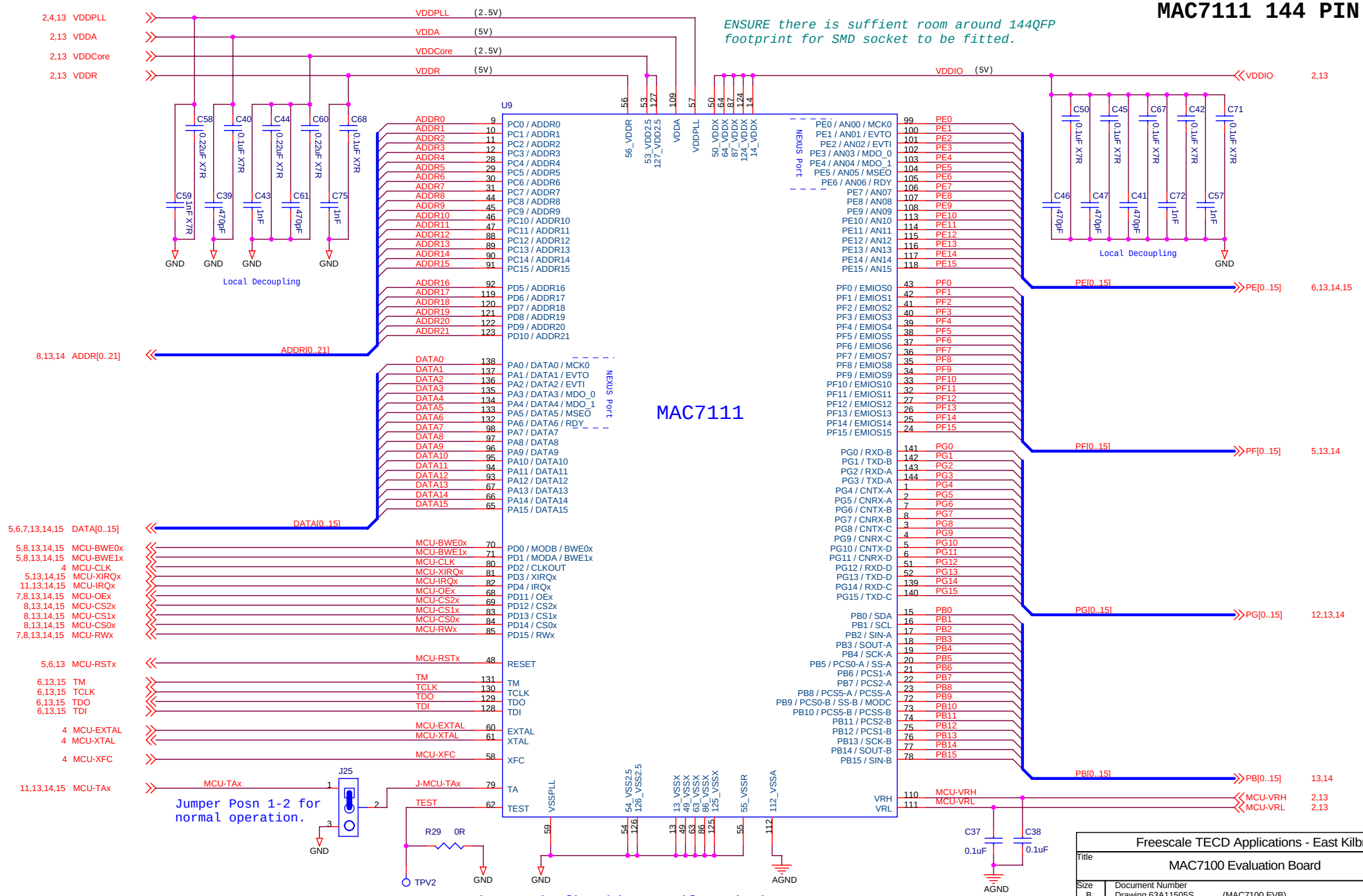
POWER SUPPLY



Freescale TECD Applications - East Kilbride		
Title: MAC7100 Evaluation Board		
Size: B	Document Number: Drawing 63A11505S (MAC7100 EVB)	Rev: 1.2
Date: Friday, November 12, 2004	Sheet 2 of 15	

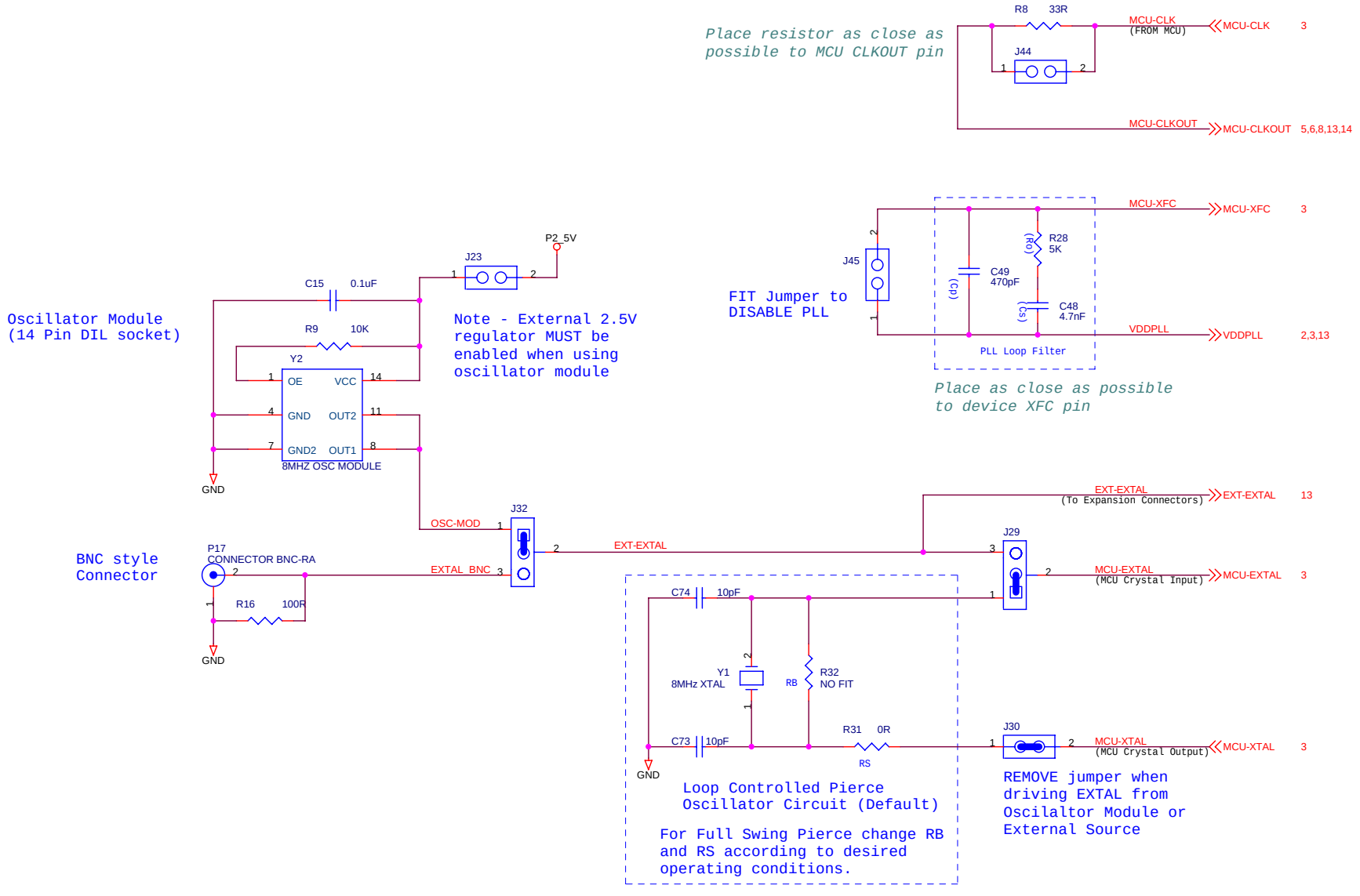
MAC7111 144 PIN MCU

ENSURE there is suffient room around 144QFP footprint for SMD socket to be fitted.



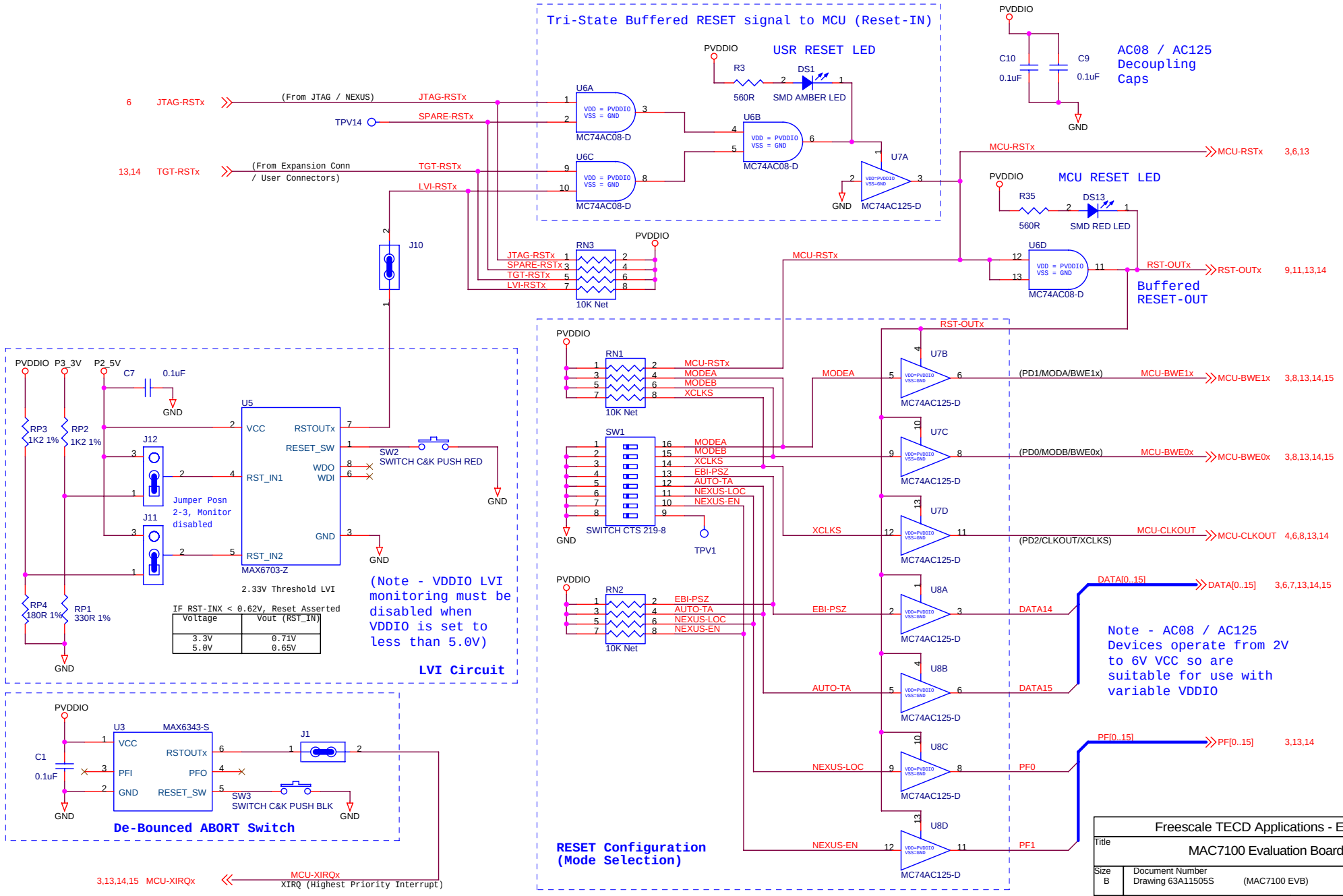
Freescale TECD Applications - East Kilbride			
Title: MAC7100 Evaluation Board			
Size: B	Document Number: Drawing 63A11505S (MAC7100 EVB)		Rev: 1.2
Date: Friday, November 12, 2004	Sheet 3 of 15		

CLOCK AND PLL CIRCUITRY



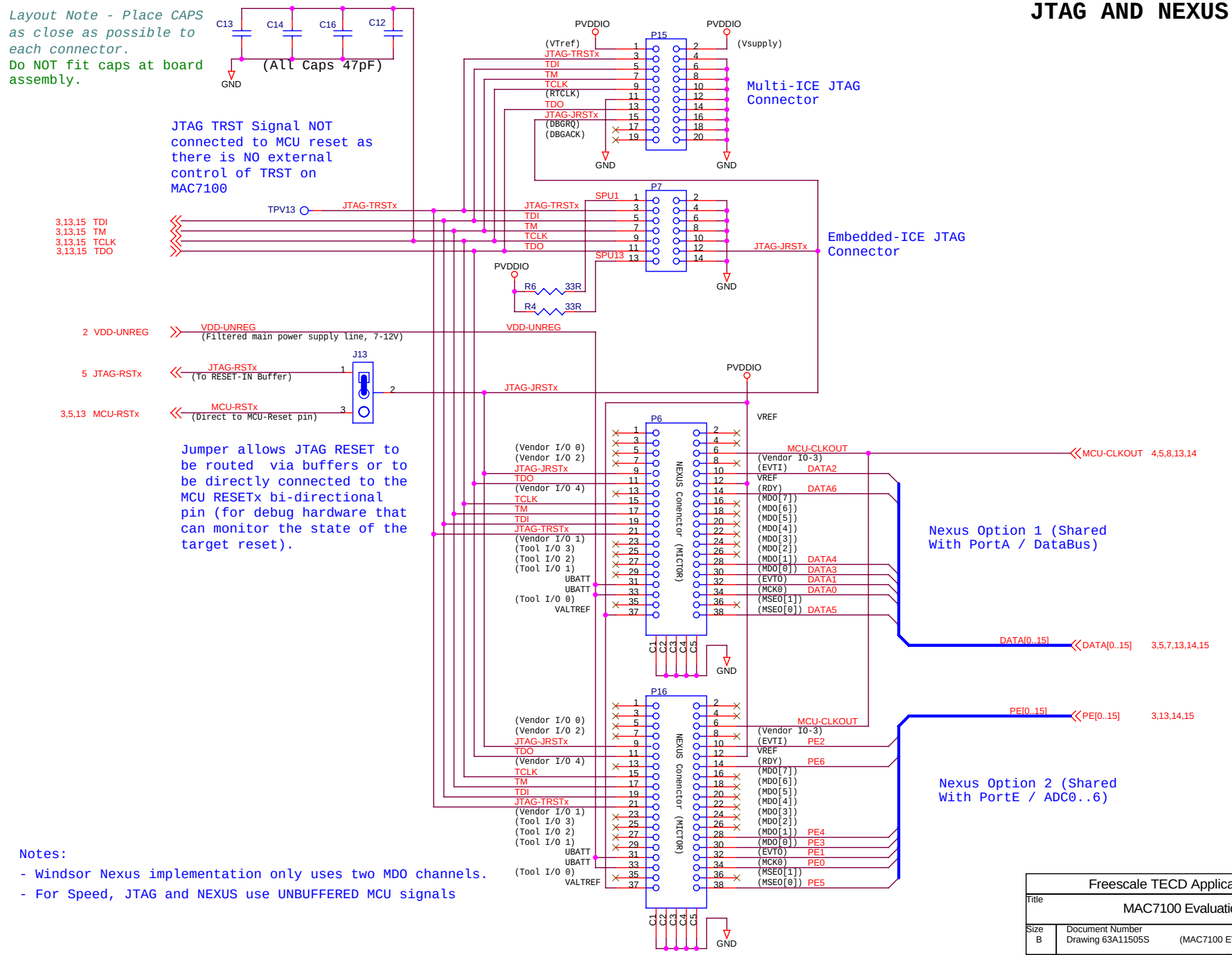
Freescale TECD Applications - East Kilbride		
Title: MAC7100 Evaluation Board		
Size: B	Document Number: Drawing 63A11505S (MAC7100 EVB)	Rev: 1.2
Date: Friday, November 12, 2004	Sheet 4 of 15	

RESET GENERATION, CONTROL AND MODE SELECTION



Freescale TECD Applications - East Kilbride	
Title	MAC7100 Evaluation Board
Size B	Document Number Drawing 63A11505S (MAC7100 EVB) Rev 1.2
Date: Friday, November 12, 2004	Sheet 5 of 15

JTAG AND NEXUS CONNECTORS

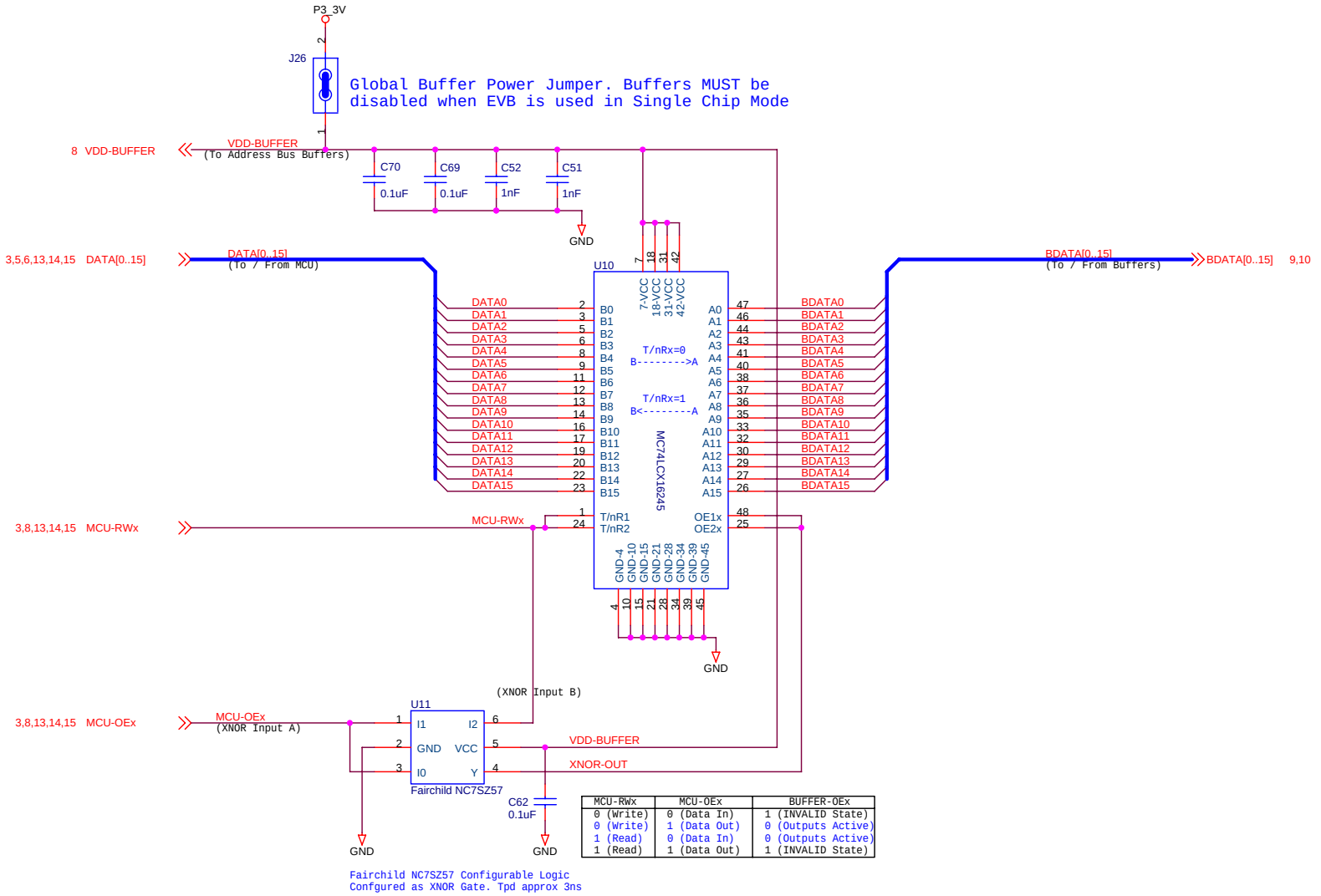


Notes:

- Windsor Nexus implementation only uses two MDO channels.
- For Speed, JTAG and NEXUS use UNBUFFERED MCU signals

Freescale TECD Applications - East Kilbride		
Title: MAC7100 Evaluation Board		
Size: B	Document Number: Drawing 63A11505S (MAC7100 EVB)	Rev: 1.2
Date: Friday, November 12, 2004	Sheet 6 of 15	

EBI BUFFERS 1 - DATABUS

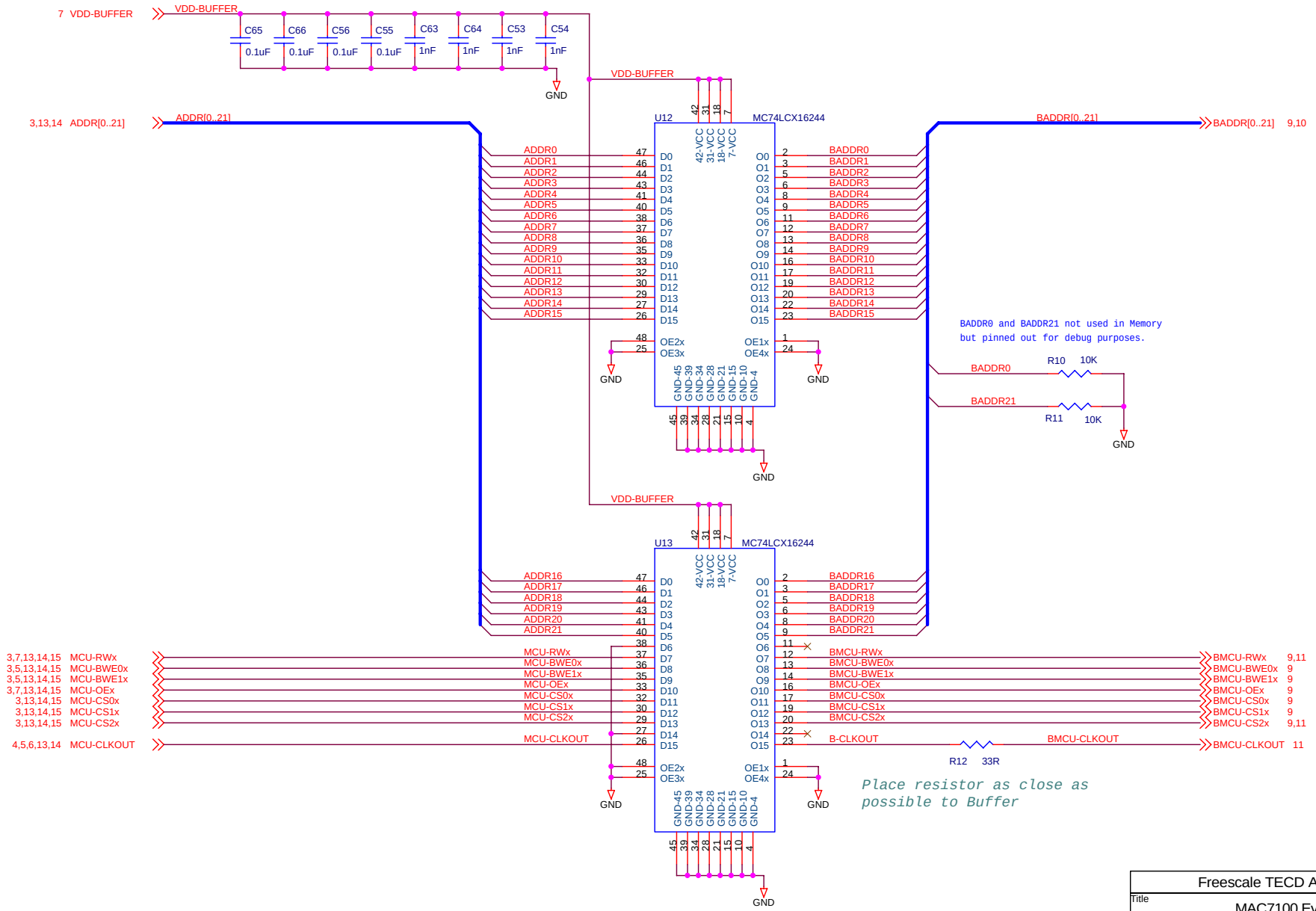


MCU-RWx	MCU-OEx	BUFFER-OEx
0 (Write)	0 (Data In)	1 (INVALID State)
0 (Write)	1 (Data Out)	0 (Outputs Active)
1 (Read)	0 (Data In)	0 (Outputs Active)
1 (Read)	1 (Data Out)	1 (INVALID State)

Note - Signal Naming Convention. All Buffered signals start with B (eg BDATA for Buffered Data)

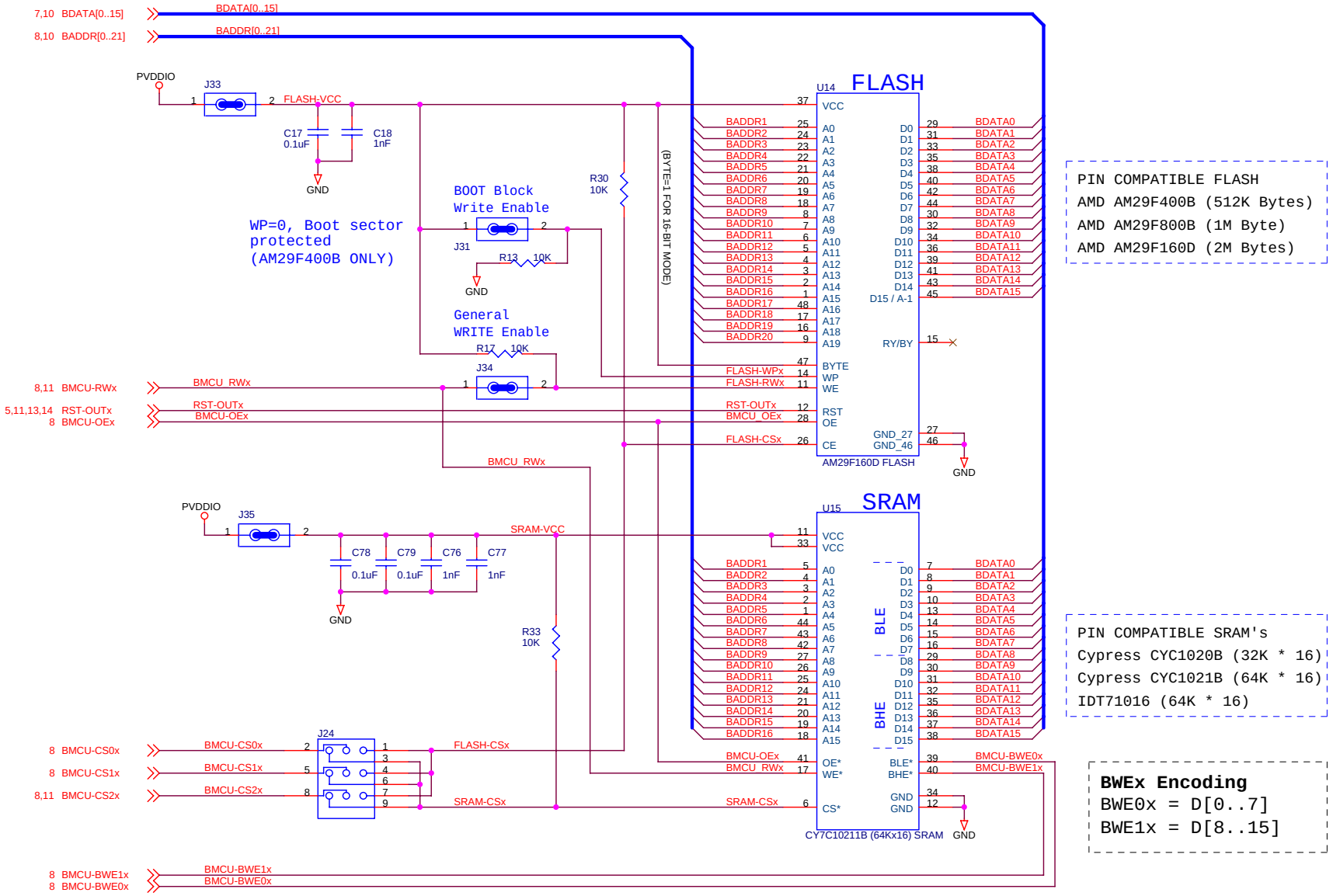
Freescale TECD Applications - East Kilbride		
Title: MAC7100 Evaluation Board		
Size: B	Document Number: Drawing 63A11505S (MAC7100 EVB)	Rev: 1.2
Date: Friday, November 12, 2004	Sheet 7 of 15	

EBI BUFFERS 2 - ADDRESS AND CONTROL



Freescale TECD Applications - East Kilbride		
Title: MAC7100 Evaluation Board		
Size: B	Document Number: Drawing 63A11505S (MAC7100 EVB)	Rev: 1.2
Date: Friday, November 12, 2004	Sheet 8 of 15	

EXTERNAL MEMORY



PIN COMPATIBLE FLASH
AMD AM29F400B (512K Bytes)
AMD AM29F800B (1M Byte)
AMD AM29F160D (2M Bytes)

PIN COMPATIBLE SRAM's
Cypress CYC1020B (32K * 16)
Cypress CYC1021B (64K * 16)
IDT71016 (64K * 16)

BWEx Encoding
BWE0x = D[0..7]
BWE1x = D[8..15]

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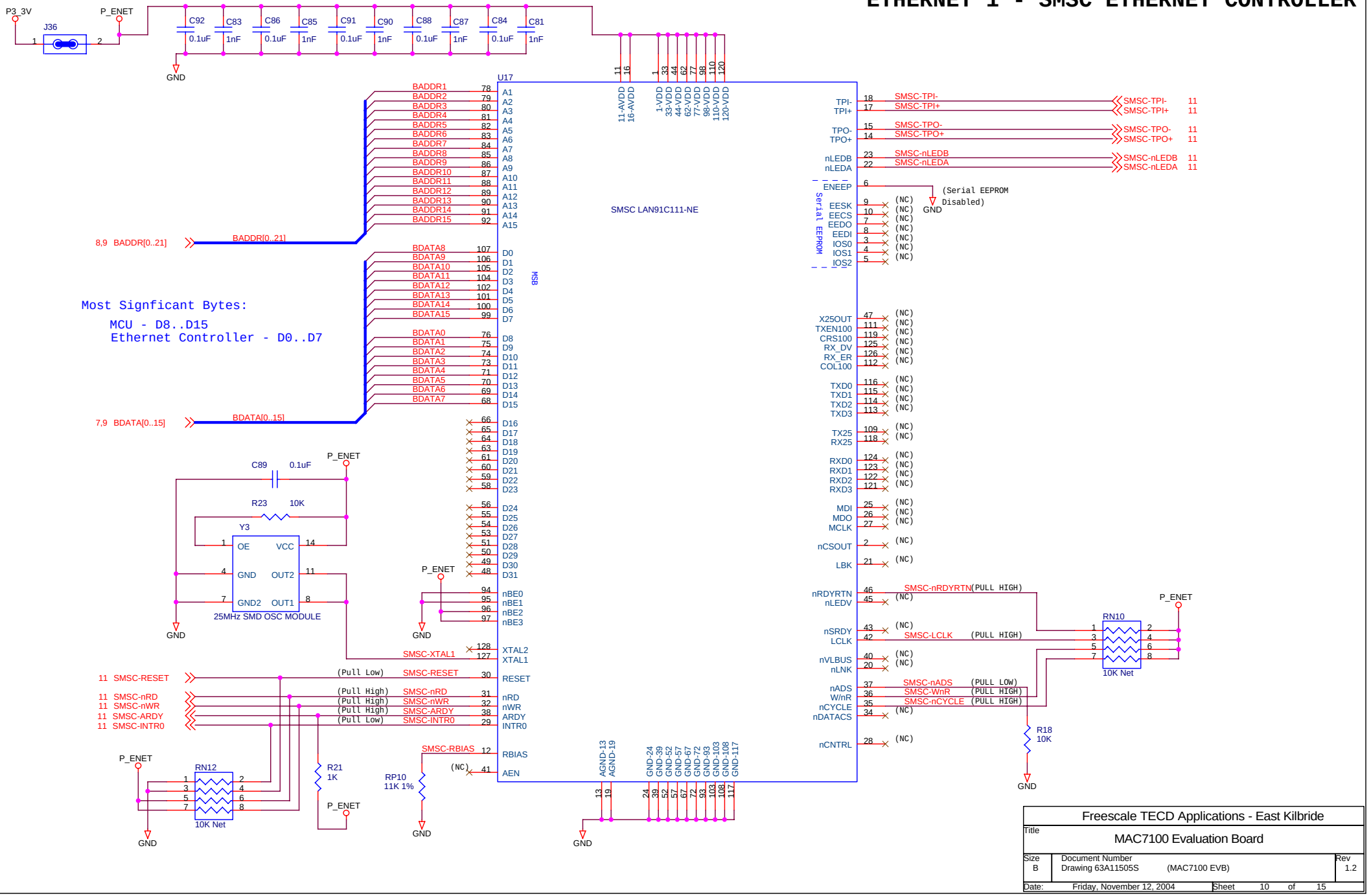
ETHERNET 1 - SMSC ETHERNET CONTROLLER



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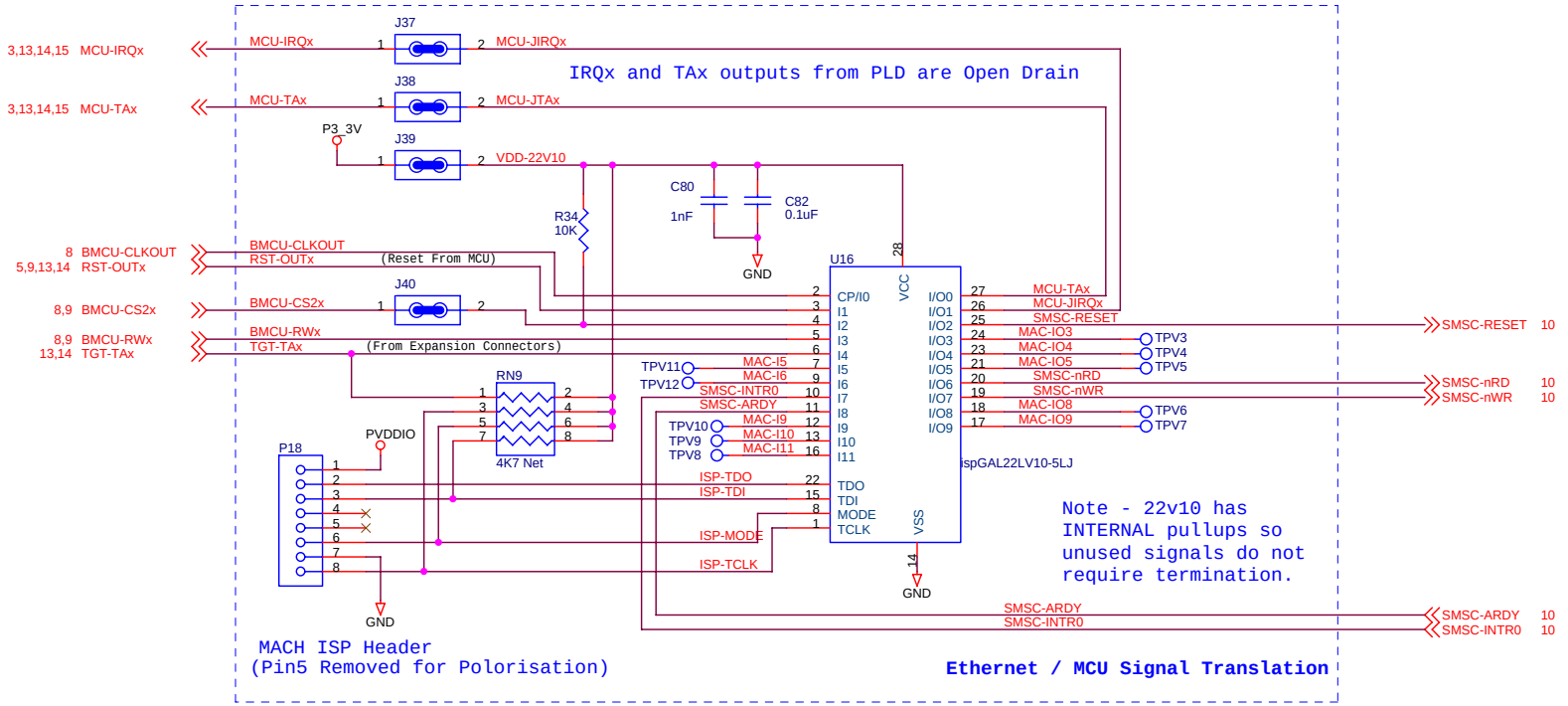
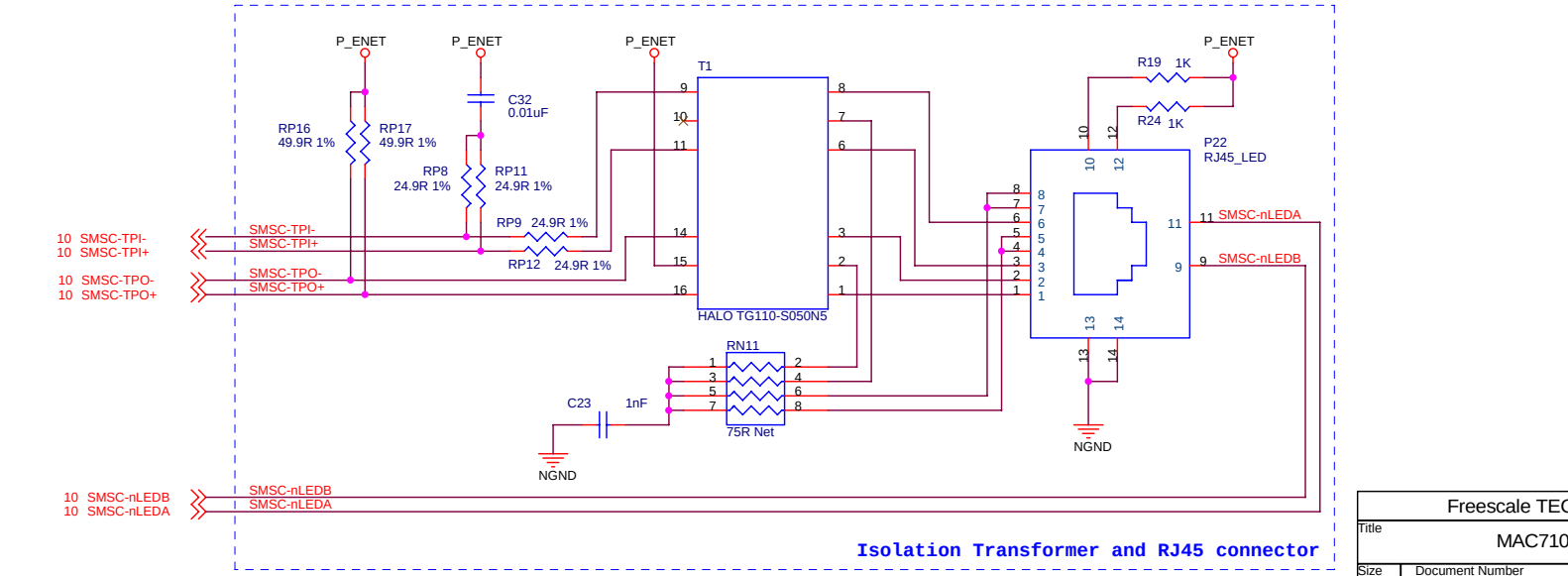
ETHERNET 2 - MCU / ETHERNET INTERFACE AND RJ45





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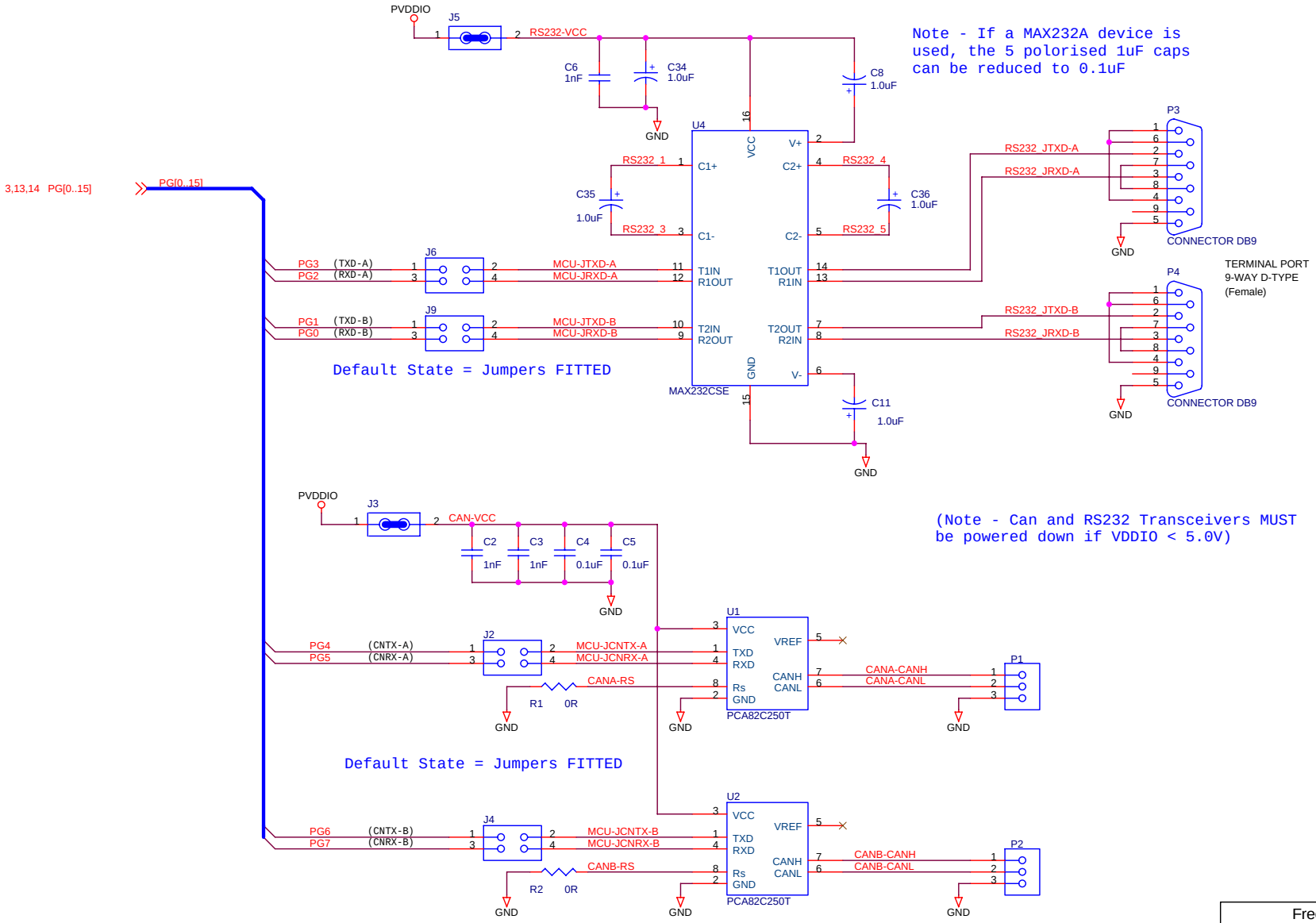
CAN AND SCI PHYSICAL INTERFACE



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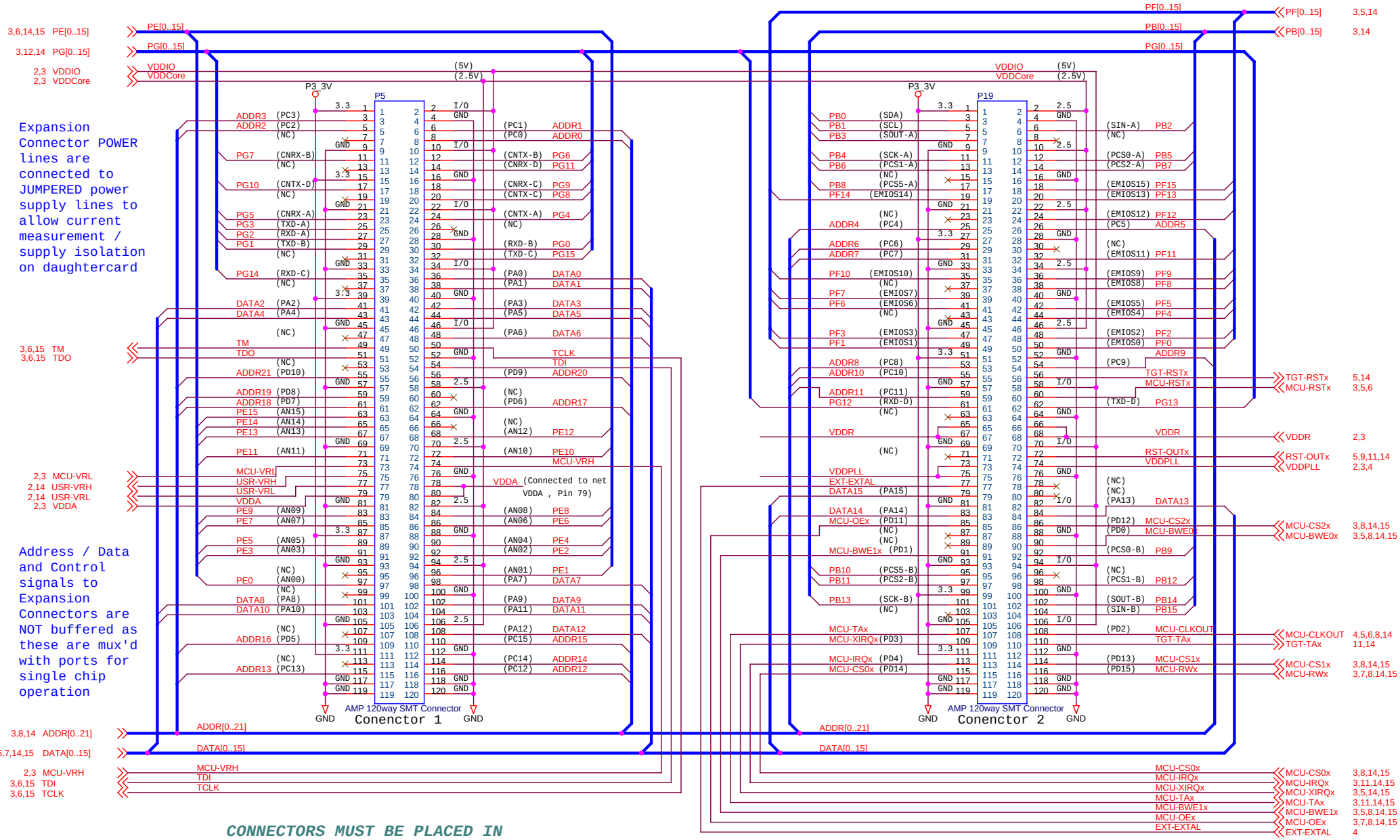
EXPANSION CONNECTORS (DAUGHTERCARD)



CONNECTORS MUST BE PLACED IN ACCORDANCE WITH PCB SPECIFICATION

AMP Connector Part number 179031-5 (8mm high, 0.8mm pitch 120way)

Suitable Mating connector - AMP 5-179009-5 (9mm high) or 5-179010-5 (13mm high)

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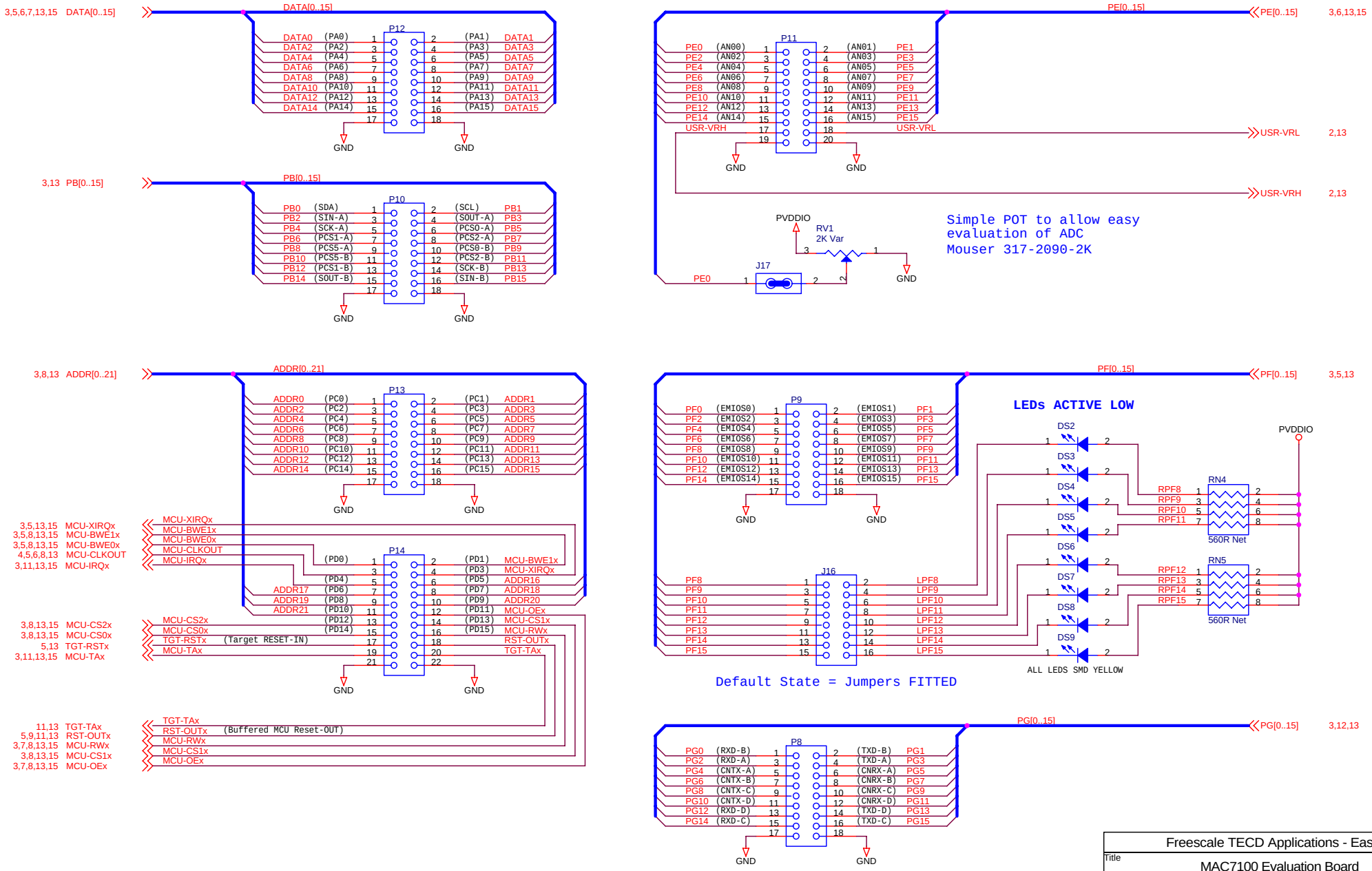
USER CONNECTORS



NOTE: All Connectors are 0.1" through-hole headers

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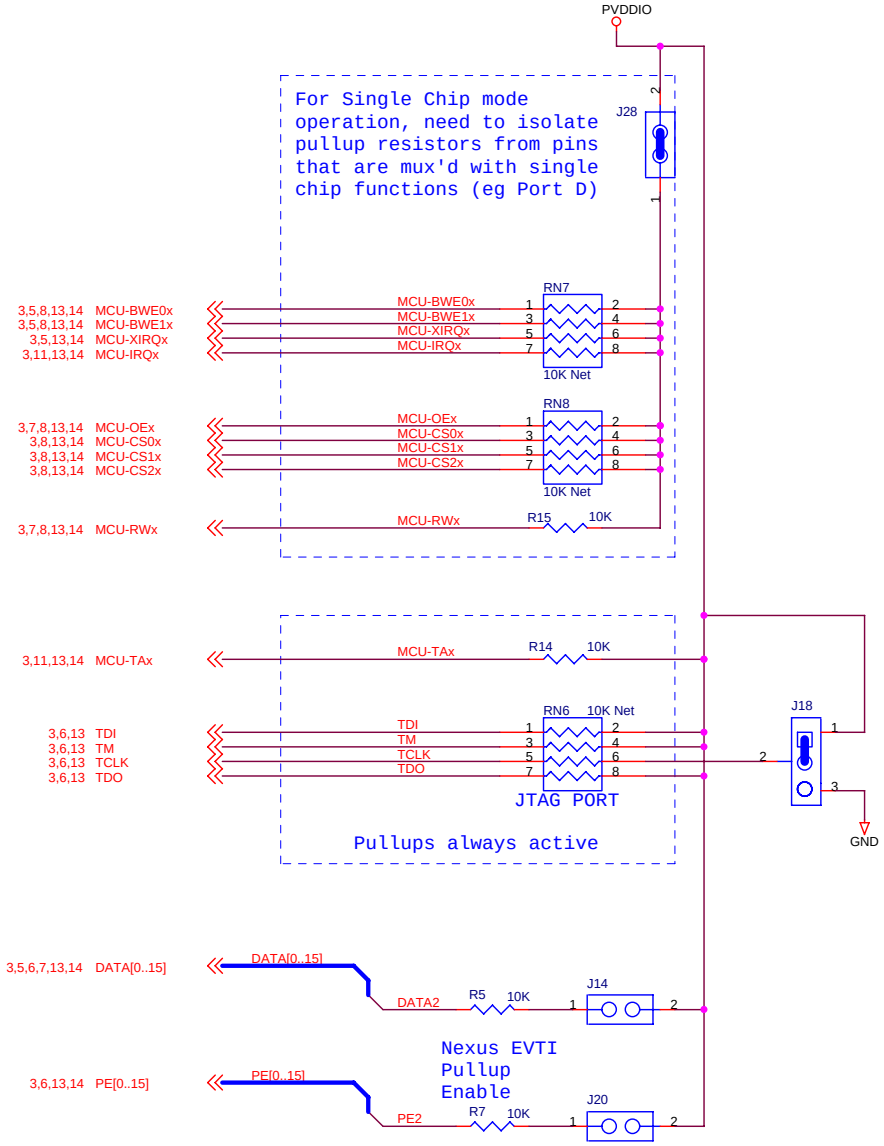
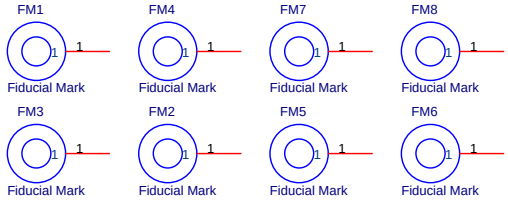
TERMINATION RESISTORS





All RESET Pullup Resistors are shown on Reset Circuitry page

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