

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source Up To 200 mA

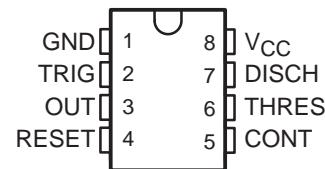
description/ordering information

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

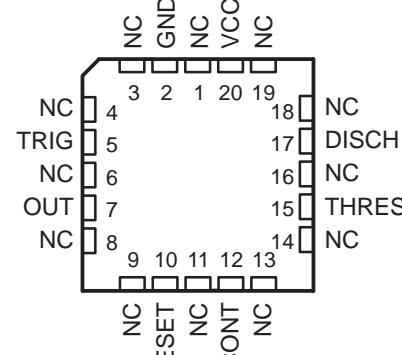
The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC} . These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

NE555 . . . D, P, PS, OR PW PACKAGE
SA555 . . . D OR P PACKAGE
SE555 . . . D, JG, OR P PACKAGE
(TOP VIEW)



SE555 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Datasheet.Directory



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

NE555, SA555, SE555 PRECISION TIMERS

SLFS022E – SEPTEMBER 1973 – REVISED MARCH 2004

description/ordering information (continued)

ORDERING INFORMATION

TA	V _{THRES MAX} V _{CC} = 15 V	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	11.2 V	PDIP (P)	Tube of 50	NE555P	NE555P
		SOIC (D)	Tube of 75	NE555D	NE555
			Reel of 2500	NE555DR	
		SOP (PS)	Reel of 2000	NE555PSR	N555
		TSSOP (PW)	Tube of 150	NE555PW	N555
			Reel of 2000	NE555PWR	
-40°C to 85°C	11.2 V	PDIP (P)	Tube of 50	SA555P	SA555P
		SOIC (D)	Tube of 75	SA555D	SA555
			Reel of 2000	SA555DR	
-55°C to 125°C	10.6 V	PDIP (P)	Tube of 50	SE555P	SE555P
		SOIC (D)	Tube of 75	SE555D	SE555D
			Reel of 2500	SE555DR	
		CDIP (JG)	Tube of 50	SE555JG	SE555JG
		LCCC (FK)	Tube of 55	SE555FK	SE555FK

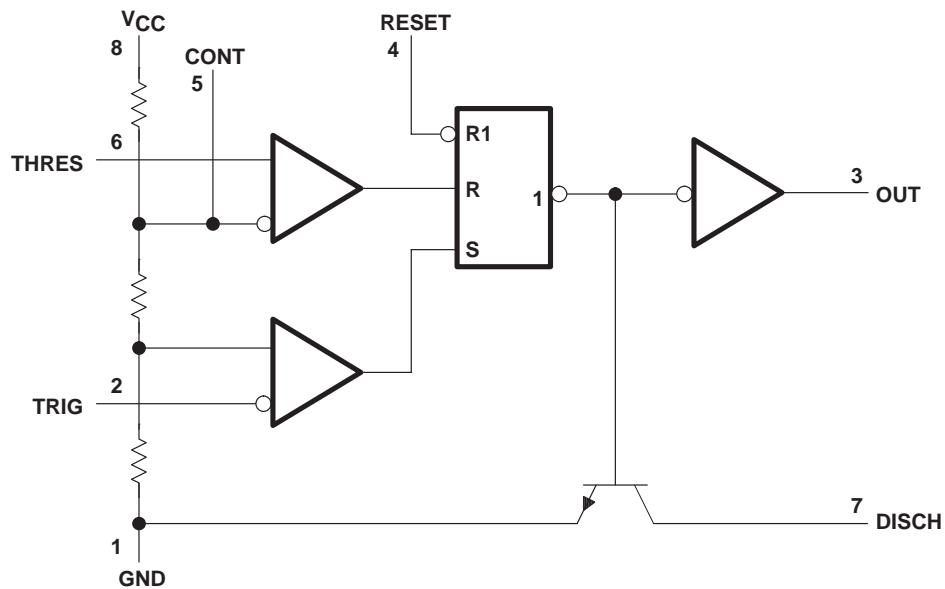
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

RESET	TRIGGER VOLTAGE [‡]	THRESHOLD VOLTAGE [‡]	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V _{DD}	Irrelevant	High	Off
High	>1/3 V _{DD}	>2/3 V _{DD}	Low	On
High	>1/3 V _{DD}	<2/3 V _{DD}	As previously established	

[‡] Voltage levels shown are nominal.

functional block diagram



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: RESET can override TRIG, which can override THRES.

NE555, SA555, SE555 PRECISION TIMERS

SLFS022E – SEPTEMBER 1973 – REVISED MARCH 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC} (see Note 1)	18 V
Input voltage (CONT, RESET, THRES, and TRIG)	V _{CC}
Output current	±225 mA
Package thermal impedance, θ _{JA} (see Notes 2 and 3): D package	97°C/W
P package	85°C/W
PS package	95°C/W
PW package	149°C/W
Package thermal impedance, θ _{JC} (see Notes 4 and 5): FK package	5.61°C/W
JG package	14.5°C/W
Operating virtual junction temperature, T _J	150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JEDEC 51-7.
4. Maximum power dissipation is a function of T_{J(max)}, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is P_D = (T_{J(max)} – T_C)/θ_{JC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage	SA555, NE555	4.5	16
		SE555	4.5	18
V _I	Input voltage (CONT, RESET, THRES, and TRIG)		V _{CC}	V
I _O	Output current		±200	mA
T _A	Operating free-air temperature	NE555	0	70
		SA555	–40	85
		SE555	–55	125

electrical characteristics, $V_{CC} = 5 \text{ V}$ to 15 V , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SE555			NE555 SA555			UNIT		
		MIN	TYP	MAX	MIN	TYP	MAX			
THRES voltage level	$V_{CC} = 15 \text{ V}$	9.4	10	10.6	8.8	10	11.2	V		
	$V_{CC} = 5 \text{ V}$	2.7	3.3	4	2.4	3.3	4.2			
THRES current (see Note 6)			30	250	30 250			nA		
TRIG voltage level	$V_{CC} = 15 \text{ V}$	4.8	5	5.2	4.5	5	5.6	V		
		$T_A = -55^\circ\text{C}$ to 125°C	3	6						
	$V_{CC} = 5 \text{ V}$	1.45	1.67	1.9	1.1	1.67	2.2			
		$T_A = -55^\circ\text{C}$ to 125°C	1.9							
TRIG current	TRIG at 0 V		0.5	0.9	0.5 2			μA		
RESET voltage level			0.3	0.7	1	0.3	0.7	V		
	$T_A = -55^\circ\text{C}$ to 125°C		1.1							
RESET current	RESET at V_{CC}		0.1	0.4	0.1 0.4			mA		
	RESET at 0 V		-0.4	-1	-0.4 -1.5					
DISCH switch off-state current			20	100	20 100			nA		
CONT voltage (open circuit)	$V_{CC} = 15 \text{ V}$	9.6	10	10.4	9	10	11	V		
		$T_A = -55^\circ\text{C}$ to 125°C	9.6	10.4						
	$V_{CC} = 5 \text{ V}$	2.9	3.3	3.8	2.6	3.3	4			
		$T_A = -55^\circ\text{C}$ to 125°C	2.9	3.8						
Low-level output voltage	$V_{CC} = 15 \text{ V}$, $I_{OL} = 10 \text{ mA}$	0.1	0.15	0.1 0.25			V			
		$T_A = -55^\circ\text{C}$ to 125°C	0.2							
	$V_{CC} = 15 \text{ V}$, $I_{OL} = 50 \text{ mA}$	0.4	0.5	0.4 0.75						
		$T_A = -55^\circ\text{C}$ to 125°C	1							
	$V_{CC} = 15 \text{ V}$, $I_{OL} = 100 \text{ mA}$	2	2.2	2 2.5						
		$T_A = -55^\circ\text{C}$ to 125°C	2.7							
	$V_{CC} = 15 \text{ V}$, $I_{OL} = 200 \text{ mA}$	2.5			2.5					
	$V_{CC} = 5 \text{ V}$, $I_{OL} = 3.5 \text{ mA}$	$T_A = -55^\circ\text{C}$ to 125°C	0.35							
High-level output voltage	$V_{CC} = 5 \text{ V}$, $I_{OH} = 5 \text{ mA}$	0.1	0.2	0.1 0.35			V			
		$T_A = -55^\circ\text{C}$ to 125°C	0.8							
	$V_{CC} = 5 \text{ V}$, $I_{OH} = 8 \text{ mA}$	0.15	0.25	0.15 0.4						
	$V_{CC} = 15 \text{ V}$, $I_{OH} = 100 \text{ mA}$	13	13.3	12.75 13.3						
Supply current	$V_{CC} = 15 \text{ V}$, $I_{OH} = 200 \text{ mA}$	12						mA		
		3	3.3	2.75 3.3						
	Output low, No load	2								
		$V_{CC} = 15 \text{ V}$	10	12	10	15				
	$V_{CC} = 5 \text{ V}$	3 5			3	6				
	Output high, No load	$V_{CC} = 15 \text{ V}$	9	10	9	13				
		$V_{CC} = 5 \text{ V}$	2	4	2	5				

NOTE 6: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when $V_{CC} = 5 \text{ V}$, the maximum value is $R = R_A + R_B \approx 3.4 \text{ M}\Omega$, and for $V_{CC} = 15 \text{ V}$, the maximum value is $10 \text{ M}\Omega$.

NE555, SA555, SE555 PRECISION TIMERS

SLFS022E – SEPTEMBER 1973 – REVISED MARCH 2004

operating characteristics, $V_{CC} = 5 \text{ V}$ and 15 V

PARAMETER		TEST CONDITIONS ^T	SE555			NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval [‡]	Each timer, monostable [§]	$T_A = 25^\circ\text{C}$	0.5	1.5*		1	3		%
	Each timer, astable [¶]		1.5			2.25			
Temperature coefficient of timing interval	Each timer, monostable [§]	$T_A = \text{MIN to MAX}$	30	100*		50			ppm/ $^\circ\text{C}$
	Each timer, astable [¶]		90			150			
Supply-voltage sensitivity of timing interval	Each timer, monostable [§]	$T_A = 25^\circ\text{C}$	0.05	0.2*		0.1	0.5		%/ V
	Each timer, astable [¶]		0.15			0.3			
Output-pulse rise time		$C_L = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$	100	200*		100	300		ns
Output-pulse fall time		$C_L = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$	100	200*		100	300		ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

§ Values specified are for a device in a monostable circuit similar to Figure 9, with the following component values: $R_A = 2 \text{ k}\Omega$ to $100 \text{ k}\Omega$, $C = 0.1 \mu\text{F}$.

¶ Values specified are for a device in an astable circuit similar to Figure 12, with the following component values: $R_A = 1 \text{ k}\Omega$ to $100 \text{ k}\Omega$, $C = 0.1 \mu\text{F}$.



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TYPICAL CHARACTERISTICS[†]

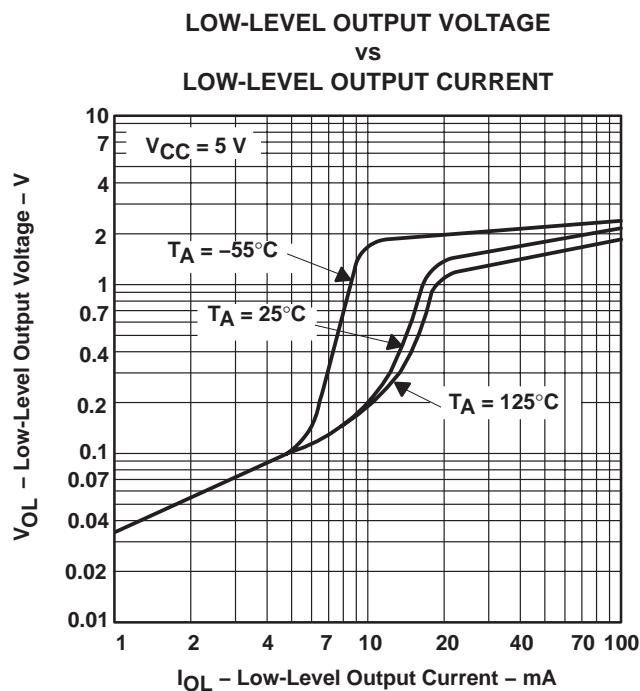


Figure 1

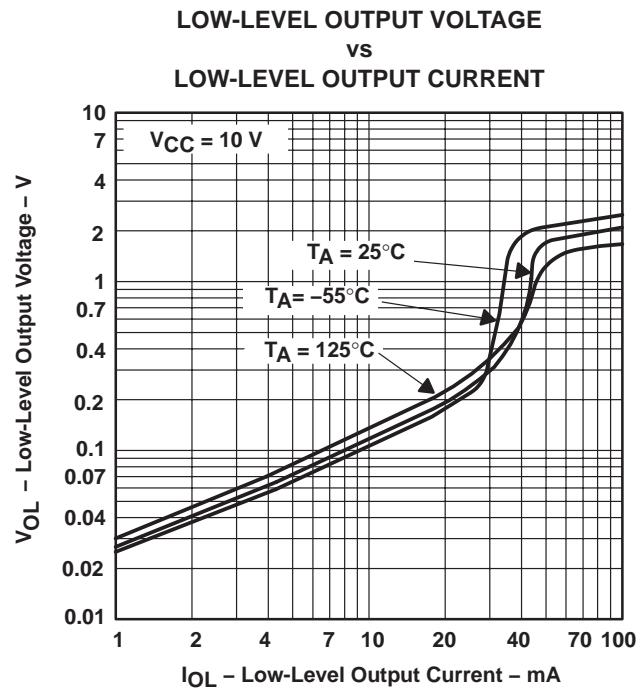


Figure 2

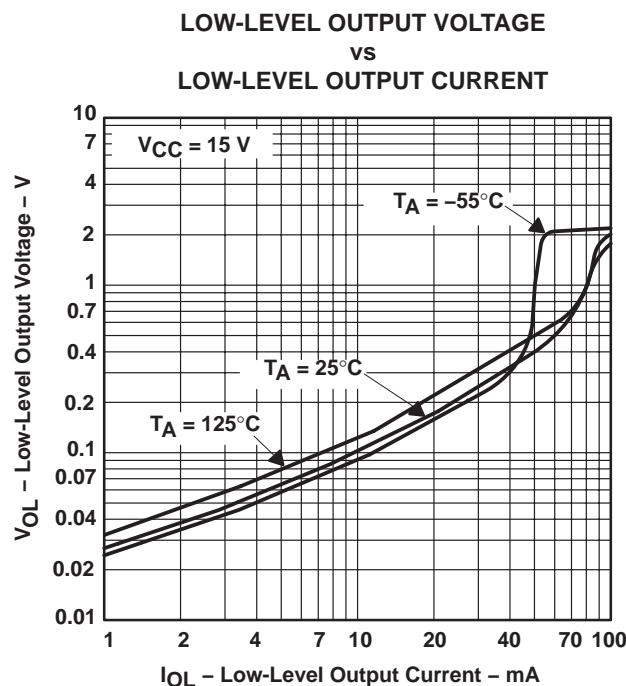


Figure 3

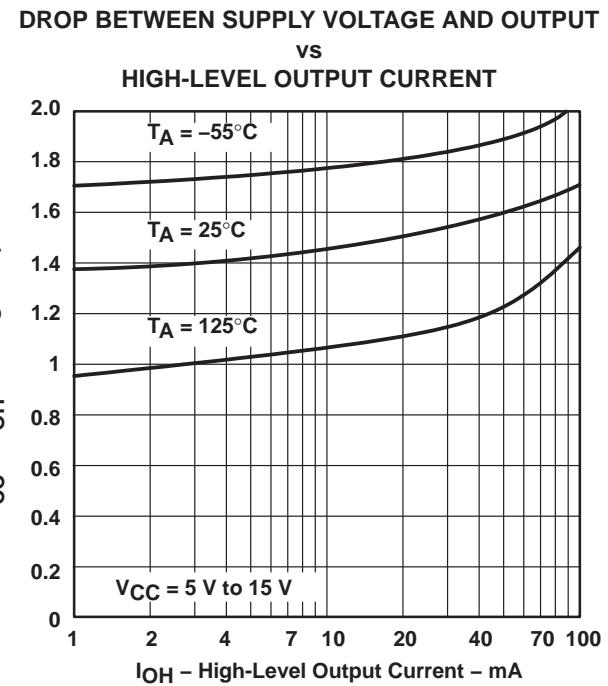


Figure 4

[†]Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

NE555, SA555, SE555 PRECISION TIMERS

SLFS022E – SEPTEMBER 1973 – REVISED MARCH 2004

TYPICAL CHARACTERISTICS[†]

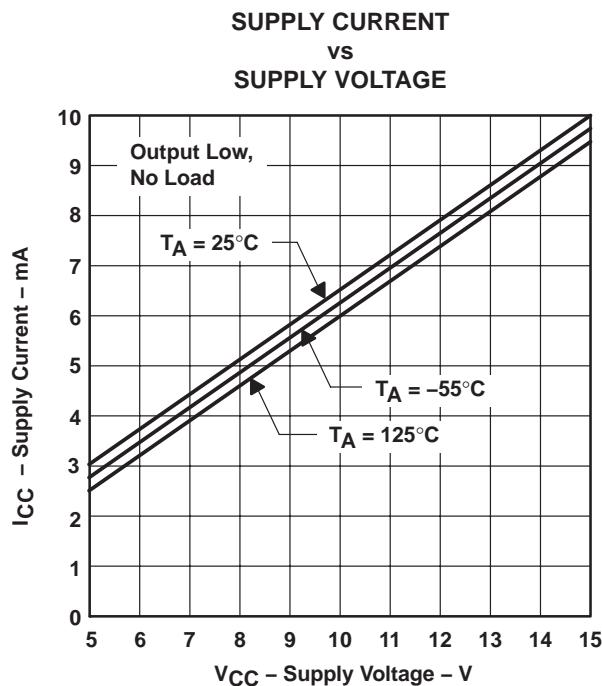


Figure 5

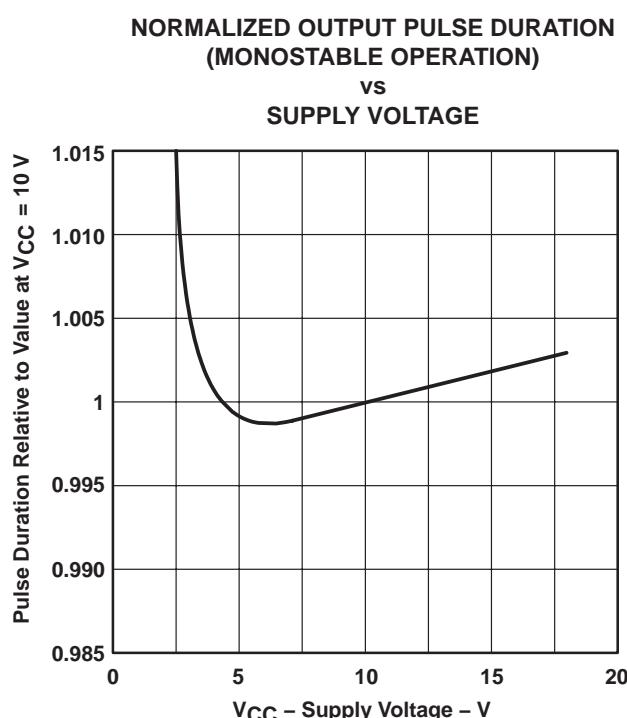


Figure 6

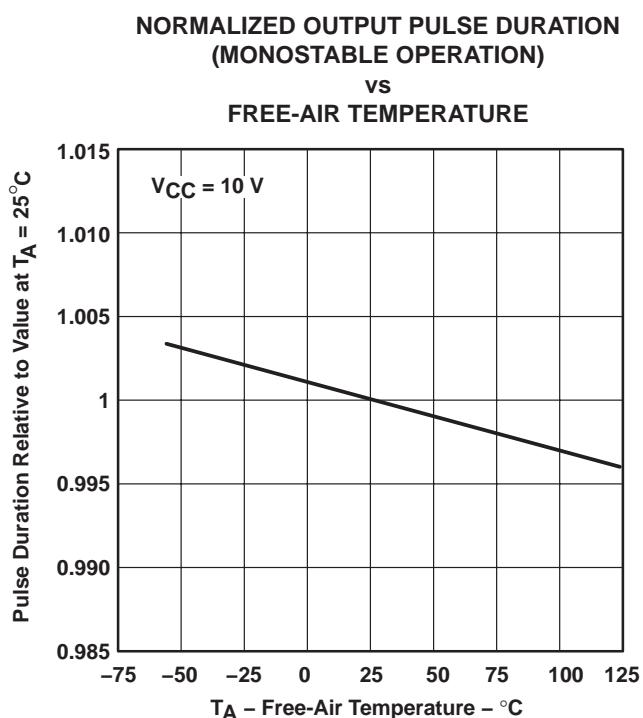


Figure 7

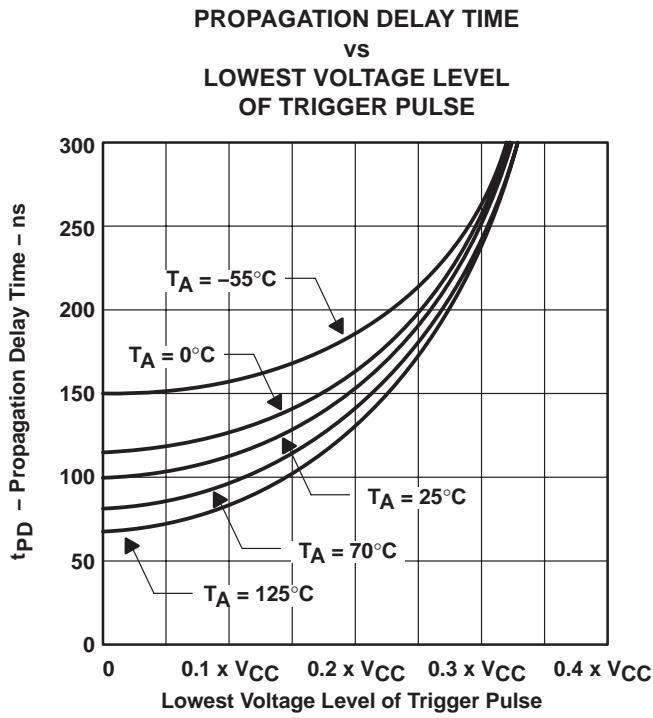


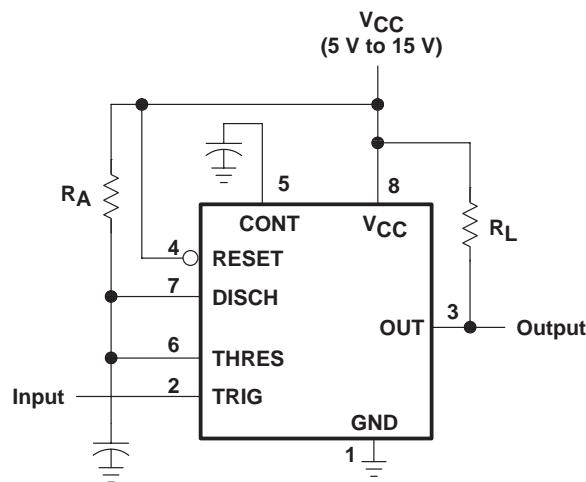
Figure 8

[†]Data for temperatures below 0°C and above 70°C are applicable for SE555 series circuits only.

APPLICATION INFORMATION

monostable operation

For monostable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop (\bar{Q} goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop (\bar{Q} goes high), drives the output low, and discharges C through Q1.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC} . The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC} .

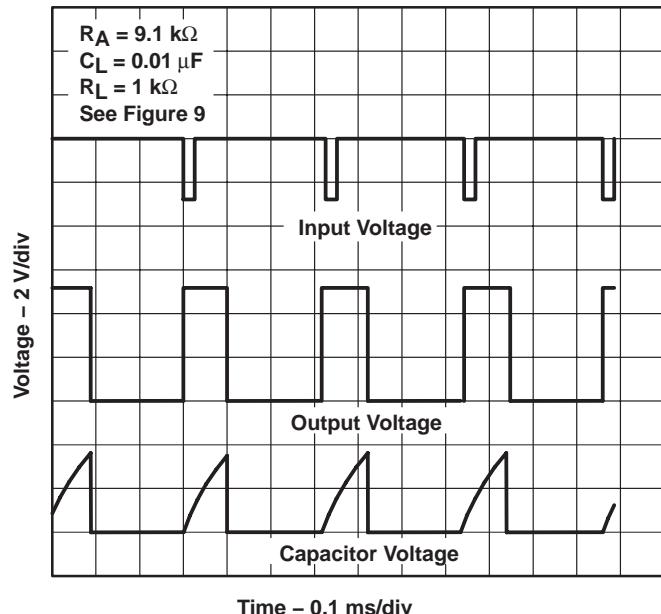


Figure 10. Typical Monostable Waveforms

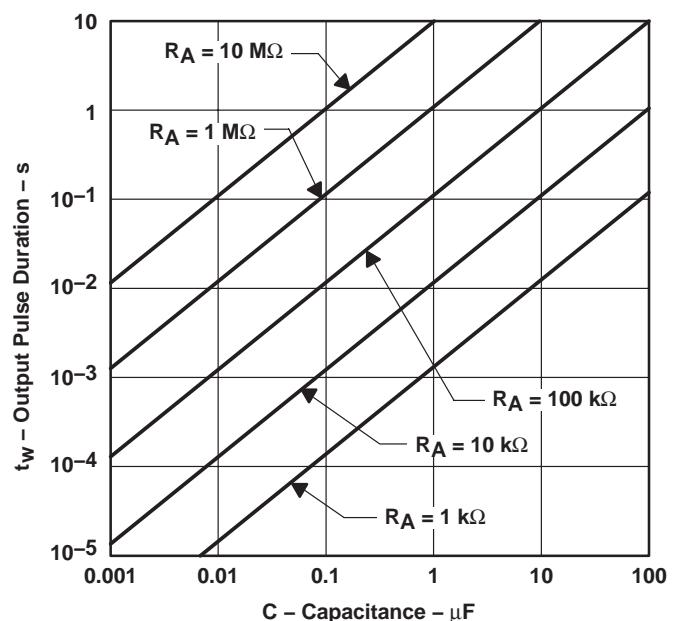


Figure 11. Output Pulse Duration vs Capacitance

NE555, SA555, SE555 PRECISION TIMERS

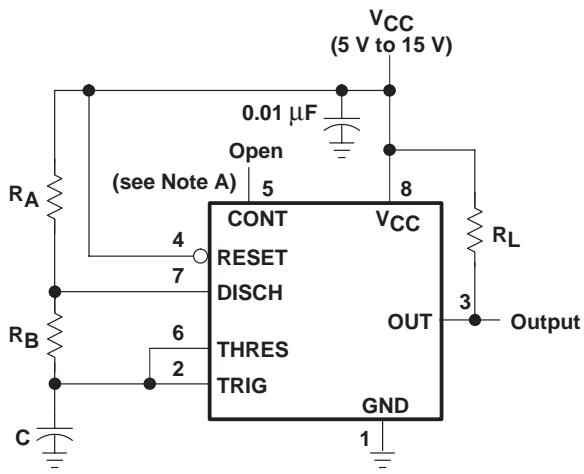
SLFS022E – SEPTEMBER 1973 – REVISED MARCH 2004

APPLICATION INFORMATION

astable operation

As shown in Figure 12, adding a second resistor, R_B , to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B .

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

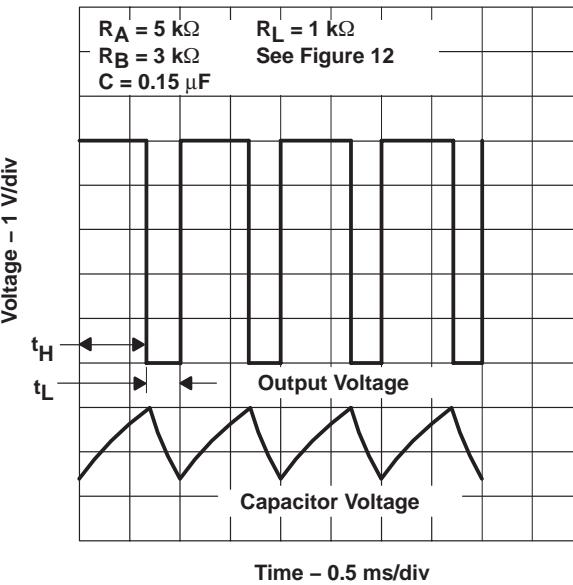


Figure 13. Typical Astable Waveforms

APPLICATION INFORMATION

astable operation (continued)

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693 (R_A + R_B) C$$

$$t_L = 0.693 (R_B) C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693 (R_A + 2R_B) C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B) C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

Output waveform duty cycle

$$= \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

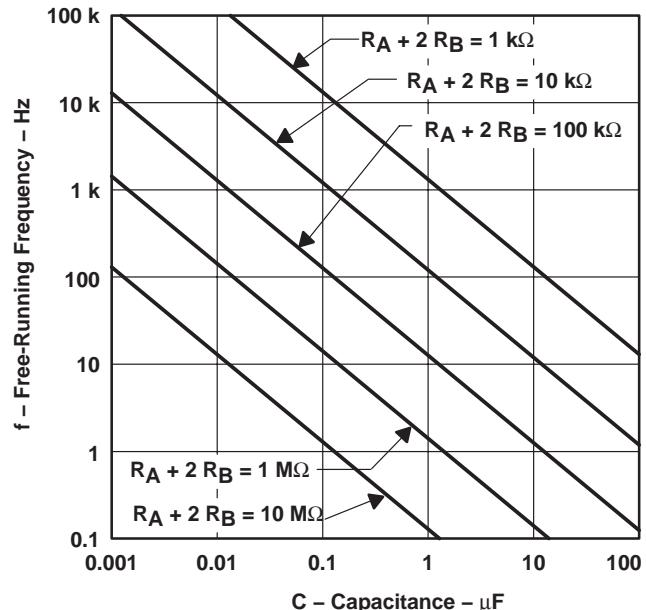


Figure 14. Free-Running Frequency

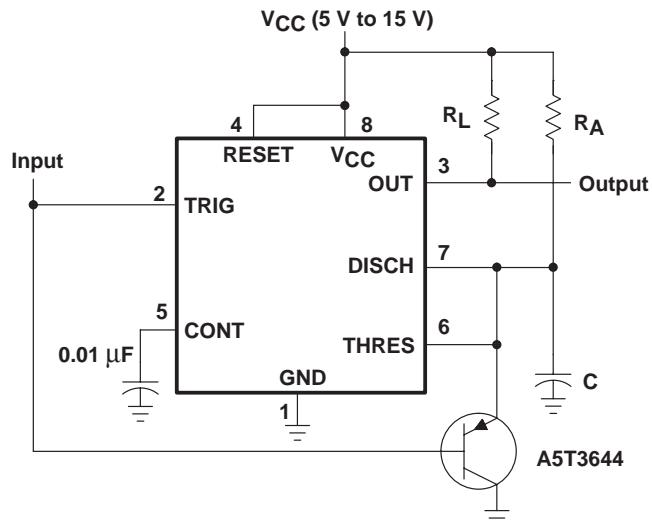
NE555, SA555, SE555 PRECISION TIMERS

SLFS022E – SEPTEMBER 1973 – REVISED MARCH 2004

APPLICATION INFORMATION

missing-pulse detector

The circuit shown in Figure 15 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 16.



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 15. Circuit for Missing-Pulse Detector

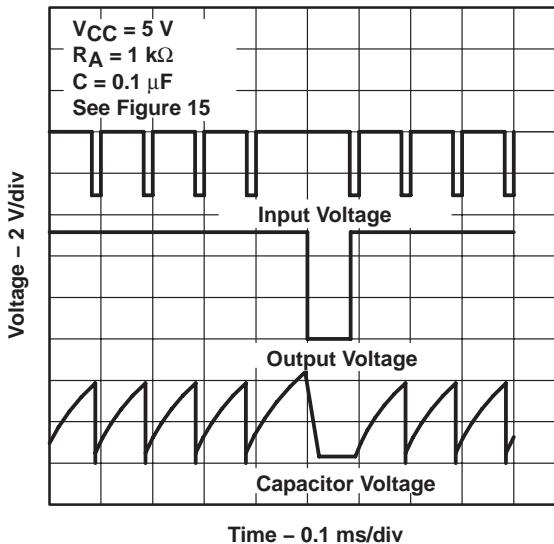


Figure 16. Completed-Timing Waveforms
for Missing-Pulse Detector

APPLICATION INFORMATION

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

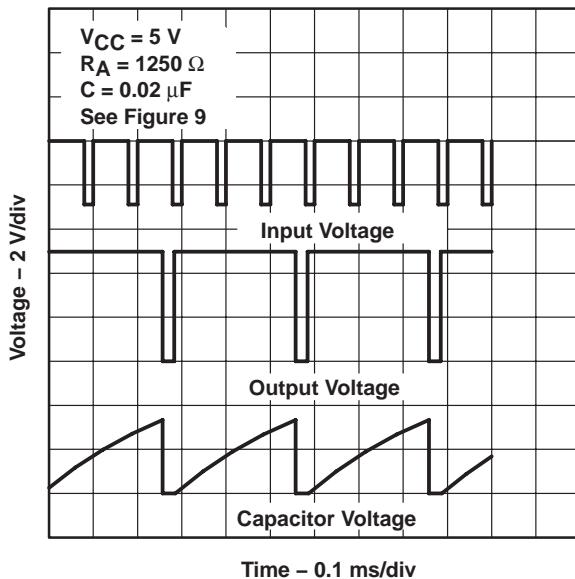


Figure 17. Divide-by-Three Circuit Waveforms

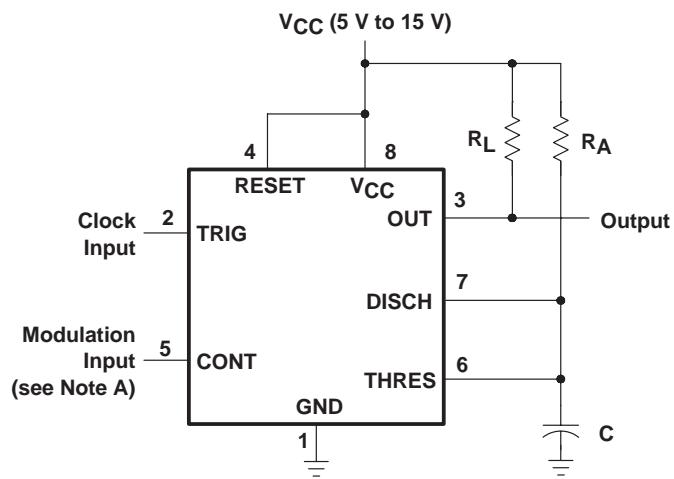
pulse-width modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.

NE555, SA555, SE555 PRECISION TIMERS

SLFS022E – SEPTEMBER 1973 – REVISED MARCH 2004

APPLICATION INFORMATION



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

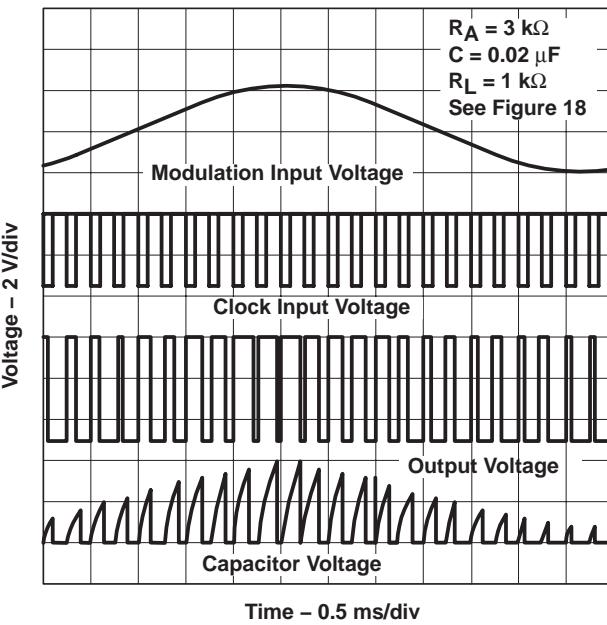
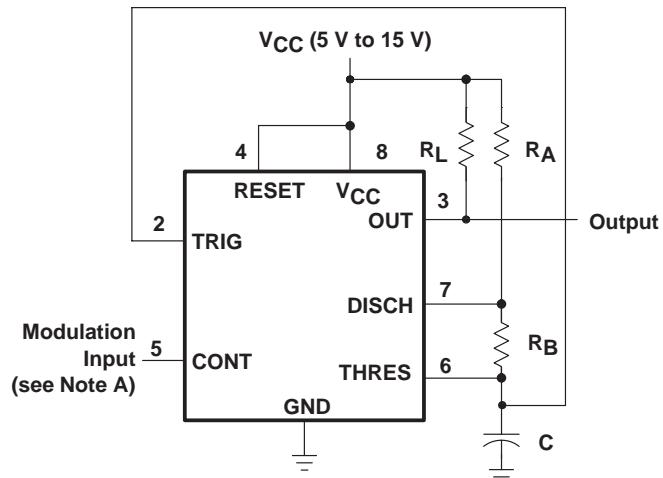


Figure 19. Pulse-Width-Modulation Waveforms

pulse-position modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

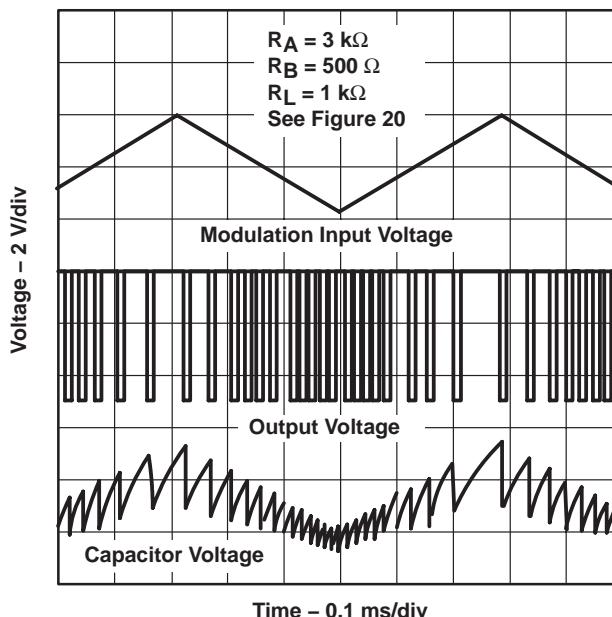
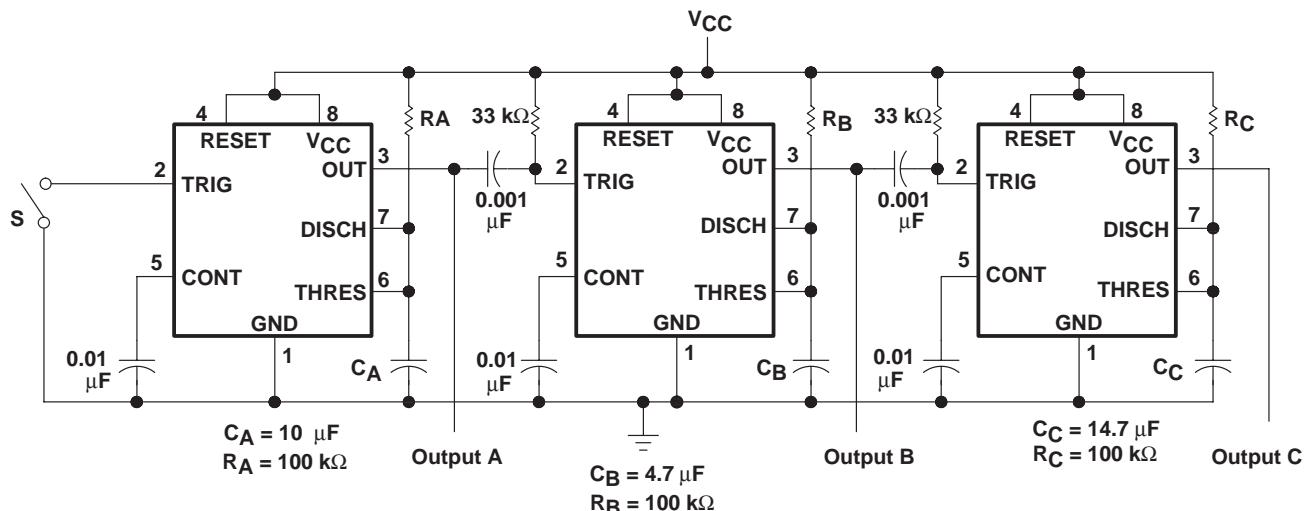


Figure 21. Pulse-Position-Modulation Waveforms

APPLICATION INFORMATION

sequential timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: S closes momentarily at $t = 0$.

Figure 22. Sequential Timer Circuit

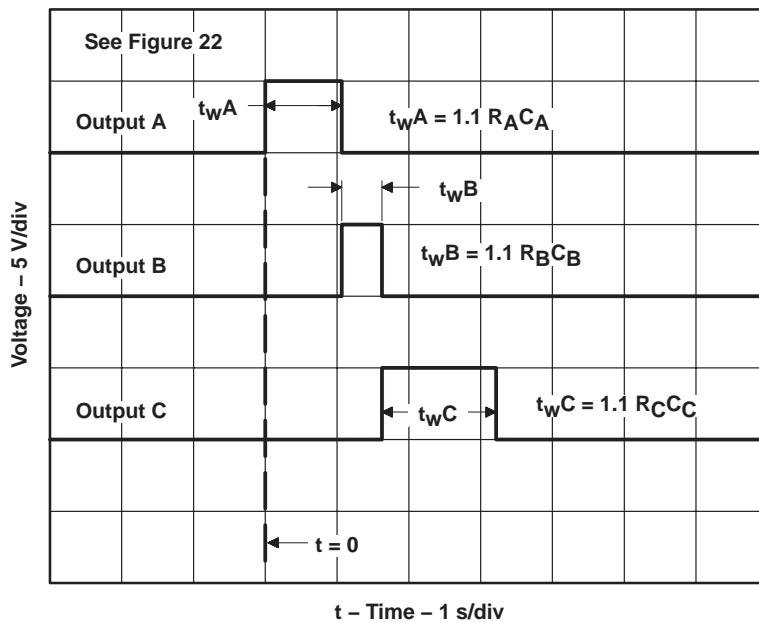


Figure 23. Sequential Timer Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/10901BPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
NE555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
NE555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
NE555PSLE	OBsolete	SO	PS	8		TBD	Call TI	Call TI
NE555PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555PWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
NE555Y	OBsolete			0		TBD	Call TI	Call TI
SA555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SA555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SA555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SE555D	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
SE555DR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
SE555FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SE555JG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SE555JGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SE555N	OBsolete	PDIP	N	8		TBD	Call TI	Call TI
SE555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

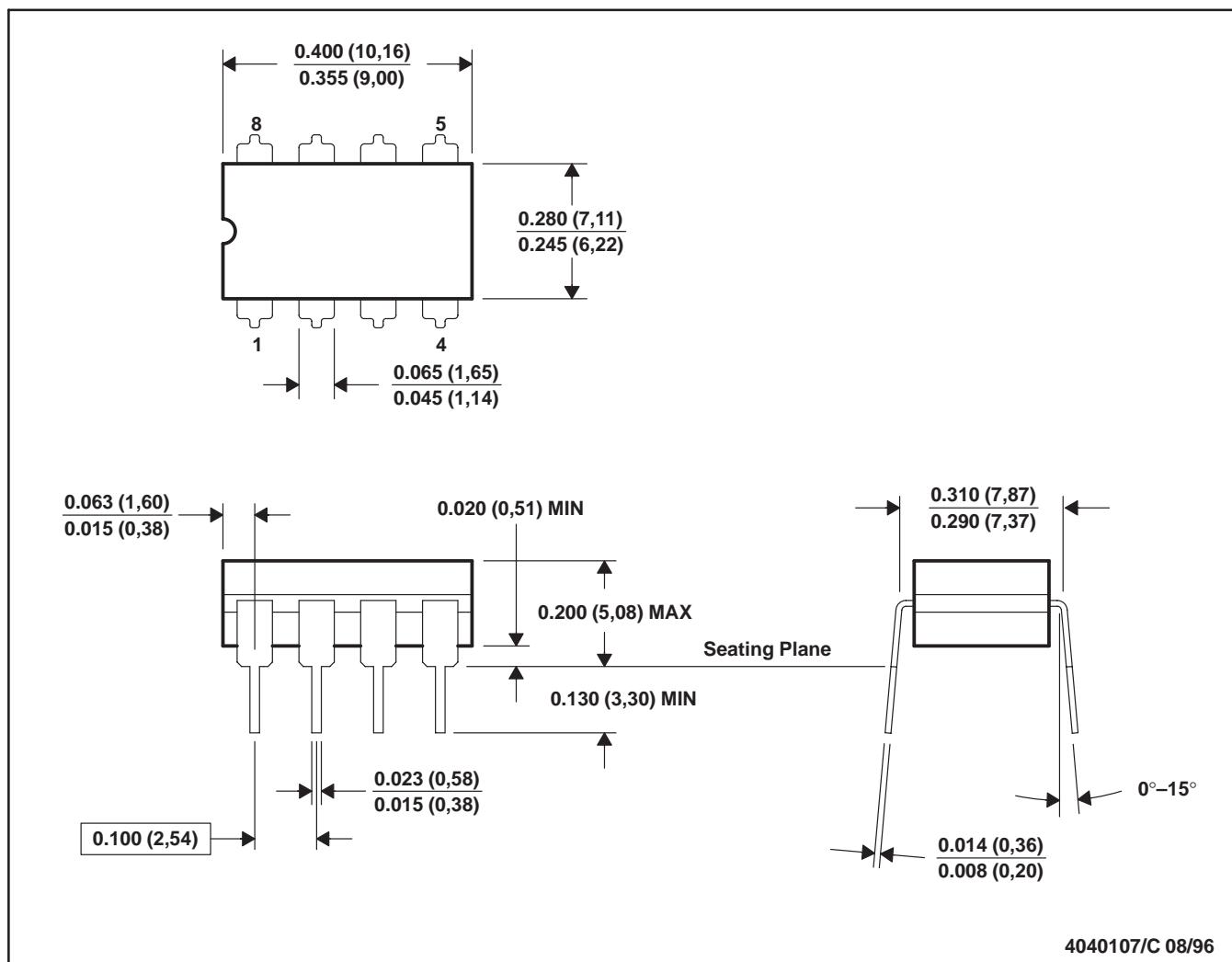
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

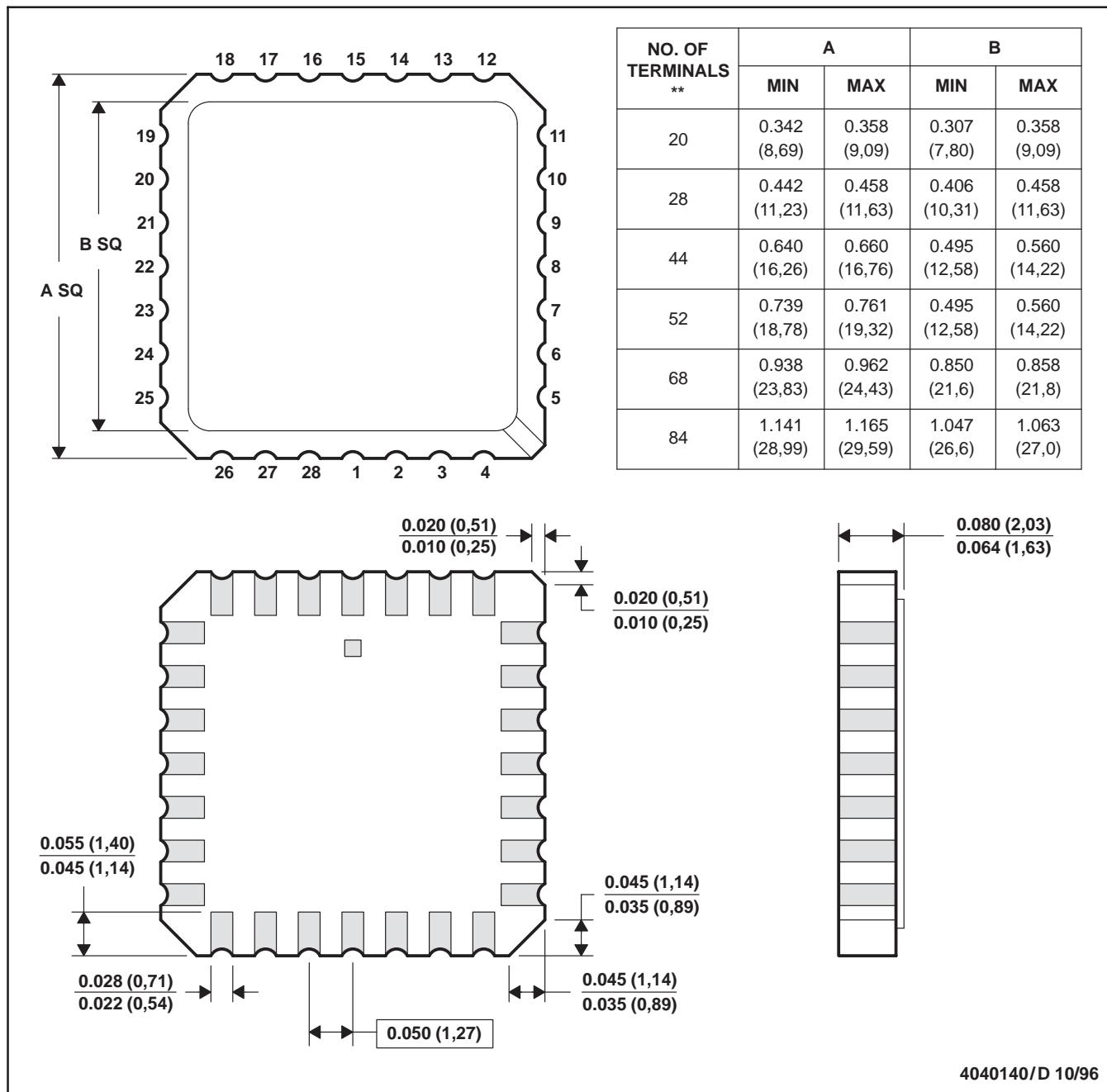


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification.
 - Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

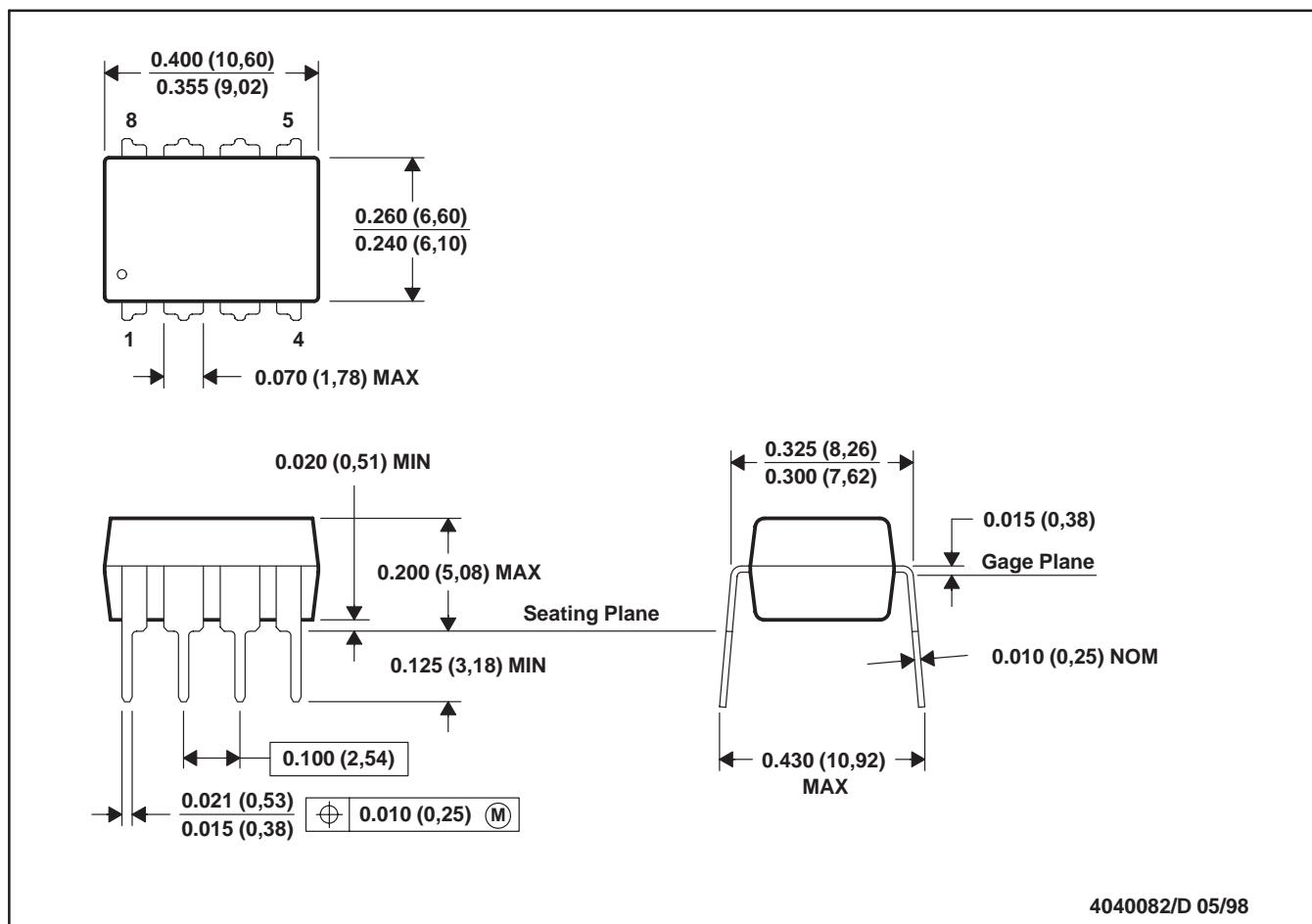
D. The terminals are gold plated.

E. Falls within JEDEC MS-004

4040140/D 10/96

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE

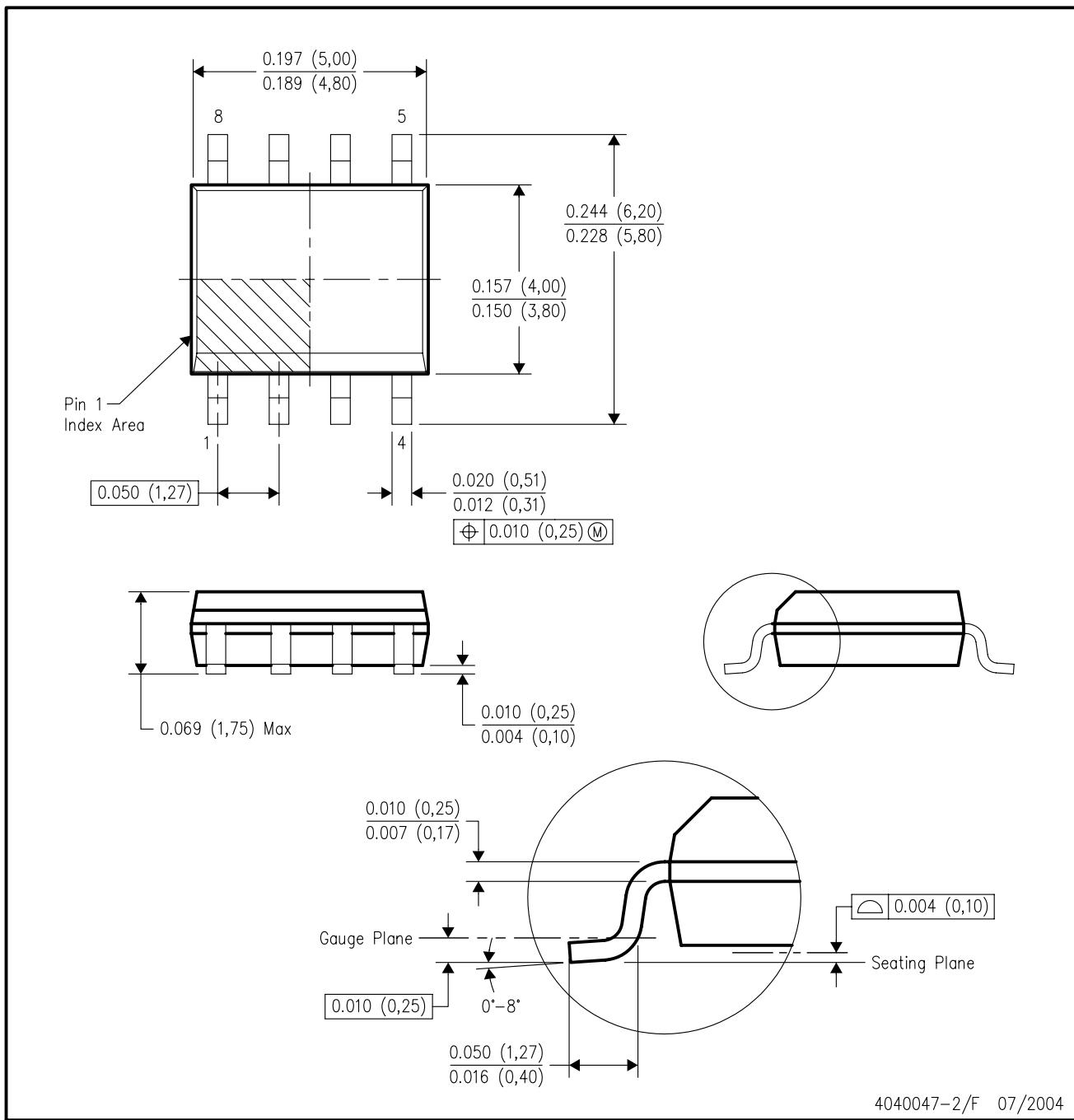


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



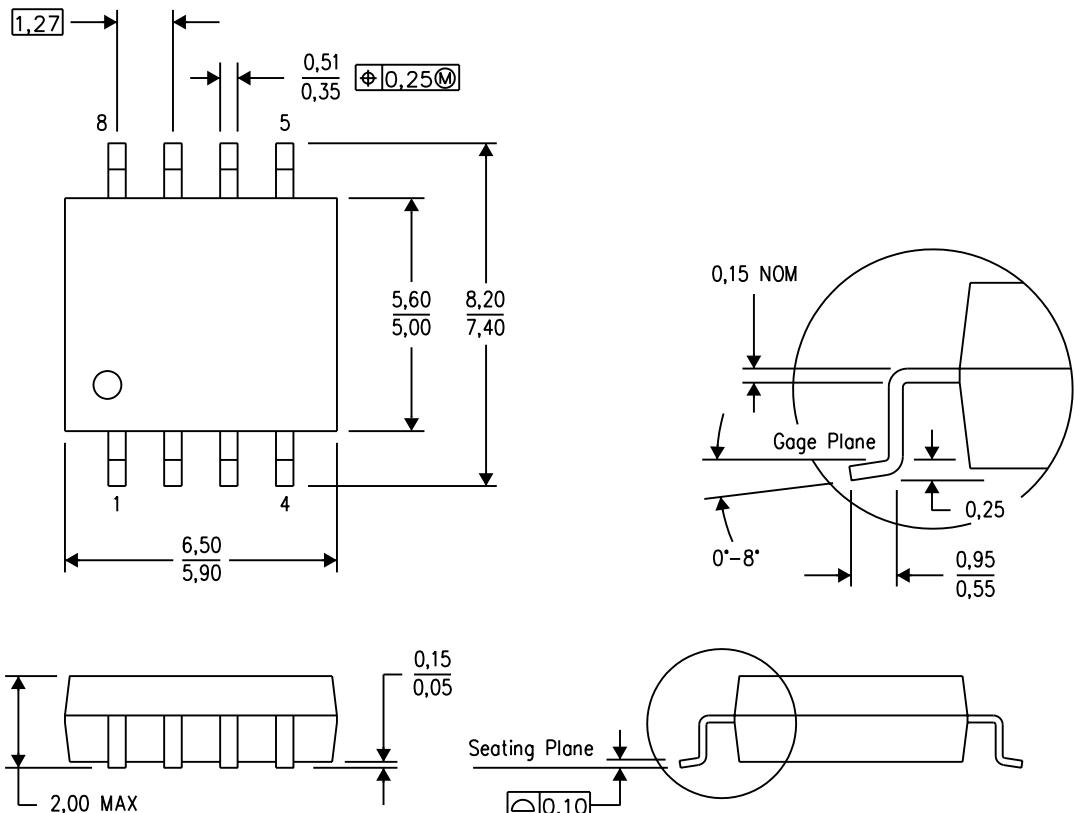
4040047-2/F 07/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



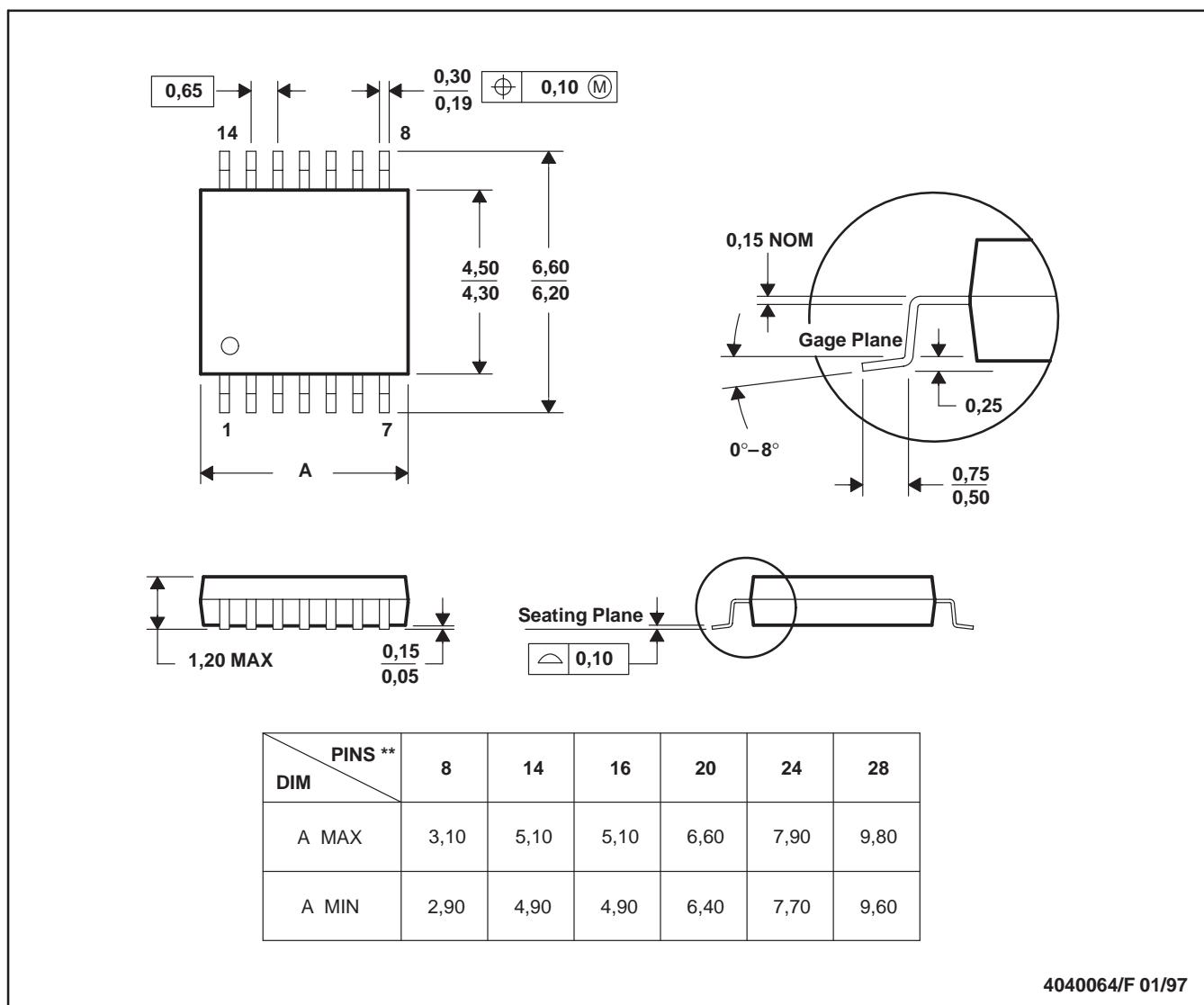
4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G^{**})

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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View ROHS Compliant Devices

View RoHS Compliant Devices

 clear gif**NE555, Status: ACTIVE**

Single Precision Timer

 View RoHS Compliant Devices clear gif clear gif Features Quality & Pb-Free Data Related Products Tools & Software Samples Pricing/Packaging Inventory Symbols/Footprints Technical Documents Applications Notes Simulation Models Reference Designs**Refine Your Selection**

- Selection Guides
- Analog & Mixed-Signal

Support

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup

Datasheet H Download Datasheet**NE555, SA555, SE555 (Rev. E)** (ne555.pdf, 479 KB)26 Mar 2004 [Download](#) !

	NE555	TLC555
VCC(Min)(V)	4.5	2
VCC(Max)(V)	16	15
Frequency(Max)(MHz)	0.5	2.1
Operating Temp Range(Celsius)	0 to 70	-40 to 125,-40 to 85,-55 to 125,0 to 70
Pin/Package	8PDIP,8SO,8SOIC,8TSSOP	14TSSOP,20LCCC,8CDIP,8PDIP,8SO,8SOIC
Approx. 1KU Price (US\$)	.16	.26
	Samples	Samples
	Inventory	Inventory

Product Information Features Save this to your personal library

Timing From Microseconds to Hours
 Astable or Monostable Operation
 Adjustable Duty Cycle
 TTL-Compatible Output Can Sink or Source up to 200 mA

 Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC} . These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools		Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Symbols	Footprints	Samples
NE555D	ACTIVE	0 to 70	0.16 1KU	SOIC (D) 8	View	75	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples
NE555DE4	ACTIVE	0 to 70	0.18 1KU	SOIC (D) 8	View	75	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples
NE555DG4	ACTIVE	0 to 70	0.18 1KU	SOIC (D) 8	View	75	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples
NE555DR	ACTIVE	0 to 70	0.16 1KU	SOIC (D) 8	View	2500	<input type="checkbox"/>	<input type="checkbox"/>	Contact TI Distributor or Sales Office
NE555DRE4	ACTIVE	0 to 70	0.18 1KU	SOIC (D) 8	View	2500	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples
NE555DRG4	ACTIVE	0 to 70	0.18 1KU	SOIC (D) 8	View	2500	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples
NE555P	ACTIVE	0 to 70	0.16 1KU	PDIP (P) 8	View	50	<input type="checkbox"/>	<input type="checkbox"/>	Contact TI Distributor or Sales Office
NE555PE4	ACTIVE	0 to 70	0.16 1KU	PDIP (P) 8	View	50	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples
NE555PSLE	OBsolete	0 to 70		SO (PS) 8	View			<input type="checkbox"/>	Not Available
NE555PSR	ACTIVE	0 to 70	0.16 1KU	SO (PS) 8	View	2000	<input type="checkbox"/>	<input type="checkbox"/>	Contact TI Distributor or Sales Office
NE555PSRE4	ACTIVE	0 to 70	0.16 1KU	SO (PS) 8	View	2000	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples
NE555PW	ACTIVE	0 to 70	0.16 1KU	TSSOP (PW) 8	View	150	<input type="checkbox"/>	<input type="checkbox"/>	Contact TI Distributor or Sales Office
NE555PWE4	ACTIVE	0 to 70	0.16 1KU	TSSOP (PW) 8	View	150	<input type="checkbox"/>	<input type="checkbox"/>	Request Free Samples
NE555PWR	ACTIVE	0 to 70	0.16 1KU	TSSOP (PW) 8	View	2000	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples
NE555PWRE4	ACTIVE	0 to 70	0.16 1KU	TSSOP (PW) 8	View	2000	<input type="checkbox"/>	<input type="checkbox"/>	Purchase Samples
NE555Y	OBsolete	0 to 70		0					Not Available

Inventory

TI Inventory Status			Reported Distributor Inventory					
As of 9:42 AM GMT, 29 Nov 2005			As of 9:42 AM GMT, 29 Nov 2005					
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
NE555D	>10k*	>10k 12 Dec	8 Weeks	Americas	Arrow	>1k	<input type="checkbox"/>	
					Avnet	>1k	<input type="checkbox"/>	
					DigiKey	>1k	<input type="checkbox"/>	
					Newark InOne	>1k	<input type="checkbox"/>	
				Europe	P&S	8	<input type="checkbox"/>	
					Abacus Polar	>1k	<input type="checkbox"/>	
					Arrow Northern Europe	>1k	<input type="checkbox"/>	
					Arrow Southern Europe	>1k	<input type="checkbox"/>	
					Avnet-SILICA	>1k	<input type="checkbox"/>	
					EBV Elektronik	>1k	<input type="checkbox"/>	
					Rutronik	50	<input type="checkbox"/>	
					Spoerle	>1k	<input type="checkbox"/>	
NE555DE4	As of 9:42 AM GMT, 29 Nov 2005			As of 9:42 AM GMT, 29 Nov 2005				
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
NE555DG4	1125*	>10k 12 Dec	8 Weeks	None Reported View Distributors				
				As of 9:42 AM GMT, 29 Nov 2005				

[View all Distributors](#)

[Choose a Region](#)



	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 19 Dec	8 Weeks	None Reported View Distributors			

NE555DR	As of 9:42 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

0*	>10k 8 Dec	8 Weeks	Americas	Avnet	>1k		
				DigiKey	>1k		
			Europe	Abacus Polar	>1k		
				Arrow Northern Europe	>1k		
				Arrow Southern Europe	>1k		
				Avnet-SILICA	>1k		
				EBV Elektronik	>1k		
				Rutronik	>1k		
				Spoerle	>1k		

NE555DRE4	As of 9:42 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

>10k*	2296 1 Dec	8 Weeks	None Reported View Distributors				
	>10k 14 Dec						

NE555DRG4	As of 9:42 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

0*	>10k 12 Dec	8 Weeks	None Reported View Distributors				
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NE555P	As of 9:42 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

>10k*	>10k 8 Dec	4 Weeks	Americas	Avnet	>1k		
				DigiKey	>1k		
				Newark InOne	>1k		
			Asia	P&S	3		
			Europe	Abacus Polar	950		
				Arrow Northern Europe	>1k		
				Arrow Southern Europe	>1k		
				Avnet-SILICA	>1k		
				EBV Elektronik	>1k		

NE555PE4	As of 9:42 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

0*		6 Weeks	None Reported View Distributors				
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NE555PSR	As of 9:42 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

0*	>10k 30 Jan	9 Weeks	Americas	DigiKey	>1k		
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NE555PSRE4	As of 9:42 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

0*	>10k 30 Jan	9 Weeks	None Reported View Distributors				
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NE555PW	As of 9:42 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 5 Jan	10 Weeks	None Reported View Distributors			
NE555PWE4	As of 9:42 AM GMT, 29 Nov 2005			As of 9:42 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 5 Jan	10 Weeks	None Reported View Distributors			
NE555PWR	As of 9:42 AM GMT, 29 Nov 2005			As of 9:42 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 5 Jan	5 Weeks	None Reported View Distributors			
NE555PWRE4	As of 9:42 AM GMT, 29 Nov 2005			As of 9:42 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 5 Jan	5 Weeks	None Reported View Distributors			

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your [TI Authorized Distributor](#), including those [listed above](#), for real time stock information.

** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred [TI Authorized Distributor](#) for additional information.

Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
NE555D <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555DE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555DG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555DR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555DRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555DRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555P <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
NE555PE4 <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
NE555PSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555PSRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555PW <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555PWE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555PWR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
NE555PWRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

Technical Documents

Datasheets	Keep track of what's new
NE555, SA555, SE555 (Rev. E) (ne555.pdf, 479 KB) 26 Mar 2004 Download	
More Literature Standard Linear Products Cross-Reference (Rev. C) (slyt017c.pdf, 632 KB) 05 Apr 2005 Download	

