

**5V / 3.3V / 12V**  
Page : 35

**1.8V / 0.9V**  
Page : 36

**1.5V / 1.05V / 1.8V**  
Page : 37

**CPU CORE**  
Page : 34

**+1.2V**  
Page : 38

**BATTERY CHARGER**  
Page : 39

**BATTERY SELECT**  
Page : 40

5VPCU  
3V\_ALWAYS  
+12V  
+5V  
3V\_S5  
3VSUS  
5VSUS  
2.5VSUS  
+2.5V  
+1.8V  
MVREF\_DM  
SMDDR\_VTERM  
1.5V\_S5  
+1.5V  
AGP\_VCC (+1.5V)  
1.2VCCT  
VTT  
VCC\_CORE  
VGA\_CORE  
2.5V\_VGA

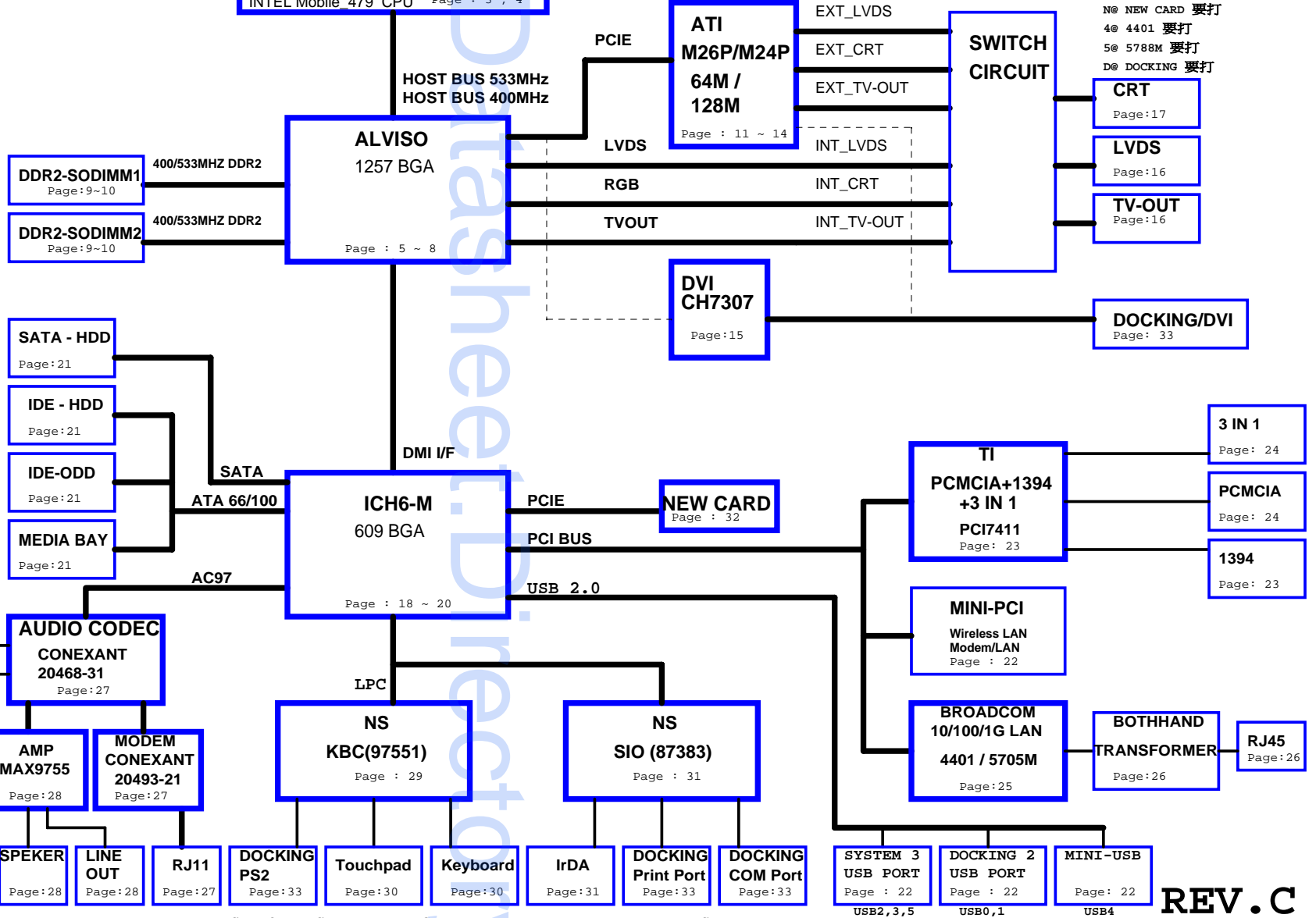
**CLOCK GEN ICS**  
ICS954201  
Page : 2

**Centrino**  
DOTHAN  
CELEROM-M  
INTEL Mobile 479 CPU Page : 3 , 4

**CRANE2 ( ZL3 )**

ED@ INT. VGA WITH DOCK  
ID@ INT. VGA WITH DOCK  
ND@ W/O DOCKING要打

BOM MARK  
E@ EXT VGA 要打  
I@ INTVGA 要打  
SA@ SATA 要打  
F@ FIXED ODD要打  
SW@ SWAPPABLE ODD 要打  
3@ 3in1 要打  
N@ NEW CARD 要打  
4@ 4401 要打  
5@ 5788M 要打  
D@ DOCKING 要打



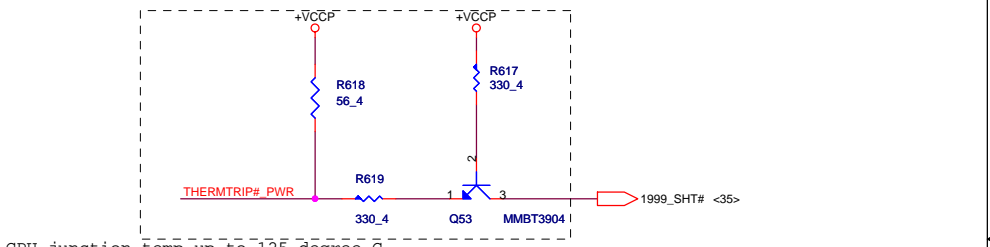
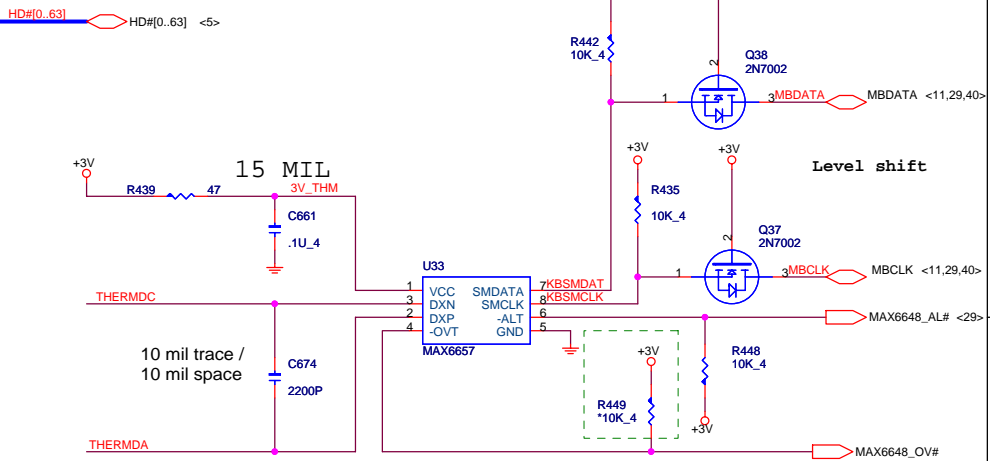
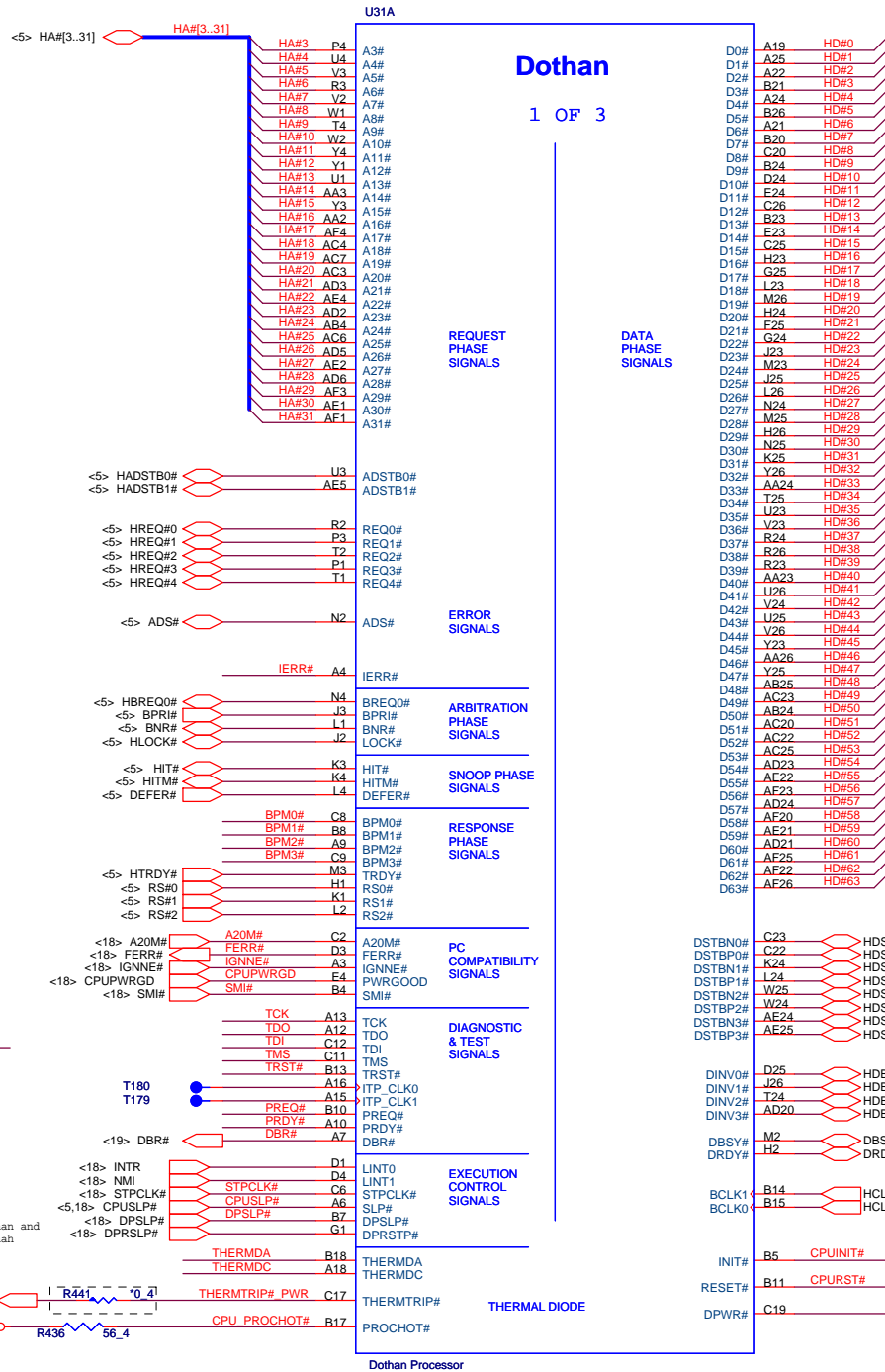
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD24	INTA#	BROADCOM LAN
REQ2# / GNT2#	AD19	INTB# , INTD#	MINI-PCI
REQ1# / GNT1#	AD17	INTC# , INTD# , INTA#	TI 7411

**REV. C**

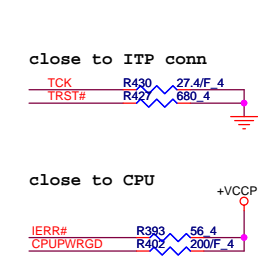
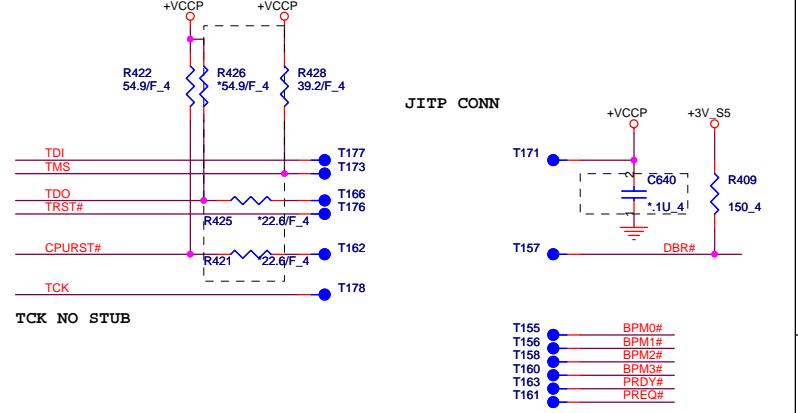
**PROJECT : ZL3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>BLOCK DIAGRAM</b>	C
Date:	Tuesday, March 29, 2005	Sheet 1 of 40





CPU junction temp up to 125 degree C  
output signal. shut down system  
DEPOP R425, R426, R421, C640 WHEN NO JITP



## QUANTA COMPUTER

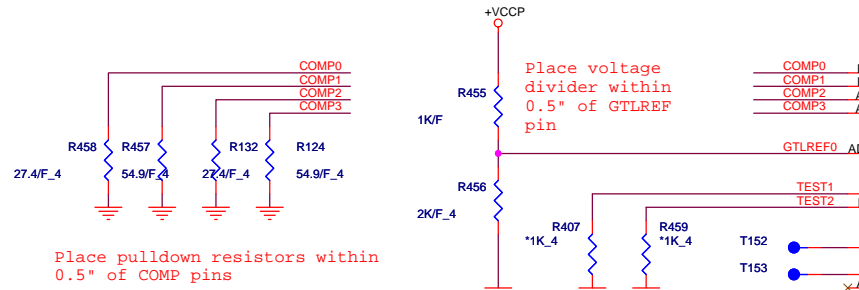
Title  
Dothan Processor (HOST)

Size  
Document Number  
ZL3

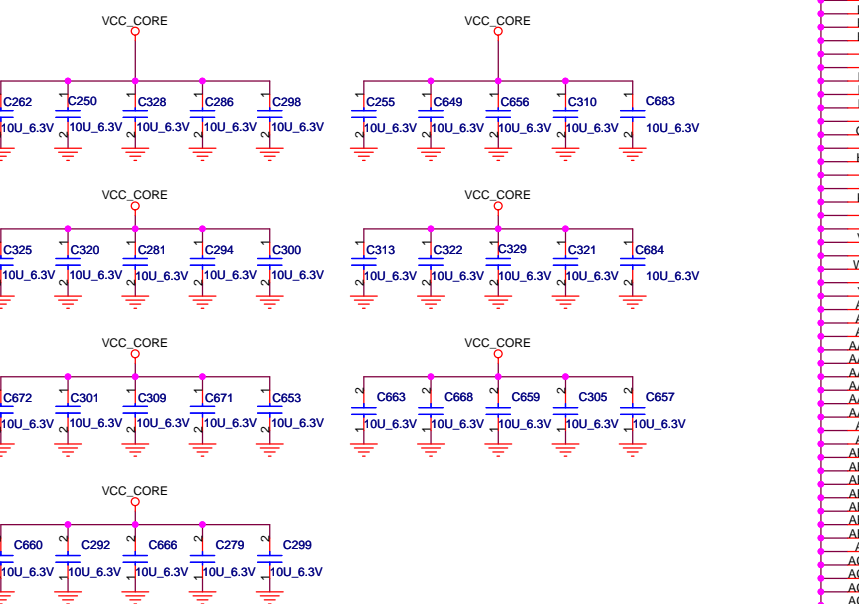
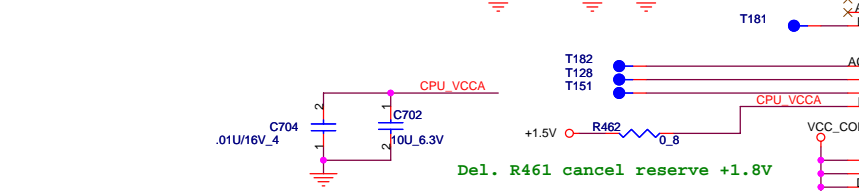
Date: Tuesday, March 29, 2005

Sheet 3 of 40

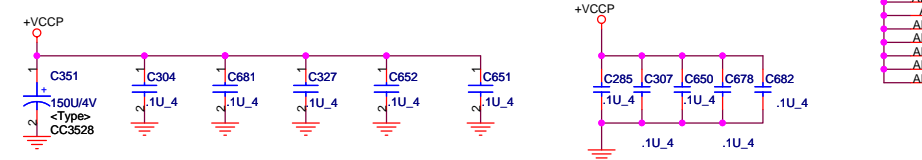
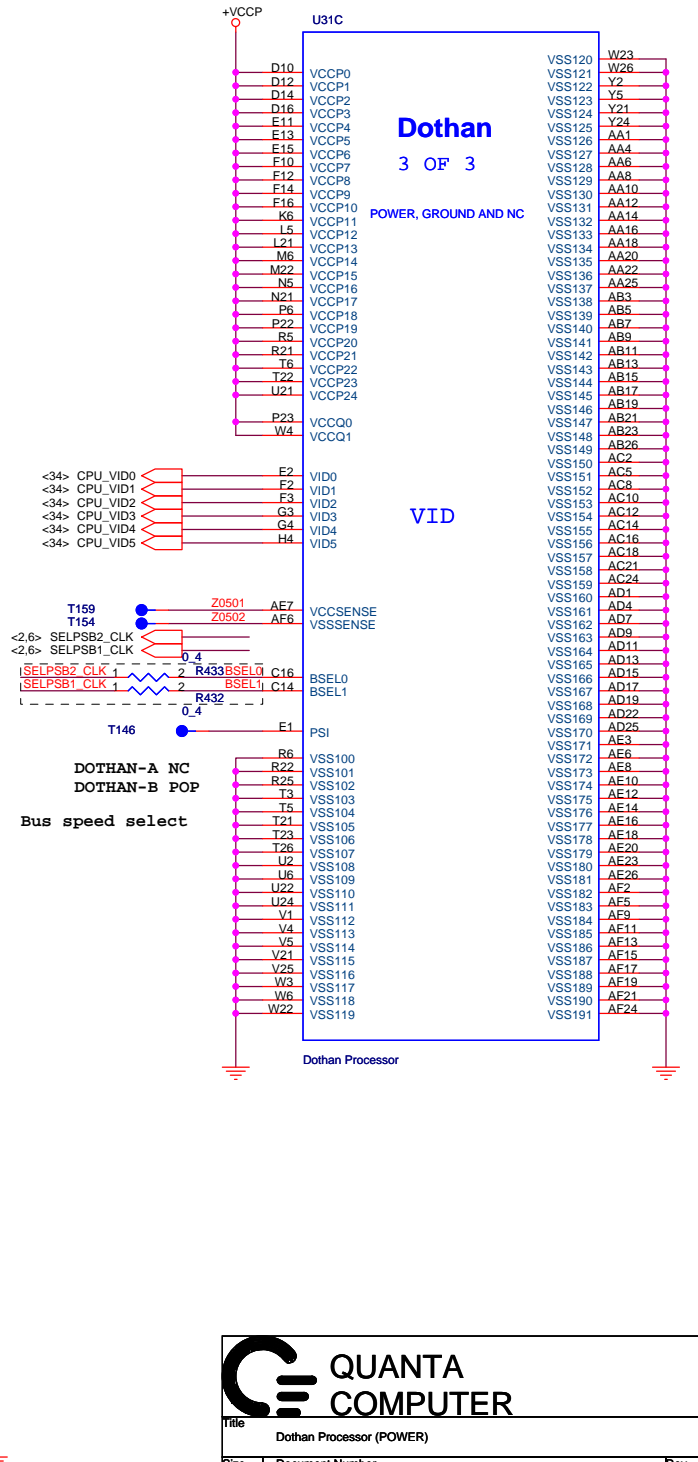
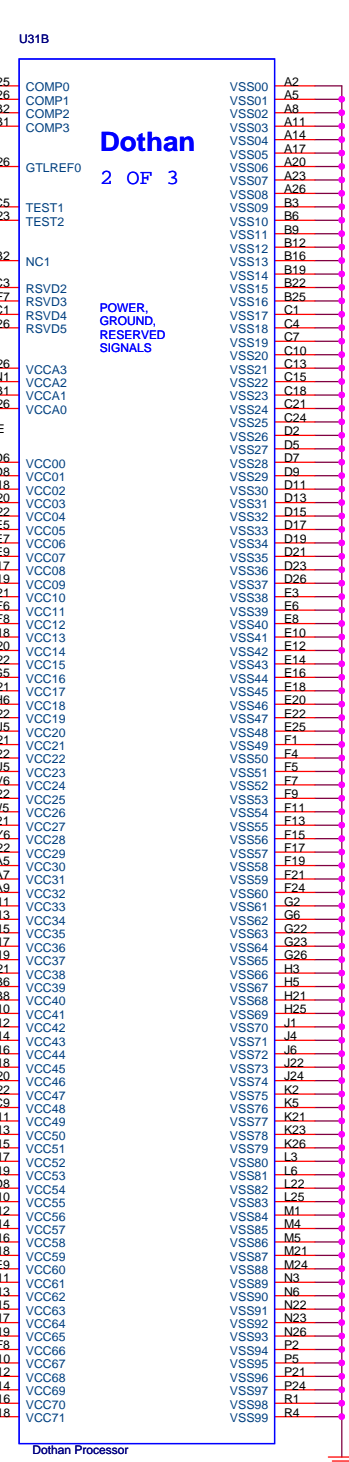
Rev C



Place pull-down resistors within 0.5" of COMP pins



Total caps = 2633 uF  
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



**QUANTA COMPUTER**

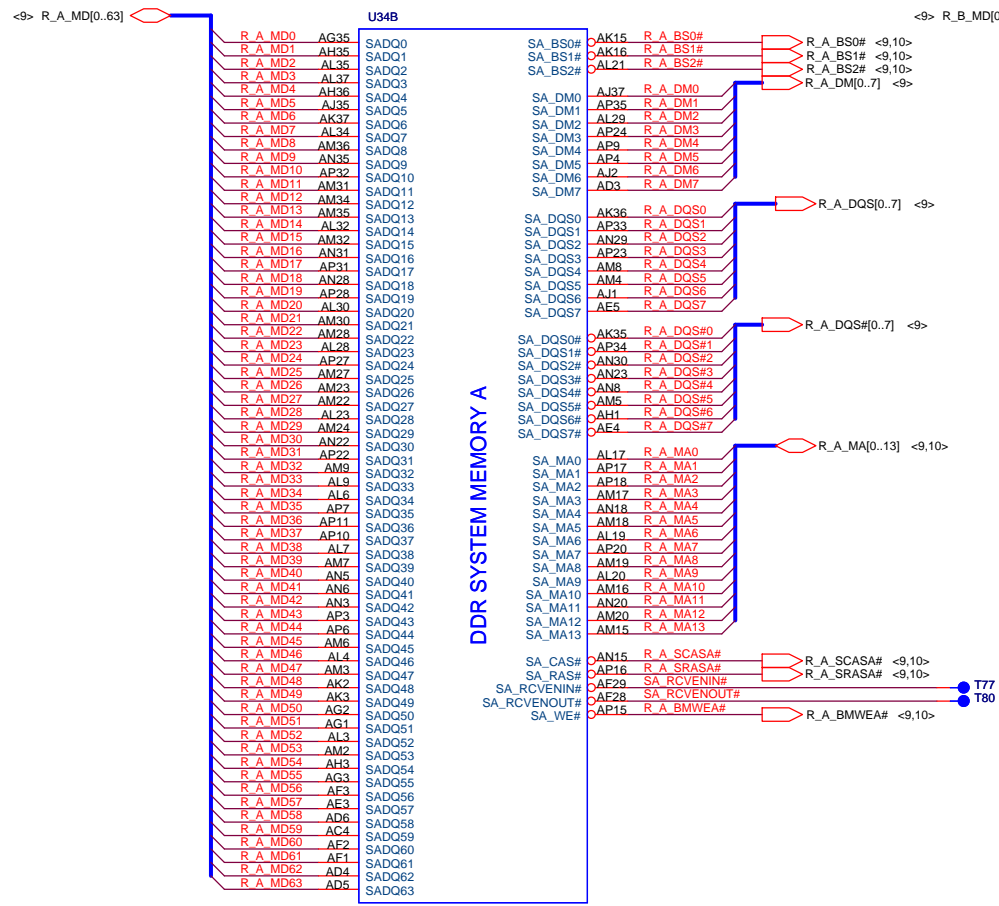
Title: Dothan Processor (POWER)

Size: Document Number ZL3

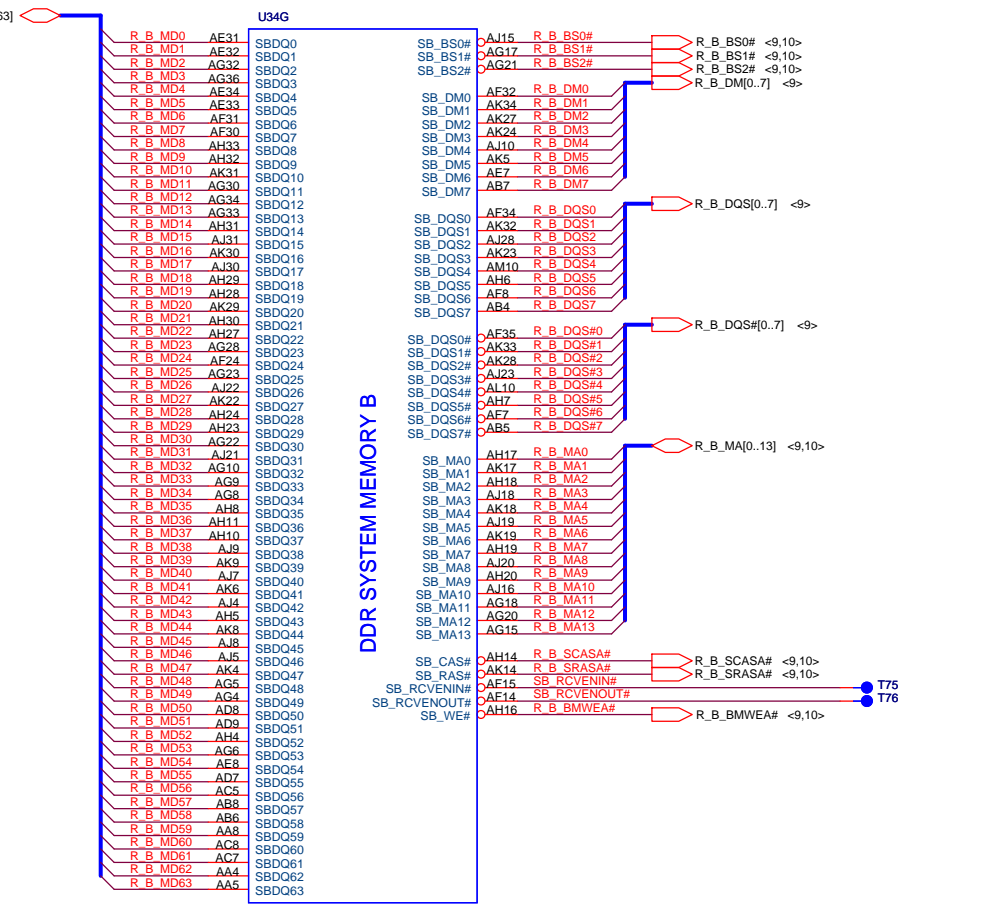
Date: Wednesday, March 30, 2006 Sheet 4 of 40 Rev C







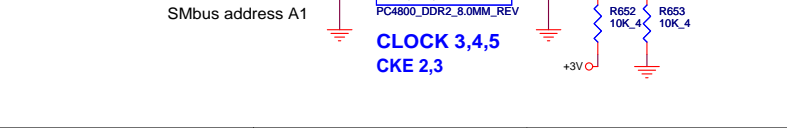
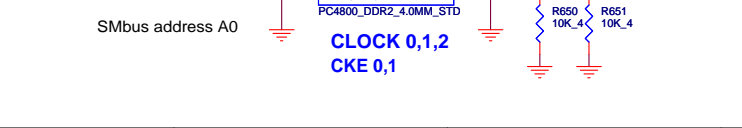
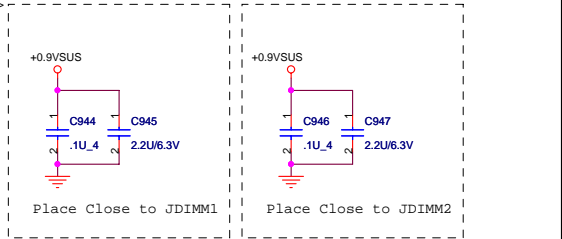
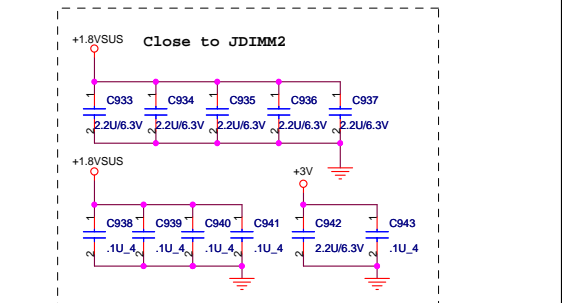
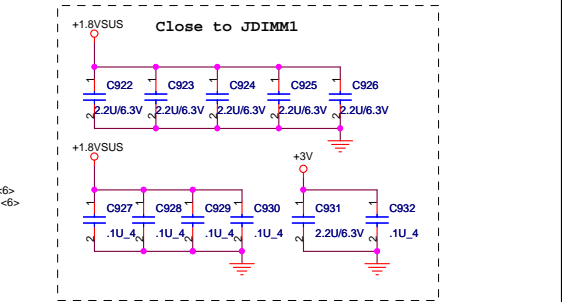
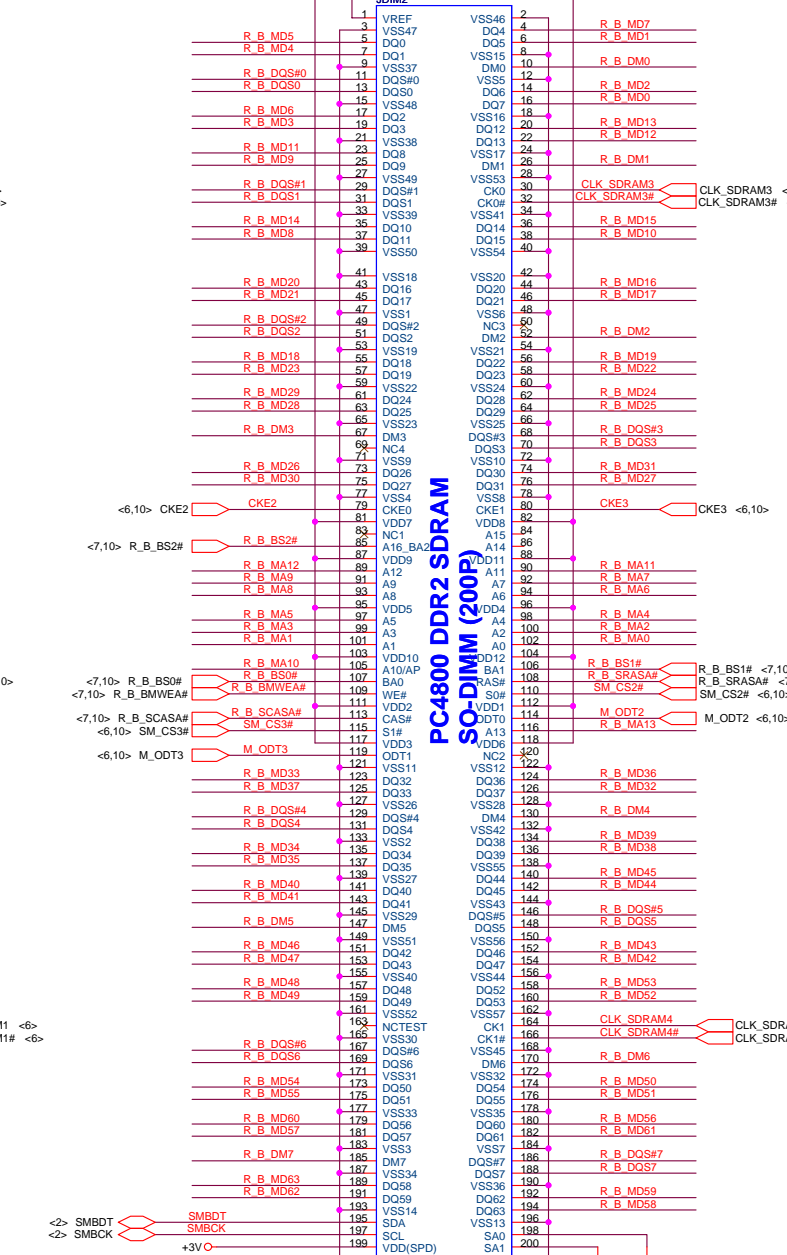
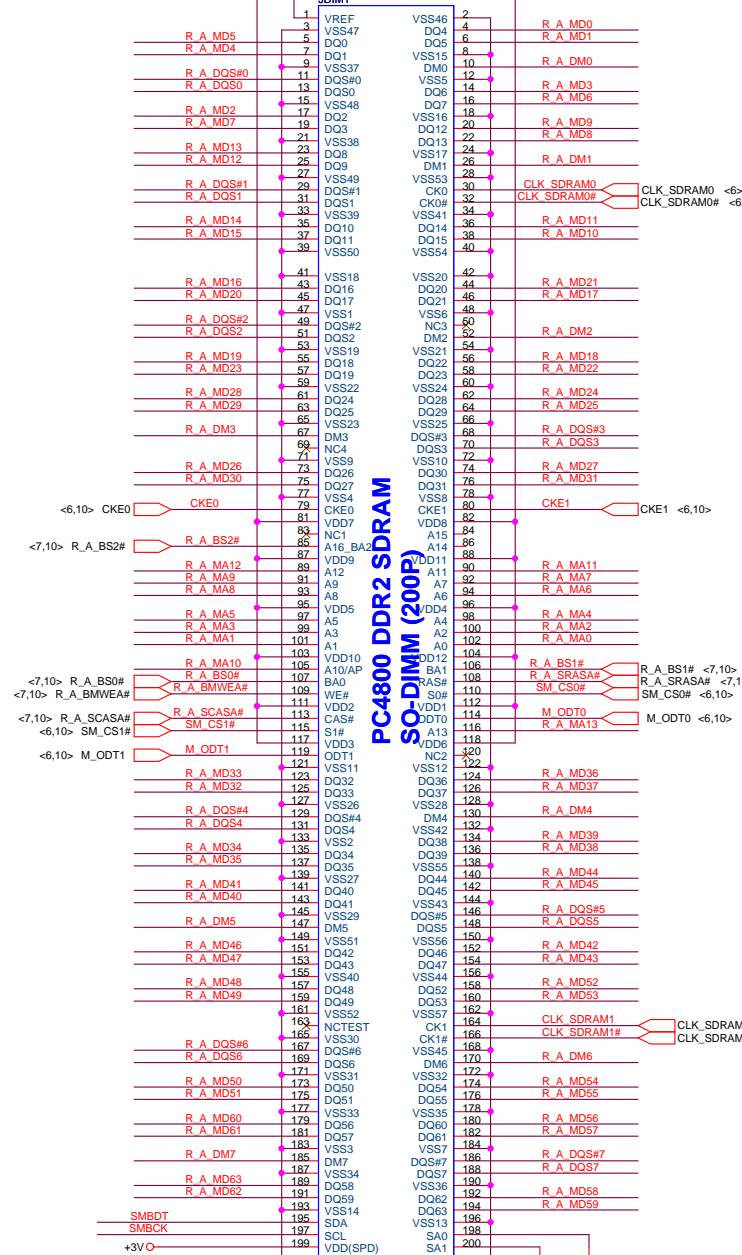
@ALVISO\_GM/GML



@ALVISO\_GM/GML

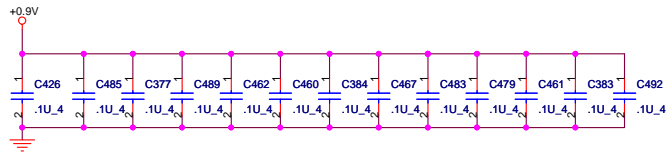




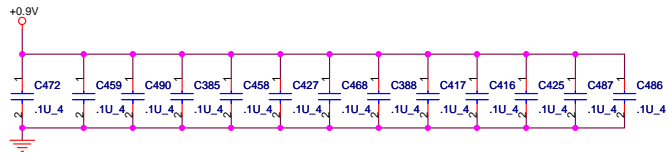


**PROJECT : ZL3**  
**Quanta Computer Inc.**

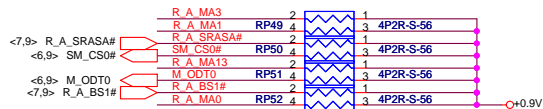
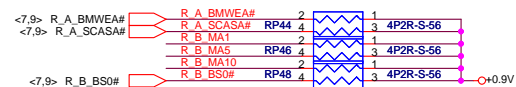
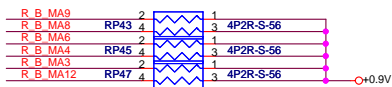
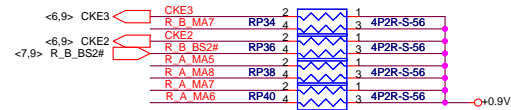
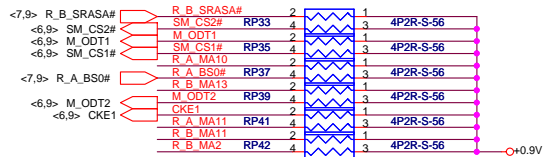
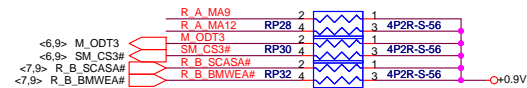
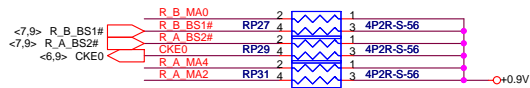
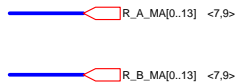
Size	Document Number	Rev
	<b>DDR2 SO-DIMM ( 200P )</b>	C
Date:	Tuesday, March 29, 2005	Sheet 9 of 40



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V

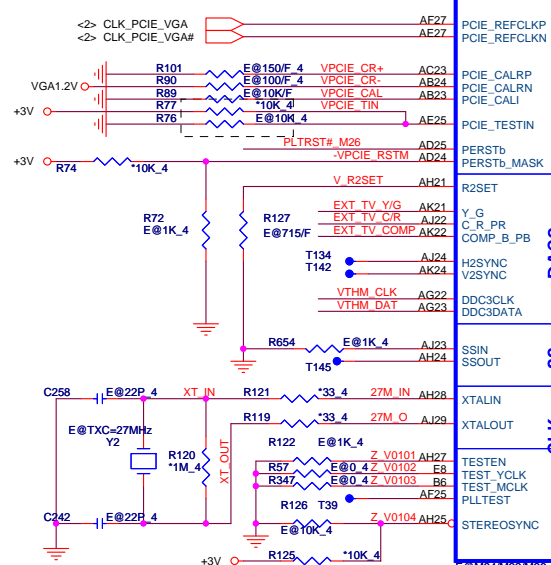


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V

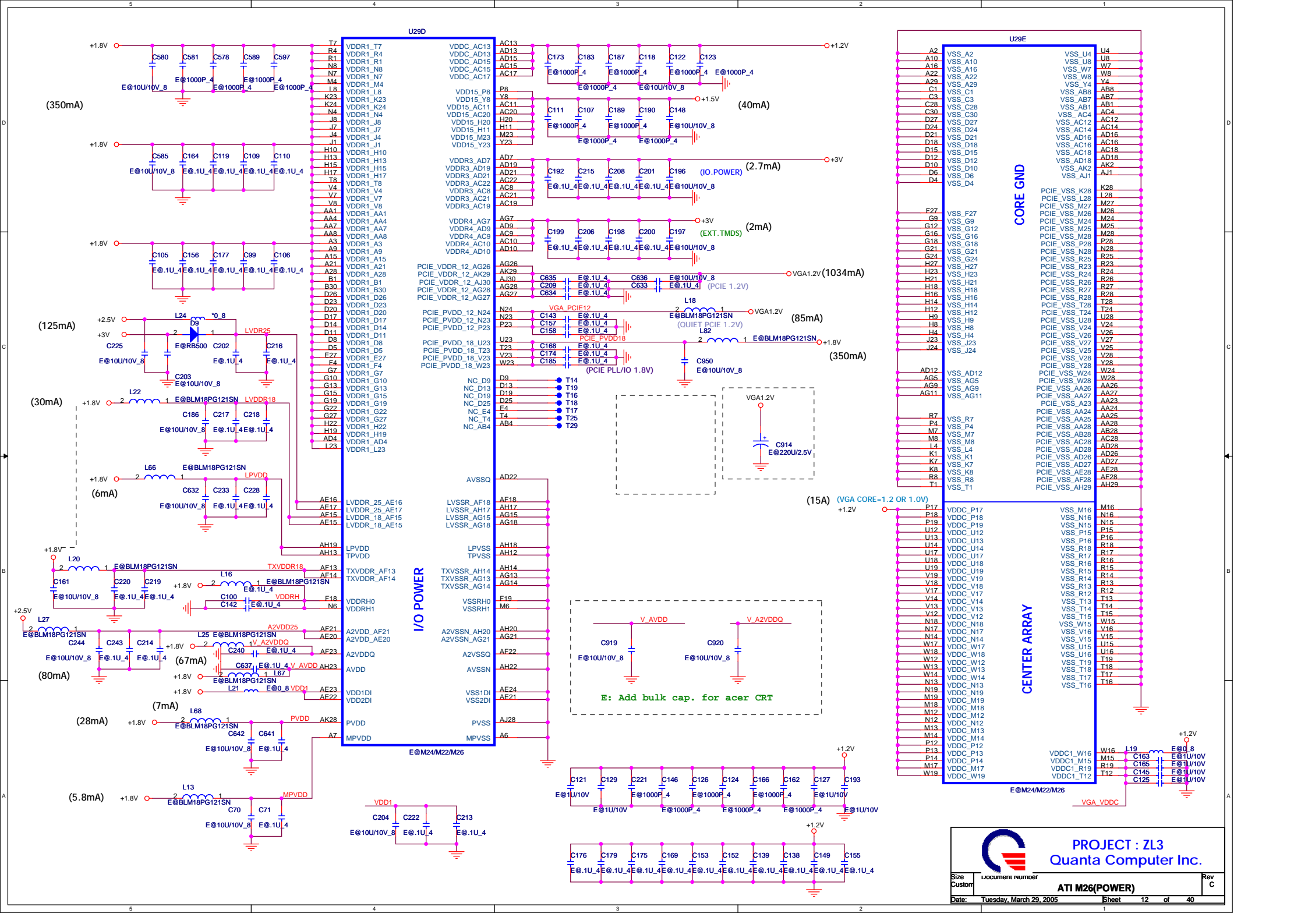


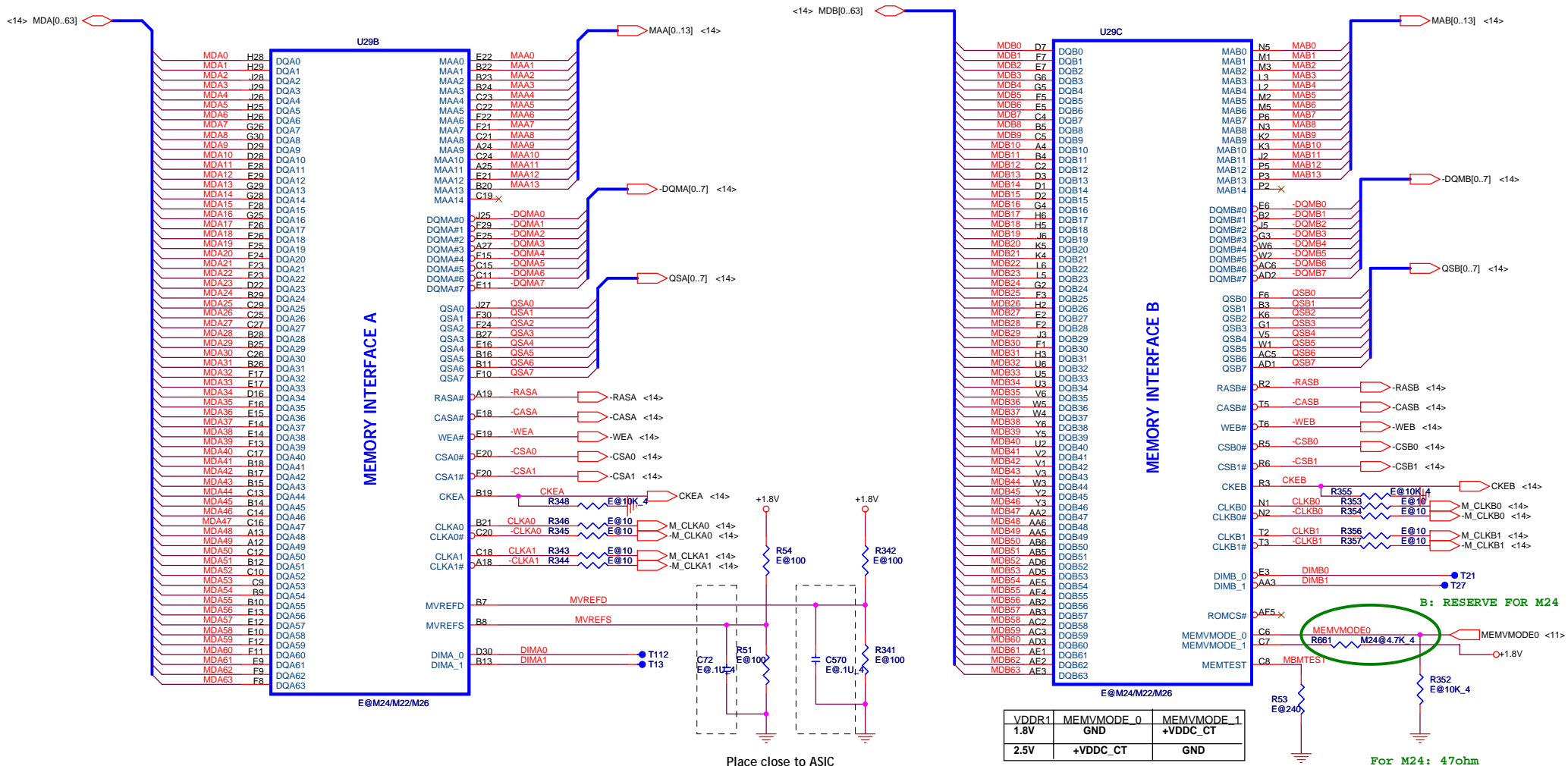
Signal	Component	Value	Notes
<6> GMCEXP_TXP[0..15]	GMCEXP_TXP0	AH30	
<6> GMCEXP_TXN[0..15]	GMCEXP_TXN0	AG30	
<6,15> GMCEXP_RXP[0..15]	GMCEXP_RXP1	AF29	
<6,15> GMCEXP_RXN[0..15]	GMCEXP_RXN1	AE29	
	GMCEXP_TXP2	AD30	
	GMCEXP_TXN2	AE30	
	GMCEXP_TXP3	AD30	
	GMCEXP_TXN3	AE30	
	GMCEXP_TXP4	AD29	
	GMCEXP_TXN4	AE29	
	GMCEXP_TXP5	AB30	
	GMCEXP_TXN5	AA30	
	GMCEXP_TXP6	AA29	
	GMCEXP_TXN6	Y29	
	GMCEXP_TXP7	W29	
	GMCEXP_TXN7	W30	
	GMCEXP_TXP8	V30	
	GMCEXP_TXN8	V29	
	GMCEXP_TXP9	U29	
	GMCEXP_TXN9	T29	
	GMCEXP_TXP10	T30	
	GMCEXP_TXN10	R30	
	GMCEXP_TXP11	P29	
	GMCEXP_TXN11	P29	
	GMCEXP_TXP12	N29	
	GMCEXP_TXN12	N30	
	GMCEXP_TXP13	M30	
	GMCEXP_TXN13	M29	
	GMCEXP_TXP14	L29	
	GMCEXP_TXN14	K29	
	GMCEXP_TXP15	K30	
	GMCEXP_TXN15	J30	

Signal	Component	Value	Notes
GMCEXP_RXP0	C231	E@1U 4 V	GMCEXP_RXP0 AF26
GMCEXP_RXN0	C234	E@1U 4 V	GMCEXP_RXN0 AE26
GMCEXP_RXP1	C227	E@1U 4 V	GMCEXP_RXP1 AC25
GMCEXP_RXN1	C224	E@1U 4 V	GMCEXP_RXN1 AB25
GMCEXP_RXP2	C211	E@1U 4 V	GMCEXP_RXP2 AC27
GMCEXP_RXN2	C205	E@1U 4 V	GMCEXP_RXN2 AB27
GMCEXP_RXP3	C212	E@1U 4 V	GMCEXP_RXP3 AC26
GMCEXP_RXN3	C207	E@1U 4 V	GMCEXP_RXN3 AC26
GMCEXP_RXP4	C194	E@1U 4 V	GMCEXP_RXP4 Y25
GMCEXP_RXN4	C188	E@1U 4 V	GMCEXP_RXN4 W25
GMCEXP_RXP5	C195	E@1U 4 V	GMCEXP_RXP5 Y27
GMCEXP_RXN5	C191	E@1U 4 V	GMCEXP_RXN5 Y26
GMCEXP_RXP6	C178	E@1U 4 V	GMCEXP_RXP6 W26
GMCEXP_RXN6	C171	E@1U 4 V	GMCEXP_RXN6 W26
GMCEXP_RXP7	C160	E@1U 4 V	GMCEXP_RXP7 U25
GMCEXP_RXN7	C154	E@1U 4 V	GMCEXP_RXN7 T25
GMCEXP_RXP8	C159	E@1U 4 V	GMCEXP_RXP8 U26
GMCEXP_RXN8	C151	E@1U 4 V	GMCEXP_RXN8 T27
GMCEXP_RXP9	C182	E@1U 4 V	GMCEXP_RXP9 U26
GMCEXP_RXN9	C172	E@1U 4 V	GMCEXP_RXN9 T26
GMCEXP_RXP10	C140	E@1U 4 V	GMCEXP_RXP10 P25
GMCEXP_RXN10	C131	E@1U 4 V	GMCEXP_RXN10 N25
GMCEXP_RXP11	C141	E@1U 4 V	GMCEXP_RXP11 P27
GMCEXP_RXN11	C135	E@1U 4 V	GMCEXP_RXN11 N27
GMCEXP_RXP12	C116	E@1U 4 V	GMCEXP_RXP12 P26
GMCEXP_RXN12	C112	E@1U 4 V	GMCEXP_RXN12 N26
GMCEXP_RXP13	C117	E@1U 4 V	GMCEXP_RXP13 P25
GMCEXP_RXN13	C113	E@1U 4 V	GMCEXP_RXN13 K25
GMCEXP_RXP14	C96	E@1U 4 V	GMCEXP_RXP14 L27
GMCEXP_RXN14	C94	E@1U 4 V	GMCEXP_RXN14 K27
GMCEXP_RXP15	C98	E@1U 4 V	GMCEXP_RXP15 L26
GMCEXP_RXN15	C95	E@1U 4 V	GMCEXP_RXN15 K26



Signal	Component	Value	Notes
GPIO0	AJ5	R369	E@10K_4
GPIO1	AH5	R367	E@10K_4
GPIO2	AJ4	T148	
GPIO3	AH4	T143	
GPIO4	AJ4	T141	
GPIO5	AH4	T33	
GPIO6	AJ3	T130	
GPIO7	AH3	T136	
GPIO8	AJ2	T127	
GPIO9	AH2	T129	
GPIO10	AJ2	T132	
GPIO11	AH1	T37	
GPIO12	AJ1	T123	
GPIO13	AH1	T125	
GPIO14	AJ1	T126	
GPIO15	AH1	T128	
GPIO16	AJ1	T129	
GPIO17	AH1	T130	
GPIO18	AJ1	T131	
GPIO19	AH1	T132	
GPIO20	AJ1	T133	
GPIO21	AH1	T134	
GPIO22	AJ1	T135	
GPIO23	AH1	T136	
GPIO24	AJ1	T137	
GPIO25	AH1	T138	
GPIO26	AJ1	T139	
GPIO27	AH1	T140	
GPIO28	AJ1	T141	
GPIO29	AH1	T142	
GPIO30	AJ1	T143	
GPIO31	AH1	T144	
GPIO32	AJ1	T145	
GPIO33	AH1	T146	
GPIO34	AJ1	T147	
GPIO35	AH1	T148	
GPIO36	AJ1	T149	
GPIO37	AH1	T150	
GPIO38	AJ1	T151	
GPIO39	AH1	T152	
GPIO40	AJ1	T153	
GPIO41	AH1	T154	
GPIO42	AJ1	T155	
GPIO43	AH1	T156	
GPIO44	AJ1	T157	
GPIO45	AH1	T158	
GPIO46	AJ1	T159	
GPIO47	AH1	T160	
GPIO48	AJ1	T161	
GPIO49	AH1	T162	

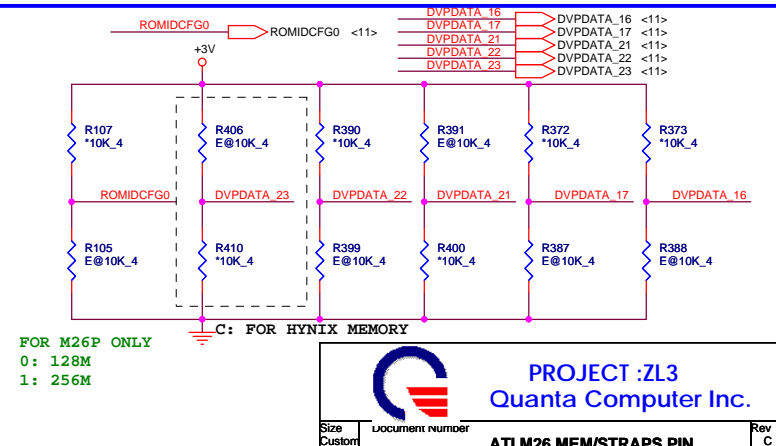




GPIO_0	PCI-Express Current Calibration Bandgap Backup 0: use reference voltage from Bandgap 1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable 0: Disable PLL force calibration 1: Enable PLL force calibration
GPIO_(3,2)	00: PCI Express 1.0 mode 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration 0: enable 1: disable
GPIO_5	Bypass PCI-Express PLL

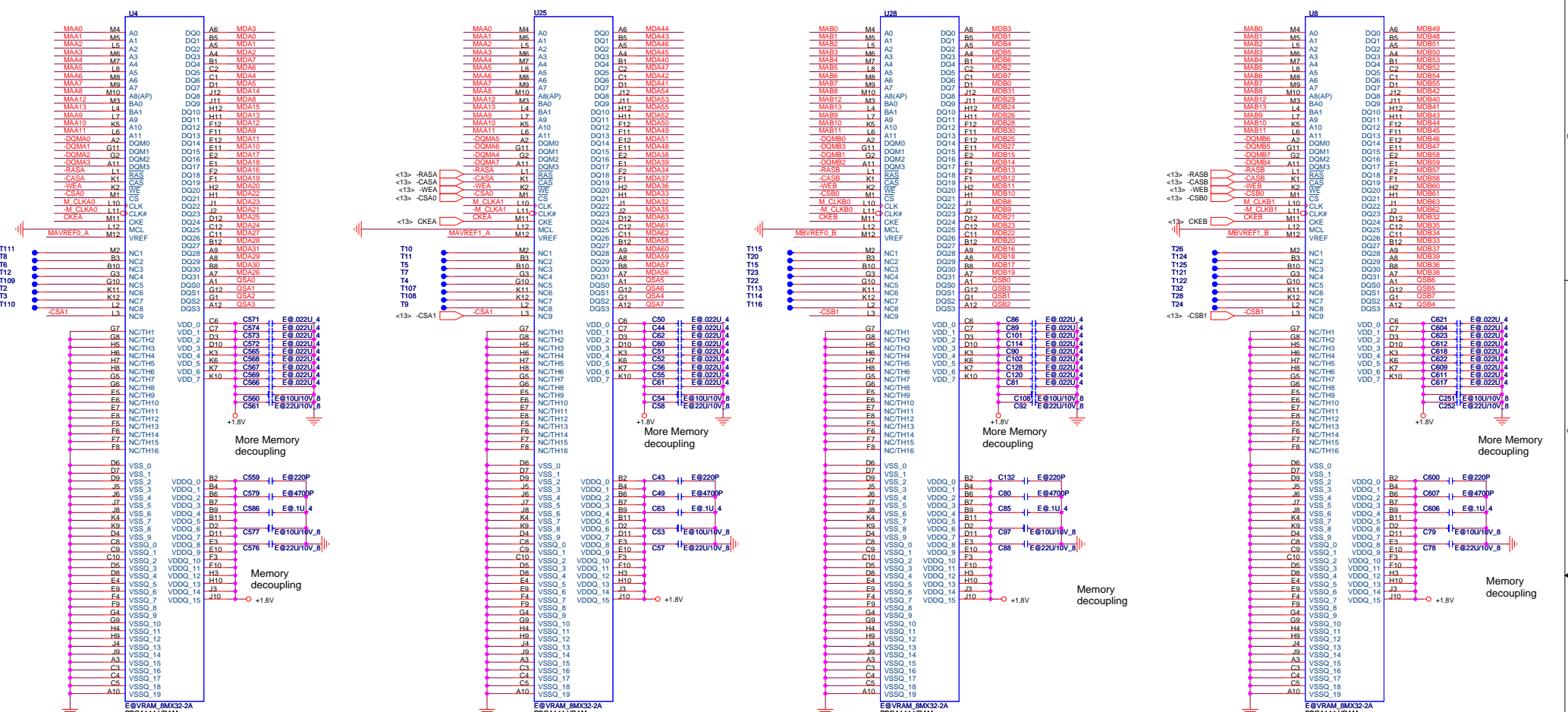
### STRAPS PIN

GPIO_6	PCI-Express transmitter current compensation 0: Normal 1: Inject extra current for output buffer switching
GPIO_8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible
GPIO(9,13:11) INT P/D	ROMIDCFG 0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23 MEM TYPE	DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung

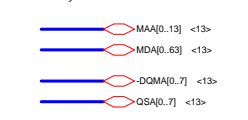


**PROJECT :ZL3**  
Quanta Computer Inc.

Size Custom	Document number	<b>ATI M26 MEM/STRAPS PIN</b>	Rev C
Date: Tuesday, March 29, 2005	Sheet 13	of 40	



**VGA DDR MEMORY A**  
 @64/128MBytes DDR 128Mbit 1MX32X4 uBGA

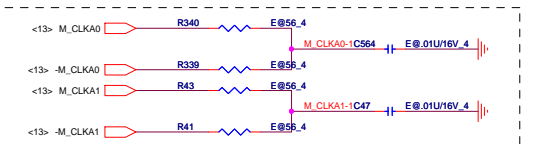


Place close to memory

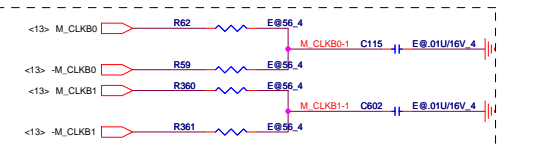
8Mx32 AKD56WC0T503 K4D553230F-GC33 1.8V  
 4Mx32 AKD35W-T506 K4D263238E-GC33 2.5V



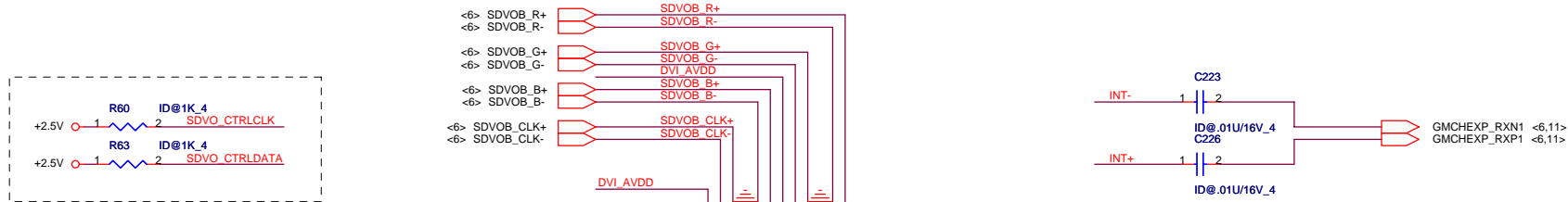
Place close to memory



At least a 2.5:1 spacing between the pair  
 These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

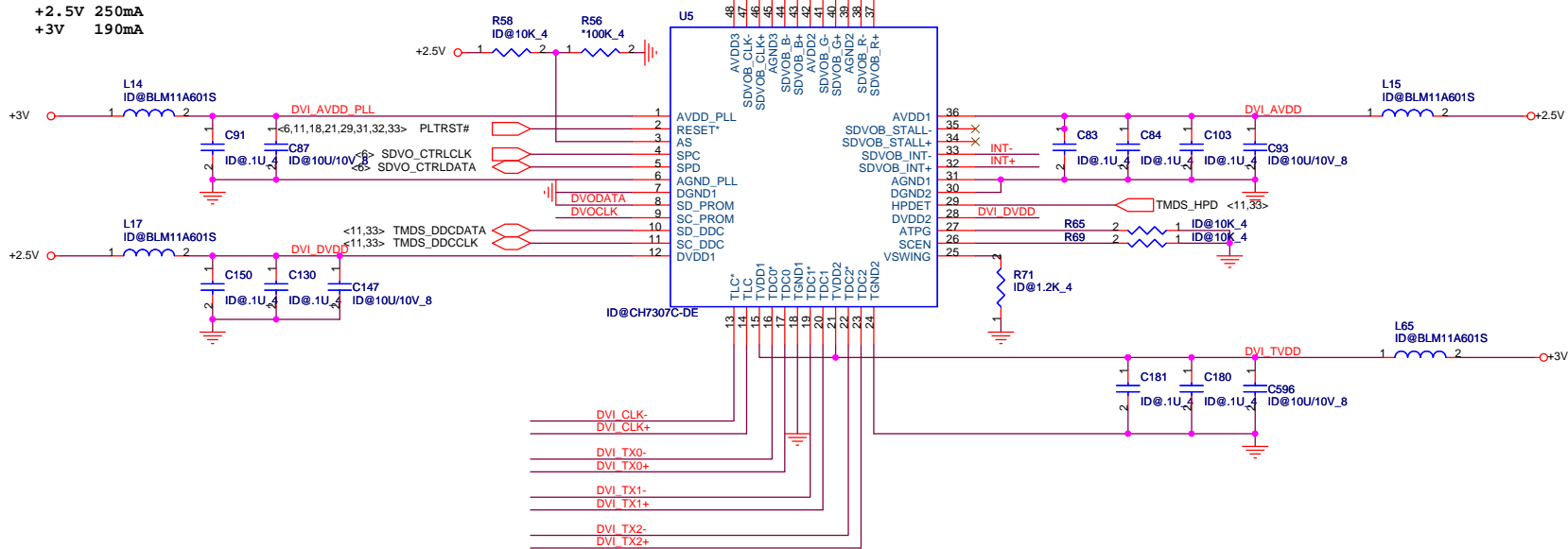


At least a 2.5:1 spacing between the pair  
 These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

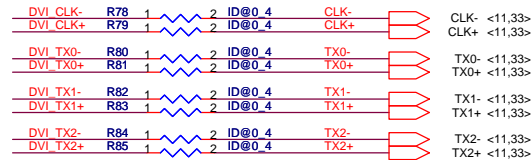
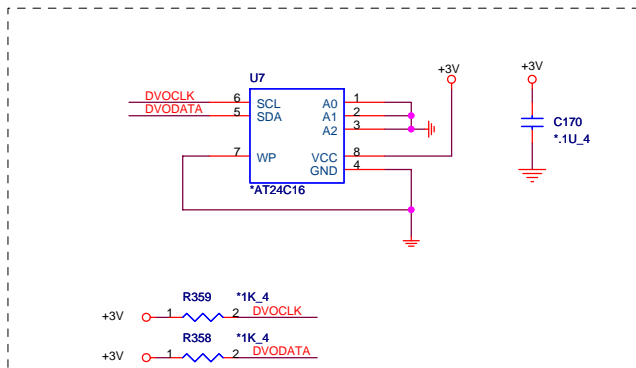


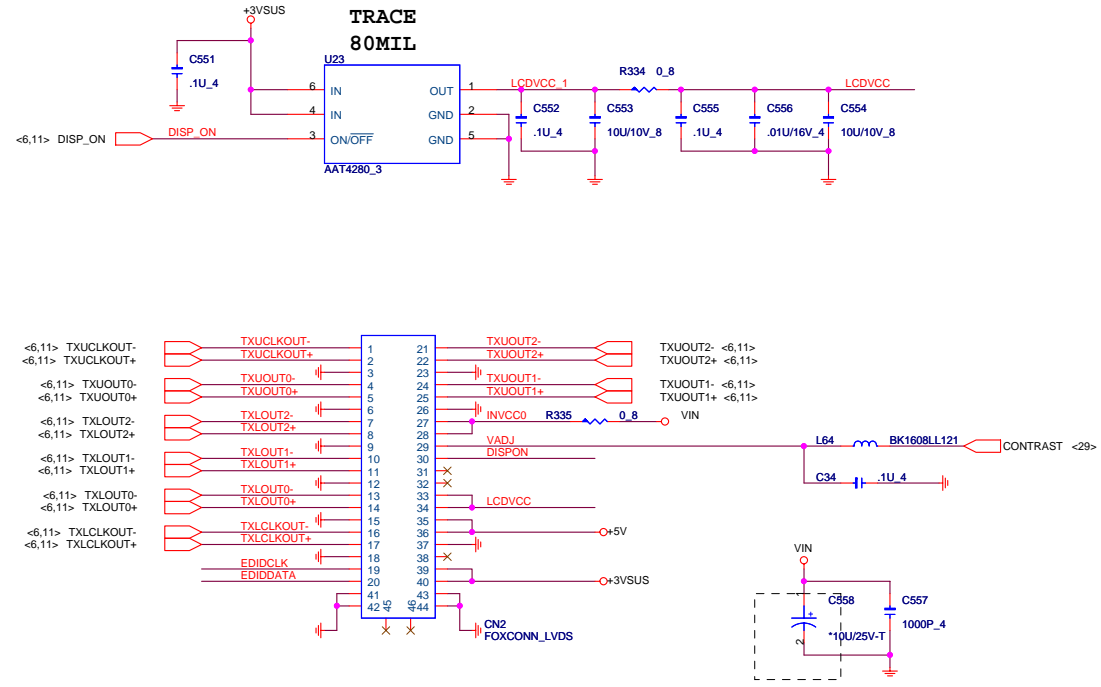
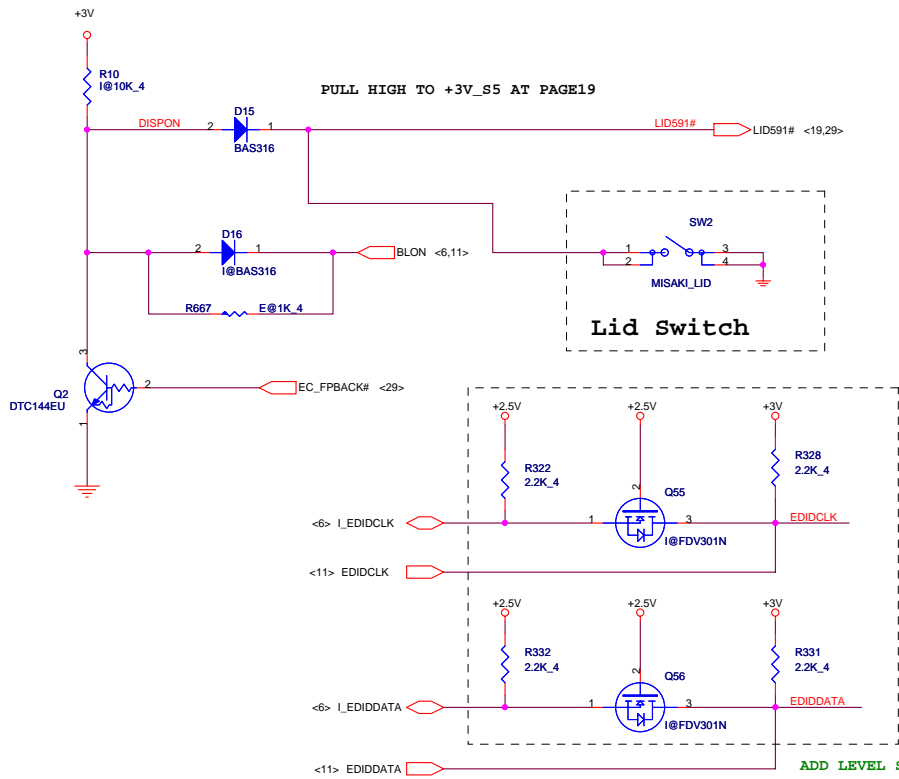
PULL LOW FOR DVO NOT PRESENT (INTERNAL PULLLOW IN 915GM)

+2.5V 250mA  
+3V 1.90mA

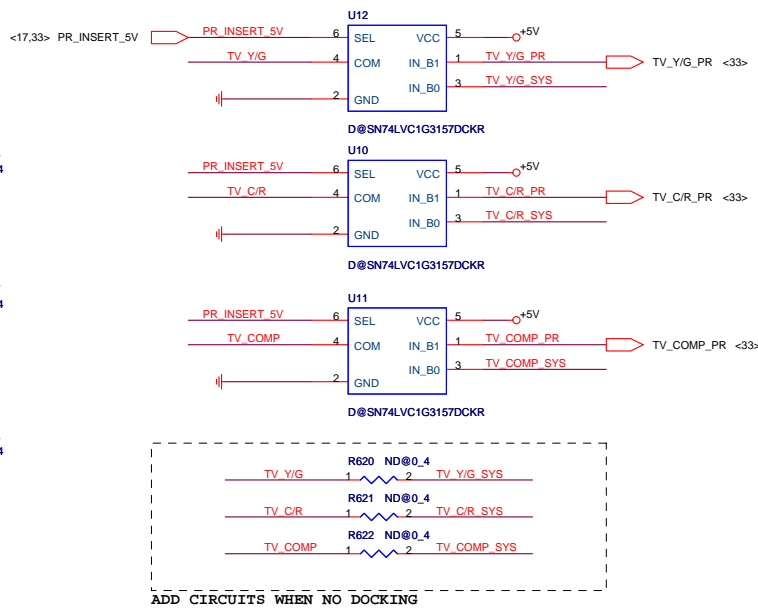


ALWAYS NOT ON, TEST ONLY

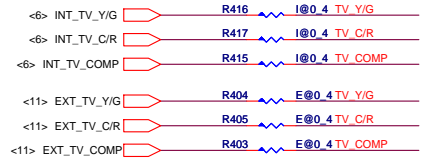
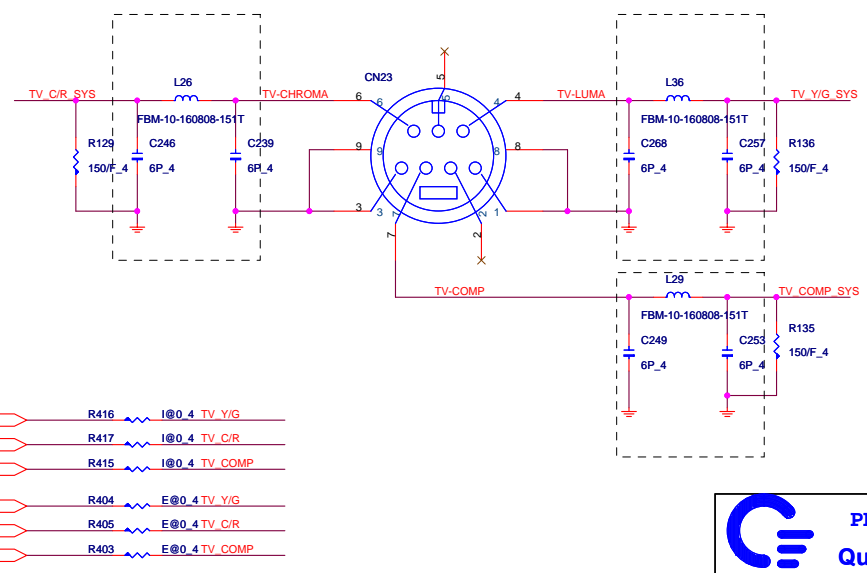




ADD LEVEL SHIFT FOR EDID  
 C: Change to FDV301 for Vgs issue



S-VIDEO

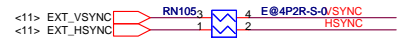
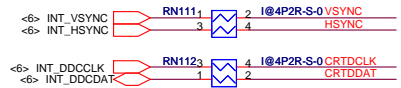


**PROJECT : ZL3**  
**Quanta Computer Inc.**

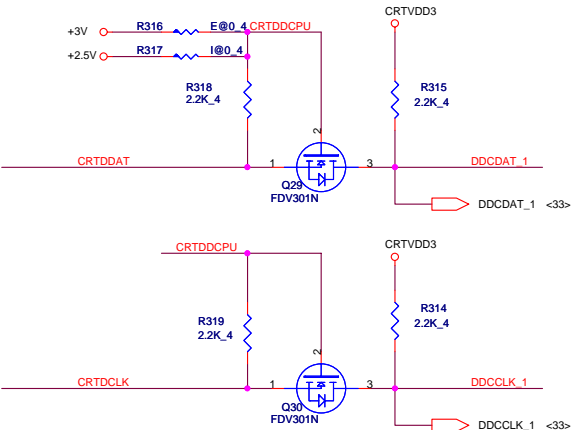
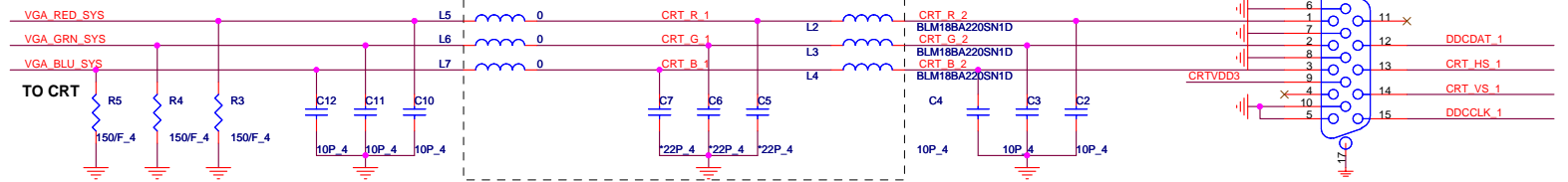
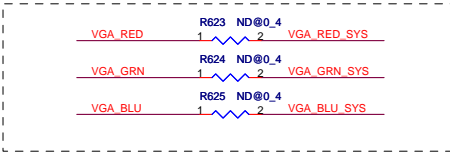
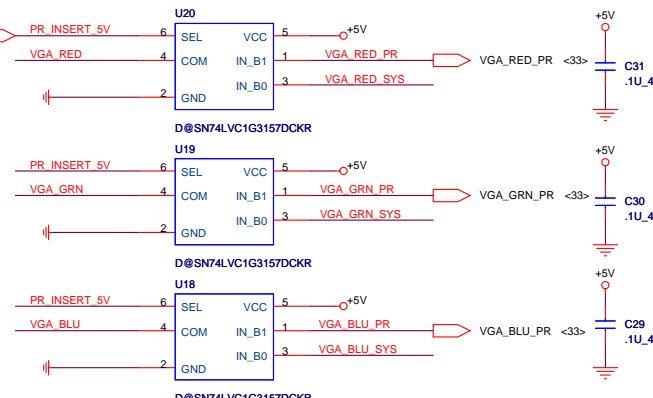
Size: Document Number  
**DVO CH7011A & RJ45-11 CON** Rev C

Date: Friday, April 15, 2005 Sheet 16 of 40

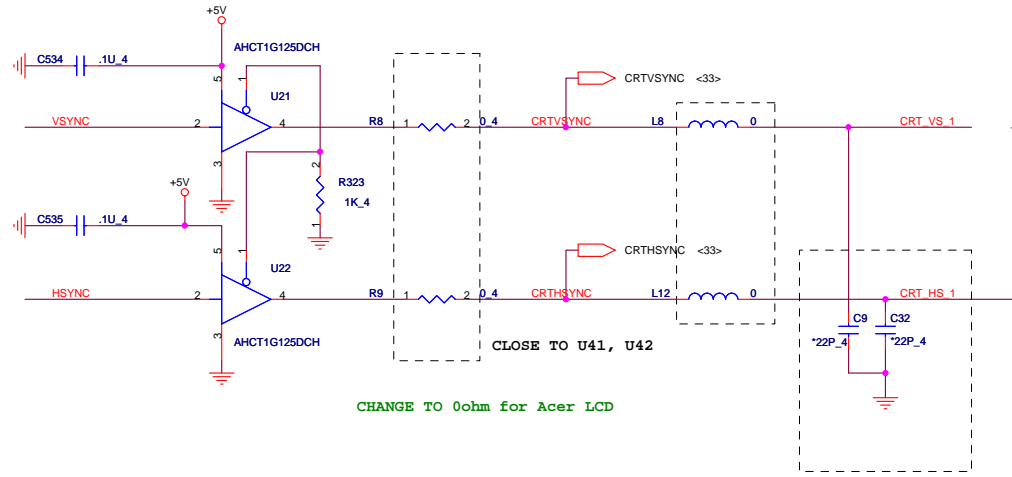
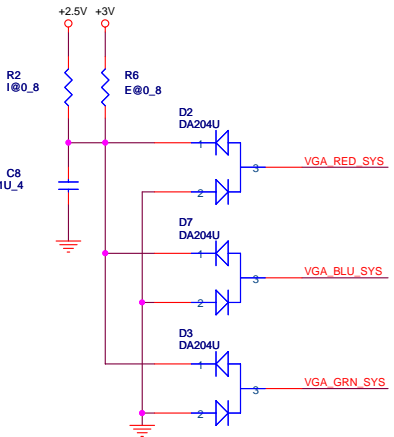




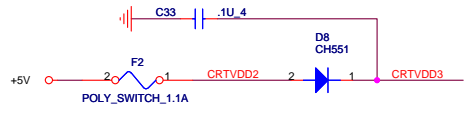
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



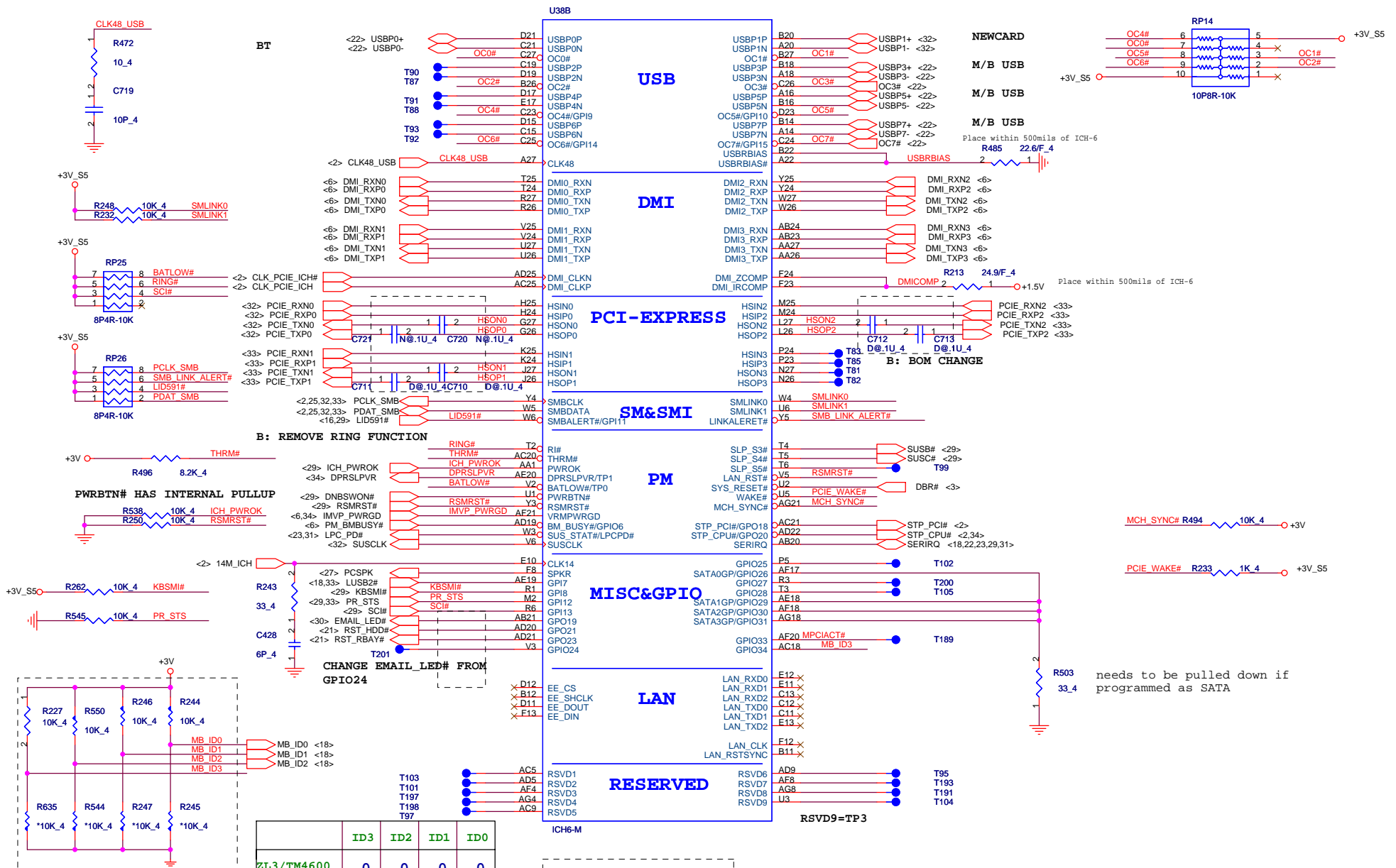
C: Change to FDV301N for Vgs issue.



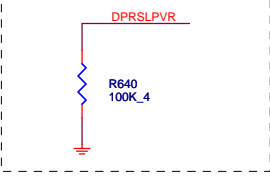
CHANGE TO 0ohm for Acer LCD







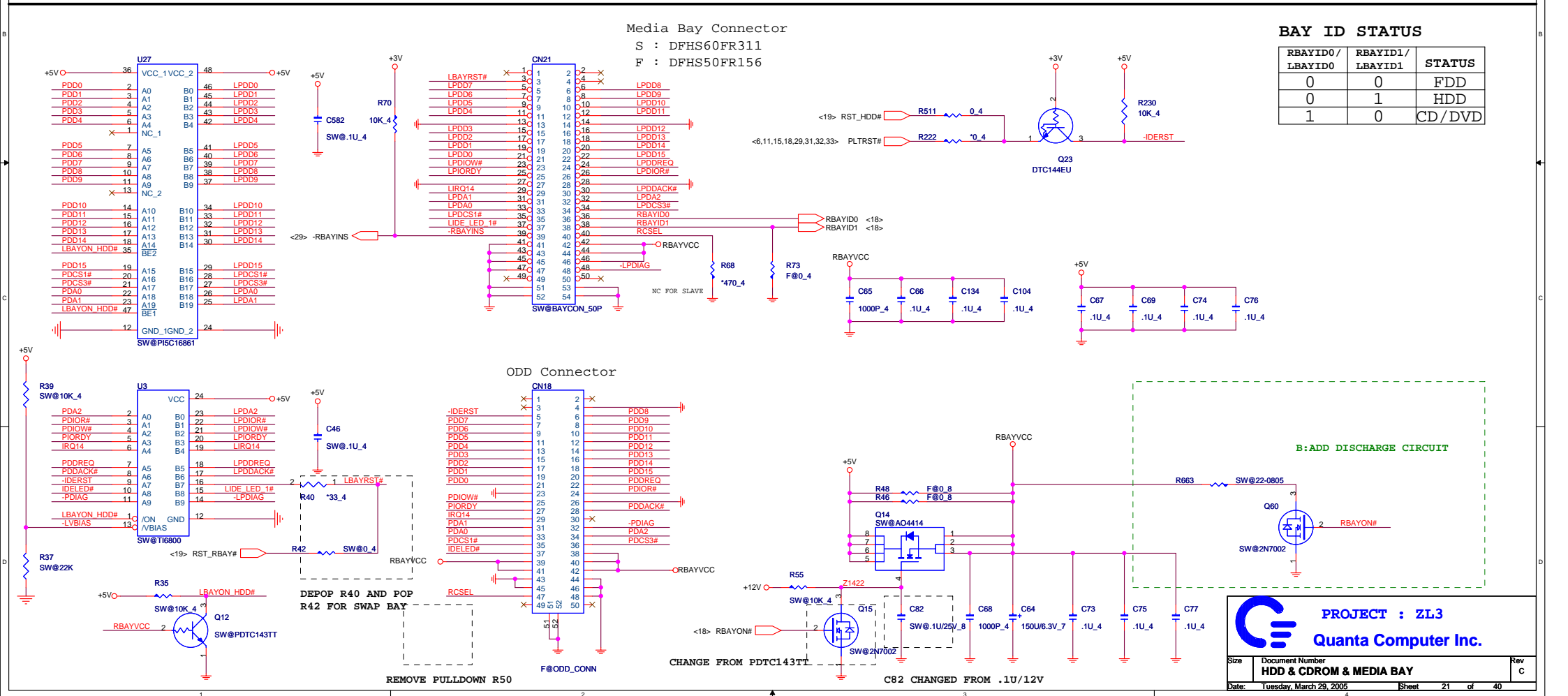
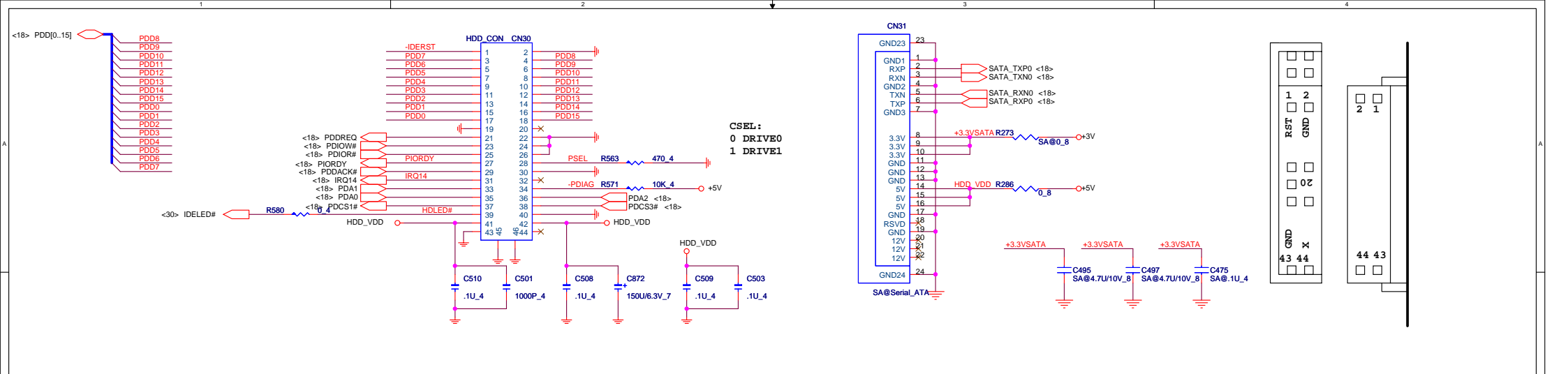
	ID3	ID2	ID1	ID0
ZL3/TM4600	0	0	0	0
ZL3B/TM4100	0	0	1	0
ZL3D/AS1690	0	1	0	0
ZL3F/AS3510	0	1	1	0
ZL3C/EX4100	1	0	1	1



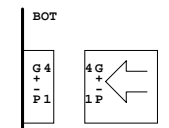
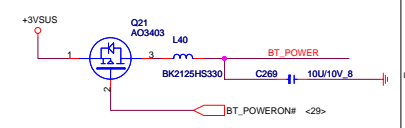
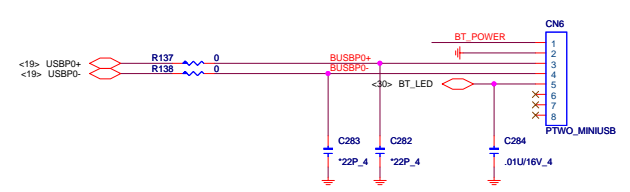
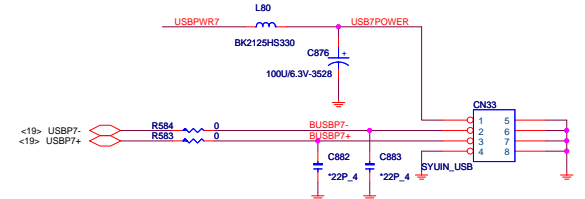
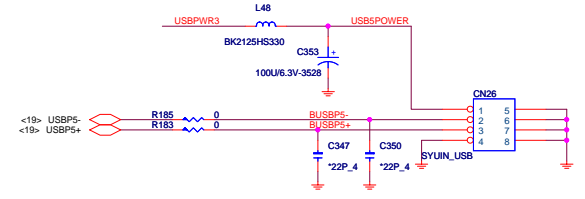
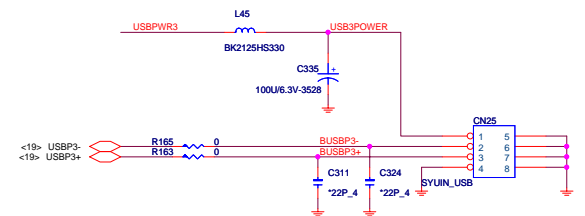
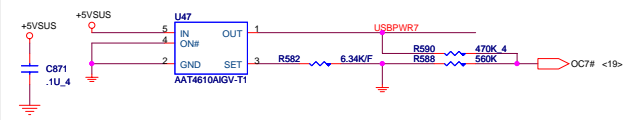
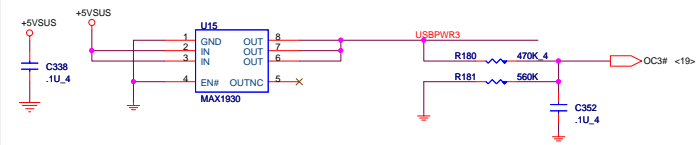
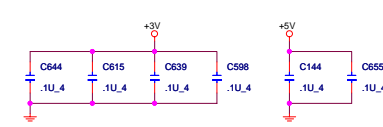
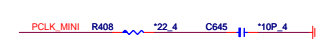
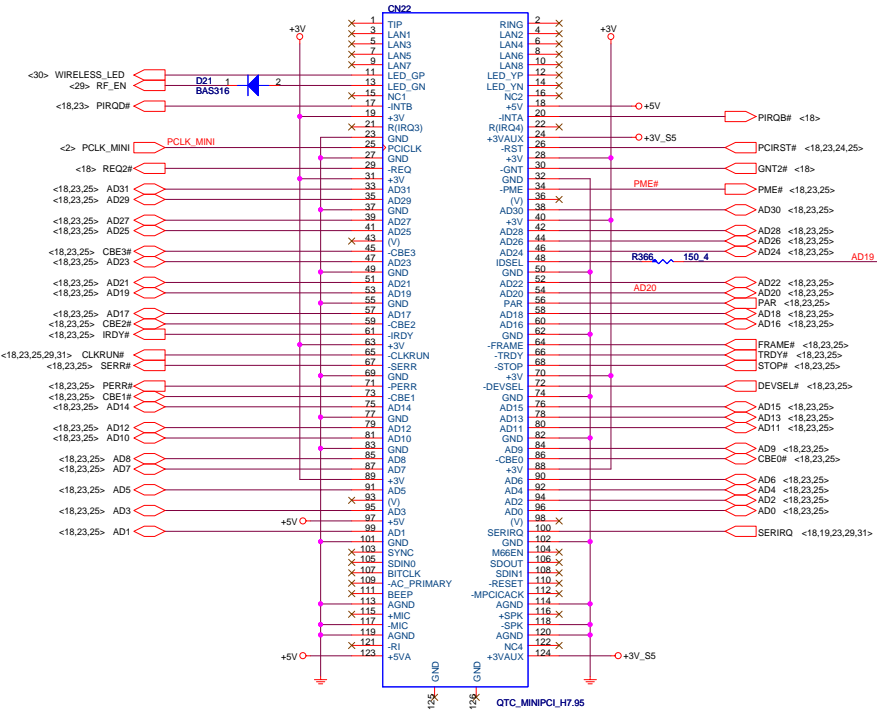
ADD PULLUP

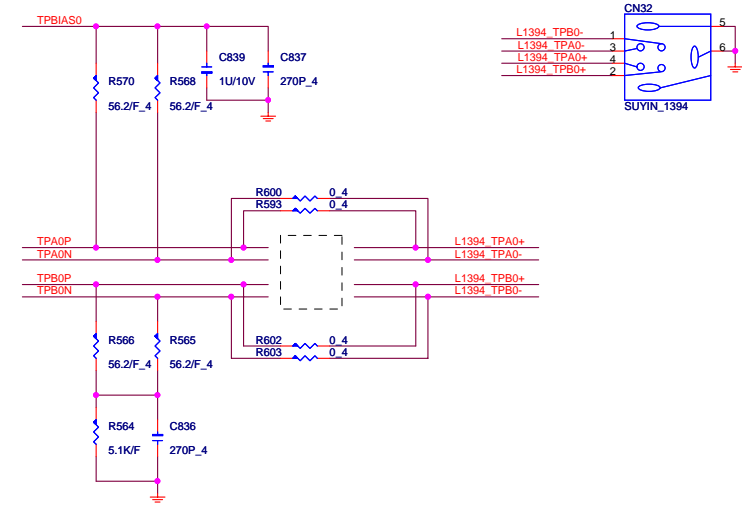
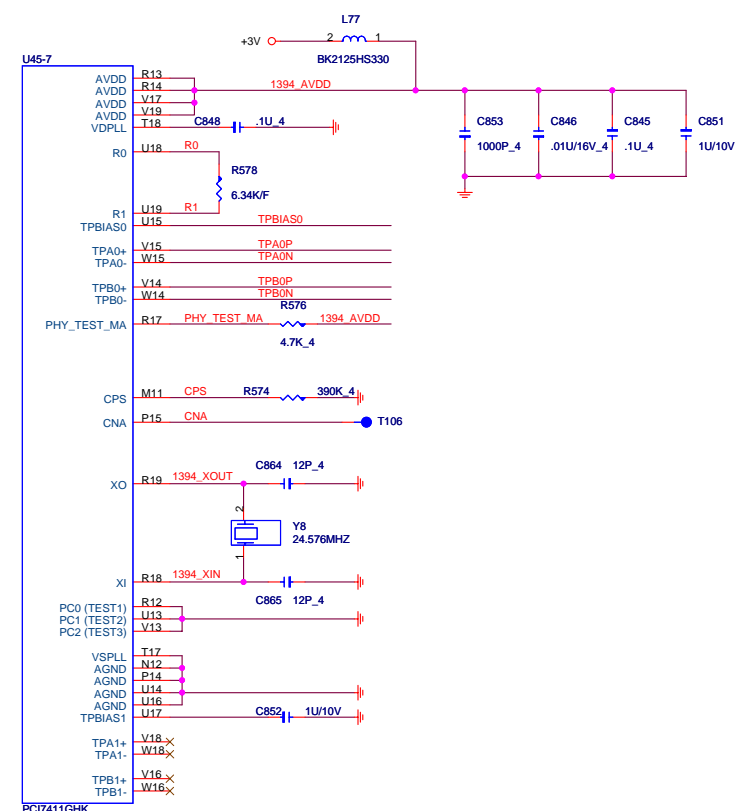
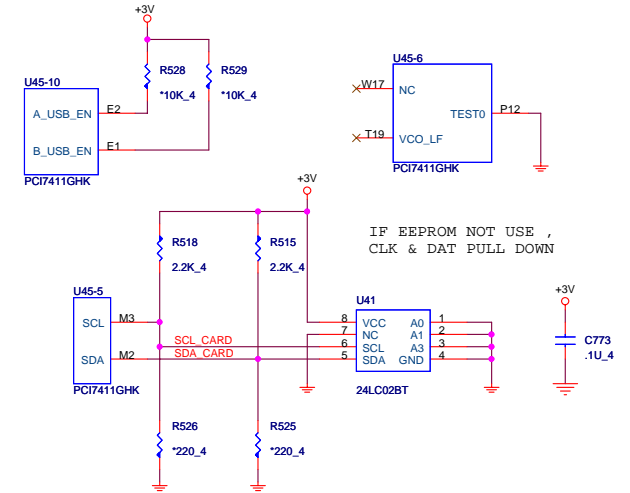
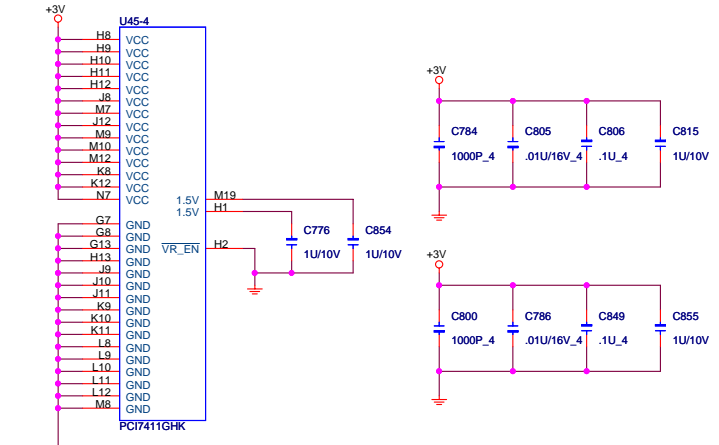
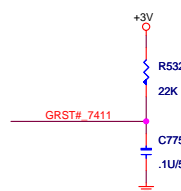
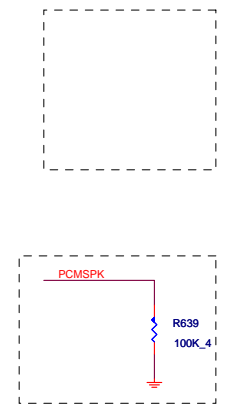
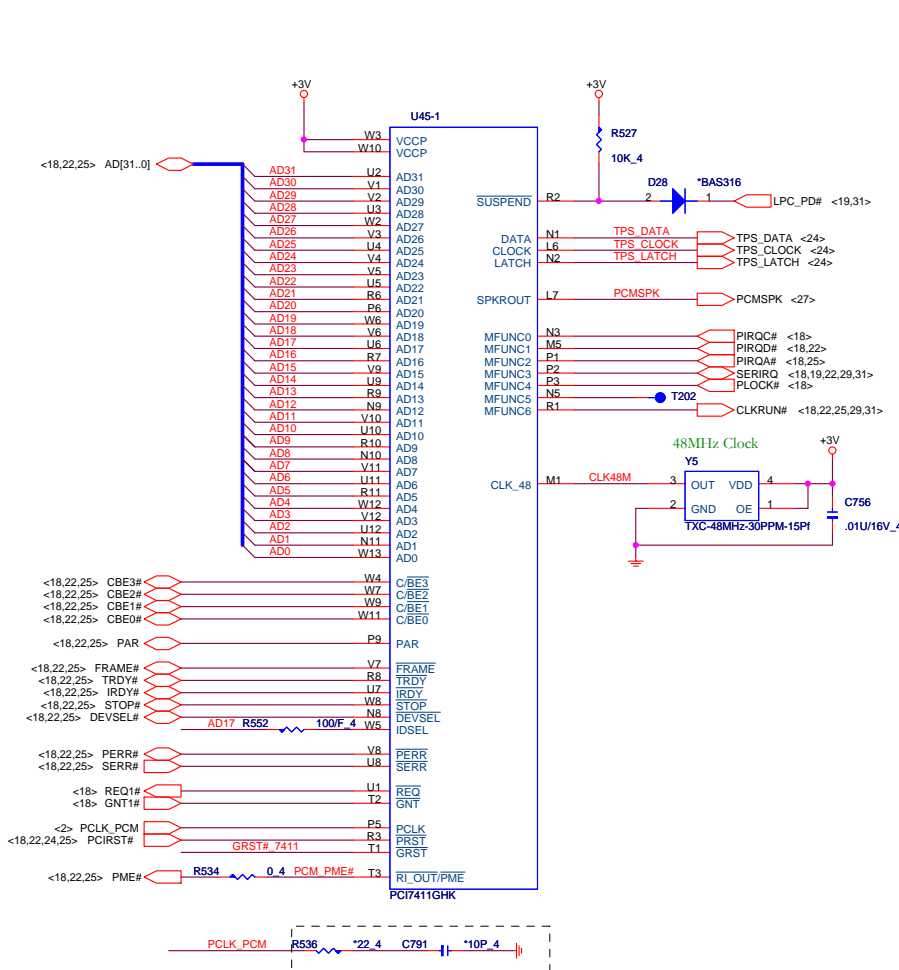


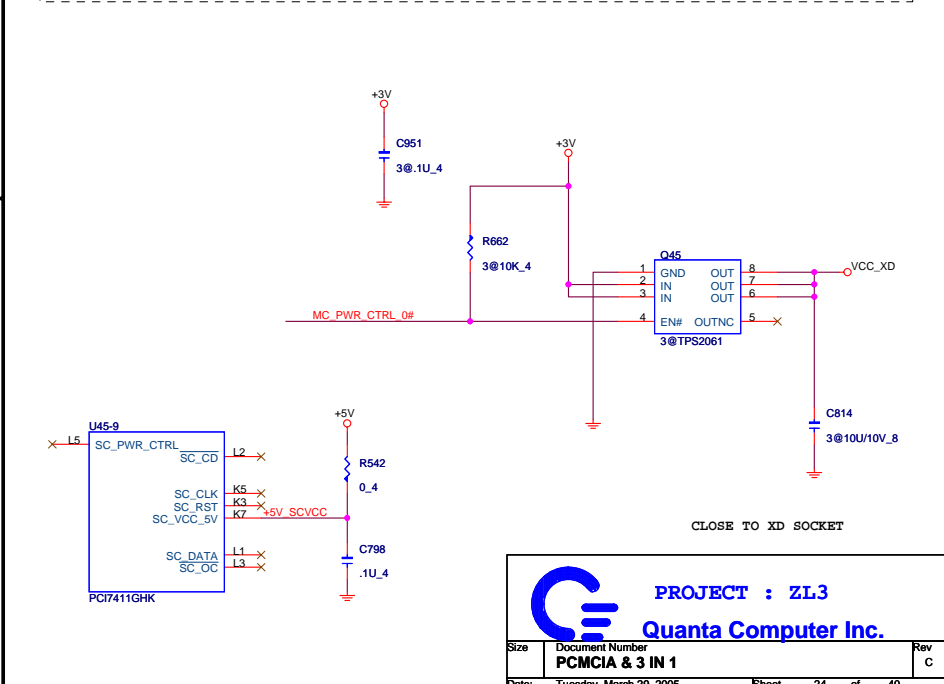
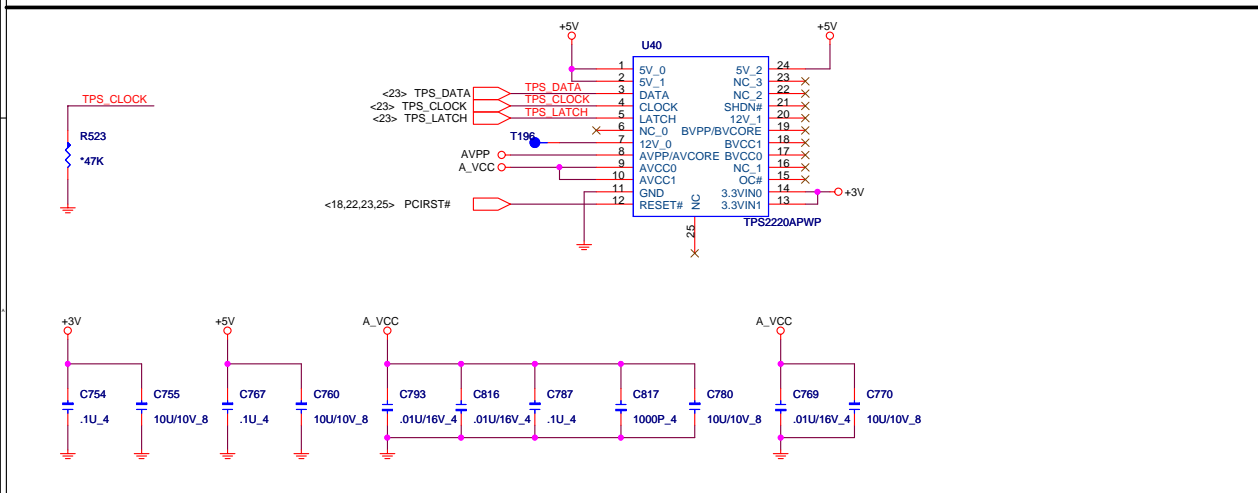
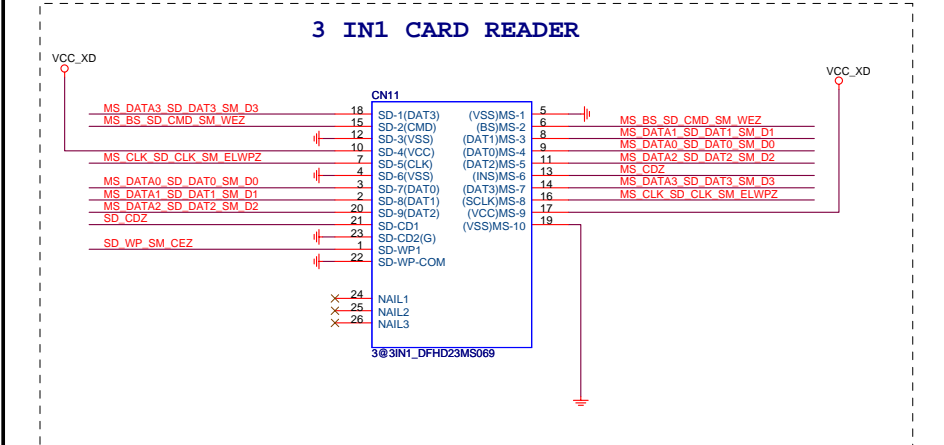
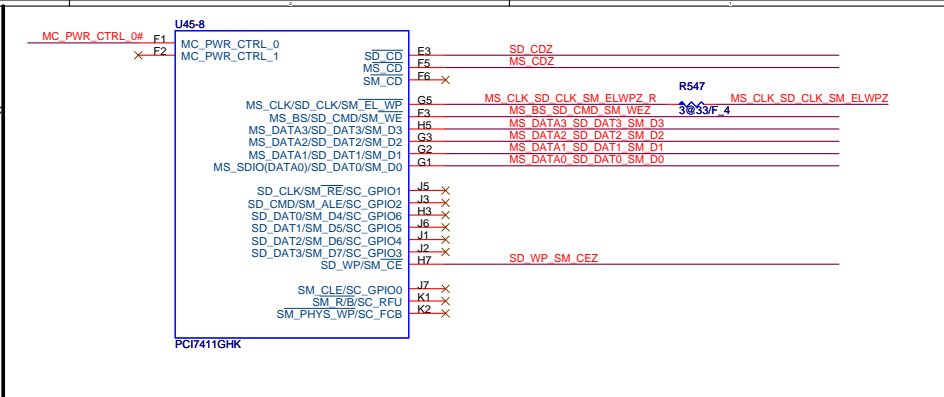
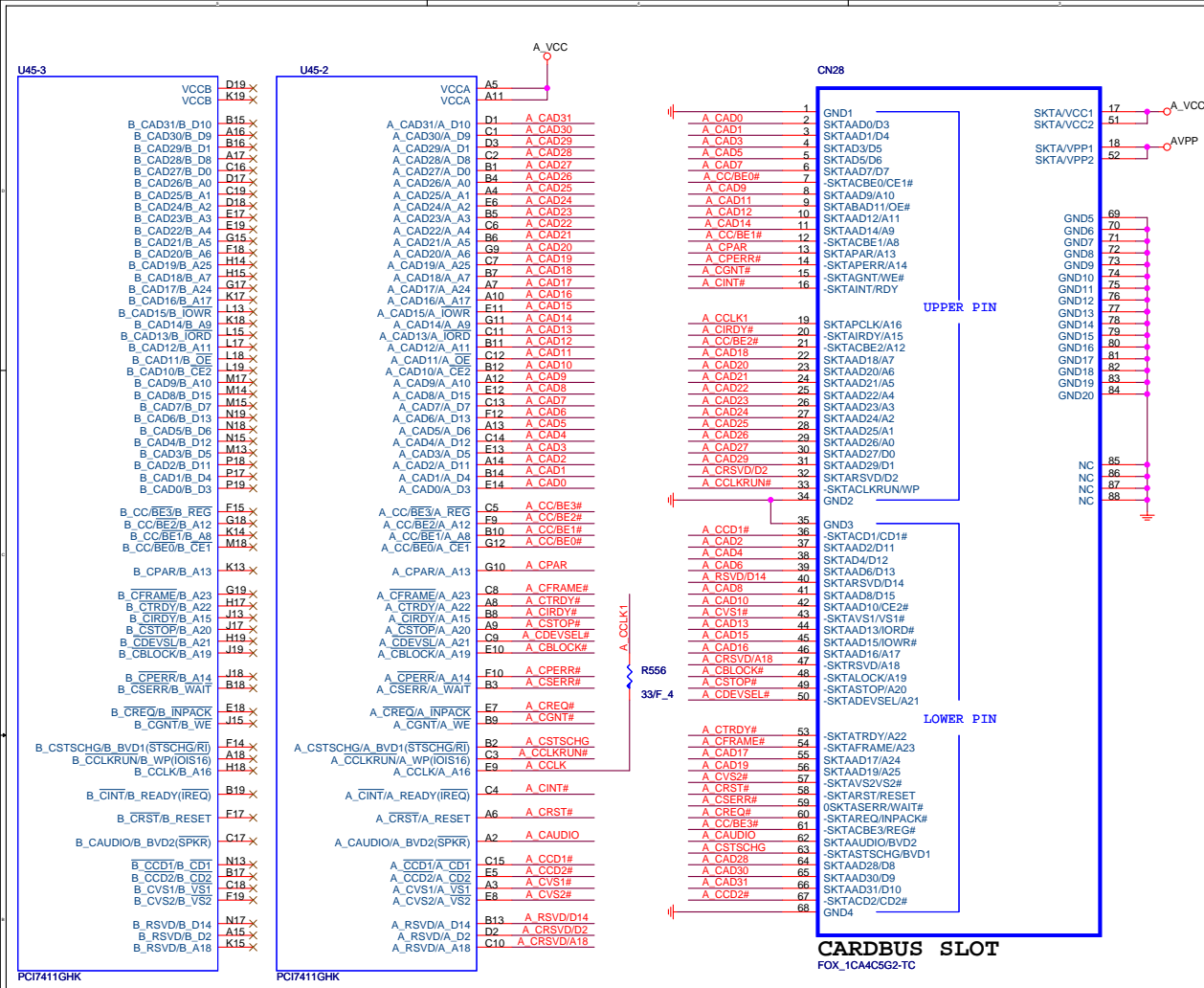




MINI-PCI

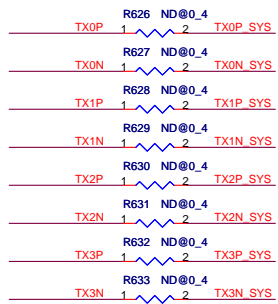
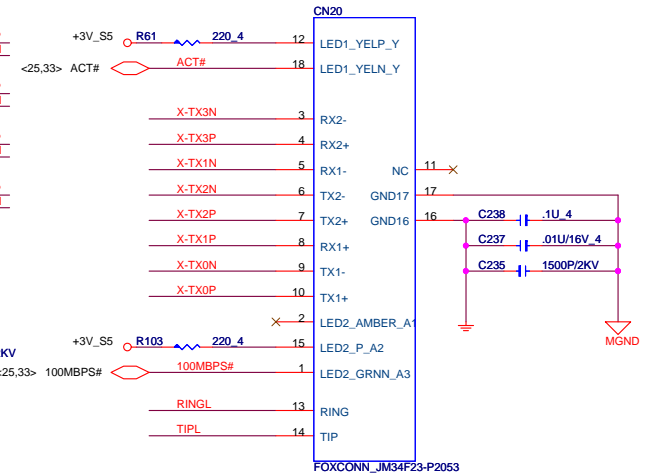
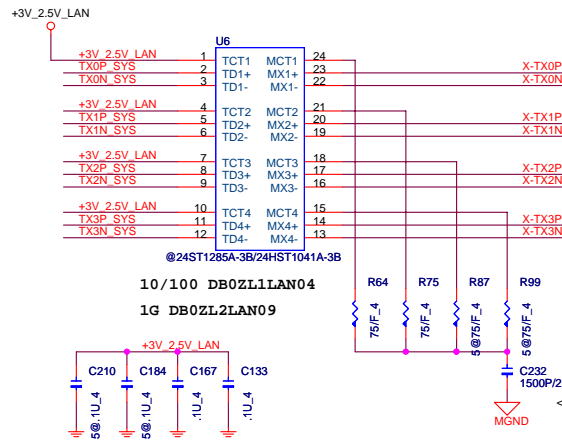
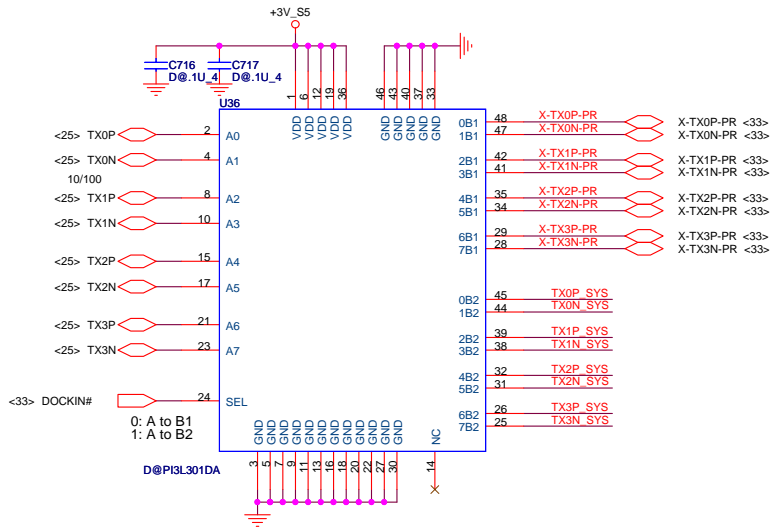




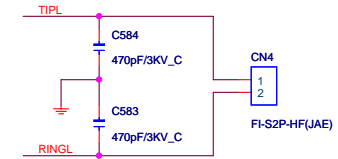




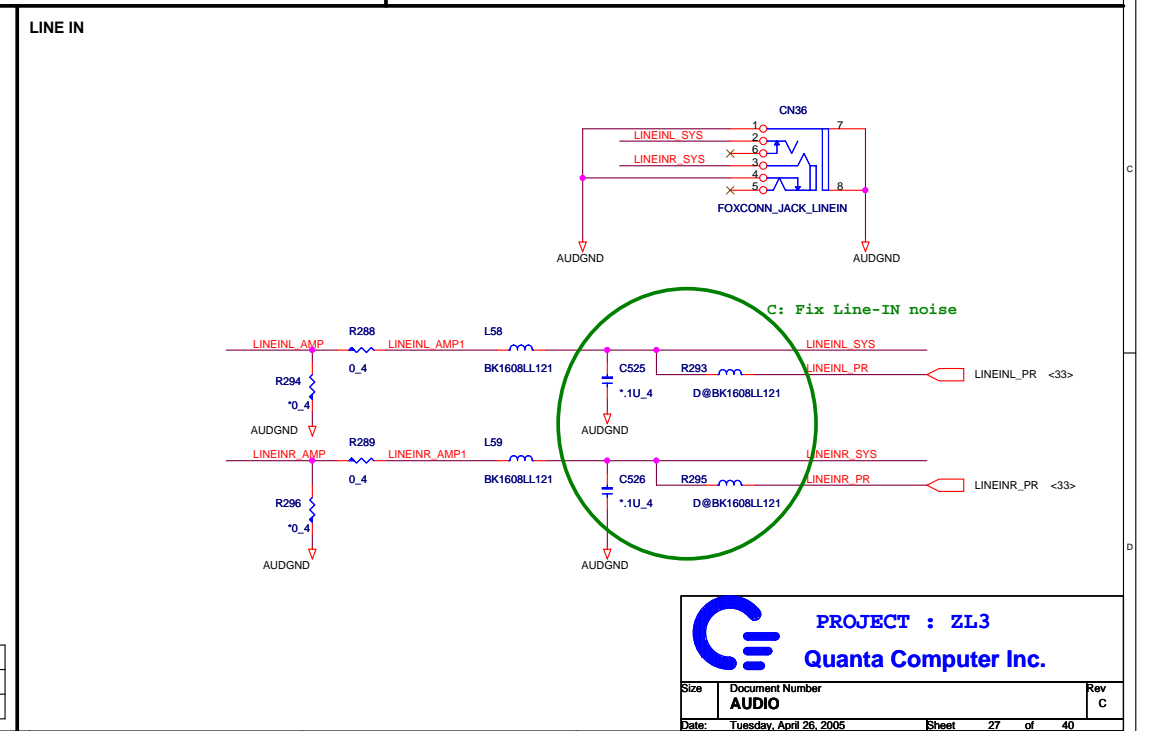
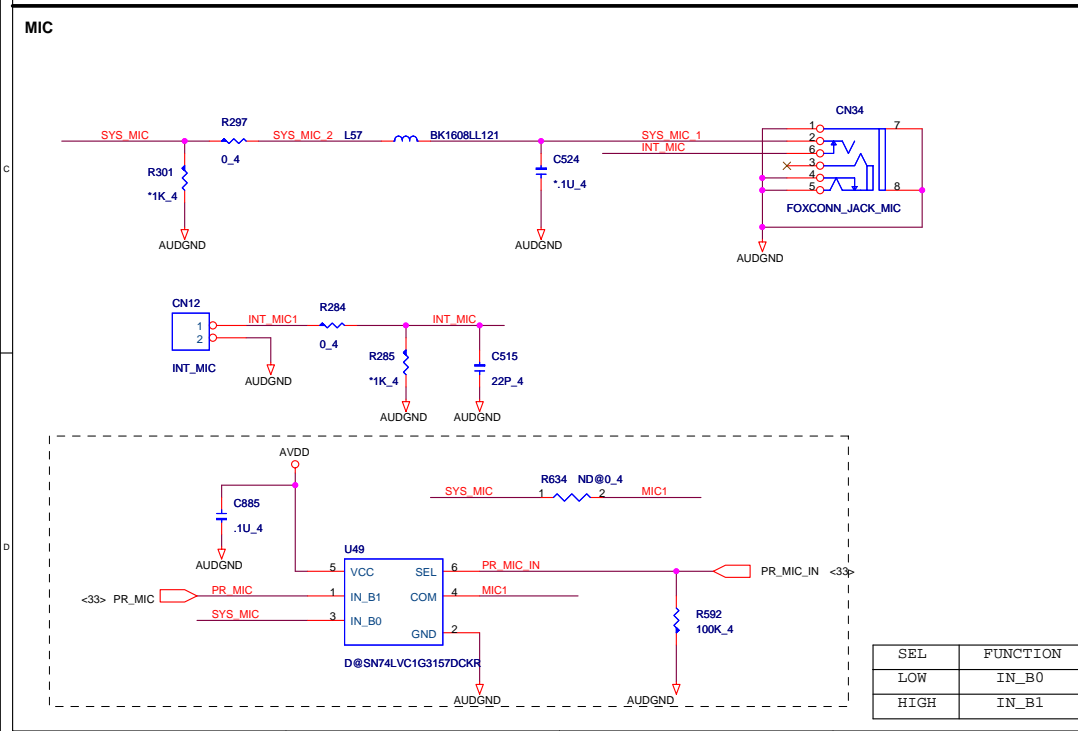
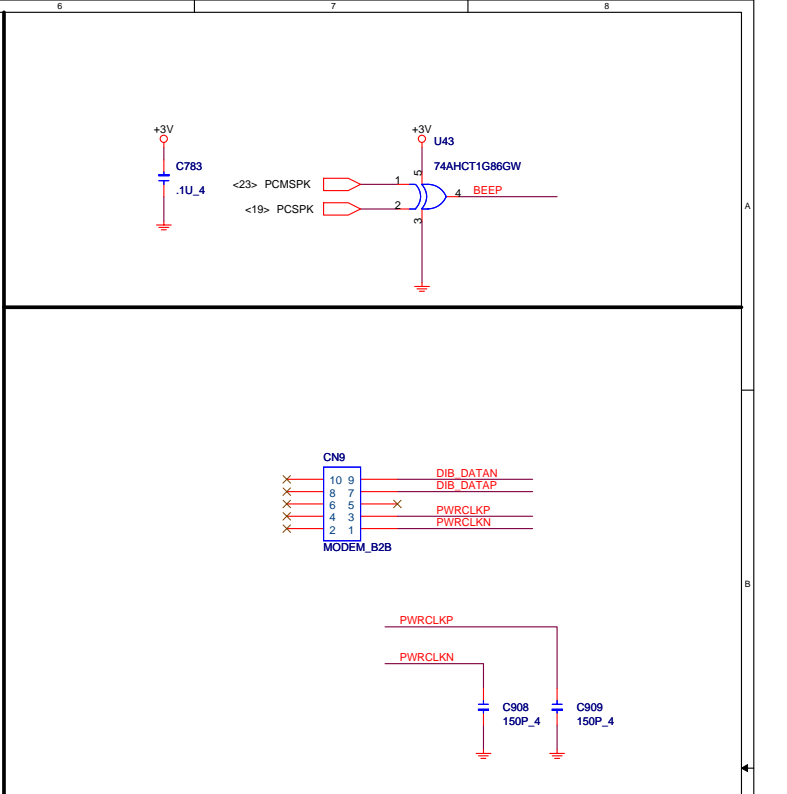
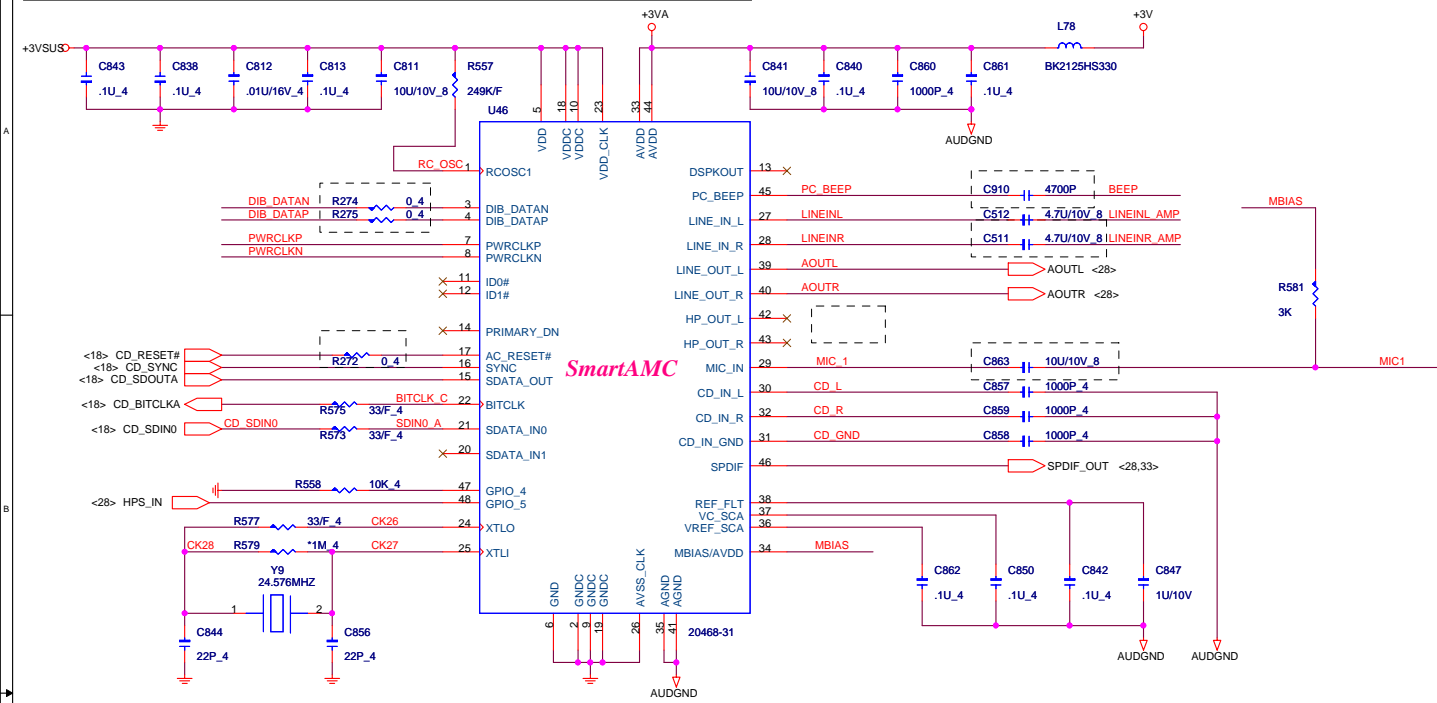




ADD CIRCUITS WHEN NO DOCKING



The AMC20463-004 modem is used for mother board family MBAMC20463-004.



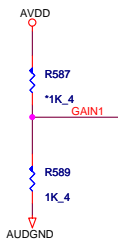
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

**PROJECT : ZL3**  
**Quanta Computer Inc.**

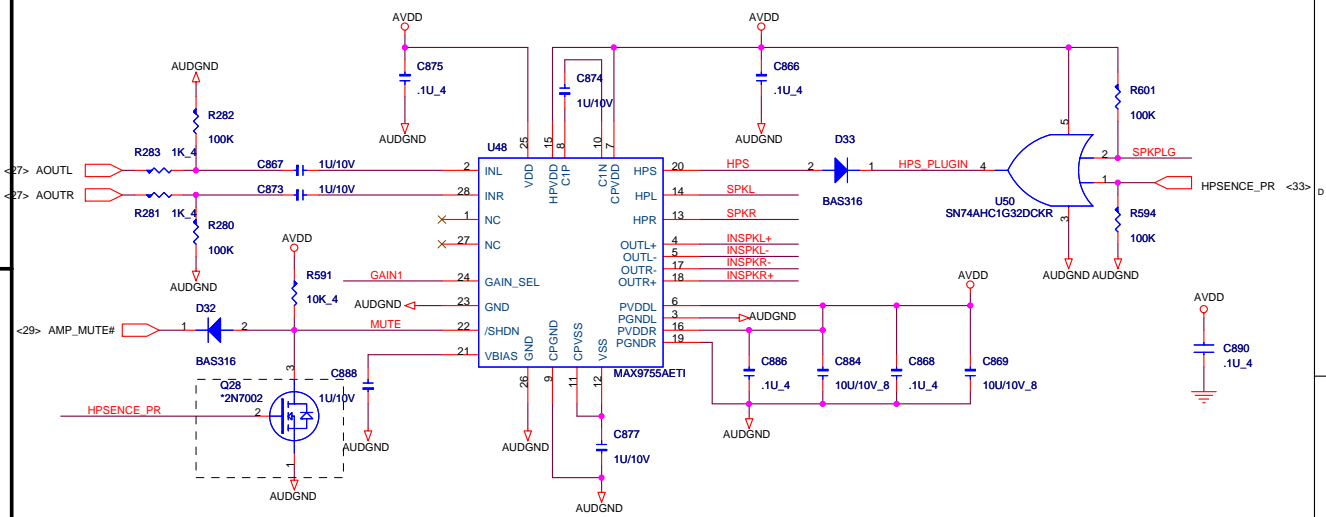
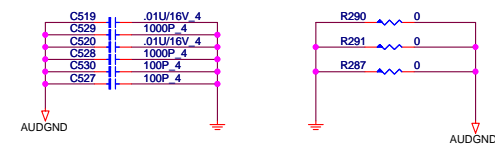
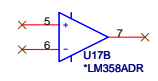
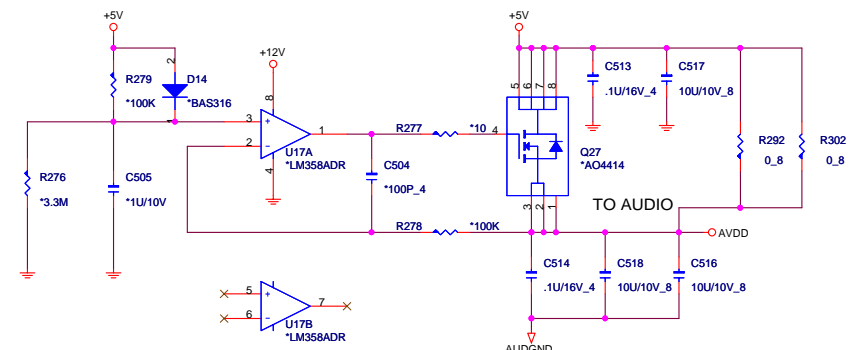
Size: Document Number  
**AUDIO**

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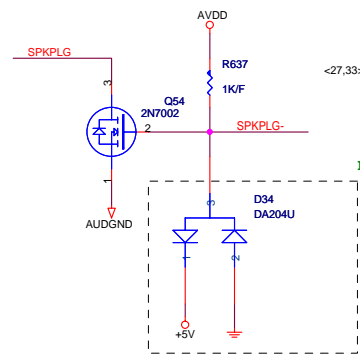
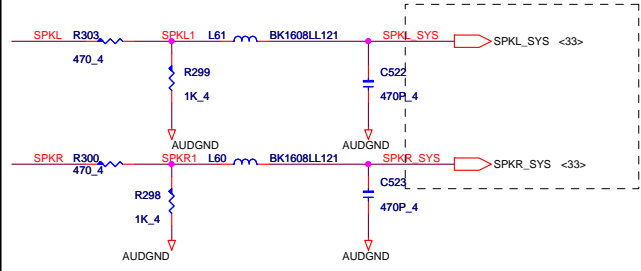
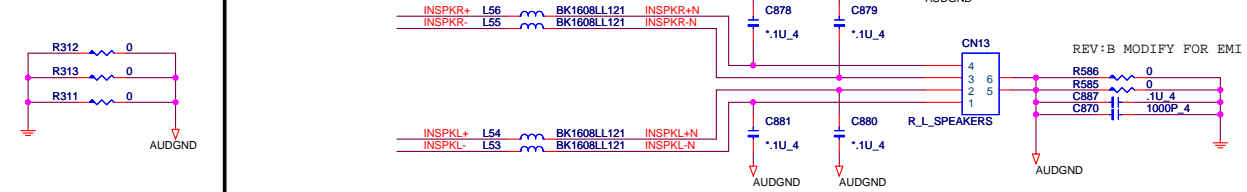
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



**AMP POWER**

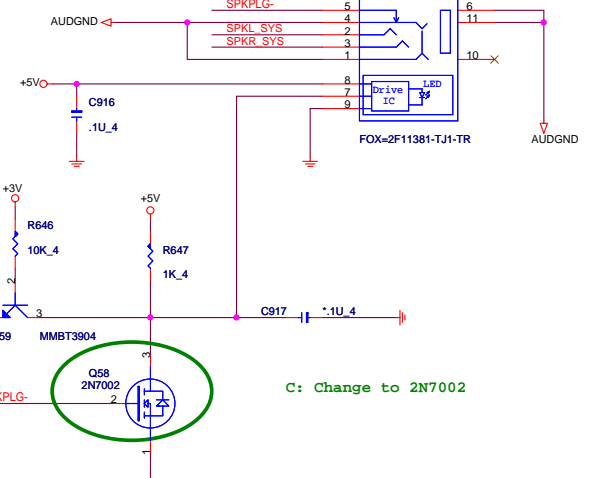


**SPEAKER CON.**



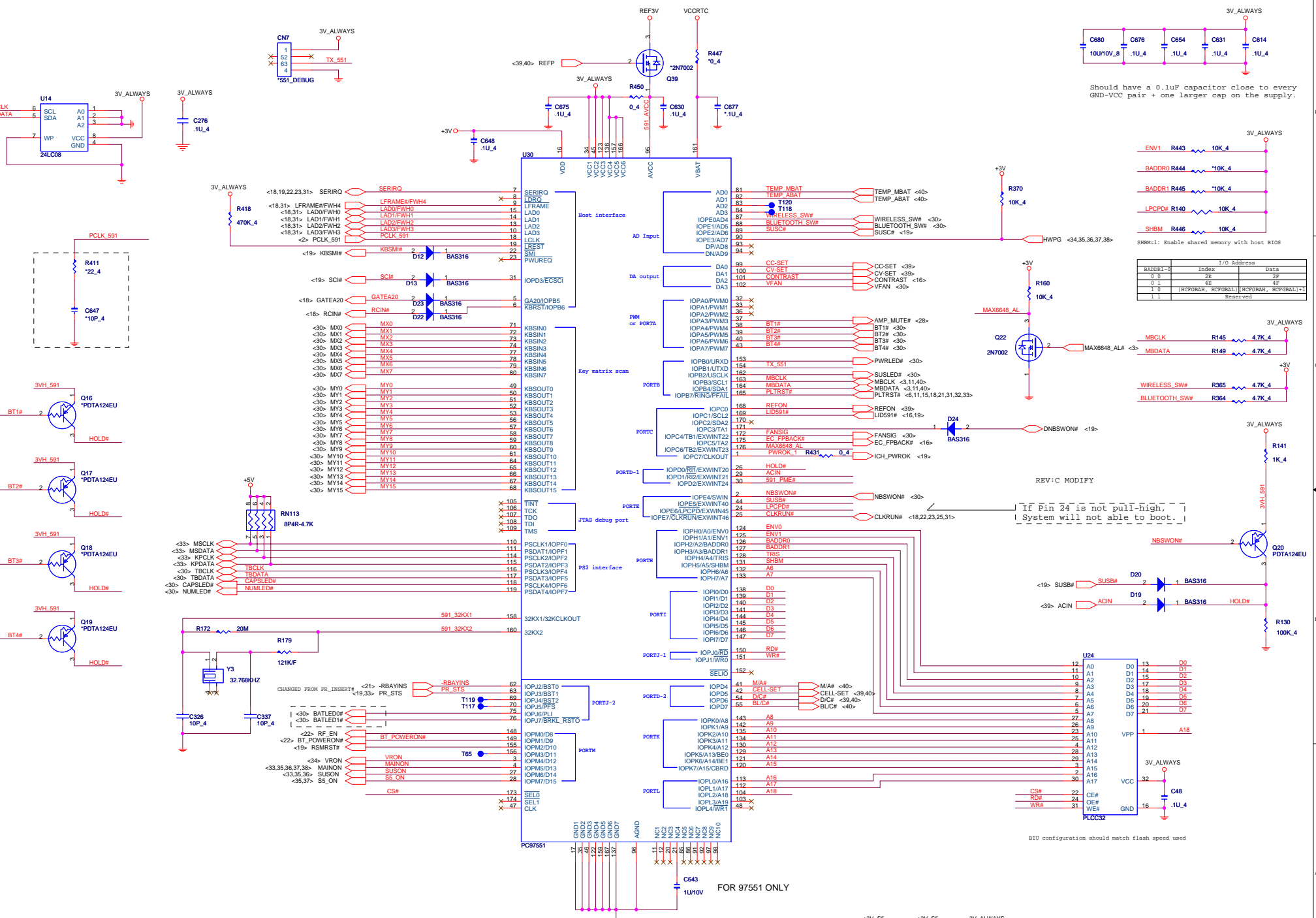
F: NEW ADD FOR ESD  
CLOSE TO CN35

**LINE OUT&SPDIF**



**PROJECT : ZL3**  
**Quanta Computer Inc.**

LDRQ#(pin 8) internal is no use



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

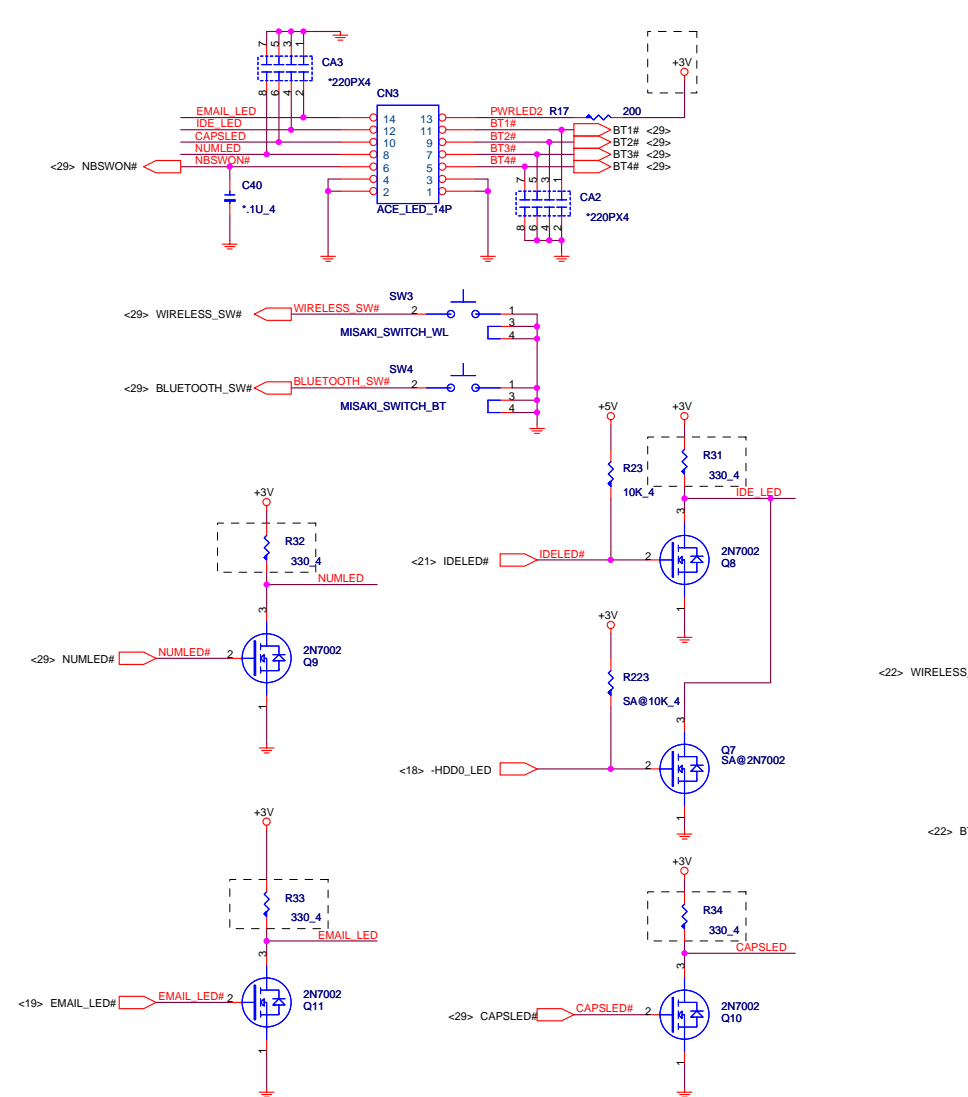
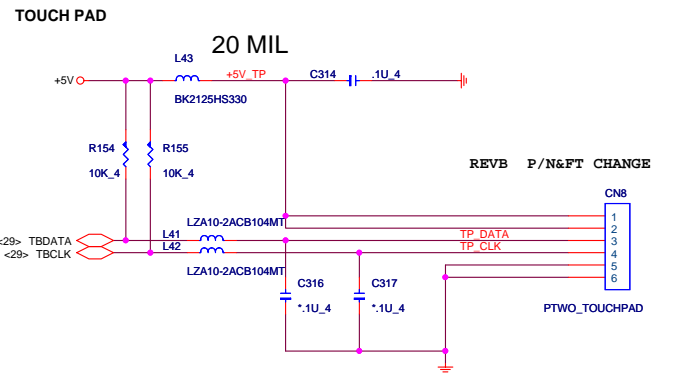
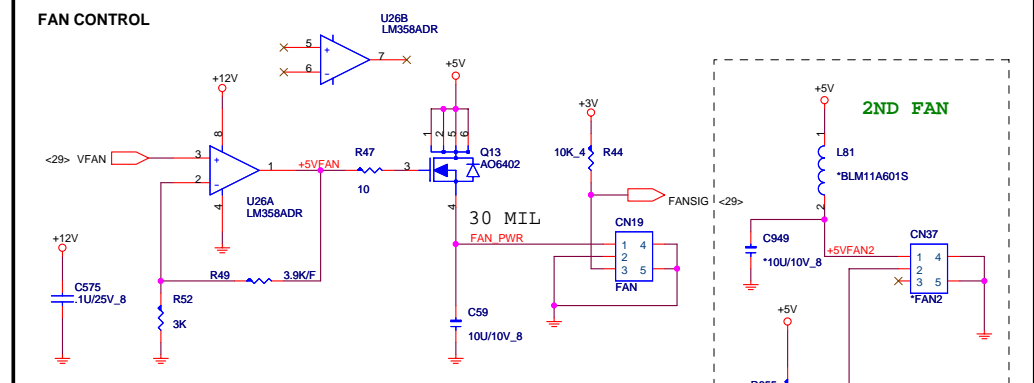
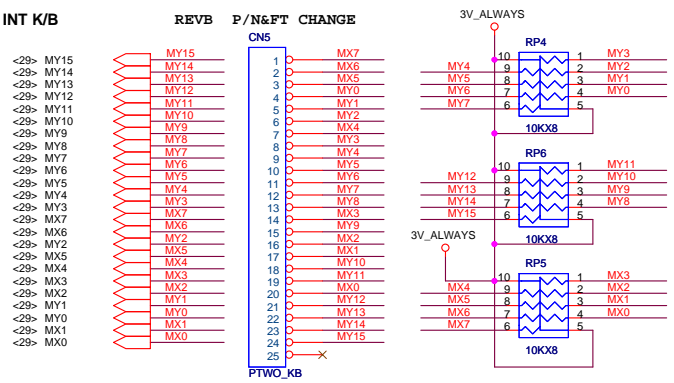
REV:C MODIFY  
If Pin 24 is not pull-high, System will not able to boot.

**PROJECT : ZL3**  
**Quanta Computer Inc.**

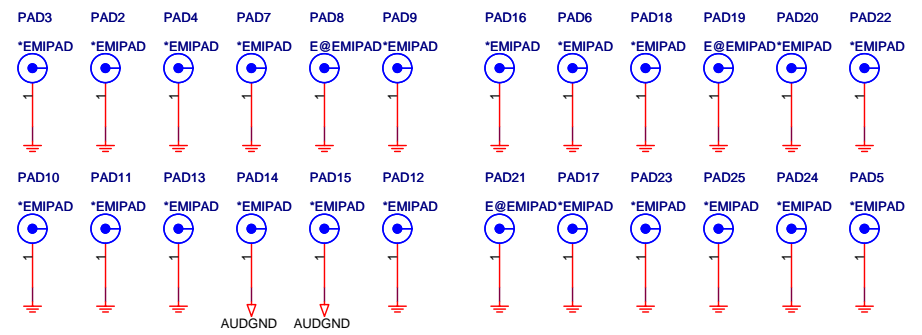
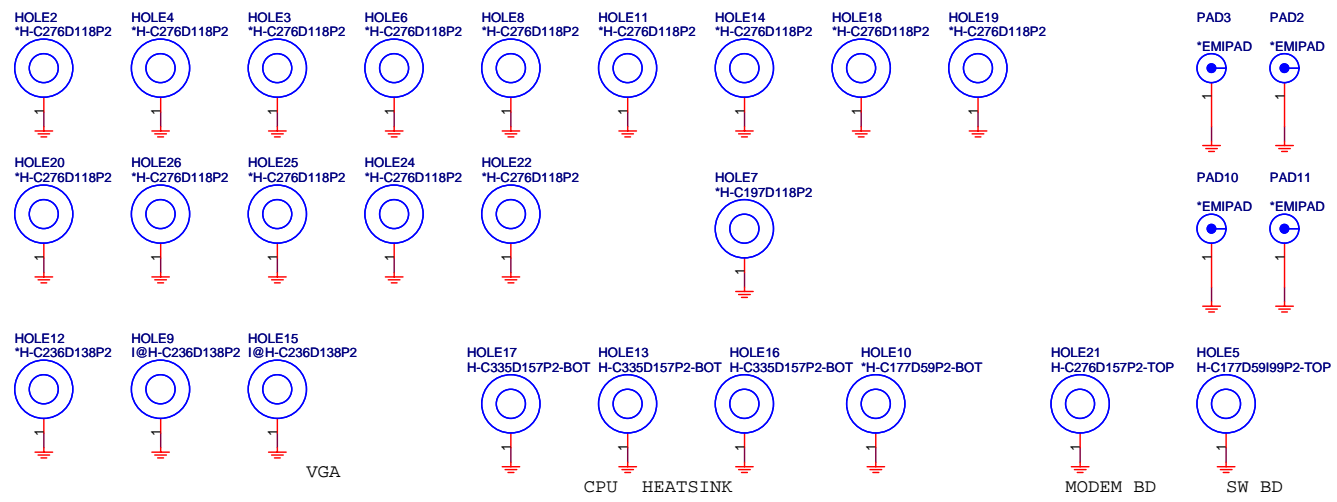
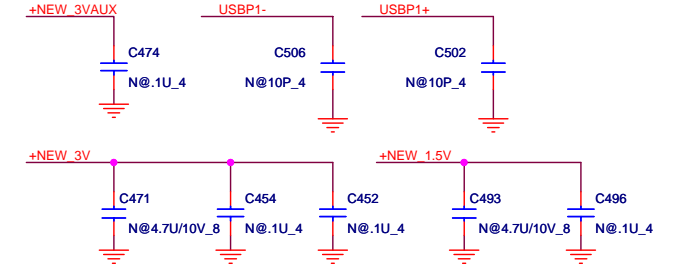
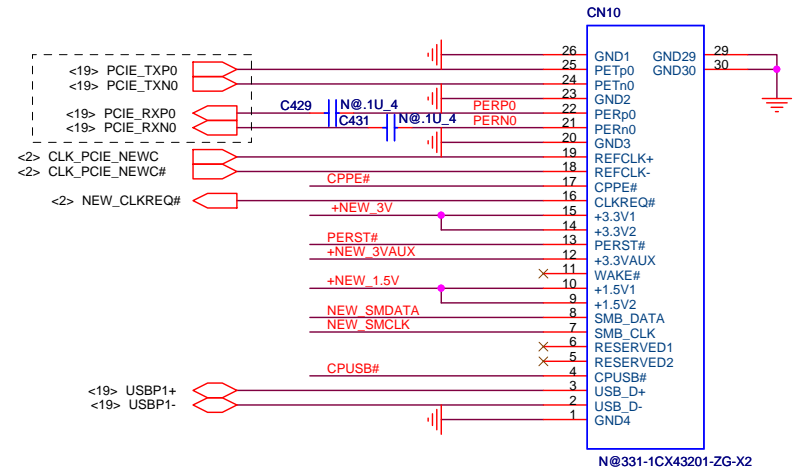
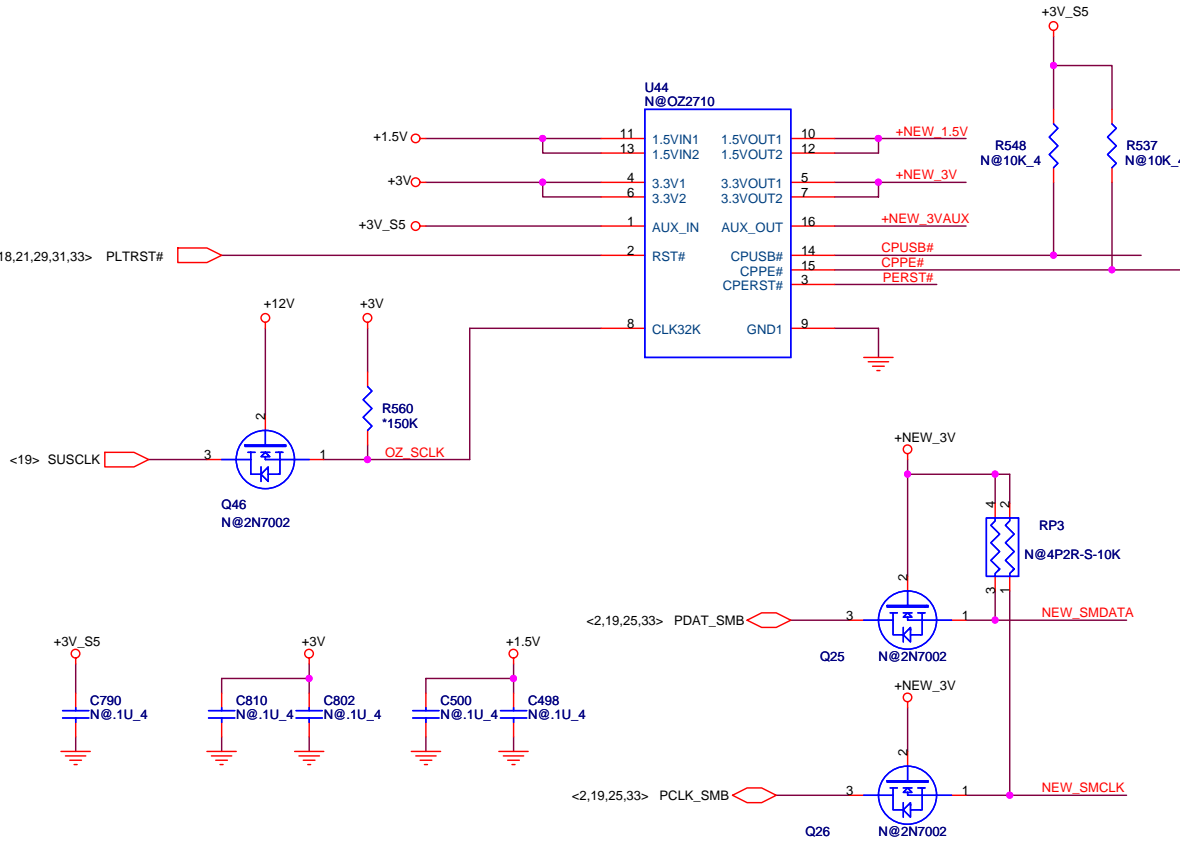
Size: Document Number  
**97551 & FLASH**

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INTERNAL PULLUP IN SB  
<25> LAN\_PME#



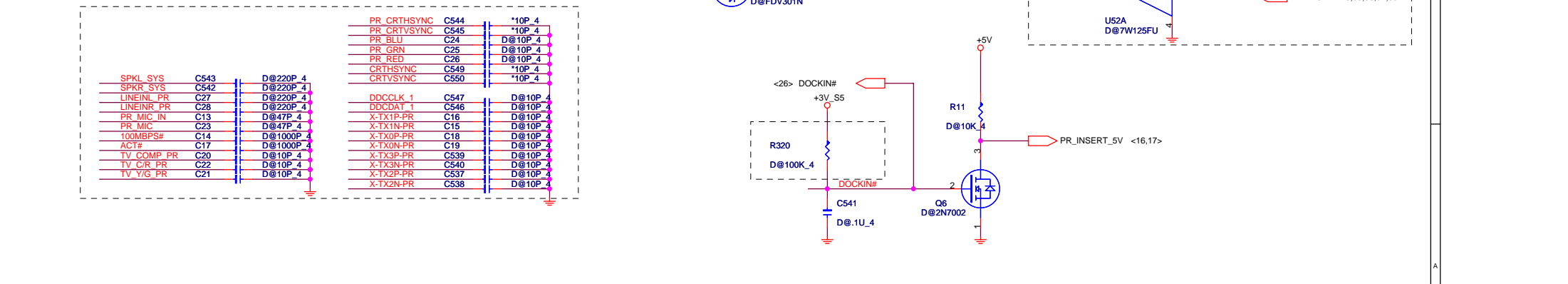
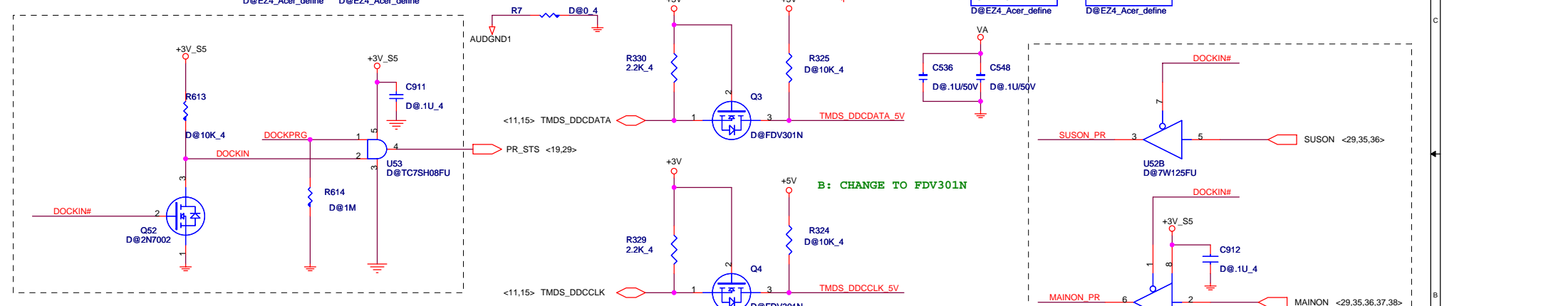
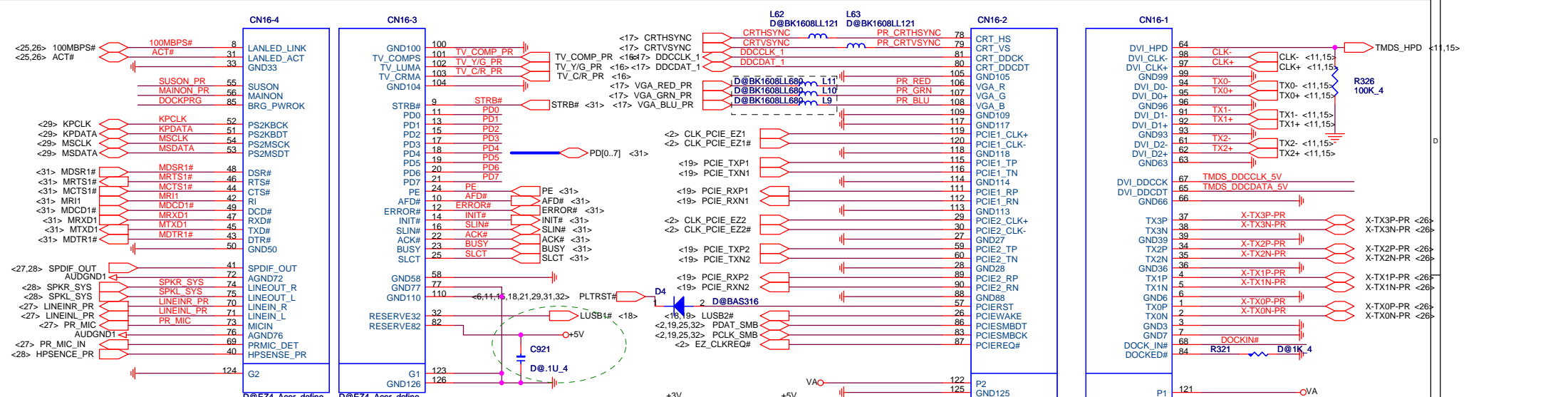





**PROJECT : ZL3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>EZ PORT &amp; SIO (87383)</b>	C
Date:	Tuesday, March 29, 2005	Sheet 32 of 40



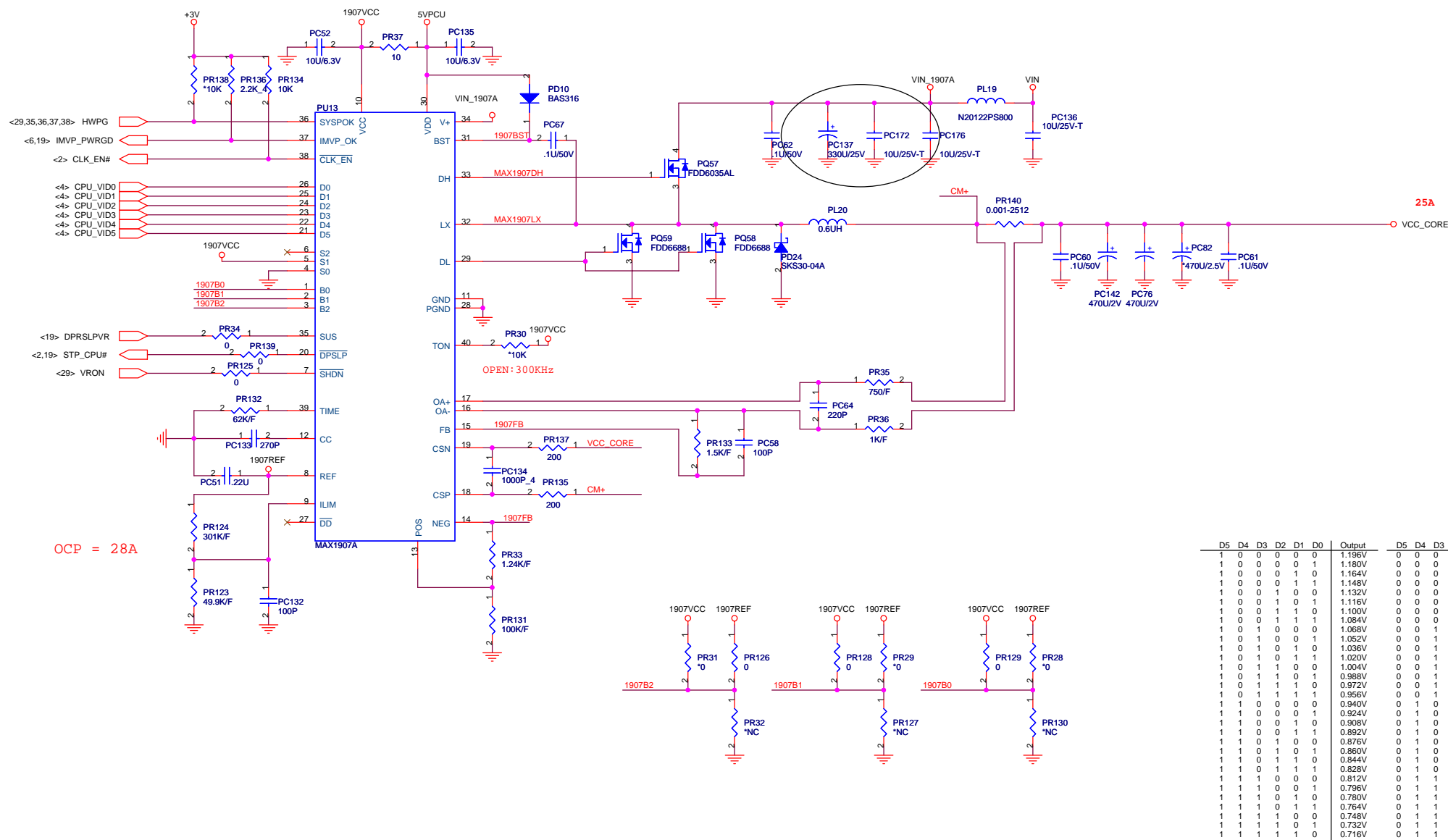


SPKL_SYS	C543	D@220P_4	PR CRTHSYNC	C544	*10P_4
SPKR_SYS	C542	D@220P_4	PR CRTVSYNC	C545	*10P_4
LINEINL_PR	C27	D@220P_4	PR BLU	C24	D@10P_4
LINEINR_PR	C28	D@220P_4	PR GRN	C25	D@10P_4
PR MIC IN	C13	D@47P_4	PR RED	C26	D@10P_4
PR MIC	C23	D@47P_4	CRTHSYNC	C549	*10P_4
100MBSPS#	C14	D@1000P_4	CRTVSYNC	C550	*10P_4
ACT#	C17	D@1000P_4	DDCCLK_1	C547	D@10P_4
TV_COMP PR	C20	D@10P_4	DDCDAT_1	C546	D@10P_4
TV_C/R PR	C22	D@10P_4	X-TX1P-PR	C16	D@10P_4
TV_Y/G PR	C21	D@10P_4	X-TX1N-PR	C15	D@10P_4
			X-TX0P-PR	C18	D@10P_4
			X-TX0N-PR	C19	D@10P_4
			X-TX3P-PR	C539	D@10P_4
			X-TX3N-PR	C540	D@10P_4
			X-TX2P-PR	C537	D@10P_4
			X-TX2N-PR	C538	D@10P_4



**PROJECT : ZL3**  
**Quanta Computer Inc.**

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	<b>EZ PORT &amp; SIO (87383)</b>	<b>C</b>
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OCP = 28A


SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output
✓ OPEN	VCC	GND	0.748V

VCC\_BOOT

B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
✓ VCC	✓ VCC	✓ VCC	0.700V
✓ REF	✓ VCC	✓ VCC	1.212V

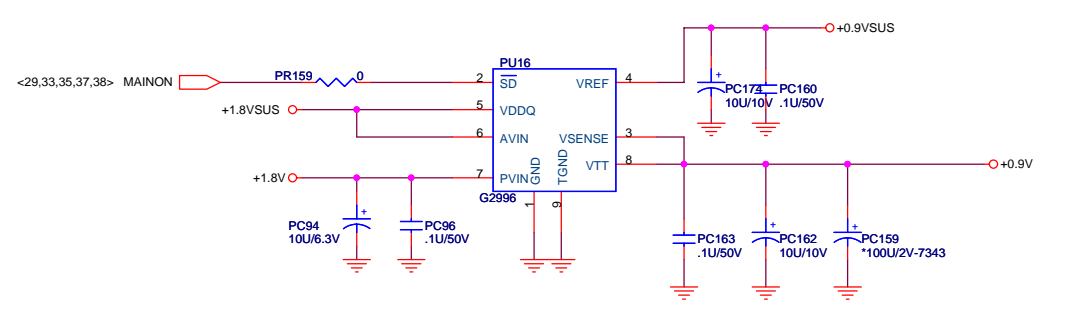
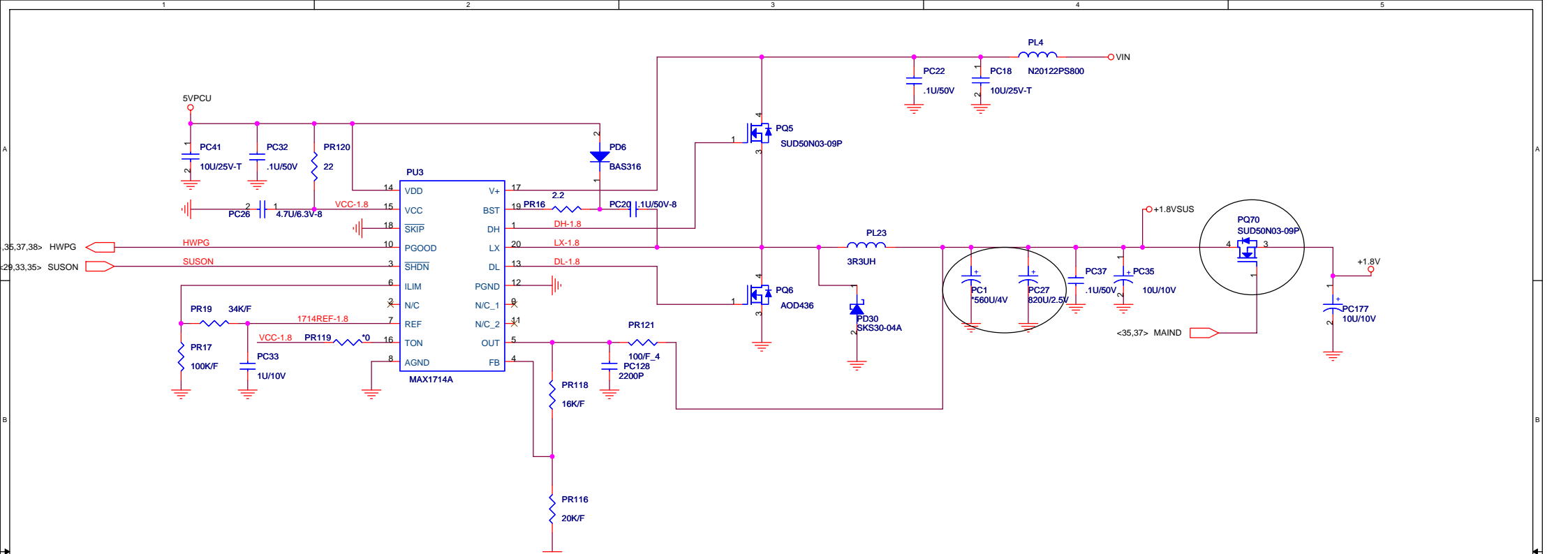
D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	1	0	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	1	1	0	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	1	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	1	0	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	1	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

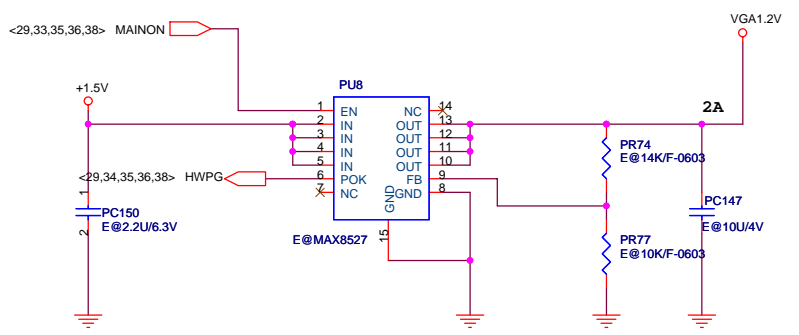
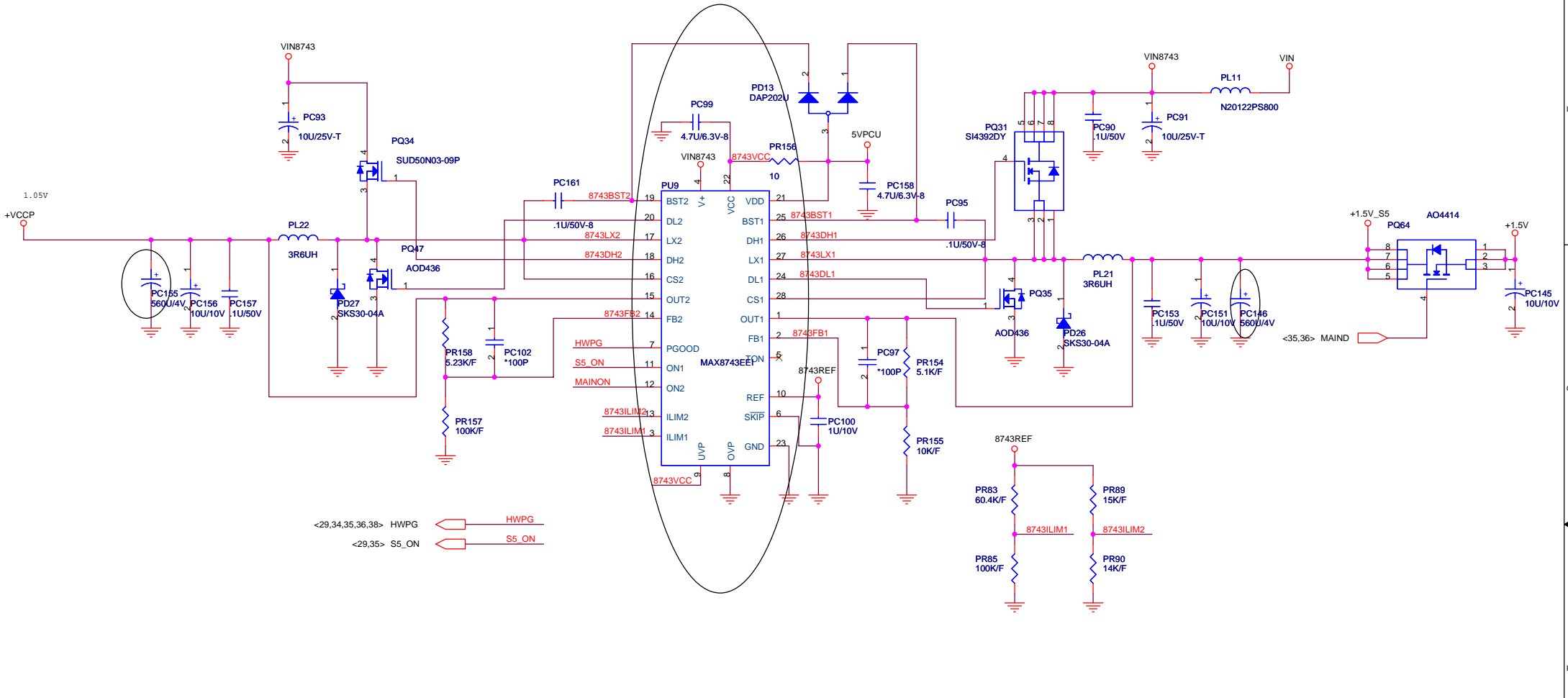


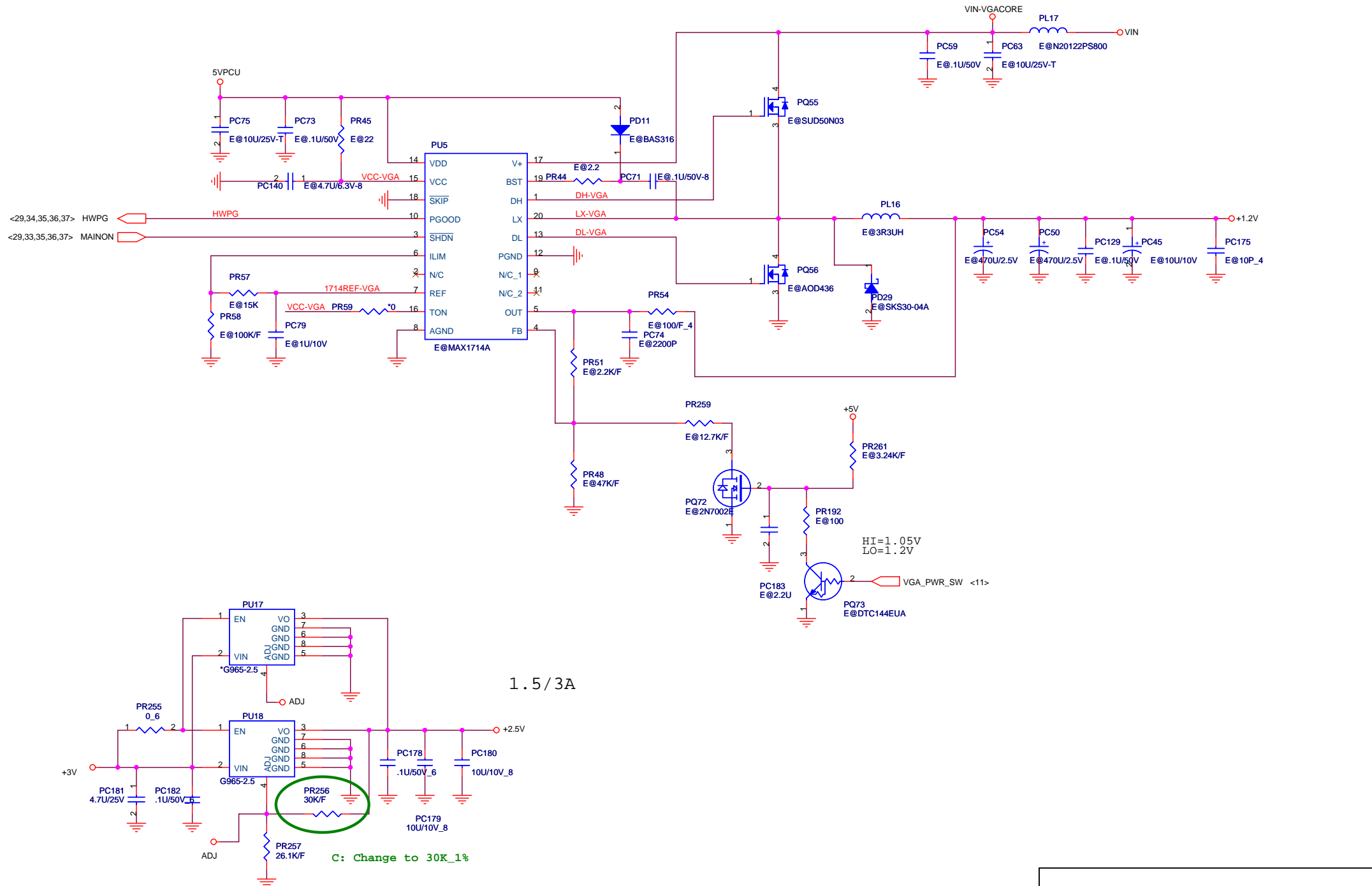
**PROJECT : ZL2**  
**Quanta Computer Inc.**

Size	Document Number <b>CPU CORE (MAX1907)</b>	Rev <b>C</b>
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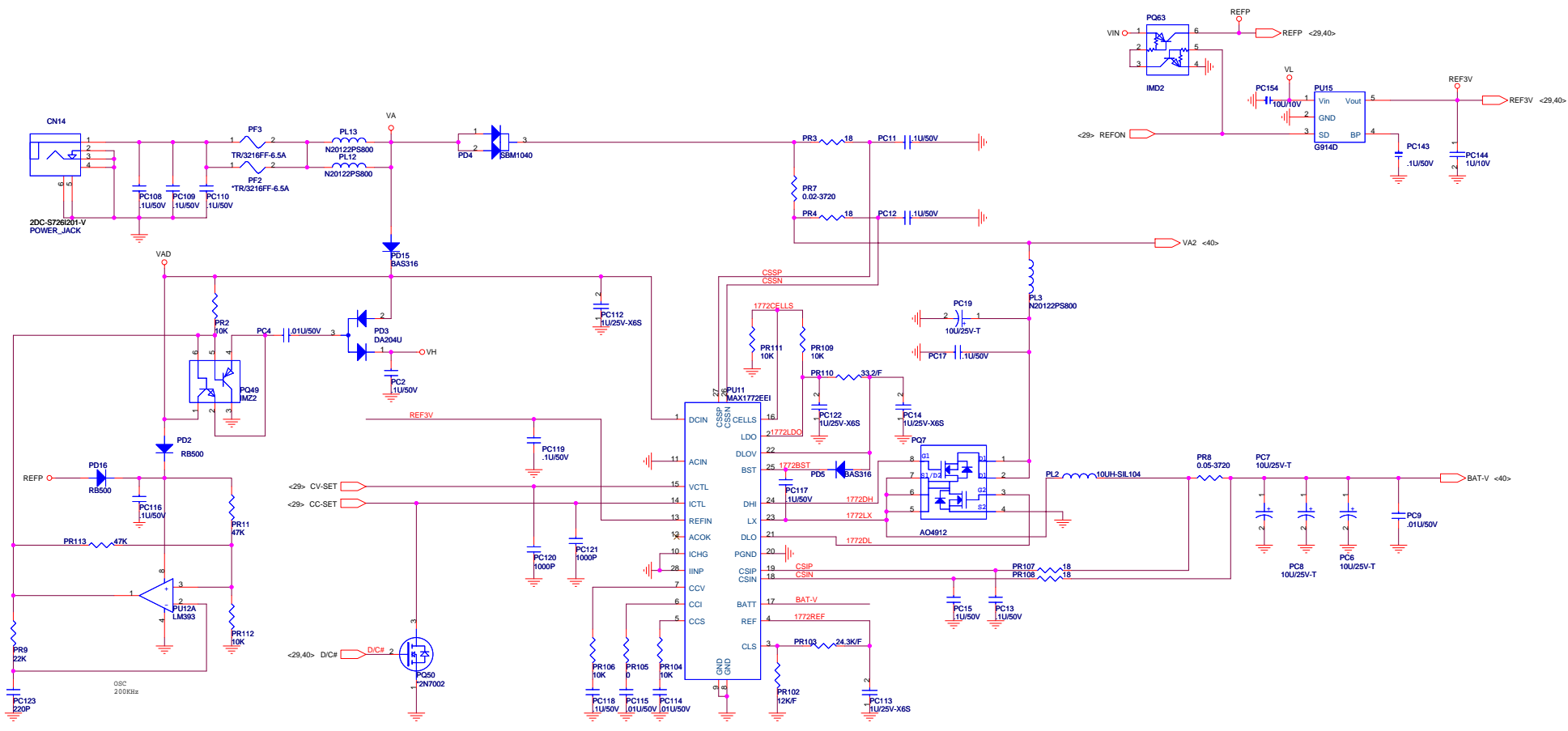




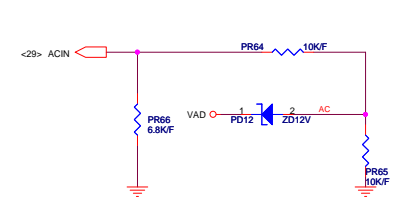
1.5/3A

C: Change to 30K\_1%

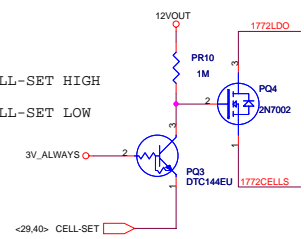
Size	Document Number	Rev
	<b>+1.2V/+1.8V</b>	C
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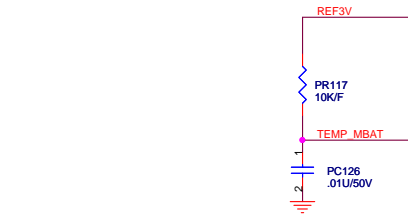
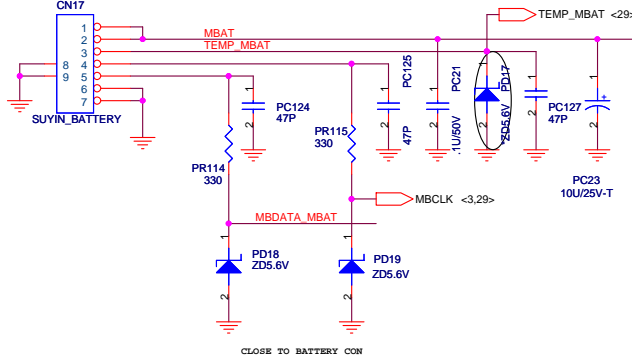
FOR 120W 6.2A



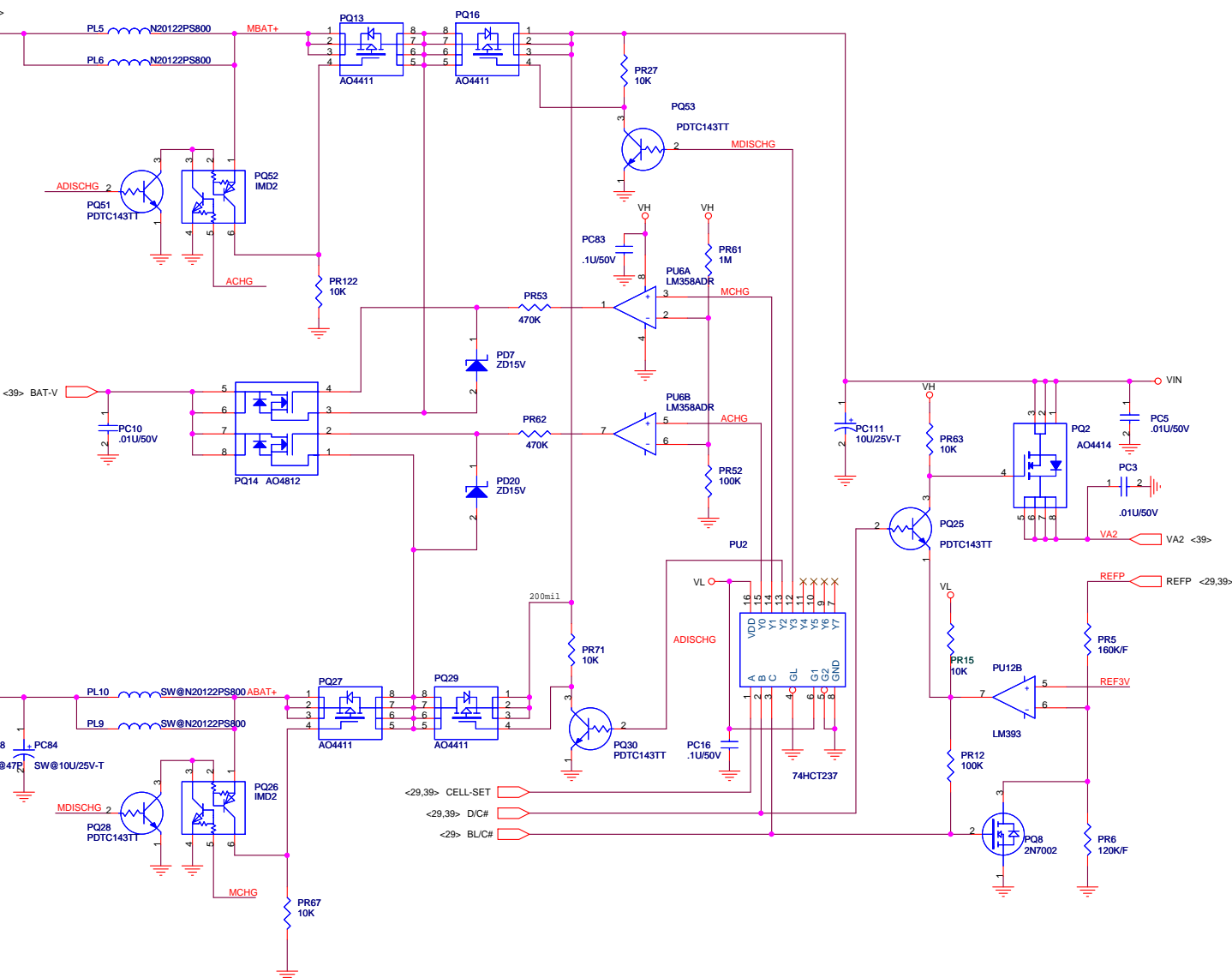
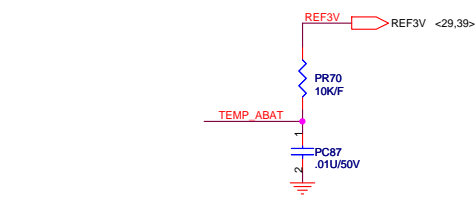
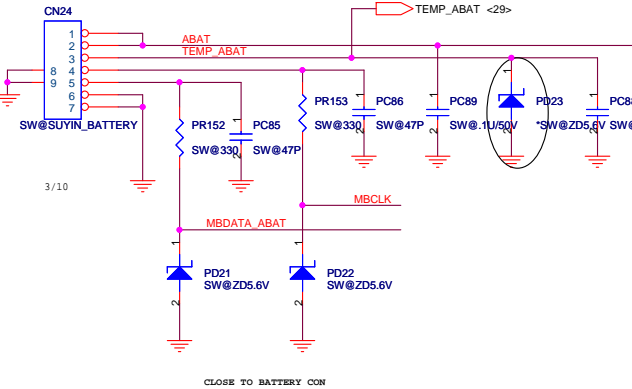
FOR 4S3P CELL-SET HIGH  
FOR 3S3P CELL-SET LOW



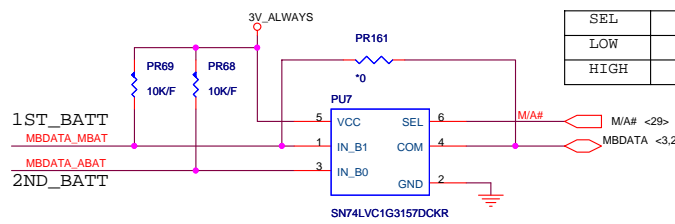
1ST\_BATT\_CONN



2ND\_BATT\_CONN



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



**PROJECT : ZL2**  
**Quanta Computer Inc.**

Size: Document Number  
**BATTERY SELECT**

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