

9. Schematic Diagram

9-1 MAIN BOARD

9-1-1 Schematic Diagrams

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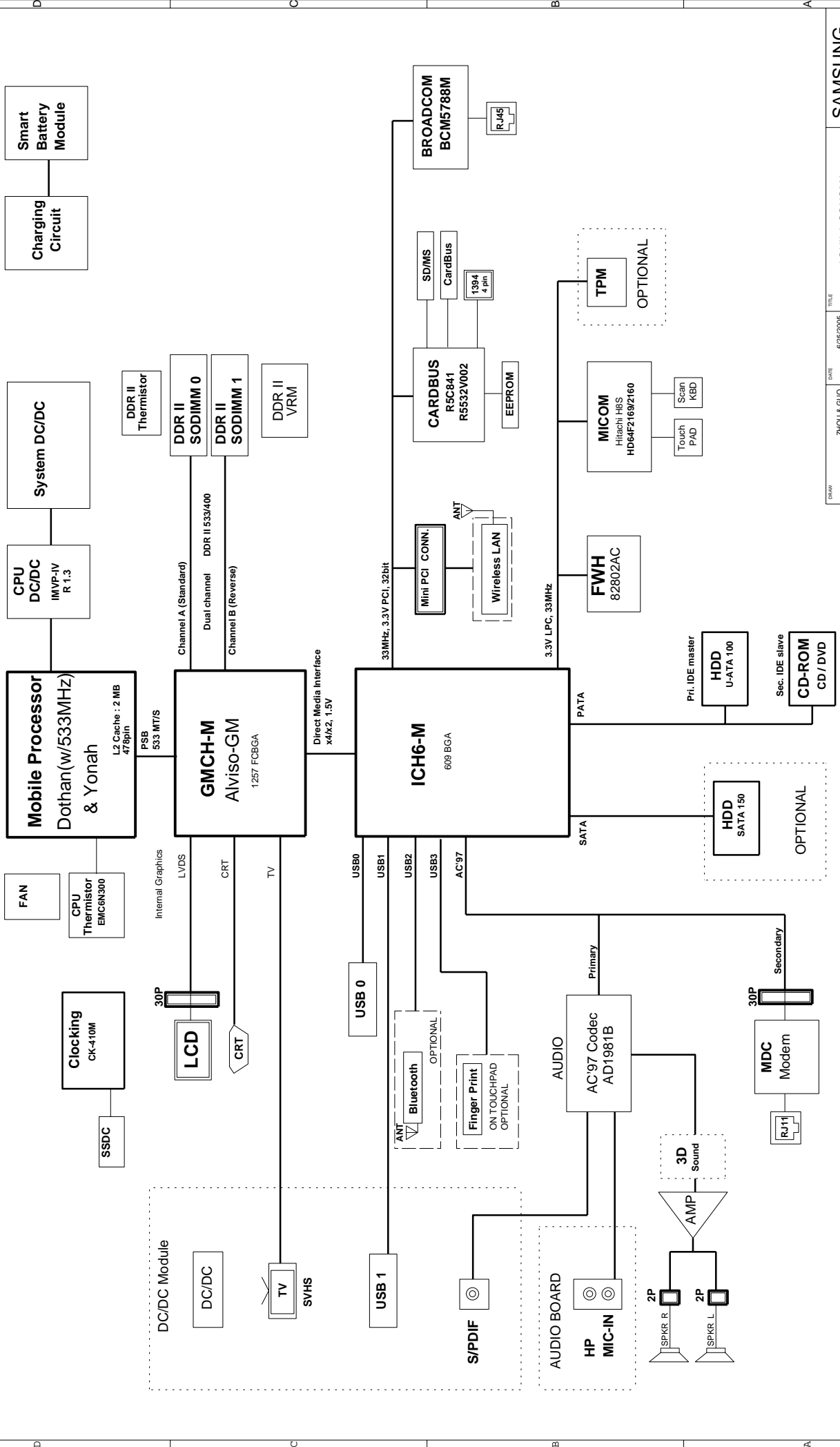
Aquila-So

CPU : Dothan
 Chip Set : Intel Alviso + ICH6-M
 Remarks : Internal Gfx.

Model Name : X06
 PBA Name : BA92-03859A
 PCB Code : BA41-00529A
 Dev. Step : MP
 Revision : 1.0
 T.R. Date : 2005-6-25

DRAW	CHECK	APPROVAL
ZHOU JUN GUO LEI	CHEN TAO	KEVIN LEE

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DATE	6/25/2005	TITLE	AQUILA-SONOMA MAIN
DRAWN	ZHOU & GUO	REV. STEP	MP
CHECK	ANTONIO	REV.	1.0
APPROVAL	KEVIN LEE	LAST EDIT	
MODULE CODE			

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PART NO. BA41-00529A	
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OPERATION BLOCK DIAGM	
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

External PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
MiniPCI SLOT	AD23	1	E,F
LOM	AD21	2	G

i²C / SMBus Address

Devices	Address	Hex	Bus
ICH6-M	Master	-	SMBUS Master
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
CY25623C(Spread Spectrum)	1101 010x	D4h	-
SODIMMO	1010 0000	A0h	-
SODIMM1	1010 010x	A4h	-
MICOM	Master	-	SMBUS Master
EMC6N300(Thermal Sensor)	0101 111x	5Eh	Thermal Sensor
BATTERY	0001 011x	16h	BATTERY INFORMATION

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
2 (OPTION)	SYSTEM PORT B (OPTION)
3 (OPTION)	FINGER PRINTER (OPTION)

Voltage Rails

VDC	Primary DC system power supply (7. to 21V)
VCC_CORE	Core voltage for DOTHAN CPU (1.356 - 0.844V)
VTT	Processor System Bus(PSB) Termination (1.05V) / MCH-M Core Voltage (1.05V)
P1.5V_AUX	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P0.9V	0.9V power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_ALWAYS	3.3V power rail (Always on@ AC-IN mode & off in S4-S5@BATT mode)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5V power rail (off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)

REVISION HISTORY

See revision notes in the changes file for more information.

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID Hex	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID Hex
0	0	0	0	0	0	1.708 V	3Eh	1	0	0	0	0	0	1.086 V	1Eh
0	0	0	0	0	1	1.692 V	3Fh	1	0	0	0	0	1	1.186 V	1Fh
0	0	0	0	1	0	1.676 V	3Dh	1	0	0	1	0	0	1.164 V	1Dh
0	0	0	0	1	1	1.660 V	3Ch	1	0	0	1	1	0	1.148 V	1Ch
0	0	0	0	1	0	1.644 V	3Bh	1	0	0	1	0	0	1.132 V	1Bh
0	0	0	0	1	0	1.628 V	3Ah	1	0	0	1	0	0	1.116 V	1Ah
0	0	0	0	1	1	1.612 V	39h	1	0	0	1	1	0	1.100 V	19h
0	0	0	0	1	1	1.596 V	38h	1	0	0	1	1	1	1.084 V	18h
0	0	0	0	1	1	1.580 V	37h	1	0	0	1	1	1	1.068 V	17h
0	0	0	0	1	0	1.564 V	36h	1	0	0	1	0	0	1.052 V	16h
0	0	0	0	1	0	1.548 V	35h	1	0	0	1	0	0	1.036 V	15h
0	0	0	0	1	1	1.532 V	34h	1	0	0	1	1	0	1.020 V	14h
0	0	0	0	1	1	1.516 V	33h	1	0	0	1	1	1	1.004 V	13h
0	0	0	0	1	0	1.500 V	32h	1	0	0	1	0	0	988 V	12h
0	0	0	0	1	0	1.484 V	31h	1	0	0	1	0	0	972 V	11h
0	0	0	0	1	1	1.468 V	30h	1	0	0	1	1	0	956 V	10h
0	0	0	0	1	0	1.452 V	2Fh	1	0	0	1	0	0	940 V	0Fh
0	0	0	0	1	0	1.436 V	2Eh	1	0	0	1	0	0	924 V	0Eh
0	0	0	0	1	1	1.420 V	2Dh	1	0	0	1	1	0	908 V	0Dh
0	0	0	0	1	1	1.404 V	2Ch	1	0	0	1	1	1	892 V	0Ch
0	0	0	0	1	0	1.388 V	2Bh	1	0	0	1	0	0	876 V	0Bh
0	0	0	0	1	0	1.372 V	2Ah	1	0	0	1	0	0	860 V	0Ah
0	0	0	0	1	0	1.356 V	29h	1	0	0	1	0	0	844 V	09h
0	0	0	0	1	1	1.340 V	28h	1	0	0	1	1	0	828 V	08h
0	0	0	0	1	1	1.324 V	27h	1	0	0	1	1	1	812 V	07h
0	0	0	0	1	0	1.308 V	26h	1	0	0	1	0	0	796 V	06h
0	0	0	0	1	1	1.292 V	25h	1	0	0	1	1	0	780 V	05h
0	0	0	0	1	0	1.276 V	24h	1	0	0	1	0	0	764 V	04h
0	0	0	0	1	1	1.260 V	23h	1	0	0	1	1	0	748 V	03h
0	0	0	0	1	1	1.244 V	22h	1	0	0	1	1	0	732 V	02h
0	0	0	0	1	1	1.228 V	21h	1	0	0	1	1	1	716 V	01h
0	0	0	0	1	0	1.212 V	20h	1	0	0	1	1	0	700 V	00h

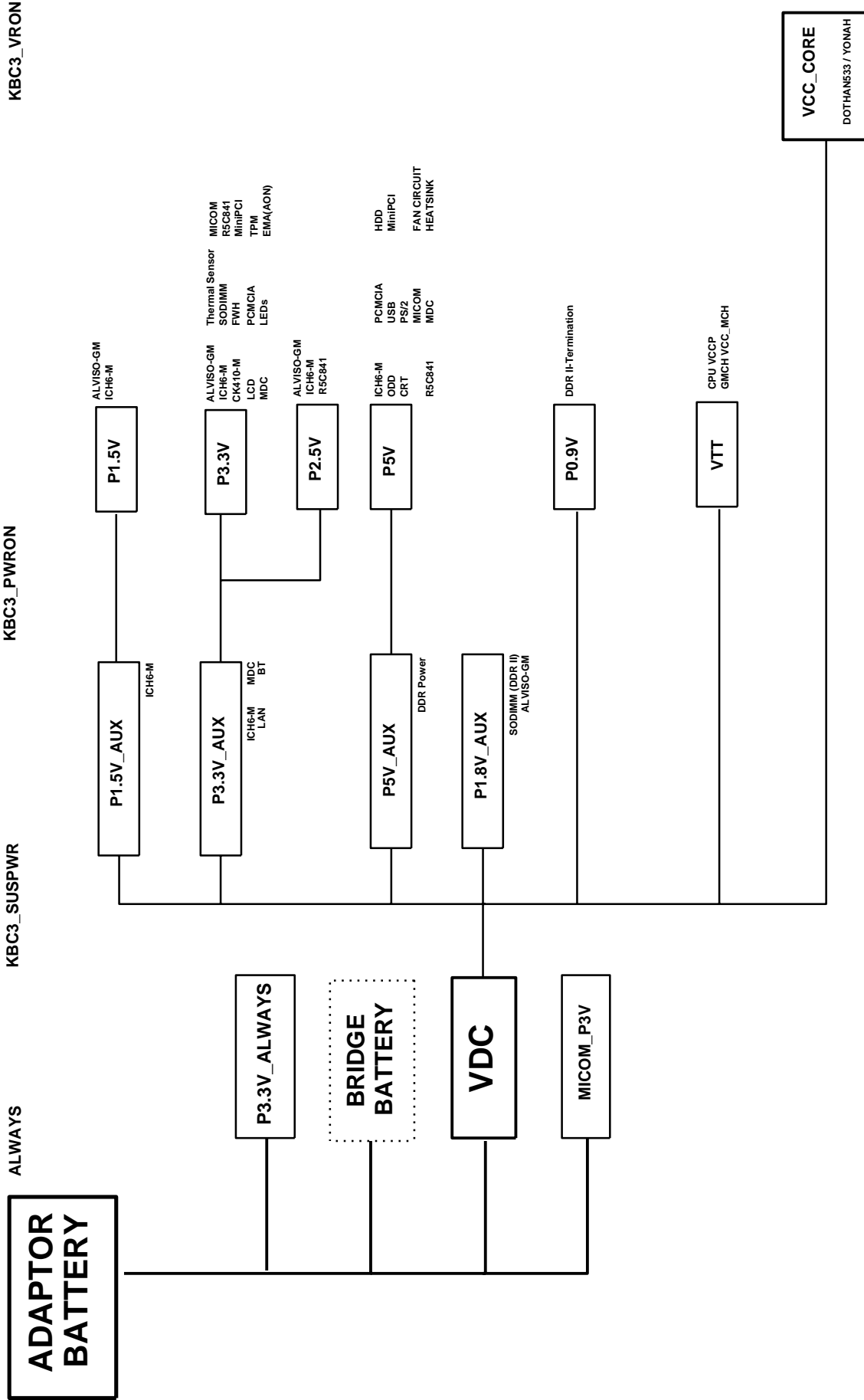
HIGHEST FREQ. LOWEST FREQ. DEEPEER SLEEP

System Power States

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V _{ALW}	+V _S	Clocks
S0 (Full On)	HIGH	HIGH	HIGH	ON	ON	ON
S3-Hot (STR)	LOW	HIGH	HIGH	ON	ON	LOW
S3-Cold (STR)	LOW	HIGH	HIGH	ON	OFF	OFF
S4 (STD)	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF

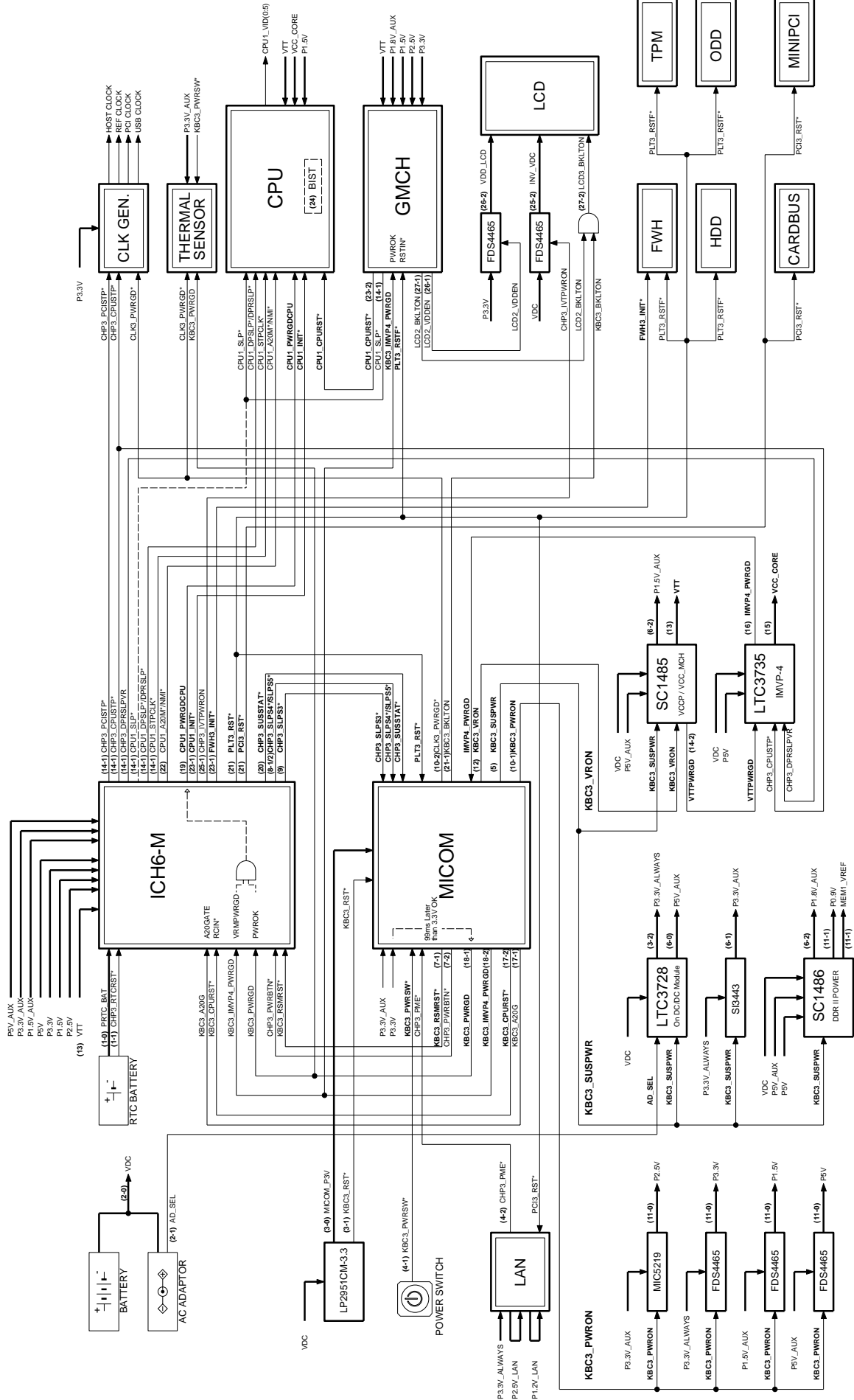
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APPROVAL	DEV. STEP	MP	BOARD INFORMATION	
MIDDLE CODE	REV	1.0	PAGE 3 OF 46	
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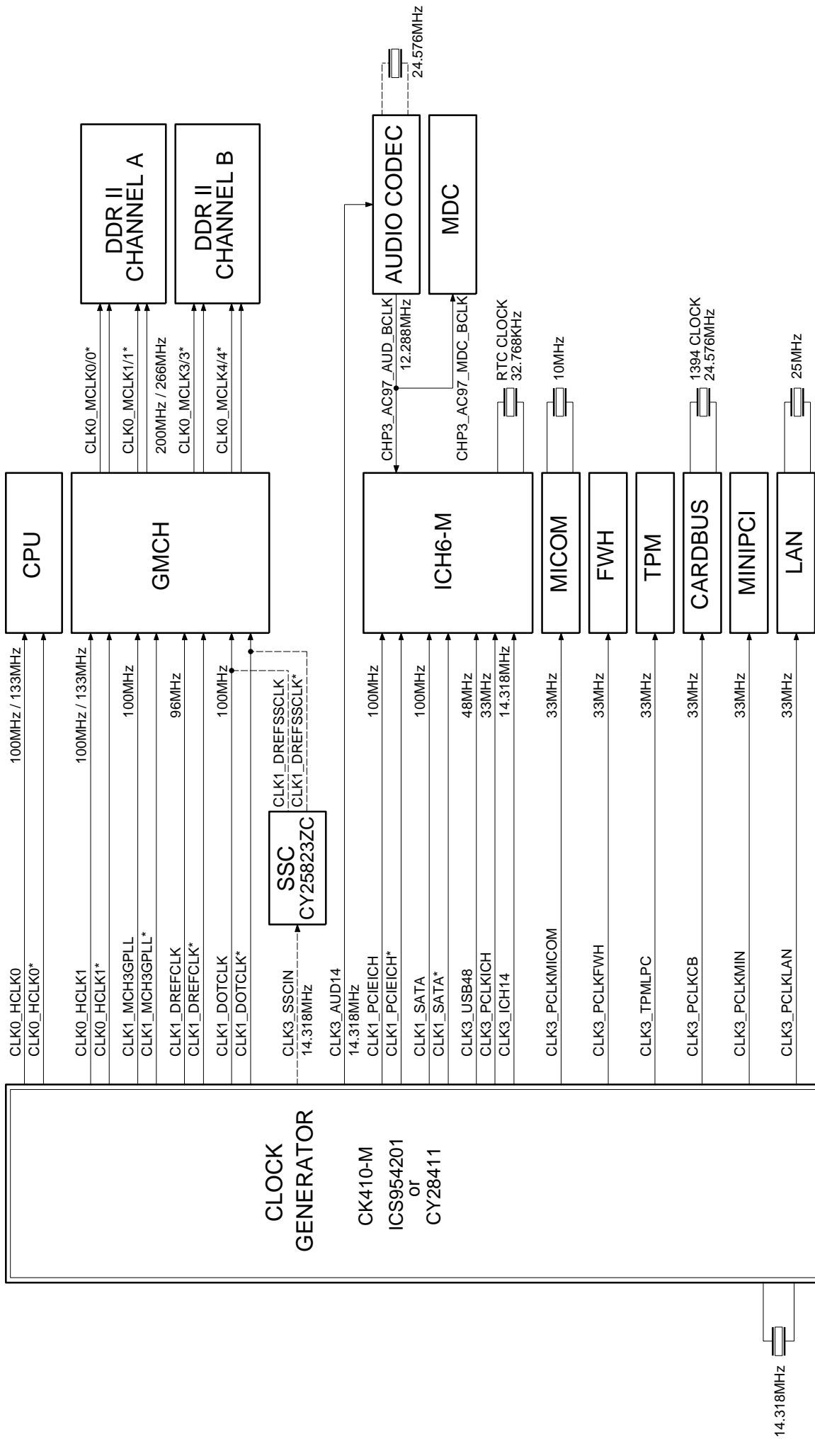
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			POWER ON SEQUENCE
			MAIN
			BA41-00529A
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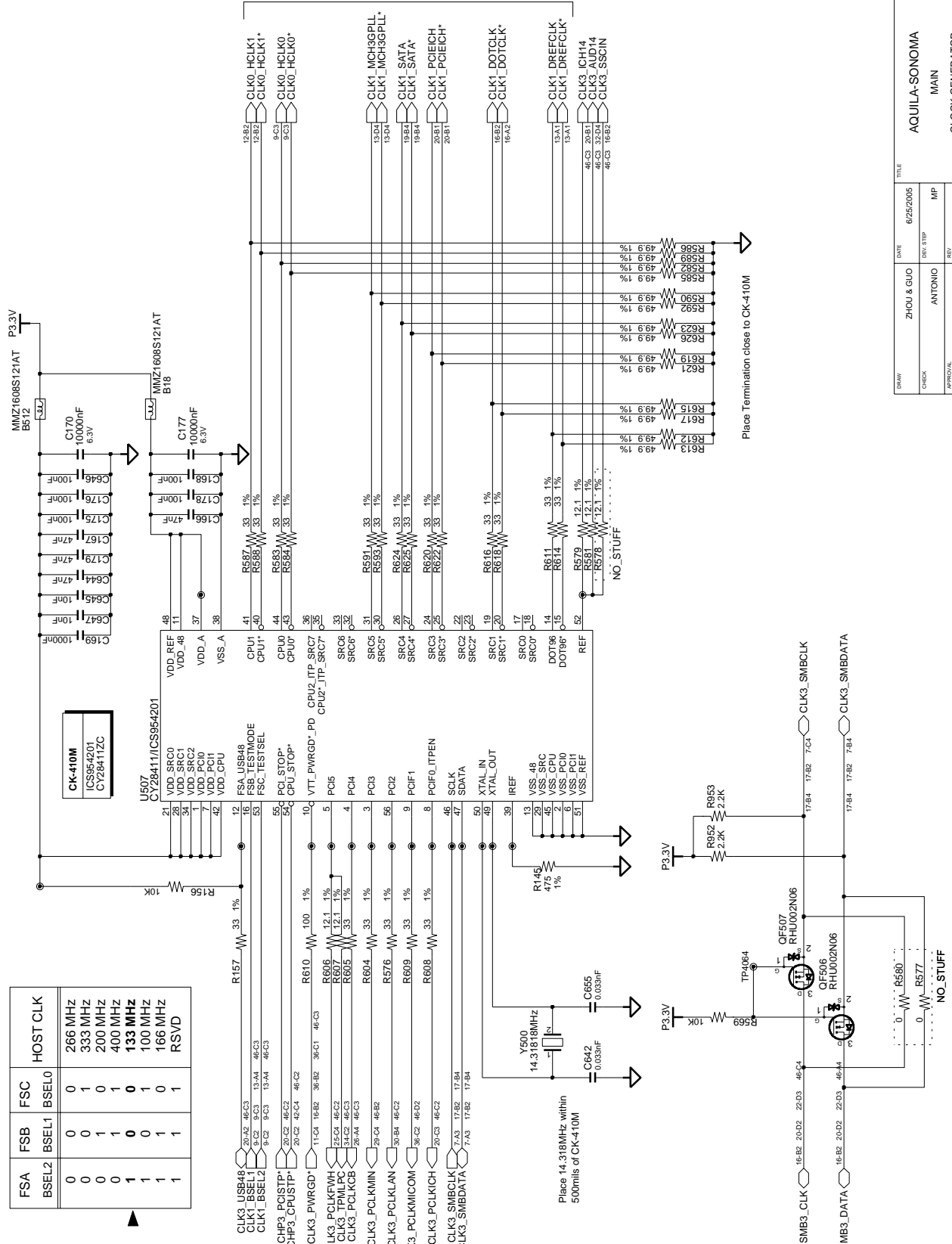
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		CLOCK DIAGRAM	
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FSA	FSB	FSC	HOST CLK
BSEL1	BSEL0	BSEL0	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



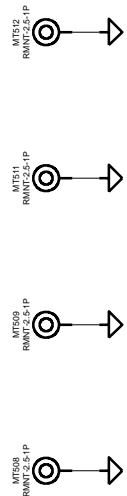
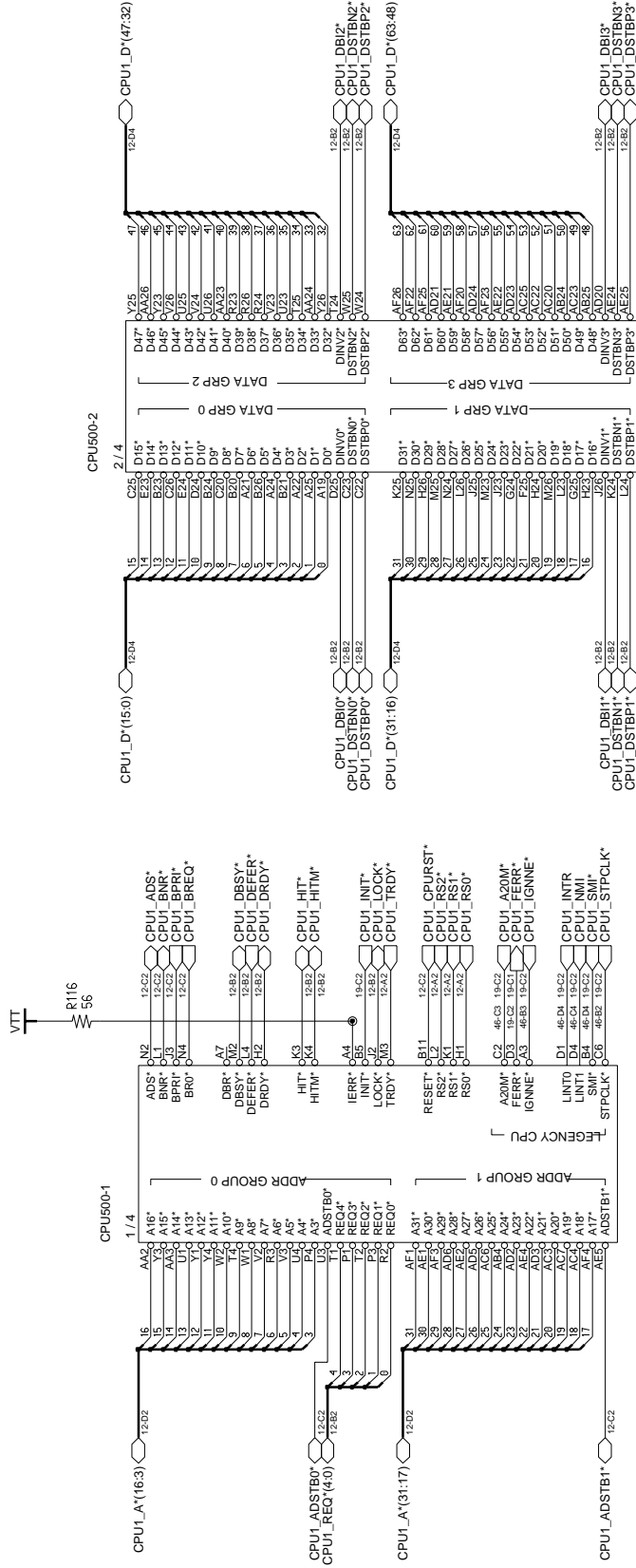
Place Termination close to CK-410M

Place 14.318MHz within
500mils of CK-410M

Zdiff=100ohm

DRAWN		DATE		TITLE	
ZHOUL & GUO		6/25/2005		AQUILA-SONOMA MAIN	
CHECKED		DWG. STAMP		CLOCK GENERATOR	
ANTONIO		REV		MP	
APPROVAL		LAST EDIT		1.0	
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MODULE CODE		PAGE		7 OF 46	
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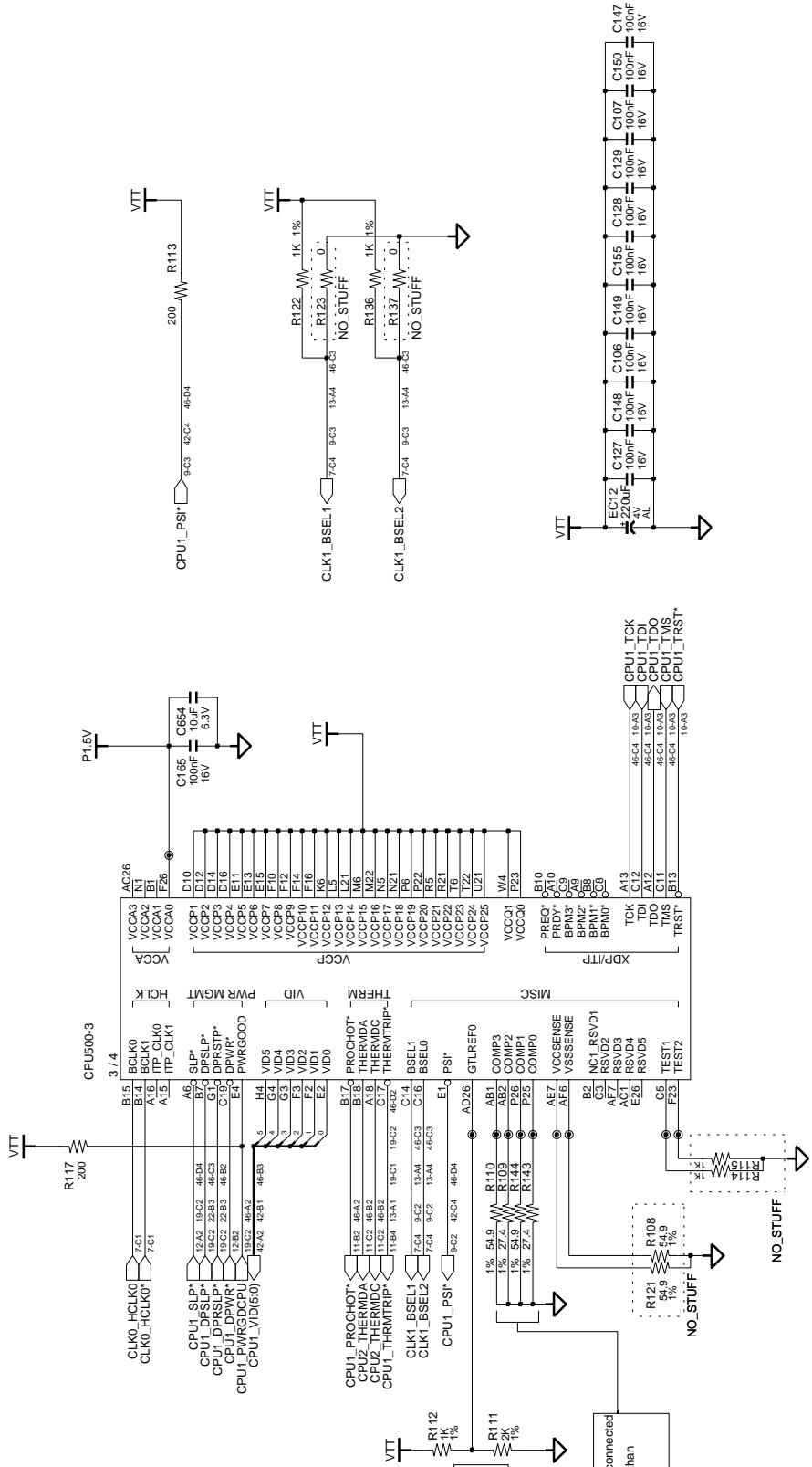
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APPROVAL	KEVIN LEE	REV	1.0
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THERTRIP* should connect to ICH6M & Alviso
 OD signal driven by CPU and GMCH

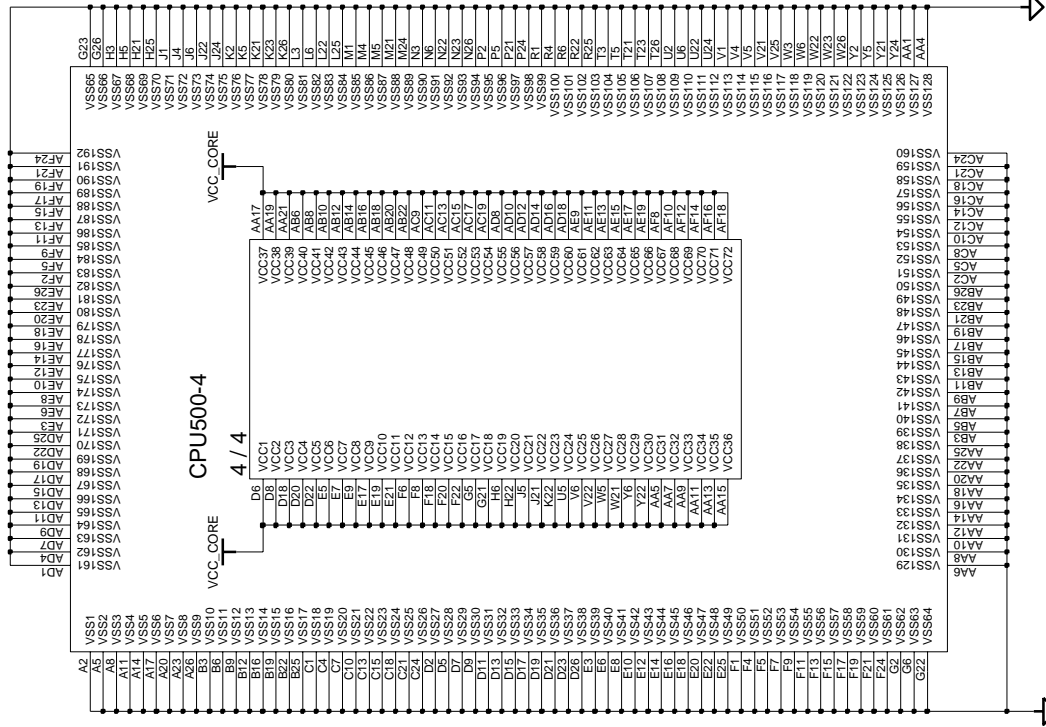
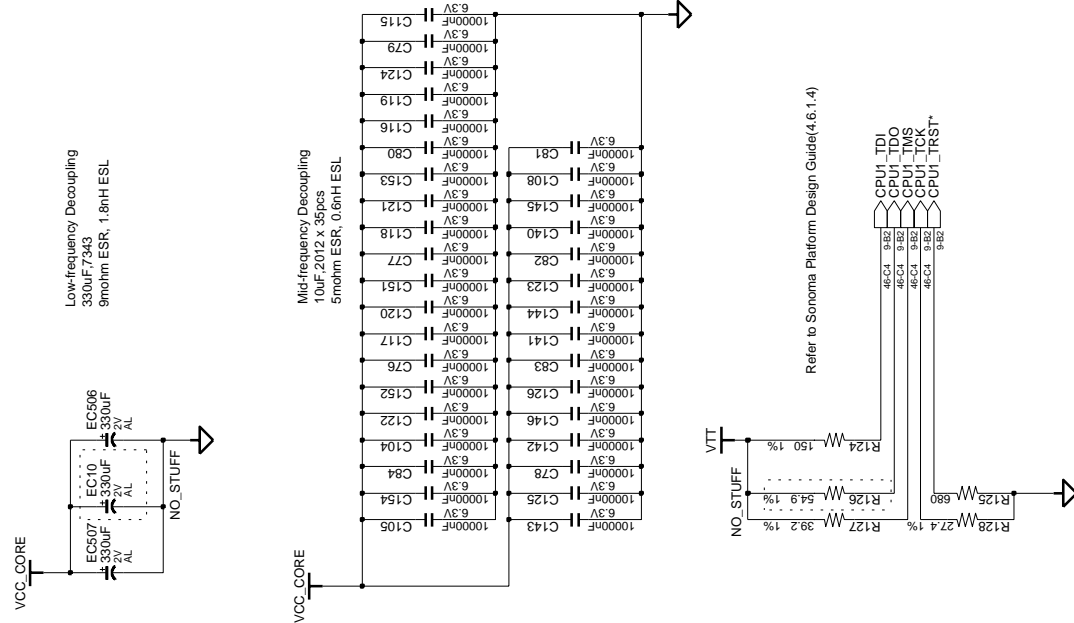
GTLREF: Keep the Voltage divider within 0.5"
 of the First GTLREF0 with Z0=55 ohm trace
 Minimize coupling of any switching signals to this net

COMP 0, 2 <(COMP 1,3) should be connected
 Z0=27.4 ohm (55 ohm) trace shorter than
 1/2" to their respective Banias Pins

DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRAWN	ZHOU & GUO	DESIGNER	ANTONIO
CHECK	ANTONIO	MP	1.0
APPROVAL	KEVIN LEE	REV	1.0
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			SAMSUNG X06 99

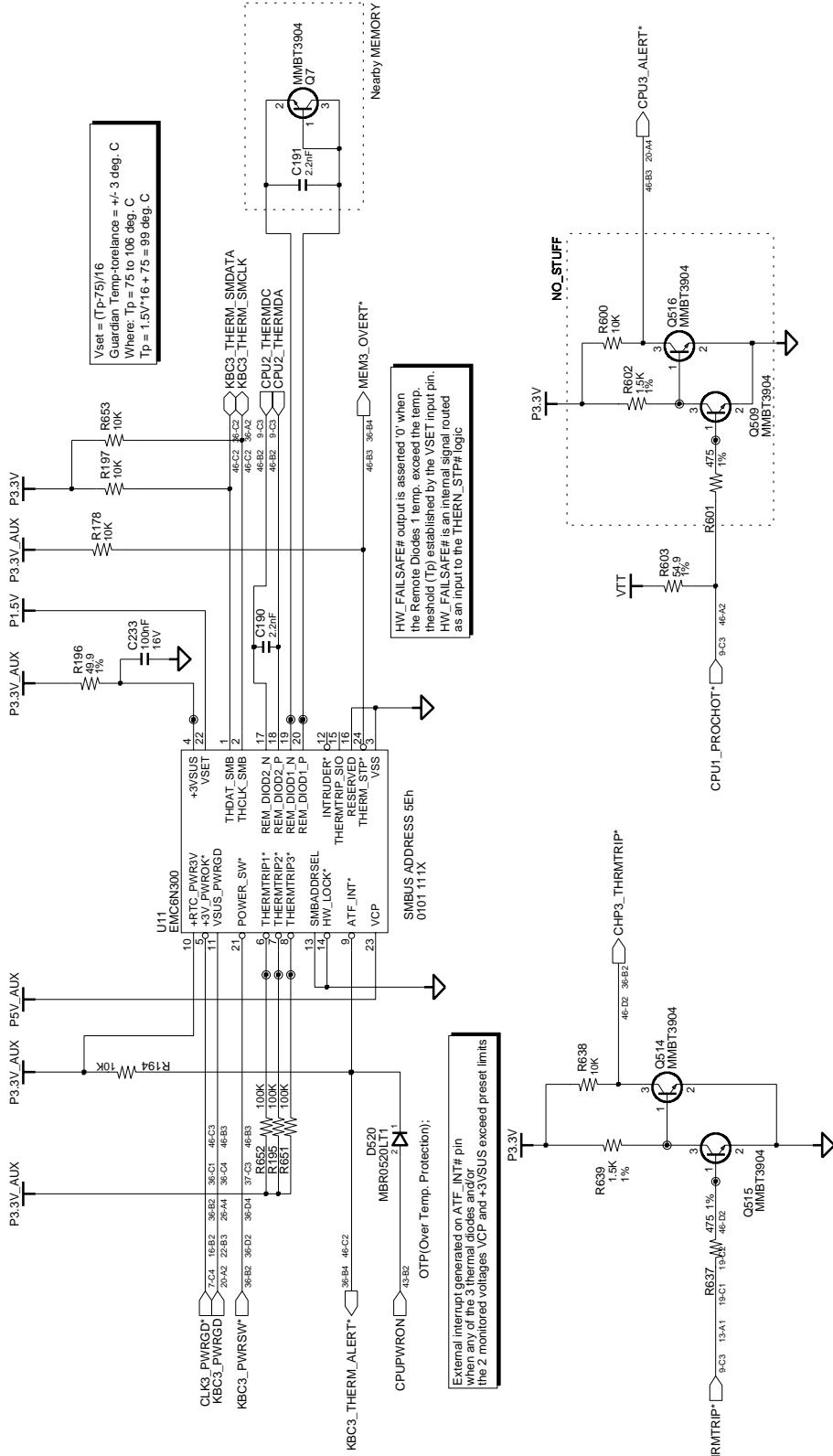
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Vcc-core Decoupling (Refer to IMVP-IV Option #4)



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CPU (3/3)		PAGE	10 OF 46

CPU / DDR Thermal Sensor



$V_{set} = (T_p - 75) / 16$
 Guardian Temp-tolerance = +/- 3 deg. C
 Where: $T_p = 75$ to 106 deg. C
 $T_p = 1.5V / 16 + 75 = 99$ deg. C

HWL_FAILSAFE# output is asserted '0' when the Remote Diodes 1 temp. exceed the temp. threshold (Tp) established by the VSET input pin. HWL_FAILSAFE# is an internal signal routed as an input to the THERN_STP# logic

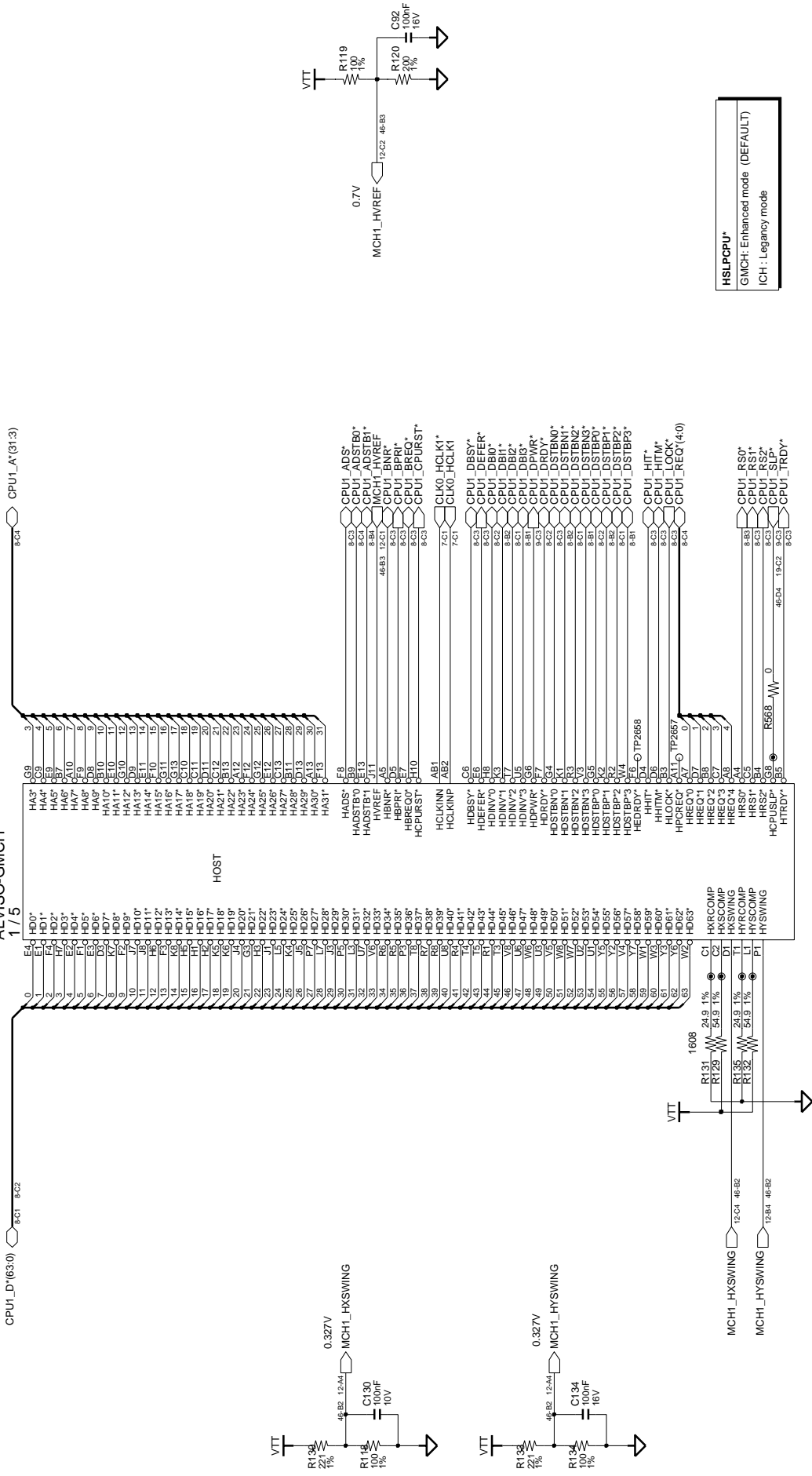
External interrupt generated on ATF_INT# pin when any of the monitored voltages (VCP and +3V(SUS) exceed preset limits

- Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
 - Keep traces away from high voltage (+12V bus)
 - Keep traces away from fast data buses and CRT signal.
 - Use recommended trace widths and spacings (10mil)
 - Place a ground plane under the traces.
 - Use guard traces flanking DXP and DXN and connecting to GND

DATE	6/25/2005	TITLE	AQUILA-SONOMA	
CHKD	ANTONIO	MP	MAIN	
APPROVAL	KEVIN LEE	REV	1.0	
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MODULE CODE		undefined	CPU/DDR Thermal Sensor	

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ALVISO500-1
ALVISO-GMCH



HSLPCPU*
 GMCH: Enhanced mode (DEFAULT)
 ICH: Legacy mode

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CHECK	ANTONIO	CHK/STEP	MP	MAIN	
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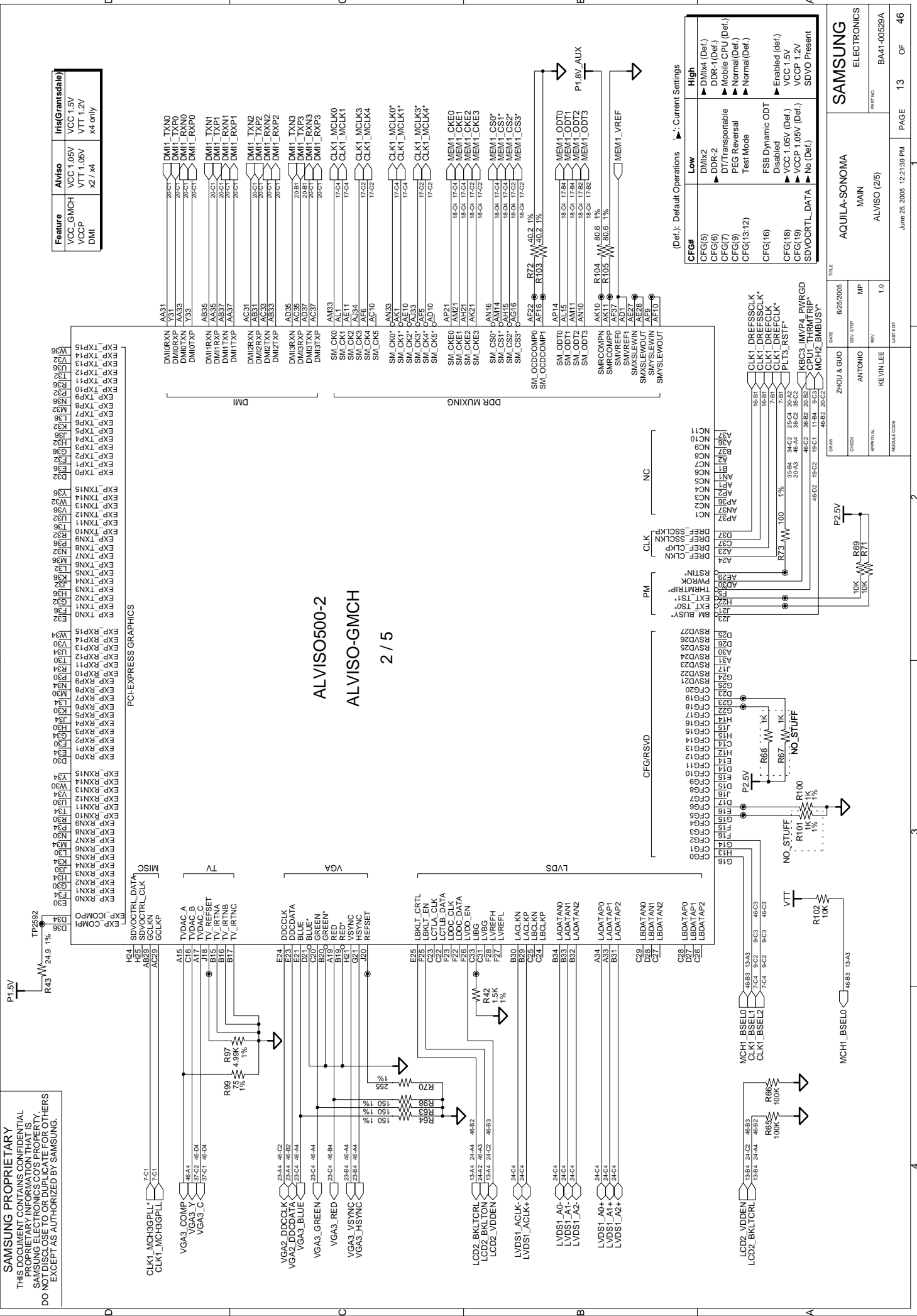
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Feature	Alviso	Iris(Grantstale)
VCC_GMCH	VCC 1.05V	VCC 1.5V
VCCP	VTT 1.05V	VTT 1.2V
DMI	x2 / x4	x4 only

ALVISO500-2

ALVISO-GMCH

2 / 5



SAMSUNG ELECTRONICS

AQUILA-SONOMA MAIN

DATE: 6/25/2005
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 APPROVAL: KEVIN LEE
 TITLE: ALVISO (2/5)

PART NO: BA41-00529A

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(Def.): Default Operations ▶: Current Settings

CFG#	Low	High
CFG(5)	DMIx4	DMIx4 (Def.)
CFG(6)	DDR-2	DDR-4 (Def.)
CFG(7)	DTT/Transportable	Mobile CPU (Def.)
CFG(8)	PEG Reversal	Normal (Def.)
CFG(9)	Test Mode	Normal (Def.)
CFG(10)	FSB Dynamic ODT	Enabled (def.)
CFG(11)	Disabled	VCC 1.5V (Def.)
CFG(12)	VCC 1.05V (Def.)	VCCP 1.2V
CFG(13)	SDVOCTRL_DATA	No (Def.)
CFG(14)	SDVOCTRL_DATA	No (Def.)
CFG(15)	SDVOCTRL_DATA	No (Def.)
CFG(16)	SDVOCTRL_DATA	No (Def.)

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AQUILA-SONOMA MAIN

DATE: 6/25/2005
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AQUILA-SONOMA MAIN

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AQUILA-SONOMA MAIN

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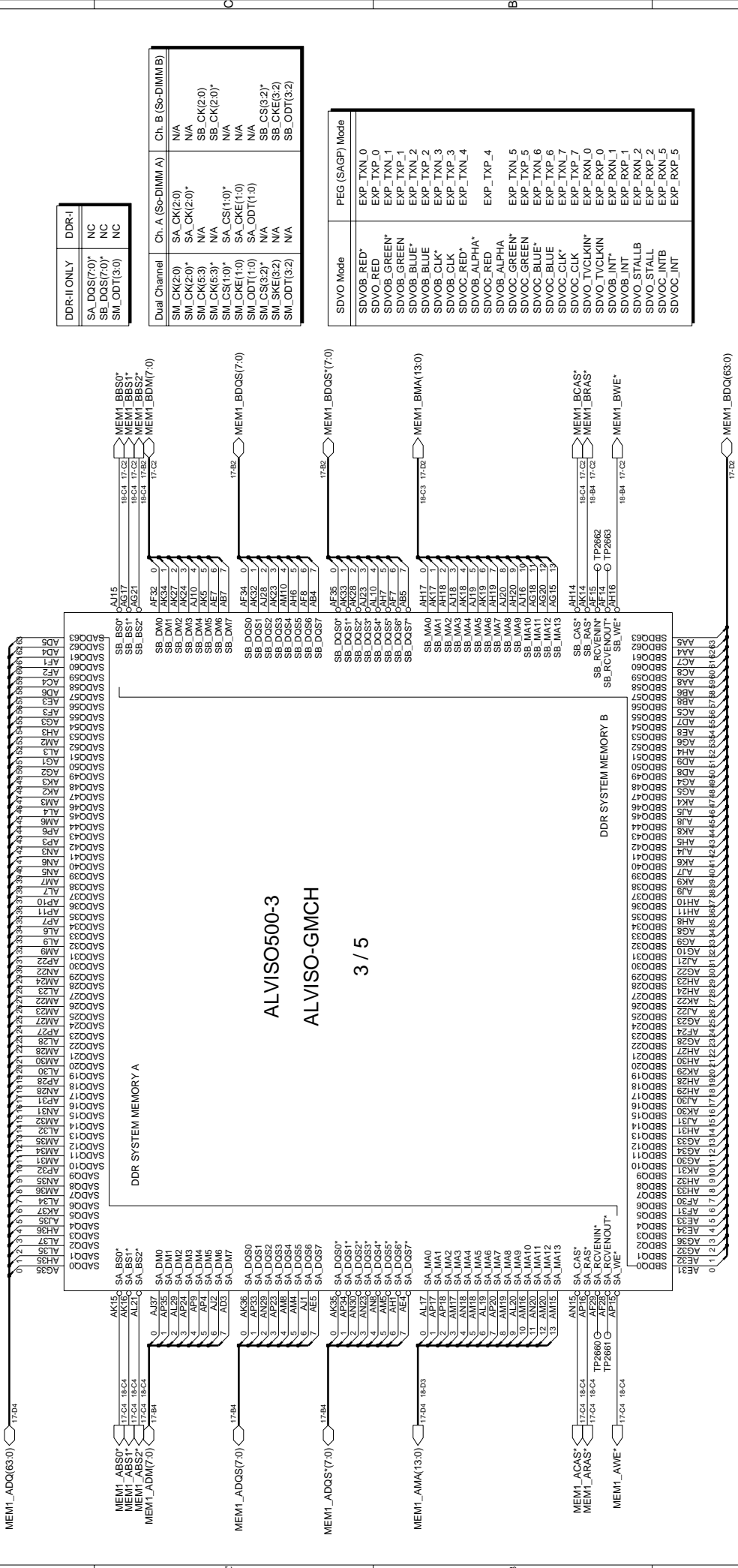
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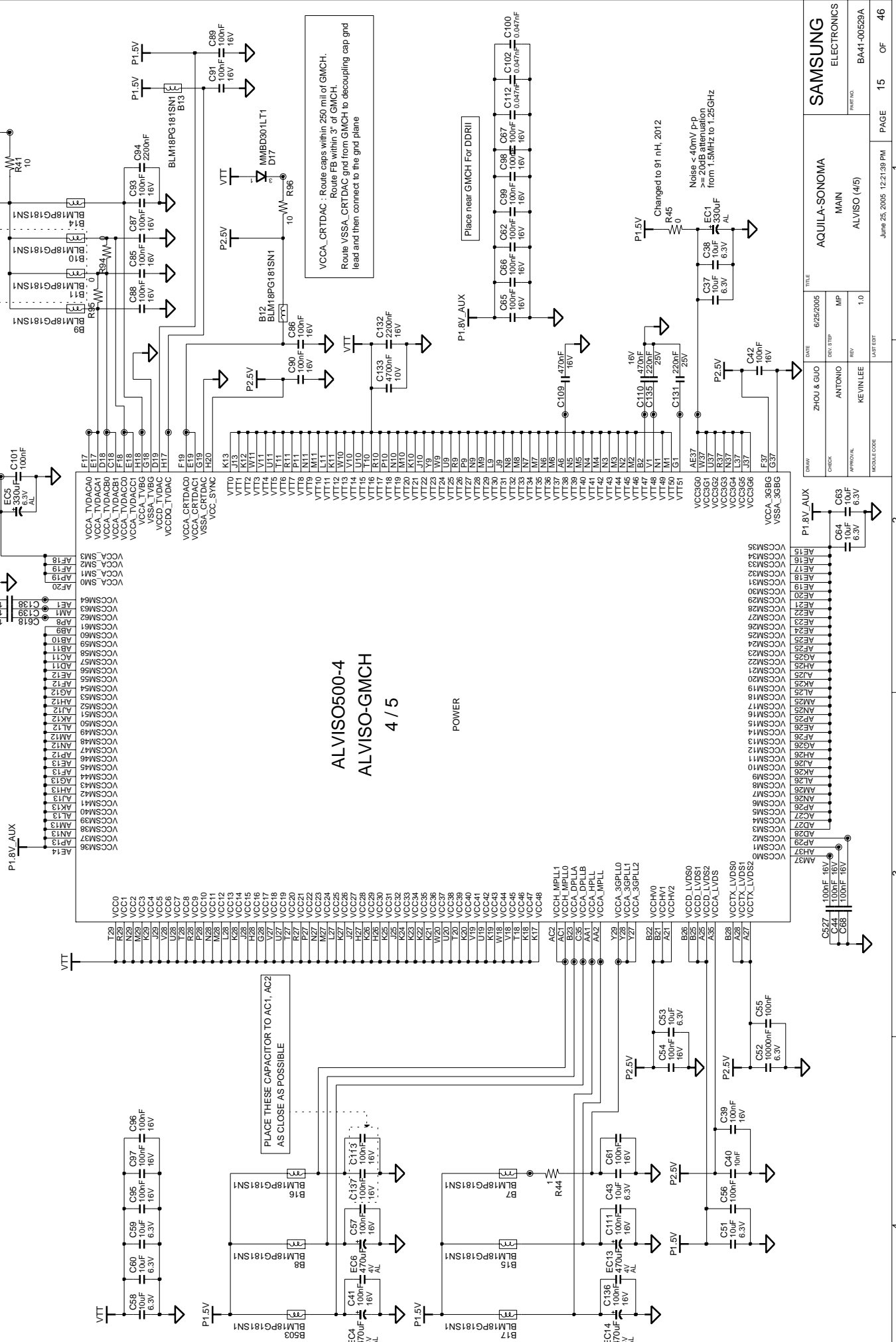
DDR-II ONLY	DDR-I
SA_BDS7(7:0)*	NC
SB_DDS7(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (Sx-DIMM A)	Ch. B (Sx-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_LCK(5:3)	N/A	SB_LCK(2:0)
SM_LCK(5:3)*	N/A	SB_LCK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_SKE(3:2)	N/A	SB_SKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SxGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVOB_RED*	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN*	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE*	EXP_TXP_2
SDVOB_BLUE*	EXP_TXN_3
SDVOB_BLUE*	EXP_TXP_3
SDVOB_ALPHA*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXP_4
SDVOB_ALPHA*	EXP_TXN_5
SDVOB_ALPHA*	EXP_TXP_5
SDVOB_ALPHA*	EXP_TXN_6
SDVOB_ALPHA*	EXP_TXP_6
SDVOB_ALPHA*	EXP_TXN_7
SDVOB_ALPHA*	EXP_TXP_7
SDVOB_ALPHA*	EXP_RXN_0
SDVOB_ALPHA*	EXP_RXP_0
SDVOB_ALPHA*	EXP_RXN_1
SDVOB_ALPHA*	EXP_RXP_1
SDVOB_ALPHA*	EXP_RXN_2
SDVOB_ALPHA*	EXP_RXP_2
SDVOB_ALPHA*	EXP_RXN_5
SDVOB_ALPHA*	EXP_RXP_5

DRAWN		DATE	6/25/2005
CHECK	ZHOU & GUO	DRW. STUP	MP
APPROVAL	ANTONIO	REV	1.0
MODULE CODE		LAST EDIT	
TITLE		PAGE 14 OF 46	
SAMSUNG ELECTRONICS		June 25, 2005 12:21:39 PM	
AQUILA-SONOMA MAIN		PART NO. BA41-00529A	
ALVISO (3E)		PAGE 14 OF 46	

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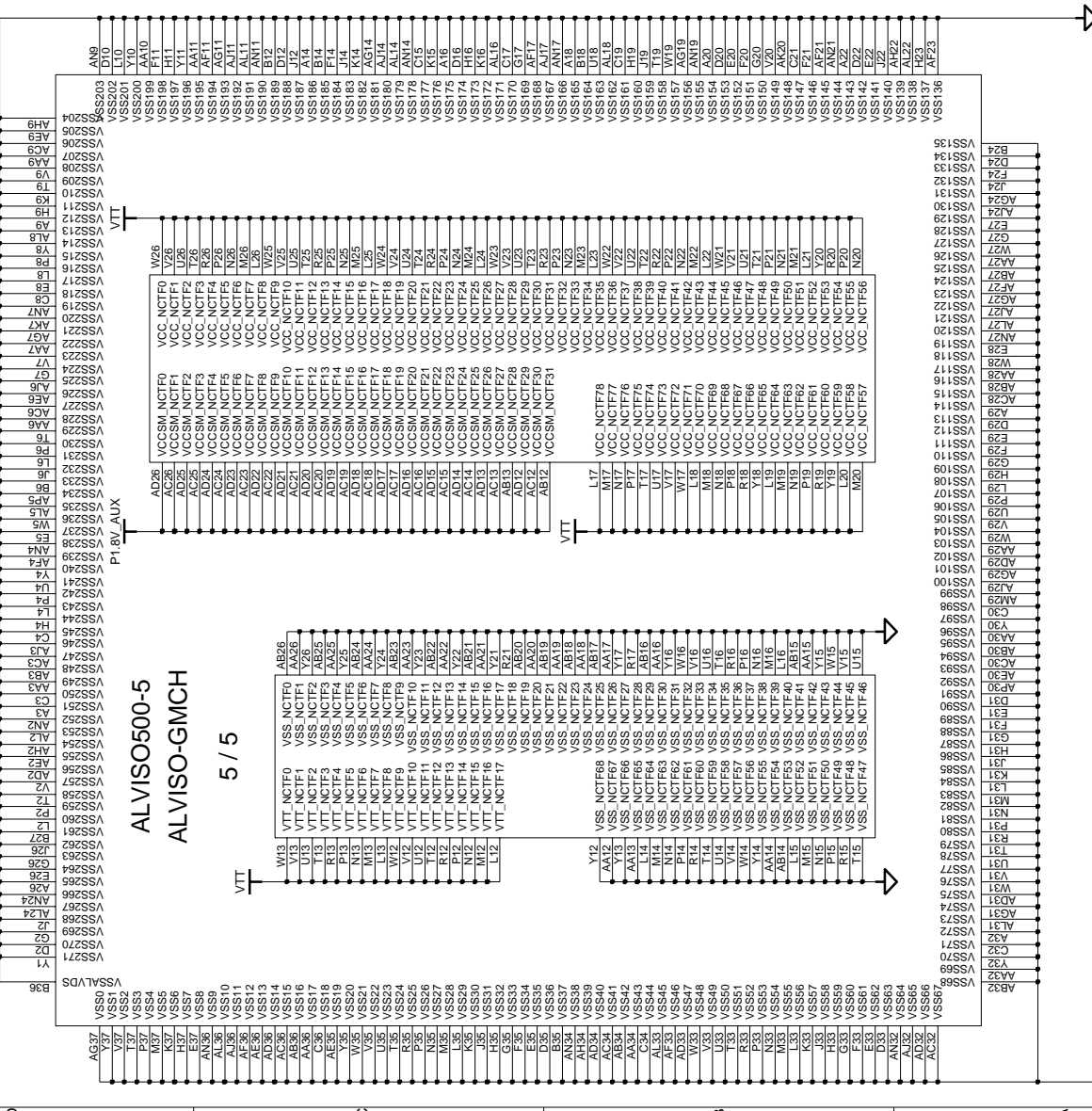


**ALVISO500-4
 ALVISO-GMCH
 4 / 5**

POWER

DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRWN	ZHOU & GUO	CHKD	ANTONIO
APPVAL	KEVIN LEE	REV	1.0
MODULE CODE		MP	MAIN
REV		APPROVAL	ALVISO (4/5)
DATE EDIT	June 25, 2005 12:21:39 PM	PAGE	15 OF 46
PART NO.	BA41-00529A	SAMSUNG ELECTRONICS	

NCTF: Non-Critical to Function
 VTT_NCTF : NCTF FSB power supply (1.05V or 1.2V)
 VCC_NCTF : NCTF Core Vcc(1.05V or 1.5V)

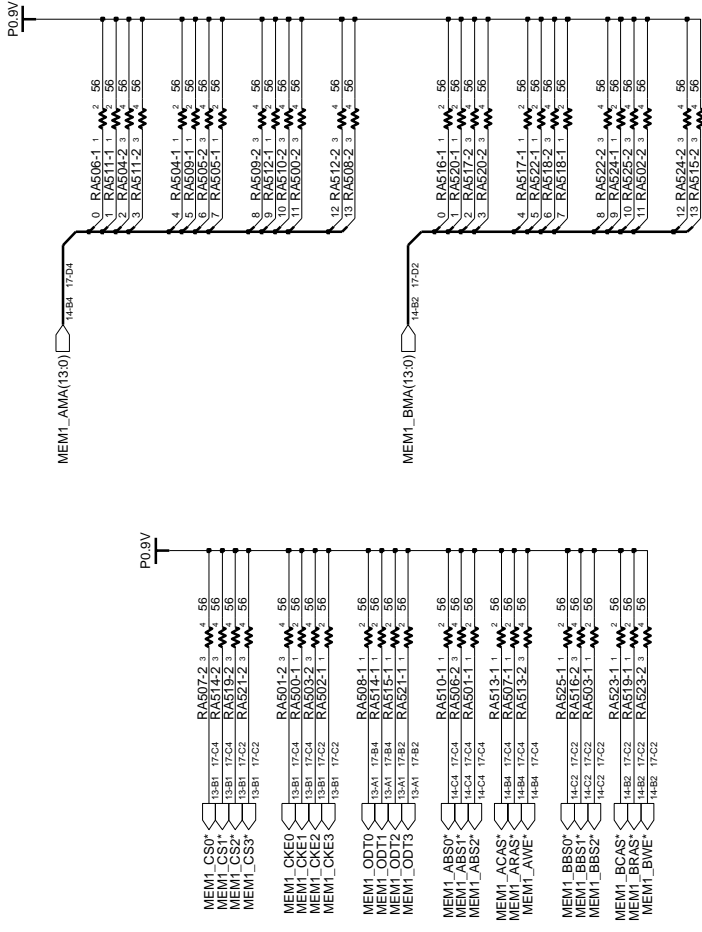


AG37	VSS0	AN8	VSS136
V37	VSS1	AN9	VSS135
V38	VSS2	AN10	VSS134
V39	VSS3	AN11	VSS133
M37	VSS4	AN12	VSS132
M38	VSS5	AN13	VSS131
K37	VSS6	AN14	VSS130
H37	VSS7	AN15	VSS129
E37	VSS8	AN16	VSS128
AN36	VSS9	AN17	VSS127
AF36	VSS10	AN18	VSS126
AS36	VSS11	AN19	VSS125
AL36	VSS12	AN20	VSS124
AD36	VSS13	AN21	VSS123
AC36	VSS14	AN22	VSS122
AA36	VSS15	AN23	VSS121
AA36	VSS16	AN24	VSS120
AA36	VSS17	AN25	VSS119
AA36	VSS18	AN26	VSS118
AE35	VSS19	AN27	VSS117
Y35	VSS20	AN28	VSS116
W35	VSS21	AN29	VSS115
V35	VSS22	AN30	VSS114
U35	VSS23	AN31	VSS113
T35	VSS24	AN32	VSS112
R35	VSS25	AN33	VSS111
Q35	VSS26	AN34	VSS110
P35	VSS27	AN35	VSS109
M35	VSS28	AN36	VSS108
K35	VSS29	AN37	VSS107
J35	VSS30	AN38	VSS106
I35	VSS31	AN39	VSS105
H35	VSS32	AN40	VSS104
G35	VSS33	AN41	VSS103
F35	VSS34	AN42	VSS102
E35	VSS35	AN43	VSS101
D35	VSS36	AN44	VSS100
C35	VSS37	AN45	VSS99
B35	VSS38	AN46	VSS98
A34	VSS39	AN47	VSS97
AA34	VSS40	AN48	VSS96
AA34	VSS41	AN49	VSS95
AA34	VSS42	AN50	VSS94
AA34	VSS43	AN51	VSS93
AA34	VSS44	AN52	VSS92
AA34	VSS45	AN53	VSS91
AA34	VSS46	AN54	VSS90
AA34	VSS47	AN55	VSS89
AA34	VSS48	AN56	VSS88
AA34	VSS49	AN57	VSS87
AA34	VSS50	AN58	VSS86
AA34	VSS51	AN59	VSS85
AA34	VSS52	AN60	VSS84
AA34	VSS53	AN61	VSS83
AA34	VSS54	AN62	VSS82
AA34	VSS55	AN63	VSS81
AA34	VSS56	AN64	VSS80
AA34	VSS57	AN65	VSS79
AA34	VSS58	AN66	VSS78
AA34	VSS59	AN67	VSS77
AA34	VSS60	AN68	VSS76
AA34	VSS61	AN69	VSS75
AA34	VSS62	AN70	VSS74
AA34	VSS63	AN71	VSS73
AA34	VSS64	AN72	VSS72
AA34	VSS65	AN73	VSS71
AA34	VSS66	AN74	VSS70
AA34	VSS67	AN75	VSS69
AA34	VSS68	AN76	VSS68
AA34	VSS69	AN77	VSS67
AA34	VSS70	AN78	VSS66
AA34	VSS71	AN79	VSS65
AA34	VSS72	AN80	VSS64
AA34	VSS73	AN81	VSS63
AA34	VSS74	AN82	VSS62
AA34	VSS75	AN83	VSS61
AA34	VSS76	AN84	VSS60
AA34	VSS77	AN85	VSS59
AA34	VSS78	AN86	VSS58
AA34	VSS79	AN87	VSS57
AA34	VSS80	AN88	VSS56
AA34	VSS81	AN89	VSS55
AA34	VSS82	AN90	VSS54
AA34	VSS83	AN91	VSS53
AA34	VSS84	AN92	VSS52
AA34	VSS85	AN93	VSS51
AA34	VSS86	AN94	VSS50
AA34	VSS87	AN95	VSS49
AA34	VSS88	AN96	VSS48
AA34	VSS89	AN97	VSS47
AA34	VSS90	AN98	VSS46
AA34	VSS91	AN99	VSS45
AA34	VSS92	AN100	VSS44
AA34	VSS93	AN101	VSS43
AA34	VSS94	AN102	VSS42
AA34	VSS95	AN103	VSS41
AA34	VSS96	AN104	VSS40
AA34	VSS97	AN105	VSS39
AA34	VSS98	AN106	VSS38
AA34	VSS99	AN107	VSS37
AA34	VSS100	AN108	VSS36
AA34	VSS101	AN109	VSS35
AA34	VSS102	AN110	VSS34
AA34	VSS103	AN111	VSS33
AA34	VSS104	AN112	VSS32
AA34	VSS105	AN113	VSS31
AA34	VSS106	AN114	VSS30
AA34	VSS107	AN115	VSS29
AA34	VSS108	AN116	VSS28
AA34	VSS109	AN117	VSS27
AA34	VSS110	AN118	VSS26
AA34	VSS111	AN119	VSS25
AA34	VSS112	AN120	VSS24
AA34	VSS113	AN121	VSS23
AA34	VSS114	AN122	VSS22
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AA34	VSS118	AN126	VSS18
AA34	VSS119	AN127	VSS17
AA34	VSS120	AN128	VSS16
AA34	VSS121	AN129	VSS15
AA34	VSS122	AN130	VSS14
AA34	VSS123	AN131	VSS13
AA34	VSS124	AN132	VSS12
AA34	VSS125	AN133	VSS11
AA34	VSS126	AN134	VSS10
AA34	VSS127	AN135	VSS9
AA34	VSS128	AN136	VSS8
AA34	VSS129	AN137	VSS7
AA34	VSS130	AN138	VSS6
AA34	VSS131	AN139	VSS5
AA34	VSS132	AN140	VSS4
AA34	VSS133	AN141	VSS3
AA34	VSS134	AN142	VSS2
AA34	VSS135	AN143	VSS1
AA34	VSS136	AN144	VSS0

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 ALVISO-GMCH
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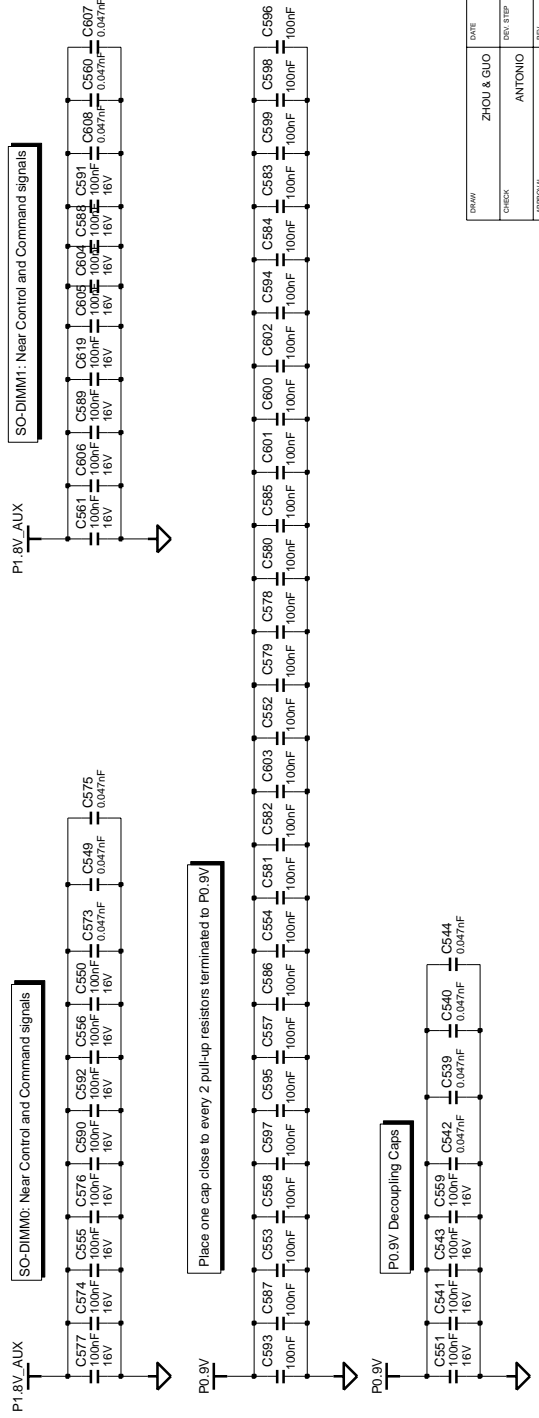
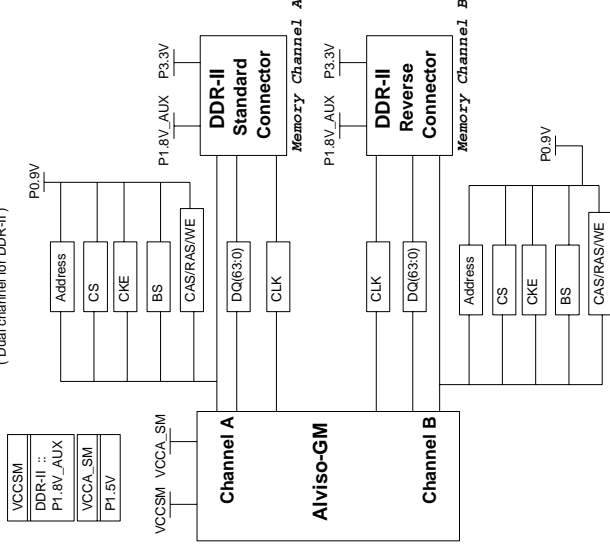
DRAWN		TITLE	
ZHOU & GUO	6/25/2005	AQUILA-SONOMA	
CHKD	ANTONIO	MAIN	
APPROVAL	KEVIN LEE	ALVISO (5/5)	
DATE	REV	DATE	REV
6/25/2005	1.0	6/25/2005	1.0
DESIGNER	ANTONIO	DATE	6/25/2005
CHECKER	ANTONIO	REV	1.0
APPROVAL	KEVIN LEE	DATE	6/25/2005
DATE	6/25/2005	TIME	12:21:39 PM
REV	1.0	PAGE	16
REV	1.0	OF	46
REV	1.0	PART NO	BA41-00529A
REV	1.0	COMP	ELECTRONICS
REV	1.0	COMP	SAMSUNG

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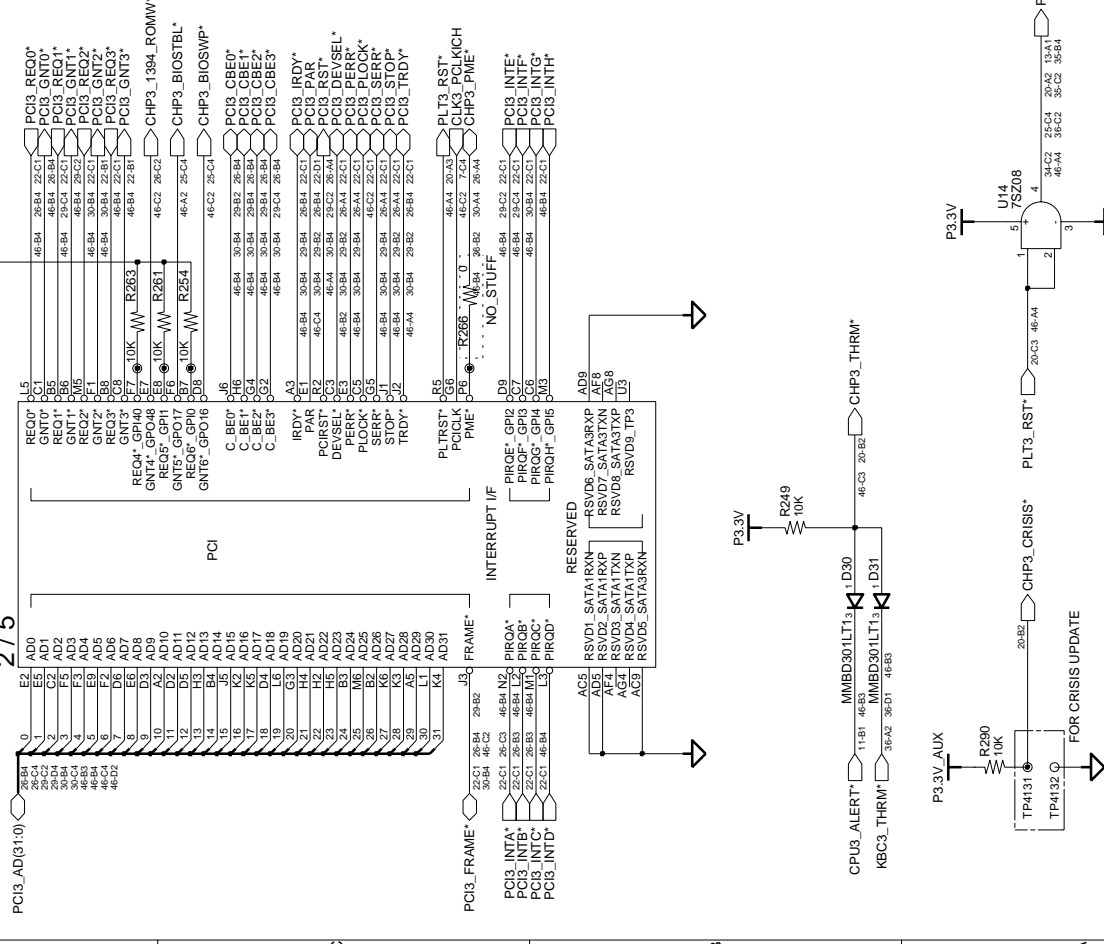
Memory Topology

(Dual channel for DDR-II)

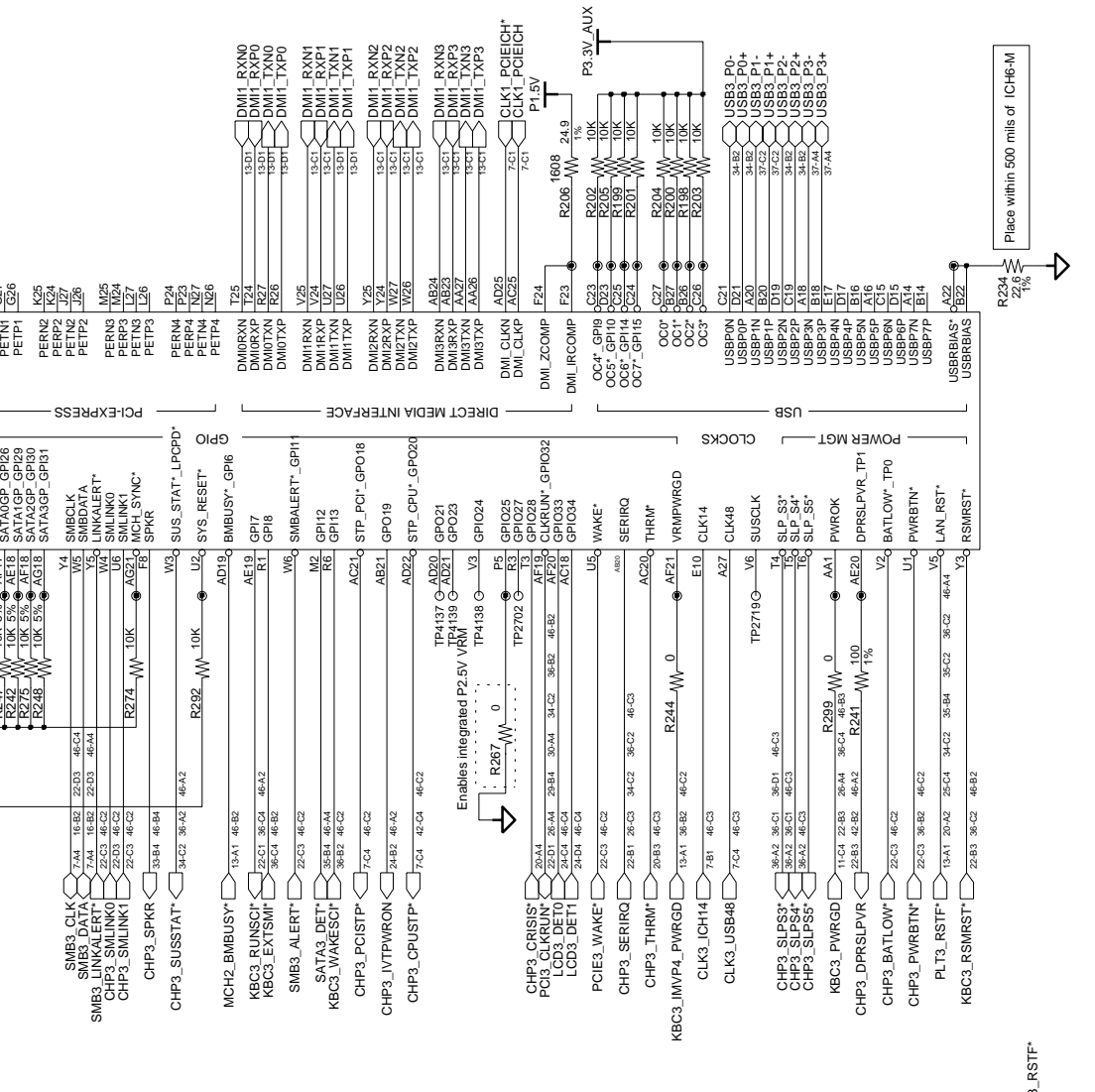


DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRWN	ZHOU & GUO	CHKD	ANTONIO
REV	1.0	MP	MP
APPROVAL	KEVIN LEE	REV	KEVIN LEE
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
		PAGE	18
		OF	46
		SAMSUNG ELECTRONICS	
		PART NO. BA41-00529A	

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82801FBM
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82801FBM
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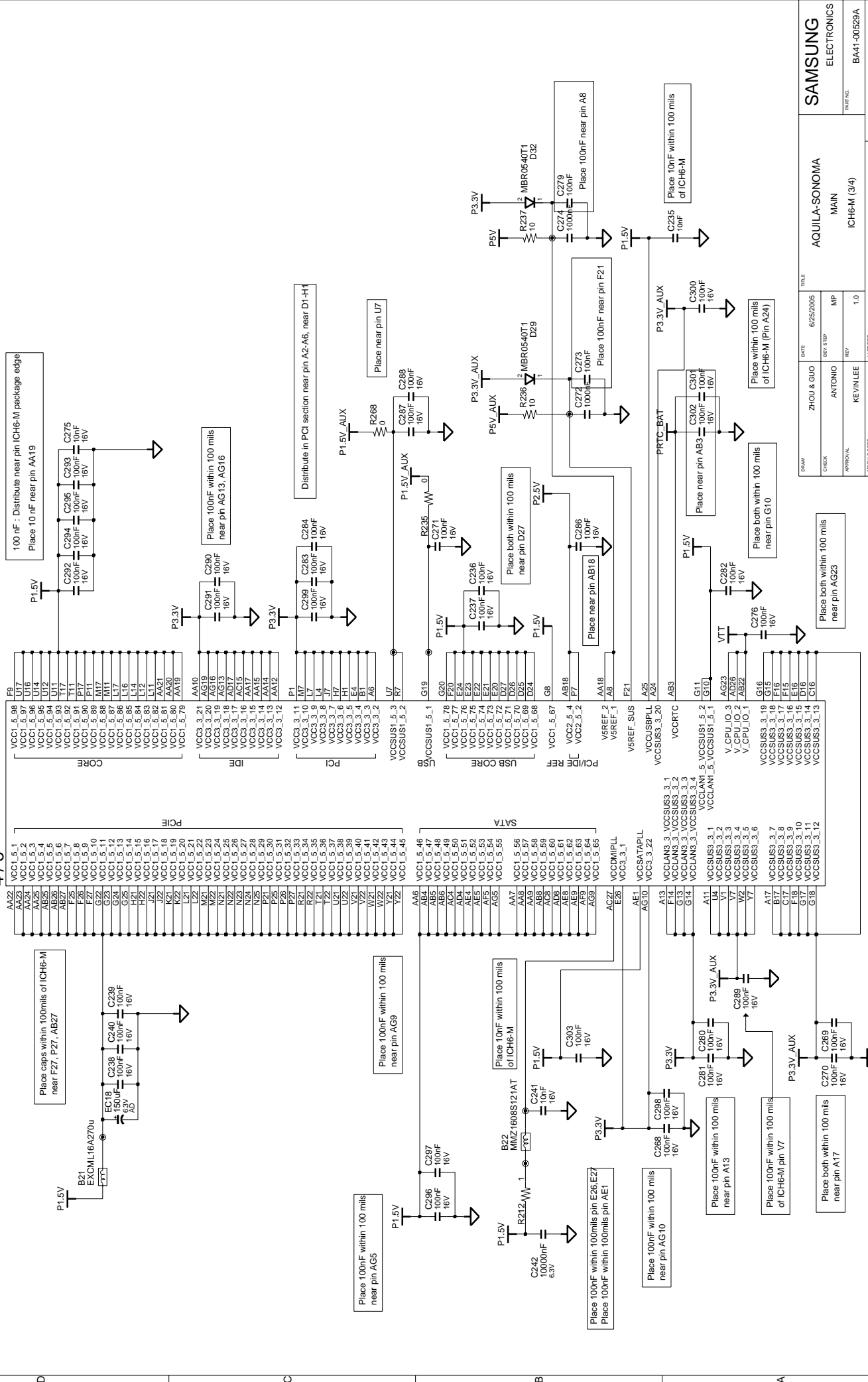


DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRWN	ZHOU & GUO	REV	MP
CHECK	ANTONIO	REV	MP
APPROVAL	KEVINLEE	REV	1.0
MIDDLE CODE		DATE	June 25, 2005 12:21:39 PM
		PAGE	20
		OF	46
SAMSUNG ELECTRONICS PART NO. BA41-00529A IC#6-M (2/4) MAIN			

DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRWN	ZHOU & GUO	REV	MP
CHECK	ANTONIO	REV	MP
APPROVAL	KEVINLEE	REV	1.0
MIDDLE CODE		DATE	June 25, 2005 12:21:39 PM
		PAGE	20
		OF	46
SAMSUNG ELECTRONICS PART NO. BA41-00529A IC#6-M (2/4) MAIN			

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U513-4
82801FBM



Place 100 nF : Distribute near pin ICH6-M package edge
Place 10 nF near pin AA19

Place 100nF within 100 mils near pin AG13, AG16

Place 100nF within 100 mils near pin AG9

Distribute in PCI section near pin A2-A6, near D1-H1

Place 100nF within 100 mils near pin AG5

Place 100nF within 100 mils near pin AG9

Place 100nF within 100 mils near pin AG5

Place 100nF within 100 mils of ICH6-M

Place 100nF within 100 mils near pin AG10

Place 100nF within 100mils pin E26,E27

Place 100nF within 100 mils near pin A13

Place 100nF within 100 mils of ICH6-M pin V7

Place both within 100 mils near pin A17

Place 100nF within 100 mils near pin AG23

Place both within 100 mils near pin G10

Place 100nF near pin AB18

Place 100nF near pin D27

Place both within 100 mils near pin AB8

Place 100nF near pin F21

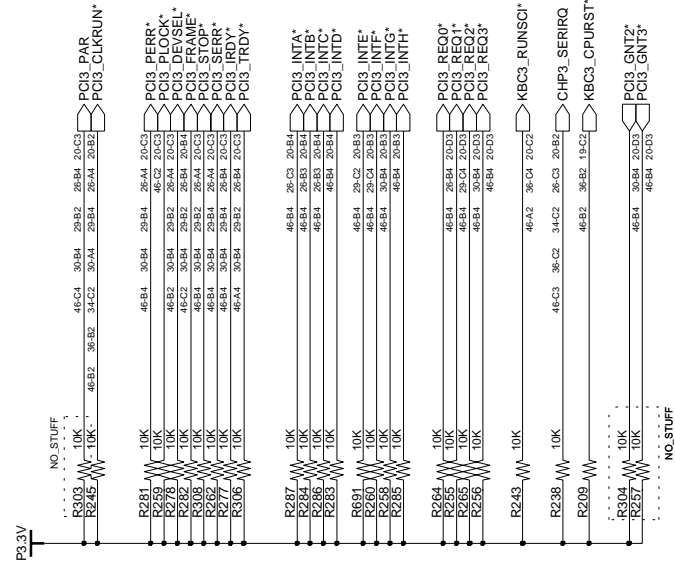
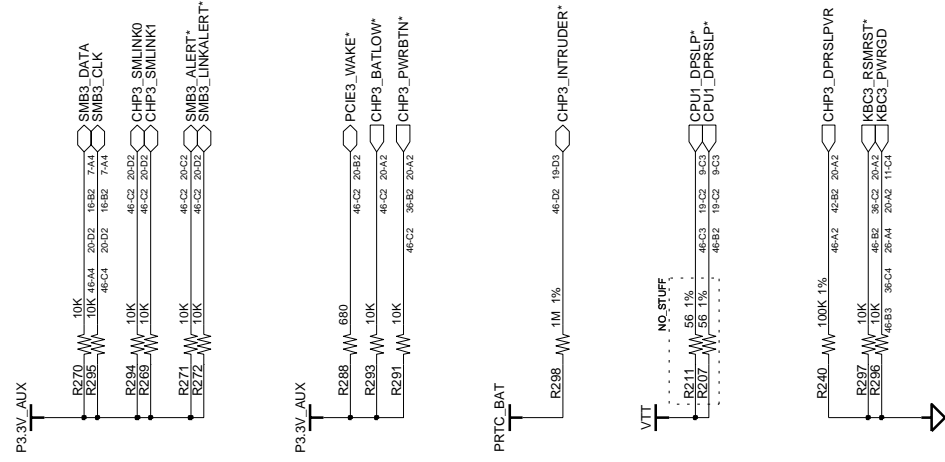
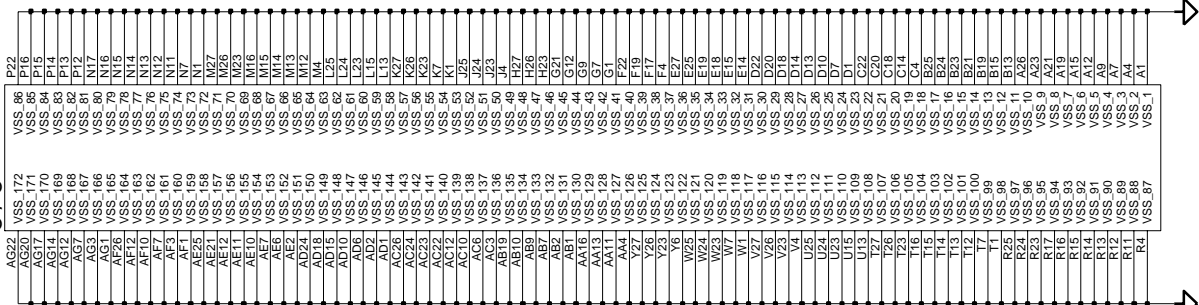
Place 100nF within 100 mils of ICH6-M

Place 100nF within 100 mils near pin A24

SAMSUNG ELECTRONICS		PART NO. BA41-00529A
AQUILA-SONOMA MAIN		IC16-M (3/4)
DATE	6/25/2005	REV
DRAWN	ZHOU & GUO	CHKD
CHECK	ANTONIO	MP
APPROVAL	KEVIN LEE	REV
MODULE CODE	1.0	LAYER
DATE	June 25, 2005 12:21:39 PM	PAGE
	21	OF
	46	

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82801FBM
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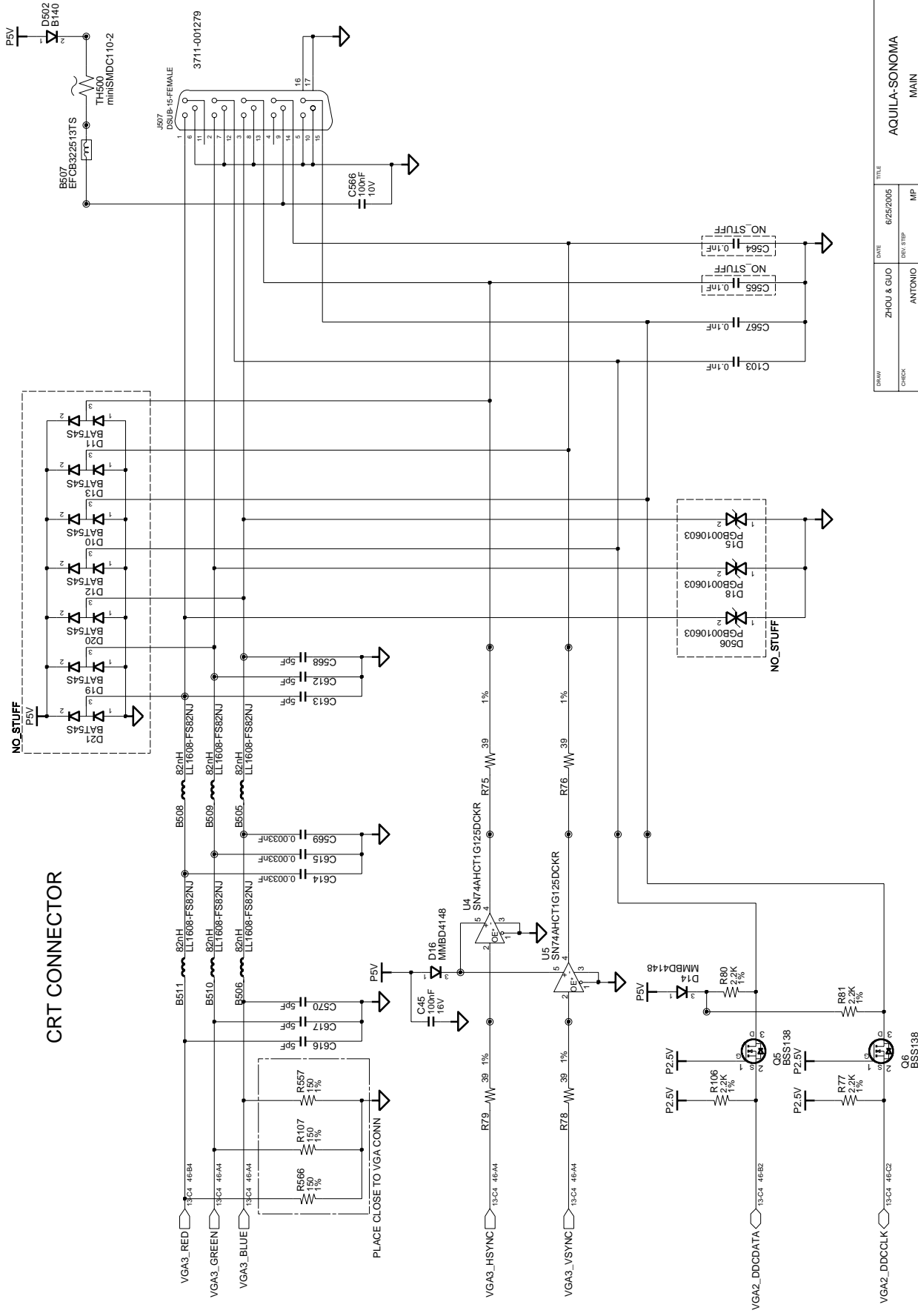
ICH6-M Strapping Options

Function	Default
CHP3_SPKR	No Reboot
CHP3_BIOSWP*	Boot BIOS
PC/PCI_GNTA*	A16 swap override
AC97_SDOUT	Safe Mode
EEP_DOUT	TBD

DRAWN	ZHOU & GUO	DATE	6/25/2005	TITLE	AQUILA-SONOMA
CHECK	ANTONIO	DRW. STEP	MP		MAIN
APPROVAL	KEVIN LEE	REV	1.0		ICH6-M (4/4)
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM	PAGE	22 OF 46

SAMSUNG ELECTRONICS	
PART NO.	BA41-00529A

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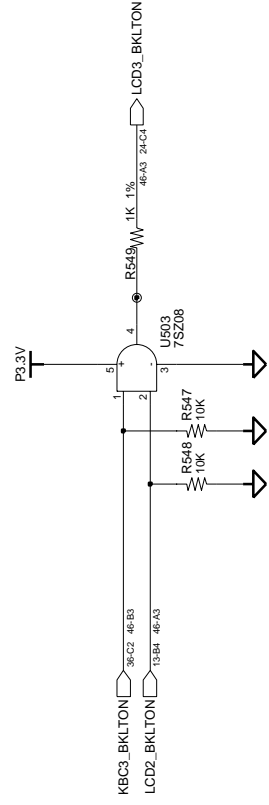
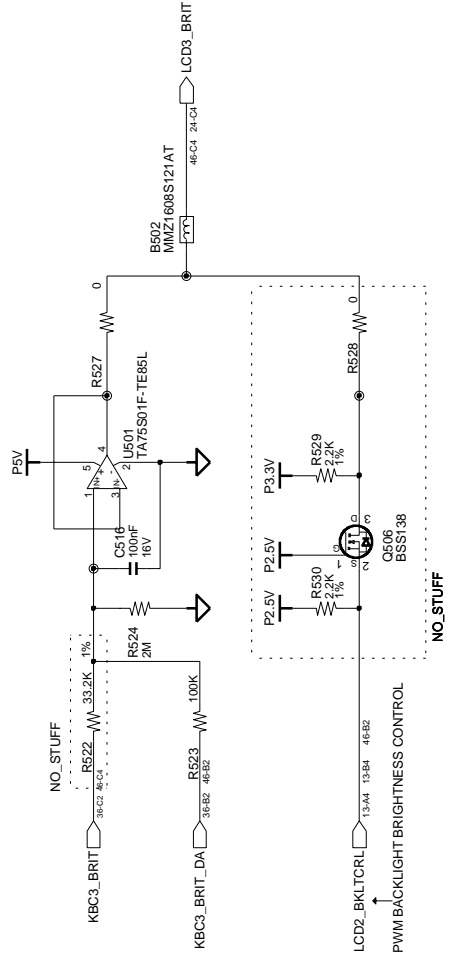
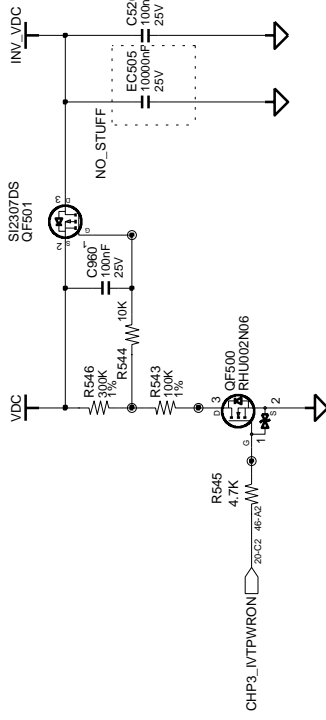
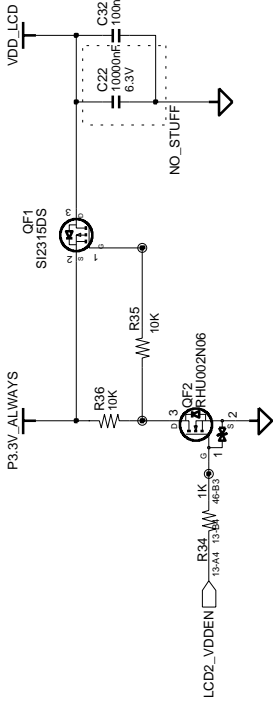
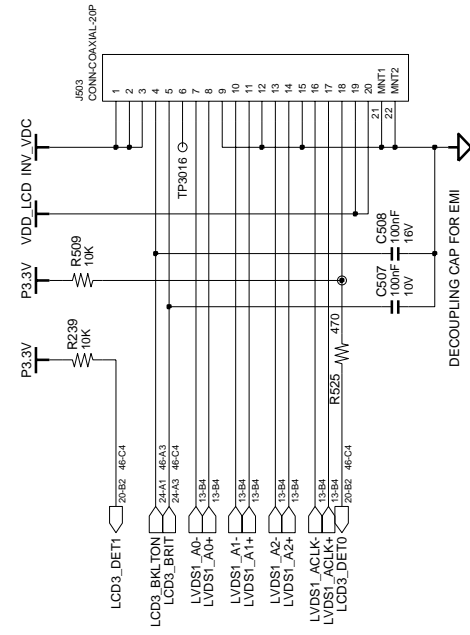
CRT CONNECTOR

DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRWN	ZHOU & GUO	DRW. STEP	MP
CHECK	ANTONIO	REV	1.0
APPROVAL	KEVIN LEE	LAST EDIT	June 25, 2005 12:21:39 PM
MODULE CODE		PAGE	23 OF 46
			SAMSUNG X06 925

DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRWN	ZHOU & GUO	DRW. STEP	MP
CHECK	ANTONIO	REV	1.0
APPROVAL	KEVIN LEE	LAST EDIT	June 25, 2005 12:21:39 PM
MODULE CODE		PAGE	23 OF 46
			SAMSUNG X06 925

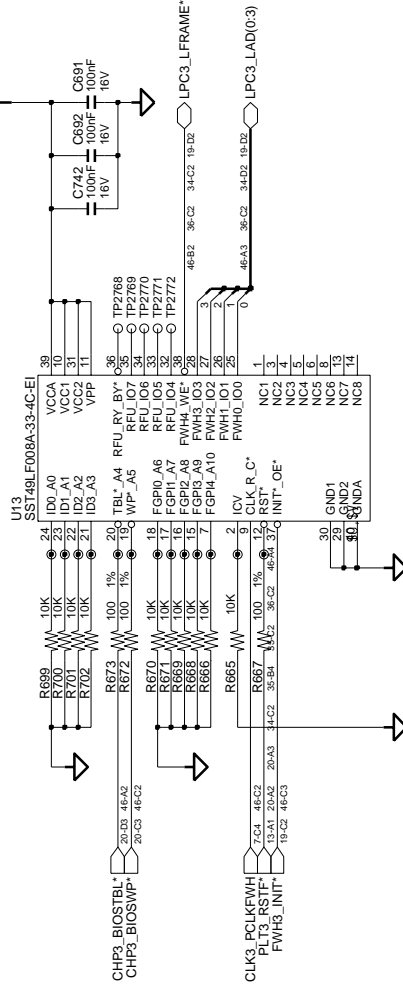
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XGA LCD CONNECTOR



DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRW	ZHOU & GUO	CHK	ANTONIO
REV	1.0	MP	MP
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		REV	1.0
		DATE	June 25, 2005 12:21:39 PM
		PAGE	24 OF 46
		PART NO.	BA41-00529A
		MANUFACTURER	SAMSUNG ELECTRONICS
		DESCRIPTION	LCD CONNECTOR

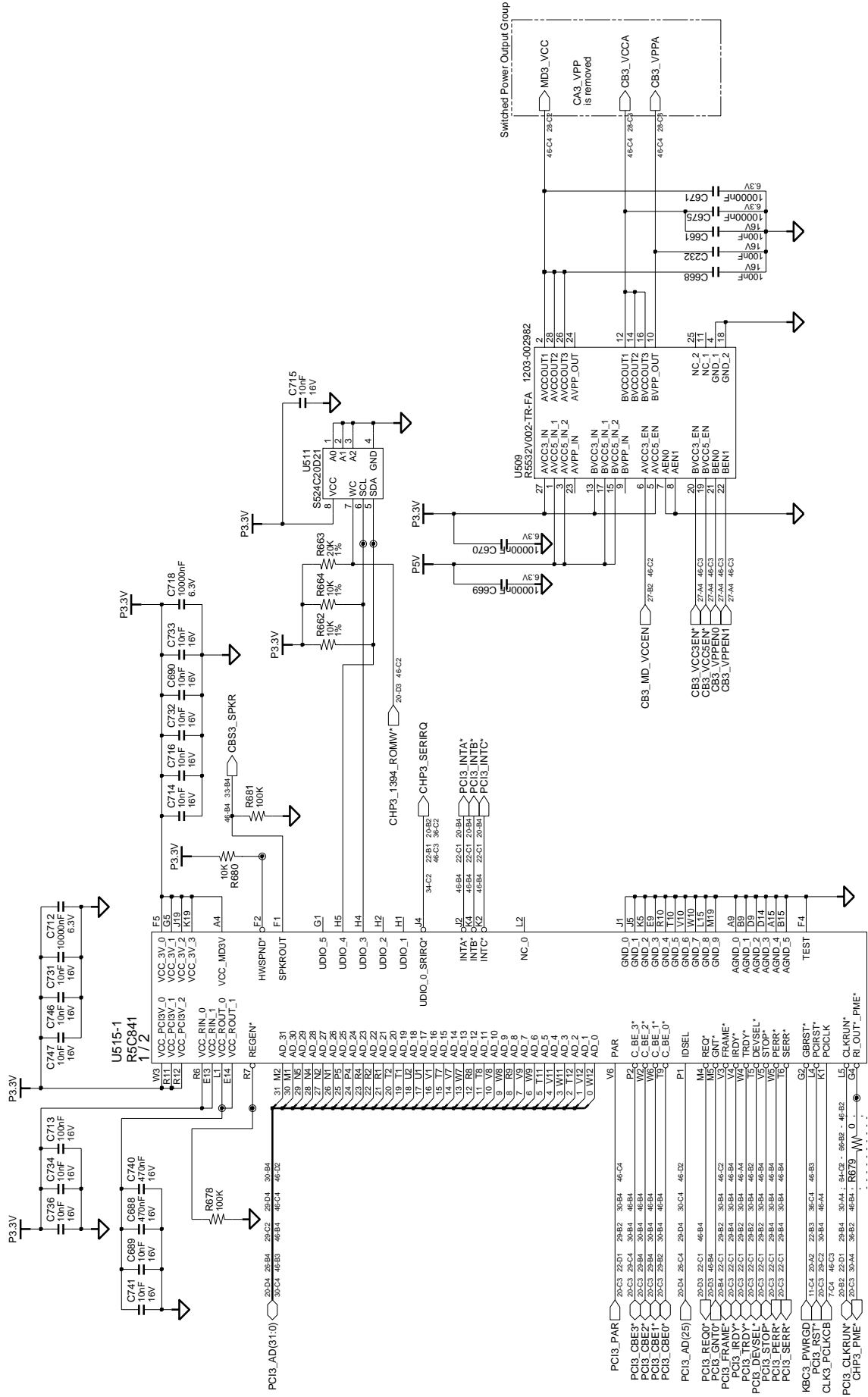
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02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT. EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPY/RIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT'9
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
4A	INIT. ALL VIDEO BIOS ROM	D2	UNKNOWN INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
50	DISPLAY CPU TYPE AND SPEED	D6	SHUTDOWN 5
52	TEST KEYBOARD	D8	SHUTDOWN ERROR
54	SET KEYCLICK IF ENABLED	DA	EXTENDED BLOCK MOVE
56	ENABLE KEYBOARD	DC	SHUTDOWN 10
58	TEST FOR UNEXPECTED INTERRUPTS	89	ENABLE NMI
5A	DISPLAY * PRESS SETUP*	90	INIT. HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	91	INIT. LOCAL BUS HDD CONTROLLER
60	TEST EXTENDED MEMORY	92	JUMP TO USER PATCH 2
62	TEST EXTENDED MEMORY ADDRESS LINE	94	DISABLE A20 ADDRESS LINE
64	JUMP TO USER PATCH 1	96	CLEAR HUGE ES SEGMENT REG.
		98	SEARCH FOR OPTION ROMS

DRAWN		DATE		TITLE	
ZHOU & GUO		6/25/2005		AQUILA-SONOMA	
CHECK	ANTONIO	REV. STEP	MP	MAIN	
APPROVAL	KEVIN LEE	REV	1.0	FWH	
MODULE CODE		LAST EDIT		June 25, 2005 12:21:39 PM	
SAMSUNG ELECTRONICS			PAGE	25	OF 46
PART NO. BA41-00529A					

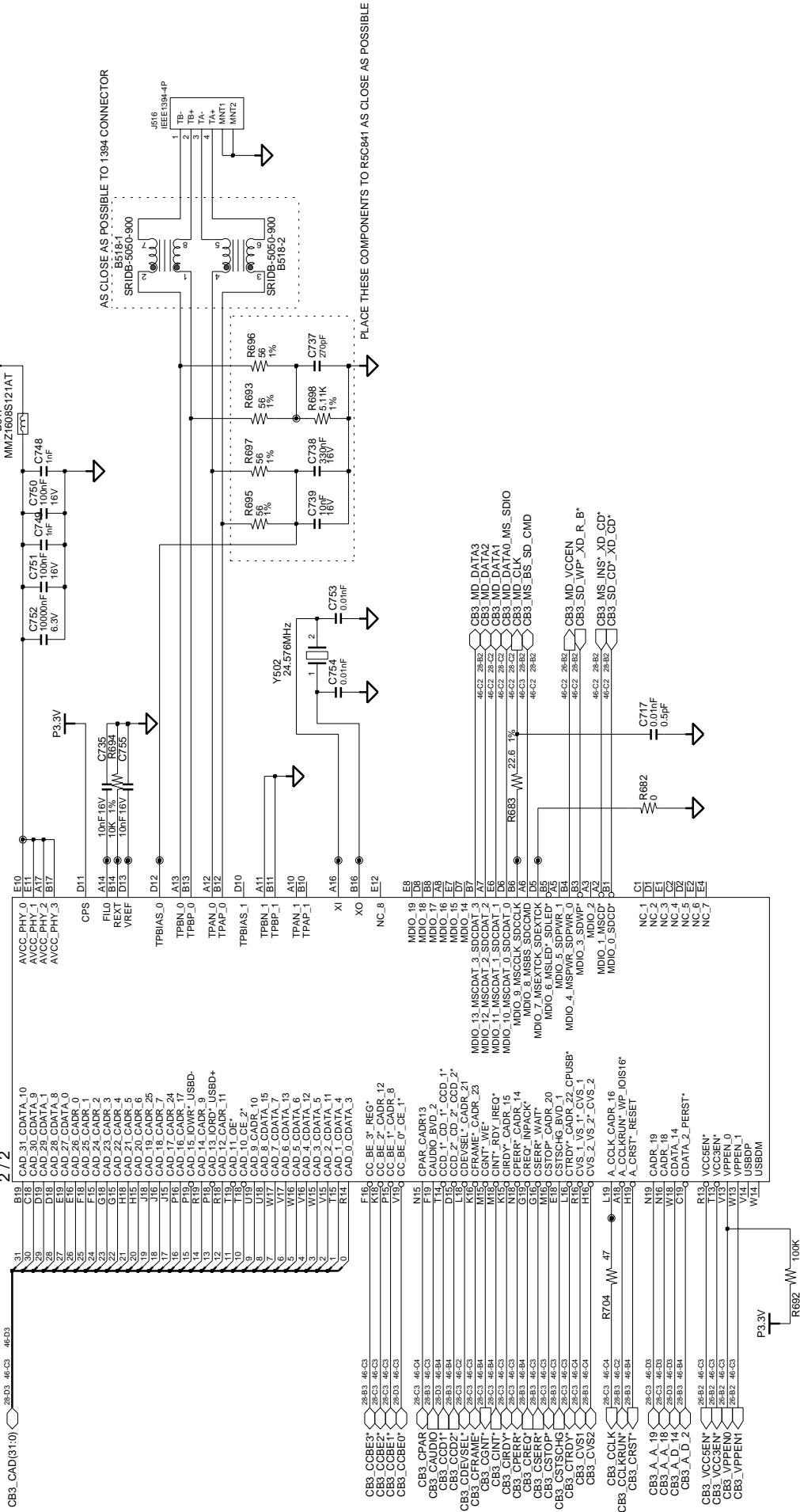
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DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRWN	ZHOU & GUO	REV	1.0
CHECK	ANTONIO	MP	
APPROVAL	KEVIN LEE		
MODULE CODE			
PAGE	26	OF	46
		SAMSUNG ELECTRONICS	
		PART NO. BA41-00529A	
		M3000	
		CARD BUS (1/2) & 1394	
		MAIN	
		June 25, 2005 12:21:39 PM	

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U515-2
R5C841
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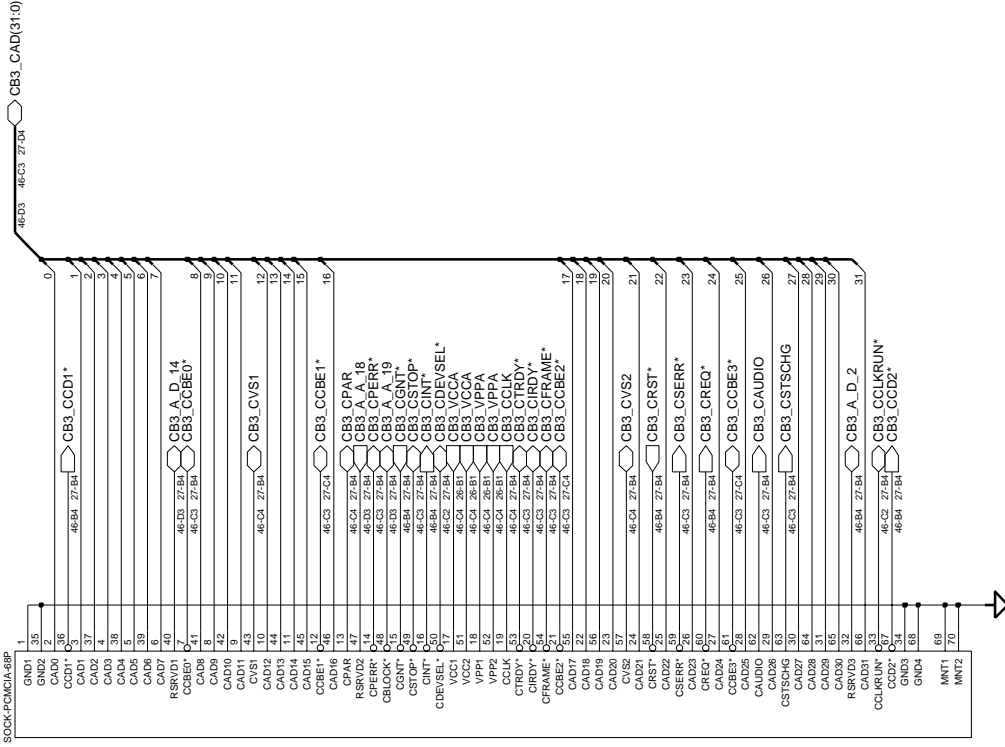


DATE	6/25/2005	TITLE	AQUILA-SONOMA MAIN
DRAWN	ZHOU & GUO	CHKD	ANTONIO
CHECK	ANTONIO	MP	MP
APPROVAL	KEVIN LEE	REV	1.0
PART NO.	BA41-00529A	PAGE	27 OF 46
MODULE CODE	CARDBUS (22)	DATE	June 25, 2005 12:21:39 PM
LAST EDIT			

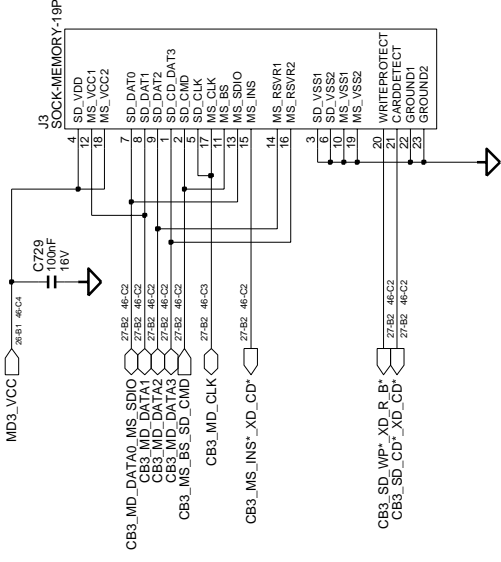
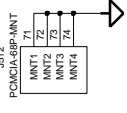
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DRAWN	ZHOU & GUO	CHKD	ANTONIO
CHECK	ANTONIO	MP	MP
APPROVAL	KEVIN LEE	REV	1.0
PART NO.	BA41-00529A	PAGE	27 OF 46
MODULE CODE	CARDBUS (22)	DATE	June 25, 2005 12:21:39 PM
LAST EDIT			

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JE13
 SOCK-PCMCIA58P



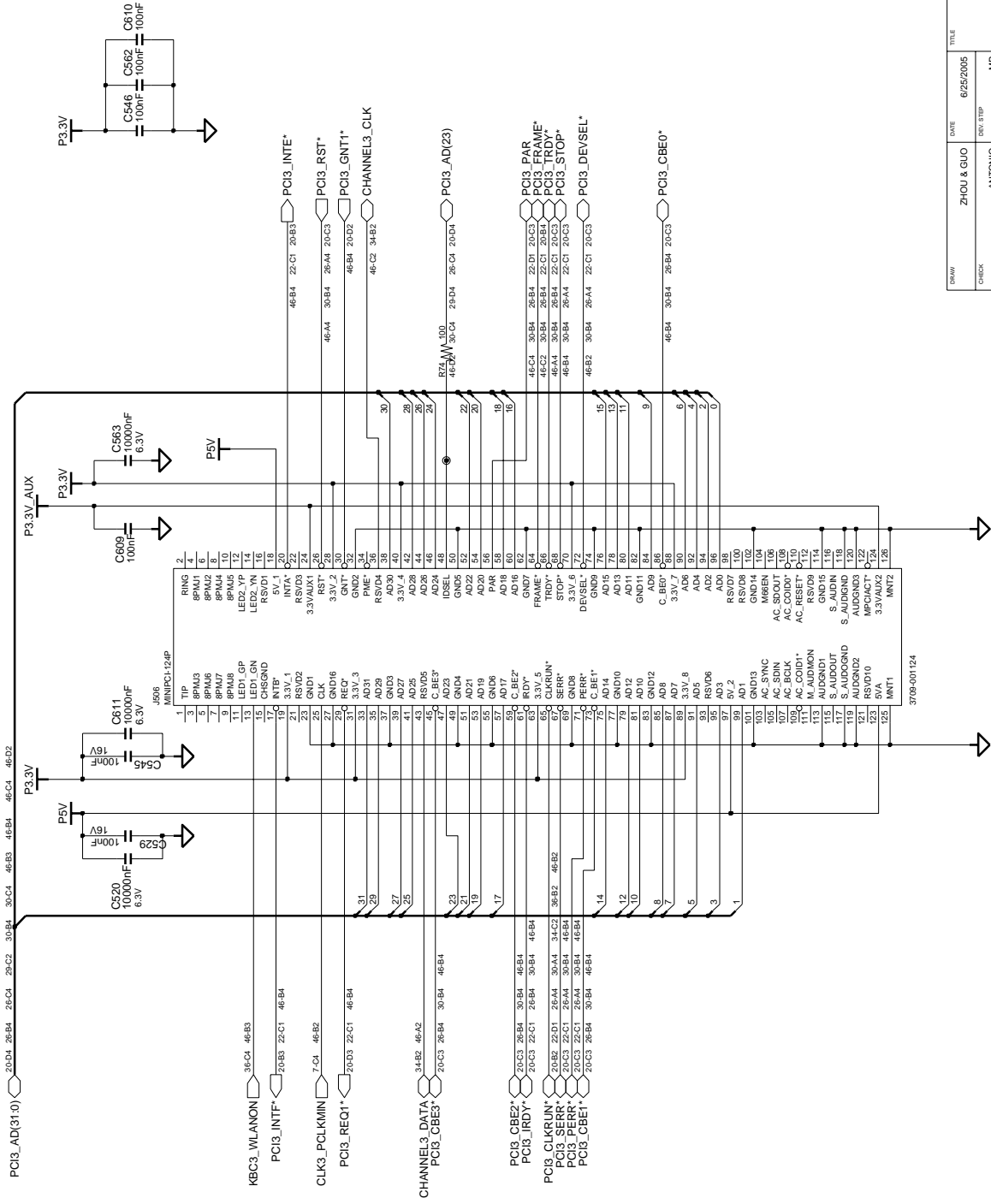
PCMCIA SOCKET BODY



DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRAWN	ZHOU & GUO	REV	MP
CHECK	ANTONIO	REV	1.0
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
SAMSUNG ELECTRONICS		PART NO. BA41-00529A	
POMC1A / MEDIA CARD SOCKET		PAGE	28 OF 46

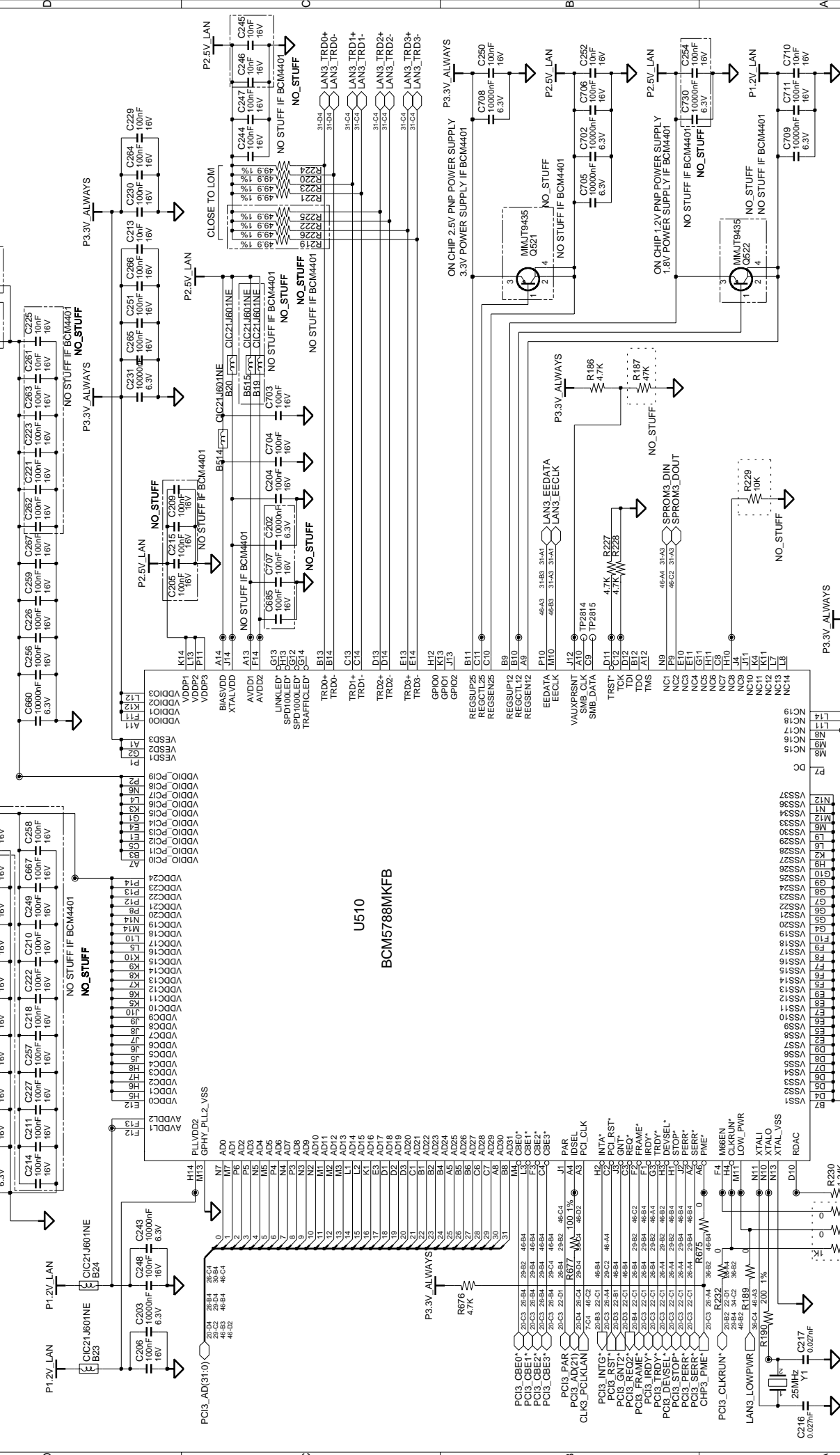
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DATE	6/25/2005	TITLE	AQUILA-SONOMA
CHK	ANTONIO	REV	1.0
APP	KEVIN LEE	DATE	June 25, 2005 12:21:39 PM
DESIGNER	ZHOU & GUO	MODULE CODE	
CHECKER	ANTONIO	MP	
APPROVAL	KEVIN LEE	REV	1.0
DATE	6/25/2005	DATE	6/25/2005
CHK	ANTONIO	CHK	ANTONIO
APP	KEVIN LEE	APP	KEVIN LEE
DESIGNER	ZHOU & GUO	DESIGNER	ZHOU & GUO
CHECKER	ANTONIO	CHECKER	ANTONIO
APPROVAL	KEVIN LEE	APPROVAL	KEVIN LEE
DATE	6/25/2005	DATE	6/25/2005
CHK	ANTONIO	CHK	ANTONIO
APP	KEVIN LEE	APP	KEVIN LEE
DESIGNER	ZHOU & GUO	DESIGNER	ZHOU & GUO
CHECKER	ANTONIO	CHECKER	ANTONIO
APPROVAL	KEVIN LEE	APPROVAL	KEVIN LEE
DATE	6/25/2005	DATE	6/25/2005
CHK	ANTONIO	CHK	ANTONIO
APP	KEVIN LEE	APP	KEVIN LEE
DESIGNER	ZHOU & GUO	DESIGNER	ZHOU & GUO
CHECKER	ANTONIO	CHECKER	ANTONIO
APPROVAL	KEVIN LEE	APPROVAL	KEVIN LEE
DATE	6/25/2005	DATE	6/25/2005
CHK	ANTONIO	CHK	ANTONIO
APP	KEVIN LEE	APP	KEVIN LEE
DESIGNER	ZHOU & GUO	DESIGNER	ZHOU & GUO
CHECKER	ANTONIO	CHECKER	ANTONIO
APPROVAL	KEVIN LEE	APPROVAL	KEVIN LEE

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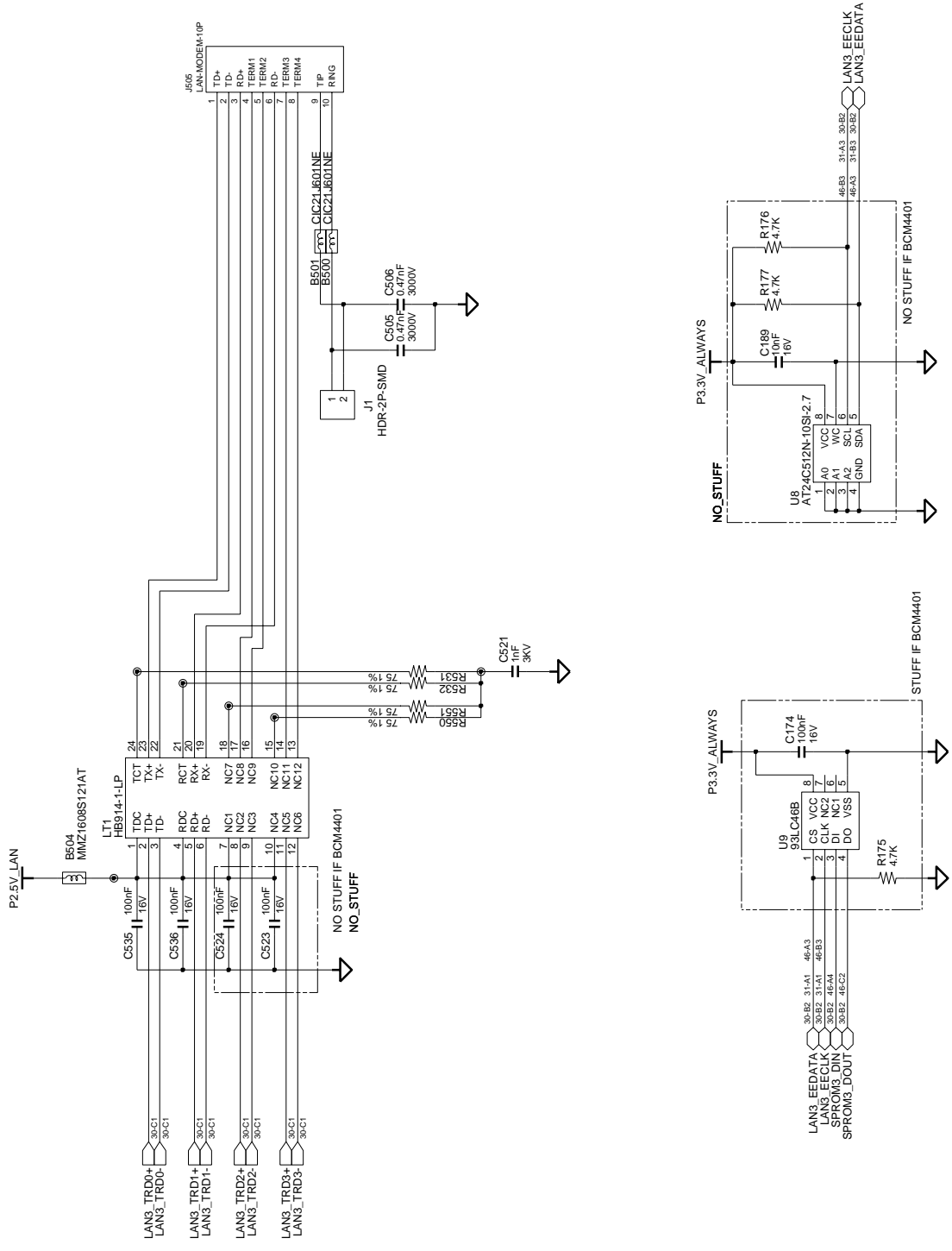


DATE	TITLE	
6/25/2005	AQUILA-SONOMA	
DRAWN	CHECK	APPROVAL
ZHOU & GUO	ANTONIO	KEVIN LEE
ENV. STEP	REV	MODULE CODE
MP	1.0	LOM (1/2)
MAIN		

SAMSUNG		ELECTRONICS	
PART NO. BA41-00529A			
DATE	TITLE	ENV. STEP	REV
6/25/2005	AQUILA-SONOMA	MP	1.0
MAIN			
LOM (1/2)			
DRAWN	CHECK	APPROVAL	MODULE CODE
ZHOU & GUO	ANTONIO	KEVIN LEE	

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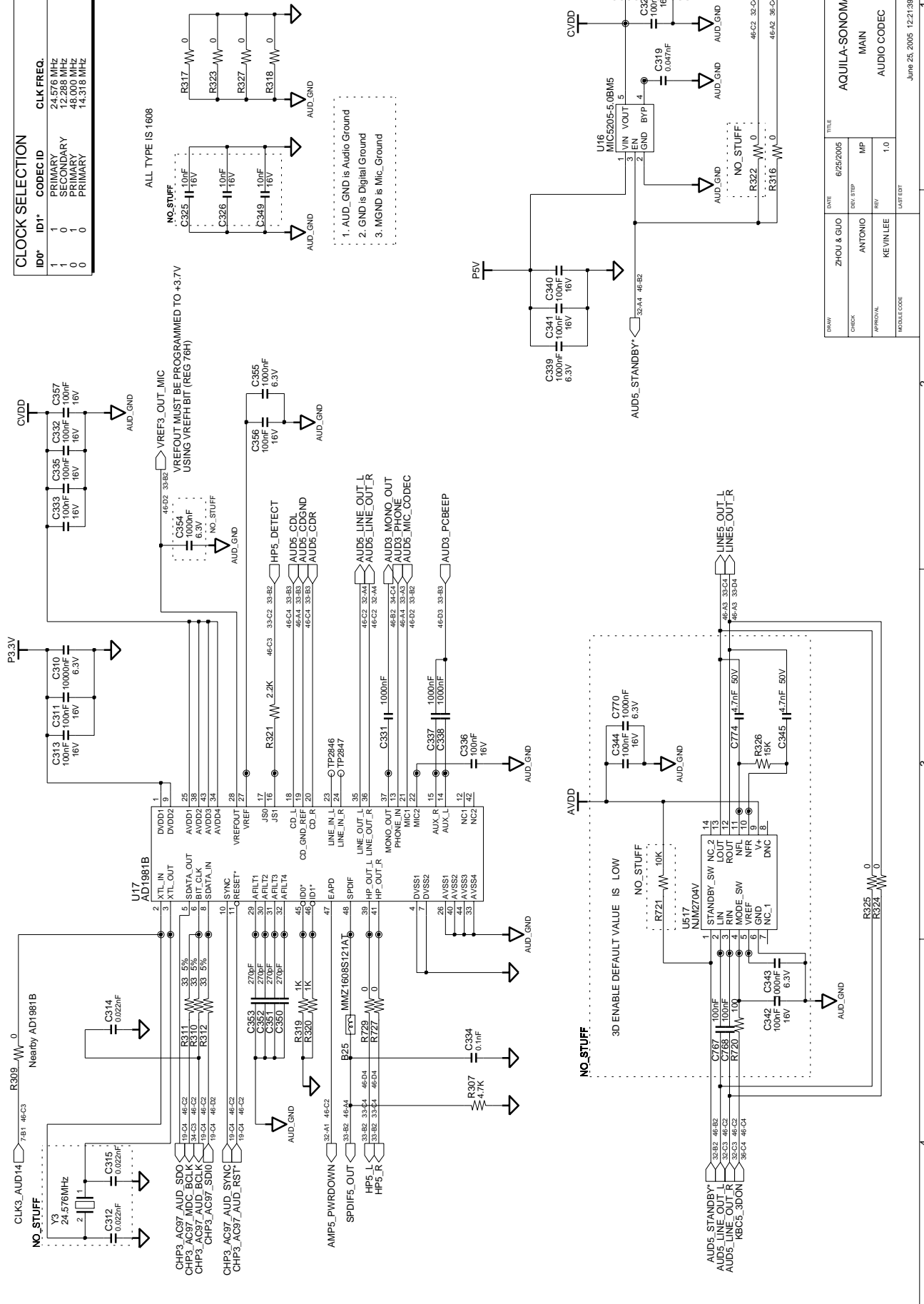


DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRAWN	ZHOU & GUO	REV. STEP	MP
CHECK	ANTONIO	REV.	KEVIN LEE
APPROVAL		REV.	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
		PAGE	31 OF 46
		PART NO.	BA41-00529A
			MAIN LOM (2/2)

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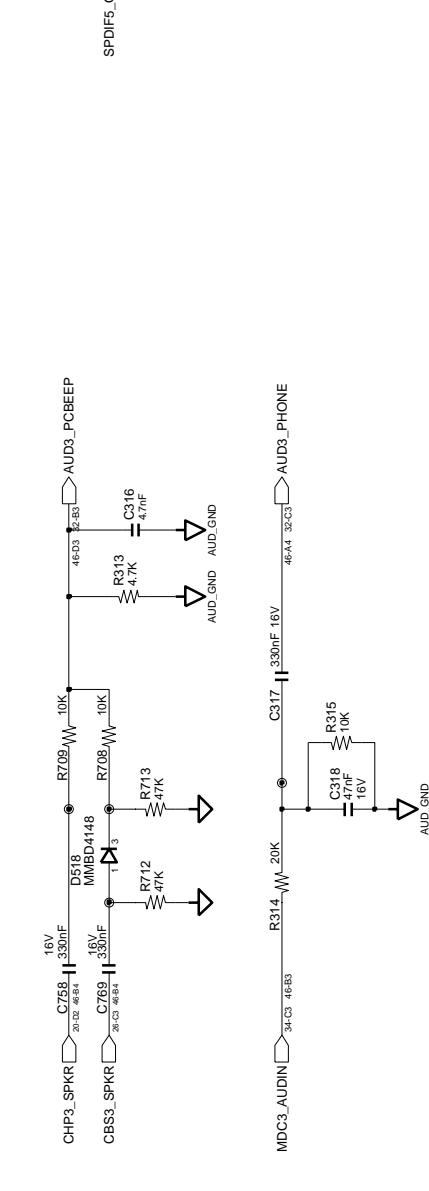
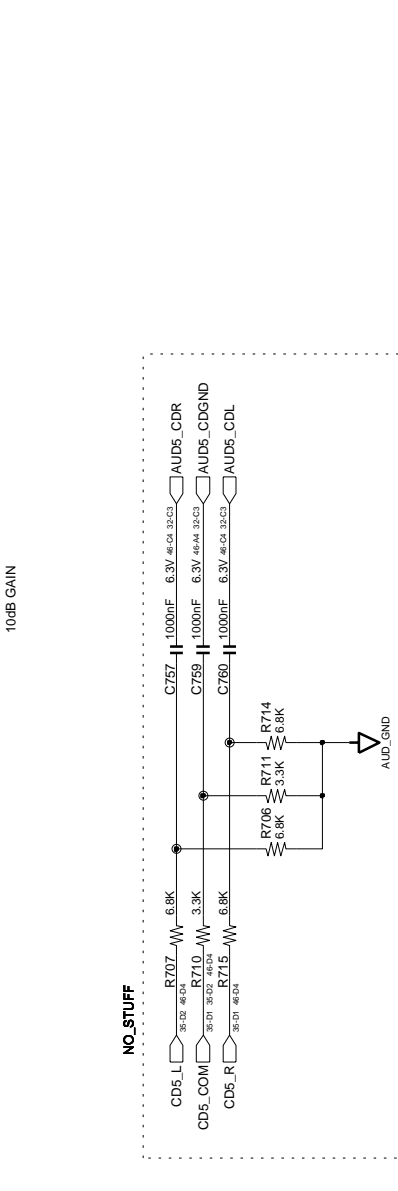
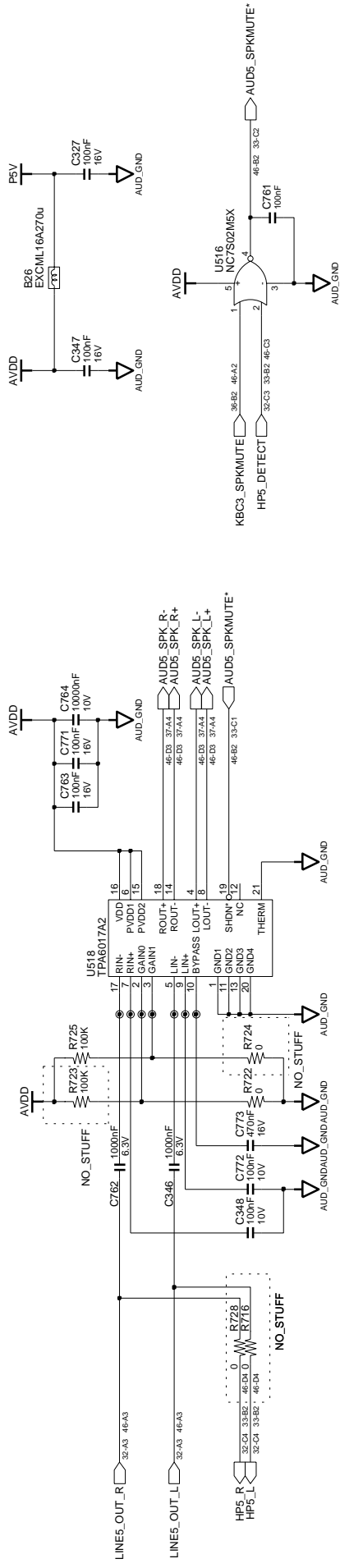
AC97 2.3 CODEC

ID0*	ID1*	CODEC ID	CLK FREQ.	SOURCE
1	1	PRIMARY	24.576 MHz	Local XTAL
0	1	EXT. CLK	19.2 MHz	Ext. Clock (into XTAL_IN)
0	0	PRIMARY	48.000 MHz	Ext. Clock (into XTAL_IN)
0	0	PRIMARY	14.318 MHz	Ext. Clock (into XTAL_IN)



DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRAWN	ZHOU & GUO	REV	MP
CHECK	ANTONIO	REV	MP
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
		PAGE	32 OF 46
		PART NO.	BA41-00529A
			SAMSUNG ELECTRONICS

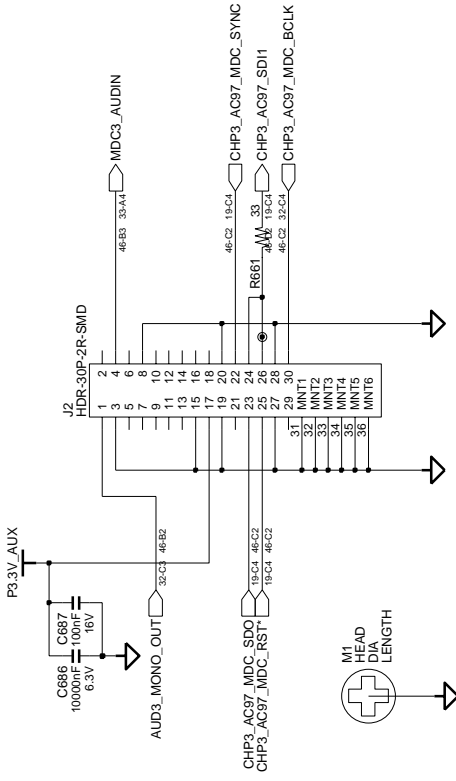
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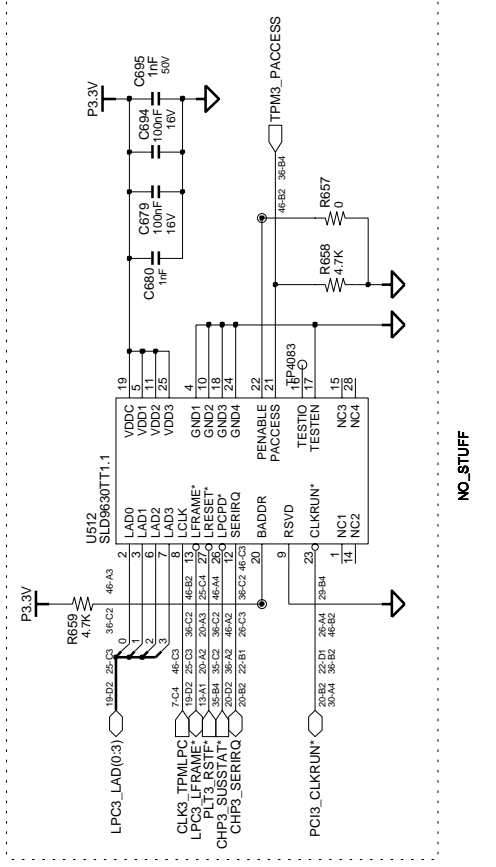
DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRWN	ZHOU & GUO	CHECK	ANTONIO
REV	1.0	APPROVAL	KEVIN LEE
MODULE CODE		MAIN AMP	
DATE EDIT	June 25, 2005 12:21:39 PM	PAGE	33 OF 46
PART NO.	BA41-00529A		

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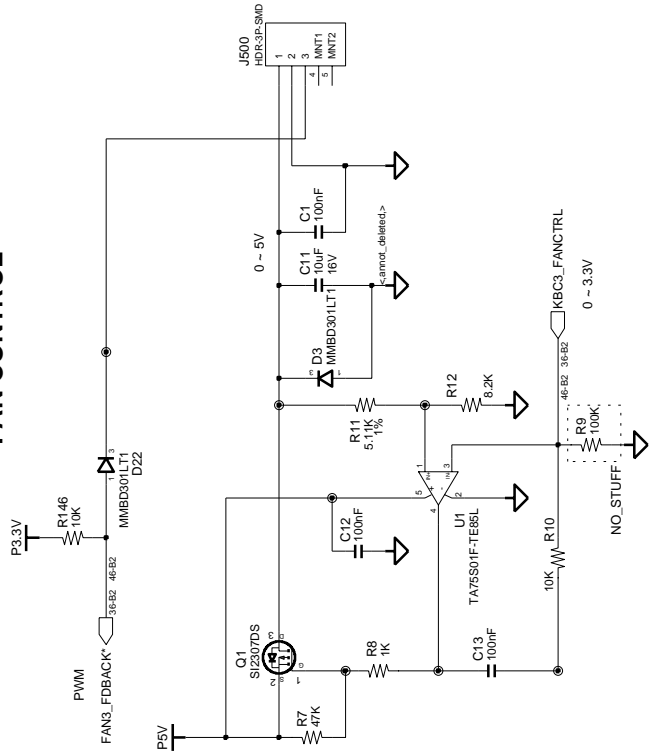
MDC Connector



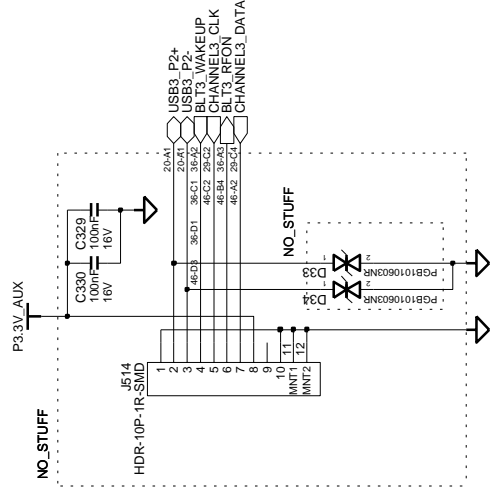
TPM



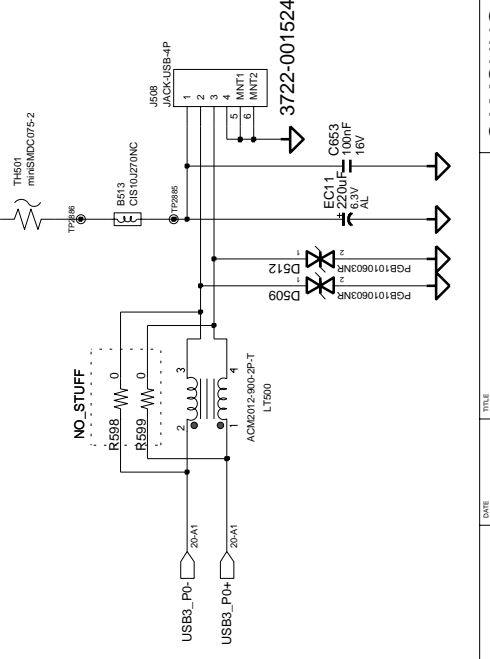
FAN CONTROL



BLUETOOTH CONNECTOR



USB connector

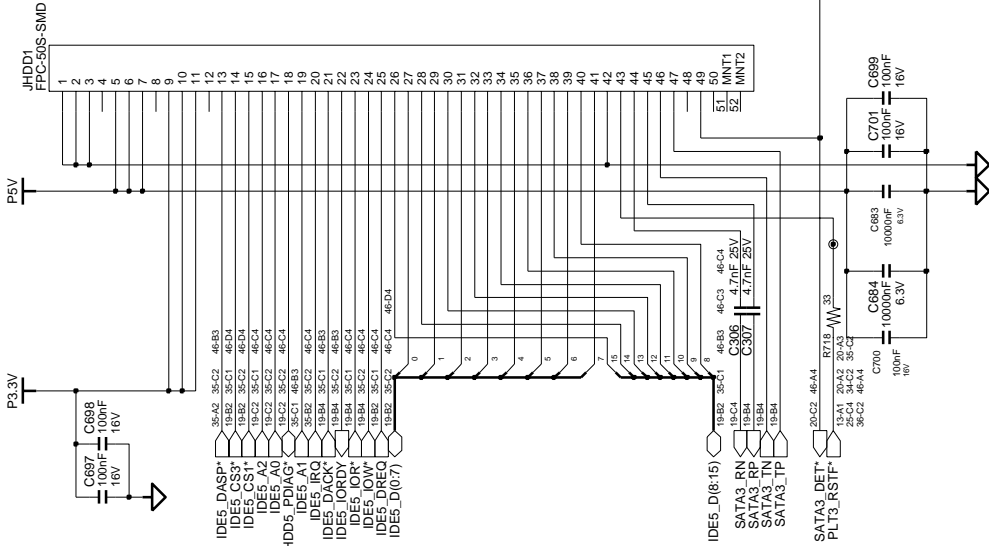


DATE	6/25/2005	TITLE	AGUILA-SONOMA
DEV. STOP	ANTONIO	MP	MAIN
REV	KEVIN/LEE	1.0	MDC/TPM/FAN/BLT/USB
MODULE CODE			

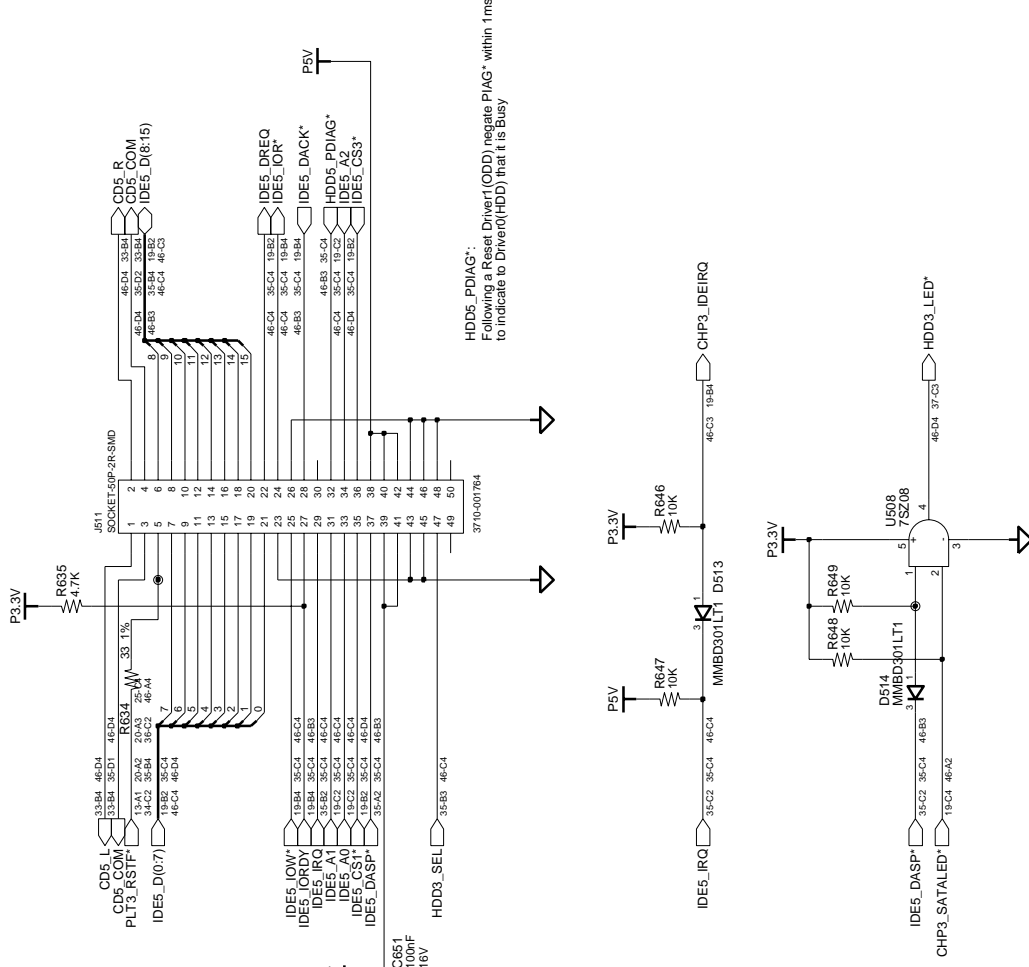
DRAWN	ZHOU & GUO	SAMSUNG ELECTRONICS
CHECK	ANTONIO	PART NO.
APPROVAL	KEVIN/LEE	BA41-00529A
LAST EDIT		

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Main to HDD



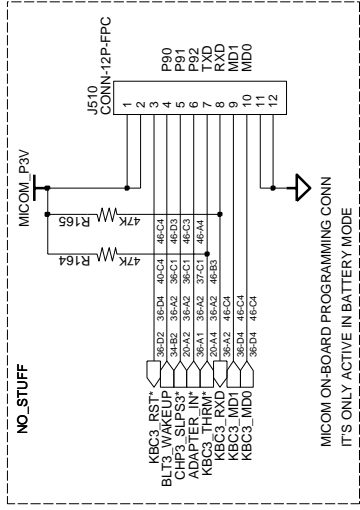
Main to ODD



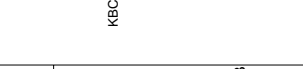
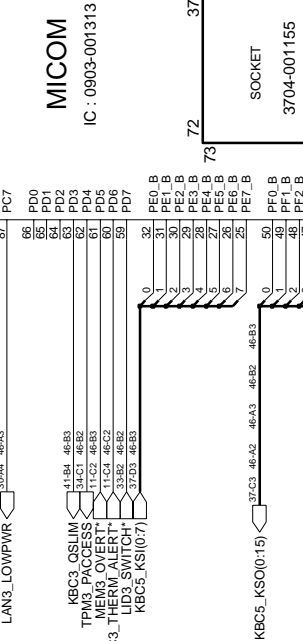
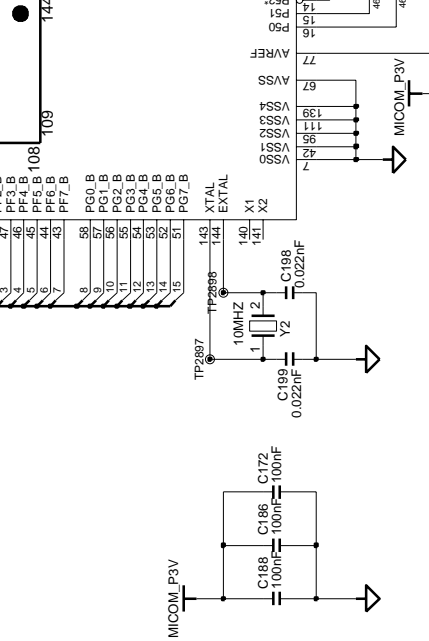
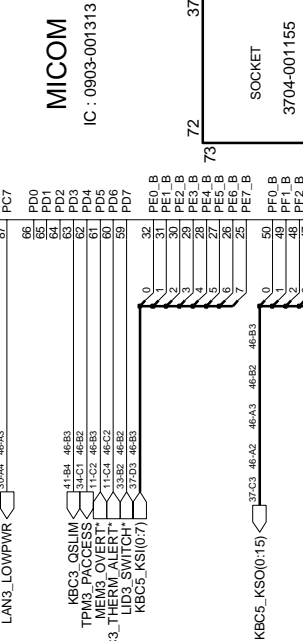
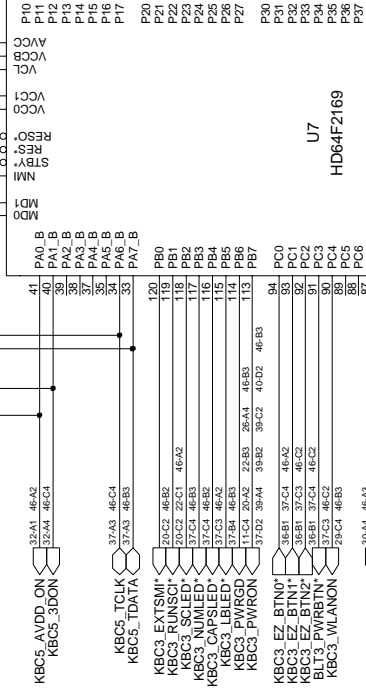
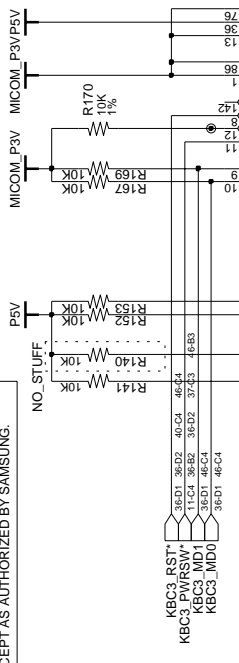
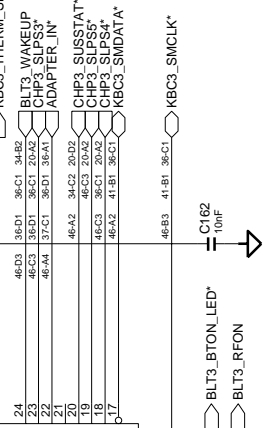
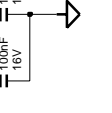
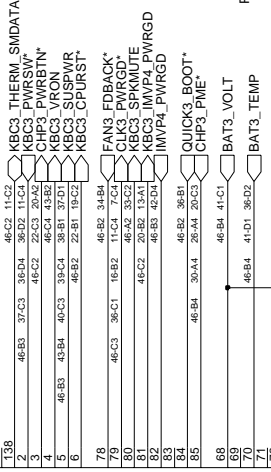
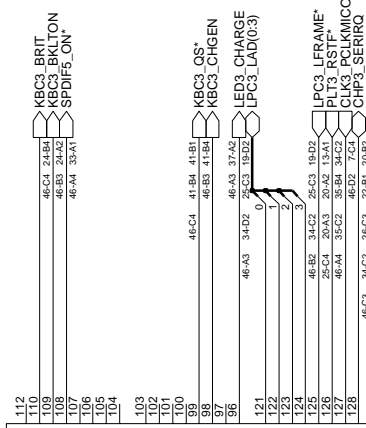
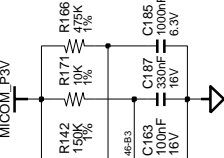
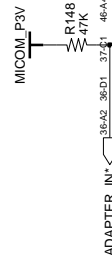
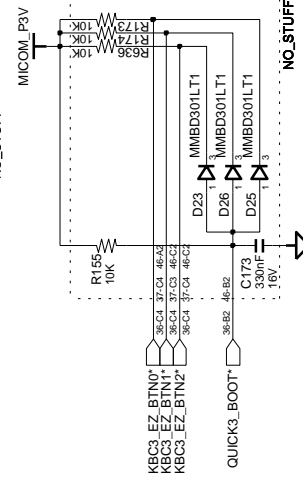
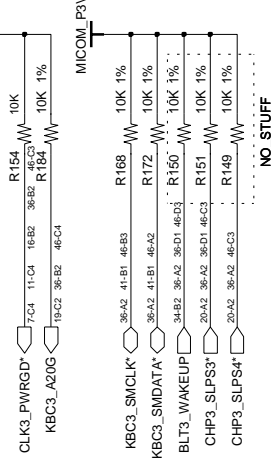
HDD5_PDIAG*:
 Following a Reset Driver1(ODD) negate P!AG* within 1ms
 to indicate to Driver0(HDD) that it is Busy

DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRAWN	ZHOU & GUO	DRW. STEP	MP
CHECK	ANTONIO	REV	1.0
APPROVAL	KEVIN LEE	LAST EDIT	June 25, 2005 12:21:39 PM
MODULE CODE		PAGE	35 OF 46
			SAMSUNG X06 9.35

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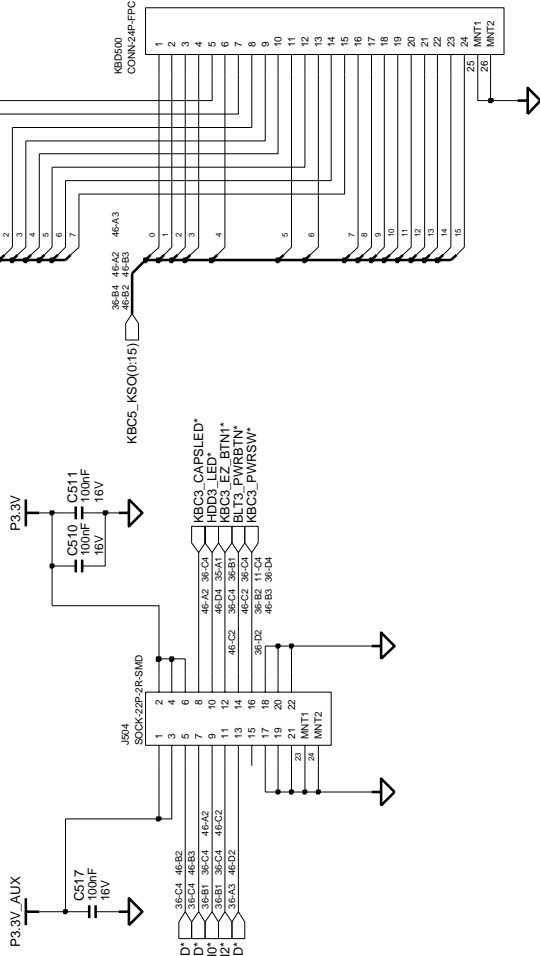
MICOM ON-BOARD PROGRAMMING CONN
 IT'S ONLY ACTIVE IN BATTERY MODE



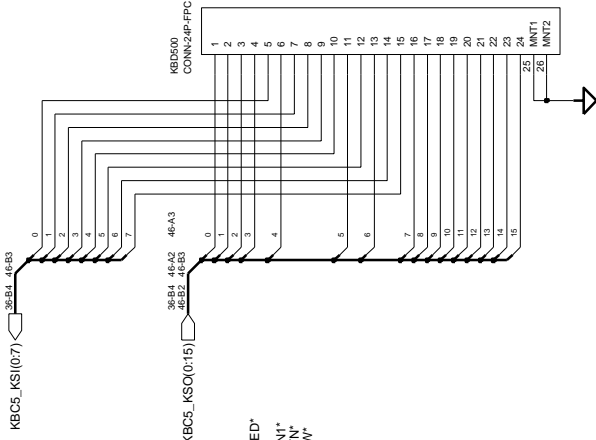
112	P10	KBC3_RST*	36-D1 36-D4 46-C4	KBC3_BRIT	46-C4 46-C4
P11	T10	KBC3_PWSW*	46-B3 20-A2	KBC3_BKLTON	46-B4 30-A1
P12	T09	KBC3_PWSW*	11-C4 36-B2 36-D4 37-C3	SPDIF5_ON*	
P13	T08				
P14	T06				
P15	T05				
P16	T04				
P17	T03				
P20	T02				
P21	T01				
P22	T00				
P23	99				
P24	98				
P25	97				
P26	96				
P27	95				
P30	121				
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P36	127				
P37	128				
P40	136				
P41	137				
P42	138				
P43	3				
P44	4				
P45	5				
P46	6				
P47	7				
P60	78				
P61	79				
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P80	129				
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P86	135				
P90	24				
P91	23				
P92	22				
P93	21				
P94	20				
P95	19				
P96	18				
P97	17				
P100	143				
P101	144				
P102	140				
P103	141				

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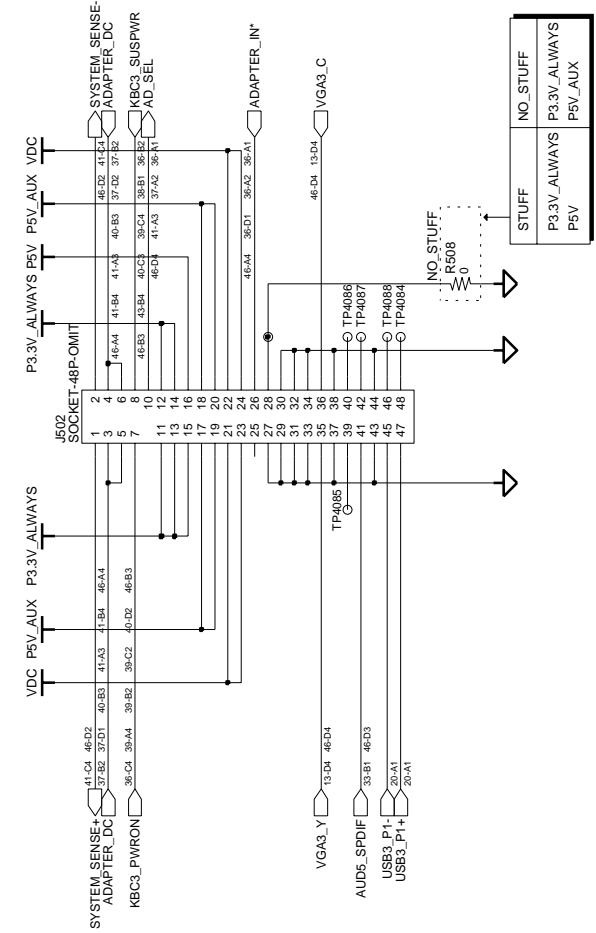
MAIN TO ON-TOP



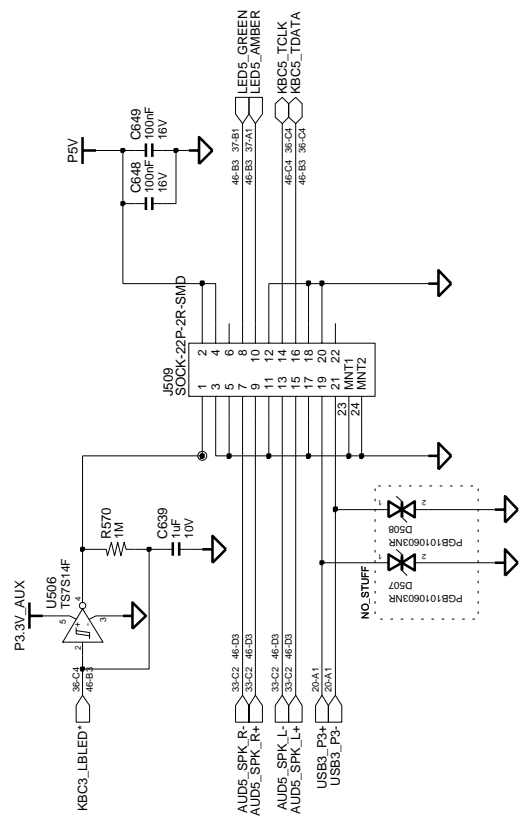
KEYBOARD



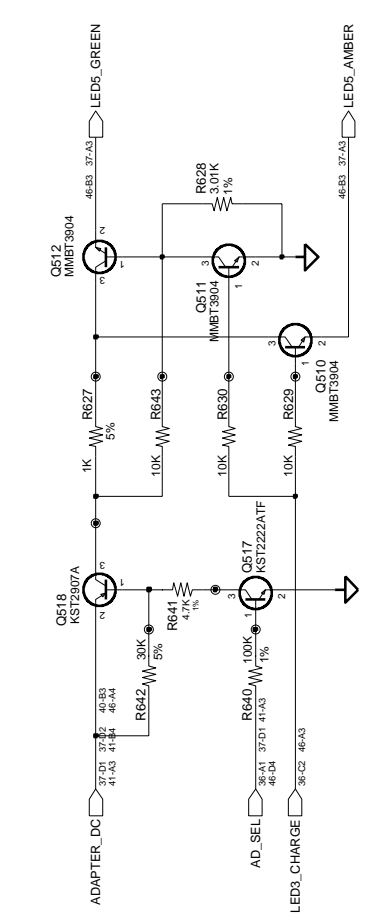
Main to DC/DC BOARD



TOUCHPAD CONNECTOR



ADAPTERIN/CHARGING LED

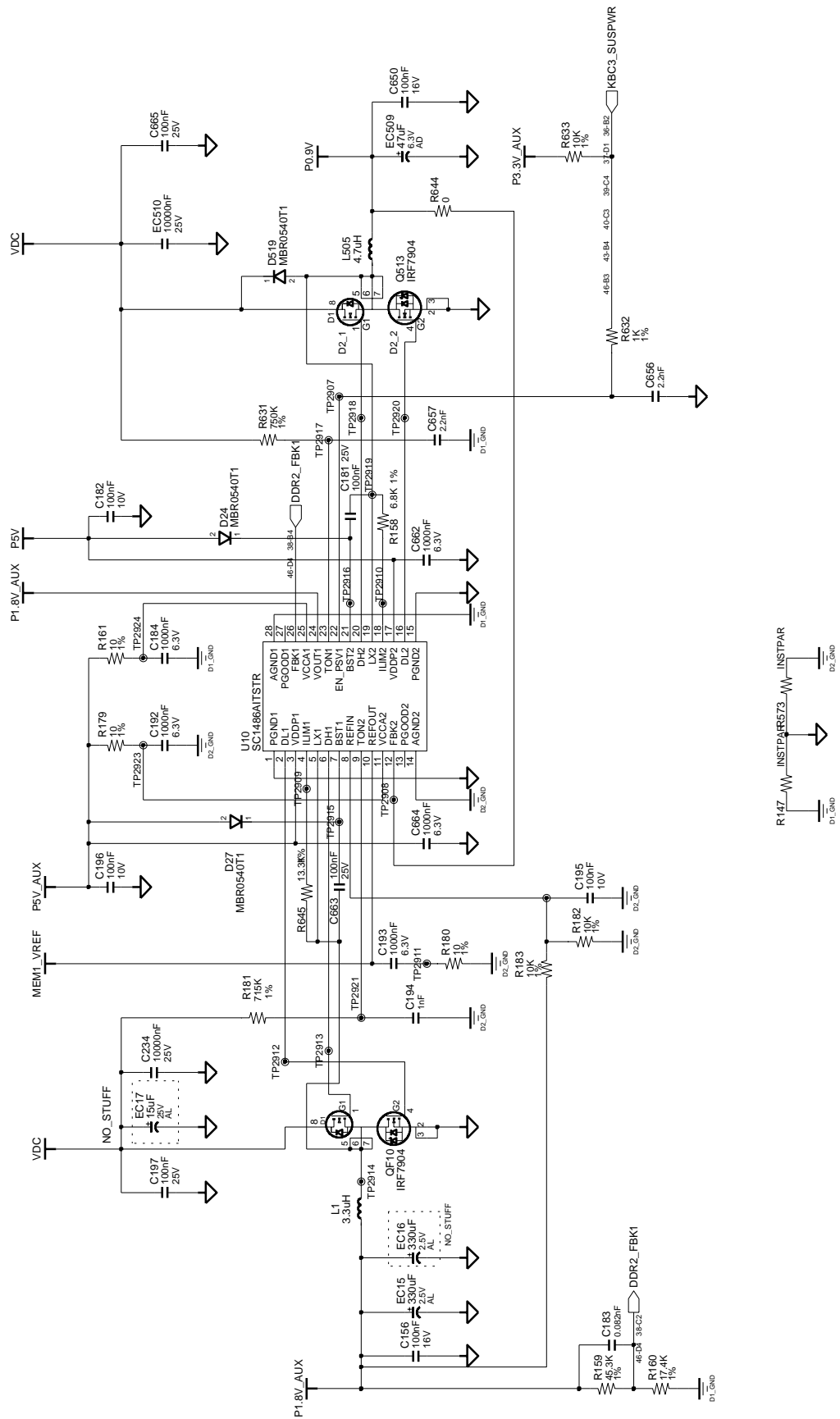


DRAWN	ZHOU & GUO	DATE	6/25/2005	TITLE	AQUILA-SONOMA
CHECK	ANTONIO	DRW. STUP		REV	MP
APPROVAL	KEVIN LEE	REV	1.0		B'd to B'd CONN
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM	PAGE	37 OF 46

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AQUILA-SONOMA MAIN		PAGE 37 OF 46	

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DDR II Power

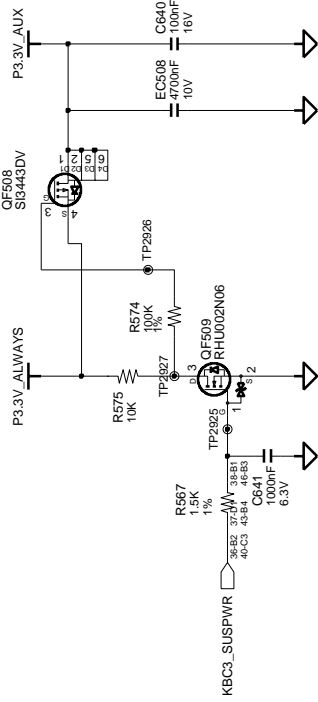


DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRAWN	ZHOU & GUO	REV	MAIN
CHECK	ANTONIO	MP	DDR II POWER
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
PART NO.	BA41-00529A	PAGE	38 OF 46
SAMSUNG ELECTRONICS		SAMSUNG X06 9-38	

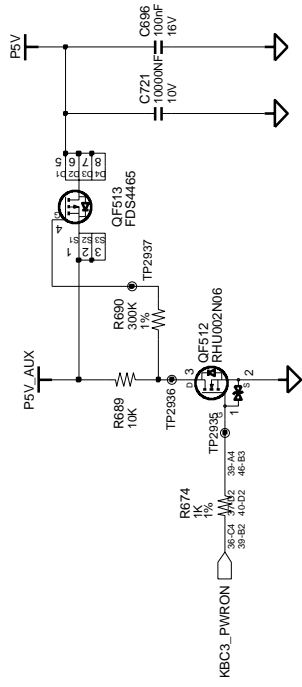
DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRAWN	ZHOU & GUO	REV	MAIN
CHECK	ANTONIO	MP	DDR II POWER
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
PART NO.	BA41-00529A	PAGE	38 OF 46
SAMSUNG ELECTRONICS		SAMSUNG X06 9-38	

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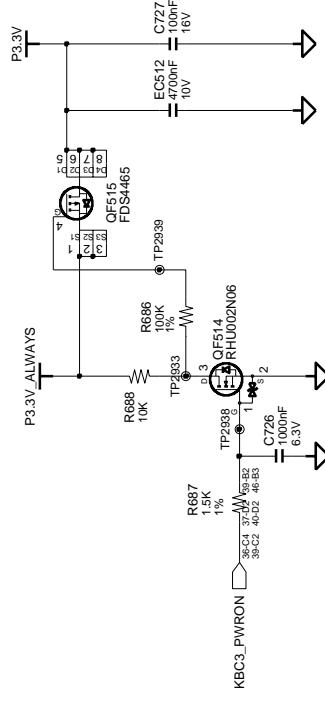
Switched Power On (P3.3V_AUX)



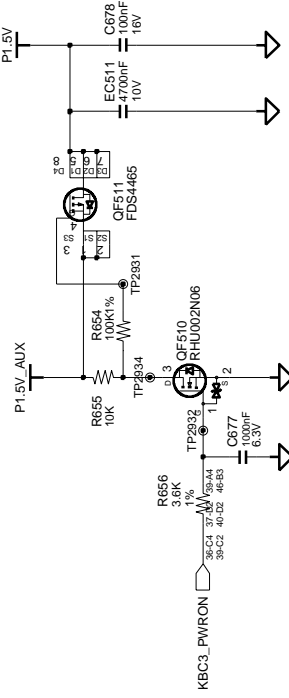
Switched Power On (P5V)



Switched Power On (P3.3V)



Switched Power On (P1.5V)



DATE	6/25/2005	TITLE	AQUILA-SONOMA
DRAWN	ZHOU & GUO	REV	MP
CHECK	ANTONIO	REV	1.0
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
		PAGE	39 OF 46
			SAMSUNG X06 9.39

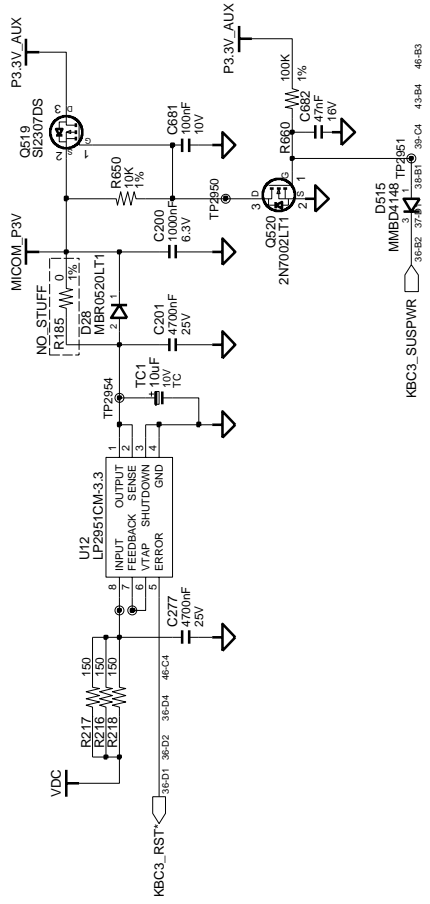
SAMSUNG
 ELECTRONICS

MAIN
 SWITCHED POWER

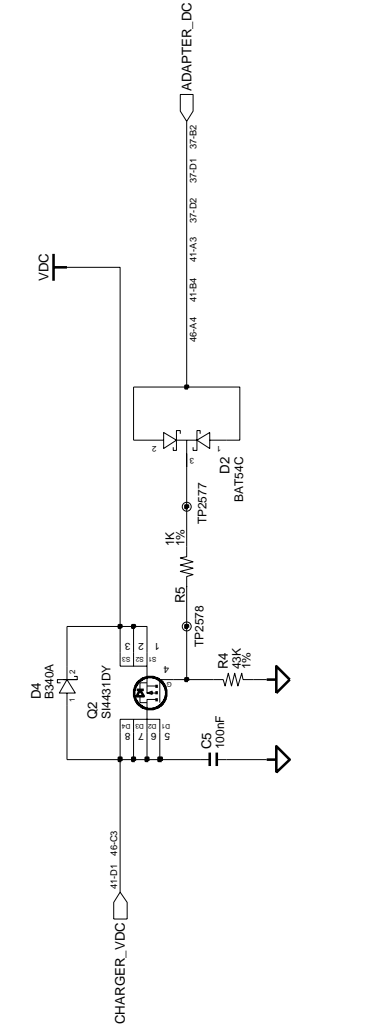
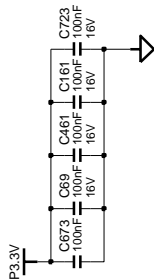
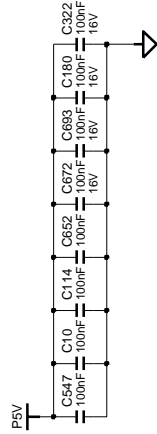
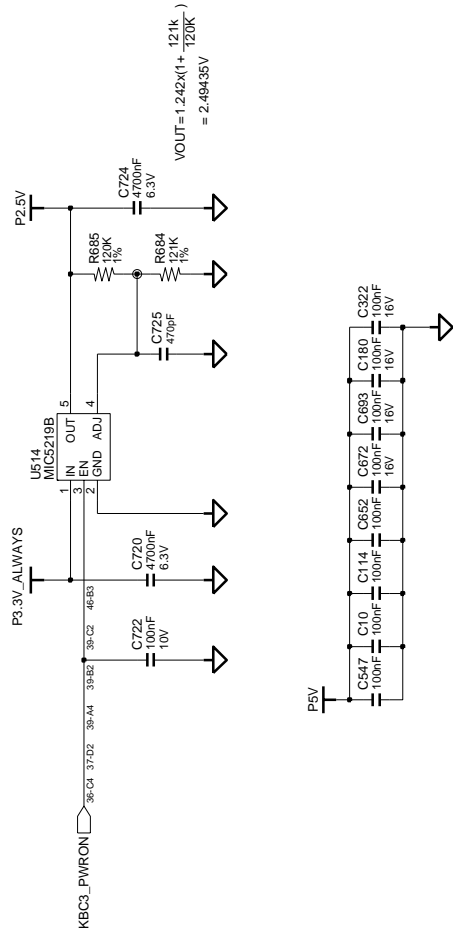
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MICOM_P3V



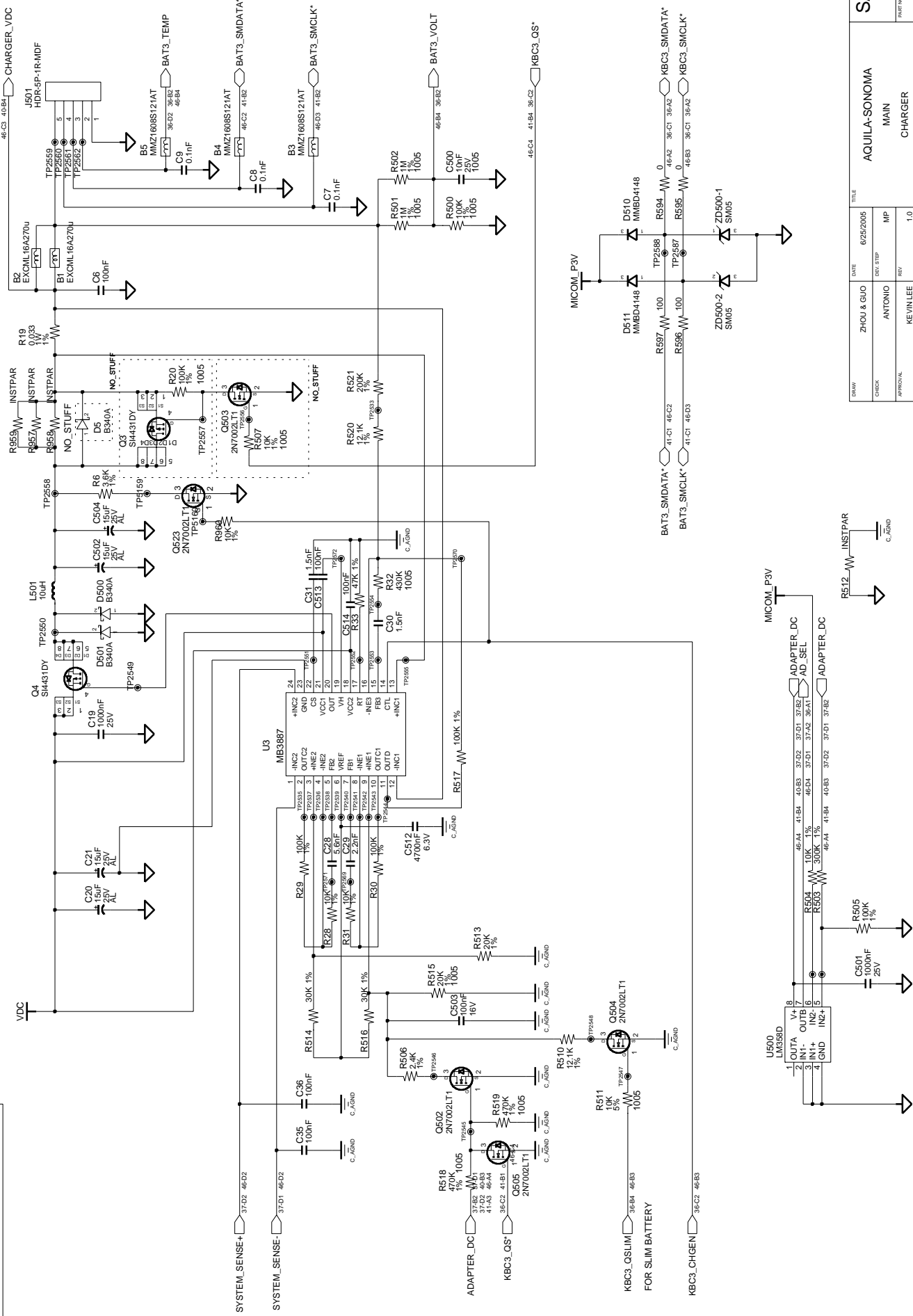
P2.5V



DATE	6/25/2005	TITLE	AQUILA-SONOMA
DESIGNER	ZHOU & GUO	REV	MAIN
CHECKED	ANTONIO	REV	MICOM_P3V / P2.5V
APPROVED	KEVIN LEE	REV	1.0
MODULE CODE	LAST EDIT	DATE	PAGE
		June 25, 2005 12:21:39 PM	40 OF 46

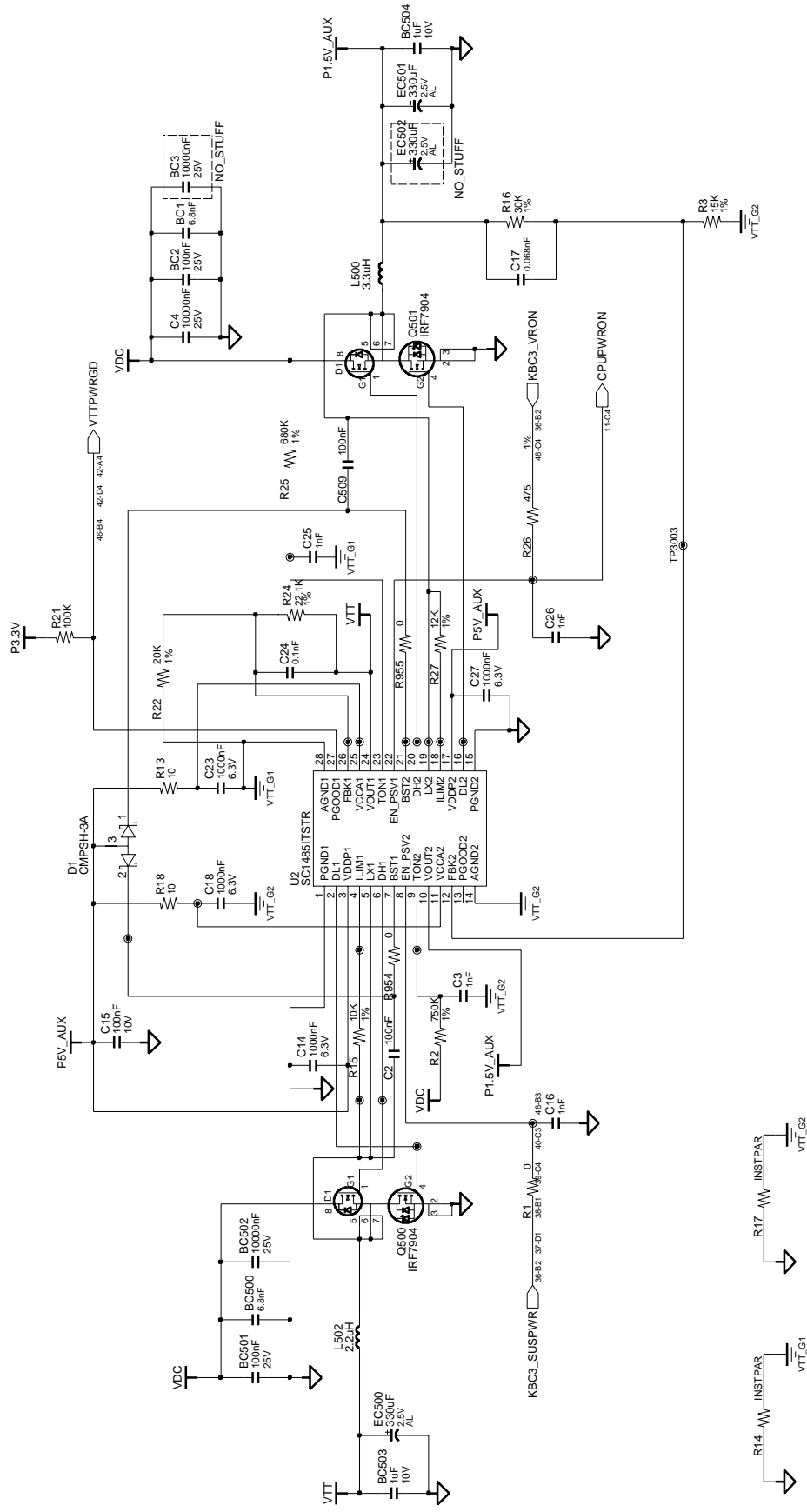
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DATE	6/25/2005	TITLE	AQUILA-SONOMA
CHK	ANTONIO	REV	MP
APPROVAL	KEVIN LEE	REV	1.0
DRAWN	ZHOU & GUO	DATE	6/25/2005
CHECK	ANTONIO	CHK. STEP	MP
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
SAMSUNG ELECTRONICS		PART NO. BA41-00529A	
MAIN CHARGER		PAGE	41 OF 46

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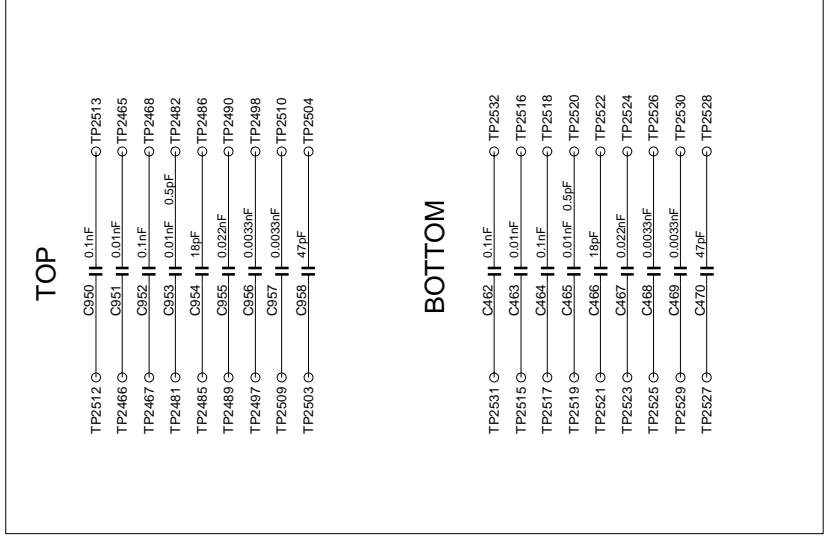


DRAWN		DATE	TITLE	
ZHOUI & GUO		6/25/2005	AQUILA-SONOMA	
CHECK	ANTONIO	DEV. STEP	MAIN	
APPROVAL	KEVIN LEE	REV	VTT / P1.5V	
MODULE CODE		LAST EDIT	PAGE	
		June 25, 2005 12:21:39 PM	43	OF 46

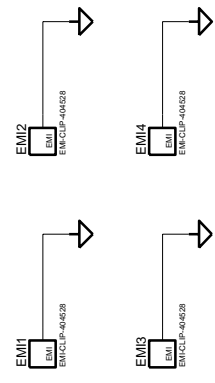
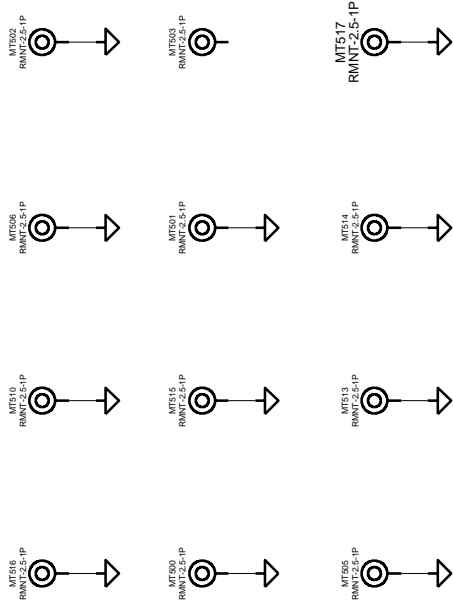
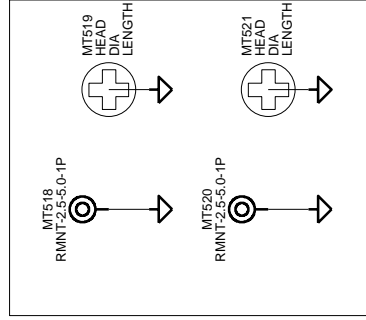
DRAWN		DATE	TITLE	
ZHOUI & GUO		6/25/2005	AQUILA-SONOMA	
CHECK	ANTONIO	DEV. STEP	MAIN	
APPROVAL	KEVIN LEE	REV	VTT / P1.5V	
MODULE CODE		LAST EDIT	PAGE	
		June 25, 2005 12:21:39 PM	43	OF 46

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THESE ARE USED FOR INTERNAL CIRCUIT TEST
 TO COMPARE CAPACITORS WHICH ARE UNDER 100pF



FOR THERMAL



PCB REVISION CONTROL (ICT)		
NO	CONNECTION DATE(Y/M/MDD)	REVISION STEP
1	N.C.	1.0 MP
2	1-2	
3	2-3	
4	3-1	
5	1-2-3	
6	N.C.	
7	1-2	
8	2-3	
9	3-1	
10	1-2-3	

REV:000
 1 O
 2 O O3

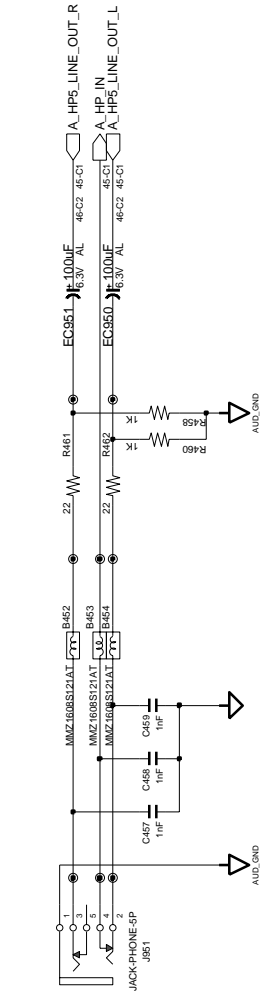
DRAWN	ZHOU & GUO	DATE	6/25/2005	TITLE	AQUILA-SONOMA
CHECK	ANTONIO	DEV. STEP	MP		MAIN
APPROVAL	KEVIN LEE	REV	1.0		PCB STUFFS
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM		
				PAGE	44 OF 46
					SAMSUNG X06 9-44

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 PART NO. BA41-00529A

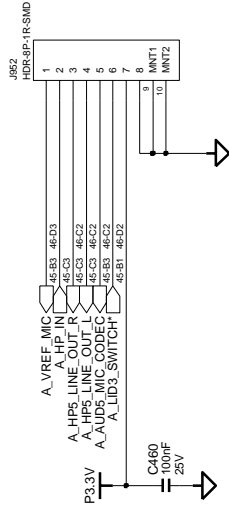
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AUDIO BOARD

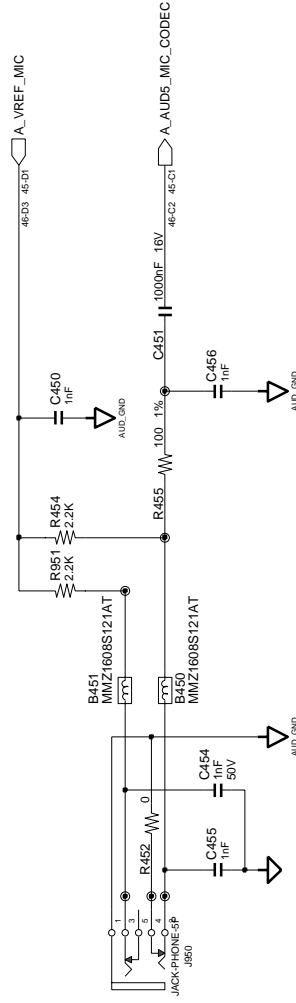
HEADPHONE



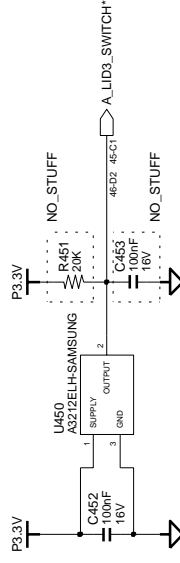
B'D TO B'D CONN



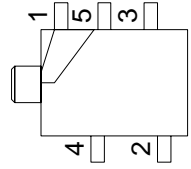
EXTERNAL MIC



LID SWITCH



TOP VIEW



DATE	6/25/2005	TITLE	AQUILA-SONOMA SUB BOARD AUDIO BOARD
DRAWN	ZHOU & GUO	CHKD	ANTONIO
CHECK	ANTONIO	MP	
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	June 25, 2005 12:21:39 PM
PAGE	45	OF	46

SAMSUNG ELECTRONICS
 PART NO. BA41-00529A

9 Schematic Diagram

9-1-2 Signal Location

Net Name	Sheet Number-Location
A_AUD5_MIC_CODEC	45-B3, 45-C1, 46-C2
A_HP_IN	45-C1, 45-C3
A_HP5_LINE_OUT_L	45-C1, 45-C3, 46-C2
A_HP5_LINE_OUT_R	45-C1, 45-C3, 46-C2
A_LID3_SWITCH*	45-B1, 45-C1, 46-D2
A_VREF_MIC	45-B3, 45-D1, 46-D3
AD_SEL	36-A1, 37-A2, 37-D1, 41-A3, 46-D4
ADAPTER_DC	37-B2, 37-D1, 37-D2, 40-B3, 41-A3, 41-A3, 41-B4, 46-A4
ADAPTER_IN*	36-A1, 36-A2, 36-D1, 37-C1, 46-A4
AMP5_PWRDOWN	32-A1, 32-C4, 46-C2
AUD3_MONO_OUT	32-C3, 34-C4, 46-B2
AUD3_PCBEEP	32-B3, 33-B3, 46-D3
AUD3_PHONE	32-C3, 33-A3, 46-A4
AUD5_CDGND	32-C3, 33-B3, 46-A4
AUD5_CDL	32-C3, 33-B3, 46-C4
AUD5_CDR	32-C3, 33-B3, 46-C4
AUD5_LINE_OUT_L	32-A4, 32-C3, 46-C2
AUD5_LINE_OUT_R	32-A4, 32-C3, 46-C2
AUD5_MIC_CODEC	32-C3, 33-B2, 46-D2
AUD5_SPDIF	33-B1, 37-C2, 46-D3
AUD5_SPK_L-	33-C2, 37-A4, 46-D3
AUD5_SPK_L+	33-C2, 37-A4, 46-D3
AUD5_SPK_R-	33-C2, 37-A4, 46-D3
AUD5_SPK_R+	33-C2, 37-A4, 46-D3
AUD5_SPKMUTE*	33-C1, 33-C2, 46-B2
AUD5_STANDBY*	32-A4, 32-B2, 46-B2
BAT3_SMCLK*	41-B2, 41-C1, 46-D3
BAT3_SMDATA*	41-B2, 41-C1, 46-C2
BAT3_TEMP	36-B2, 36-D2, 41-D1, 46-B4
BAT3_VOLT	36-B2, 41-C1, 46-B4
BLT3_BTON_LED*	36-A3, 37-C4, 46-D2
BLT3_PWRBTN*	36-C4, 37-C3, 46-C2
BLT3_RFON	34-B2, 36-A3, 46-B4
BLT3_WAKEUP	34-B2, 36-A2, 36-C1, 36-D1, 46-D3

Net Name	Sheet Number-Location
CB3_A_A_18	27-B4, 28-C3, 46-D3
CB3_A_A_19	27-B4, 28-C3, 46-D3
CB3_A_D_14	27-B4, 28-D3, 46-D3
CB3_A_D_2	27-B4, 28-B3, 46-B4
CB3_CAD(0)	27-D4, 28-D3, 46-D3
CB3_CAD(1)	27-D4, 28-D3, 46-D3
CB3_CAD(10)	27-D4, 28-D3, 46-D3
CB3_CAD(11)	27-D4, 28-D3, 46-D3
CB3_CAD(12)	27-D4, 28-D3, 46-D3
CB3_CAD(13)	27-D4, 28-D3, 46-D3
CB3_CAD(14)	27-D4, 28-D3, 46-D3
CB3_CAD(15)	27-D4, 28-D3, 46-D3
CB3_CAD(16)	27-D4, 28-D3, 46-D3
CB3_CAD(17)	27-D4, 28-D3, 46-C3
CB3_CAD(18)	27-D4, 28-D3, 46-C3
CB3_CAD(19)	27-D4, 28-D3, 46-C3
CB3_CAD(2)	27-D4, 28-D3, 46-D3
CB3_CAD(20)	27-D4, 28-D3, 46-C3
CB3_CAD(21)	27-D4, 28-D3, 46-C3
CB3_CAD(22)	27-D4, 28-D3, 46-C3
CB3_CAD(23)	27-D4, 28-D3, 46-C3
CB3_CAD(24)	27-D4, 28-D3, 46-C3
CB3_CAD(25)	27-D4, 28-D3, 46-C3
CB3_CAD(26)	27-D4, 28-D3, 46-C3
CB3_CAD(27)	27-D4, 28-D3, 46-C3
CB3_CAD(28)	27-D4, 28-D3, 46-C3
CB3_CAD(29)	27-D4, 28-D3, 46-C3
CB3_CAD(3)	27-D4, 28-D3, 46-D3
CB3_CAD(30)	27-D4, 28-D3, 46-C3
CB3_CAD(31)	27-D4, 28-D3, 46-C3
CB3_CAD(31:0)	27-D4, 28-D3
CB3_CAD(4)	27-D4, 28-D3, 46-D3
CB3_CAD(5)	27-D4, 28-D3, 46-D3
CB3_CAD(6)	27-D4, 28-D3, 46-D3
CB3_CAD(7)	27-D4, 28-D3, 46-D3
CB3_CAD(8)	27-D4, 28-D3, 46-D3
CB3_CAD(9)	27-D4, 28-D3, 46-C3
CB3_CAUDIO	27-B4, 28-B3, 46-C3

9 Schematic Diagram

Net Name	Sheet Number-Location
CB3_CCBE0*	27-B4, 28-D3, 46-C3
CB3_CCBE1*	27-C4, 28-C3, 46-C3
CB3_CCBE2*	27-C4, 28-C3, 46-C3
CB3_CCBE3*	27-C4, 28-B3, 46-C3
CB3_CCD1*	27-B4, 28-D3, 46-B4
CB3_CCD2*	27-B4, 28-B3, 46-B4
CB3_CCLK	27-B4, 28-C3, 46-C4
CB3_CCLKRUN*	27-B4, 28-B3, 46-C2
CB3_CDEVSEL*	27-B4, 28-C3, 46-C2
CB3_CFRAME*	27-B4, 28-C3, 46-C3
CB3_CGNT*	27-B4, 28-C3, 46-B4
CB3_CINT*	27-B4, 28-C3, 46-B4
CB3_CIRDY*	27-B4, 28-C3, 46-C3
CB3_CPAR	27-B4, 28-C3, 46-C4
CB3_CPERR*	27-B4, 28-C3, 46-C3
CB3_CREQ*	27-B4, 28-B3, 46-B4
CB3_CRST*	27-B4, 28-B3, 46-B4
CB3_CSERR*	27-B4, 28-B3, 46-C3
CB3_CSTOP*	27-B4, 28-C3, 46-C3
CB3_CSTSCHG	27-B4, 28-B3, 46-C3
CB3_CTRDY*	27-B4, 28-C3, 46-C3
CB3_CVS1	27-B4, 28-C3, 46-C4
CB3_CVS2	27-B4, 28-B3, 46-C4
CB3_MD_CLK	27-B2, 28-B2, 46-C3
CB3_MD_DATA0_MS_SDIO	27-B2, 28-C2, 46-C2
CB3_MD_DATA1	27-B2, 28-C2, 46-C2
CB3_MD_DATA2	27-B2, 28-C2, 46-C2
CB3_MD_DATA3	27-B2, 28-B2, 46-C2
CB3_MD_VCCEN	26-B2, 27-B2, 46-C2
CB3_MS_BS_SD_CMD	27-B2, 28-B2, 46-C2
CB3_MS_INS*_XD_CD*	27-B2, 28-B2, 46-C2
CB3_SD_CD*_XD_CD*	27-B2, 28-B2, 46-C2
CB3_SD_WP*_XD_R_B*	27-B2, 28-B2, 46-C2
CB3_VCC3EN*	26-B2, 27-A4, 46-C3
CB3_VCC5EN*	26-B2, 27-A4, 46-C3
CB3_VCCA	26-B1, 28-C3, 28-C3, 46-C4
CB3_VPPA	26-B1, 28-C3, 28-C3, 46-C4
CB3_VPPEN0	26-B2, 27-A4, 46-C3
CB3_VPPEN1	26-B2, 27-A4, 46-C3
CBS3_SPKR	26-C3, 33-B4, 46-B4

Net Name	Sheet Number-Location
CD5_COM	33-B4, 35-D1, 35-D2, 46-D4
CD5_L	33-B4, 35-D2, 46-D4
CD5_R	33-B4, 35-D1, 46-D4
CHANNEL3_CLK	29-C2, 34-B2, 46-C2
CHANNEL3_DATA	29-C4, 34-B2, 46-A2
CHARGER_VDC	40-B4, 41-D1, 46-C3
CHP3_1394_ROMW*	20-D3, 26-C2, 46-C2
CHP3_AC97_AUD_BCLK	19-C4, 32-C4, 46-C2
CHP3_AC97_AUD_RST*	19-C4, 32-C4, 46-C2
CHP3_AC97_AUD_SDO	19-C4, 32-C4, 46-C2
CHP3_AC97_AUD_SYNC	19-C4, 32-C4, 46-C2
CHP3_AC97_MDC_BCLK	32-C4, 34-C3, 46-C2
CHP3_AC97_MDC_RST*	19-C4, 34-C4, 46-C2
CHP3_AC97_MDC_SDO	19-C4, 34-C4, 46-C2
CHP3_AC97_MDC_SYNC	19-C4, 34-C3, 46-C2
CHP3_AC97_SDI0	19-C4, 32-C4, 46-D2
CHP3_AC97_SDI1	19-C4, 34-C3, 46-D2
CHP3_BATLOW*	20-A2, 22-C3, 46-C2
CHP3_BIOSTBL*	20-D3, 25-C4, 46-A2
CHP3_BIOSWP*	20-C3, 25-C4, 46-C2
CHP3_CPUSTP*	7-C4, 20-C2, 42-C4, 46-C2
CHP3_CRISIS*	20-A4, 20-B2
CHP3 DPRSLPVR	20-A2, 22-B3, 42-B2, 46-A2
CHP3_IDEIRQ	19-B4, 35-B1, 46-C3
CHP3_INTRUDER*	19-D3, 22-B3, 46-D2
CHP3_IVTPWRON	20-C2, 24-B2, 46-A2
CHP3_PCISTP*	7-C4, 20-C2, 46-C2
CHP3_PME*	20-C3, 26-A4, 30-A4, 36-B2, 46-B4
CHP3_PWRBTN*	20-A2, 22-C3, 36-B2, 46-C2
CHP3_RTCRST*	19-A2, 19-D3
CHP3_SATALED*	19-C4, 35-A2, 46-A2
CHP3_SERIRQ	20-B2, 22-B1, 26-C3, 34-C2, 36-C2, 46-C3
CHP3_SLPS3*	20-A2, 36-A2, 36-C1, 36-D1, 46-C3
CHP3_SLPS4*	20-A2, 36-A2, 36-C1, 46-C3
CHP3_SLPS5*	20-A2, 36-A2, 46-C3
CHP3_SMLINK0	20-D2, 22-D3, 46-C2
CHP3_SMLINK1	20-D2, 22-C3, 46-C2

9 Schematic Diagram

Net Name	Sheet Number-Location
CHP3_SPKR	20-D2, 33-B4, 46-B4
CHP3_SUSSTAT*	20-D2, 34-C2, 36-A2, 46-A2
CHP3_THRM*	20-B2, 20-B3, 46-C3
CHP3_THRMTRIP*	11-B3, 36-B2, 46-D2
CLK0_HCLK0	7-C1, 9-C3
CLK0_HCLK0*	7-C1, 9-C3
CLK0_HCLK1	7-C1, 12-B2
CLK0_HCLK1*	7-C1, 12-B2
CLK1_BSEL1	7-C4, 9-C2, 9-C3, 13-A4, 46-C3
CLK1_BSEL2	7-C4, 9-C2, 9-C3, 13-A4, 46-C3
CLK1_DOTCLK	7-B1, 16-B2
CLK1_DOTCLK*	7-B1, 16-A2
CLK1_DREFCLK	7-B1, 13-A1
CLK1_DREFCLK*	7-B1, 13-A1
CLK1_DREFSSCLK	13-A1, 16-B1
CLK1_DREFSSCLK*	13-A1, 16-B1
CLK1_MCH3GPLL	7-C1, 13-D4
CLK1_MCH3GPLL*	7-C1, 13-D4
CLK1_MCLK0	13-C1, 17-C4
CLK1_MCLK0*	13-B1, 17-C4
CLK1_MCLK1	13-C1, 17-C4
CLK1_MCLK1*	13-B1, 17-C4
CLK1_MCLK3	13-C1, 17-C2
CLK1_MCLK3*	13-B1, 17-C2
CLK1_MCLK4	13-C1, 17-C2
CLK1_MCLK4*	13-B1, 17-C2
CLK1_PCIEICH	7-C1, 20-B1
CLK1_PCIEICH*	7-C1, 20-B1
CLK1_SATA	7-C1, 19-B4
CLK1_SATA*	7-C1, 19-B4
CLK3_AUD14	7-B1, 32-D4, 46-C3
CLK3_ICH14	7-B1, 20-B1, 46-C3
CLK3_PCLKCB	7-C4, 26-A4, 46-C3
CLK3_PCLKFWH	7-C4, 25-C4, 46-C2
CLK3_PCLKICH	7-C4, 20-C3, 46-C2
CLK3_PCLKLAN	7-C4, 30-B4, 46-C2
CLK3_PCLKMICOM	7-C4, 36-C2, 46-D2
CLK3_PCLKMIN	7-C4, 29-C4, 46-B2

Net Name	Sheet Number-Location
CLK3_PWRGD*	7-C4, 11-C4, 16-B2, 36-B2, 36-C1, 46-C3
CLK3_SMBCLK	7-A3, 7-C4, 17-B2, 17-B4
CLK3_SMBDATA	7-A3, 7-B4, 17-B2, 17-B4
CLK3_SSCIN	7-B1, 16-B2, 46-C3
CLK3_TPMLPC	7-C4, 34-C2, 46-C3
CLK3_USB48	7-C4, 20-A2, 46-C3
CPU1_A*(10)	8-C4, 12-D2
CPU1_A*(11)	8-C4, 12-D2
CPU1_A*(12)	8-C4, 12-D2
CPU1_A*(13)	8-C4, 12-D2
CPU1_A*(14)	8-C4, 12-D2
CPU1_A*(15)	8-C4, 12-D2
CPU1_A*(16)	8-C4, 12-D2
CPU1_A*(16:3)	8-C4
CPU1_A*(17)	8-C4, 12-D2
CPU1_A*(18)	8-C4, 12-D2
CPU1_A*(19)	8-C4, 12-D2
CPU1_A*(20)	8-C4, 12-D2
CPU1_A*(21)	8-C4, 12-D2
CPU1_A*(22)	8-C4, 12-D2
CPU1_A*(23)	8-C4, 12-D2
CPU1_A*(24)	8-C4, 12-D2
CPU1_A*(25)	8-C4, 12-D2
CPU1_A*(26)	8-C4, 12-D2
CPU1_A*(27)	8-C4, 12-D2
CPU1_A*(28)	8-C4, 12-D2
CPU1_A*(29)	8-C4, 12-D2
CPU1_A*(3)	8-C4, 12-D2
CPU1_A*(30)	8-C4, 12-D2
CPU1_A*(31)	8-C4, 12-D2
CPU1_A*(31:17)	8-C4
CPU1_A*(31:3)	12-D2
CPU1_A*(4)	8-C4, 12-D2
CPU1_A*(5)	8-C4, 12-D2
CPU1_A*(6)	8-C4, 12-D2
CPU1_A*(7)	8-C4, 12-D2
CPU1_A*(8)	8-C4, 12-D2
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CPU1_D*(1)	8-C2, 12-D4
CPU1_D*(10)	8-C2, 12-D4
CPU1_D*(11)	8-C2, 12-D4
CPU1_D*(12)	8-C2, 12-D4
CPU1_D*(13)	8-C2, 12-D4
CPU1_D*(14)	8-C2, 12-D4
CPU1_D*(15)	8-C2, 12-D4
CPU1_D*(15:0)	8-C2
CPU1_D*(16)	8-C2, 12-D4
CPU1_D*(17)	8-C2, 12-D4
CPU1_D*(18)	8-C2, 12-D4
CPU1_D*(19)	8-C2, 12-D4
CPU1_D*(2)	8-C2, 12-D4
CPU1_D*(20)	8-C2, 12-D4
CPU1_D*(21)	8-C2, 12-D4
CPU1_D*(22)	8-C2, 12-D4
CPU1_D*(23)	8-C2, 12-D4
CPU1_D*(24)	8-C2, 12-D4
CPU1_D*(25)	8-C2, 12-D4
CPU1_D*(26)	8-C2, 12-D4
CPU1_D*(27)	8-C2, 12-D4
CPU1_D*(28)	8-C2, 12-D4
CPU1_D*(29)	8-C2, 12-D4
CPU1_D*(3)	8-C2, 12-D4
CPU1_D*(30)	8-C2, 12-D4
CPU1_D*(31)	8-C2, 12-D4
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CPU1_D*(32)	8-C1, 12-D4
CPU1_D*(33)	8-C1, 12-D4
CPU1_D*(34)	8-C1, 12-D4
CPU1_D*(35)	8-C1, 12-D4
CPU1_D*(36)	8-C1, 12-D4

Net Name	Sheet Number-Location
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CPU1_D*(39)	8-C1, 12-D4
CPU1_D*(4)	8-C2, 12-D4
CPU1_D*(40)	8-C1, 12-D4
CPU1_D*(41)	8-C1, 12-D4
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CPU1_D*(43)	8-C1, 12-D4
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CPU1_D*(50)	8-C1, 12-D4
CPU1_D*(51)	8-C1, 12-D4
CPU1_D*(52)	8-C1, 12-D4
CPU1_D*(53)	8-C1, 12-D4
CPU1_D*(54)	8-C1, 12-D4
CPU1_D*(55)	8-C1, 12-D4
CPU1_D*(56)	8-C1, 12-D4
CPU1_D*(57)	8-C1, 12-D4
CPU1_D*(58)	8-C1, 12-D4
CPU1_D*(59)	8-C1, 12-D4
CPU1_D*(6)	8-C2, 12-D4
CPU1_D*(60)	8-C1, 12-D4
CPU1_D*(61)	8-C1, 12-D4
CPU1_D*(62)	8-C1, 12-D4
CPU1_D*(63)	8-C1, 12-D4
CPU1_D*(63:0)	12-D4
CPU1_D*(63:48)	8-C1
CPU1_D*(7)	8-C2, 12-D4
CPU1_D*(8)	8-C2, 12-D4
CPU1_D*(9)	8-C2, 12-D4
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CPU1_REQ*(1)	8-C4, 12-B2
CPU1_REQ*(2)	8-C4, 12-B2
CPU1_REQ*(3)	8-C4, 12-B2
CPU1_REQ*(4)	8-C4, 12-B2
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Net Name	Sheet Number-Location
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DMI1_RXN2	13-C1, 20-C1
DMI1_RXN3	13-C1, 20-C1
DMI1_RXP0	13-D1, 20-C1
DMI1_RXP1	13-C1, 20-C1
DMI1_RXP2	13-C1, 20-C1
DMI1_RXP3	13-C1, 20-C1
DMI1_TXN0	13-D1, 20-C1
DMI1_TXN1	13-D1, 20-C1
DMI1_TXN2	13-C1, 20-C1
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DMI1_TXP0	13-D1, 20-C1
DMI1_TXP1	13-D1, 20-C1
DMI1_TXP2	13-C1, 20-C1
DMI1_TXP3	13-C1, 20-B1
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IDE5_A2	19-C2, 35-C1, 35-C4, 46-C4
IDE5_CS1*	19-B2, 35-C2, 35-C4, 46-D4
IDE5_CS3*	19-B2, 35-C1, 35-C4, 46-D4
IDE5_D(0)	19-B2, 35-C2, 35-C4, 46-D4
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IDE5_D(10)	19-B2, 35-B4, 35-C1, 46-C3
IDE5_D(11)	19-B2, 35-B4, 35-C1, 46-C3
IDE5_D(12)	19-B2, 35-B4, 35-C1, 46-C3
IDE5_D(13)	19-B2, 35-B4, 35-C1, 46-C3
IDE5_D(14)	19-B2, 35-B4, 35-C1, 46-C3
IDE5_D(15)	19-B2, 35-B4, 35-C1, 46-B3
IDE5_D(2)	19-B2, 35-C2, 35-C4, 46-C4
IDE5_D(3)	19-B2, 35-C2, 35-C4, 46-C4
IDE5_D(4)	19-B2, 35-C2, 35-C4, 46-C4
IDE5_D(5)	19-B2, 35-C2, 35-C4, 46-C4
IDE5_D(6)	19-B2, 35-C2, 35-C4, 46-C4
IDE5_D(7)	19-B2, 35-C2, 35-C4, 46-C4
IDE5_D(8)	19-B2, 35-B4, 35-C1, 46-C4
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IDE5_IORDY	19-B4, 35-C2, 35-C4, 46-B3
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KBC3_BKLTON	24-A2, 36-C2, 46-B3
KBC3_BRIT	24-B4, 36-C2, 46-C4
KBC3_BRIT_DA	24-A4, 36-B2, 46-B2
KBC3_CAPSLED*	36-C4, 37-C3, 46-A2
KBC3_CHGEN	36-C2, 41-B4, 46-B3

Net Name	Sheet Number-Location
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KBC3_EZ_BTN0*	36-B1, 36-C4, 37-C4, 46-A2
KBC3_EZ_BTN1*	36-B1, 36-C4, 37-C3, 46-C2
KBC3_EZ_BTN2*	36-B1, 36-C4, 37-C4, 46-C2
KBC3_FANCTRL	34-A4, 36-B2, 46-B2
KBC3_IMVP4_PWRGD	13-A1, 20-B2, 36-B2, 46-C2
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KBC3_MD0	36-D1, 36-D4, 46-C4
KBC3_MD1	36-D1, 36-D4, 46-C4
KBC3_NUMLED*	36-C4, 37-C4, 46-B2
KBC3_PWRGD	11-C4, 20-A2, 22-B3, 26-A4, 36-C4, 46-B3
KBC3_PWRON	36-C4, 37-D2, 39-A4, 39-B2, 39-C2, 40-D2, 46-B3
KBC3_PWRSW*	11-C4, 36-B2, 36-D2, 36-D4, 37-C3, 46-B3
KBC3_QS*	36-C2, 41-B1, 41-B4, 46-C4
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KBC3_RSMRST*	20-A2, 22-B3, 36-C2, 46-B2
KBC3_RST*	36-D1, 36-D2, 36-D4, 40-C4, 46-C4
KBC3_RUNSCI*	20-C2, 22-C1, 36-C4, 46-A2
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KBC3_SCLED*	36-C4, 37-C4, 46-B3
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KBC3_SMDATA*	36-A2, 36-C1, 41-B1, 46-A2
KBC3_SPKMUTE	33-C2, 36-B2, 46-A2
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KBC3_THERM_ALERT*	11-C4, 36-B4, 46-C2
KBC3_THERM_SMCLK	11-C2, 36-A2, 46-C2
KBC3_THERM_SMDATA	11-C2, 36-C2, 46-C2
KBC3_THRM*	20-A4, 36-A2, 36-D1, 46-B3
KBC3_VRON	36-B2, 43-B2, 46-C4
KBC3_WAKESCI*	20-C2, 36-B2, 46-C2
KBC3_WLANON	29-C4, 36-C4, 46-B3
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KBC5_AVDD_ON	32-A1, 36-C4, 46-A2
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KBC5_KSI(2)	36-B4, 37-D3, 46-B3
KBC5_KSI(3)	36-B4, 37-D3, 46-B3
KBC5_KSI(4)	36-B4, 37-D3, 46-B3
KBC5_KSI(5)	36-B4, 37-D3, 46-B3
KBC5_KSI(6)	36-B4, 37-D3, 46-B3
KBC5_KSI(7)	36-B4, 37-D3, 46-B3
KBC5_KSO(0)	36-B4, 37-C3, 46-B3
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KBC5_KSO(1)	36-B4, 37-C3, 46-B3
KBC5_KSO(10)	36-B4, 37-C3, 46-A2
KBC5_KSO(11)	36-B4, 37-C3, 46-A2
KBC5_KSO(12)	36-B4, 37-C3, 46-A2
KBC5_KSO(13)	36-B4, 37-C3, 46-A2
KBC5_KSO(14)	36-B4, 37-C3, 46-A2
KBC5_KSO(15)	36-B4, 37-C3, 46-B2
KBC5_KSO(2)	36-B4, 37-C3, 46-B3
KBC5_KSO(3)	36-B4, 37-C3, 46-A3
KBC5_KSO(4)	36-B4, 37-C3, 46-A3
KBC5_KSO(5)	36-B4, 37-C3, 46-A3
KBC5_KSO(6)	36-B4, 37-C3, 46-A3
KBC5_KSO(7)	36-B4, 37-C3, 46-A3
KBC5_KSO(8)	36-B4, 37-C3, 46-B3
KBC5_KSO(9)	36-B4, 37-C3, 46-B3
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LAN3_EEDATA	30-B2, 31-A1, 31-B3, 46-A3
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LAN3_TRD0+	30-C1, 31-D4
LAN3_TRD1-	30-C1, 31-C4
LAN3_TRD1+	30-C1, 31-C4
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LAN3_TRD2+	30-C1, 31-C4
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LED5_GREEN	37-A3, 37-B1, 46-B3
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LPC3_LAD(1)	19-D2, 25-C3, 34-D2, 36-C2, 46-A3
LPC3_LAD(2)	19-D2, 25-C3, 34-D2, 36-C2, 46-A3
LPC3_LAD(3)	19-D2, 25-C3, 34-D2, 36-C2, 46-A3
LPC3_LFRAME*	19-D2, 25-C3, 34-C2, 36-C2, 46-B2
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LVDS1_A0+	13-B4, 24-C4
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MEM1_ADM(2)	14-C4, 17-B4
MEM1_ADM(3)	14-C4, 17-B4
MEM1_ADM(4)	14-C4, 17-B4
MEM1_ADM(5)	14-C4, 17-B4
MEM1_ADM(6)	14-C4, 17-B4
MEM1_ADM(7)	14-C4, 17-B4
MEM1_ADM(7:0)	14-C4, 17-B4
MEM1_ADQ(0)	14-D4, 17-D4
MEM1_ADQ(1)	14-D4, 17-D4
MEM1_ADQ(10)	14-D4, 17-D4
MEM1_ADQ(11)	14-D4, 17-D4
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MEM1_ADQ(13)	14-D4, 17-D4
MEM1_ADQ(14)	14-D4, 17-D4
MEM1_ADQ(15)	14-D4, 17-D4
MEM1_ADQ(16)	14-D4, 17-D4
MEM1_ADQ(17)	14-D4, 17-D4
MEM1_ADQ(18)	14-D4, 17-D4
MEM1_ADQ(19)	14-D4, 17-D4
MEM1_ADQ(2)	14-D4, 17-D4
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MEM1_ADQ(21)	14-D4, 17-D4
MEM1_ADQ(22)	14-D4, 17-D4
MEM1_ADQ(23)	14-D4, 17-D4
MEM1_ADQ(24)	14-D4, 17-D4
MEM1_ADQ(25)	14-D4, 17-D4
MEM1_ADQ(26)	14-D4, 17-D4
MEM1_ADQ(27)	14-D4, 17-D4
MEM1_ADQ(28)	14-D4, 17-D4
MEM1_ADQ(29)	14-D4, 17-D4
MEM1_ADQ(3)	14-D4, 17-D4
MEM1_ADQ(30)	14-D4, 17-D4
MEM1_ADQ(31)	14-D4, 17-D4
MEM1_ADQ(32)	14-D4, 17-D4
MEM1_ADQ(33)	14-D4, 17-D4
MEM1_ADQ(34)	14-D4, 17-D4
MEM1_ADQ(35)	14-D4, 17-D4

Net Name	Sheet Number-Location
MEM1_ADQ(36)	14-D4, 17-D4
MEM1_ADQ(37)	14-D4, 17-D4
MEM1_ADQ(38)	14-D4, 17-D4
MEM1_ADQ(39)	14-D4, 17-D4
MEM1_ADQ(4)	14-D4, 17-D4
MEM1_ADQ(40)	14-D4, 17-D4
MEM1_ADQ(41)	14-D4, 17-D4
MEM1_ADQ(42)	14-D4, 17-D4
MEM1_ADQ(43)	14-D4, 17-D4
MEM1_ADQ(44)	14-D4, 17-D4
MEM1_ADQ(45)	14-D4, 17-D4
MEM1_ADQ(46)	14-D4, 17-D4
MEM1_ADQ(47)	14-D4, 17-D4
MEM1_ADQ(48)	14-D4, 17-D4
MEM1_ADQ(49)	14-D4, 17-D4
MEM1_ADQ(5)	14-D4, 17-D4
MEM1_ADQ(50)	14-D4, 17-D4
MEM1_ADQ(51)	14-D4, 17-D4
MEM1_ADQ(52)	14-D4, 17-D4
MEM1_ADQ(53)	14-D4, 17-D4
MEM1_ADQ(54)	14-D4, 17-D4
MEM1_ADQ(55)	14-D4, 17-D4
MEM1_ADQ(56)	14-D4, 17-D4
MEM1_ADQ(57)	14-D4, 17-D4
MEM1_ADQ(58)	14-D4, 17-D4
MEM1_ADQ(59)	14-D4, 17-D4
MEM1_ADQ(6)	14-D4, 17-D4
MEM1_ADQ(60)	14-D4, 17-D4
MEM1_ADQ(61)	14-D4, 17-D4
MEM1_ADQ(62)	14-D4, 17-D4
MEM1_ADQ(63)	14-D4, 17-D4
MEM1_ADQ(63:0)	14-D4, 17-D4
MEM1_ADQ(7)	14-D4, 17-D4
MEM1_ADQ(8)	14-D4, 17-D4
MEM1_ADQ(9)	14-D4, 17-D4
MEM1_ADQS(0)	14-C4, 17-B4
MEM1_ADQS(1)	14-C4, 17-B4
MEM1_ADQS(2)	14-C4, 17-B4
MEM1_ADQS(3)	14-C4, 17-B4
MEM1_ADQS(4)	14-C4, 17-B4

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Net Name	Sheet Number-Location
MEM1_ADQS(5)	14-C4, 17-B4
MEM1_ADQS(6)	14-C4, 17-B4
MEM1_ADQS(7)	14-C4, 17-B4
MEM1_ADQS(7:0)	14-C4, 17-B4
MEM1_ADQS*(0)	14-C4, 17-B4
MEM1_ADQS*(1)	14-C4, 17-B4
MEM1_ADQS*(2)	14-C4, 17-B4
MEM1_ADQS*(3)	14-C4, 17-B4
MEM1_ADQS*(4)	14-C4, 17-B4
MEM1_ADQS*(5)	14-C4, 17-B4
MEM1_ADQS*(6)	14-C4, 17-B4
MEM1_ADQS*(7)	14-C4, 17-B4
MEM1_ADQS*(7:0)	14-C4, 17-B4
MEM1_AMA(0)	14-B4, 17-D4, 18-D3
MEM1_AMA(1)	14-B4, 17-D4, 18-D3
MEM1_AMA(10)	14-B4, 17-D4, 18-D3
MEM1_AMA(11)	14-B4, 17-D4, 18-D3
MEM1_AMA(12)	14-B4, 17-D4, 18-D3
MEM1_AMA(13)	14-B4, 17-D4, 18-D3
MEM1_AMA(13:0)	14-B4, 17-D4, 18-D3
MEM1_AMA(2)	14-B4, 17-D4, 18-D3
MEM1_AMA(3)	14-B4, 17-D4, 18-D3
MEM1_AMA(4)	14-B4, 17-D4, 18-D3
MEM1_AMA(5)	14-B4, 17-D4, 18-D3
MEM1_AMA(6)	14-B4, 17-D4, 18-D3
MEM1_AMA(7)	14-B4, 17-D4, 18-D3
MEM1_AMA(8)	14-B4, 17-D4, 18-D3
MEM1_AMA(9)	14-B4, 17-D4, 18-D3
MEM1_ARAS*	14-B4, 17-C4, 18-C4
MEM1_AWE*	14-B4, 17-C4, 18-C4
MEM1_BBS0*	14-C2, 17-C2, 18-C4
MEM1_BBS1*	14-C2, 17-C2, 18-C4
MEM1_BBS2*	14-C2, 17-C2, 18-C4
MEM1_BCAS*	14-B2, 17-C2, 18-C4
MEM1_BDM(0)	14-C2, 17-B2
MEM1_BDM(1)	14-C2, 17-B2
MEM1_BDM(2)	14-C2, 17-B2
MEM1_BDM(3)	14-C2, 17-B2
MEM1_BDM(4)	14-C2, 17-B2
MEM1_BDM(5)	14-C2, 17-B2

Net Name	Sheet Number-Location
MEM1_BDM(6)	14-C2, 17-B2
MEM1_BDM(7)	14-C2, 17-B2
MEM1_BDM(7:0)	14-C2, 17-B2
MEM1_BDQ(0)	14-A2, 17-D2
MEM1_BDQ(1)	14-A2, 17-D2
MEM1_BDQ(10)	14-A2, 17-D2
MEM1_BDQ(11)	14-A2, 17-D2
MEM1_BDQ(12)	14-A2, 17-D2
MEM1_BDQ(13)	14-A2, 17-D2
MEM1_BDQ(14)	14-A2, 17-D2
MEM1_BDQ(15)	14-A2, 17-D2
MEM1_BDQ(16)	14-A2, 17-D2
MEM1_BDQ(17)	14-A2, 17-D2
MEM1_BDQ(18)	14-A2, 17-D2
MEM1_BDQ(19)	14-A2, 17-D2
MEM1_BDQ(2)	14-A2, 17-D2
MEM1_BDQ(20)	14-A2, 17-D2
MEM1_BDQ(21)	14-A2, 17-D2
MEM1_BDQ(22)	14-A2, 17-D2
MEM1_BDQ(23)	14-A2, 17-D2
MEM1_BDQ(24)	14-A2, 17-D2
MEM1_BDQ(25)	14-A2, 17-D2
MEM1_BDQ(26)	14-A2, 17-D2
MEM1_BDQ(27)	14-A2, 17-D2
MEM1_BDQ(28)	14-A2, 17-D2
MEM1_BDQ(29)	14-A2, 17-D2
MEM1_BDQ(3)	14-A2, 17-D2
MEM1_BDQ(30)	14-A2, 17-D2
MEM1_BDQ(31)	14-A2, 17-D2
MEM1_BDQ(32)	14-A2, 17-D2
MEM1_BDQ(33)	14-A2, 17-D2
MEM1_BDQ(34)	14-A2, 17-D2
MEM1_BDQ(35)	14-A2, 17-D2
MEM1_BDQ(36)	14-A2, 17-D2
MEM1_BDQ(37)	14-A2, 17-D2
MEM1_BDQ(38)	14-A2, 17-D2
MEM1_BDQ(39)	14-A2, 17-D2
MEM1_BDQ(4)	14-A2, 17-D2
MEM1_BDQ(40)	14-A2, 17-D2
MEM1_BDQ(41)	14-A2, 17-D2

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Net Name	Sheet Number-Location
MEM1_BDQ(42)	14-A2, 17-D2
MEM1_BDQ(43)	14-A2, 17-D2
MEM1_BDQ(44)	14-A2, 17-D2
MEM1_BDQ(45)	14-A2, 17-D2
MEM1_BDQ(46)	14-A2, 17-D2
MEM1_BDQ(47)	14-A2, 17-D2
MEM1_BDQ(48)	14-A2, 17-D2
MEM1_BDQ(49)	14-A2, 17-D2
MEM1_BDQ(5)	14-A2, 17-D2
MEM1_BDQ(50)	14-A2, 17-D2
MEM1_BDQ(51)	14-A2, 17-D2
MEM1_BDQ(52)	14-A2, 17-D2
MEM1_BDQ(53)	14-A2, 17-D2
MEM1_BDQ(54)	14-A2, 17-D2
MEM1_BDQ(55)	14-A2, 17-D2
MEM1_BDQ(56)	14-A2, 17-D2
MEM1_BDQ(57)	14-A2, 17-D2
MEM1_BDQ(58)	14-A2, 17-D2
MEM1_BDQ(59)	14-A2, 17-D2
MEM1_BDQ(6)	14-A2, 17-D2
MEM1_BDQ(60)	14-A2, 17-D2
MEM1_BDQ(61)	14-A2, 17-D2
MEM1_BDQ(62)	14-A2, 17-D2
MEM1_BDQ(63)	14-A2, 17-D2
MEM1_BDQ(63:0)	14-A2, 17-D2
MEM1_BDQ(7)	14-A2, 17-D2
MEM1_BDQ(8)	14-A2, 17-D2
MEM1_BDQ(9)	14-A2, 17-D2
MEM1_BDQS(0)	14-C2, 17-B2
MEM1_BDQS(1)	14-C2, 17-B2
MEM1_BDQS(2)	14-C2, 17-B2
MEM1_BDQS(3)	14-C2, 17-B2
MEM1_BDQS(4)	14-C2, 17-B2
MEM1_BDQS(5)	14-C2, 17-B2
MEM1_BDQS(6)	14-C2, 17-B2
MEM1_BDQS(7)	14-C2, 17-B2
MEM1_BDQS(7:0)	14-C2, 17-B2
MEM1_BDQS*(0)	14-C2, 17-B2
MEM1_BDQS*(1)	14-C2, 17-B2
MEM1_BDQS*(2)	14-C2, 17-B2

Net Name	Sheet Number-Location
MEM1_BDQS*(3)	14-C2, 17-B2
MEM1_BDQS*(4)	14-C2, 17-B2
MEM1_BDQS*(5)	14-C2, 17-B2
MEM1_BDQS*(6)	14-C2, 17-B2
MEM1_BDQS*(7)	14-C2, 17-B2
MEM1_BDQS*(7:0)	14-C2, 17-B2
MEM1_BMA(0)	14-B2, 17-D2, 18-C3
MEM1_BMA(1)	14-B2, 17-D2, 18-C3
MEM1_BMA(10)	14-B2, 17-D2, 18-C3
MEM1_BMA(11)	14-B2, 17-D2, 18-C3
MEM1_BMA(12)	14-B2, 17-D2, 18-C3
MEM1_BMA(13)	14-B2, 17-D2, 18-C3
MEM1_BMA(13:0)	14-B2, 17-D2, 18-C3
MEM1_BMA(2)	14-B2, 17-D2, 18-C3
MEM1_BMA(3)	14-B2, 17-D2, 18-C3
MEM1_BMA(4)	14-B2, 17-D2, 18-C3
MEM1_BMA(5)	14-B2, 17-D2, 18-C3
MEM1_BMA(6)	14-B2, 17-D2, 18-C3
MEM1_BMA(7)	14-B2, 17-D2, 18-C3
MEM1_BMA(8)	14-B2, 17-D2, 18-C3
MEM1_BMA(9)	14-B2, 17-D2, 18-C3
MEM1_BRAS*	14-B2, 17-C2, 18-B4
MEM1_BWE*	14-B2, 17-C2, 18-B4
MEM1_CKE0	13-B1, 17-C4, 18-C4
MEM1_CKE1	13-B1, 17-C4, 18-C4
MEM1_CKE2	13-B1, 17-C2, 18-C4
MEM1_CKE3	13-B1, 17-C2, 18-C4
MEM1_CS0*	13-B1, 17-C4, 18-D4
MEM1_CS1*	13-B1, 17-C4, 18-D4
MEM1_CS2*	13-B1, 17-C2, 18-D4
MEM1_CS3*	13-B1, 17-C2, 18-C4
MEM1_ODT0	13-A1, 17-B4, 18-C4
MEM1_ODT1	13-A1, 17-B4, 18-C4
MEM1_ODT2	13-A1, 17-B2, 18-C4
MEM1_ODT3	13-A1, 17-B2, 18-C4
MEM3_OVERT*	11-C2, 36-B4, 46-B3
PCI3_AD(0)	20-D4, 26-C4, 29-D4, 30-C4, 46-C4
PCI3_AD(1)	20-D4, 26-C4, 29-D4, 30-C4, 46-C4

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Net Name	Sheet Number-Location
PCI3_AD(10)	20-D4, 26-C4, 29-D4, 30-C4, 46-B3
PCI3_AD(11)	20-D4, 26-C4, 29-D4, 30-C4, 46-B3
PCI3_AD(12)	20-D4, 26-C4, 29-D4, 30-C4, 46-B3
PCI3_AD(13)	20-D4, 26-C4, 29-D4, 30-C4, 46-B3
PCI3_AD(14)	20-D4, 26-C4, 29-D4, 30-C4, 46-B3
PCI3_AD(15)	20-D4, 26-C4, 29-D4, 30-C4, 46-B3
PCI3_AD(16)	20-D4, 26-C4, 29-D4, 30-C4, 46-B3
PCI3_AD(17)	20-D4, 26-C4, 29-D4, 30-C4, 46-B3
PCI3_AD(18)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(19)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(2)	20-D4, 26-C4, 29-D4, 30-C4, 46-C4
PCI3_AD(20)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(21)	20-D4, 26-C4, 29-D4, 30-B4, 30-C4, 46-D2
PCI3_AD(22)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(23)	20-D4, 26-C4, 29-C2, 29-D4, 30-C4, 46-D2
PCI3_AD(24)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(25)	20-D4, 26-B4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(26)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(27)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(28)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2

Net Name	Sheet Number-Location
PCI3_AD(29)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(3)	20-D4, 26-C4, 29-D4, 30-C4, 46-C4
PCI3_AD(30)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(31)	20-D4, 26-C4, 29-D4, 30-C4, 46-D2
PCI3_AD(31:0)	20-D4, 26-C4, 29-D4, 30-C4
PCI3_AD(4)	20-D4, 26-C4, 29-D4, 30-C4, 46-C4
PCI3_AD(5)	20-D4, 26-C4, 29-D4, 30-C4, 46-C4
PCI3_AD(6)	20-D4, 26-C4, 29-D4, 30-C4, 46-B4
PCI3_AD(7)	20-D4, 26-C4, 29-D4, 30-C4, 46-B4
PCI3_AD(8)	20-D4, 26-C4, 29-D4, 30-C4, 46-B4
PCI3_AD(9)	20-D4, 26-C4, 29-D4, 30-C4, 46-B4
PCI3_CBE0*	20-C3, 26-B4, 29-B2, 30-B4, 46-B4
PCI3_CBE1*	20-C3, 26-B4, 29-B4, 30-B4, 46-B4
PCI3_CBE2*	20-C3, 26-B4, 29-B4, 30-B4, 46-B4
PCI3_CBE3*	20-C3, 26-B4, 29-C4, 30-B4, 46-B4
PCI3_CLKRUN*	20-B2, 22-D1, 26-A4, 29-B4, 30-A4, 34-C2, 36-B2, 46-B2
PCI3_DEVSEL*	20-C3, 22-C1, 26-A4, 29-B2, 30-B4, 46-B2
PCI3_FRAME*	20-B4, 22-C1, 26-B4, 29-B2, 30-B4, 46-C2
PCI3_GNT0*	20-D3, 26-B4, 46-B4
PCI3_GNT1*	20-D2, 29-C2, 46-B4
PCI3_GNT2*	20-D3, 22-B1, 30-B4, 46-B4
PCI3_GNT3*	20-D3, 22-B1, 46-B4
PCI3_INTA*	20-B4, 22-C1, 26-C3, 46-B4

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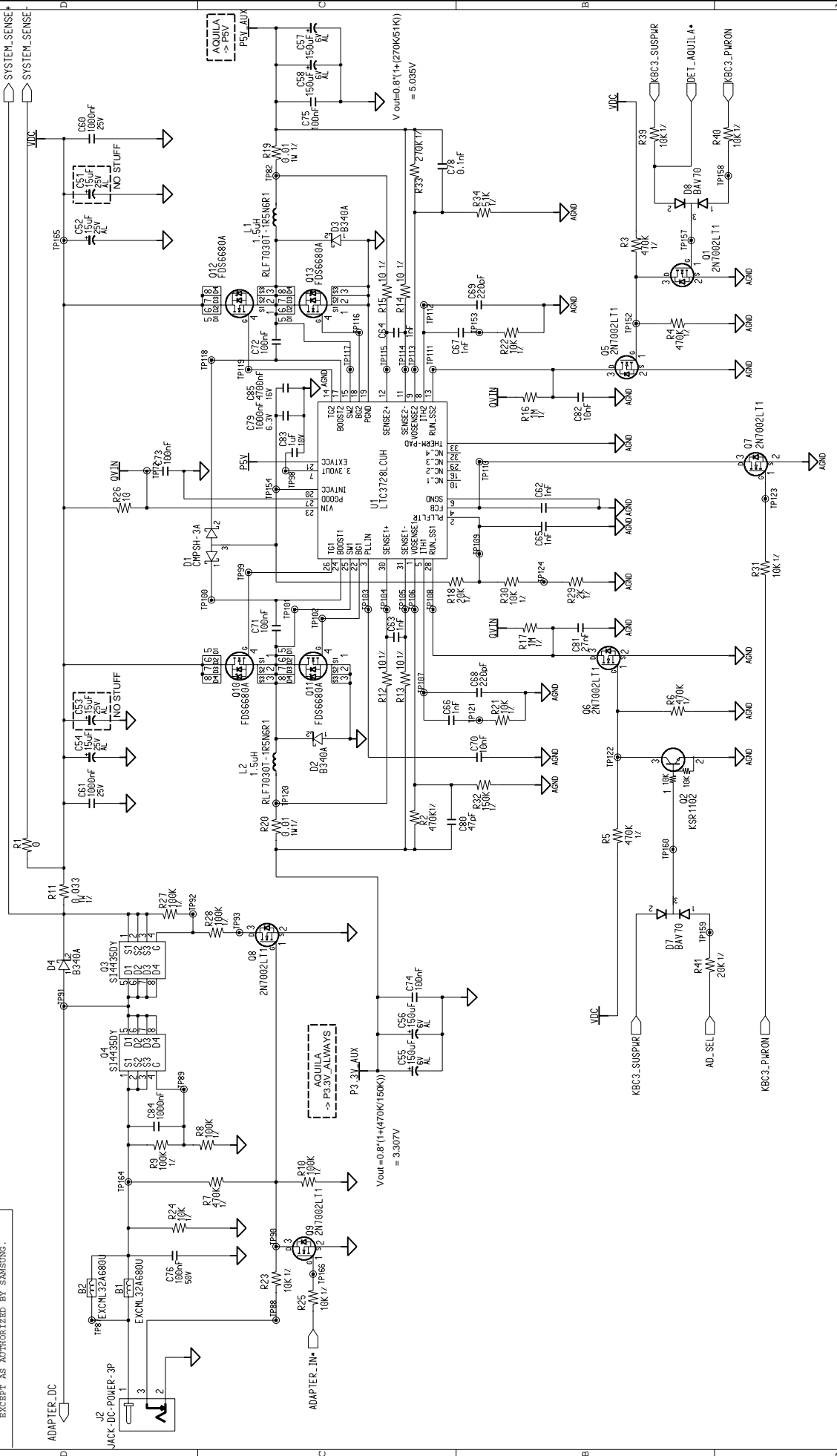
Net Name	Sheet Number-Location
PCI3_INTB*	20-B4, 22-C1, 26-B3, 46-B4
PCI3_INTC*	20-B4, 22-C1, 26-B3, 46-B4
PCI3_INTD*	20-B4, 22-C1, 46-B4
PCI3_INTE*	20-B3, 22-C1, 29-C2, 46-B4
PCI3_INTF*	20-B3, 22-C1, 29-C4, 46-B4
PCI3_INTG*	20-B3, 22-C1, 30-B4, 46-B4
PCI3_INTH*	20-B3, 22-C1, 46-B4
PCI3_IRDY*	20-C3, 22-C1, 26-B4, 29-B4, 30-B4, 46-B4
PCI3_PAR	20-C3, 22-D1, 26-B4, 29-B2, 30-B4, 46-C4
PCI3_PERR*	20-C3, 22-C1, 26-A4, 29-B4, 30-B4, 46-B4
PCI3_PLOCK*	20-C3, 22-C1, 46-C2
PCI3_REQ0*	20-D3, 22-C1, 26-B4, 46-B4
PCI3_REQ1*	20-D3, 22-C1, 29-C4, 46-B4
PCI3_REQ2*	20-D3, 22-C1, 30-B4, 46-B4
PCI3_REQ3*	20-D3, 22-C1, 46-B4
PCI3_RST*	20-C3, 26-A4, 29-C2, 30-B4, 46-A4
PCI3_SERR*	20-C3, 22-C1, 26-A4, 29-B4, 30-B4, 46-B4
PCI3_STOP*	20-C3, 22-C1, 26-A4, 29-B2, 30-B4, 46-B4
PCI3_TRDY*	20-C3, 22-C1, 26-B4, 29-B2, 30-B4, 46-A4
PCIE3_WAKE*	20-B2, 22-C3, 46-C2
PLT3_RST*	20-A3, 20-C3, 46-A4
PLT3_RSTF*	13-A1, 20-A2, 20-A3, 25-C4, 34-C2, 35-B4, 35-C2, 36-C2, 46-A4
QUICK3_BOOT*	36-B1, 36-B2, 46-B2
S1-	42-C4, 42-D1, 46-D4
S1+	42-B4, 42-C4, 42-D1, 46-D4
S2-	42-B1, 42-B4, 46-D4
S2+	42-B1, 42-B4, 42-C4, 46-D4
SATA3_DET*	20-C2, 35-B4, 46-A4
SATA3_RN	19-C4, 35-B4
SATA3_RP	19-B4, 35-B4
SATA3_TN	19-B4, 35-B4

Net Name	Sheet Number-Location
SATA3_TP	19-B4, 35-B4
SMB3_ALERT*	20-C2, 22-C3, 46-C2
SMB3_CLK	7-A4, 16-B2, 20-D2, 22-D3, 46-C4
SMB3_DATA	7-A4, 16-B2, 20-D2, 22-D3, 46-A4
SMB3_LINKALERT*	20-D2, 22-C3, 46-C2
SPDIF5_ON*	33-A1, 36-C2, 46-A4
SPDIF5_OUT	32-C4, 33-B2, 46-A4
SPROM3_DIN	30-B2, 31-A3, 46-A4
SPROM3_DOUT	30-B2, 31-A3, 46-C2
SYSTEM_SENSE-	37-D1, 41-C4, 46-D2
SYSTEM_SENSE+	37-D2, 41-C4, 46-D2
TPM3_PACCESS	34-C1, 36-B4, 46-B2
USB3_P0-	20-A1, 34-B2
USB3_P0+	20-A1, 34-B2
USB3_P1-	20-A1, 37-C2
USB3_P1+	20-A1, 37-C2
USB3_P2-	20-A1, 34-B2
USB3_P2+	20-A1, 34-B2
USB3_P3-	20-A1, 37-A4
USB3_P3+	20-A1, 37-A4
VGA2_DDCCLK	13-C4, 23-A4, 46-C2
VGA2_DDCDATA	13-C4, 23-A4, 46-B2
VGA3_BLUE	13-C4, 23-C4, 46-A4
VGA3_C	13-D4, 37-C1, 46-D4
VGA3_COMP	13-D4, 46-A4
VGA3_GREEN	13-C4, 23-C4, 46-A4
VGA3_HSYNC	13-C4, 23-B4, 46-A4
VGA3_RED	13-C4, 23-C4, 46-B4
VGA3_VSYNC	13-C4, 23-B4, 46-A4
VGA3_Y	13-D4, 37-C2, 46-D4
VOA-	42-A2, 42-C4
VOA+	42-B4, 42-C4
VOS-	42-C1, 42-C4, 46-D4
VREF3_OUT_MIC	32-C2, 33-B2, 46-D2
VTTTPWRGD	42-A4, 42-D4, 43-D2, 46-B4

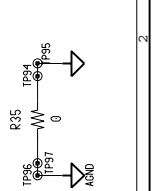
9 Schematic Diagram

9-2 DCDC BOARD

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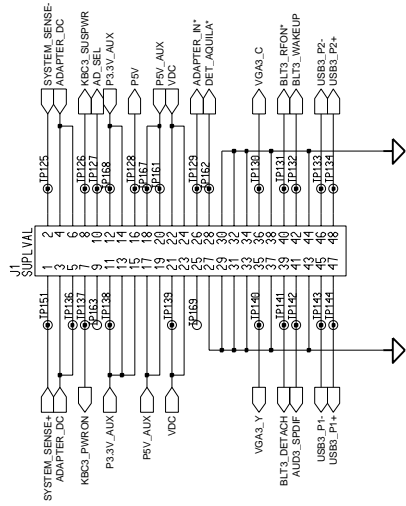


DRWN	SEO, HJ	DATE	02/08/2003	TITLE	AQUILA-C
CHECK	HA, JS	REV.	REV. 310*	PR	DC-DC BOARD
APPROVAL	LEE, CH	REV.	10		3.3V & 5V GENERATION
MODULE CODE		LAST EDIT	March, 9, 2002 4:21:54 PM	PAGE	2 OF 3

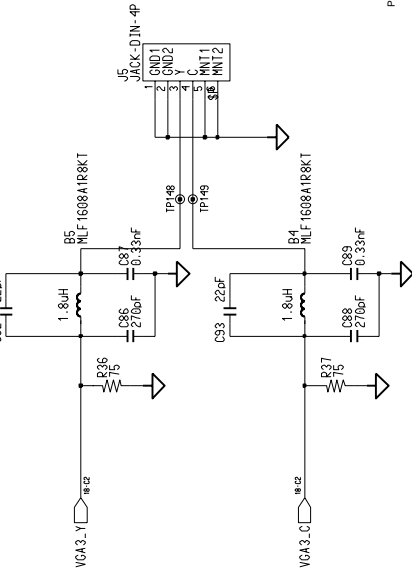


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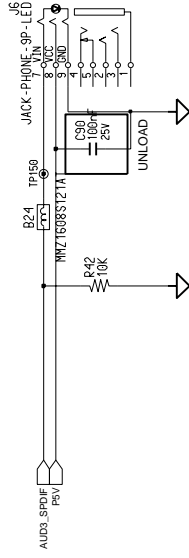
**CHANGE THIS CONNECTOR TO HEADER < 12809A-48G5T >
 FROM DCDC TO MAIN BOARD**



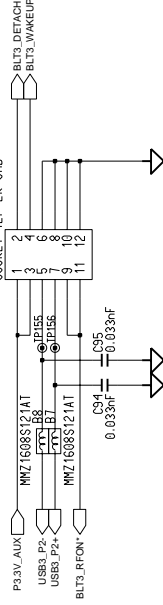
SUPER - VHS TV OUT



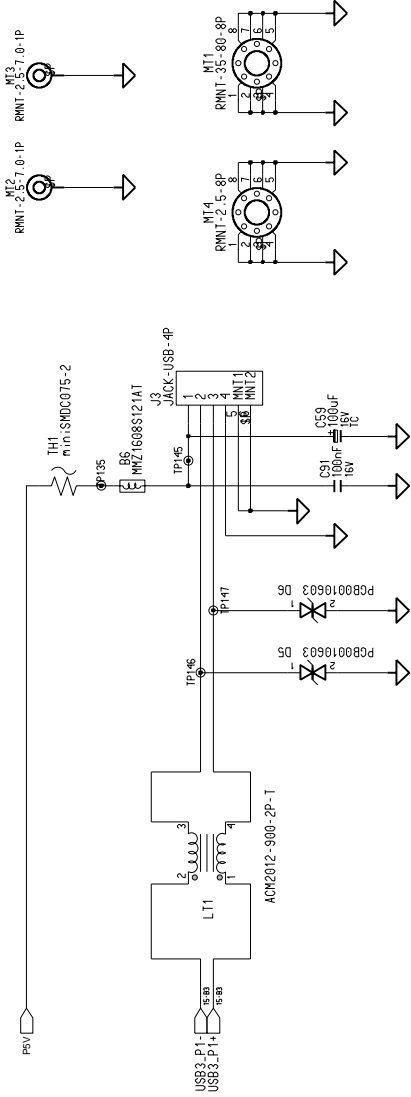
SPDIF OUT



bluetooth connector

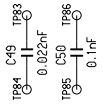


USB
 90ohm +- 10%



REV1 6
20 03

NO	CONNECTION	DATE	BY	REV	DD	REVISION	STEP
1	N.C.						
2	1-2						
3	2-3						
4	3-1						
5	1-2-3						
6	N.C.						
7	1-2						
8	2-3						
9	3-1						
10	1-2-3						



RAW	DATE	TITLE
SEO, HJ	02/08/2003	AQUILA_C
HA, JS	REV. 31P	DC-DC BOARD
LEE, CH	REV 10	CONNECTOR & PORT
MODULE CODE	LAST EDIT	

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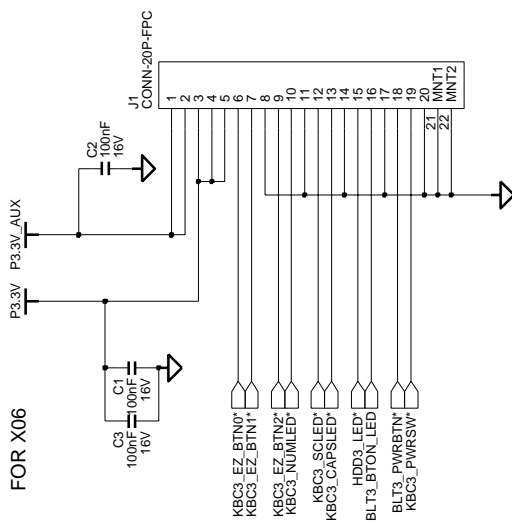
SAMSUNG
 ELECTRONICS
 PART NO. BA411-#####

9 Schematic Diagram

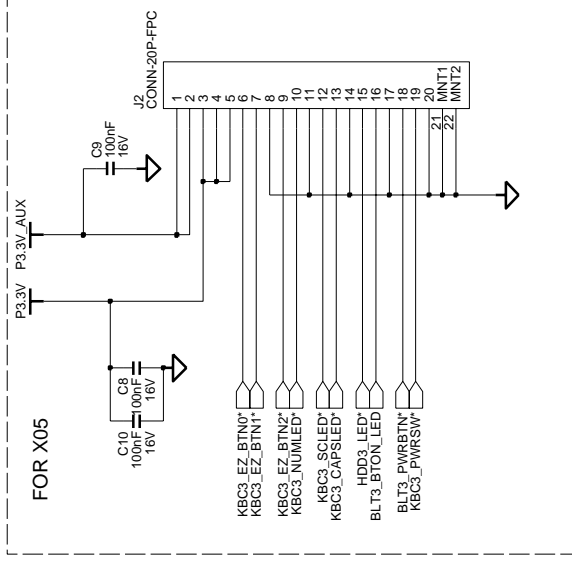
9-3 ONTOP BOARD

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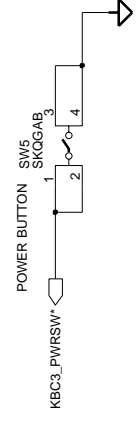
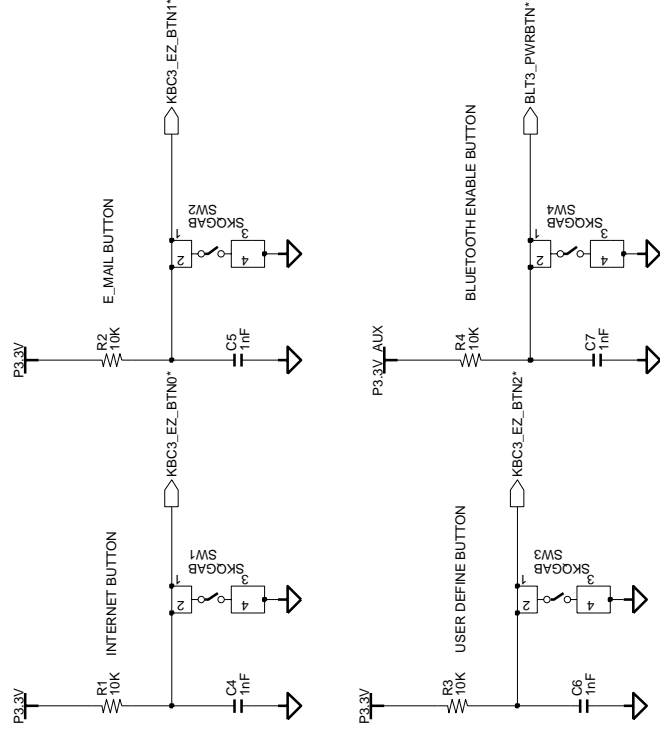
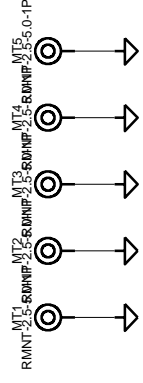
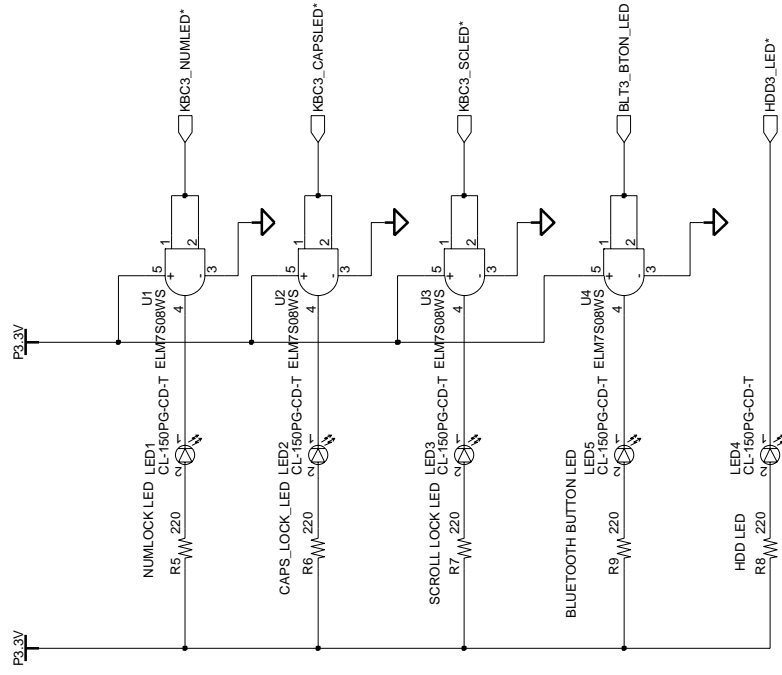
FOR X06



FOR X05



NO_STUFF



DRAW	GUO, MICKY	DATE	5/25/2005	TITLE	AGUILA-SO
CHECK	ZHOU, PHIL	DEV. STEP	MP	ONTOP PCB	ONTOP MAIN
APPROVAL	CHEN, ANTONIO	REV	1.0	ONTOP MAIN	ONTOP MAIN
MODULE CODE		LAST EDIT	May, 25, 2005, 10:09:07 AM	PAGE	1 OF 1