



HARRIS

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# IRF530/531/532/533 IRF530R/531R/532R/533R

N-Channel Power MOSFETs  
Avalanche Energy Rated\*

May 1992

### Features

- 12A and 14A, 80V - 100V
- $r_{DS(on)} = 0.16\Omega$  and  $0.23\Omega$
- Single Pulse Avalanche Energy Rated\*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

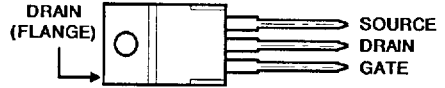
### Description

The IRF530, IRF531, IRF532, and IRF533 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF530R, IRF531R, IRF532R and IRF533R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

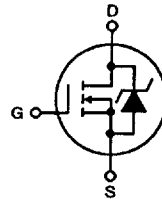
### Package

TO-220AB  
TOP VIEW



### Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



### Absolute Maximum Ratings ( $T_C = +25^\circ\text{C}$ ), Unless Otherwise Specified

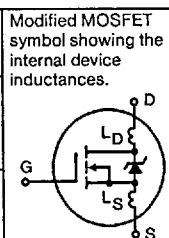
	IRF530 IRF530R	IRF531 IRF531R	IRF532 IRF532R	IRF533 IRF533R	UNITS
Drain-Source Voltage (1) .....	$V_{DS}$ 100	80	100	80	V
Drain-Gate Voltage ( $R_{GS} = 20k\Omega$ ) (1) .....	$V_{DGR}$ 100	80	100	80	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$ .....	$I_D$ 14	14	12	12	A
$T_C = +100^\circ\text{C}$ .....	$I_D$ 10	10	8.3	8.3	A
Pulsed Drain Current (3) .....	$I_{DM}$ 56	56	48	48	A
Gate-Source Voltage .....	$V_{GS}$ $\pm 20$	$\pm 20$	$\pm 20$	$\pm 20$	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$ .....	$P_D$ 79	79	79	79	W
Linear Derating Factor .....	0.53	0.53	0.53	0.53	W/ $^\circ\text{C}$
Inductive Current, Clamped .....	$I_{LM}$ 56	56	48	48	A
(See Figure 14, $L = 100\mu\text{H}$ )					
Single Pulse Avalanche Energy Rating (4) .....	$E_{AS}^*$ 69	69	69	69	mJ
Operating and Storage Junction .....	$T_J, T_{STG}$ -55 to +175	-55 to +175	-55 to +175	-55 to +175	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering .....	$T_L$ 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

#### NOTES:

- $T_J = +25^\circ\text{C}$  to  $+150^\circ\text{C}$ .
  - Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
  - Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
  - $V_{DD} = 25\text{V}$ , starting  $T_J = +25^\circ\text{C}$ ,  $L = 530\mu\text{H}$ ,  $R_{GS} = 25\Omega$ ,  $I_{PEAK} = 14\text{A}$ . See Figure 15.
- \*R Suffix Types Only

Electrical Characteristics  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF530/532, IRF530R/532R IRF531/533, IRF531R/533R	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250 $\mu$ A	100	-	-	V
			80	-	-	V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 $\mu$ A	2.0	-	4.0	V
Gate-Source Leakage Forward	I <sub>GSS</sub>	V <sub>GS</sub> = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I <sub>GSS</sub>	V <sub>GS</sub> = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = Max Rating, V <sub>GS</sub> = 0V	-	-	250	$\mu$ A
		V <sub>DS</sub> = Max Rating x 0.8, V <sub>GS</sub> = 0V, T <sub>J</sub> = +125 $^\circ$ C	-	-	1000	$\mu$ A
On-State Drain Current (Note 2) IRF530/531, IRF530R/531R IRF532/533, IRF532R/533R	I <sub>D(ON)</sub>	V <sub>DS</sub> > I <sub>D(ON)</sub> x r <sub>DS(ON)</sub> Max, V <sub>GS</sub> = 10V	14	-	-	A
			12	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF530/531, IRF530R/531R IRF532/533, IRF532R/533R	r <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8.3A	-	0.14	0.16	$\Omega$
			-	0.20	0.23	$\Omega$
Forward Transconductance (Note 2)	g <sub>fs</sub>	V <sub>DS</sub> $\geq$ 50V, I <sub>D</sub> = 8.3A	5.1	7.6	-	S( $\bar{S}$ )
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz	-	600	-	pF
Output Capacitance	C <sub>OSS</sub>	See Figure 10	-	250	-	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	50	-	pF
Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>DD</sub> = 50V, I <sub>D</sub> $\approx$ 14A, R <sub>G</sub> = 12 $\Omega$ See Figure 18. (MOSFET switching times are essentially independent of operating temperature)	-	12	15	ns
Rise Time	t <sub>r</sub>		-	35	51	ns
Turn-Off Delay Time	t <sub>d(OFF)</sub>		-	25	35	ns
Fall Time	t <sub>f</sub>		-	25	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q <sub>g</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 14A, V <sub>DS</sub> = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	18	26	nC
Gate-Source Charge	Q <sub>gs</sub>		-	4	-	nC
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>		-	7	-	nC
Internal Drain Inductance	L <sub>D</sub>	Measured from the contact screw on tab to center of die	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH



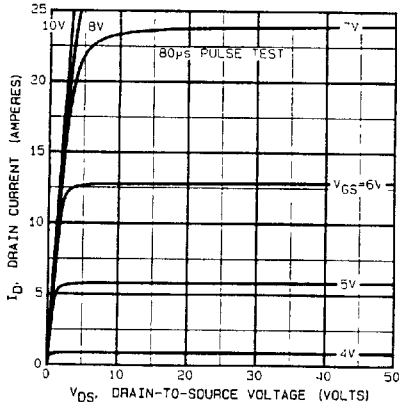
Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I <sub>S</sub>	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	14	A
Pulse Source Current (Body Diode) (Note 3)	I <sub>SM</sub>		-	-	56	A
Diode Forward Voltage (Note 2)	V <sub>SD</sub>	T <sub>J</sub> = +25 $^\circ$ C, I <sub>S</sub> = 14A, V <sub>GS</sub> = 0V	-	-	2.5	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = +25 $^\circ$ C, I <sub>F</sub> = 14A, di <sub>F</sub> /dt = 100A/ $\mu$ s	5.5	120	250	ns
Reverse Recovered Charge	Q <sub>RR</sub>	T <sub>J</sub> = +25 $^\circ$ C, I <sub>F</sub> = 14A, di <sub>F</sub> /dt = 100A/ $\mu$ s	0.26	0.6	1.3	$\mu$ C
Forward Turn-on Time	t <sub>ON</sub>	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .	-	-	-	-

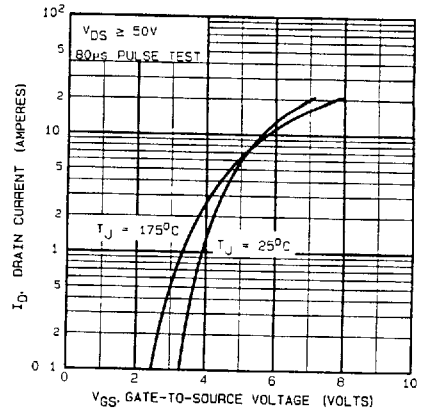
NOTES: 1. T<sub>J</sub> = +25 $^\circ$ C to +150 $^\circ$ C  
 2. Pulse Test: Pulse width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2%  
 3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)  
 4. V<sub>DD</sub> = 25V, Start T<sub>J</sub> = +25 $^\circ$ C, L = 350 $\mu$ H, R<sub>GS</sub> = 25 $\Omega$ , I<sub>PEAK</sub> = 14A (See Figure 15)

4  
N-CHANNEL  
POWER MOSFETS

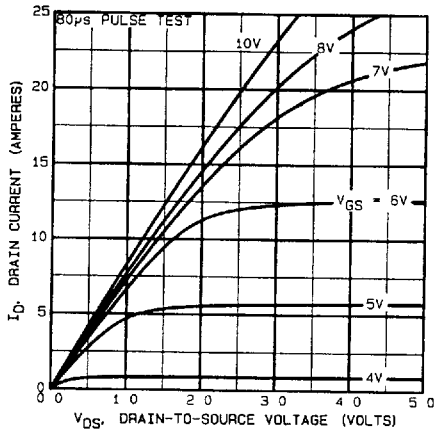
**Performance Curves**



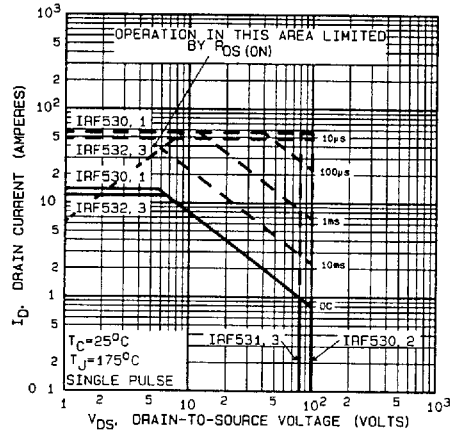
**FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS**



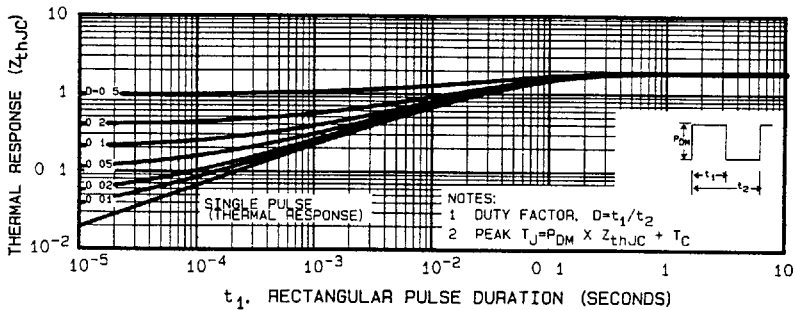
**FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS**



**FIGURE 3. TYPICAL SATURATION CHARACTERISTICS**



**FIGURE 4. MAXIMUM SAFE OPERATING AREA**



**FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION**

Performance Curves (Continued)

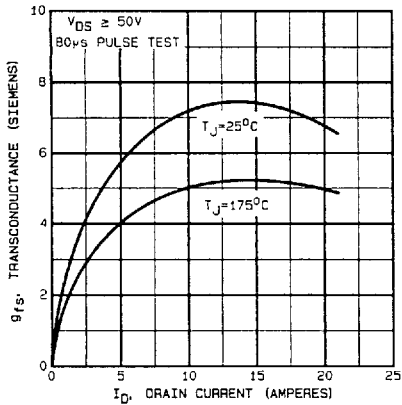


FIGURE 6. TRANSCONDUCTANCE vs DRAIN CURRENT

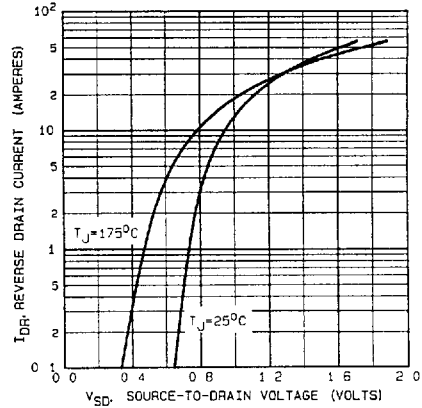


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

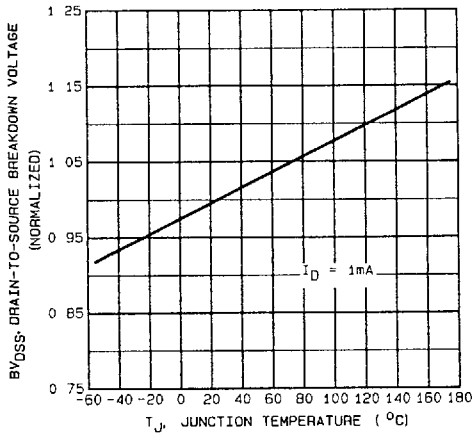


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

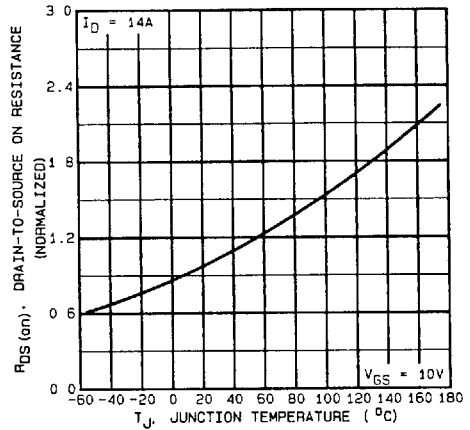


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

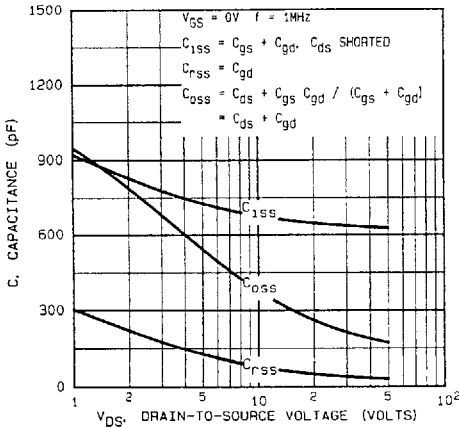


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

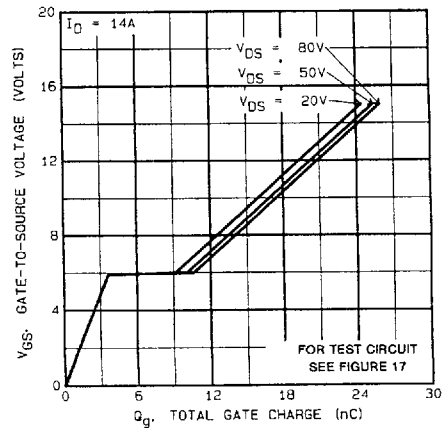
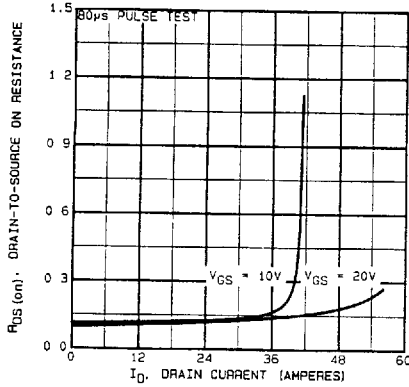
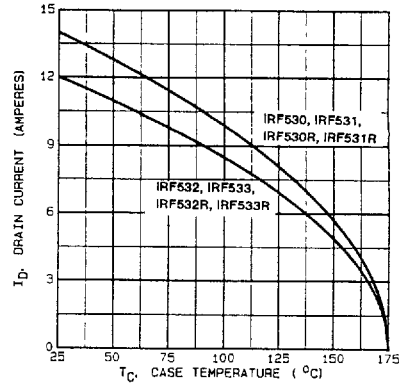


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

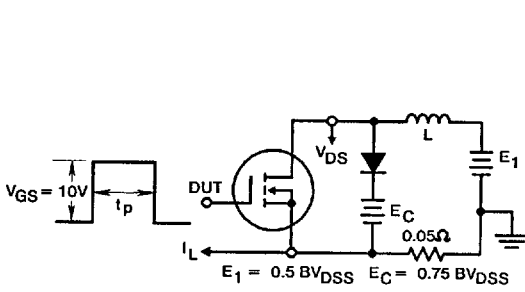
**Performance Curves (Continued)**



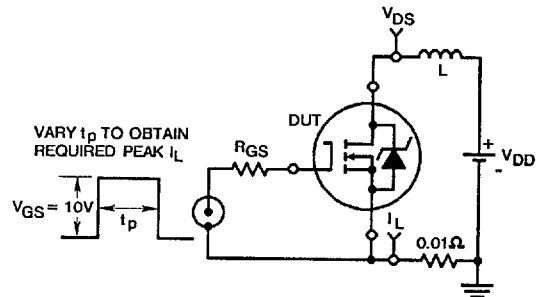
**FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT**



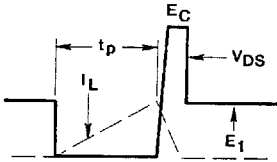
**FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE**



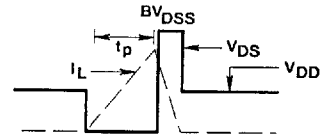
**FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT**



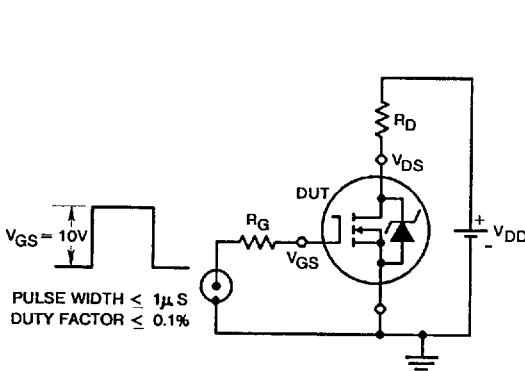
**FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT**



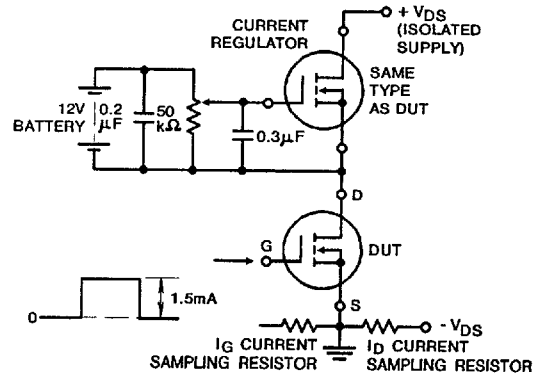
**FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS**



**FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS**



**FIGURE 16. SWITCHING TIME TEST CIRCUIT**



**FIGURE 17. GATE CHARGE TEST CIRCUIT**