SOT-223 SCR

Silicon Controlled Rectifiers
Reverse Blocking Triode Thyristors

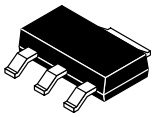
MCR08BT1 Series*

***Motorola preferred devices**

PNPN devices designed for line powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in surface mount package for use in automated manufacturing.

- Sensitive Gate Trigger Current
- Blocking Voltage to 600 Volts
- Glass Passivated Surface for Reliability and Uniformity
- Surface Mount Package
- Devices Supplied on 1 K Reel

SCR
0.8 AMPERE RMS
200 thru 600 Volts



CASE 318E-04
(SOT-223)
STYLE 10

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage(1) (1/2 Sine Wave, R_{GK} = 1000 Ω, T_J = 25 to 110°C) MCR08BT1 MCR08DT1 MCR08MT1	V_{DRM}, V_{RRM}	 200 400 600	Volts
On-State Current RMS (T_C = 80°C)	$I_{T(RMS)}$	0.8	Amps
Peak Non-repetitive Surge Current (One Full Cycle, 60 Hz, T_C = 25°C)	I_{TSM}	10	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.4	A^2s
Peak Gate Power, Forward, T_A = 25°C	P_{GM}	0.1	Watts
Average Gate Power (T_C = 80°C, t = 8.3 ms)	$P_{G(AV)}$	0.01	Watts
Operating Junction Temperature Range	T_J	–40 to +110	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C
Maximum Device Temperature for Soldering Purposes (for 10 Seconds Maximum)	T_L	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient PCB Mounted per Figure 1	$R_{\theta JA}$	156	°C/W
Thermal Resistance, Junction to Tab Measured on Anode Tab Adjacent to Epoxy	$R_{\theta JT}$	25	°C/W

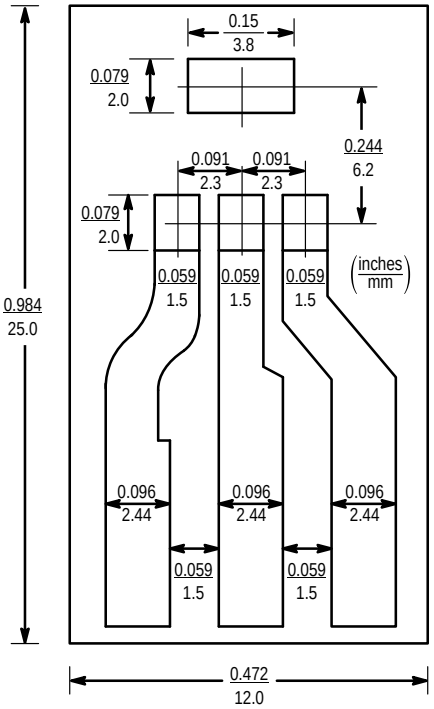
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant source such that the voltage ratings of the devices are exceeded.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1 KΩ)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Repetitive Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}, R_{GK} = 1000 Ω)	T_J = 25°C T_J = 110°C	I_{DRM}, I_{RRM}	— —	— —	10 200	μA μA
Maximum On-State Voltage (Either Direction)* (I_T = 1.0 A Peak, T_A = 25°C)		V_{TM}	—	—	1.7	Volts
Gate Trigger Current (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ω)		I_{GT}	—	—	200	μA
Holding Current (V_D = 7.0 Vdc, Initializing Current = 20 mA, R_{GK} = 1000 Ω)		I_H	—	—	5.0	mA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ω)		V_{GT}	—	—	0.8	Volts
Critical Rate-of-Rise of Off State Voltage (V_{pk} = Rated V_{DRM}, T_C = 110°C, R_{GK} = 1000 Ω, Exponential Method)		dv/dt	10	—	—	V/μs

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



BOARD MOUNTED VERTICALLY IN CINCH 8840 EDGE CONNECTOR.
BOARD THICKNESS = 65 MIL., FOIL THICKNESS = 2.5 MIL.
MATERIAL: G10 FIBERGLASS BASE EPOXY

Figure 1. PCB for Thermal Impedance and Power Testing of SOT-223

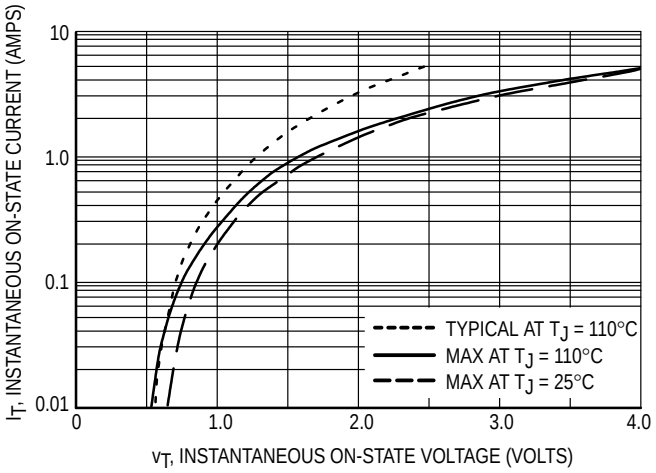


Figure 2. On-State Characteristics

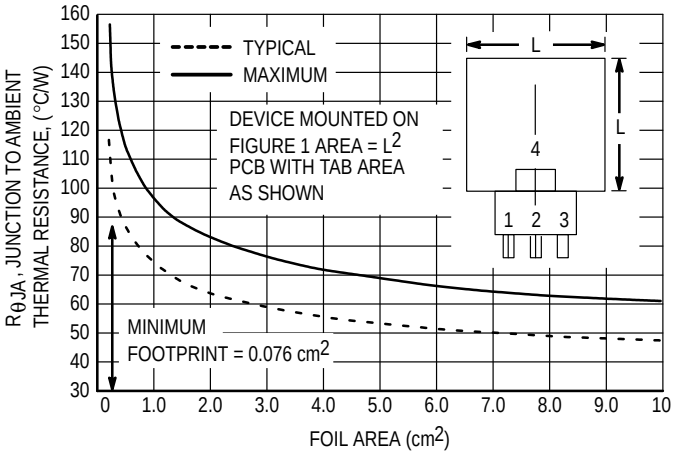


Figure 3. Junction to Ambient Thermal Resistance versus Copper Tab Area

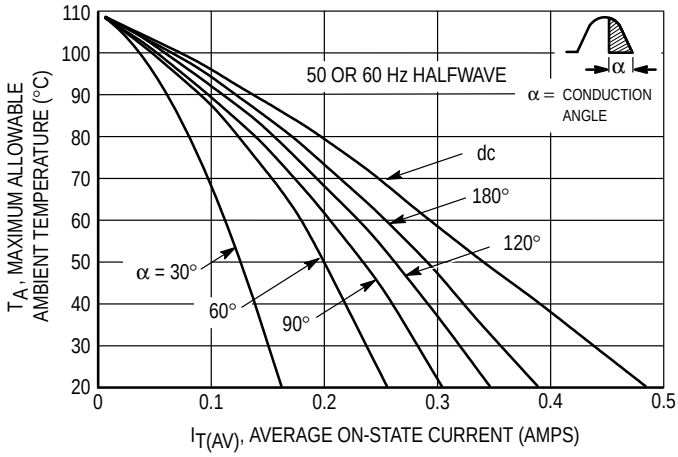


Figure 4. Current Derating, Minimum Pad Size Reference: Ambient Temperature

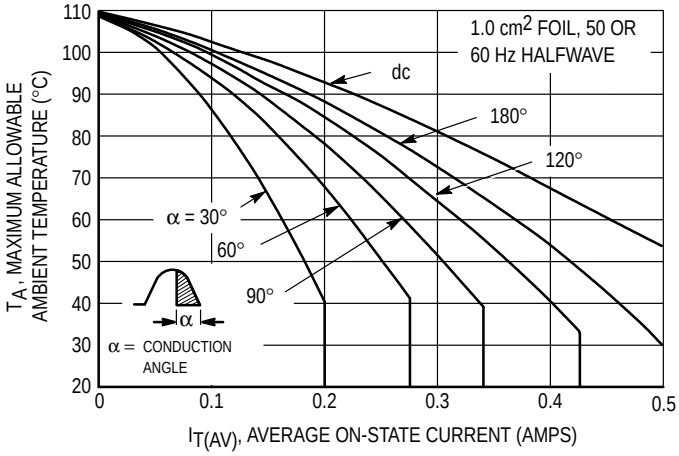


Figure 5. Current Derating, 1.0 cm Square Pad Reference: Ambient Temperature

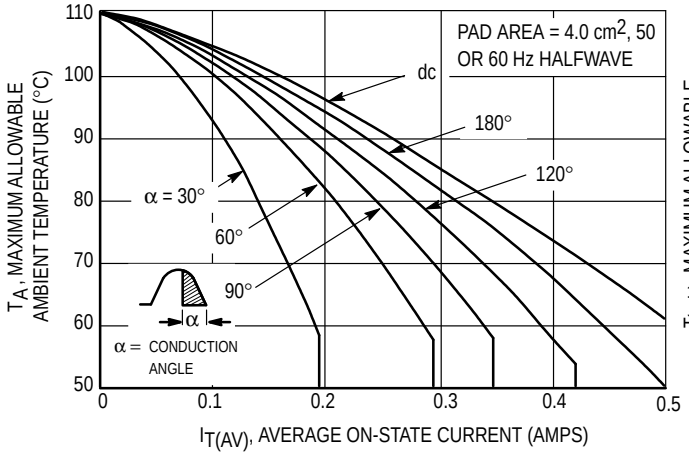


Figure 6. Current Derating, 2.0 cm Square Pad Reference: Ambient Temperature

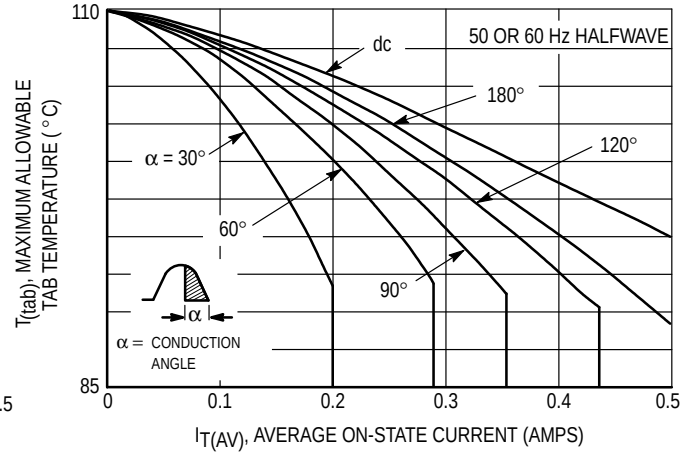


Figure 7. Current Derating Reference: Anode Tab

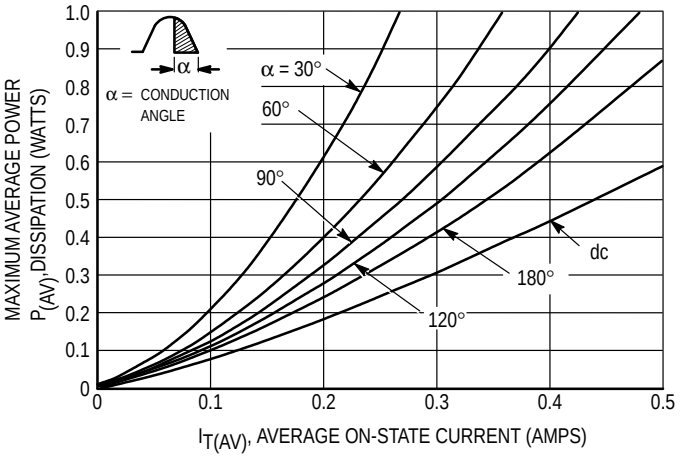


Figure 8. Power Dissipation

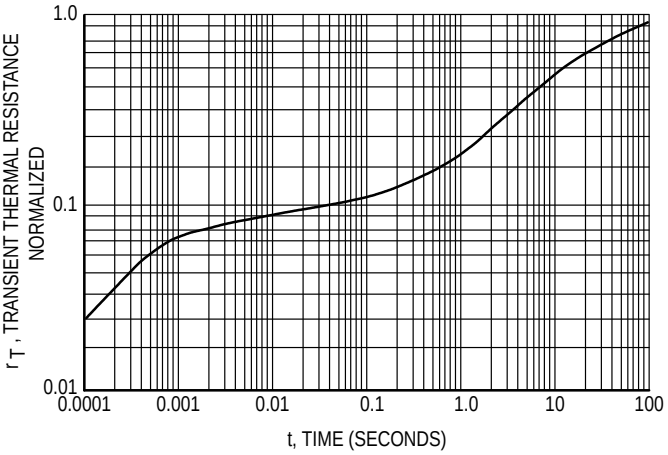


Figure 9. Thermal Response Device Mounted on Figure 1 Printed Circuit Board

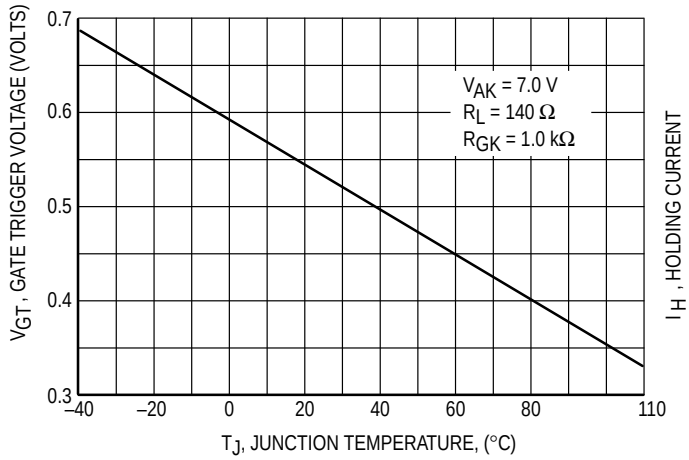


Figure 10. Typical Gate Trigger Voltage versus Junction Temperature

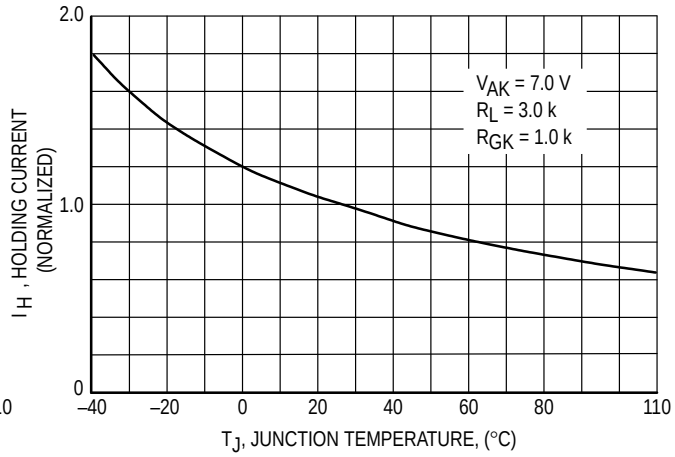


Figure 11. Typical Normalized Holding Current versus Junction Temperature

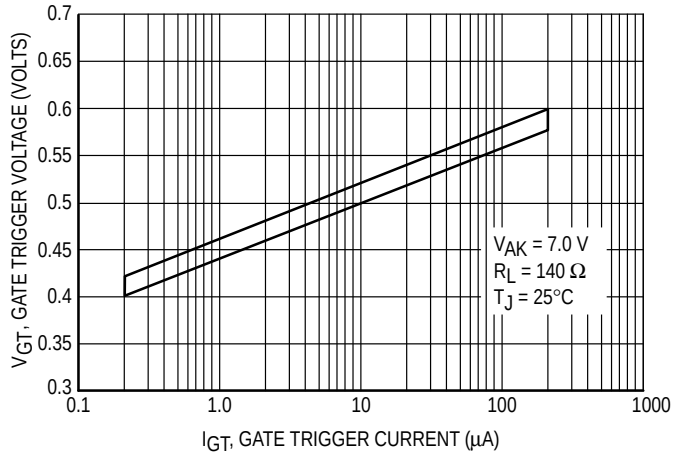


Figure 12. Typical Range of V_{GT} versus Measured I_{GT}

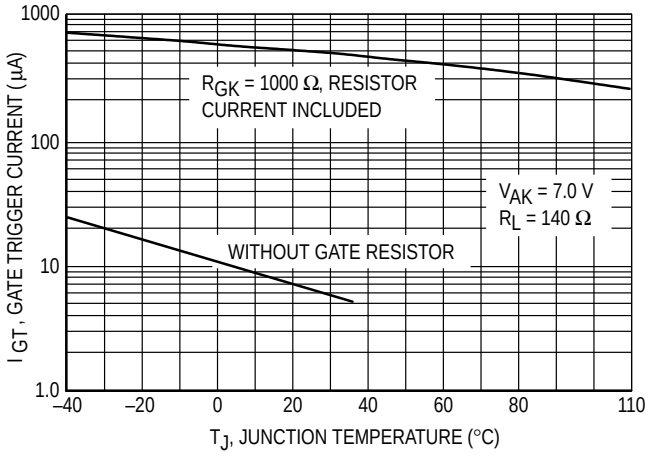


Figure 13. Typical Gate Trigger Current versus Junction Temperature

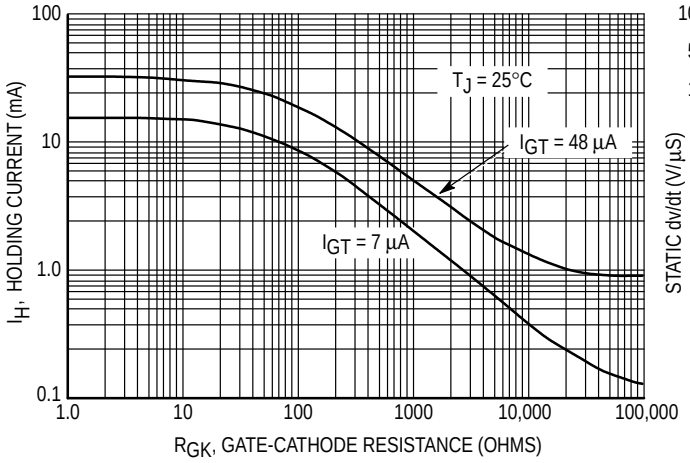


Figure 14. Holding Current Range versus Gate-Cathode Resistance

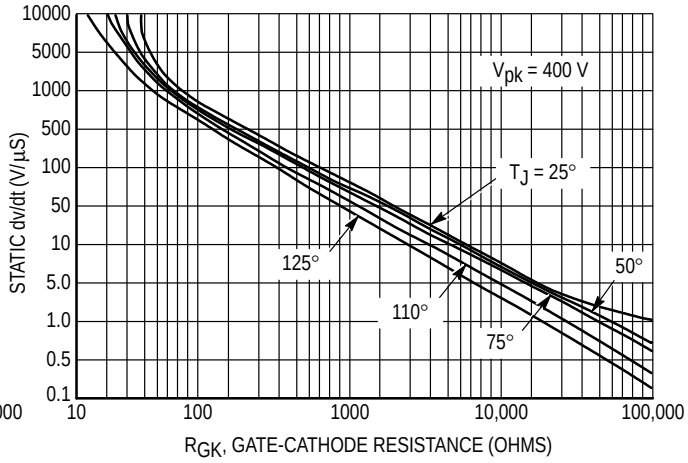


Figure 15. Exponential Static dv/dt versus Junction Temperature and Gate-Cathode Termination Resistance

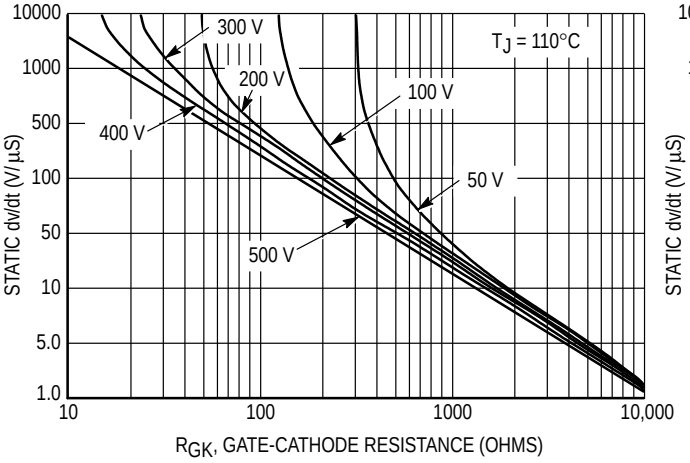


Figure 16. Exponential Static dv/dt versus Peak Voltage and Gate-Cathode Termination Resistance

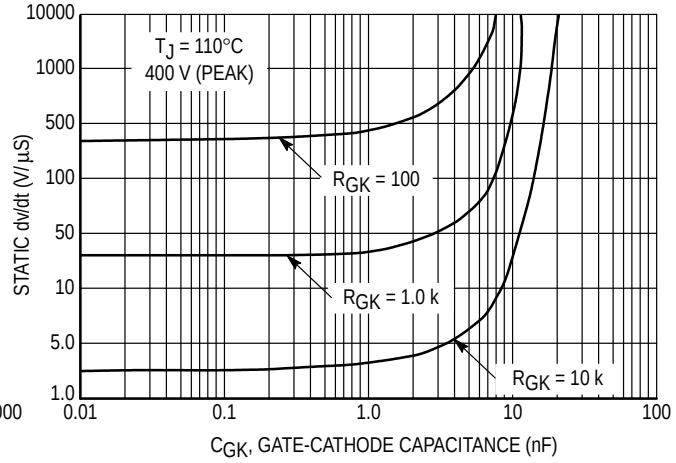


Figure 17. Exponential Static dv/dt versus Gate-Cathode Capacitance and Resistance

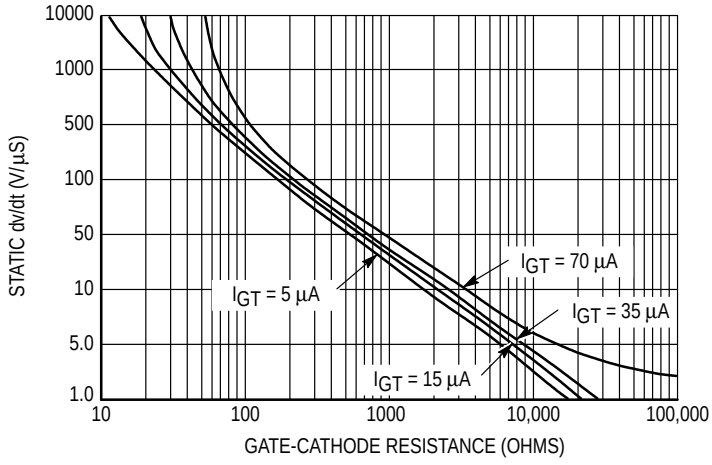
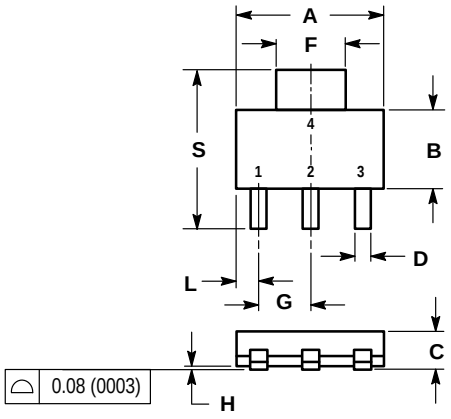
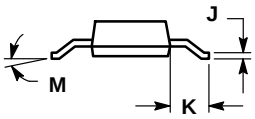


Figure 18. Exponential Static dv/dt versus Gate-Cathode Termination Resistance and Product Trigger Current Sensitivity

PACKAGE DIMENSIONS



STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE



NOTES:
2 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

CASE 318E-04
(SOT–223)

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