

S-SERIES 2009

INVICTA (Intel-Discrete)

MV Build (A03) - Final

2009.03.18

Datasharedirectory

DATE	CHANGE NO.	REV

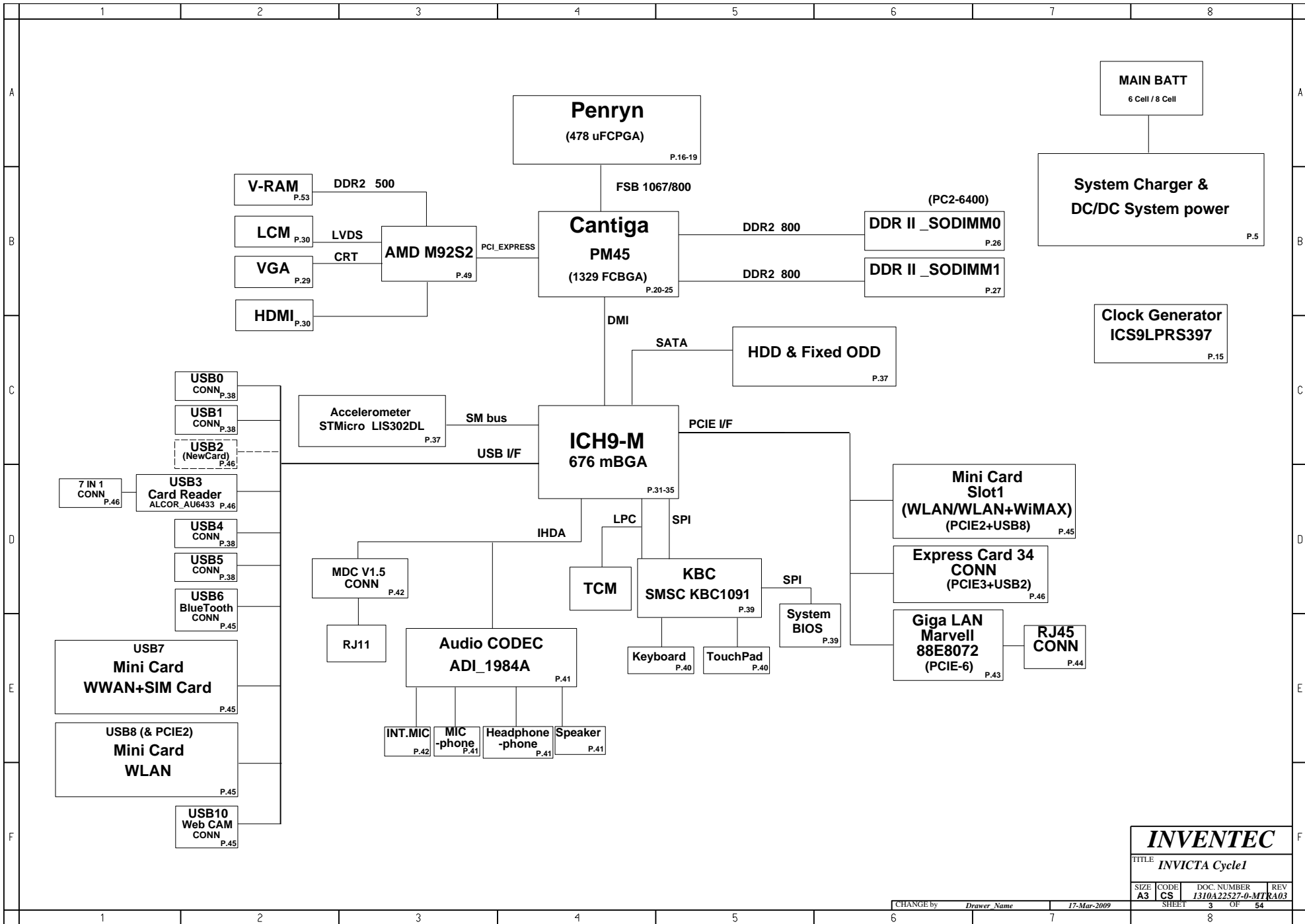
DRAWER	EE	DATE	POWER	DATE	INVENTEC			
DESIGN								
CHECK								
RESPONSIBLE								
TITLE					<i>INVICTA Cycle1</i>			
SIZE =	3	VER :						
FILE NAME :	XXXX-XXXXXX-XX				SIZE	CODE	DOC NUMBER	REV
P/N	XXXXXXXXXXXX				A3	CS	J310A22527-0-MTR	A03
					SHEET	1	OF	54

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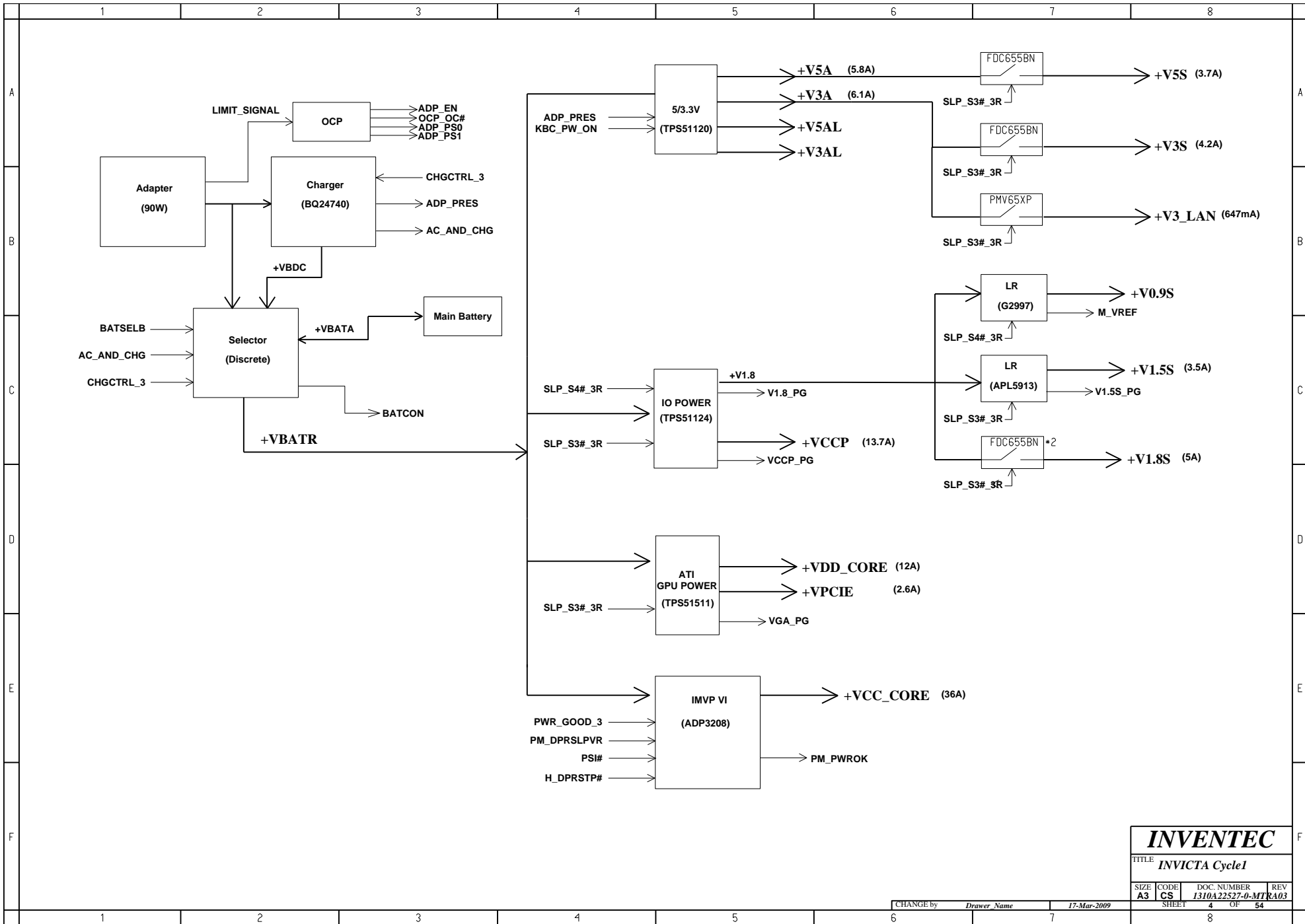
Page	Page	Page
5- DC & Battery Charger & OCP.	15- Clock Generator.	36- Power, LID, APP SW/B.
6- Select & Battery CONN.	16- CPU Penryn-1.	37- HDD & ODD,Accelerometer,15" ODD EXT/B.
7- System Power (+V3A/+V5A).	17- CPU Penryn-2.	38- USB CONN.
8- System Power (+V1.8/+VCCP) .	18- CPU Penryn-3.	39- KBC, BIOS ROM, Debug Port.
9- Graphic Power (+VDD_CORE & +VPCIE).	19- XDP & Thermal & Fan.	40- Internal Keyboard & TouchPad CONN.
10- System Power (+V1.5S) .	20- N/B Cantiga-1.	41- Audio CODEC & Earphone & Speaker.
11- CPU Power (+VCC_CORE).	21- N/B Cantiga-2.	42- Audio MIC & MDC CONN.
12- DDR Termination Voltage(+V0.9S).	22- N/B Cantiga-3.	43- Giga LAN controller.
13- Power (Sleep: +V5S/+V3S/+V1.8S).	23- N/B Cantiga-4.	44- Magnetic & RJ45 CONN.
14- Power (Sequence).	24- N/B Cantiga-5.	45- Mini Card(WLAN/WWAN), BT.
	25- N/B Cantiga-6.	46- New Card & 4 in 1 Card (SD/MMC/MS/XD).
	26- DDR2-DIMM0.	47- LEDs, TCM CONN.
	27- DDR2-DIMM1.	48- Screws, Crack testing circuit.
	28- DDR2-Termination.	49- AMD M92S2-1.
	29- VGA CONN.	50- AMD M92S2-2.
	30- LCD,WebCam,HDMI CONN.	51- AMD M92S2-3.
	31- S/B ICH9-1.	52- AMD M92S2-4.
	32- S/B ICH9-2.	53- Video RAM-1 (DDR2).
	33- S/B ICH9-3.	54- Video RAM-2 (DDR2).
	34- S/B ICH9-4.	
	35- S/B ICH9-5.	

INVENTEC

TITLE INVICTA Cycle1			
Contents			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		DRAWER Name	17-Mar-2009
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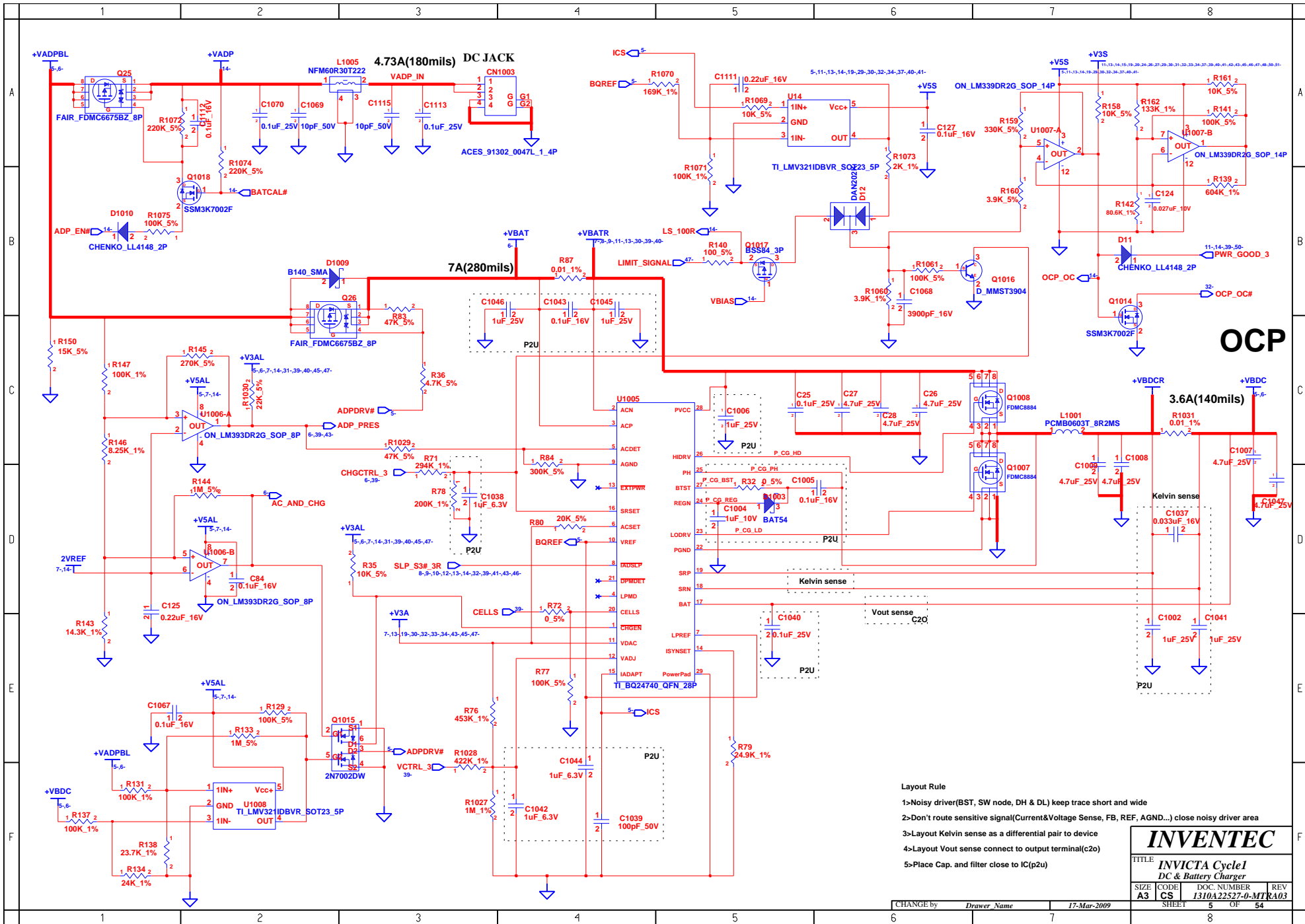
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SIZE	CODE	DOC. NUMBER	REV
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CHANGE by		Drawer Name	17-Mar-2009
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INVENTEC

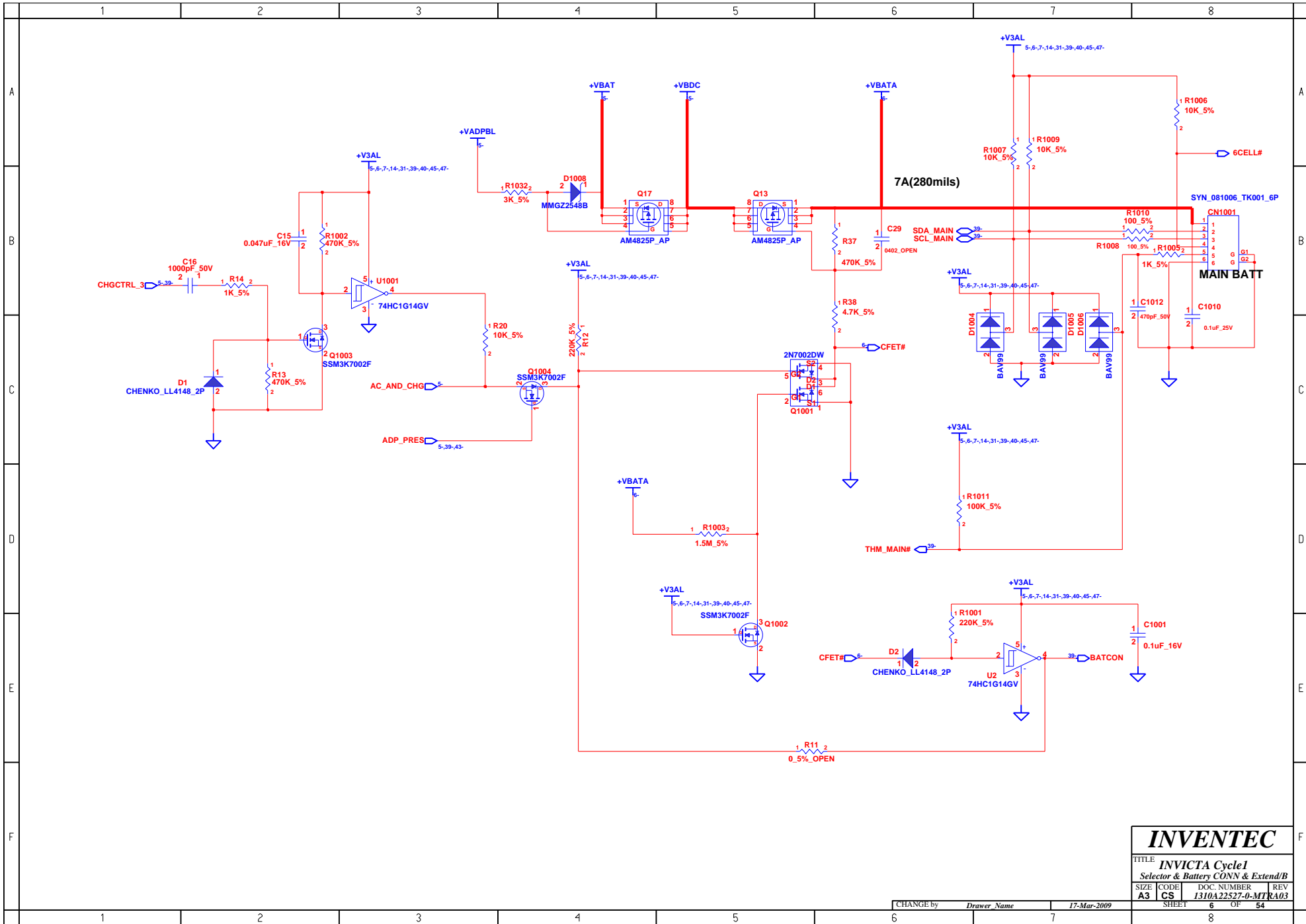
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SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03

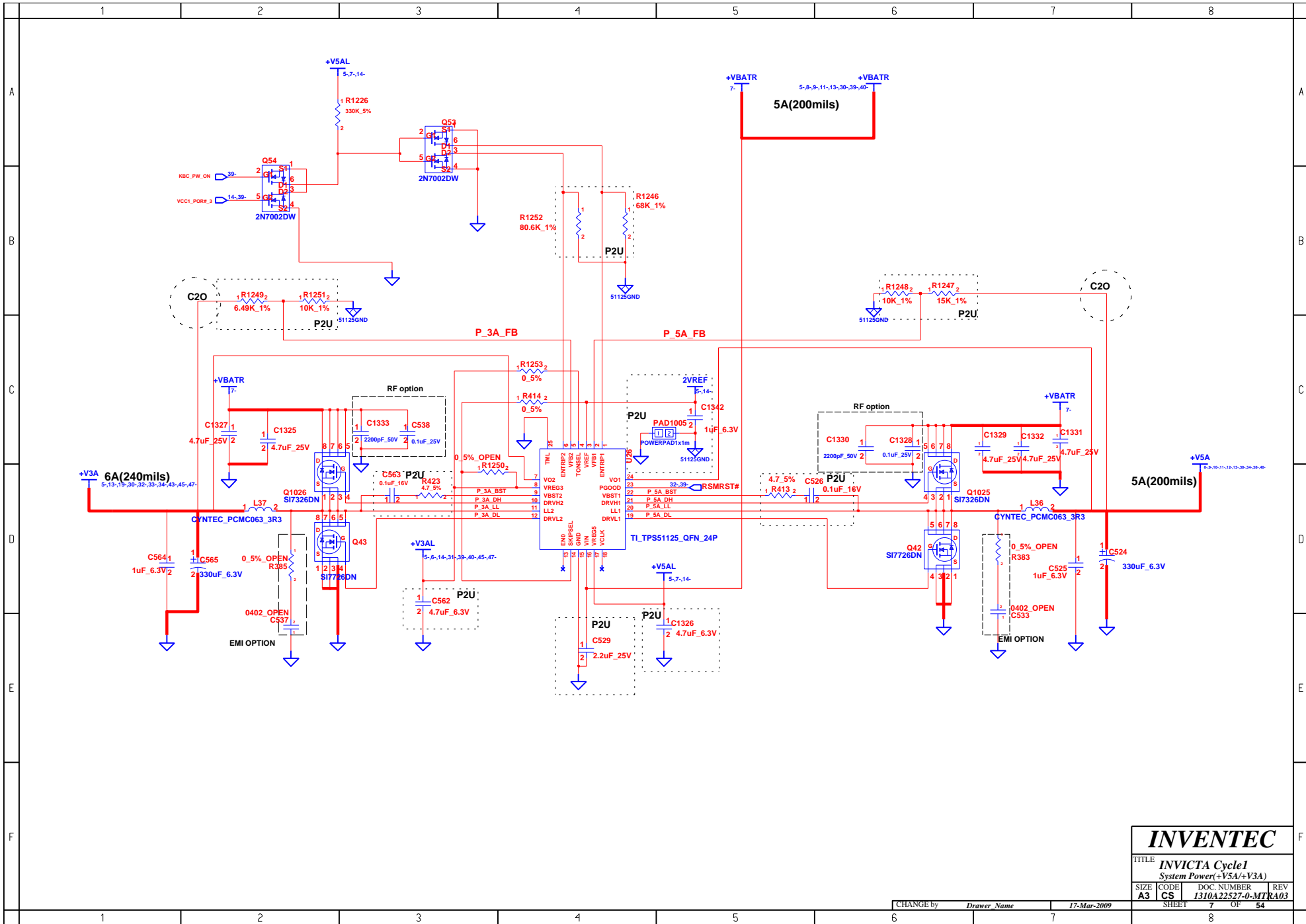


- Layout Rule**
- 1>Noisy driver(BST, SW node, DH & DL) keep trace short and wide
 - 2>Don't route sensitive signal(Current&Voltage Sense, FB, REF, AGND...) close noisy driver area
 - 3>Layout Kelvin sense as a differential pair to device
 - 4>Layout Vout sense connect to output terminal(c2o)
 - 5>Place Cap. and filter close to IC(p2u)

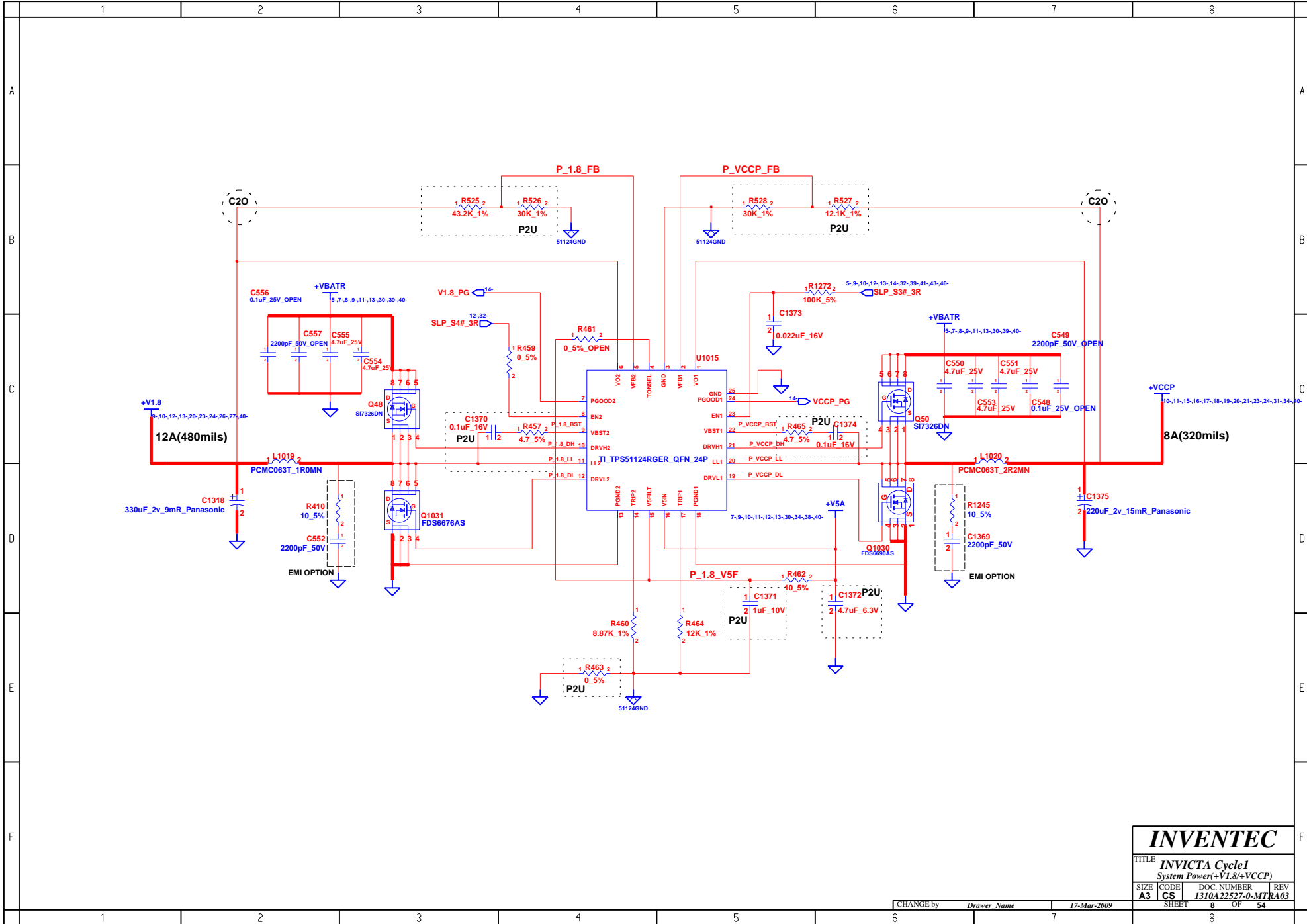
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TITLE: INVICTA Cycle1 DC & Battery Charger			
SIZE	CODE	DOC NUMBER	REV
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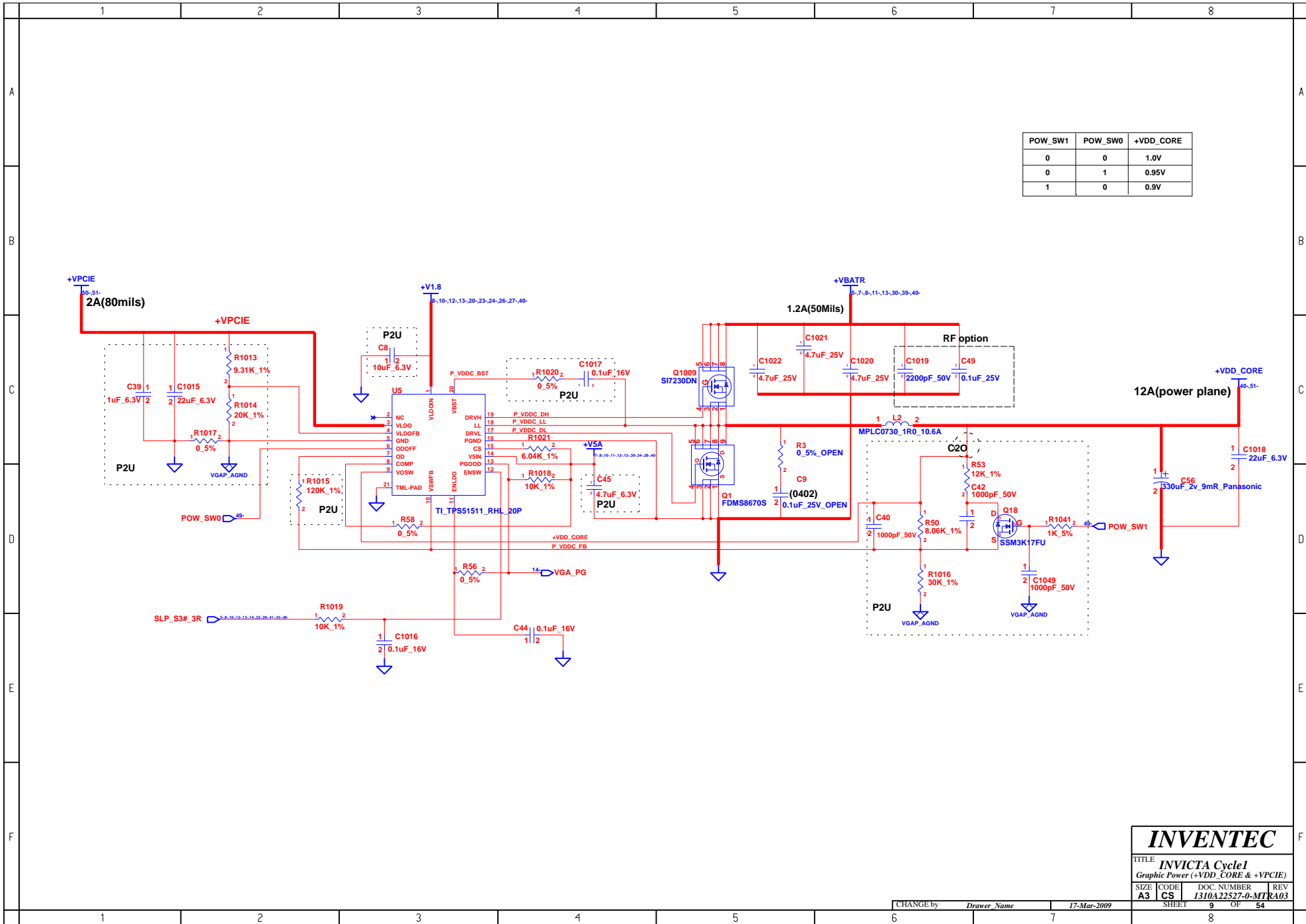
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TITLE <i>INVICTA Cycle1</i>			
Selector & Battery CONN & Extend/B			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MT	A03
CHANGE by		Drawer Name	17-Mar-2009
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INVENTEC			
TITLE: INVICTA Cycle 1			
System Power(+V5A/+V3A)			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MT	R03



INVENTEC			
TITLE: INVICTA Cycle 1			
System Power(+V1.8/+VCCP)			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MT	R403
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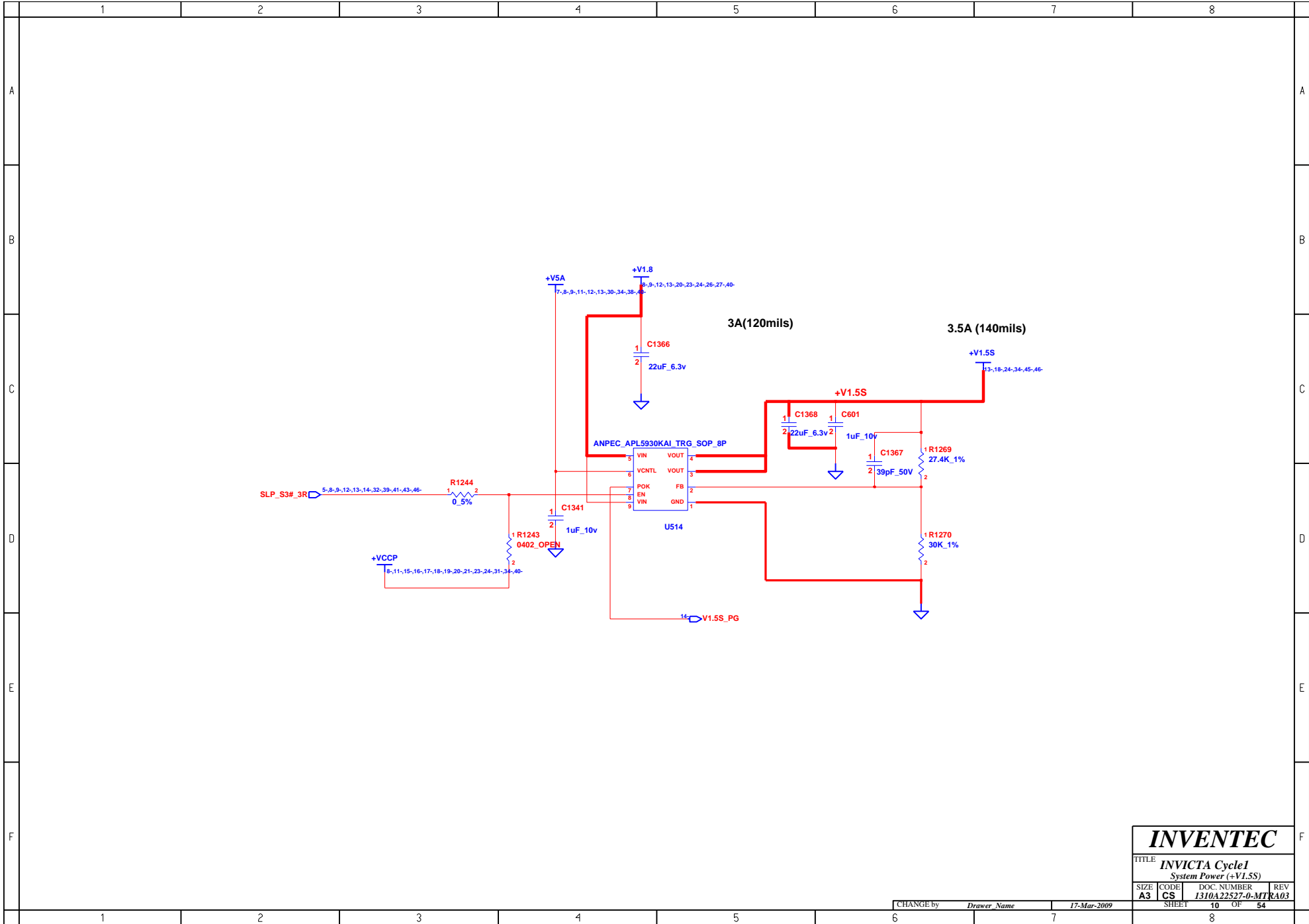


INVENTEC

TITLE: **INVICTA Cycle1**
 Graphic Power (+VDD_CORE & +VPCIE)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A22527-0-MTR	A03

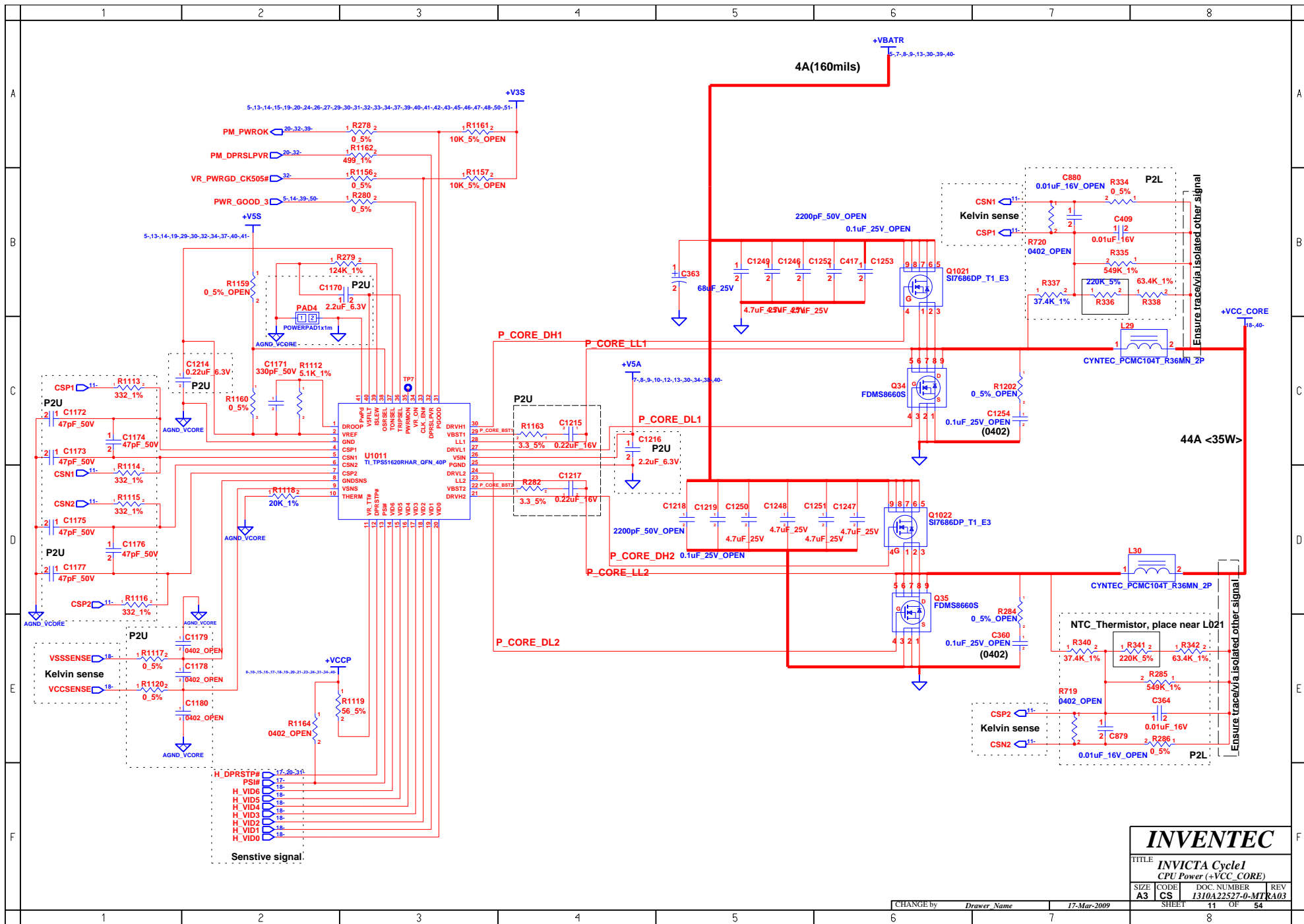
CHANGE by: *Drawer Name* 17-Mar-2009 SHEET 9 OF 54



INVENTEC

TITLE *INVICTA Cycle 1*
System Power (+V1.5S)

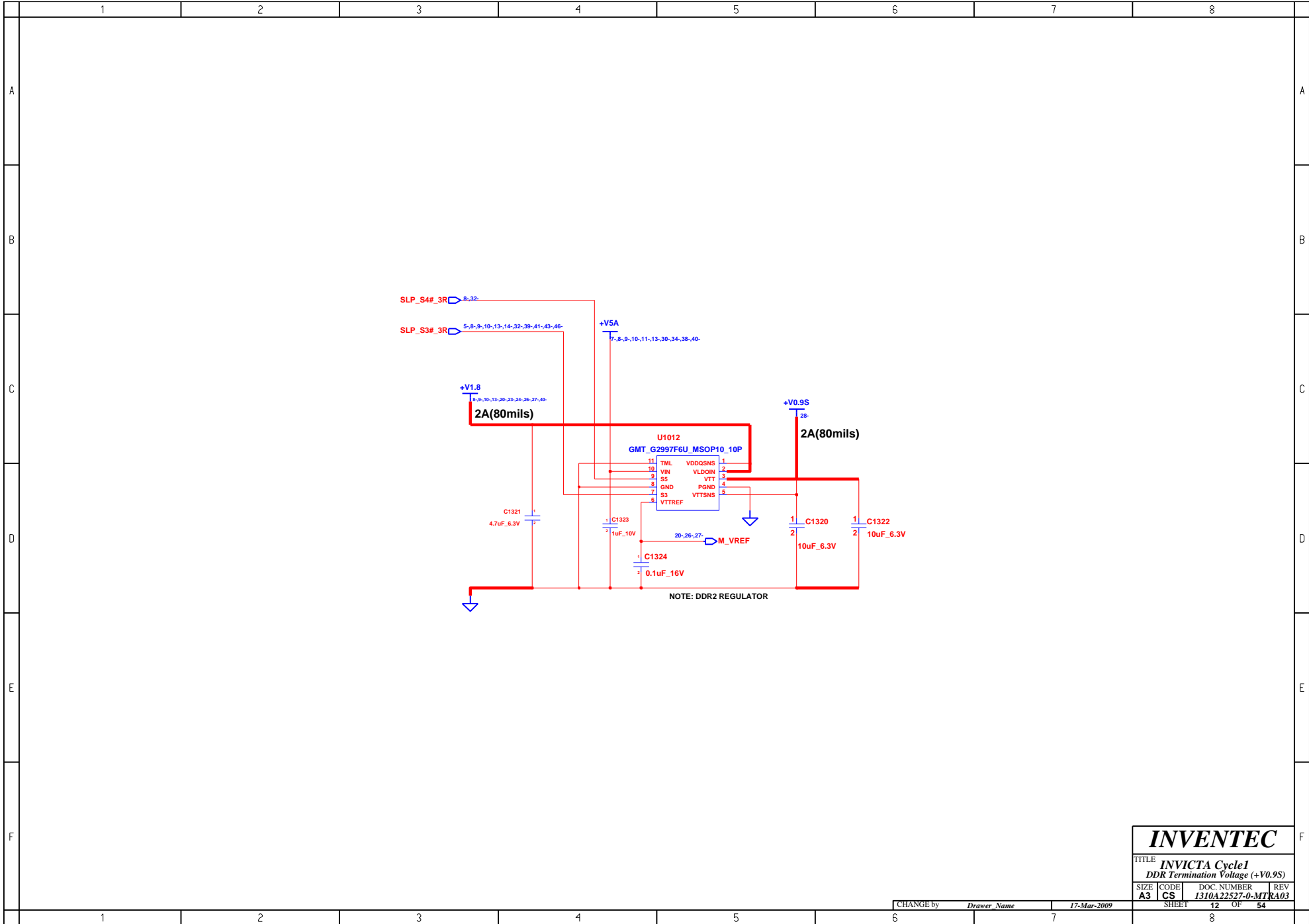
SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MTR	REV A03
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INVENTEC

TITLE			
INVICTA Cycle1			
CPU Power (+VCC_CORE)			
SIZE	CODE	DOC NUMBER	REV
A3	CS	I310A22527-0-MTR	A03

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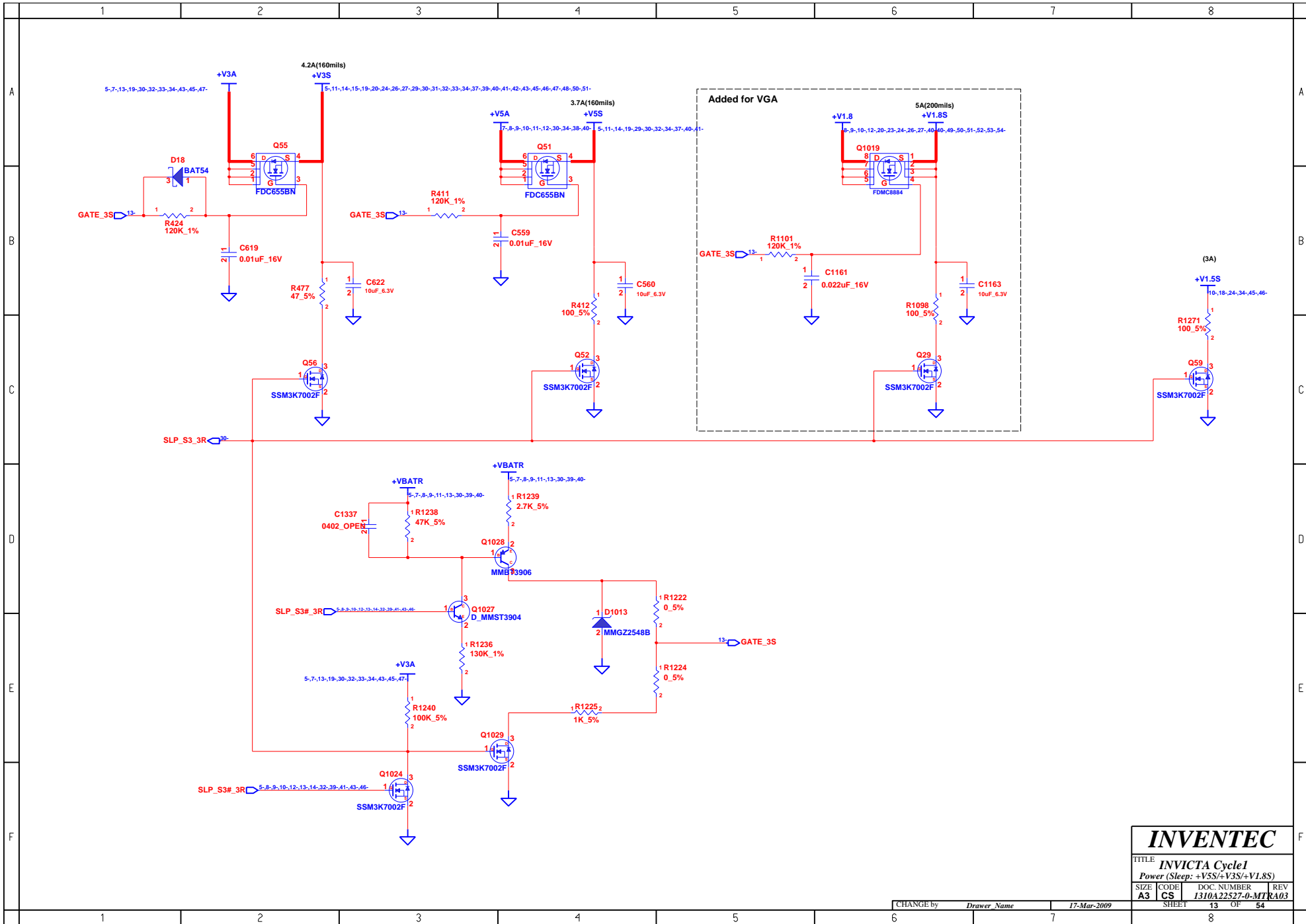
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TITLE **INVICTA Cycle1**
DDR Termination Voltage (+V0.9S)

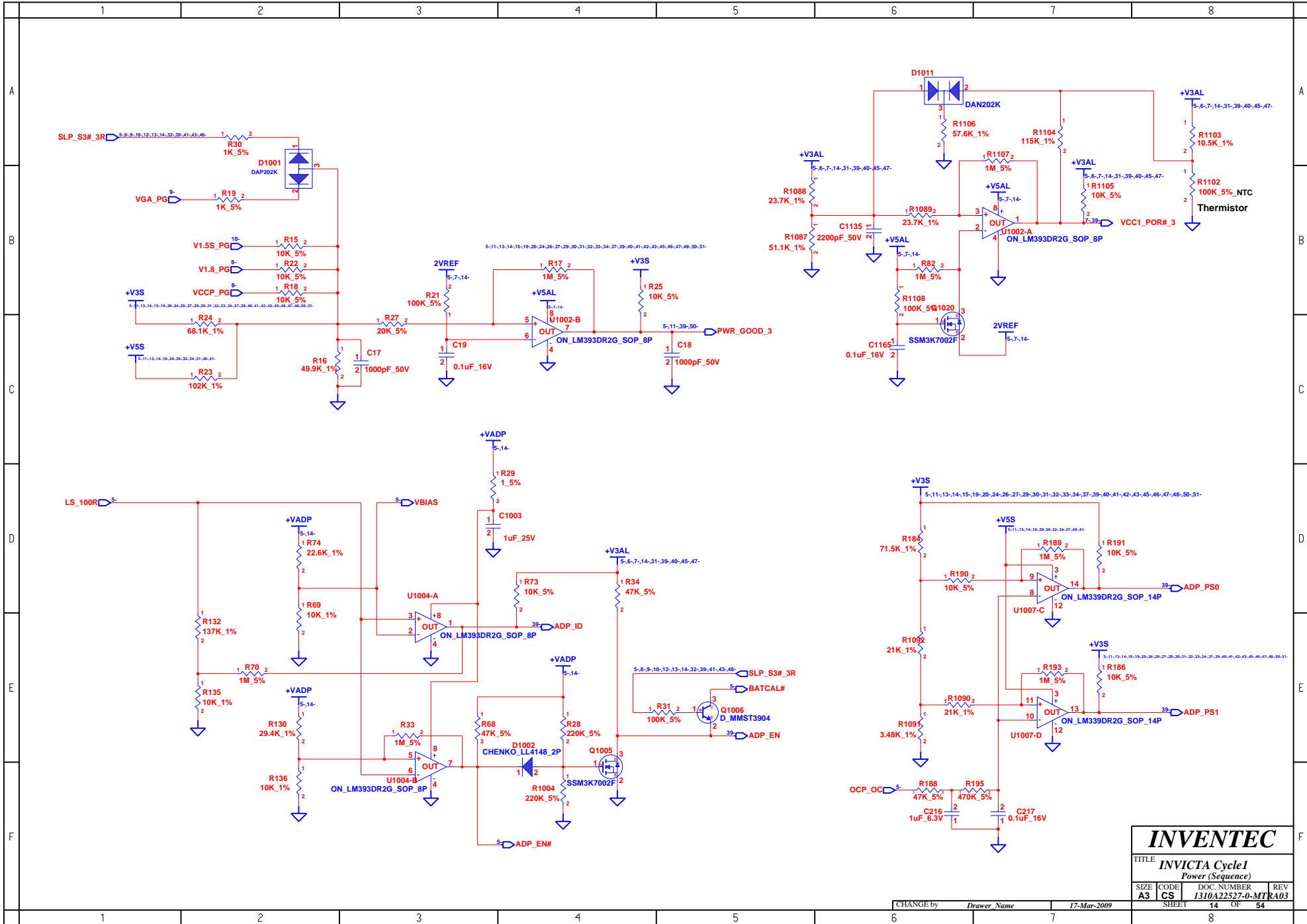
SIZE **A3** CODE **CS** DOC. NUMBER **1310A22527-0-MT** REV **RA03**

CHANGE by *Drawer Name* 17-Mar-2009

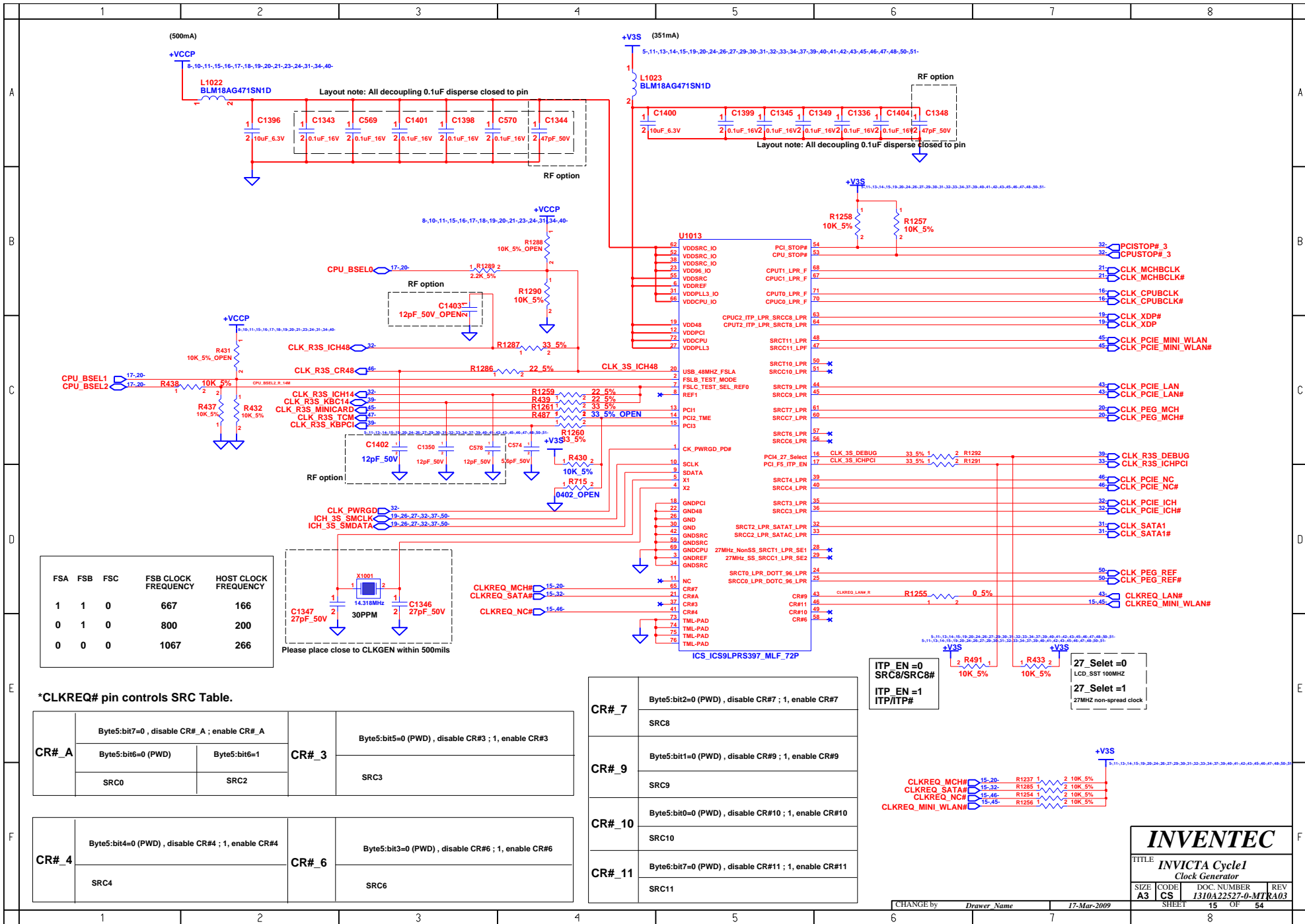
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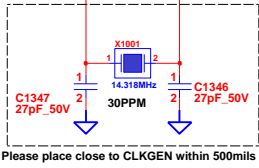
INVENTEC			
TITLE <i>INVICTA Cycle 1</i>			
Power (Sleep: +VSS/+V3S/+V1.8S)			
SIZE	CODE	DOC NUMBER	REV
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INVENTEC			
TITLE INVICTA Cycle1 Power (Sequence)			
SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MTR	REV A03
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FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266



*CLKREQ# pin controls SRC Table.

CR#_A	Byte5:bit7=0 (PWD), disable CR#_A ; enable CR#_A	Byte5:bit6=0 (PWD)	Byte5:bit6=1	CR#_3	Byte5:bit5=0 (PWD), disable CR#3 ; 1, enable CR#3
	SRC0				SRC3

CR#_4	Byte5:bit4=0 (PWD), disable CR#4 ; 1, enable CR#4	CR#_6	Byte5:bit3=0 (PWD), disable CR#6 ; 1, enable CR#6
	SRC4		SRC6

CR#_7	Byte5:bit2=0 (PWD), disable CR#7 ; 1, enable CR#7
	SRC8
CR#_9	Byte5:bit1=0 (PWD), disable CR#9 ; 1, enable CR#9
	SRC9
CR#_10	Byte5:bit0=0 (PWD), disable CR#10 ; 1, enable CR#10
	SRC10
CR#_11	Byte6:bit7=0 (PWD), disable CR#11 ; 1, enable CR#11
	SRC11

ITP_EN=0
SRC8/SRC8#
ITP_EN=1
ITP/ITP#

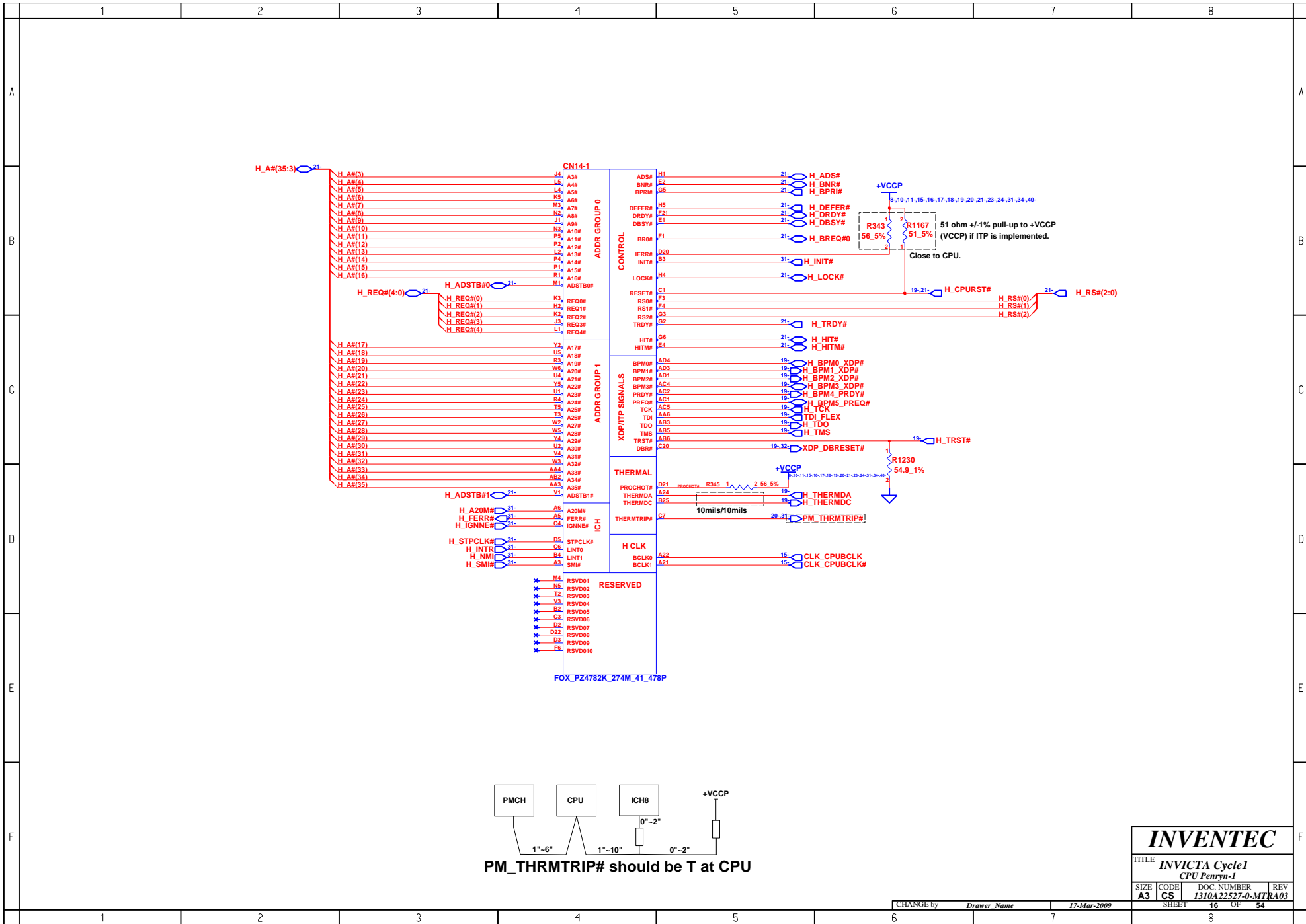
27_Selet=0
LCD_SST 100MHz
27_Selet=1
27MHz non-spread clock

CLKREQ_MCH# 15-20 R1237 2 10K 5%
CLKREQ_SATA# 15-32 R1255 2 10K 5%
CLKREQ_NC# 15-46 R1254 2 10K 5%
CLKREQ_MINI_WLAN# 15-45 R1256 2 10K 5%

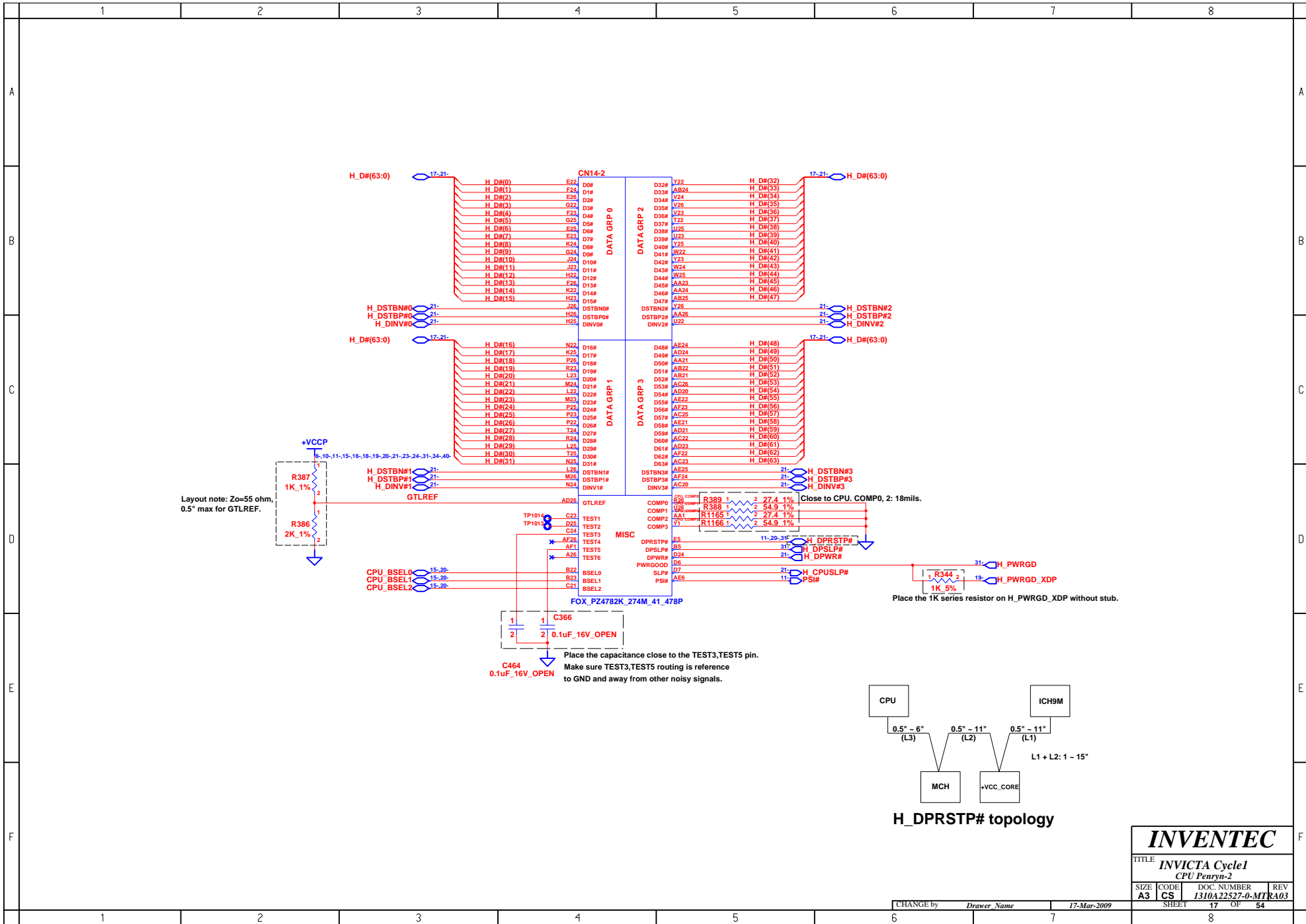
INVENTEC

TITLE
INVICTA Cycle1
Clock Generator

SIZE A3	CODE CS	DOC NUMBER I310A22527-0-MTR	REV A03
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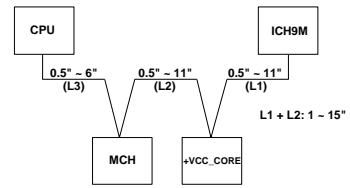
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TITLE <i>INVICTA Cycle1</i>			
CPU Penryn-1			
SIZE	CODE	DOC NUMBER	REV
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Layout note: Zo=55 ohm,
0.5" max for GTLREF.

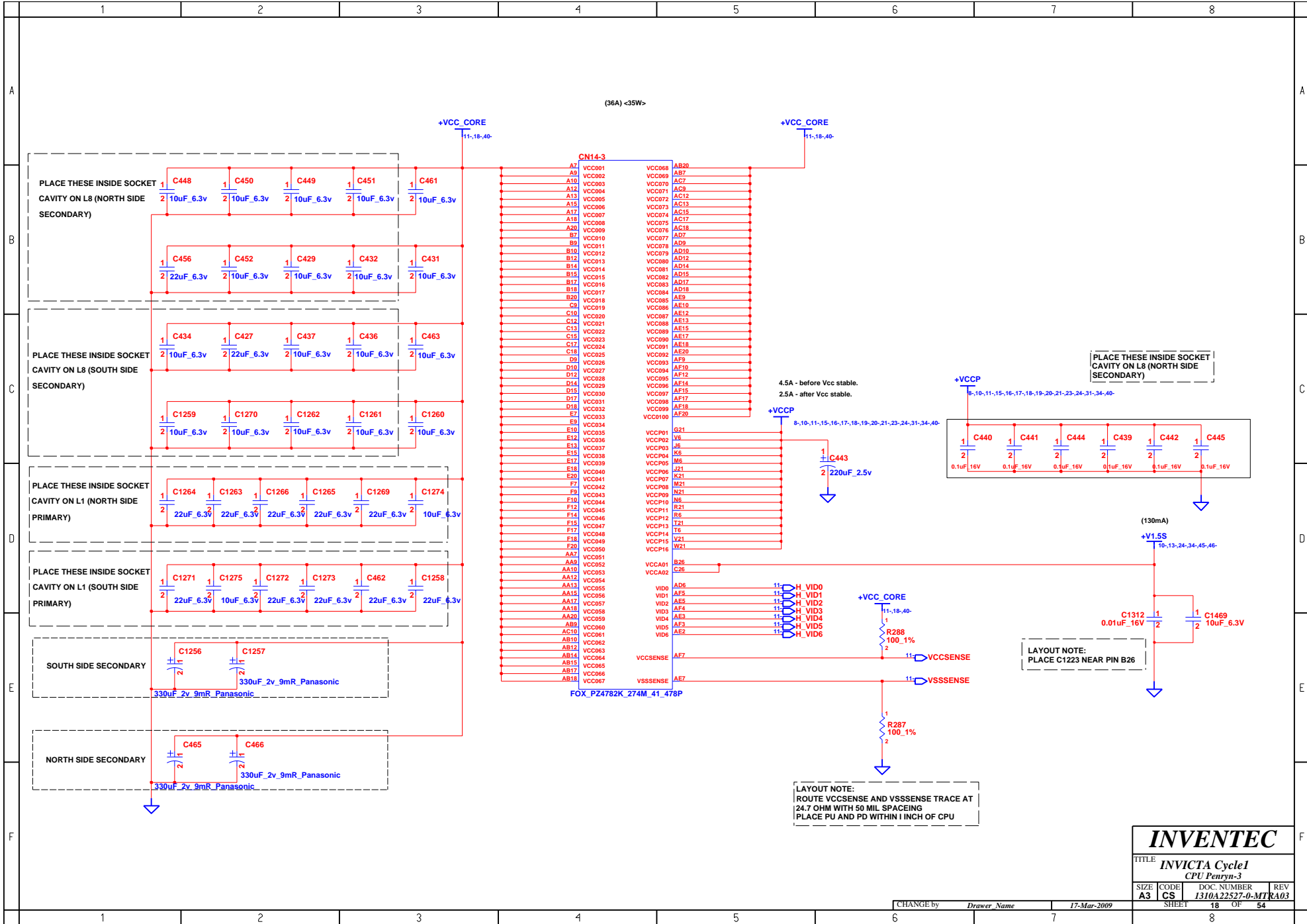
Place the capacitance close to the TEST3, TEST5 pin.
Make sure TEST3, TEST5 routing is reference
to GND and away from other noisy signals.

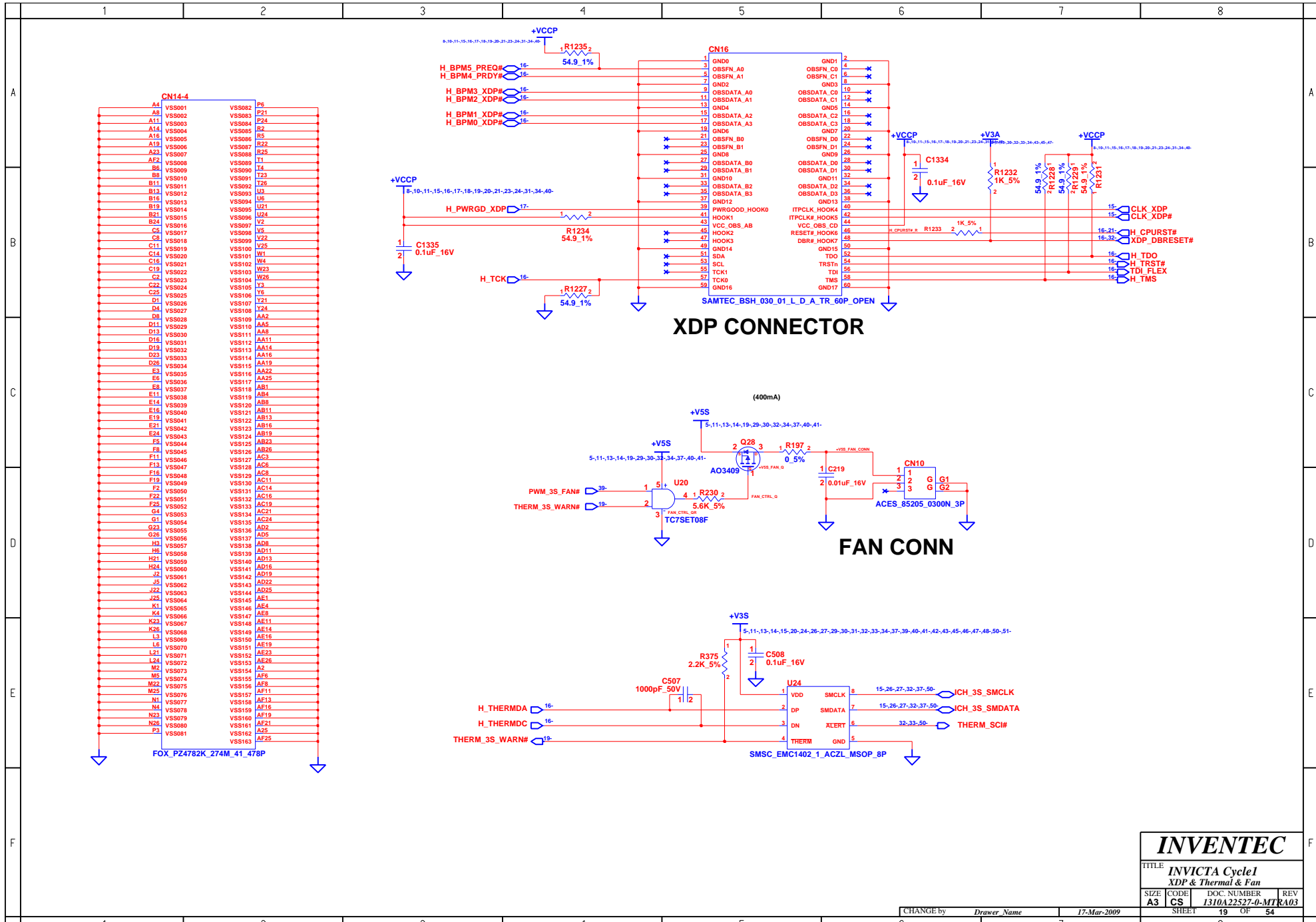
Close to CPU_COMP0, 2: 18mils.
Place the 1K series resistor on H_PWRGD_XDP without stub.



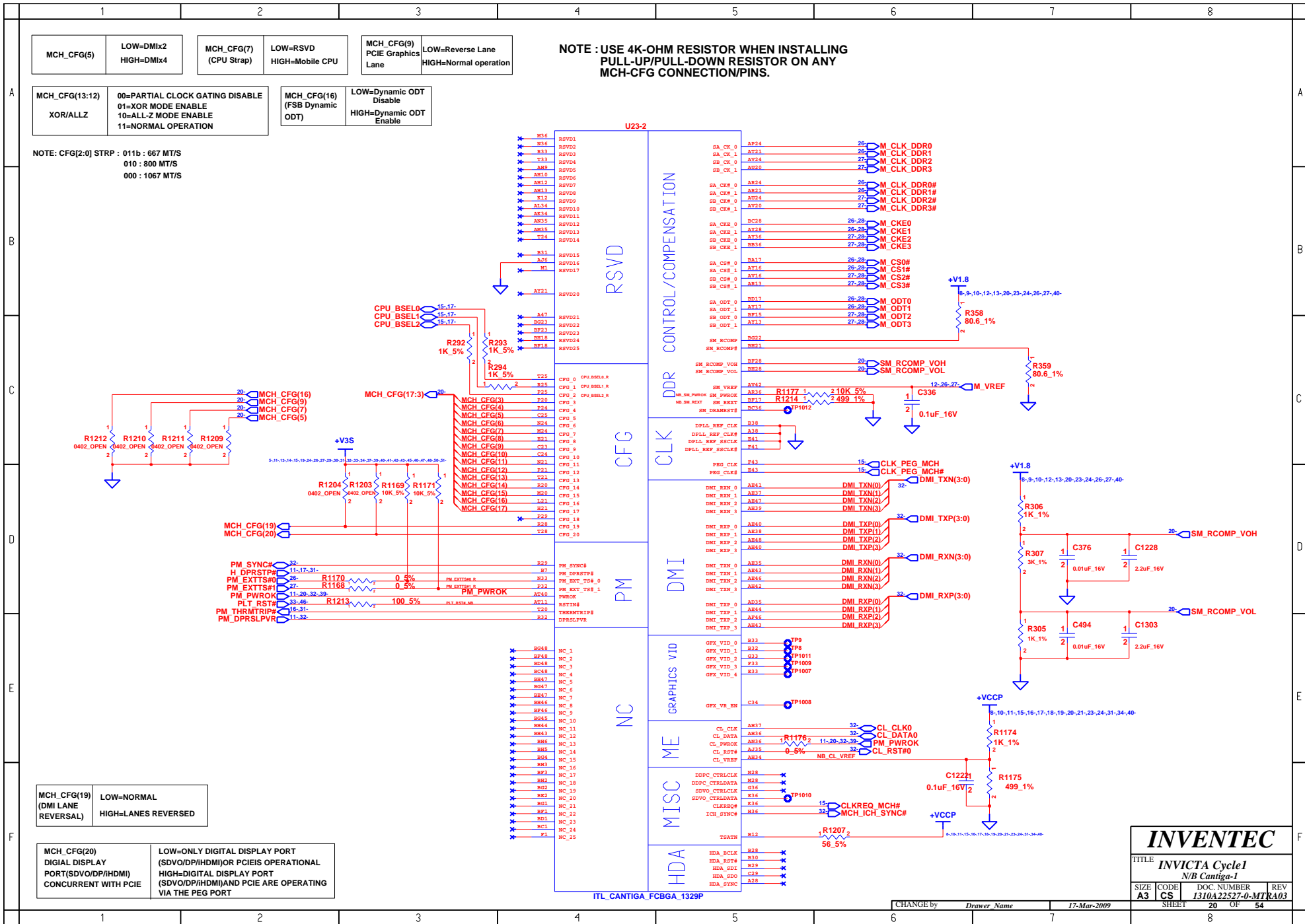
H_DPRSTP# topology

INVENTEC			
TITLE INVICTA Cycle1			
CPU Penryn-2			
SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MTR	REV A03
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INVENTEC			
TITLE INVICTA Cycle1 XDP & Thermal & Fan			
SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MTR	REV A03
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MCH_CFG(5)	LOW=DMiX2 HIGH=DMiX4	MCH_CFG(7) (CPU Strap)	LOW=RSVD HIGH=Mobile CPU	MCH_CFG(9) PCIE Graphics Lane	LOW=Reverse Lane HIGH=Normal operation
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MCH_CFG(13:12) XOR/ALLZ	00=PARTIAL CLOCK GATING DISABLE 01=XOR MODE ENABLE 10=ALL-Z MODE ENABLE 11=NORMAL OPERATION	MCH_CFG(16) (FSB Dynamic ODT)	LOW=Dynamic ODT HIGH=Dynamic ODT Enable
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NOTE: CFG[2:0] STRP : 011b : 667 MT/S
010 : 800 MT/S
000 : 1067 MT/S

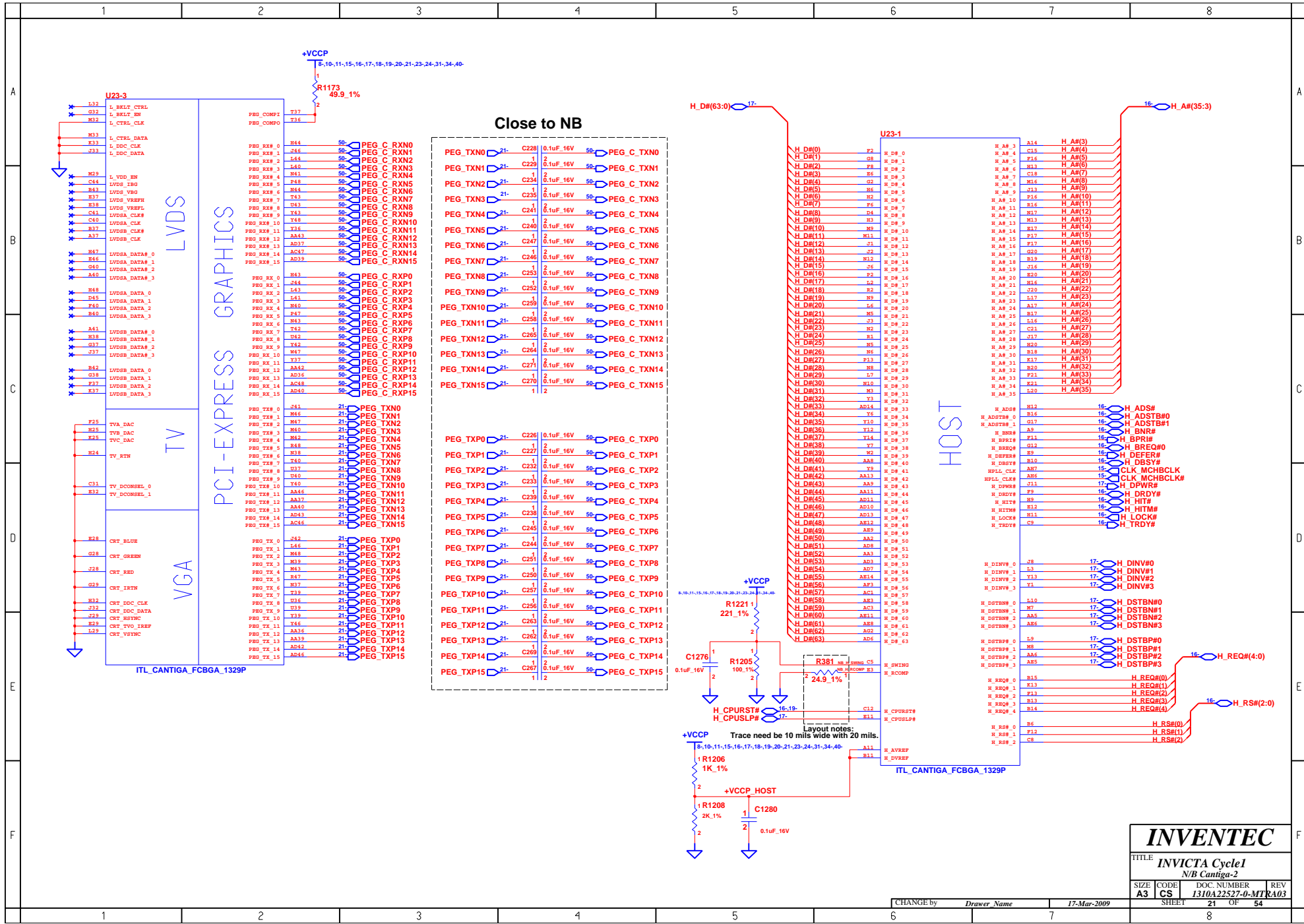
MCH_CFG(19) (DMI LANE REVERSAL)	LOW=NORMAL HIGH=LANES REVERSED
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MCH_CFG(20) DIGIAL DISPLAY PORT(SDVO/DP/HDMI)OR PCIEIS OPERATIONAL PORT(SDVO/DP/HDMI) CONCURRENT WITH PCIE	LOW=ONLY DIGITAL DISPLAY PORT (SDVO/DP/HDMI)OR PCIEIS OPERATIONAL HIGH=DIGITAL DISPLAY PORT (SDVO/DP/HDMI)AND PCIE ARE OPERATING VIA THE PEG PORT
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INVENTEC

TITLE: INVICTA Cycle1
N/B Cantiga-1

SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MTR	REV A03
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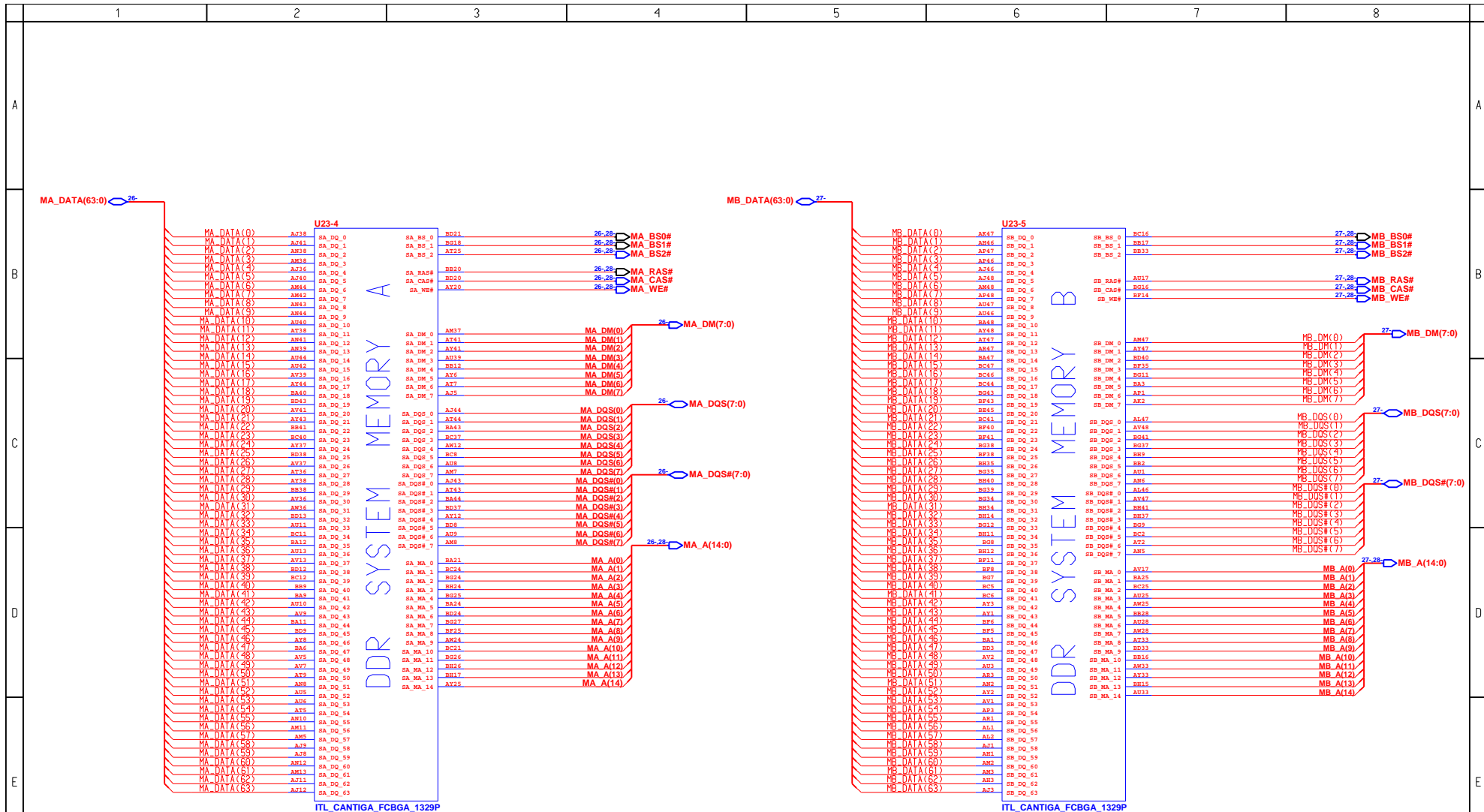
INVENTEC

TITLE: **INVICTA Cycle1**
N/B Cantiga-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03

CHANGE by: *Drawer Name* 17-Mar-2009

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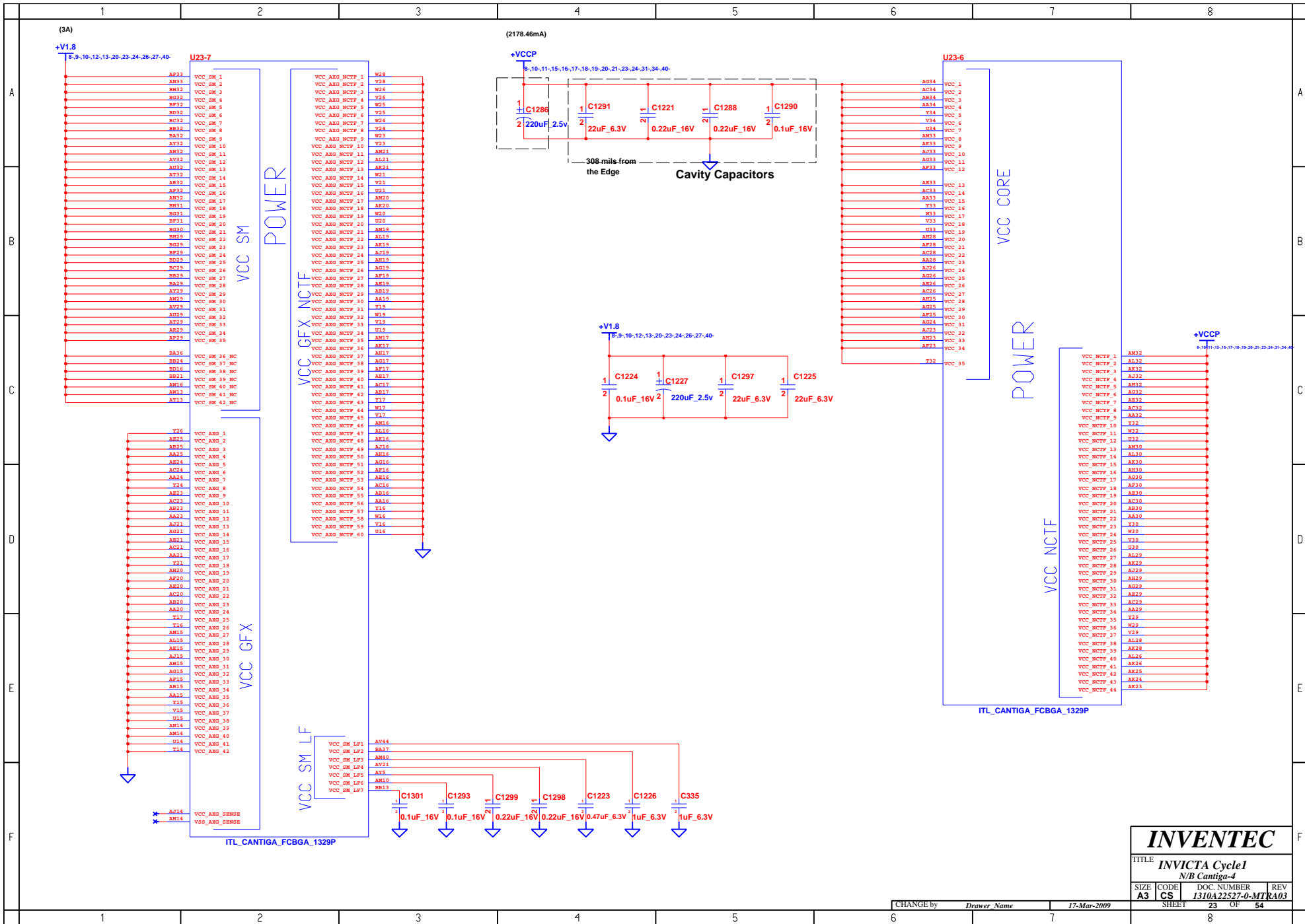


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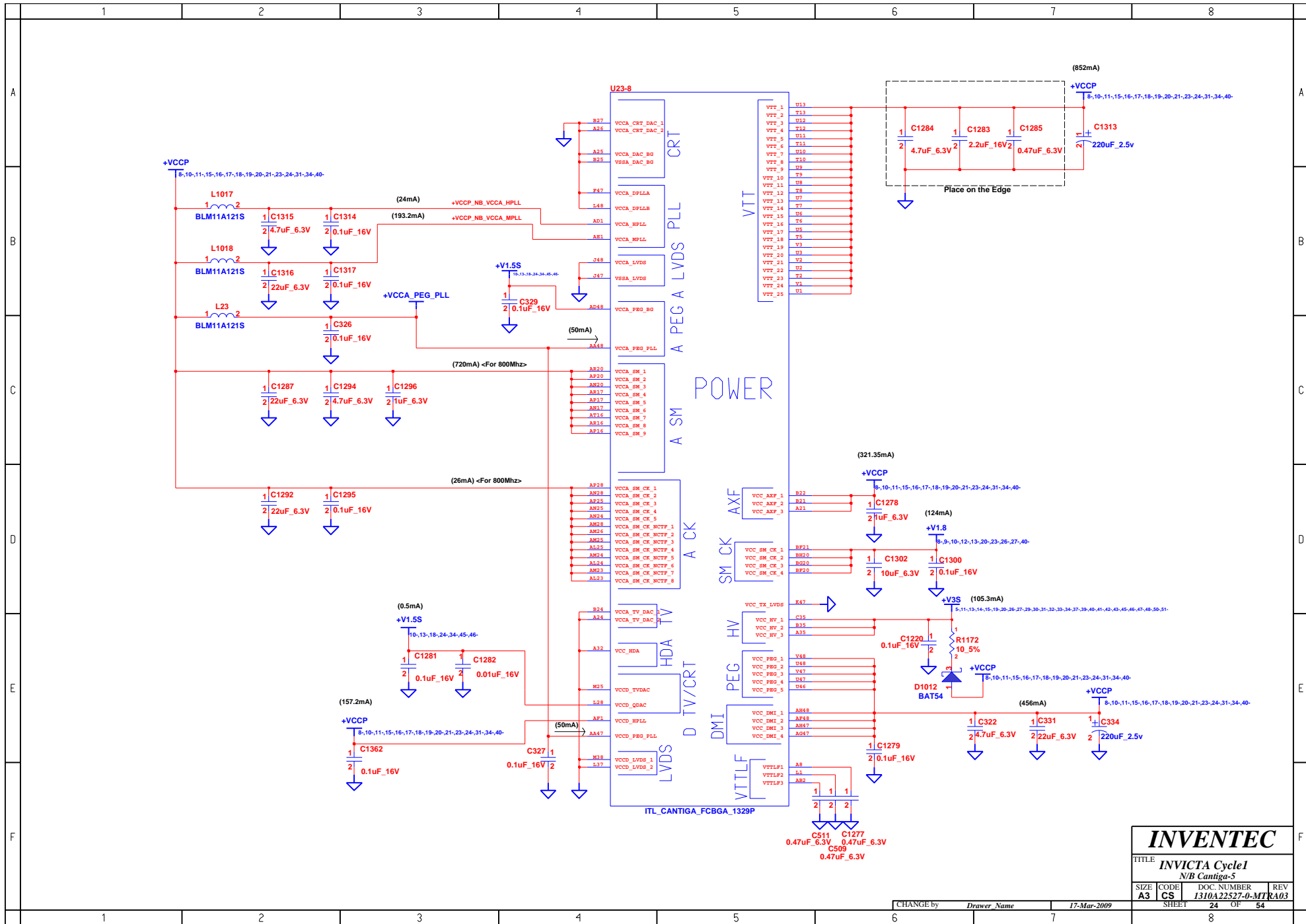
TITLE: **INVICTA Cycle1**
N/B Cantiga-3

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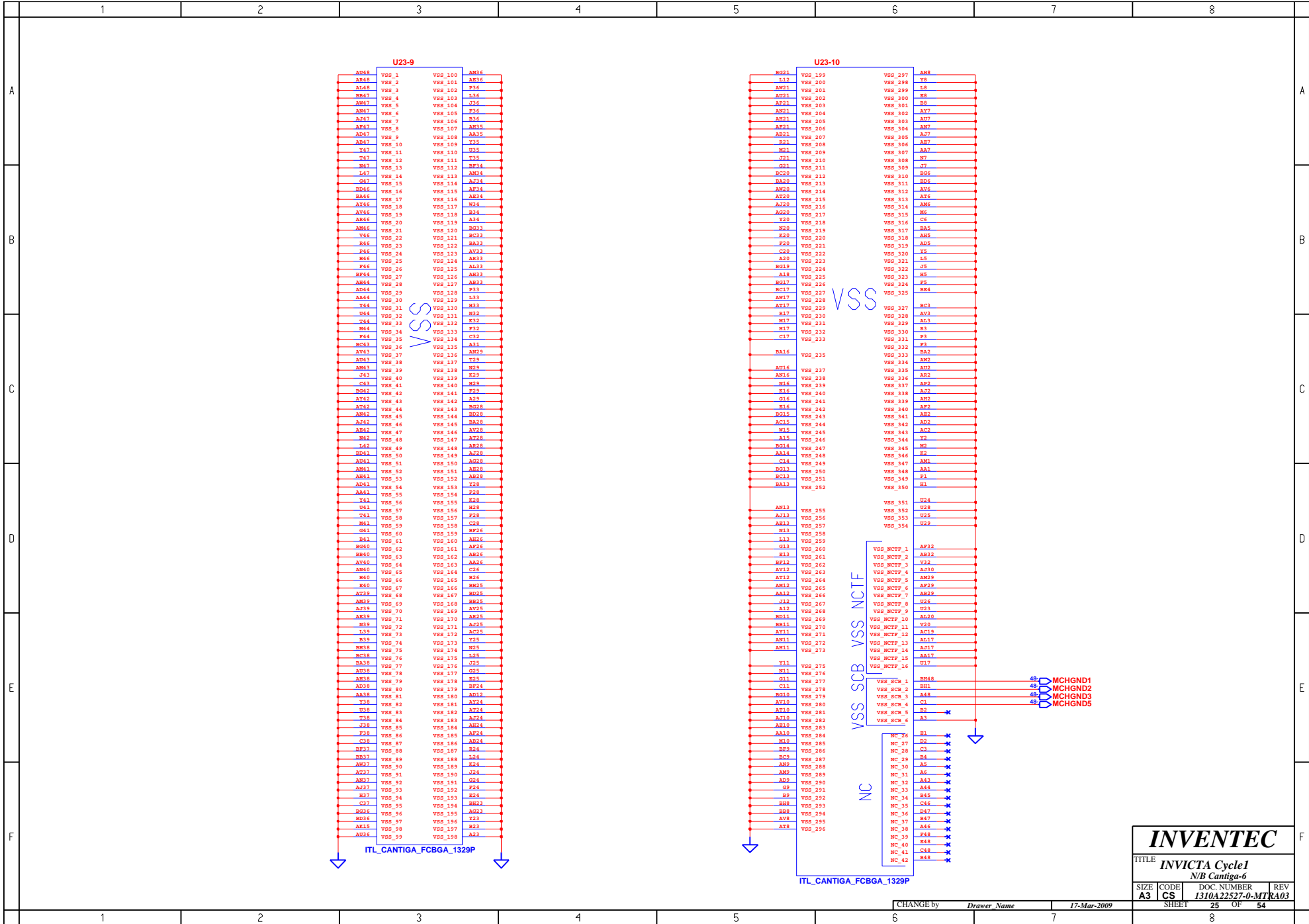
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INVENTEC			
TITLE INVICTA Cycle1 <i>N/B Cantiga-4</i>			
SIZE A3	CODE CS	DOC NUMBER I310A22527-0-MTR	REV A03
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INVENTEC			
TITLE <i>INVICTA Cycle1</i> <i>N/B Cantiga-5</i>			
SIZE A3	CODE CS	DOC NUMBER <i>1310A22527-0-MIT</i>	REV R403
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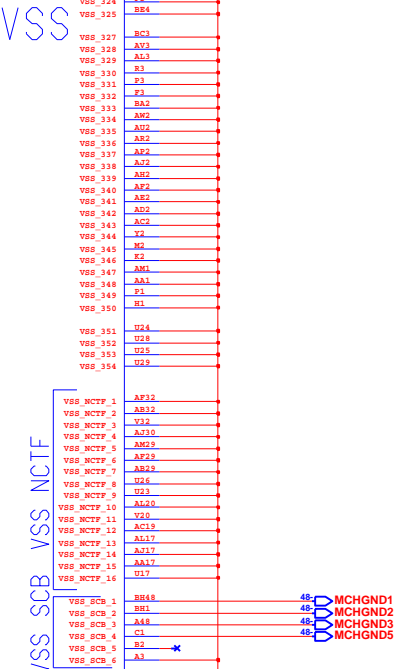
AR48	V88_1	AM16
AR48	V88_2	AR16
AL48	V88_3	F16
BR47	V88_4	V16
AM47	V88_5	F16
AM47	V88_6	F16
A747	V88_7	V16
AR47	V88_8	AR16
MD47	V88_9	AM16
AB47	V88_10	V16
Y47	V88_11	V16
T47	V88_12	V16
N47	V88_13	RF14
L47	V88_14	AM14
Q47	V88_15	A214
RA16	V88_16	AR14
BA16	V88_17	AR14
AY46	V88_18	V14
AV46	V88_19	R14
AR46	V88_20	A14
AM46	V88_21	RG13
V46	V88_22	BC13
R46	V88_23	RA13
FA6	V88_24	AR13
H46	V88_25	V13
FA6	V88_26	V13
RF44	V88_27	AR13
AR44	V88_28	AR13
AD44	V88_29	P13
AA44	V88_30	V13
T44	V88_31	R13
D44	V88_32	R13
T44	V88_33	K13
M44	V88_34	V13
K44	V88_35	C13
BC43	V88_36	A13
AV43	V88_37	AM19
AM43	V88_38	V19
AM43	V88_39	V19
AM43	V88_40	K19
C43	V88_41	V19
AY42	V88_42	V19
AT42	V88_43	V19
AM42	V88_44	RG19
AM42	V88_45	RG19
AR42	V88_46	AR19
AR42	V88_47	AR19
R42	V88_48	V19
L42	V88_49	AR19
BR41	V88_50	AR19
AM41	V88_51	AR19
AM41	V88_52	AR19
AM41	V88_53	AR19
AM41	V88_54	V19
AM41	V88_55	V19
Y41	V88_56	K19
D41	V88_57	V19
T41	V88_58	V19
M41	V88_59	C19
G41	V88_60	BP16
R41	V88_61	AR16
RG40	V88_62	AR16
AV40	V88_63	AA16
AM40	V88_64	V16
R40	V88_65	V16
R40	V88_66	V16
AT19	V88_67	ND15
AM19	V88_68	ND15
AM19	V88_69	AR15
AM19	V88_70	AR15
AR19	V88_71	AR15
N19	V88_72	A215
L19	V88_73	AC15
B19	V88_74	V15
BB18	V88_75	V15
BC18	V88_76	V15
BA18	V88_77	V15
AD18	V88_78	Q15
AB18	V88_79	R15
AD18	V88_80	RF14
AA18	V88_81	AR14
Y18	V88_82	AR14
V18	V88_83	AT14
T18	V88_84	AR14
F18	V88_85	AR14
F18	V88_86	AR14
C18	V88_87	AR14
RF17	V88_88	R14
BR17	V88_89	R14
AM17	V88_90	R14
AT17	V88_91	V14
AM17	V88_92	V14
AM17	V88_93	V14
H17	V88_94	R14
C17	V88_95	RB13
BR16	V88_96	AG13
BR16	V88_97	V13
AK15	V88_98	R13
AD16	V88_99	A13

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RG21	V88_199	AM8
L12	V88_200	V8
AM21	V88_201	V8
AM21	V88_202	V8
AM21	V88_203	V8
AM21	V88_204	V8
AM21	V88_205	V8
AR21	V88_206	V8
AR21	V88_207	V8
R21	V88_208	V8
RG1	V88_209	V8
Q21	V88_210	V8
Q21	V88_211	V8
BC20	V88_212	V8
RA20	V88_213	V8
AR20	V88_214	V8
AT20	V88_215	V8
A220	V88_216	V8
AG20	V88_217	V8
V20	V88_218	V8
R20	V88_219	V8
F20	V88_220	V8
F20	V88_221	V8
C20	V88_222	V8
A20	V88_223	V8
RG19	V88_224	V8
R19	V88_225	V8
BR19	V88_226	V8
BC17	V88_227	V8
AM17	V88_228	V8
AM17	V88_229	V8
R17	V88_230	V8
M17	V88_231	V8
H17	V88_232	V8
C17	V88_233	V8
BA16	V88_235	V8
AM16	V88_237	V8
AM16	V88_238	V8
R16	V88_239	V8
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RG15	V88_242	V8
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AM14	V88_245	V8
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AM14	V88_248	V8
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V12	V88_267	V8
A12	V88_268	V8
BB11	V88_269	V8
BB11	V88_270	V8
AT11	V88_271	V8
AM11	V88_272	V8
AM11	V88_273	V8
V11	V88_275	V8
R11	V88_276	V8
Q11	V88_277	V8
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AM10	V88_280	V8
AT10	V88_281	V8
AG10	V88_282	V8
AM10	V88_283	V8
AM10	V88_284	V8
M10	V88_285	V8
BP2	V88_286	V8
BC2	V88_287	V8
AM2	V88_288	V8
AM2	V88_289	V8
AG2	V88_290	V8
Q2	V88_291	V8
R2	V88_292	V8
BB2	V88_293	V8
BB2	V88_294	V8
AM2	V88_295	V8
AT2	V88_296	V8

ITL_CANTIGA_FCBGA_1329P

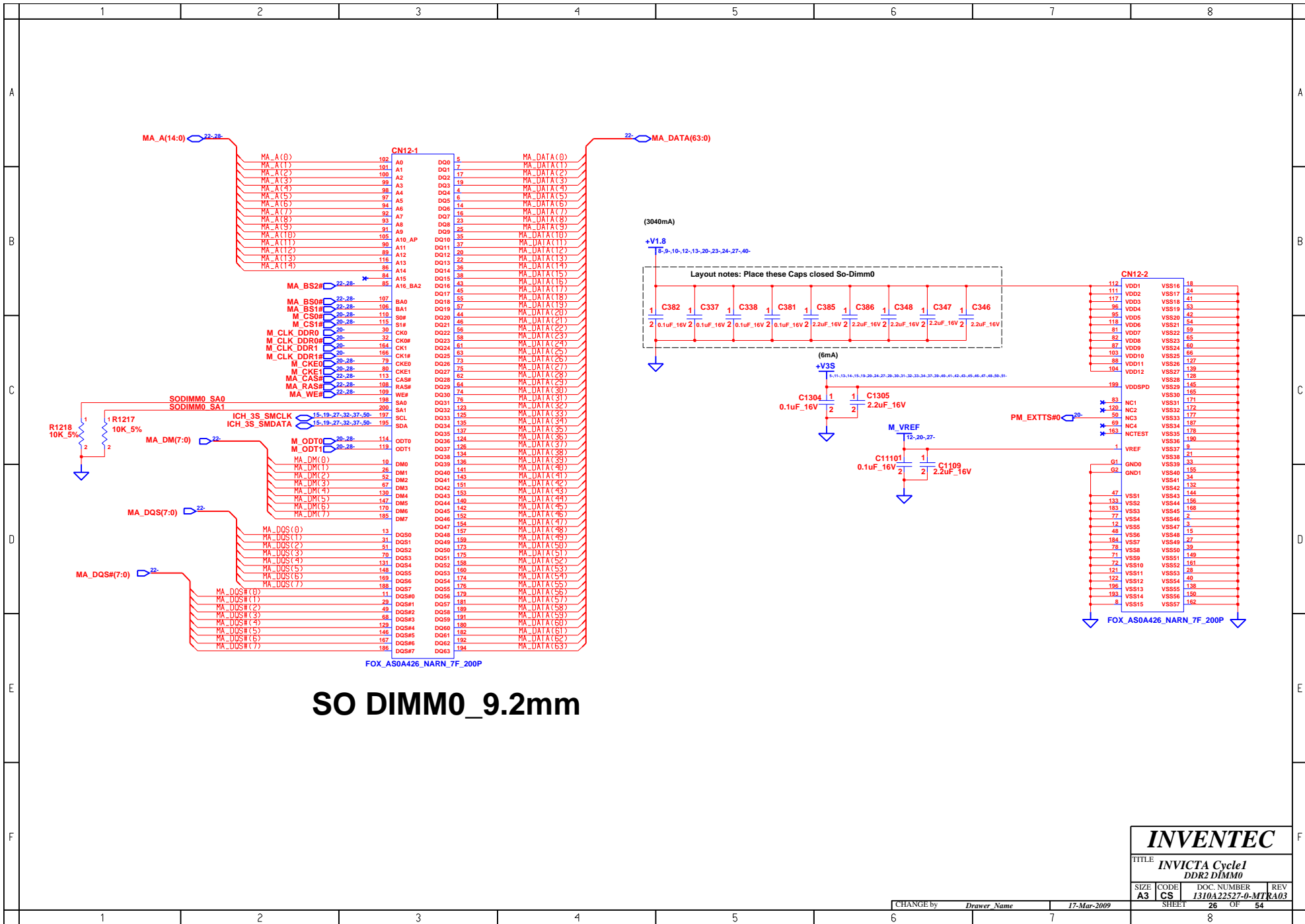


INVENTEC

TITLE **INVICTA Cycle1**
N/B Cantiga-6

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MT	R403

SHEET 25 OF 54

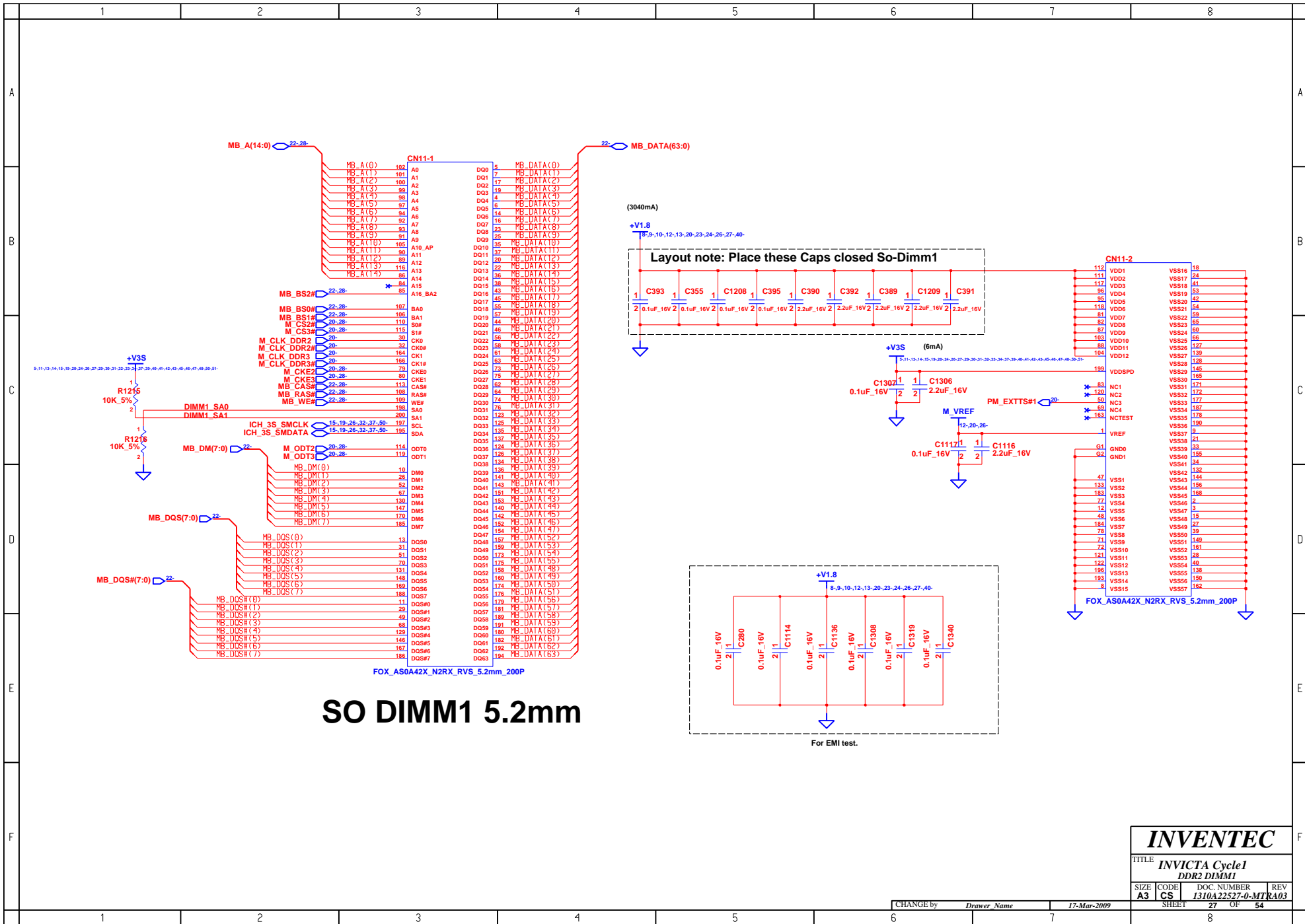


INVENTEC

TITLE: **INVICTA Cycle1 DDR2 DIMM0**

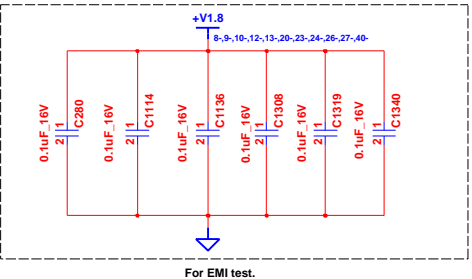
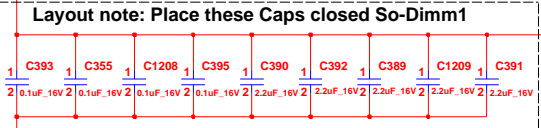
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03

CHANGE by: *Drawer Name* 17-Mar-2009 SHEET 26 OF 54

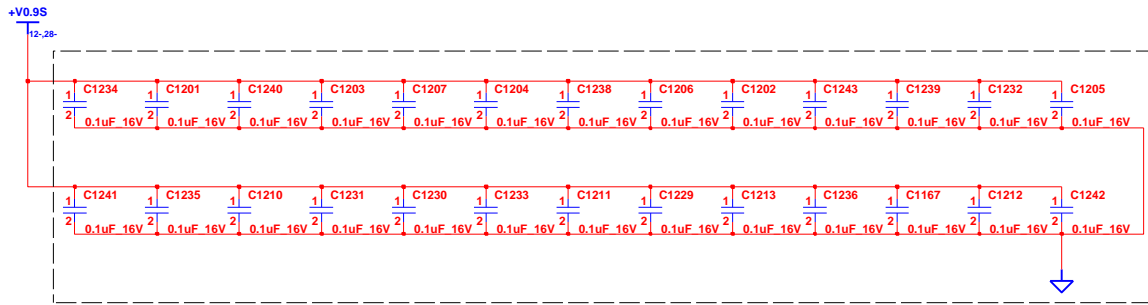


SO DIMM1 5.2mm

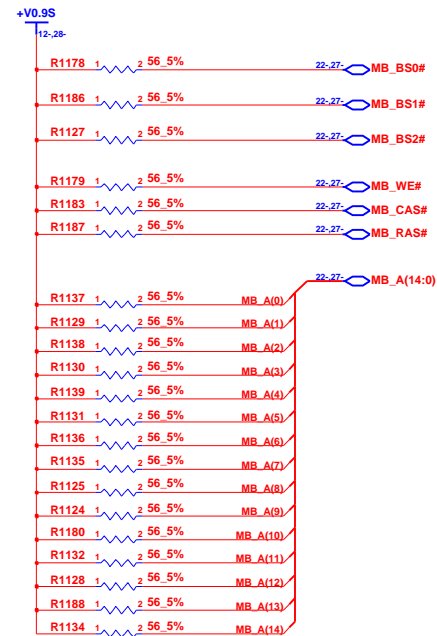
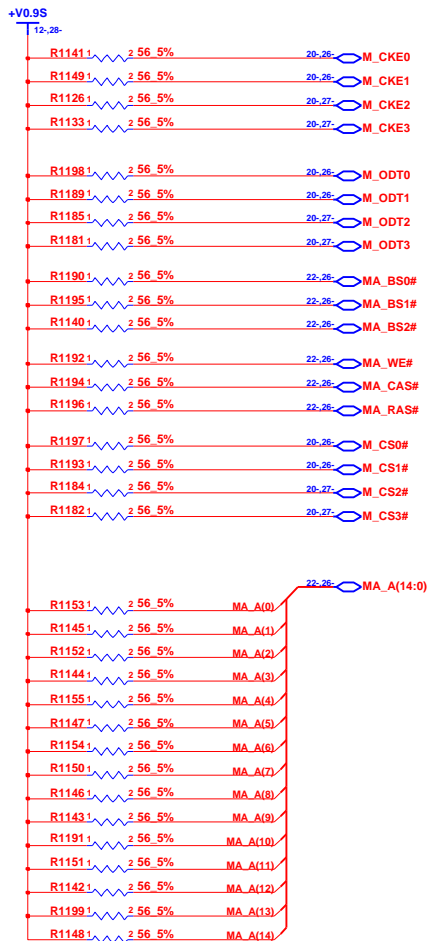
FOX_AS0A42X_N2RX_RVS_5.2mm_200P



INVENTEC			
TITLE INVICTA Cycle1 DDR2 DIMM1			
SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MT	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
SHEET 27		OF 54	



Layout notes : Place one Cap close to every 2 pull up resistor terminated to +V0.9S.

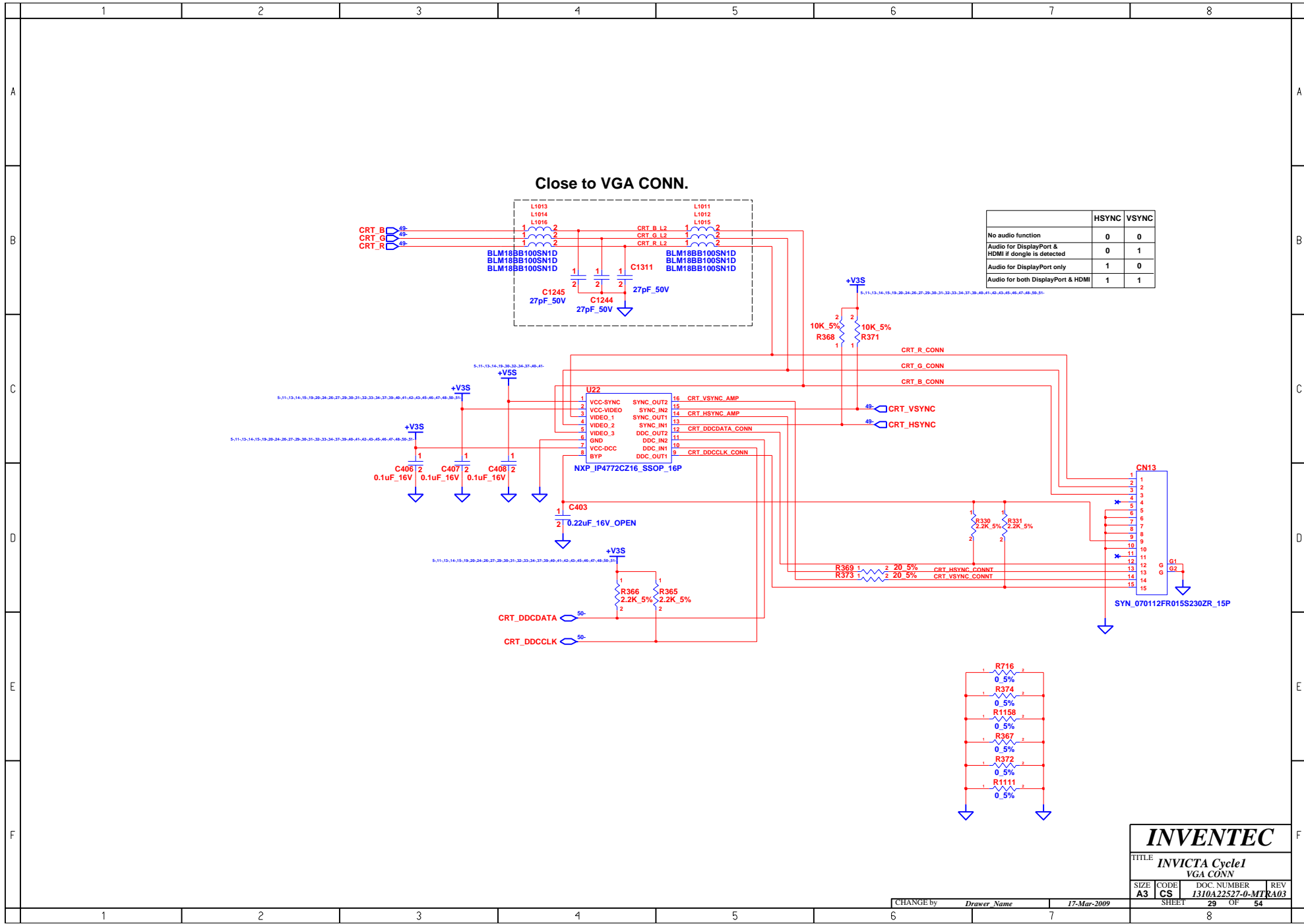


INVENTEC

TITLE
INVICTA Cycle1
DDR2 termination

SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MTR	REV A03
SHEET 28		OF 54	

CHANGE by *Drawer Name* 27-Sep-2003



	HSYNC	VSYNC
No audio function	0	0
Audio for DisplayPort & HDMI if dongle is detected	0	1
Audio for DisplayPort only	1	0
Audio for both DisplayPort & HDMI	1	1

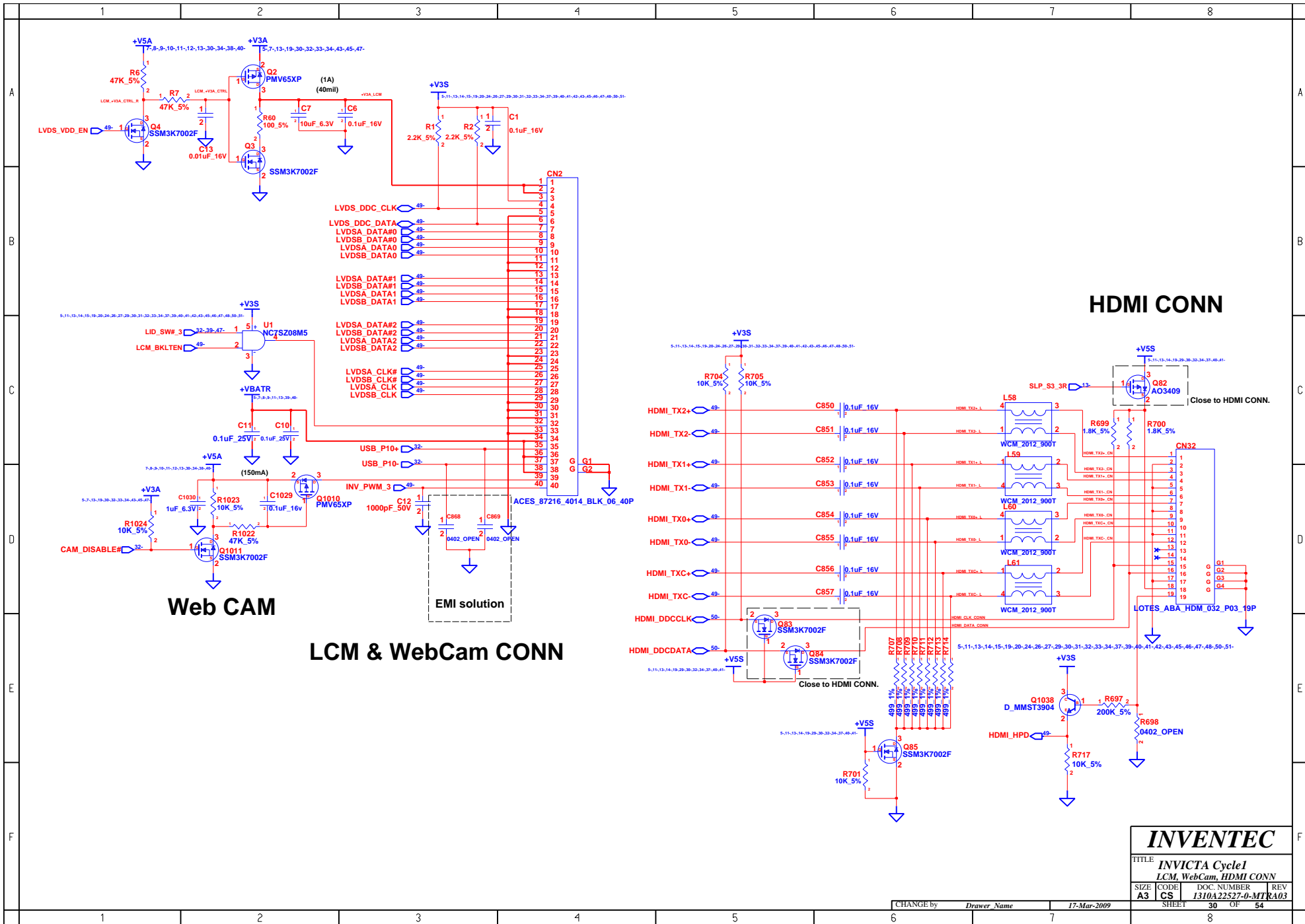
CN13	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
												G1	G2	G	G

INVENTEC

TITLE: **INVICTA Cycle1
VGA CONN**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03

CHANGE by: *Drawer Name* 17-Mar-2009 SHEET 29 OF 54



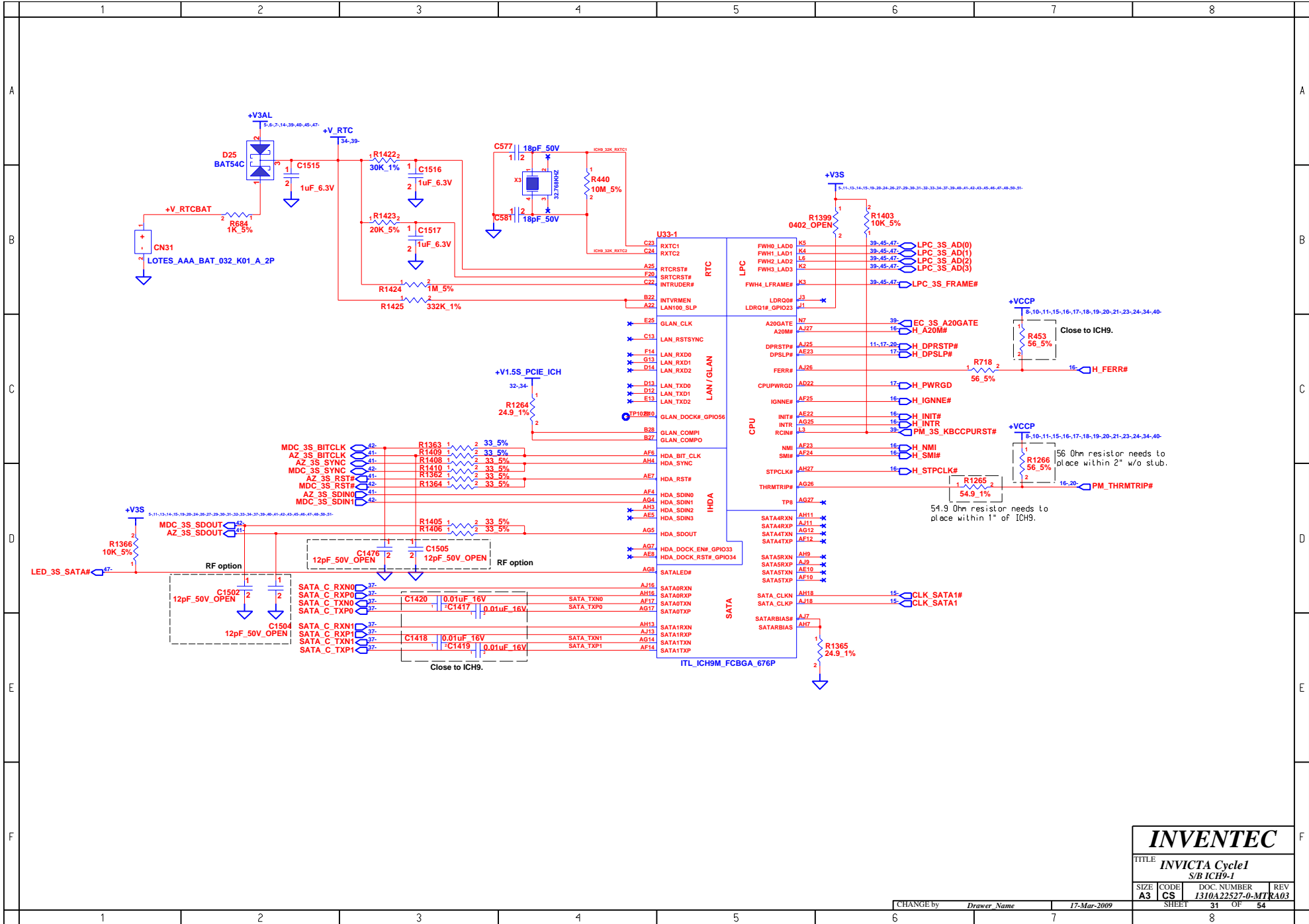
Web CAM

LCM & WebCam CONN

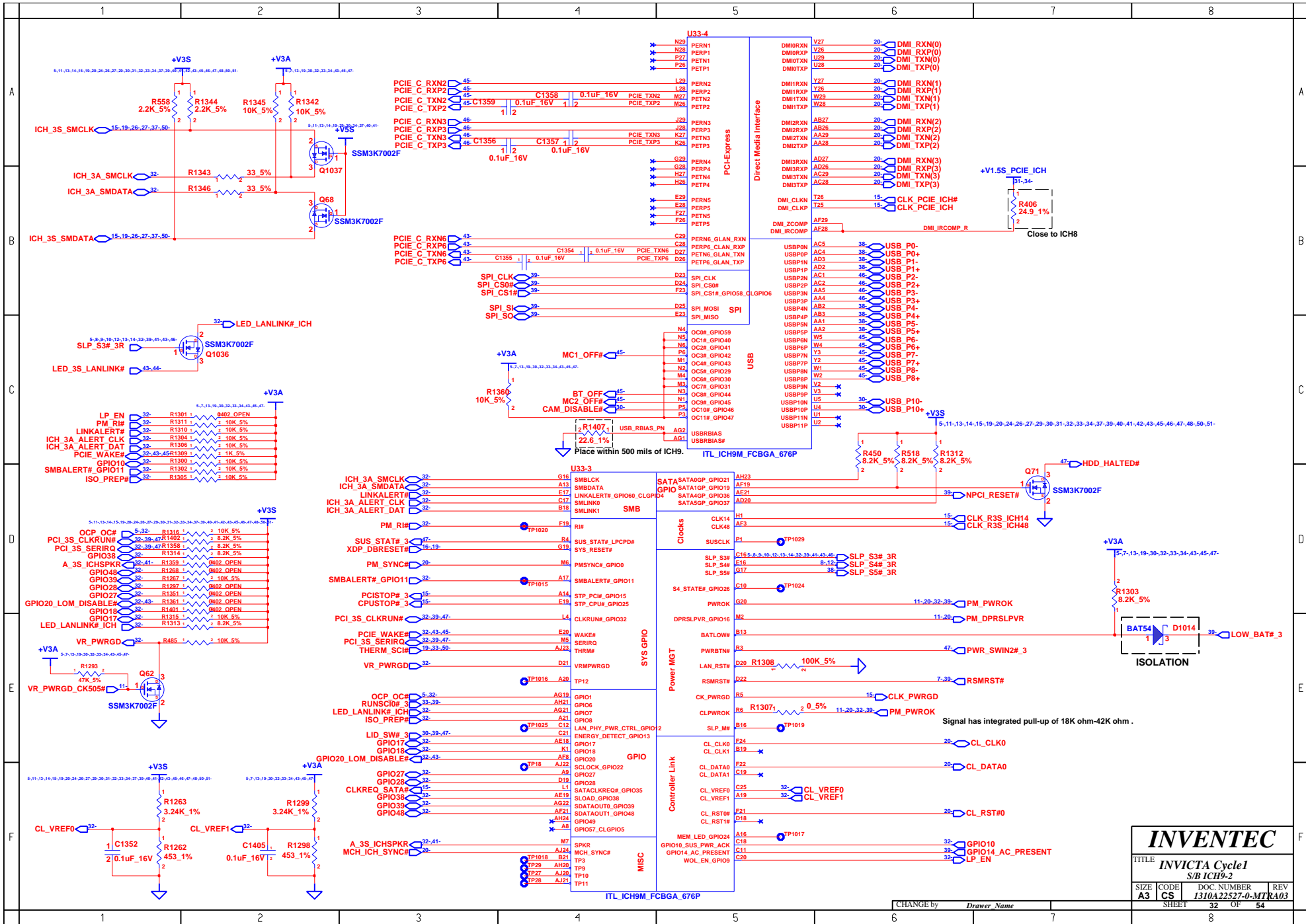
HDMI CONN

INVENTEC

TITLE INVICTA Cycle1			
LCM, WebCam, HDMI CONN			
SIZE A3	CODE CS	DOC NUMBER I310A22527-0-MTR	REV A03
CHANGE by <i>Drawer Name</i>		DATE 17-Mar-2009	SHEET 30 OF 54

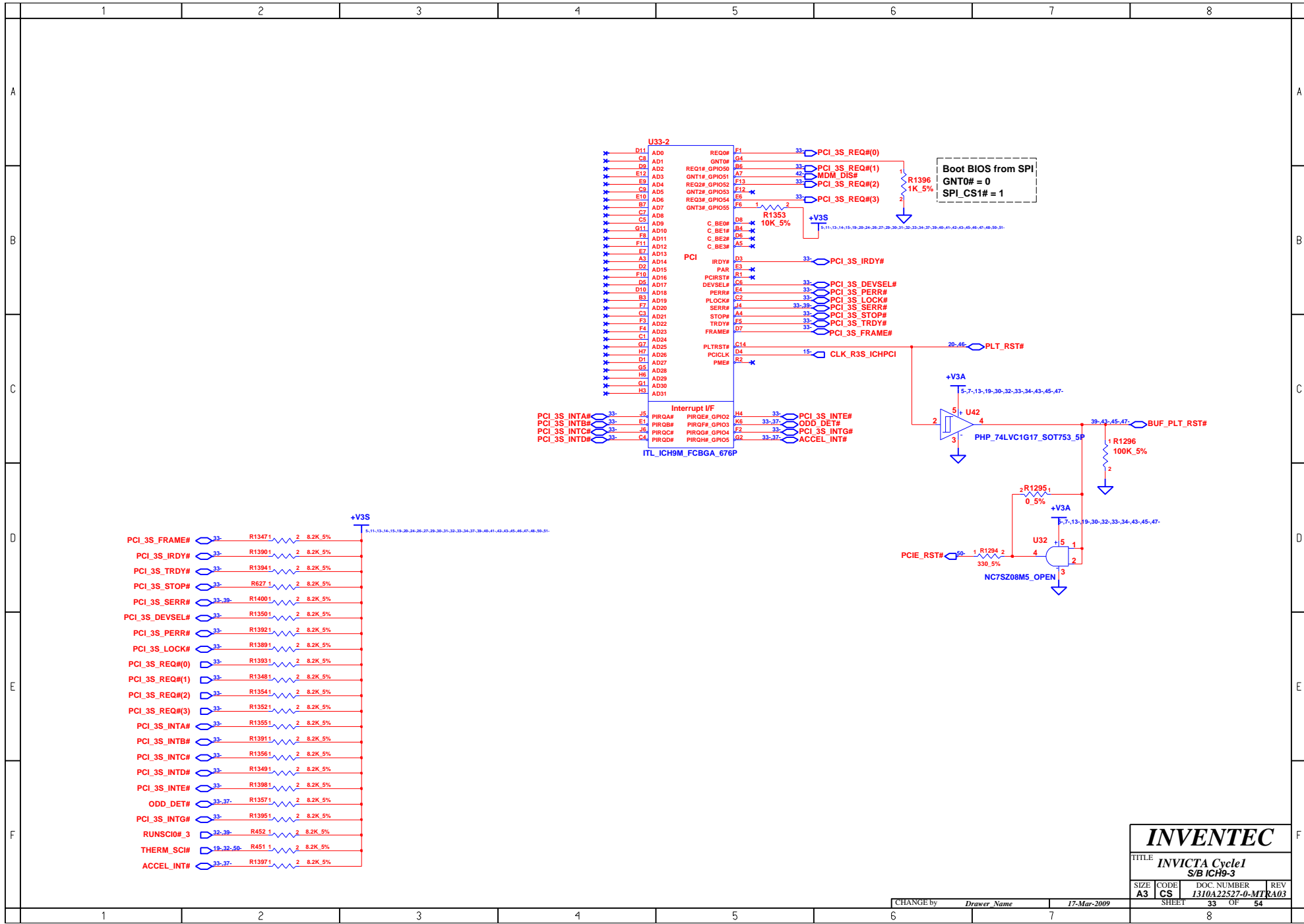


INVENTEC			
TITLE <i>INVICTA Cycle1</i> S/B ICH9-1			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		31	OF 54

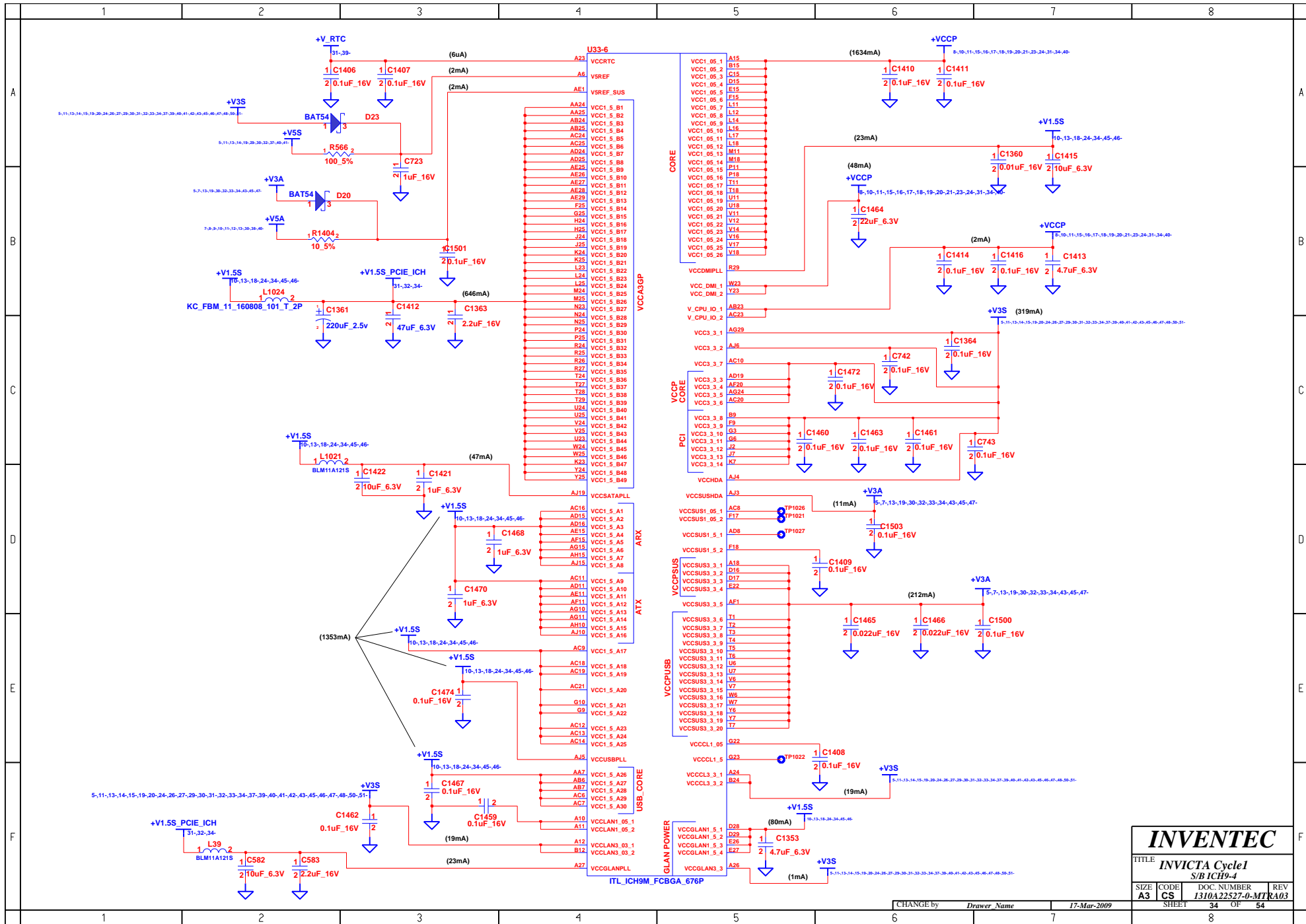


INVENTEC			
TITLE <i>INVICTA Cycle1</i> <i>S/B ICH9-2</i>			
SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MTR	REV A03
SHEET 32		OF 54	

CHANGE by *Drawer Name* 8



INVENTEC			
TITLE INVICTA Cycle1 S/B ICH9-3			
SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MT	REV RA03
CHANGE by Drawer Name		17-Mar-2009	SHEET 33 OF 54



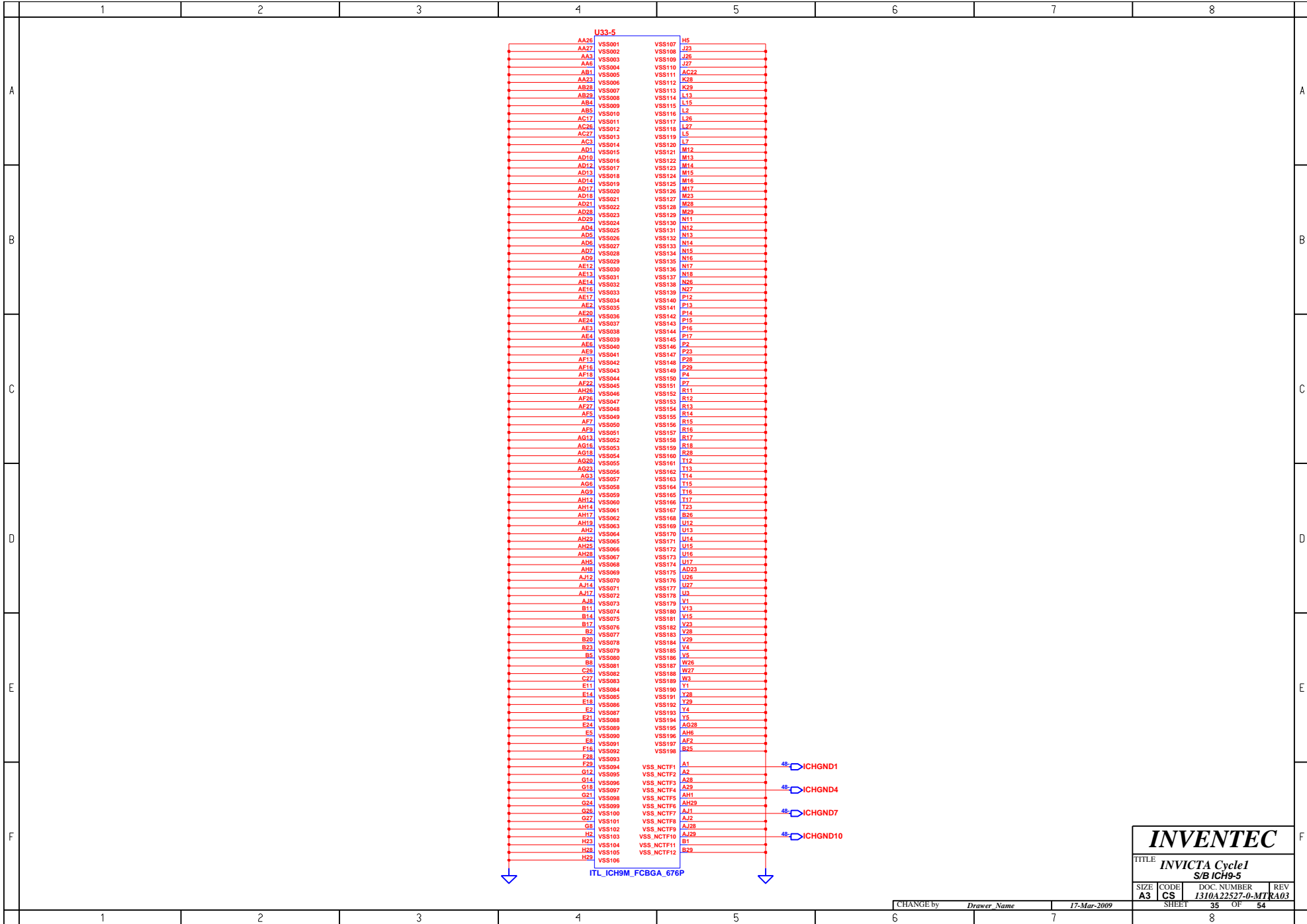
INVENTEC

TITLE: INVICTA Cycle1
S/B ICH9-d

SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A22527-0-MIT	R403

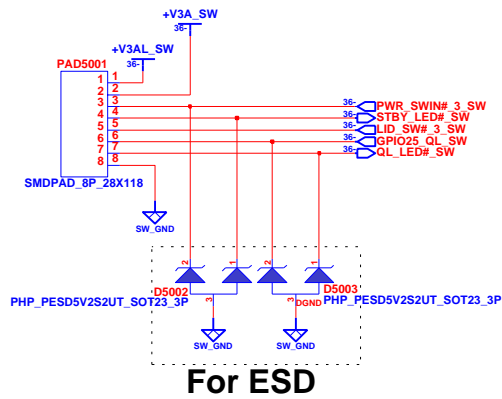
SHEET 34 OF 54

CHANGE by *Drawer Name* 17-Mar-2009



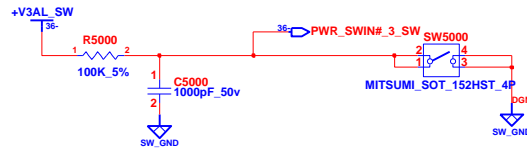
INVENTEC			
TITLE <i>INVICTA Cycle 1</i>			
S/B <i>ICH9-5</i>			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		35	OF 54

PWR SW B/B CONN

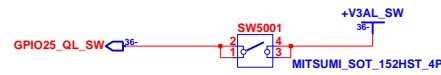


For ESD

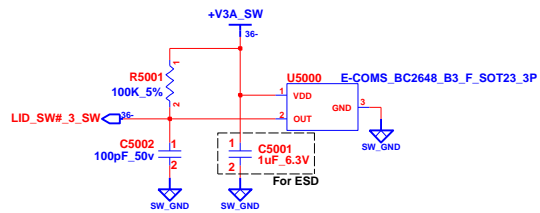
Power Button



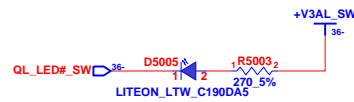
Quick Look Button



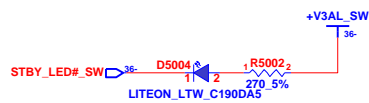
LID Switch



Quick Look LED



Power / Standby LED



- FIX5000
- FIX_MASK
- FIX5001
- FIX_MASK
- FIX5002
- FIX_MASK
- FIX5003
- FIX_MASK
- FIX5004
- FIX_MASK
- FIX5005
- FIX_MASK

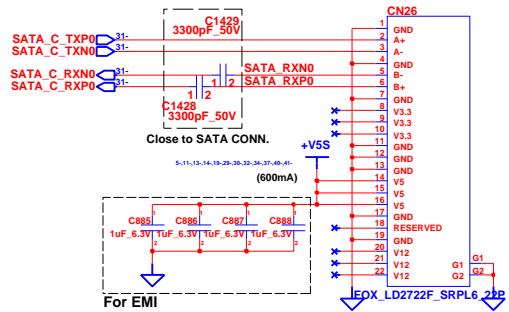
Power & LID Switch Board

INVENTEC

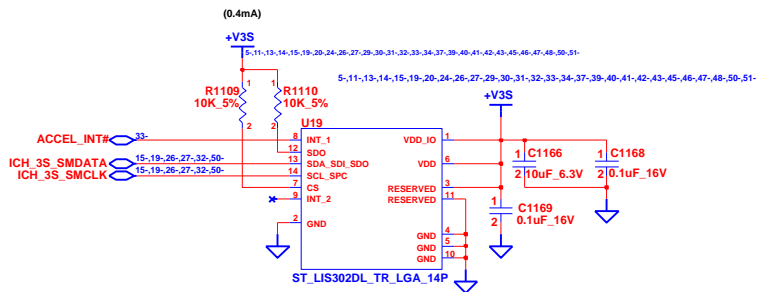
TITLE INVICTA Cycle1			
PWR, LID, APP SW/Bs			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		36	OF 54

CHANGE by *Drawer Name* 17-Mar-2009

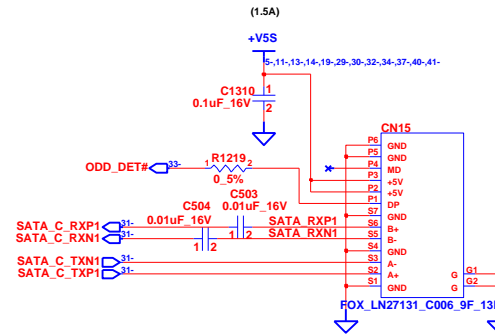
SHEET 36 OF 54



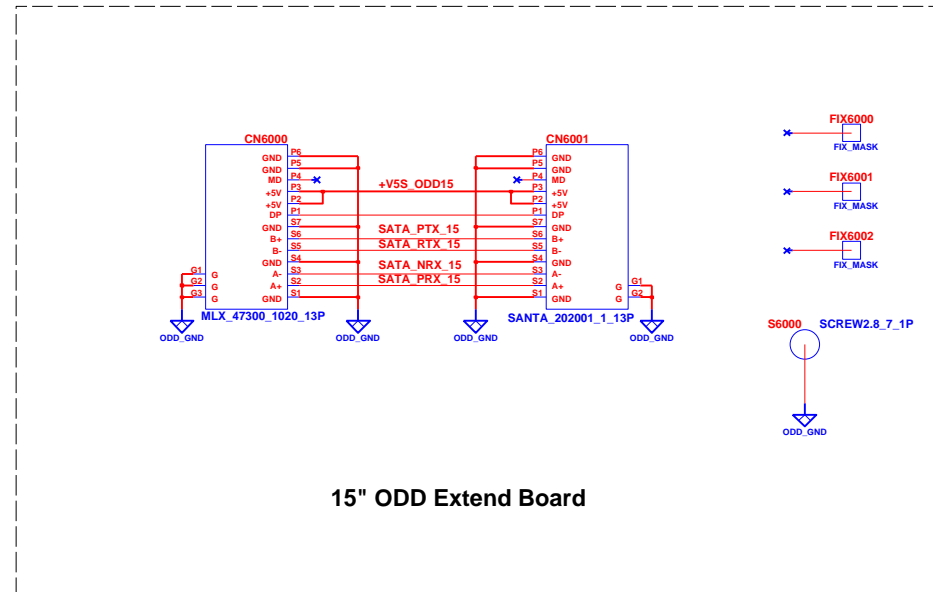
SATA HDD



Accelerometer



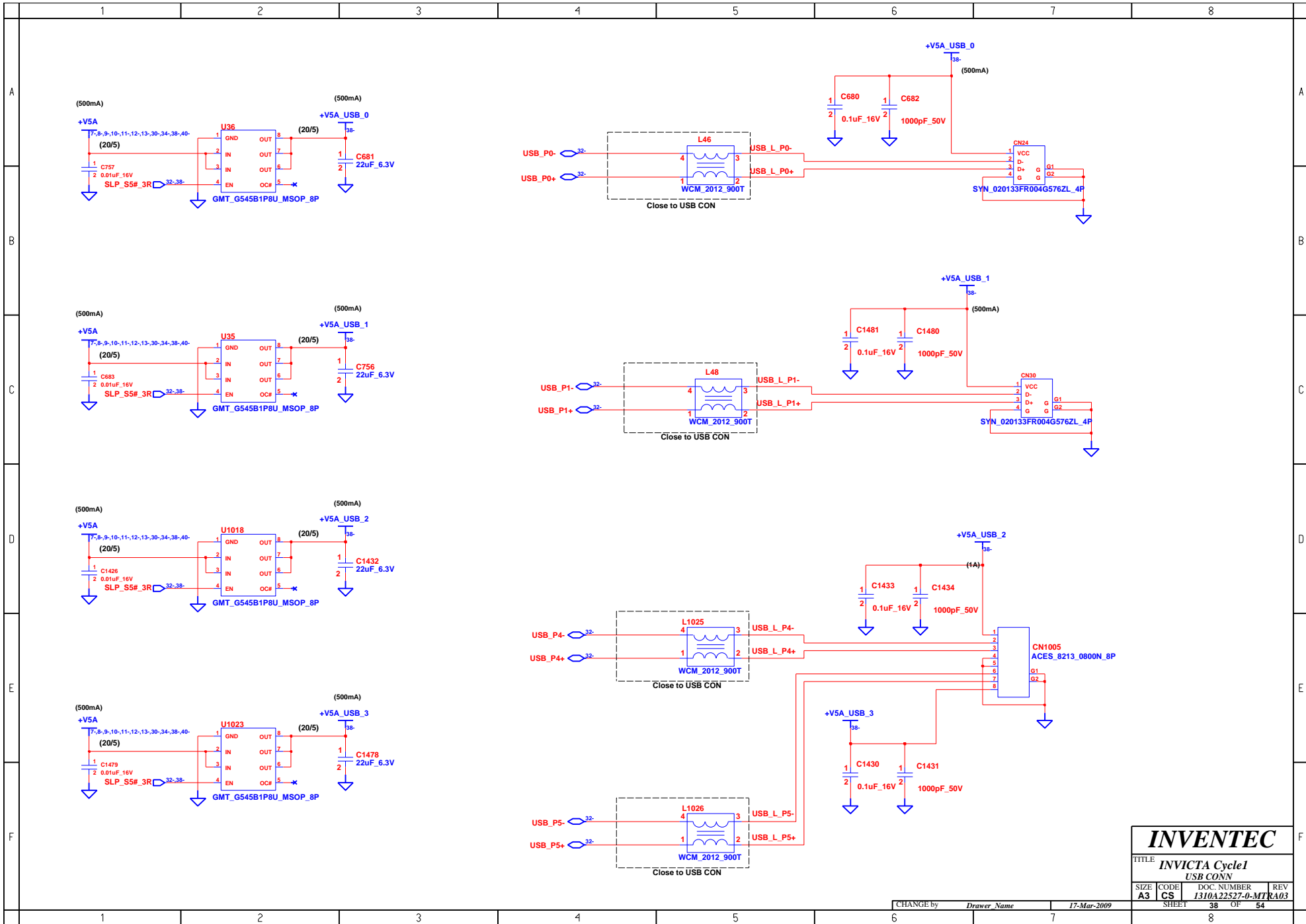
SATA ODD



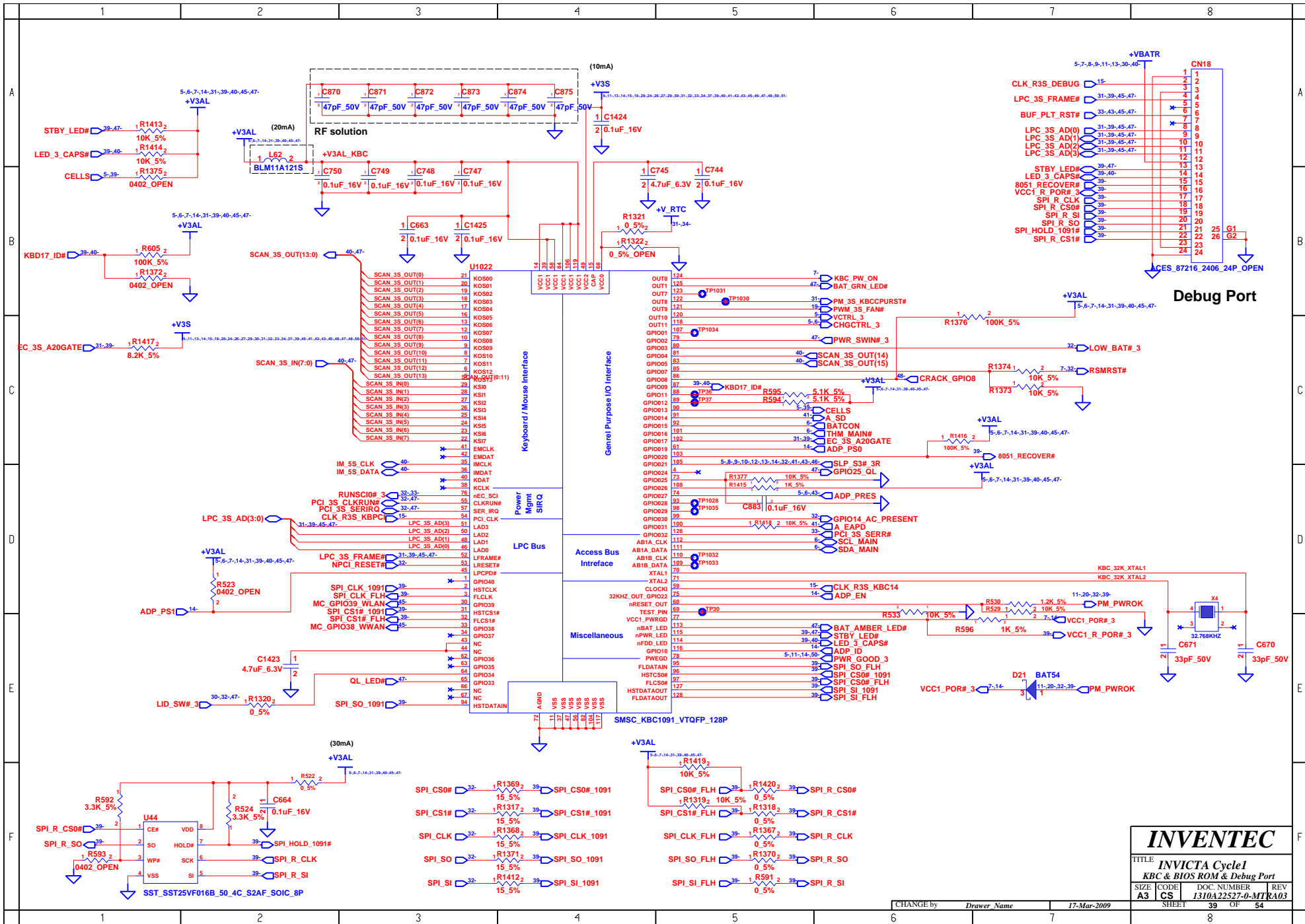
15" ODD Extend Board

INVENTEC

TITLE			
INVICTA Cycle1			
HDD & ODD CONN & Accelerometer & 15" ODD EXT B			
SIZE	CODE	DOC NUMBER	REV
A3	CS	I310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		37	OF 54

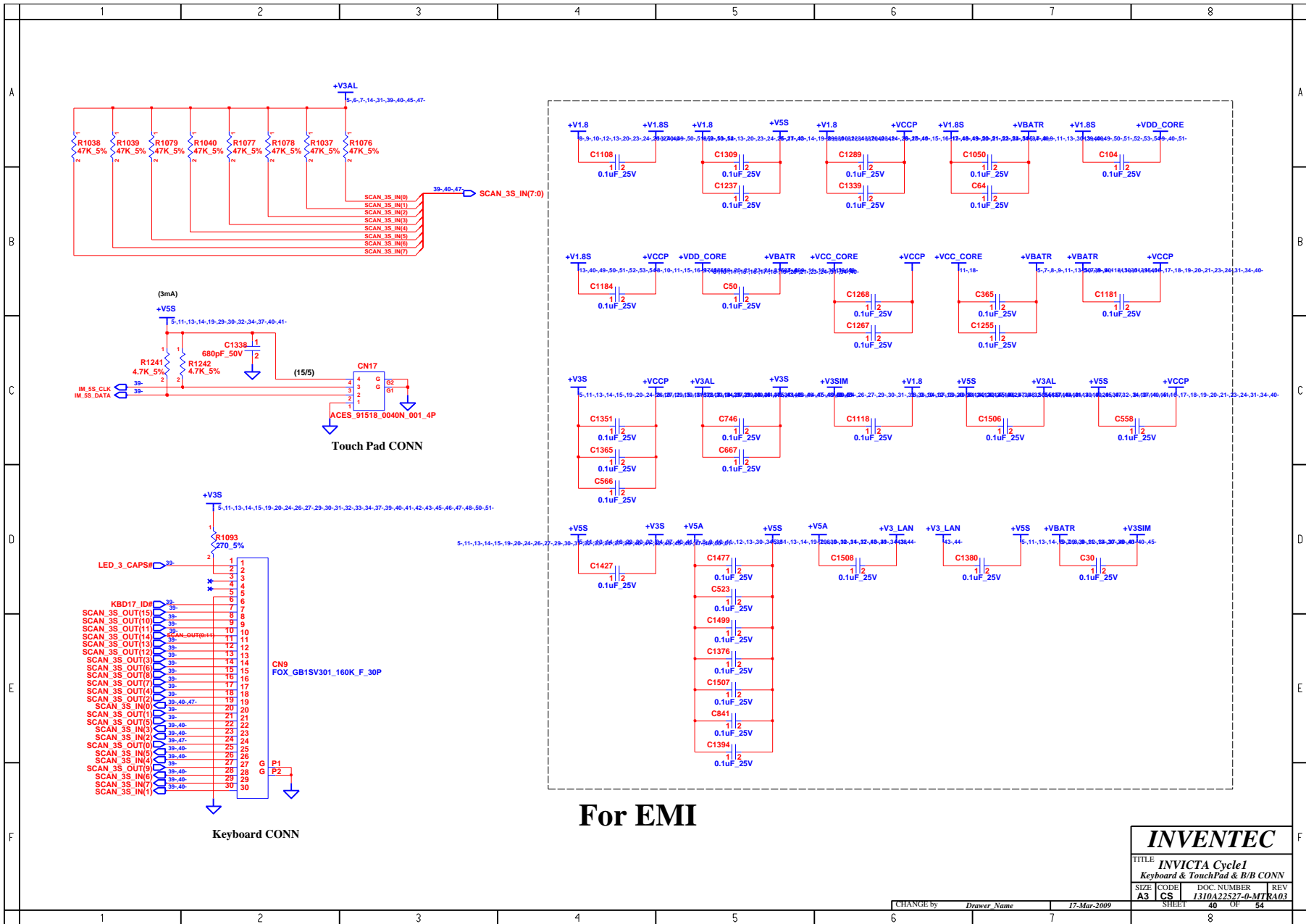


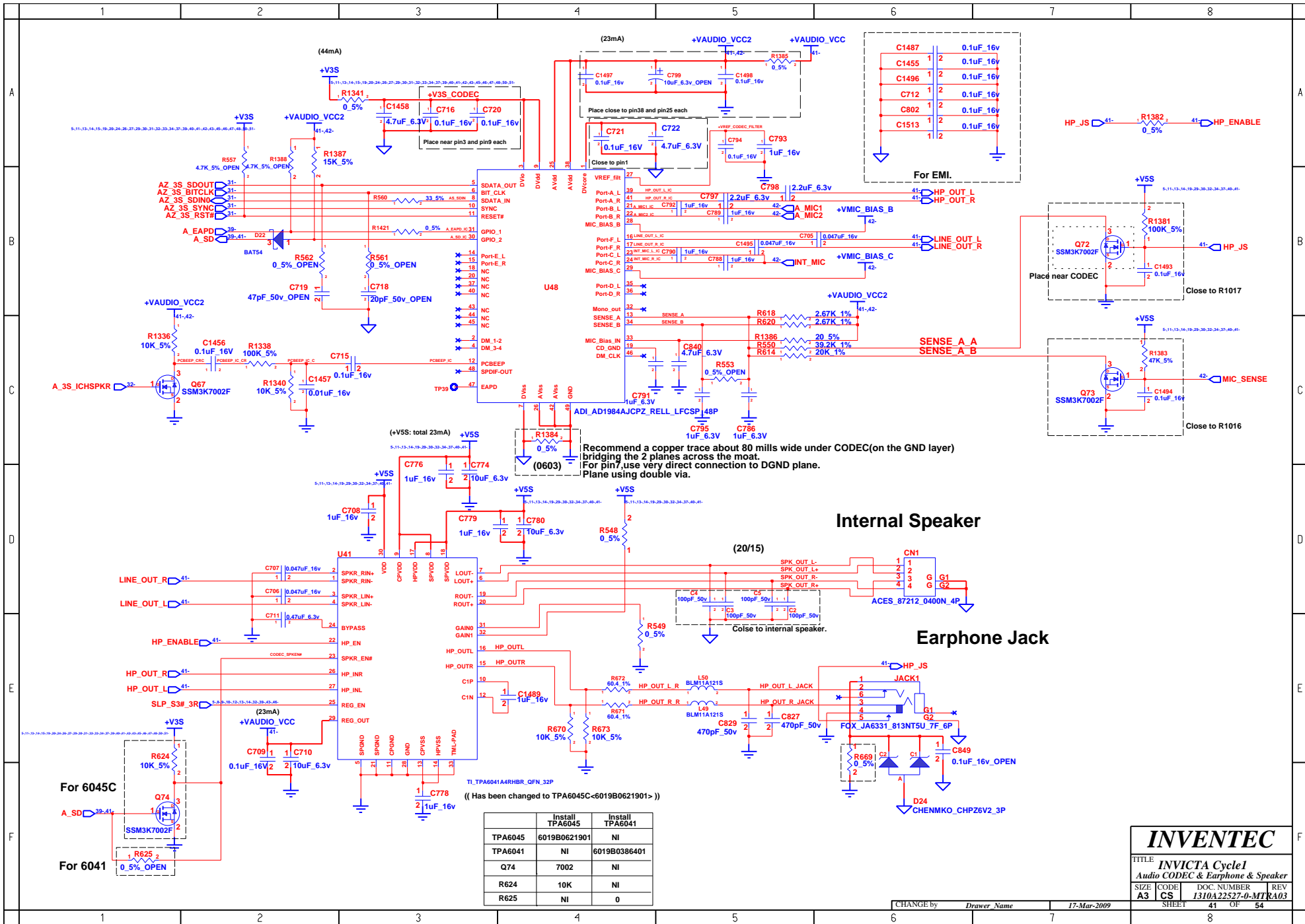
INVENTEC			
TITLE: <i>INVICTA Cycle1</i>			
USB CONN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		38	OF 54



INVENTEC			
TITLE INVICTA Cycle1			
KBC & BIOS ROM & Debug Port			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
SHEET		OF	
39		54	

CHANGE by *Drawer Name* 17-Mar-2009





Recommend a copper trace about 80 mills wide under CODEC (on the GND layer) bridging the 2 planes across the moat.
For pin7, use very direct connection to DGND plane.
Plane using double via.

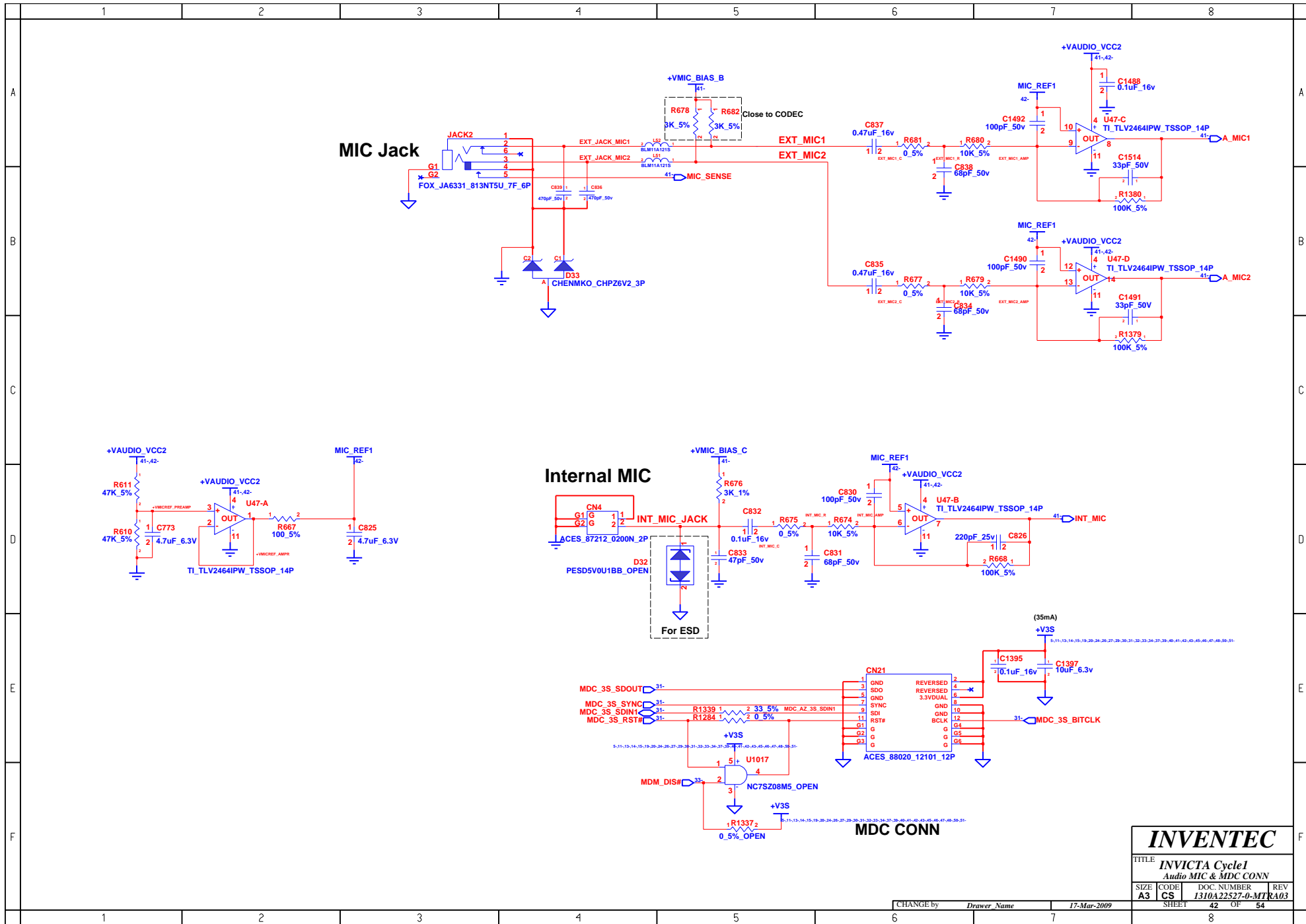
Internal Speaker

Earphone Jack

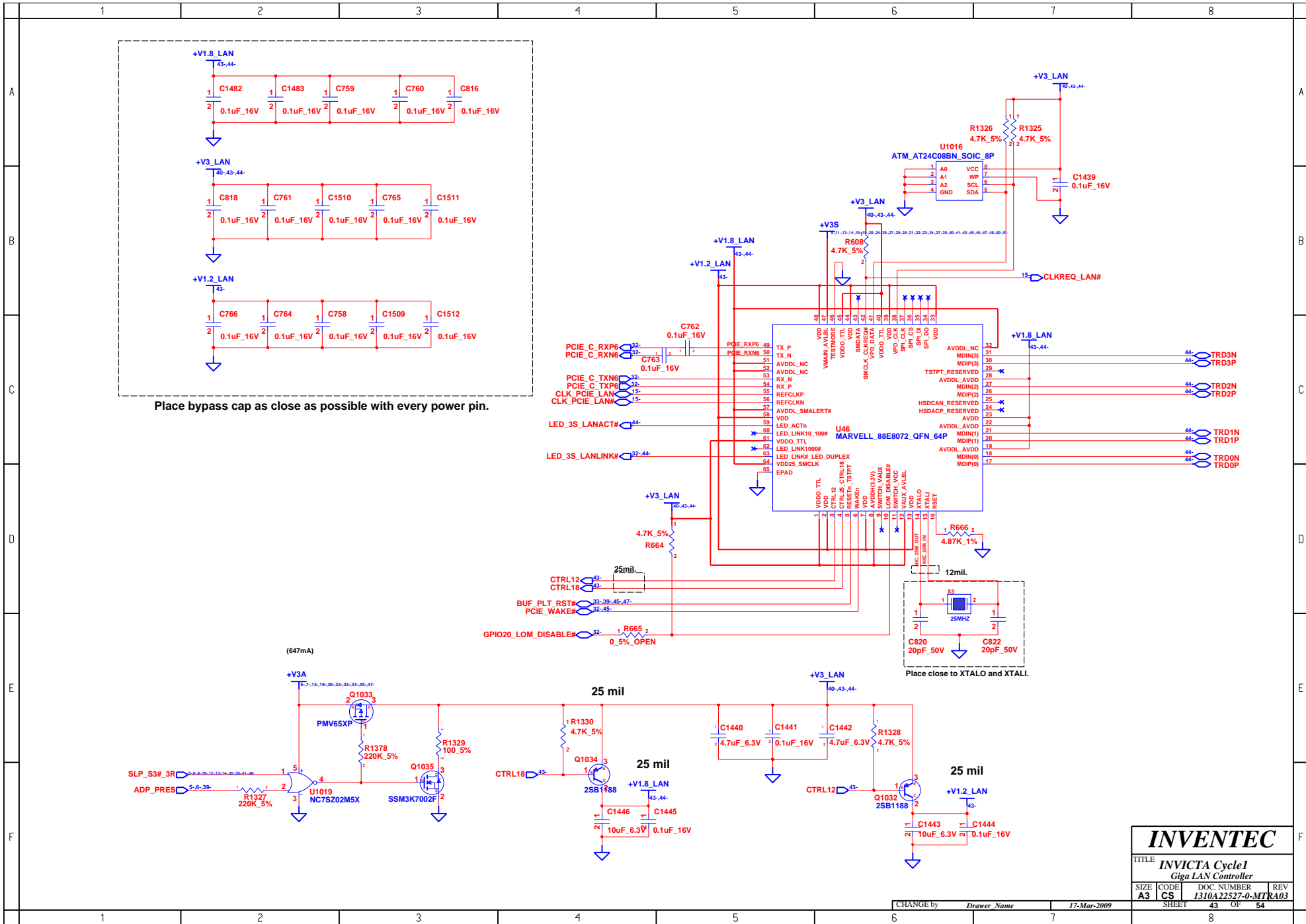
	Install TPA6045	Install TPA6041
TPA6045	6019B0621901	NI
TPA6041	NI	6019B0386401
Q74	7002	NI
R624	10K	NI
R625	NI	0

INVENTEC

TITLE: INVICTA Cycle1
Audio CODEC & Earphone & Speaker
SIZE: A3 CODE: CS DOC. NUMBER: 1310A22527-0-MTR REV: A03
SHEET: 41 OF 54



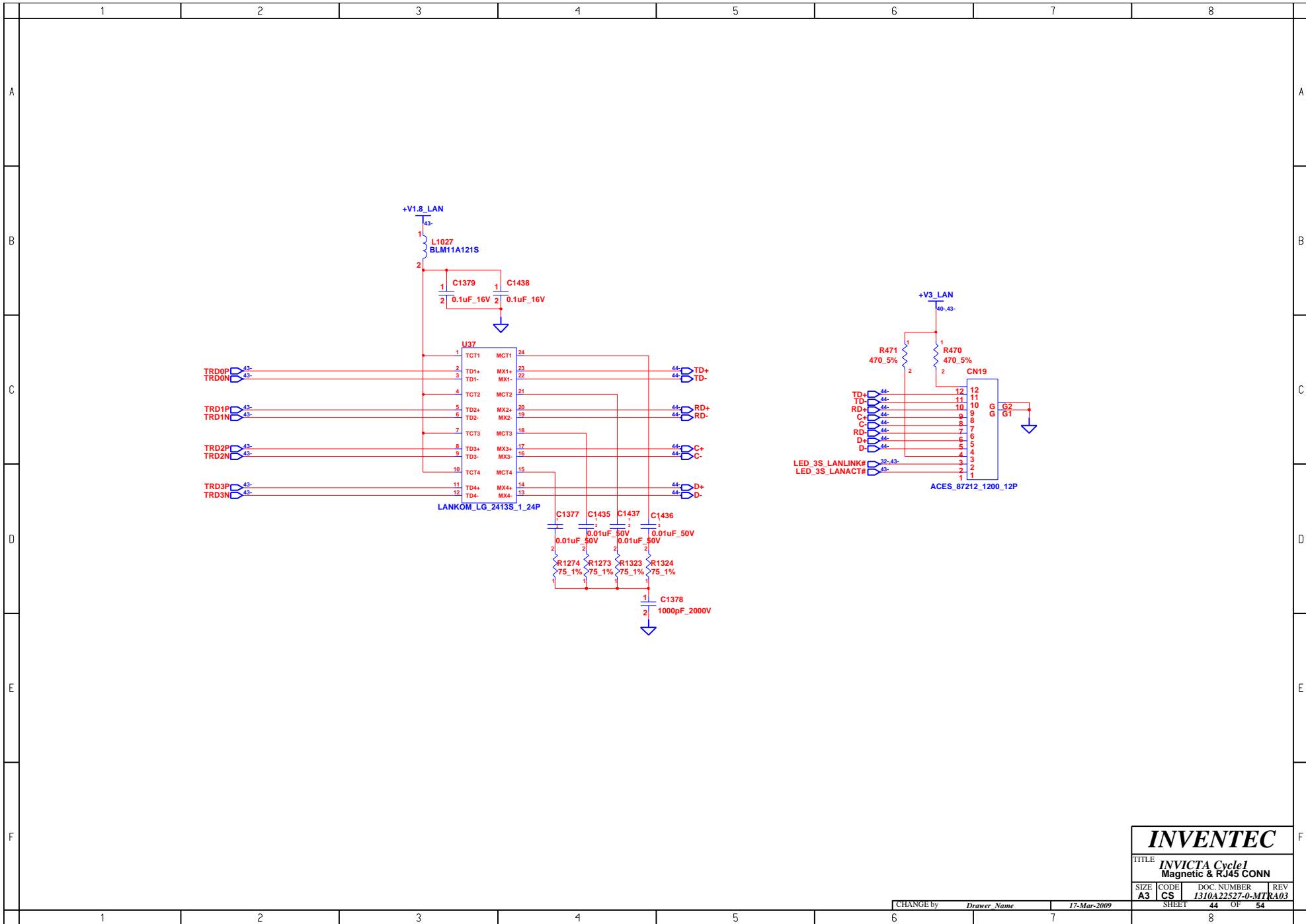
INVENTEC			
TITLE: INVICTA Cycle1			
Audio MIC & MDC CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		42	OF 54



Place bypass cap as close as possible with every power pin.

Place close to XTAL0 and XTAL1.

INVENTEC			
TITLE: INVICTA Cycle1			
Giga LAN Controller			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MIT	R403
CHANGE by		Drawer Name	17-Mar-2009
SHEET		43	OF 54



INVENTEC

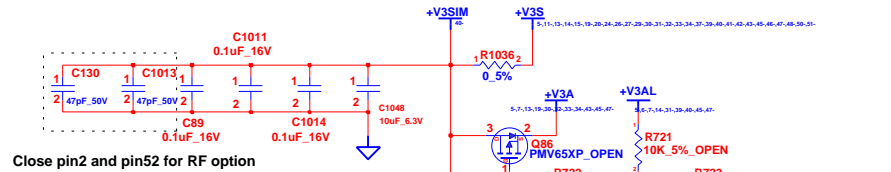
TITLE *INVICTA Cycle1*
Magnetic & RJ45 CONN

SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTR	REV A03
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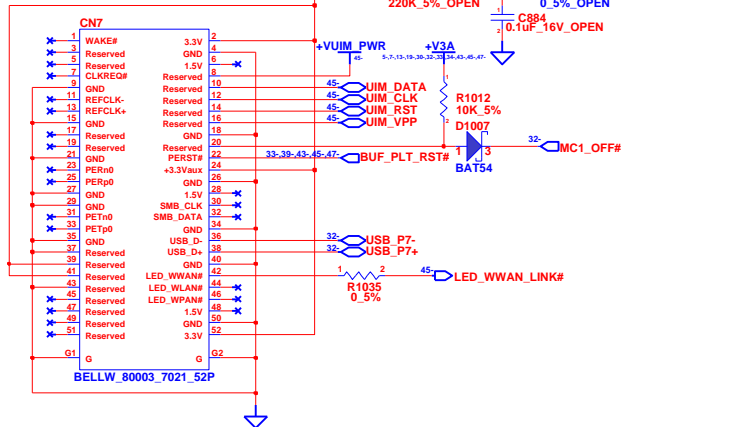
CHANGE by *Drawer Name* 17-Mar-2009

SHEET 44 OF 54

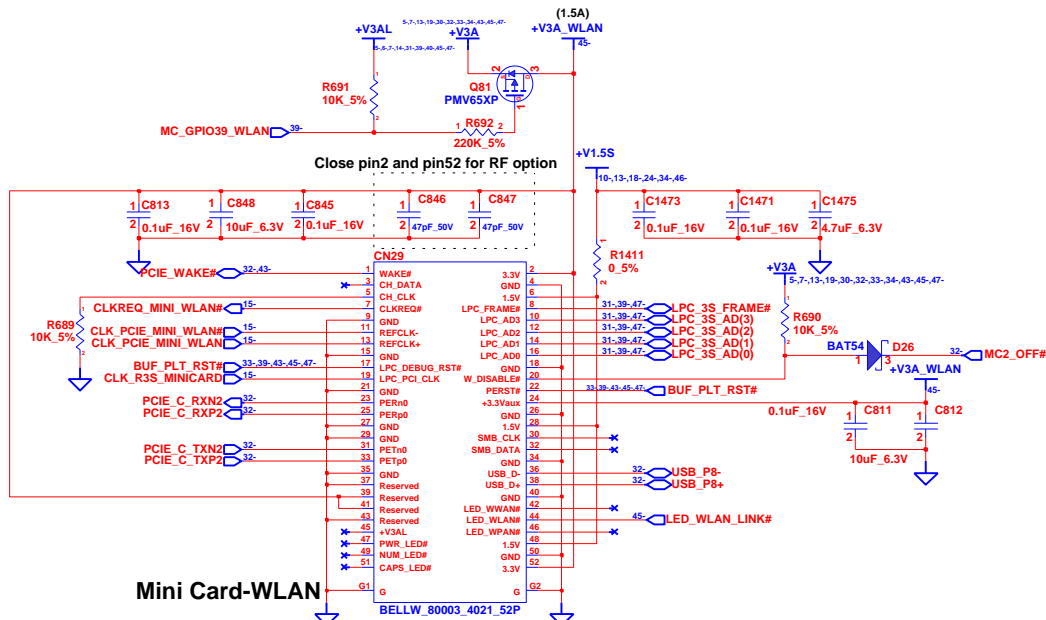
MINI Card-WWAN



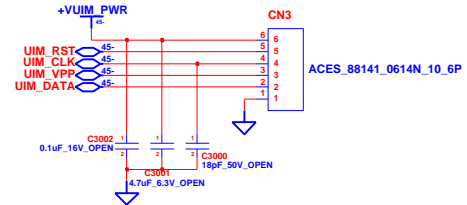
Close pin2 and pin52 for RF option



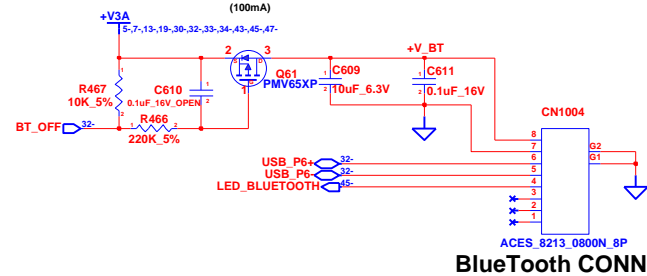
Close pin2 and pin52 for RF option



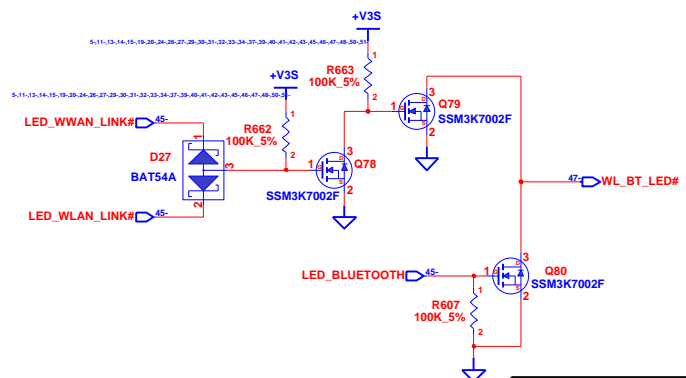
Mini Card-WLAN



SIM Card B2B MB side CONN

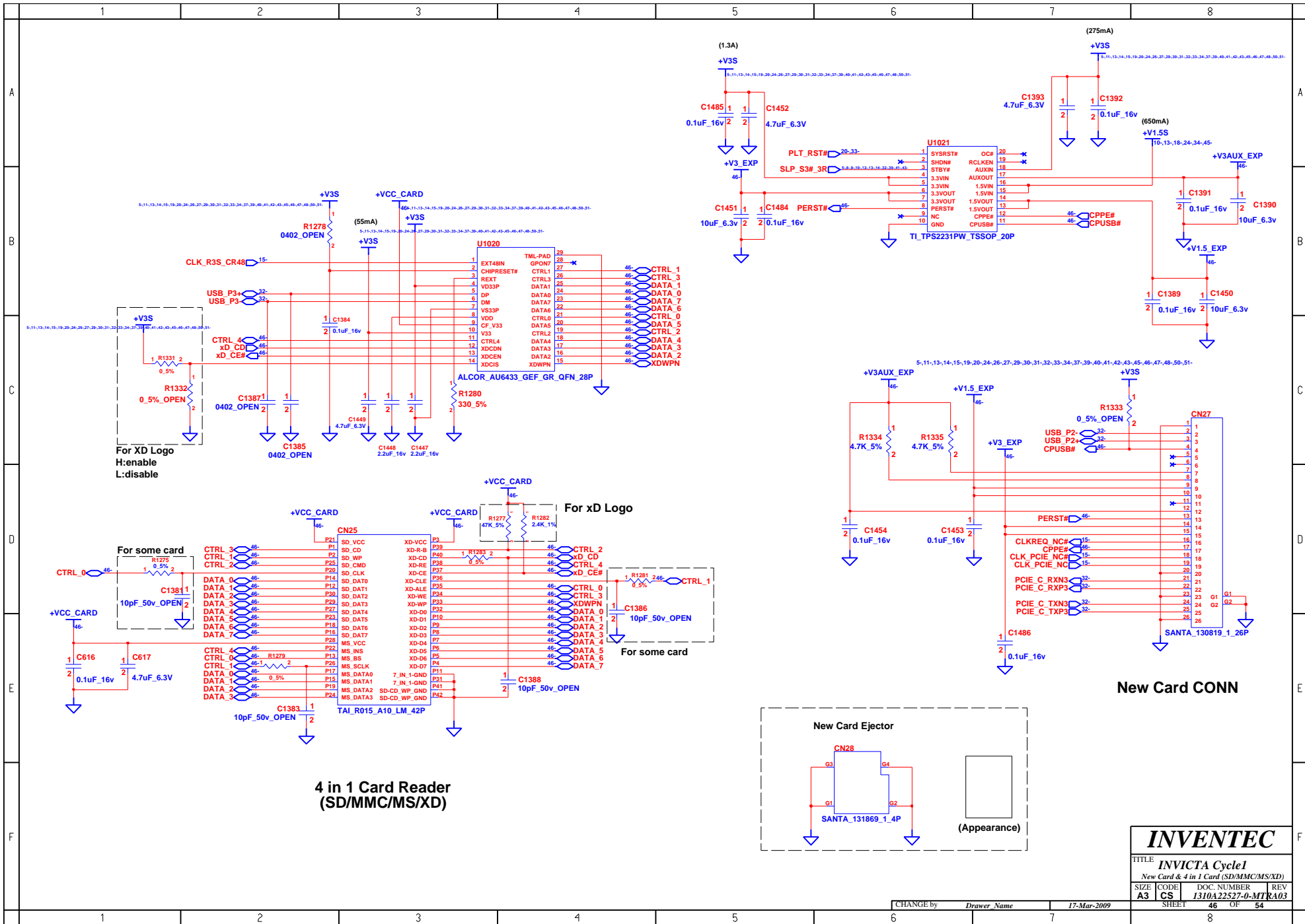


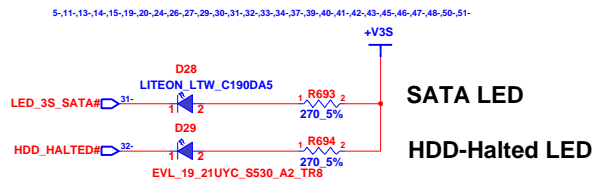
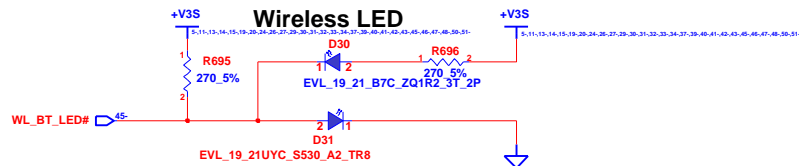
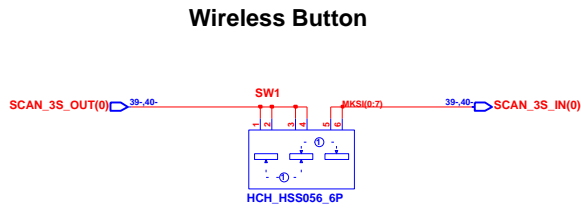
BlueTooth CONN



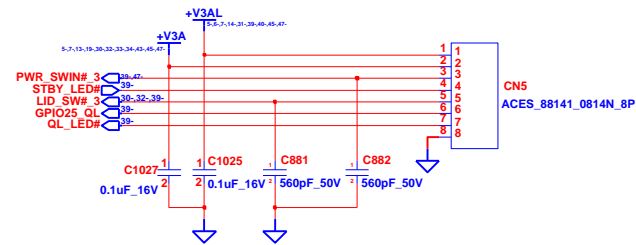
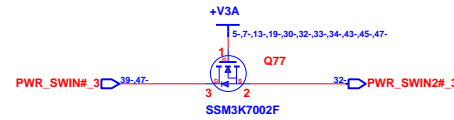
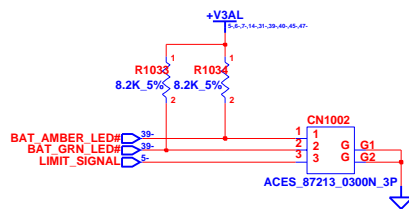
INVENTEC

TITLE: INVICTA Cycle1			
Mini Card (WLAN/WWAN) / BT			
SIZE: A3	CODE: CS	DOC. NUMBER: I310A22527-0-MTR	REV: A03
CHANGE by: <i>Drawer Name</i>		17-Mar-2009	
SHEET: 45		OF: 54	

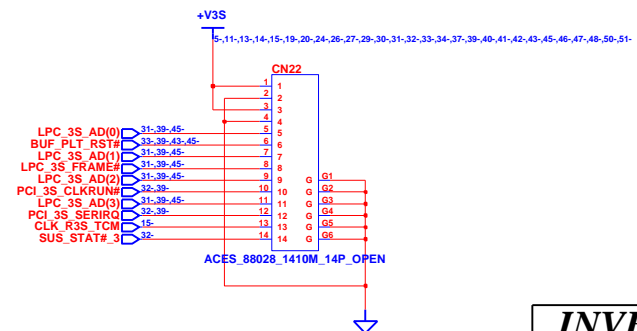




Battery Charge LED CONN



TCM CONN

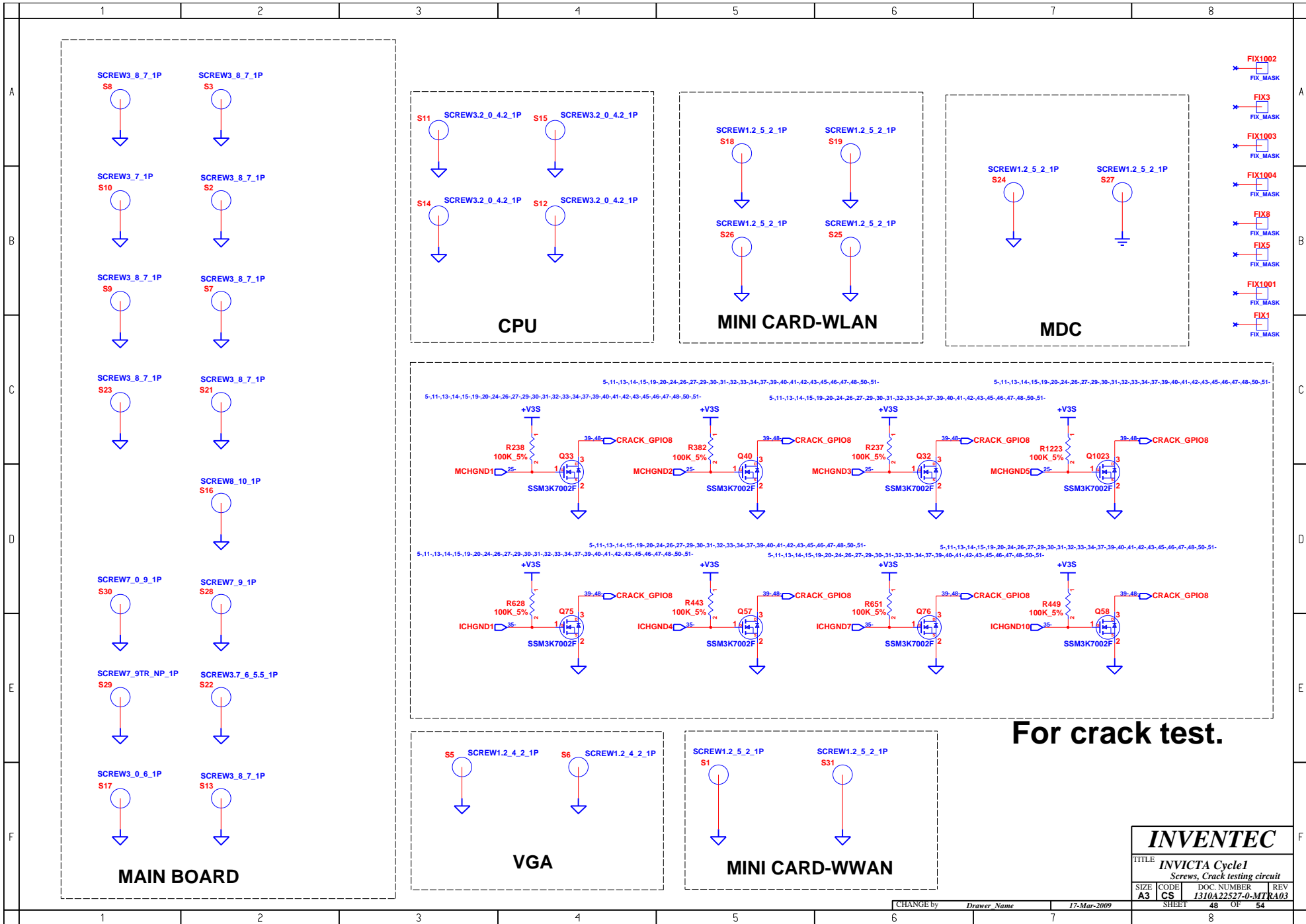


INVENTEC

TITLE			
INVICTA Cycle1			
LEDs & TCM CONN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	I310A22527-0-MTR	A03
CHANGE by		SHEET	
Drawer Name		47 OF 54	

17-Mar-2009

8



For crack test.

INVENTEC			
TITLE <i>INVICTA Cycle1</i>			
Screws, Crack testing circuit			
SIZE A3	CODE CS	DOC NUMBER <i>1310A22527-0-MTR</i>	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
SHEET 48		OF 54	

STRAPS	PIN	Description of default settings	
TX_PWRS_ENB	GPIO0	PCIe full TX output swing.	1
TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enabled.	1
BIF_DEBUG_ACCESS	GPIO4	Debug signals muxed out.	0
ROMIDCFG(0:3)	GPIO[11:13,9]	Memory aperture type	X X X X

X = DESIGN DEPENDANT
0 = DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR

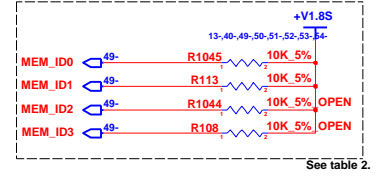
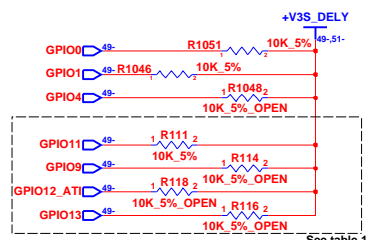
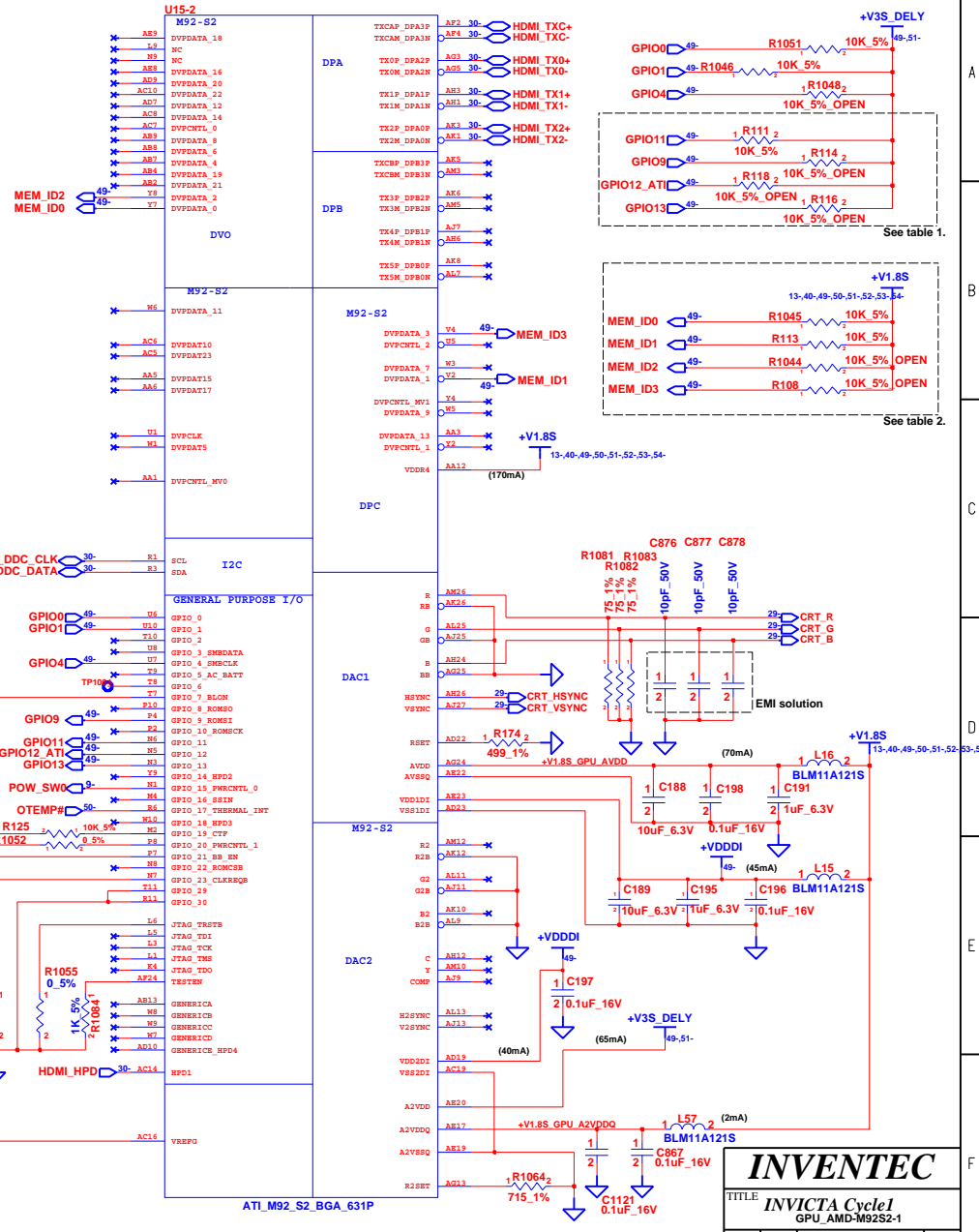
Table 1

GPIO_13	GPIO_12	GPIO_11	For DIS-GDDR2
0	0	1	512MB/256MB memory aperture (Default)
1	1	0	reserved

POW_SW1	POW_SW0	+VDD_CORE
0	0	1.0V
0	1	0.95V
1	0	0.9V

Table 2

For DIS-VRAM DDR2				
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	vendor
0	0	0	1	Samsung (512MB)
0	0	1	0	Qimonda (512MB)
0	0	1	1	Hynix (512MB) (Default)

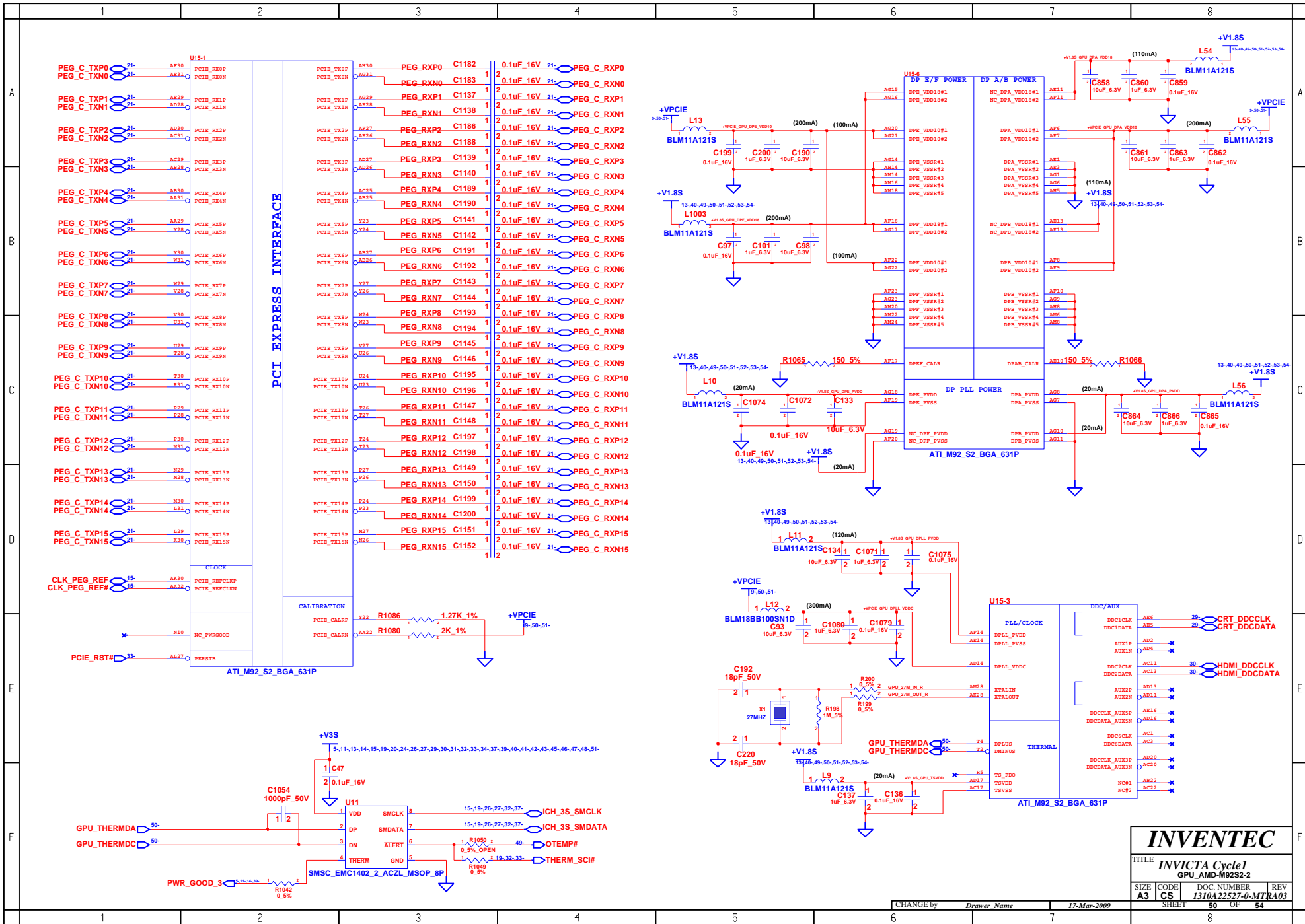


INVENTEC

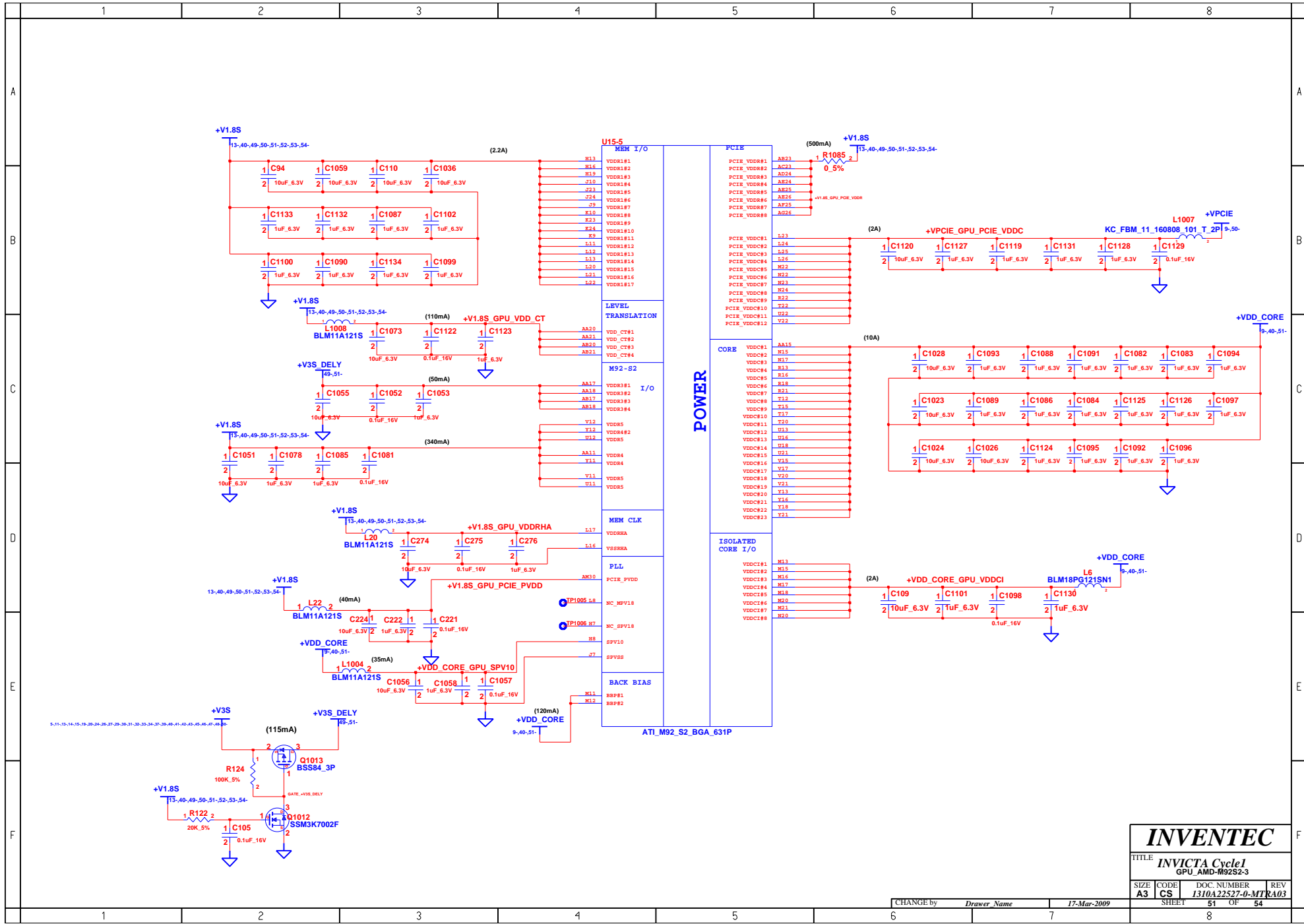
TITLE: **INVICTA Cycle1 GPU_AMD-M92S2-1**

SIZE: **A3** CODE: **CS** DOC. NUMBER: **I310A22527-0-MTR** REV: **A03**

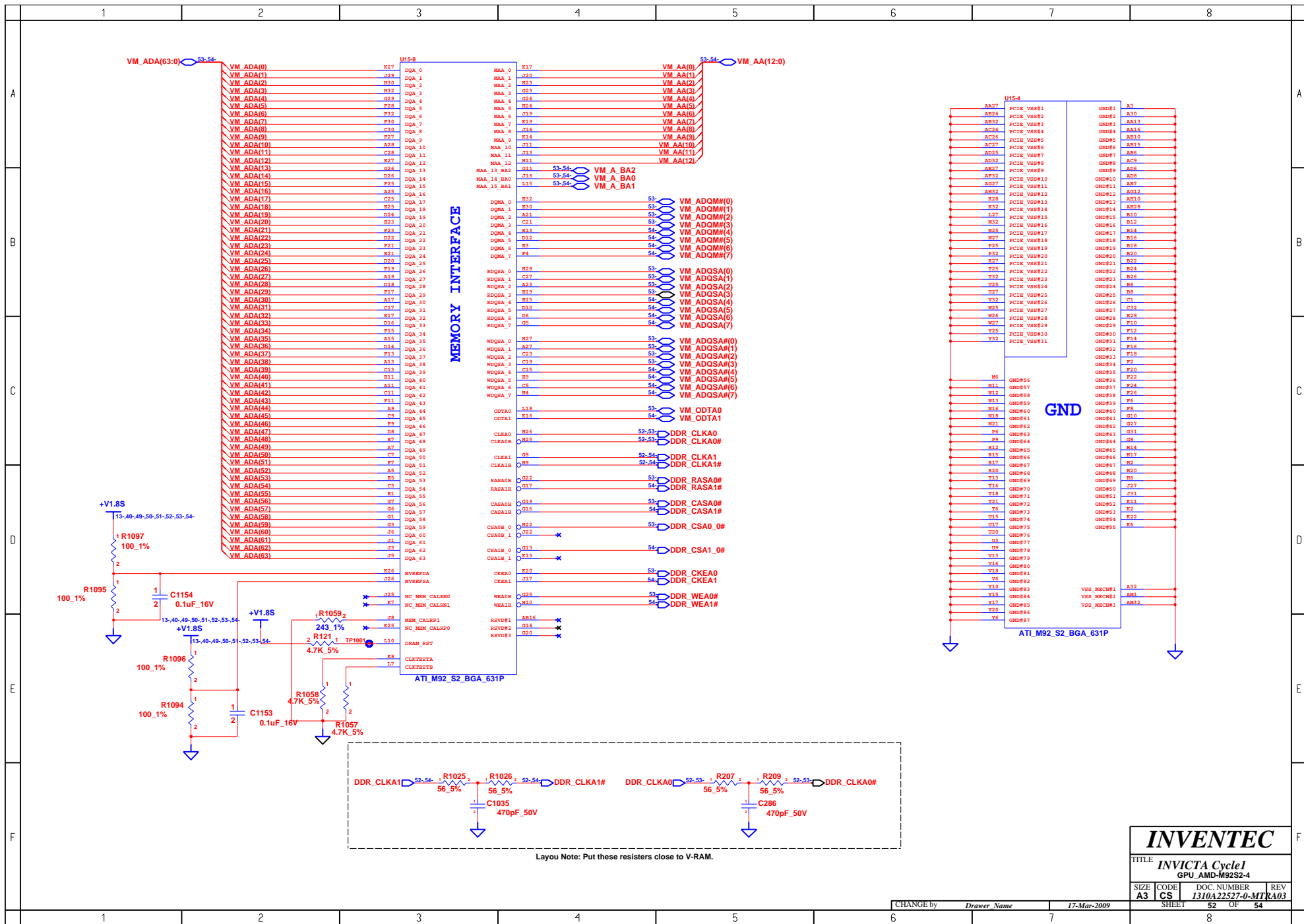
SHEET: **49** OF: **54**



INVENTEC			
TITLE INVICTA Cycle1 GPU_AMD-M92S2-2			
SIZE A3	CODE CS	DOC NUMBER I310A2327-0-MTR	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
SHEET 50		OF 54	

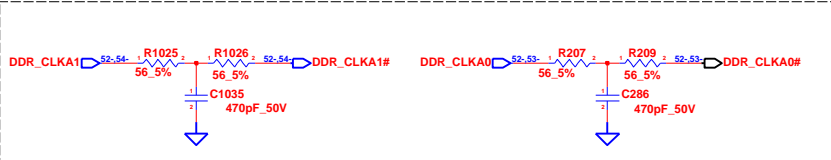


INVENTEC			
TITLE: INVICTA Cycle1 GPU_AMD-M92S2-3			
SIZE: A3	CODE: CS	DOC. NUMBER: I310A22527-0-MTR	REV: A03
CHANGE by: Drawer Name		17-Mar-2009	
SHEET: 51		OF: 54	

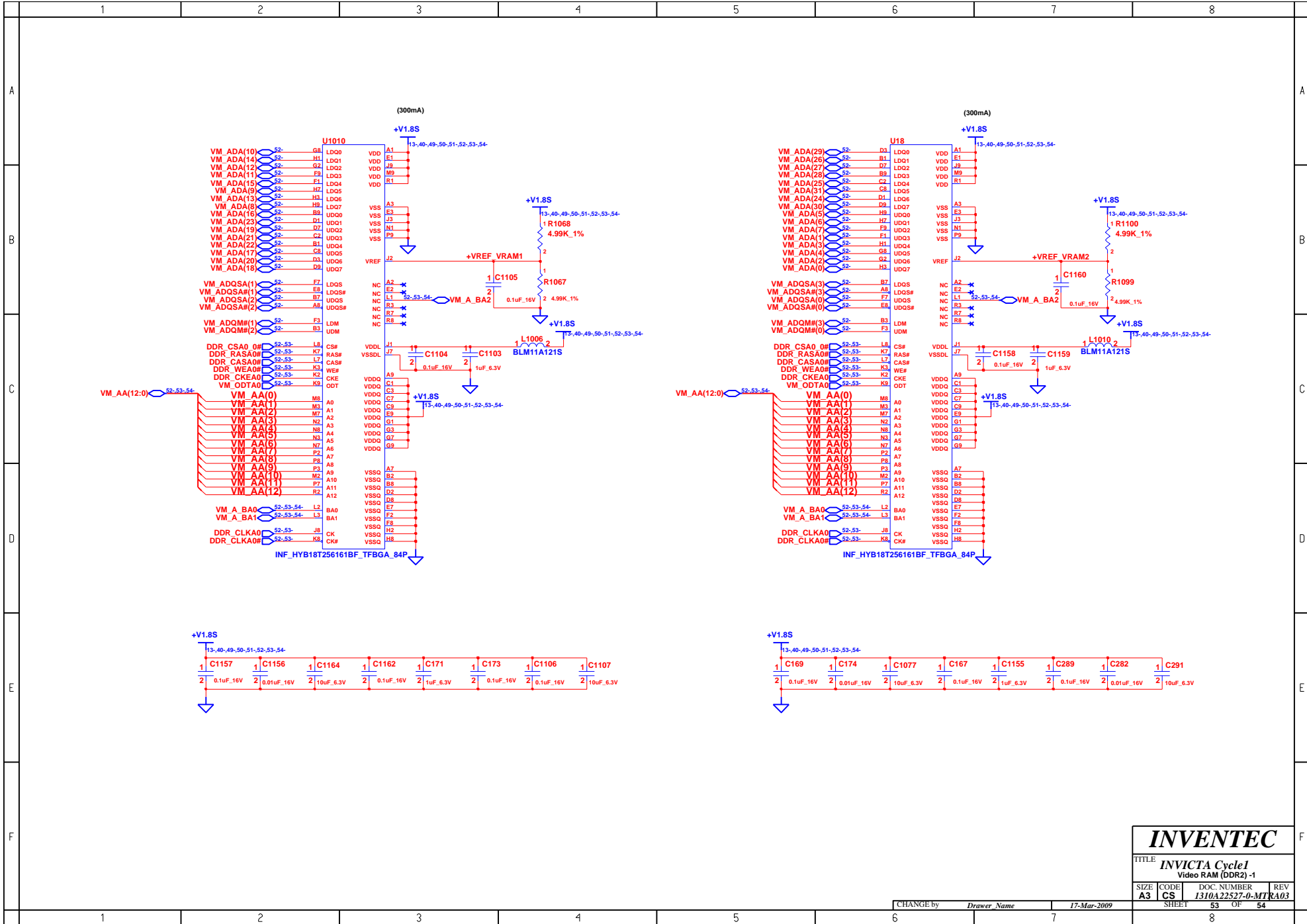


MEMORY INTERFACE

GND



INVENTEC			
TITLE: INVICTA Cycle1 GPU_AMD-M92S2-4			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
SHEET		52	OF 54



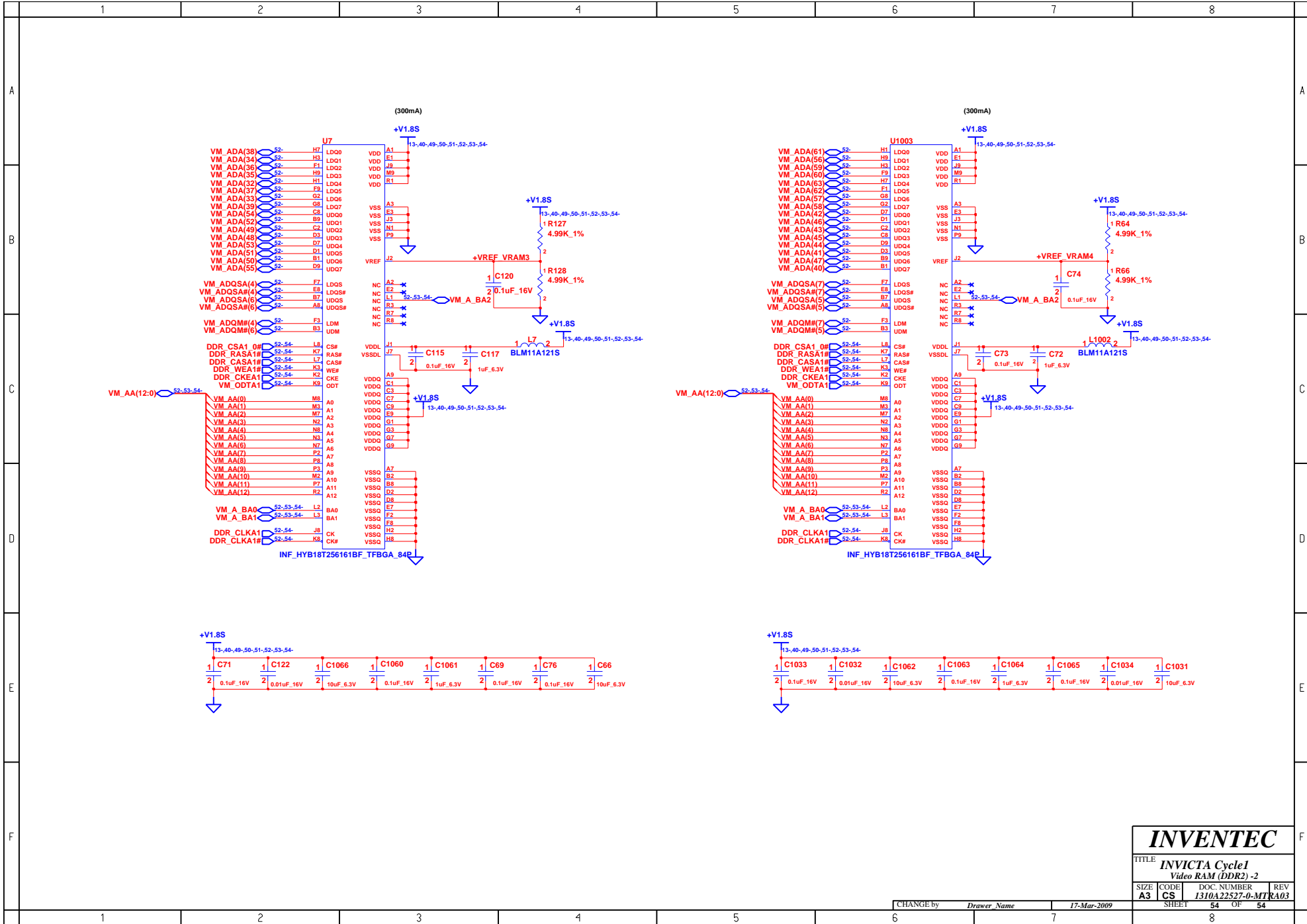
INVENTEC

TITLE: **INVICTA Cycle1**
Video RAM (DDR2) -1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03

CHANGE by: *Drawer Name* 17-Mar-2009

SHEET 53 OF 54



INVENTEC			
TITLE INVICTA Cycle1 Video RAM (DDR2) -2			
SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MTR	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
SHEET 54		OF 54	