

DatashareDirectory

# S-SERIES

## Zygo(D) & Zodiac(D) & Ikon

### PV\_Build (A01)

2008.04.02

DATE	CHANGE NO.	REV

DRAWN	EE	DATE	POWER	DATE	<b>INVENTEC</b> TITLE <i>S-SERIES - Discrete</i>
DESIGN					
CHECK					
RESPONSIBLE					
SIZE =	3	VER :			SIZE CODE DOC. NUMBER REV
FILE NAME :	XXXX-XXXXXX-XX				<b>A3 CS 1310A21614 A01</b>
P/N	XXXXXXXXXXXX				SHEET 1 OF 54

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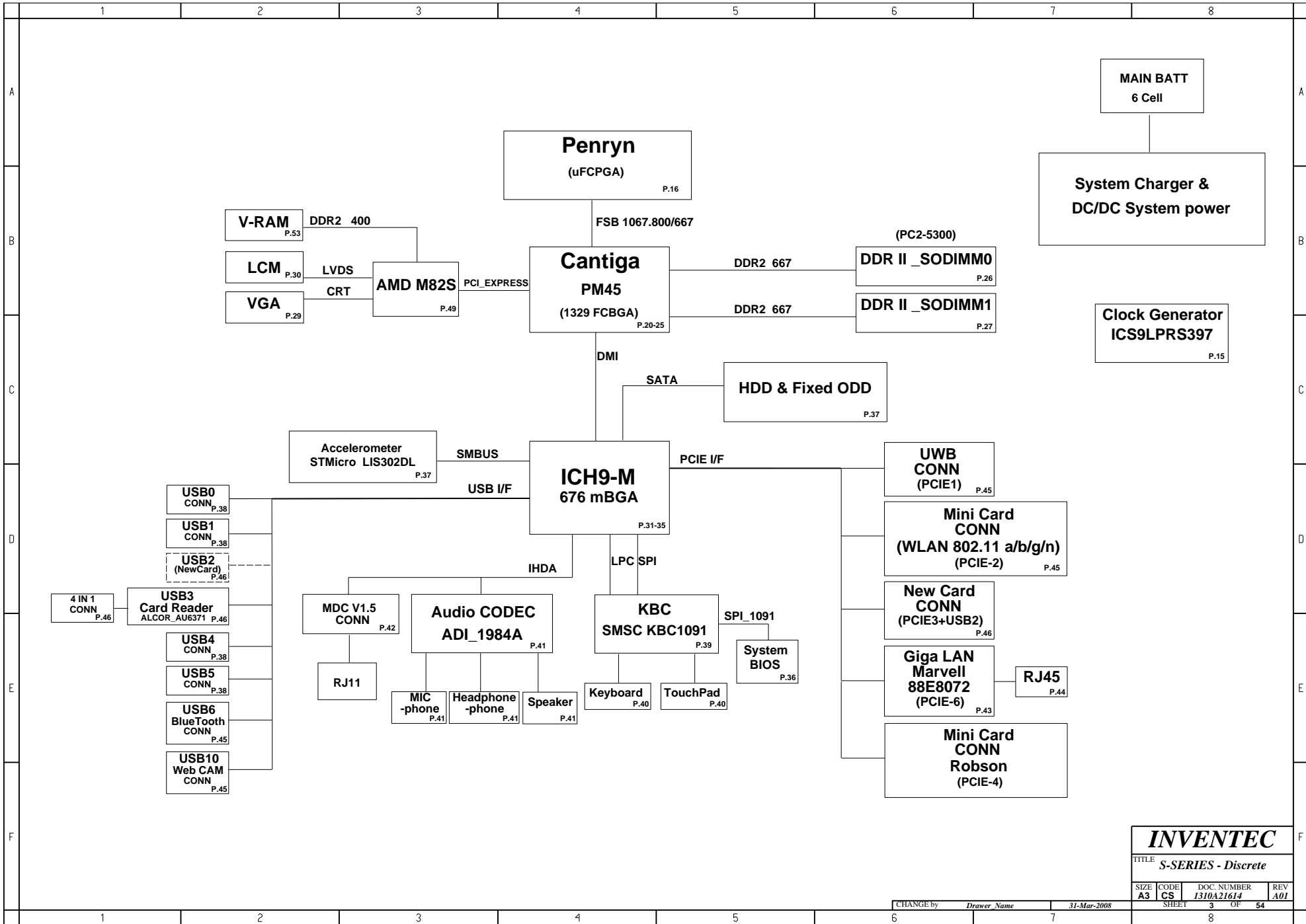
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TITLE *S-SERIES - Discrete*

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
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CHANGE by *Drawer Name*      31-Mar-2008

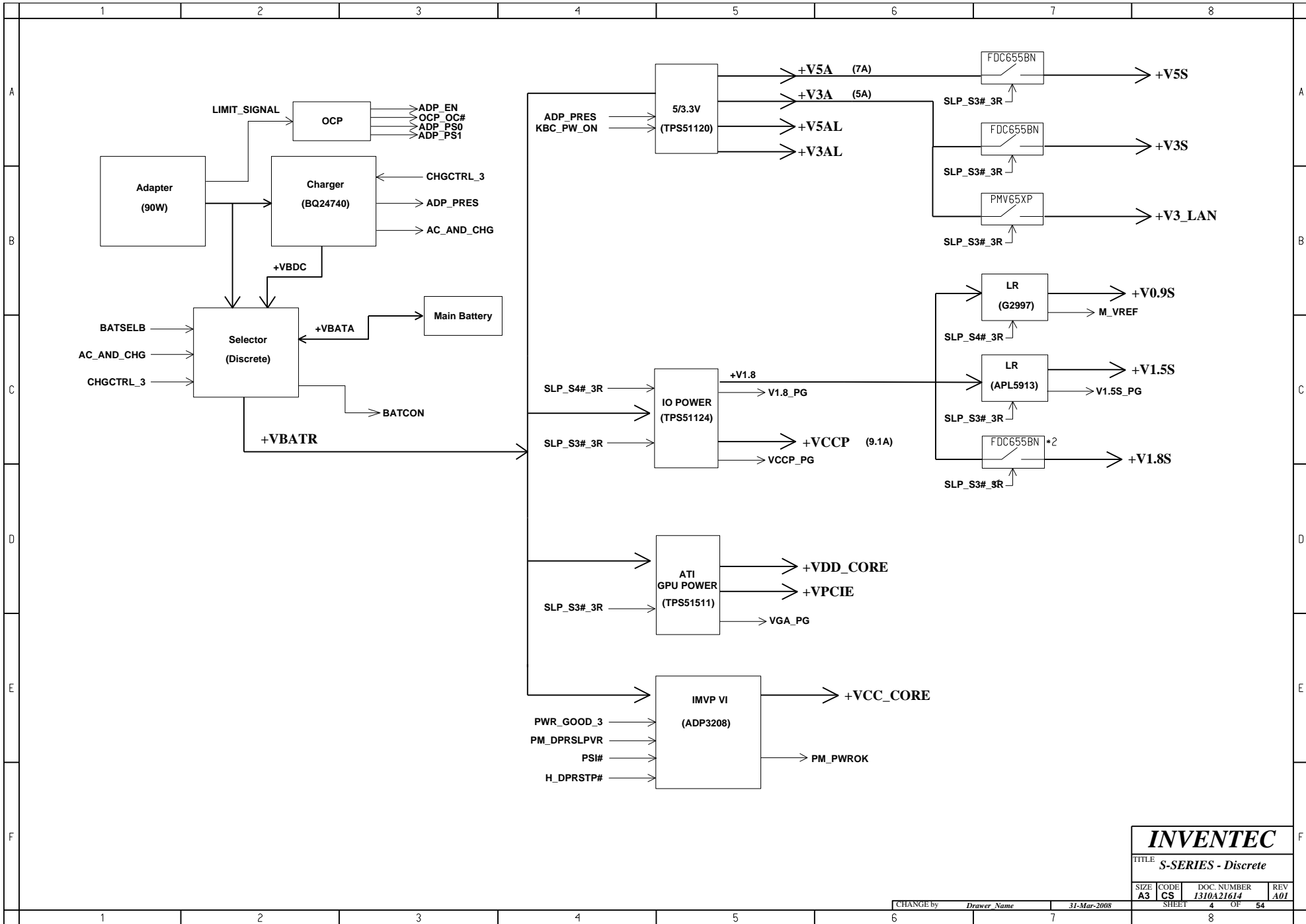
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**INVENTEC**

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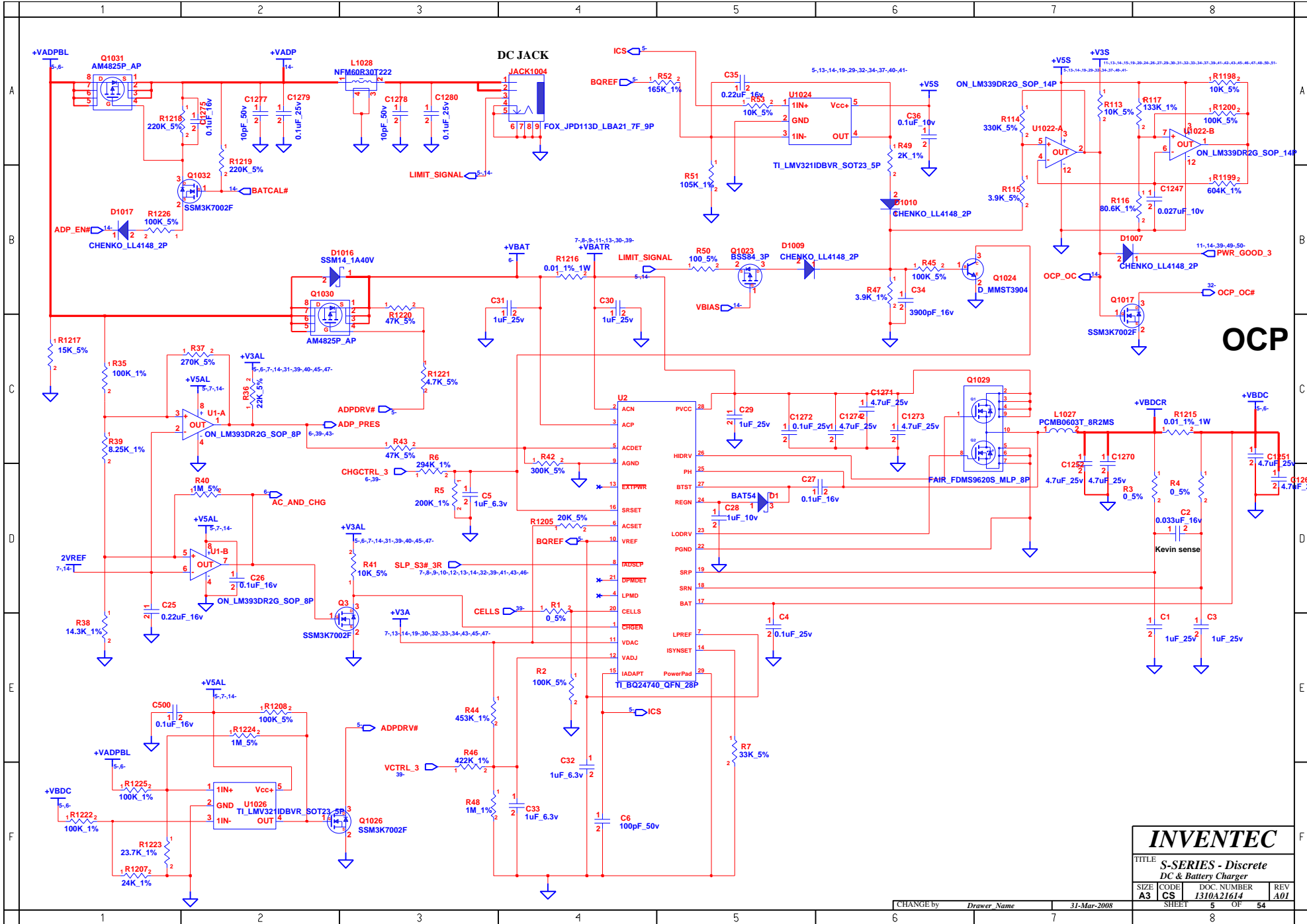
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A3	CS	1310A21614	A01



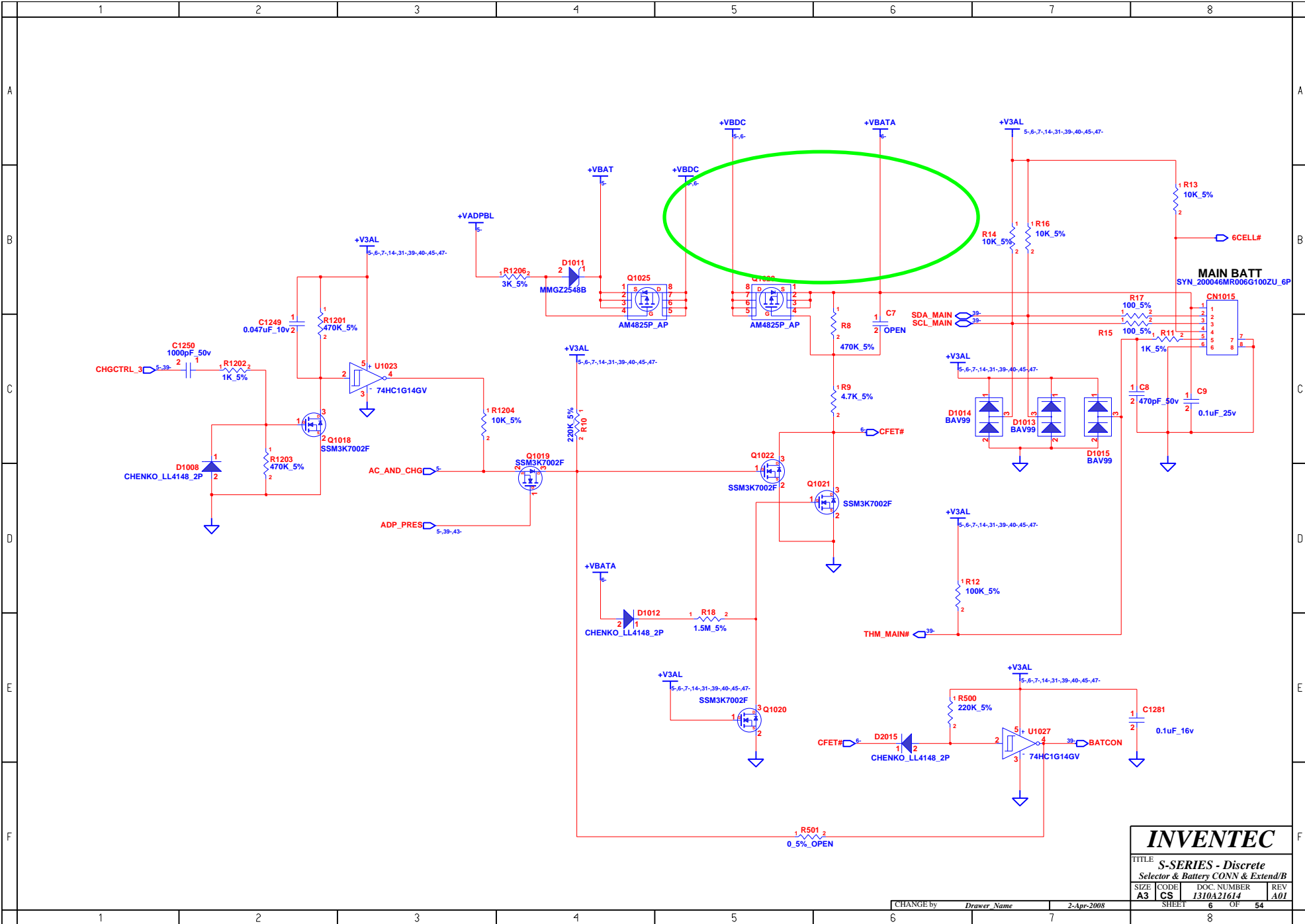
**INVENTEC**

TITLE **S-SERIES - Discrete**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01



<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete DC &amp; Battery Charger</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>I310A21614</b>	REV <b>A01</b>
CHANGE by <i>Drawer Name</i>		31-Mar-2008	
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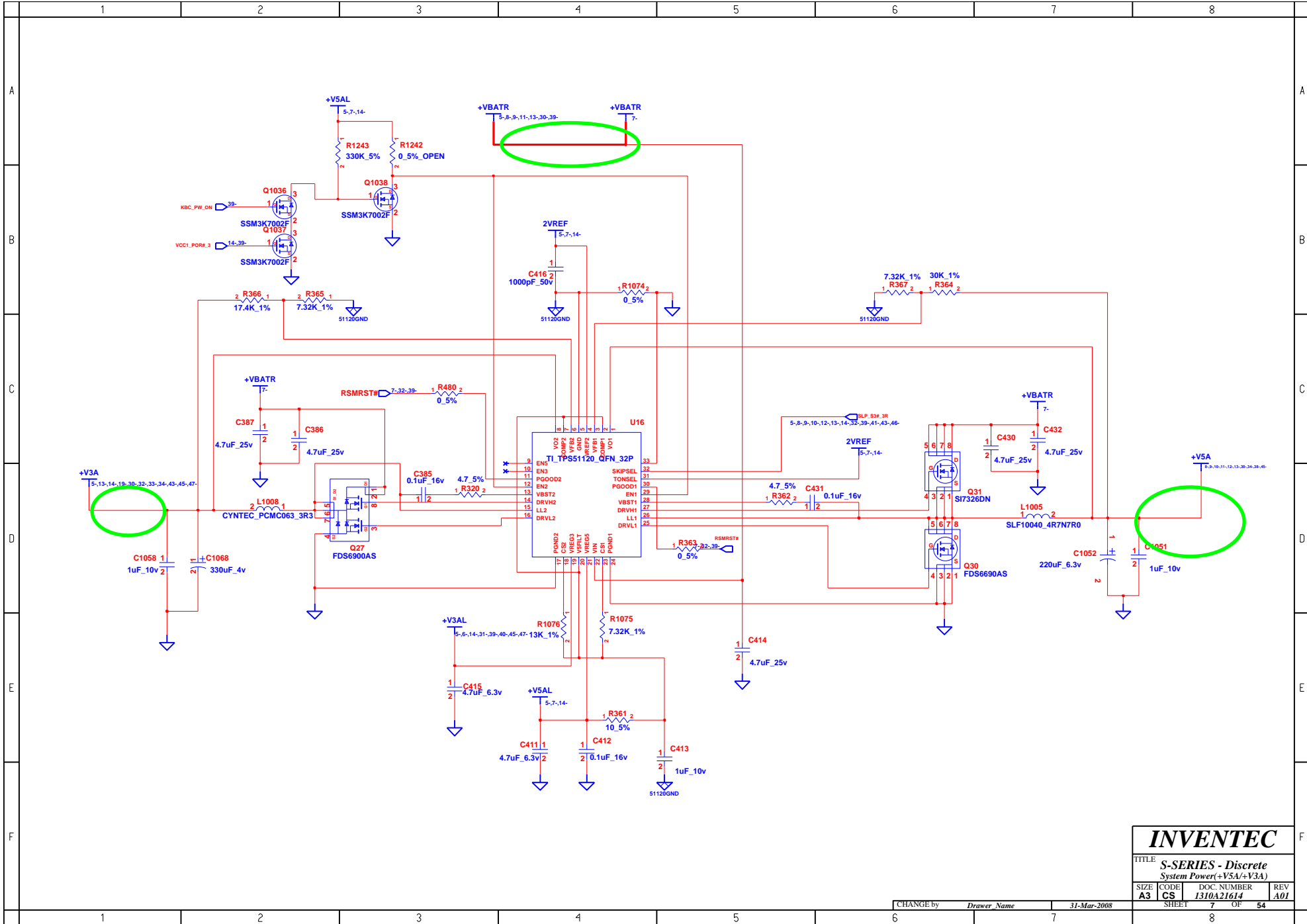


**INVENTEC**

TITLE  
**S-SERIES - Discrete**  
 Selector & Battery CONN & Extend/B

SIZE	CODE	DOC NUMBER	REV
A3	CS	I310A21614	A01

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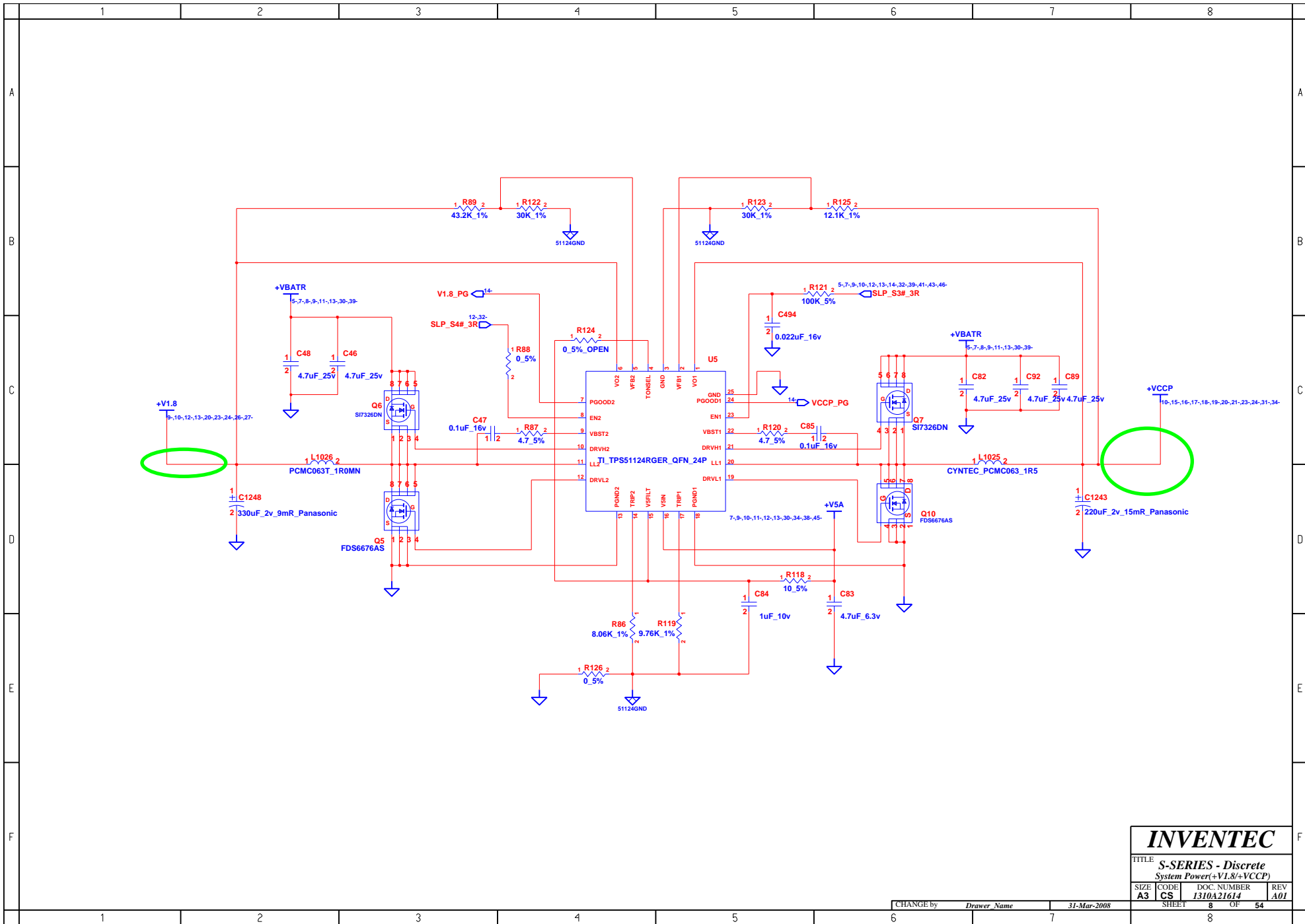
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TITLE  
**S-SERIES - Discrete**  
 System Power(+VSA/+V3A)

SIZE	CODE	DOC. NUMBER	REV
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CHANGE by *Drawer Name* 31-Mar-2008

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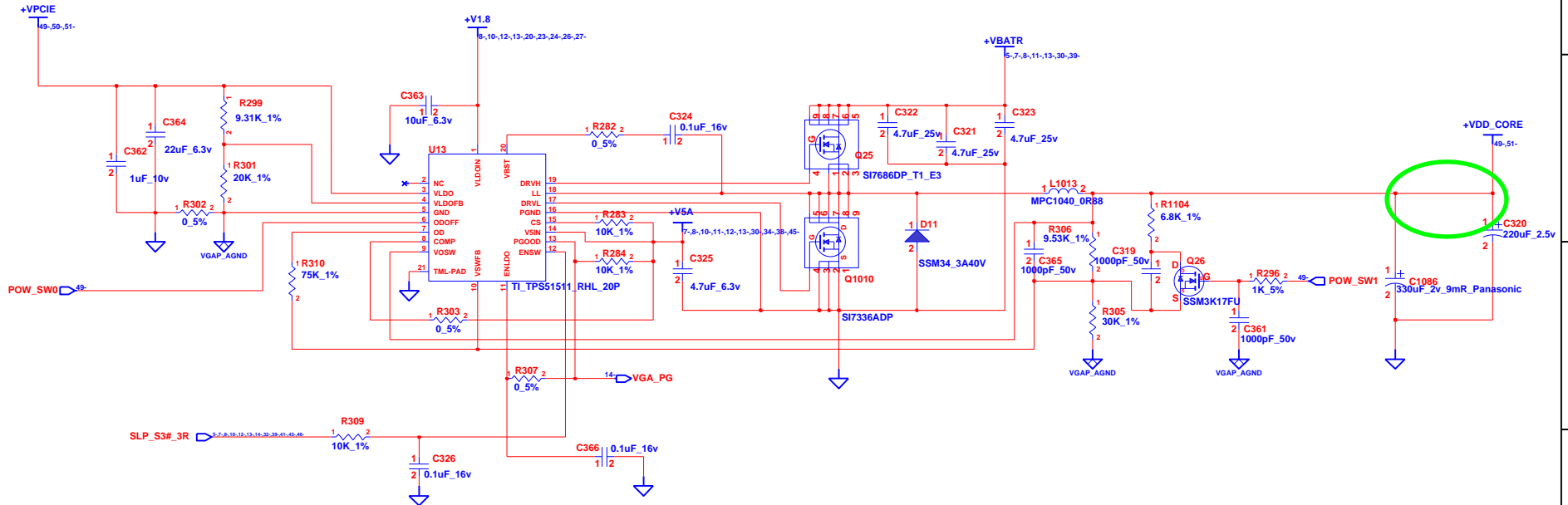
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TITLE  
**S-SERIES - Discrete**  
 System Power(+V1.8/+VCCP)

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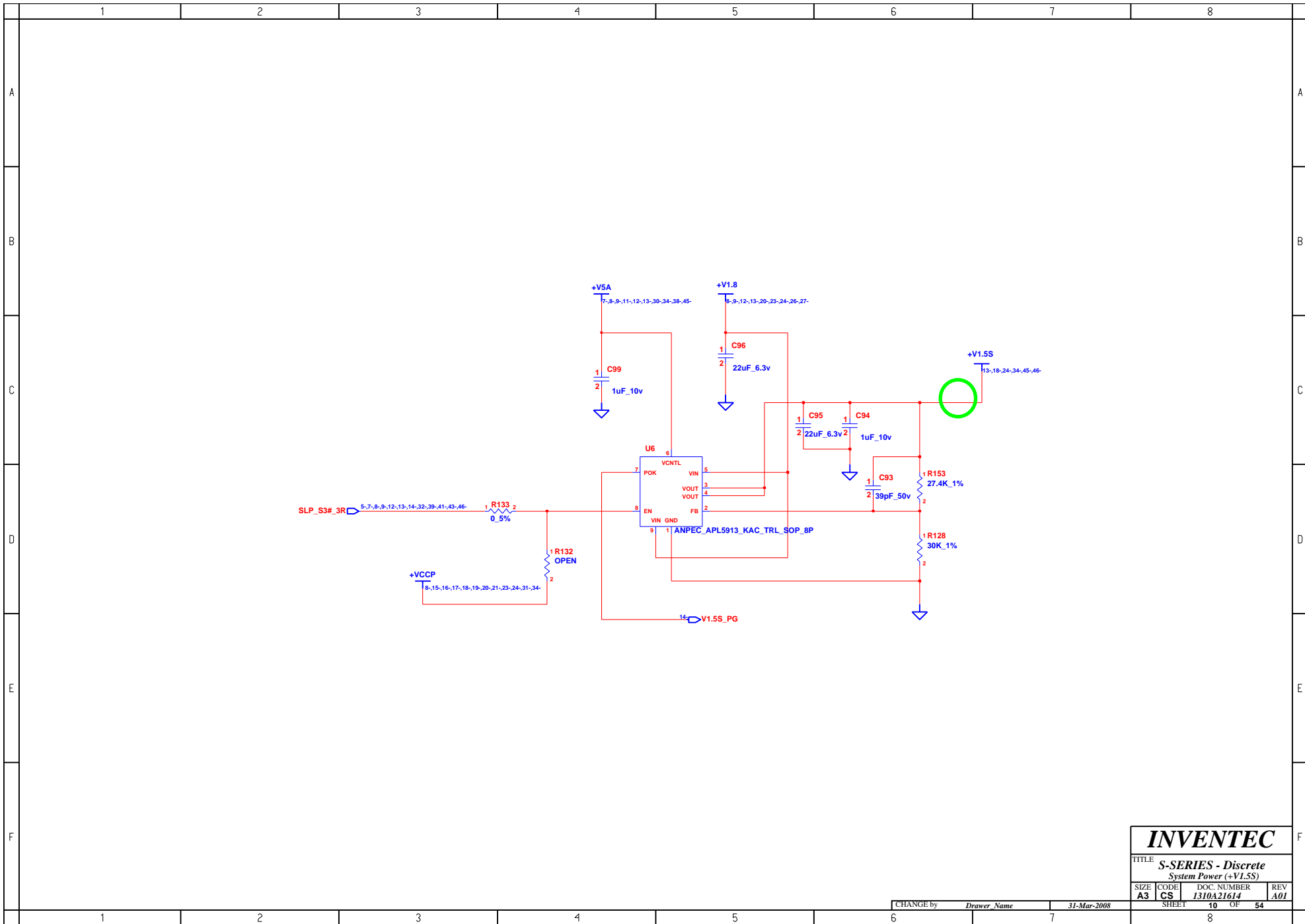
POW_SW1	POW_SW0	+VDD_CORE
0	0	1.1V
0	1	1.0V
1	0	0.9V



**INVENTEC**  
 TITLE: **S-SERIES - Discrete**  
 Graphic Power (+VDD\_CORE & +VPCIE)

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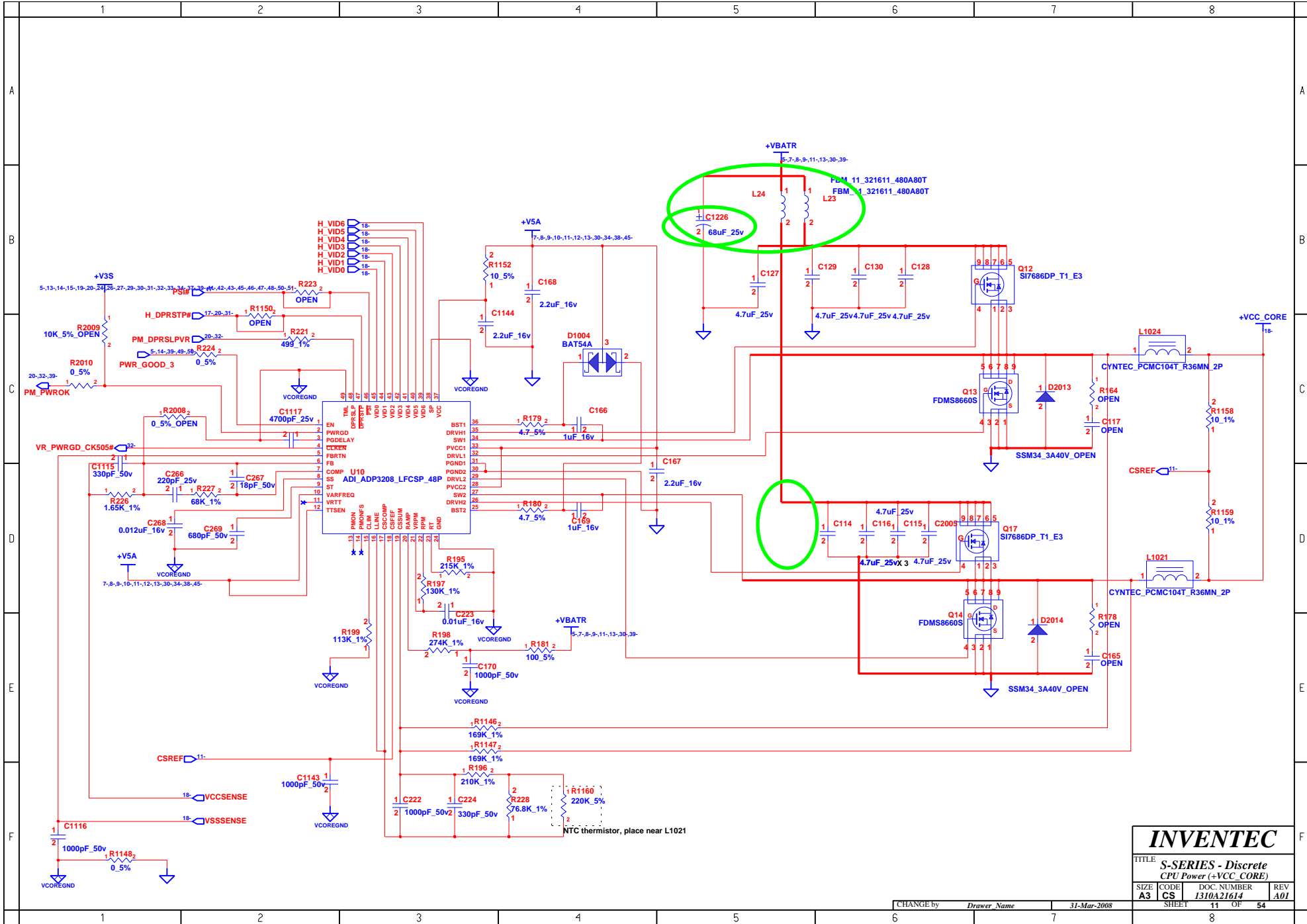
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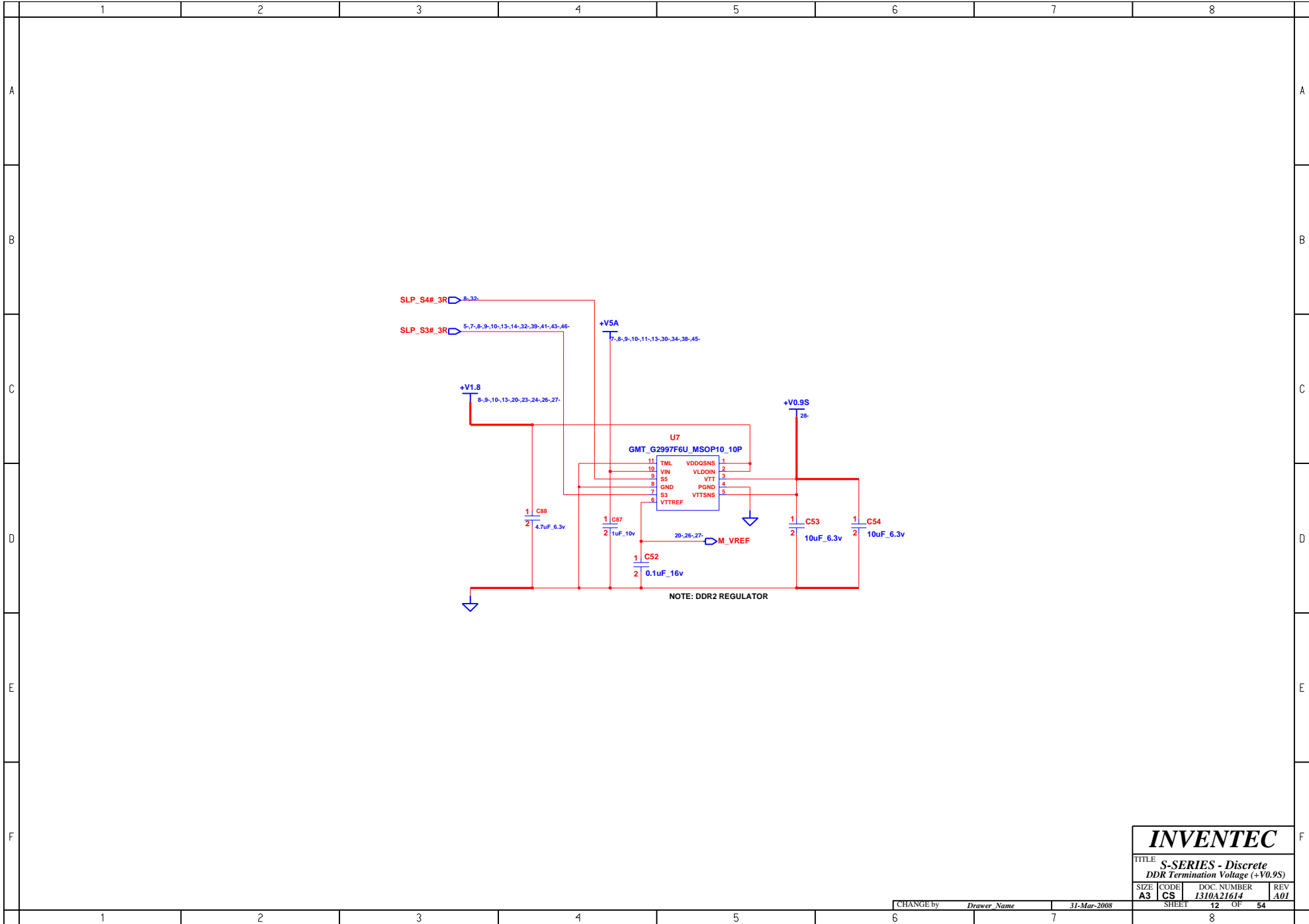
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TITLE  
**S-SERIES - Discrete**  
 System Power (+V1.5S)

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
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<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete CPU Power (+VCC_CORE)</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>I310A21614</b>	REV <b>A01</b>
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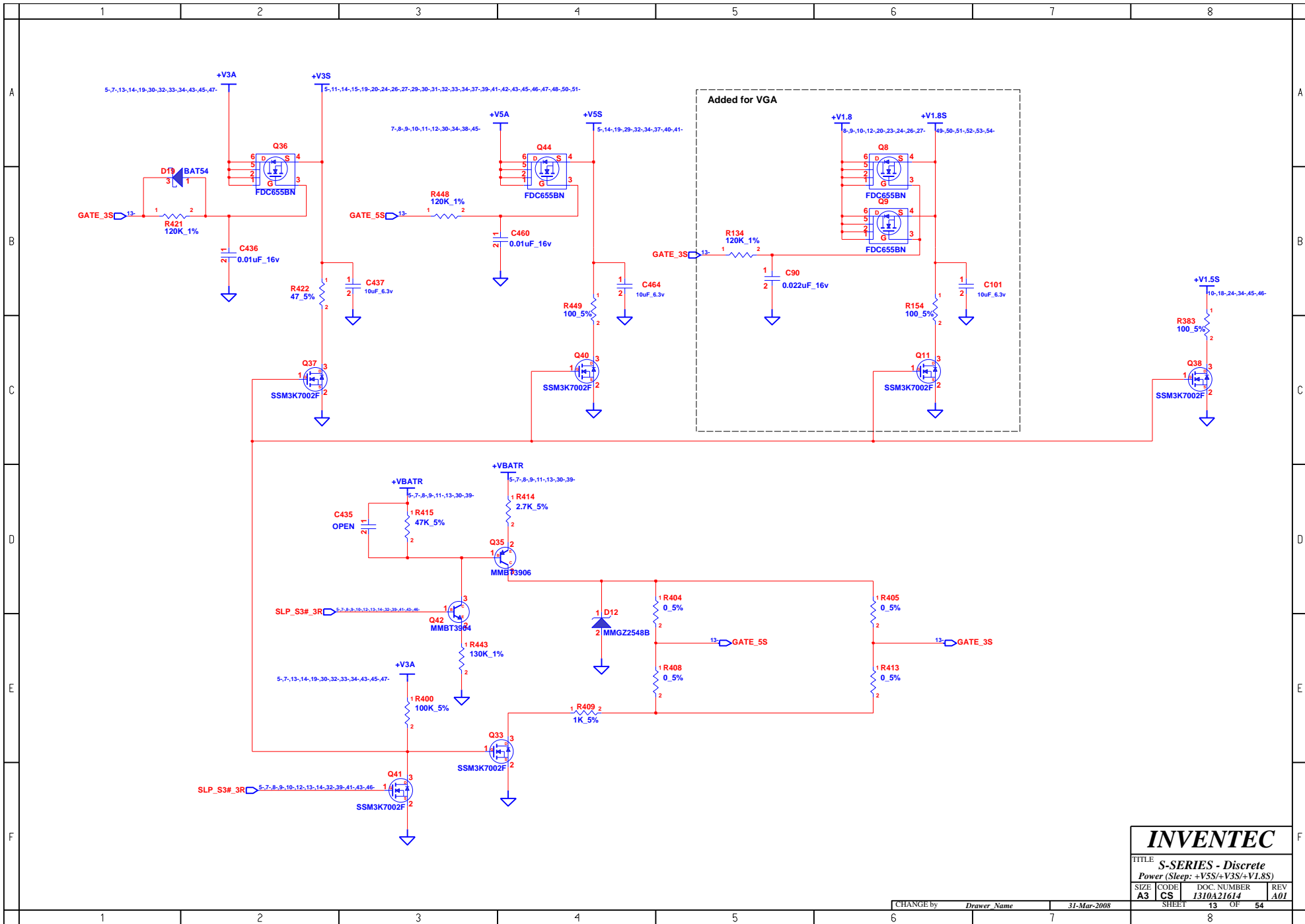


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TITLE **S-SERIES - Discrete**  
**DDR Termination Voltage (+V0.9S)**

SIZE	CODE	DOC. NUMBER	REV
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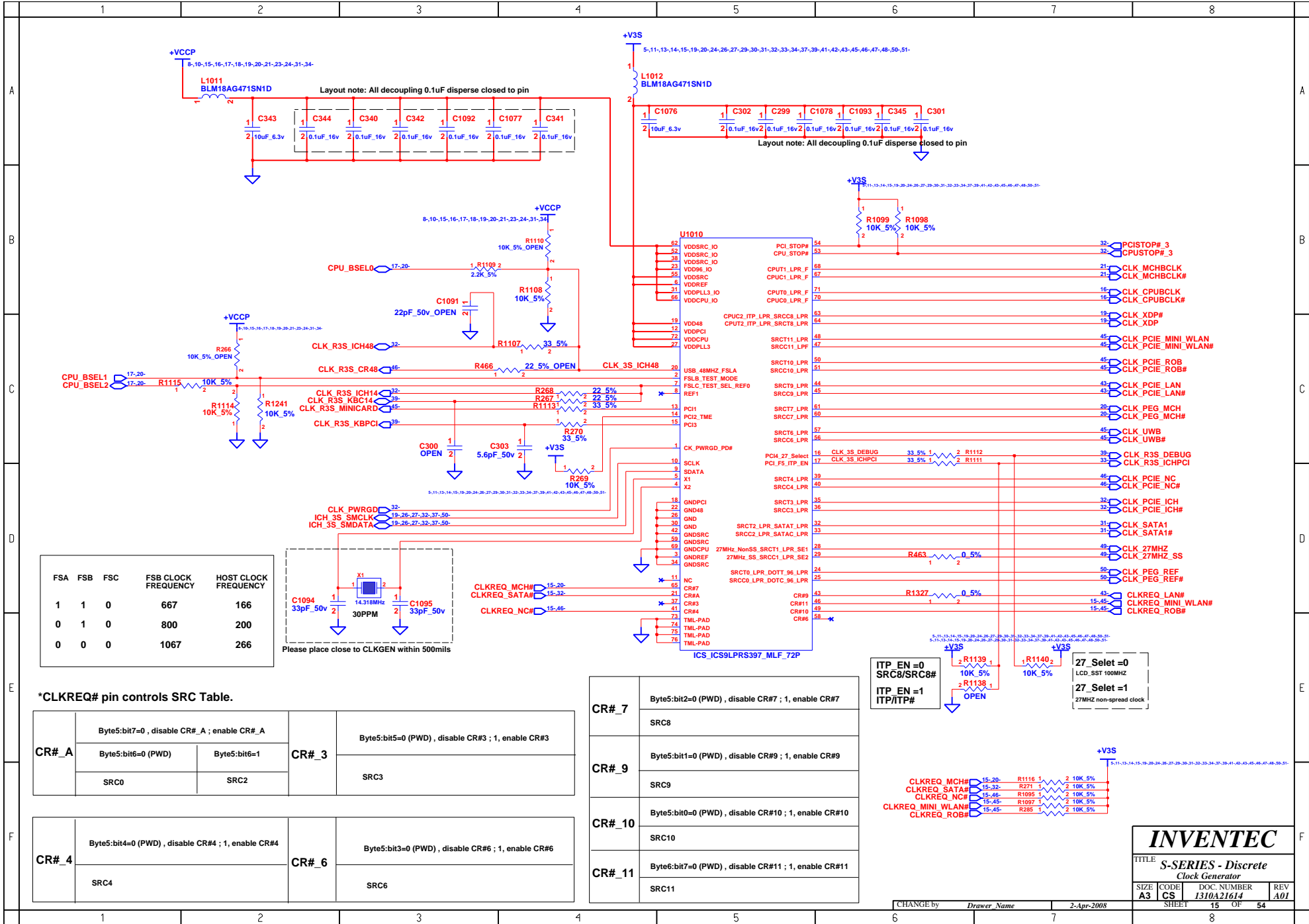
TITLE  
**S-SERIES - Discrete**  
 Power (Sleep: +V5S/+V3S/+V1.8S)

SIZE <b>A3</b>	CODE <b>CS</b>	DOC NUMBER <b>I310A21614</b>	REV <b>A01</b>
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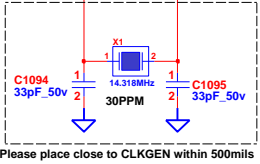
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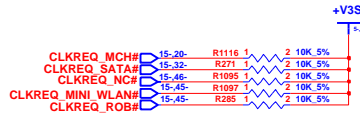
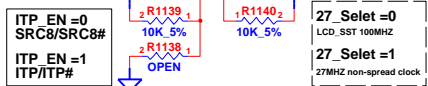
FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266



\*CLKREQ# pin controls SRC Table.

CR#_A	Byte5:bit7=0 (PWD), disable CR#_A ; enable CR#_A	Byte5:bit6=0 (PWD)	Byte5:bit6=1	CR#_3	Byte5:bit5=0 (PWD), disable CR#3 ; 1, enable CR#3
		SRC0			SRC3
CR#_4	Byte5:bit4=0 (PWD), disable CR#4 ; 1, enable CR#4			CR#_6	Byte5:bit3=0 (PWD), disable CR#6 ; 1, enable CR#6
		SRC4			SRC6

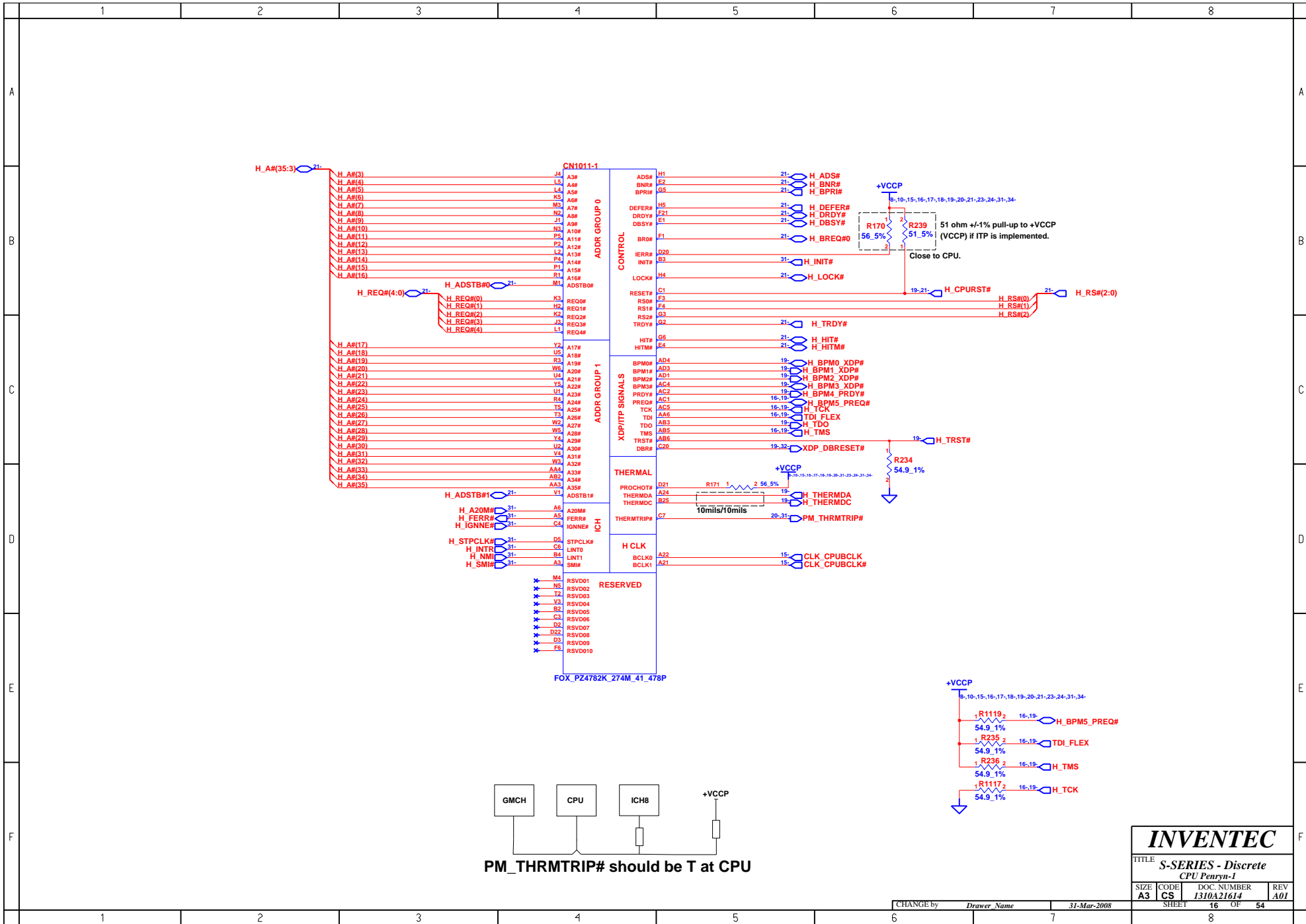
CR#_7	Byte5:bit2=0 (PWD), disable CR#7 ; 1, enable CR#7
	SRC8
CR#_9	Byte5:bit1=0 (PWD), disable CR#9 ; 1, enable CR#9
	SRC9
CR#_10	Byte5:bit0=0 (PWD), disable CR#10 ; 1, enable CR#10
	SRC10
CR#_11	Byte6:bit7=0 (PWD), disable CR#11 ; 1, enable CR#11
	SRC11



**INVENTEC**

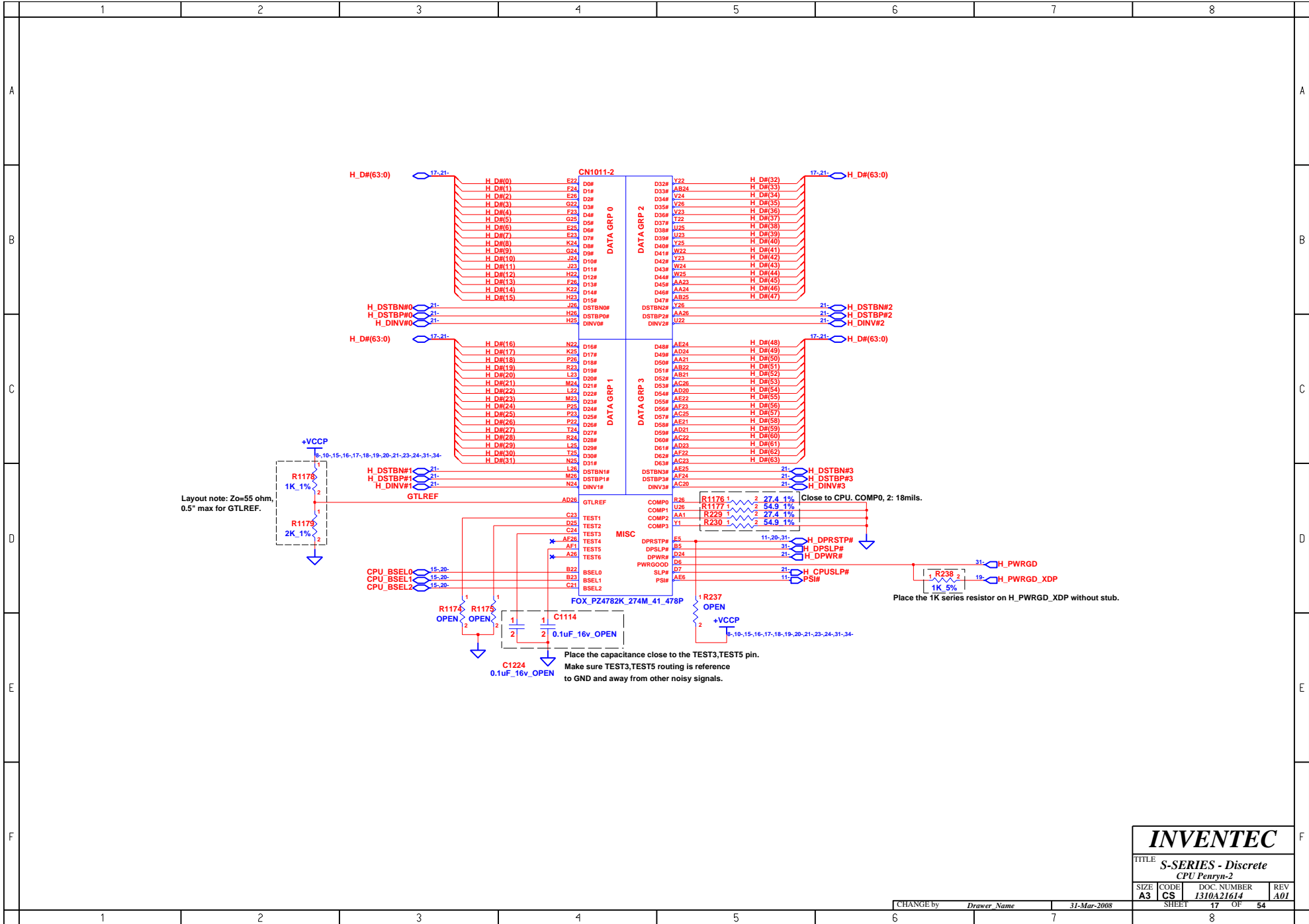
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**S-SERIES - Discrete**  
Clock Generator

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A21614	A01



<b>INVENTEC</b>			
TITLE <i>S-SERIES - Discrete</i>			
CPU Penryn-1			
SIZE	CODE	DOC. NUMBER	REV
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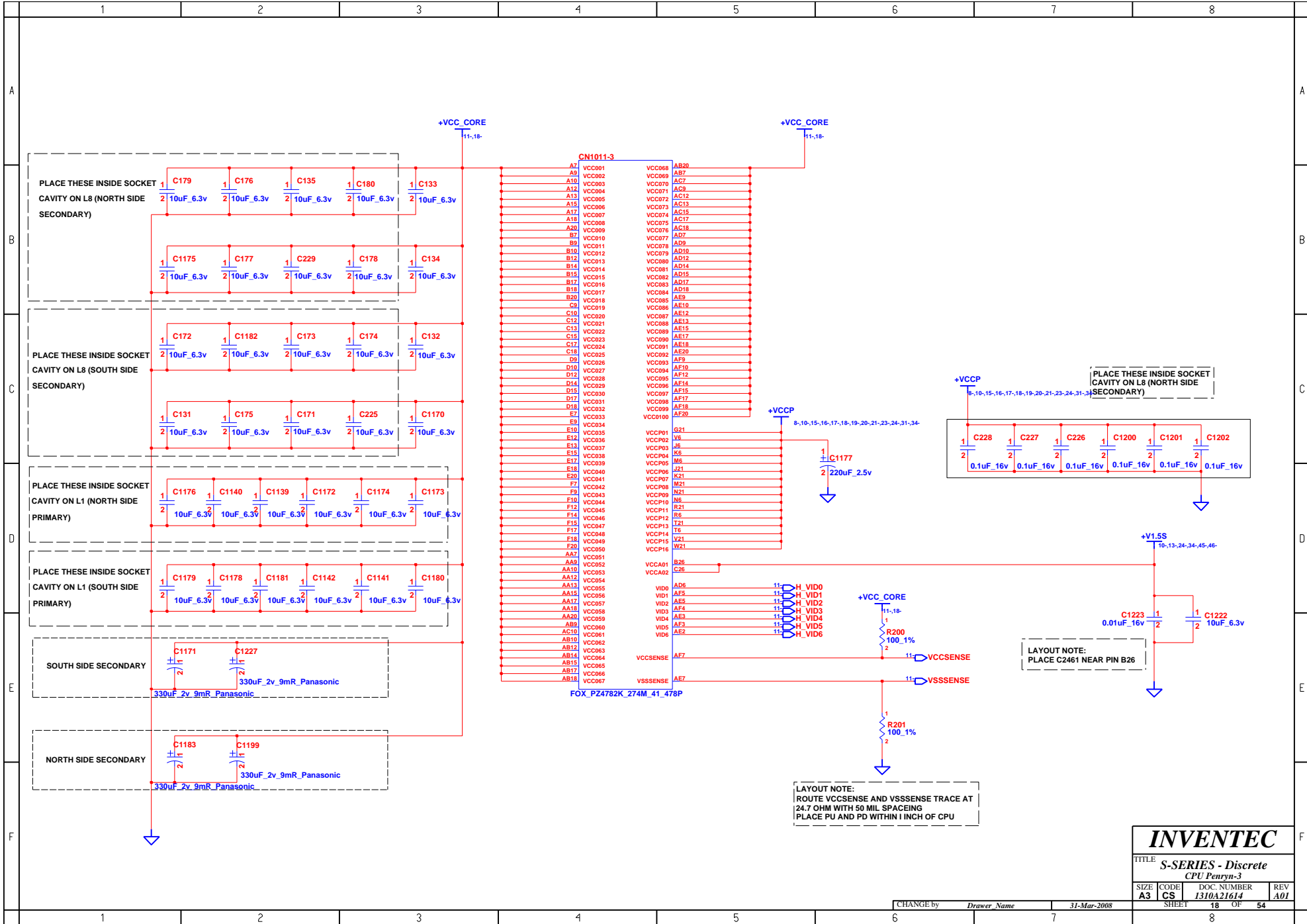
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TITLE  
**S-SERIES - Discrete**  
 CPU Penryn-2

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
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CHANGE by *Drawer Name* 31-Mar-2008

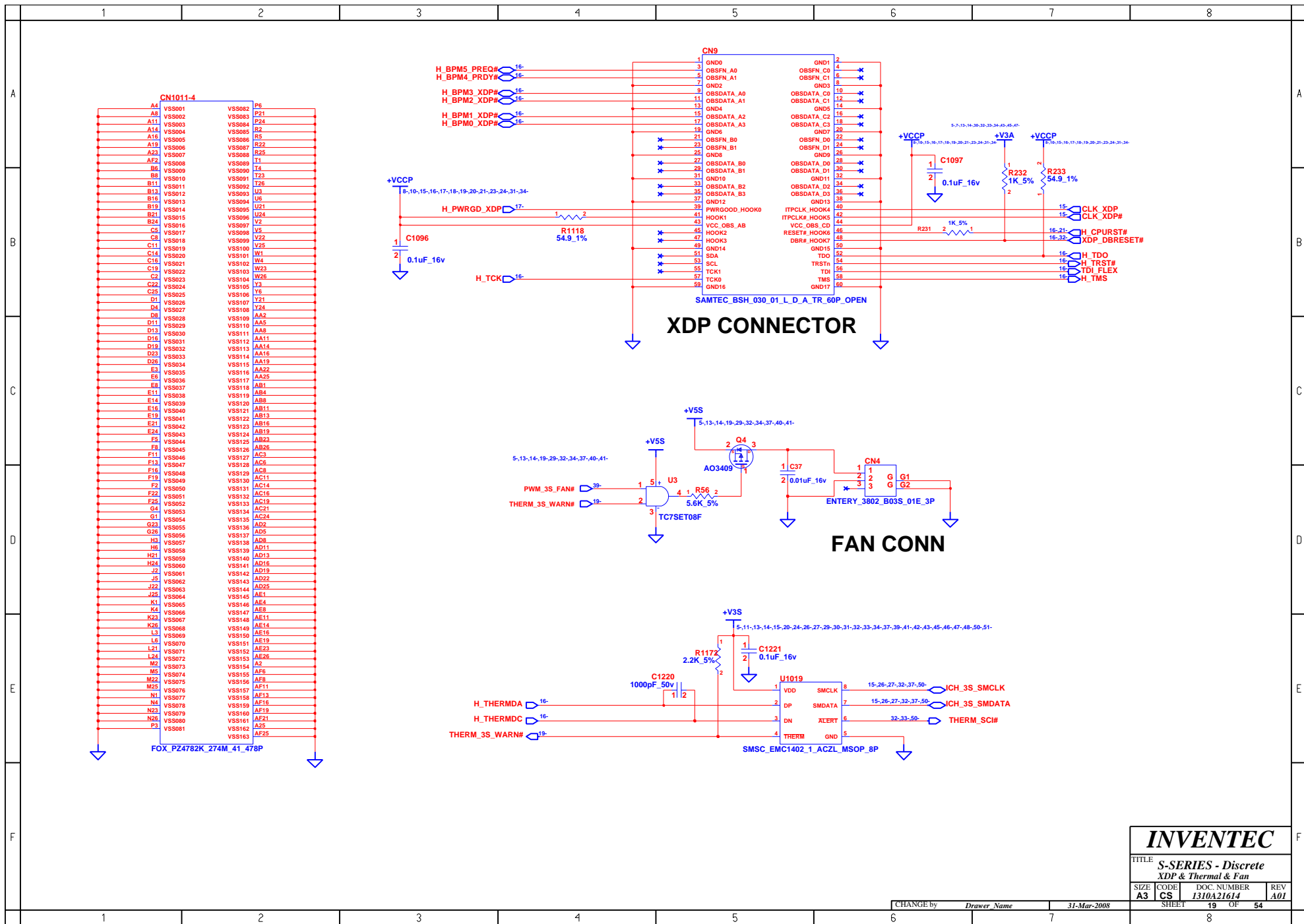
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LAYOUT NOTE:  
ROUTE VCCSENSE AND VSSSENSE TRACE AT  
24.7 OHM WITH 50 MIL SPACING  
PLACE PU AND PD WITHIN 1 INCH OF CPU

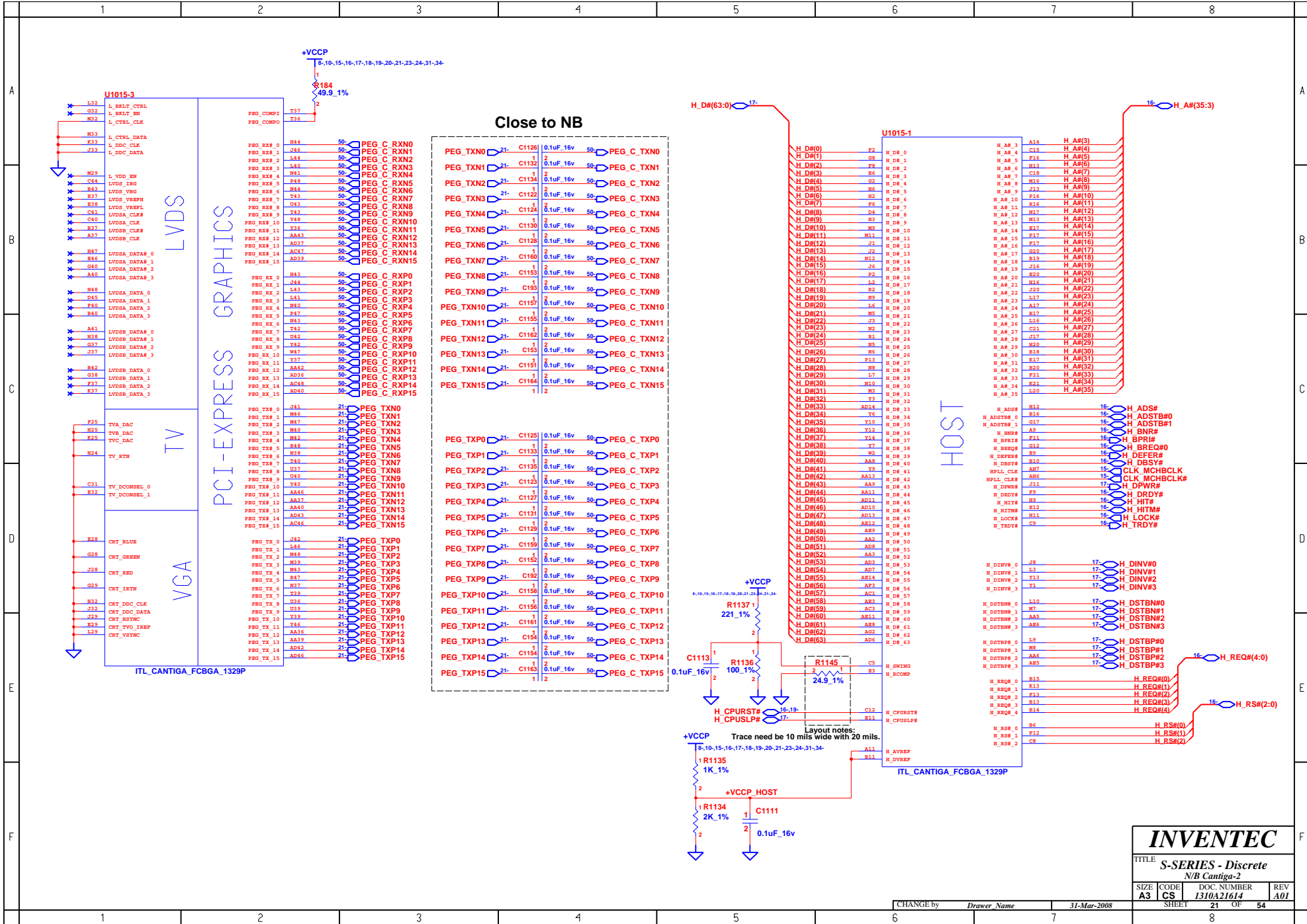
LAYOUT NOTE:  
PLACE C2461 NEAR PIN B26

<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete</b>			
CPU Penryn-3			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>I310A21614</b>	REV <b>A01</b>



<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete XDP &amp; Thermal &amp; Fan</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>I310A21614</b>	REV <b>A01</b>
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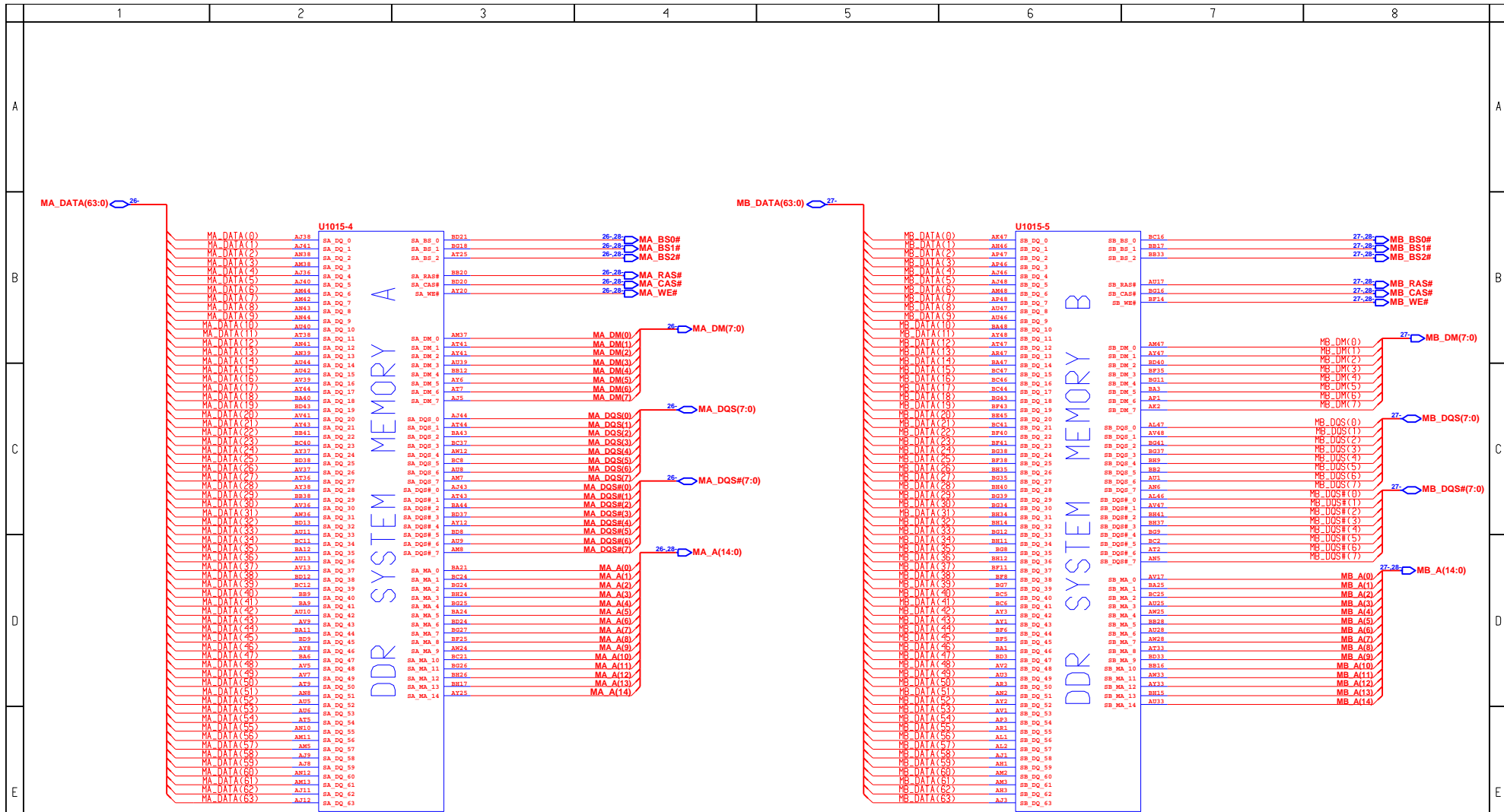
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TITLE  
**S-SERIES - Discrete**  
N/B Cantiga-2

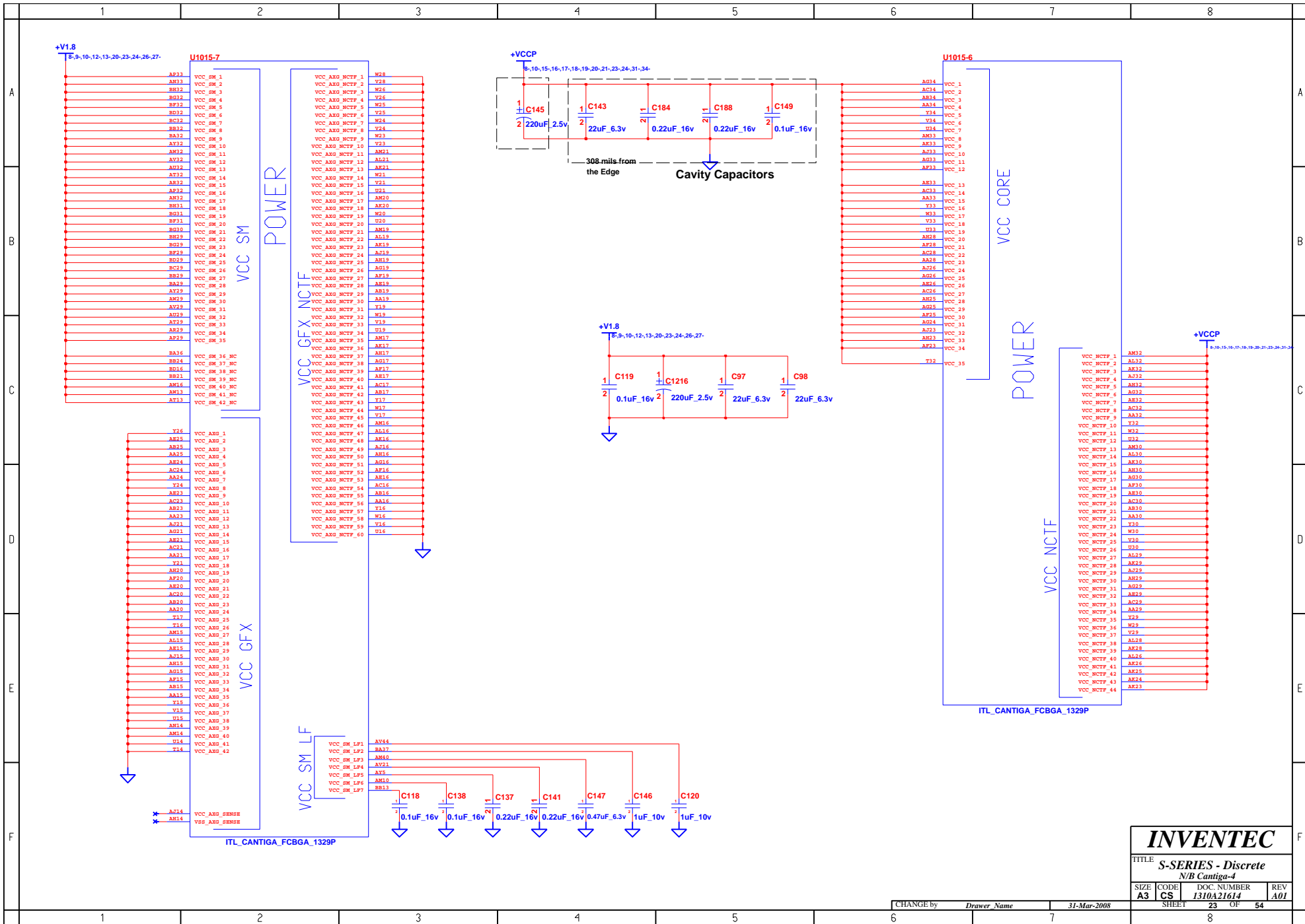
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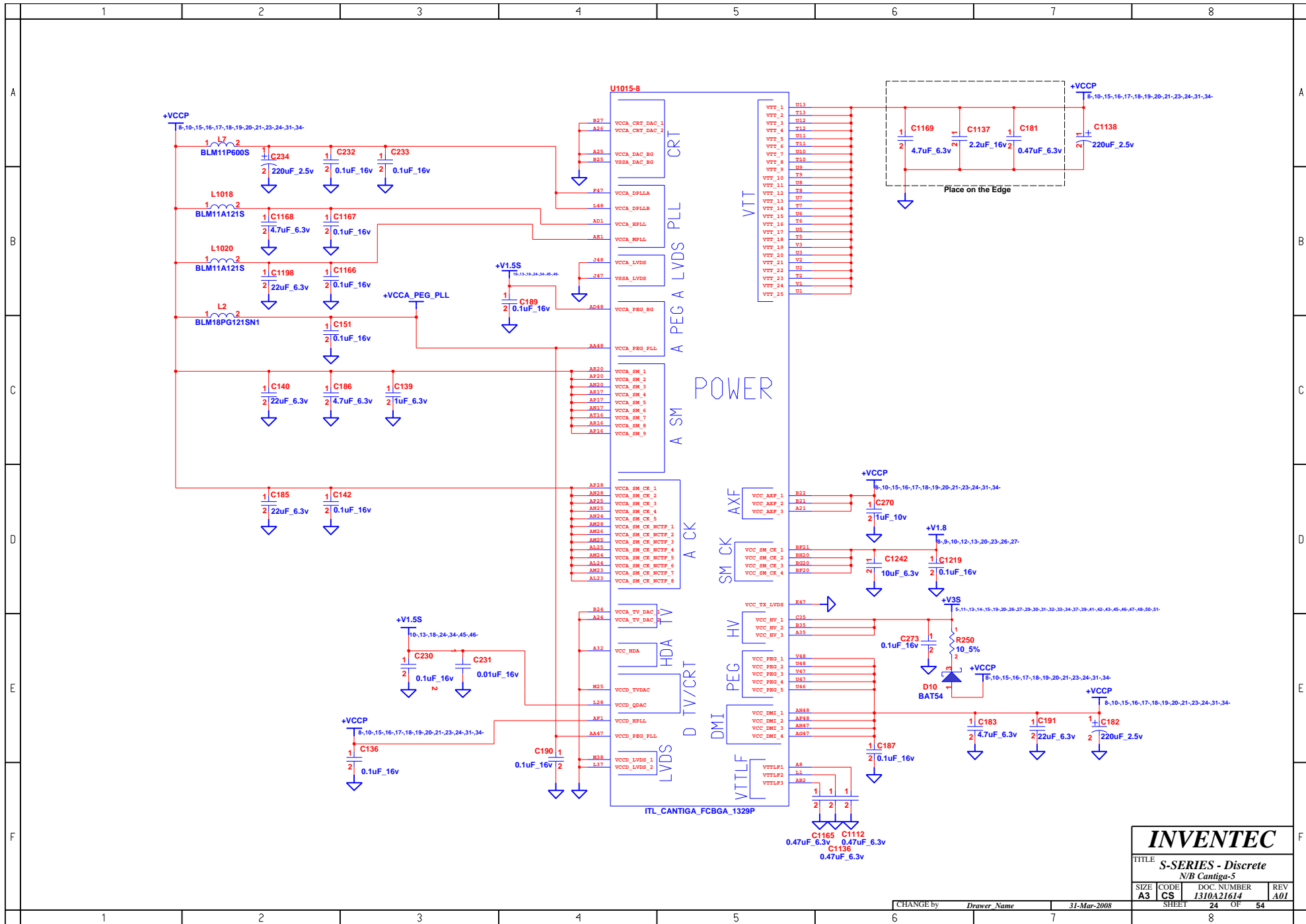
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<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete</b> N/B Cantiga-3			
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CHANGE by		Drawer Name	31-Mar-2008
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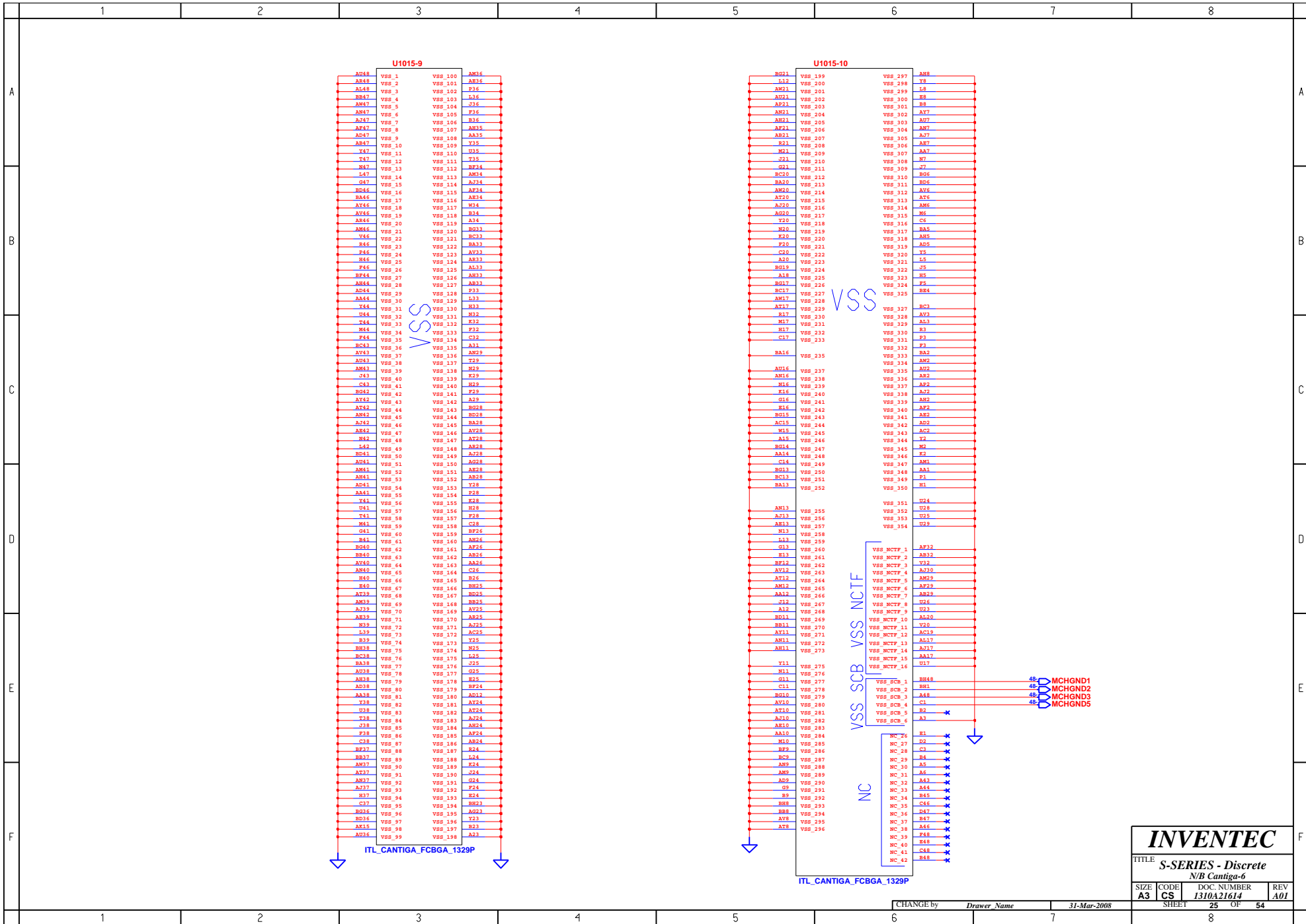
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CHANGE by <i>Drawer Name</i>		31-Mar-2008	
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**INVENTEC**  
 TITLE: S-SERIES - Discrete  
 N/B Cantiga-5

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01





**U1015-9**

AV48	V88_1	AM16
AK48	V88_2	AK16
AL48	V88_3	AL16
BM47	V88_4	BM16
AM47	V88_5	AM16
AM47	V88_6	F36
AV47	V88_7	AV16
AK47	V88_8	AK16
AM47	V88_9	AM16
AB47	V88_10	Y35
Y47	V88_11	Y35
AV47	V88_12	AV16
AK47	V88_13	AK16
Y47	V88_14	Y34
AV47	V88_15	AV16
AK46	V88_16	AK16
AM46	V88_17	AM16
AY46	V88_18	Y34
AV46	V88_19	AV16
AM46	V88_20	AM16
AM46	V88_21	AM16
Y46	V88_22	Y33
AV46	V88_23	AV16
AK46	V88_24	AK16
AV46	V88_25	AV16
AV46	V88_26	AV16
AV44	V88_27	AV16
AM44	V88_28	AM16
AD44	V88_29	D33
AM44	V88_30	AM16
Y44	V88_31	Y33
D44	V88_32	D32
T44	V88_33	T32
M44	V88_34	M32
AV43	V88_35	AV16
AV43	V88_36	AV16
AM43	V88_37	AM16
AM43	V88_38	AM16
AM43	V88_39	AM16
AV43	V88_40	AV16
AV43	V88_41	AV16
AV42	V88_42	AV16
AV42	V88_43	AV16
AV42	V88_44	AV16
AM42	V88_45	AM16
AV42	V88_46	AV16
AK42	V88_47	AK16
AV42	V88_48	AV16
AV42	V88_49	AV16
AV42	V88_50	AV16
AV42	V88_51	AV16
AM41	V88_52	AM16
AV41	V88_53	AV16
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AV41	V88_99	AV16

**U1015-10**

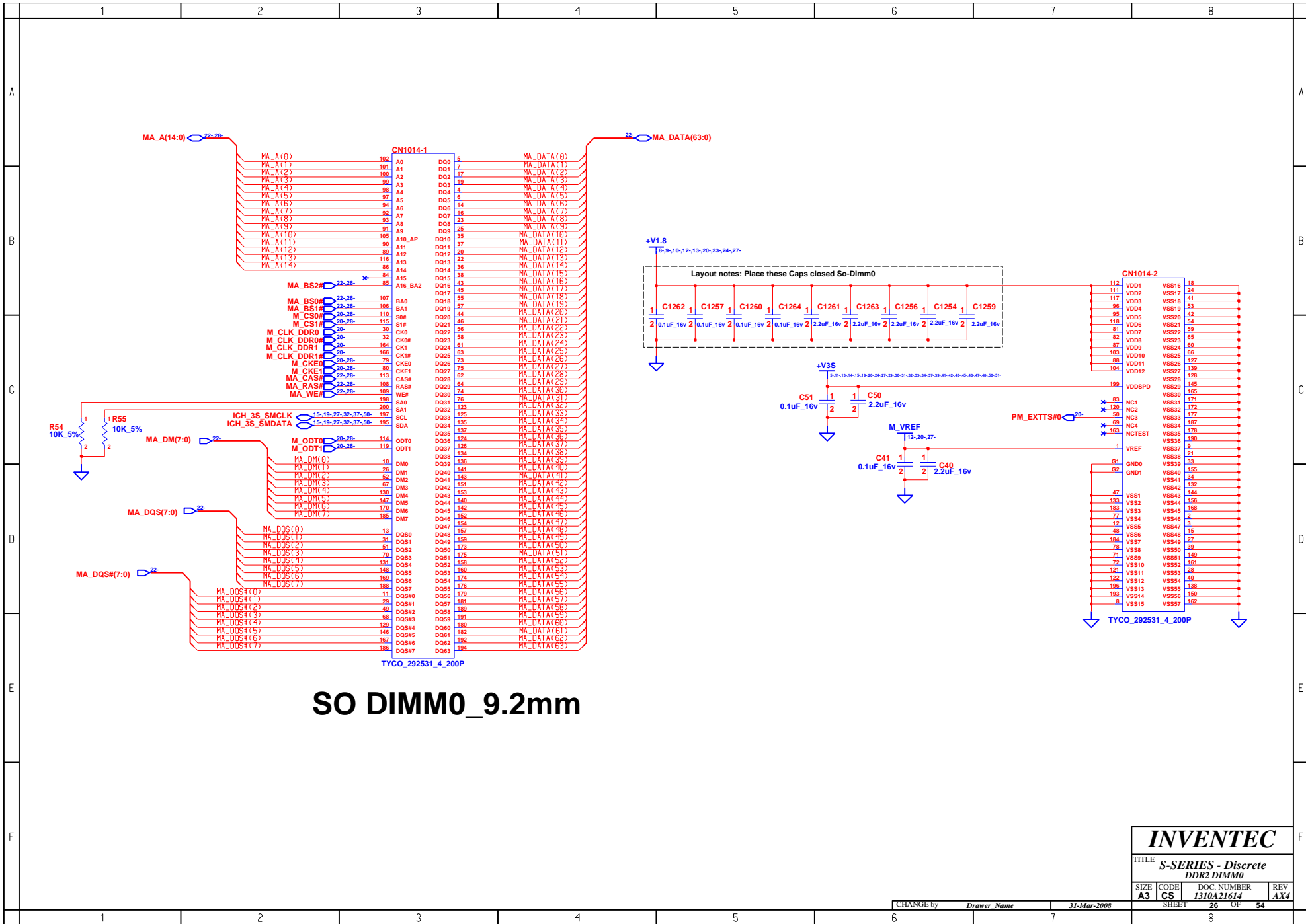
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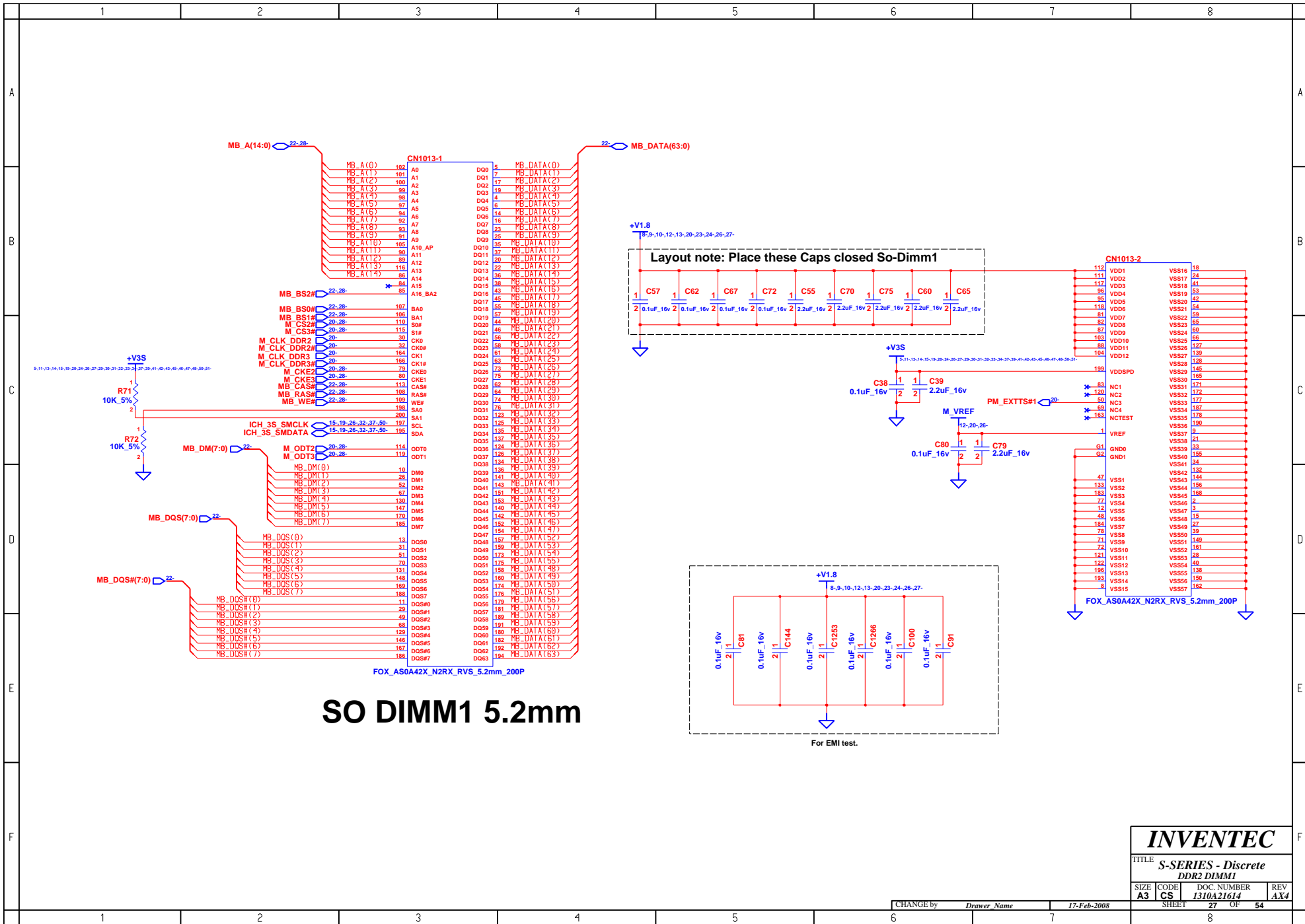
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N/B Cantiga-6

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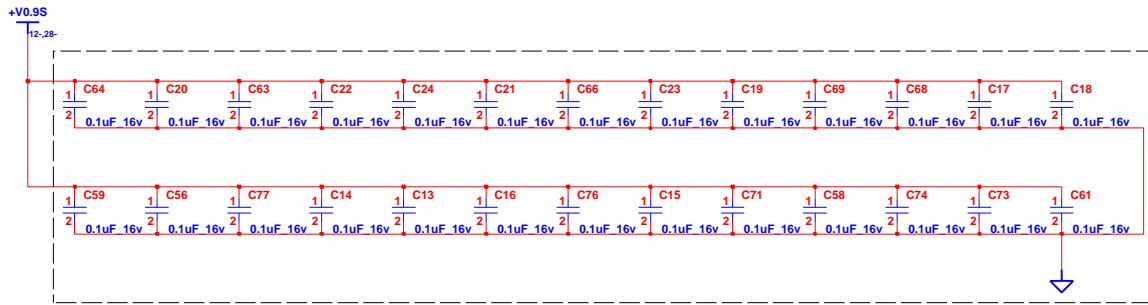
CHANGE by: *Drawer Name* 31-Mar-2008 SHEET 25 OF 54



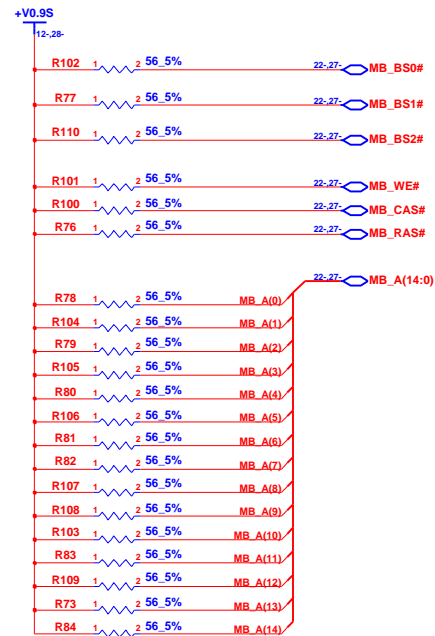
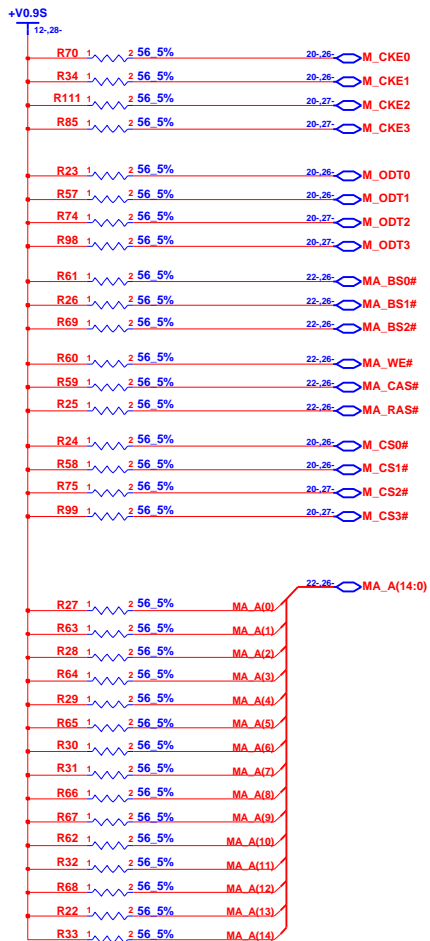
<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete DDR2 DIMM0</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>AX4</b>
CHANGE by <i>Drawer Name</i>		31-Mar-2008	SHEET 26 OF 54



<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete DDR2 DIMM1</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>AX4</b>
CHANGE by <i>Drawer Name</i>		17-Feb-2008	
SHEET <b>27</b>		OF <b>54</b>	



Layout notes : Place one Cap close to every 2 pull up resistor terminated to +V0.9S.



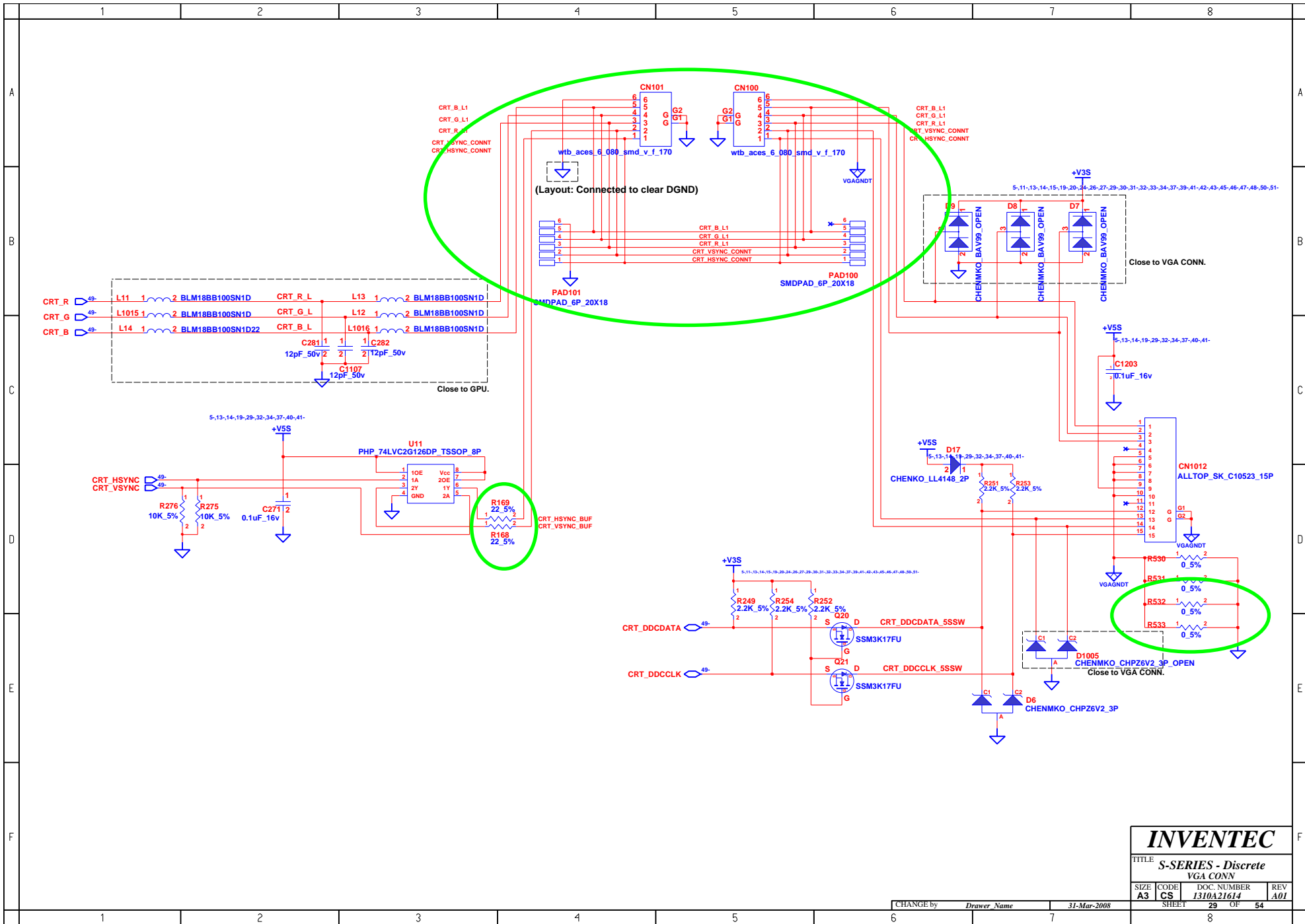
# INVENTEC

TITLE  
**S-SERIES - Discrete**  
DDR2 Damping

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
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CHANGE by *Drawer Name* 27-Sep-2003

SHEET 28 OF 54

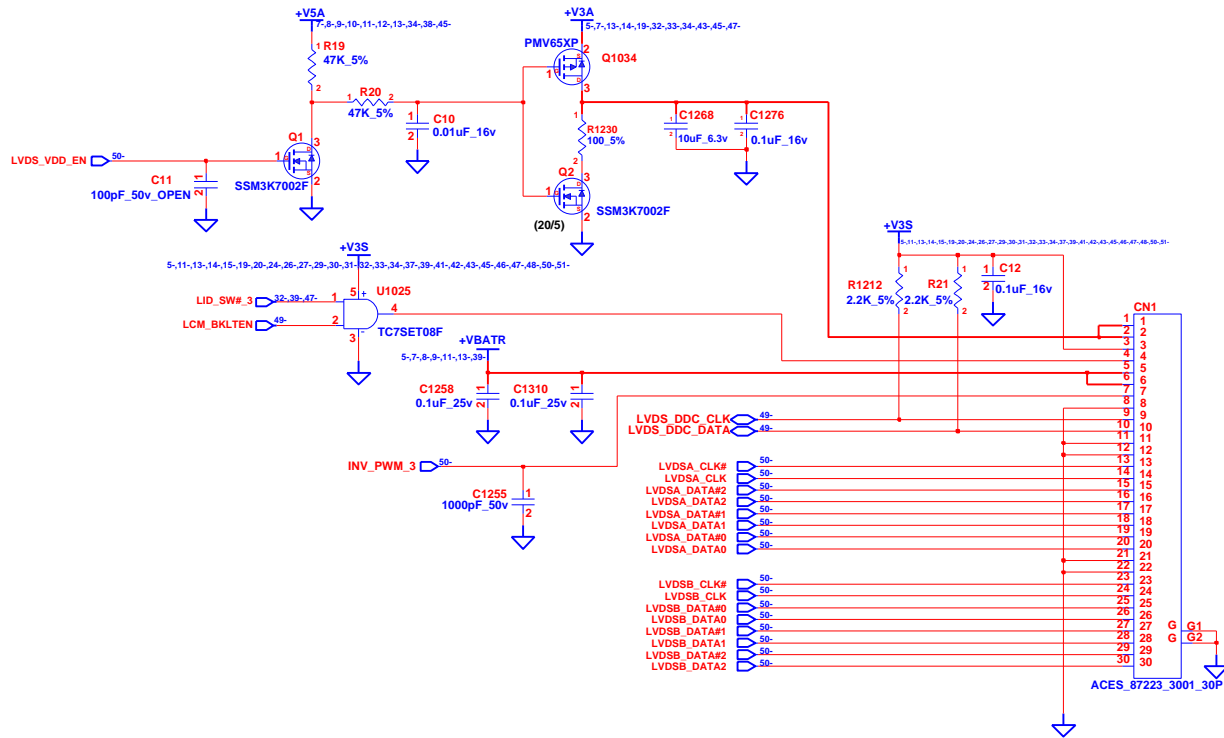


# INVENTEC

TITLE  
**S-SERIES - Discrete**  
 VGA CONN

SIZE CODE CS DOC. NUMBER REV  
 A3 1310A21614 A01

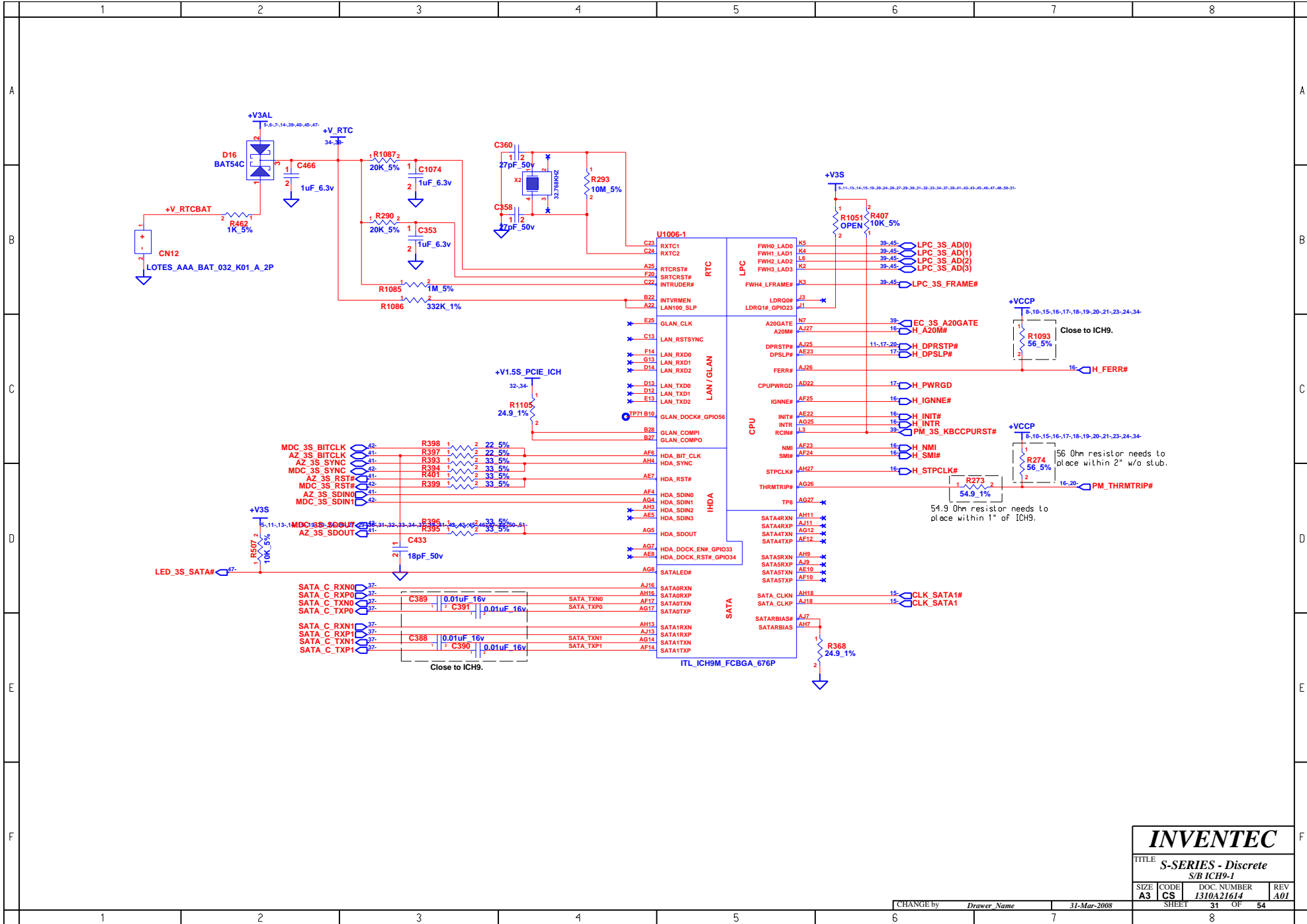
Place closed to connector



**INVENTEC**

TITLE  
**S-SERIES - Discrete**  
 LCM CONN

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
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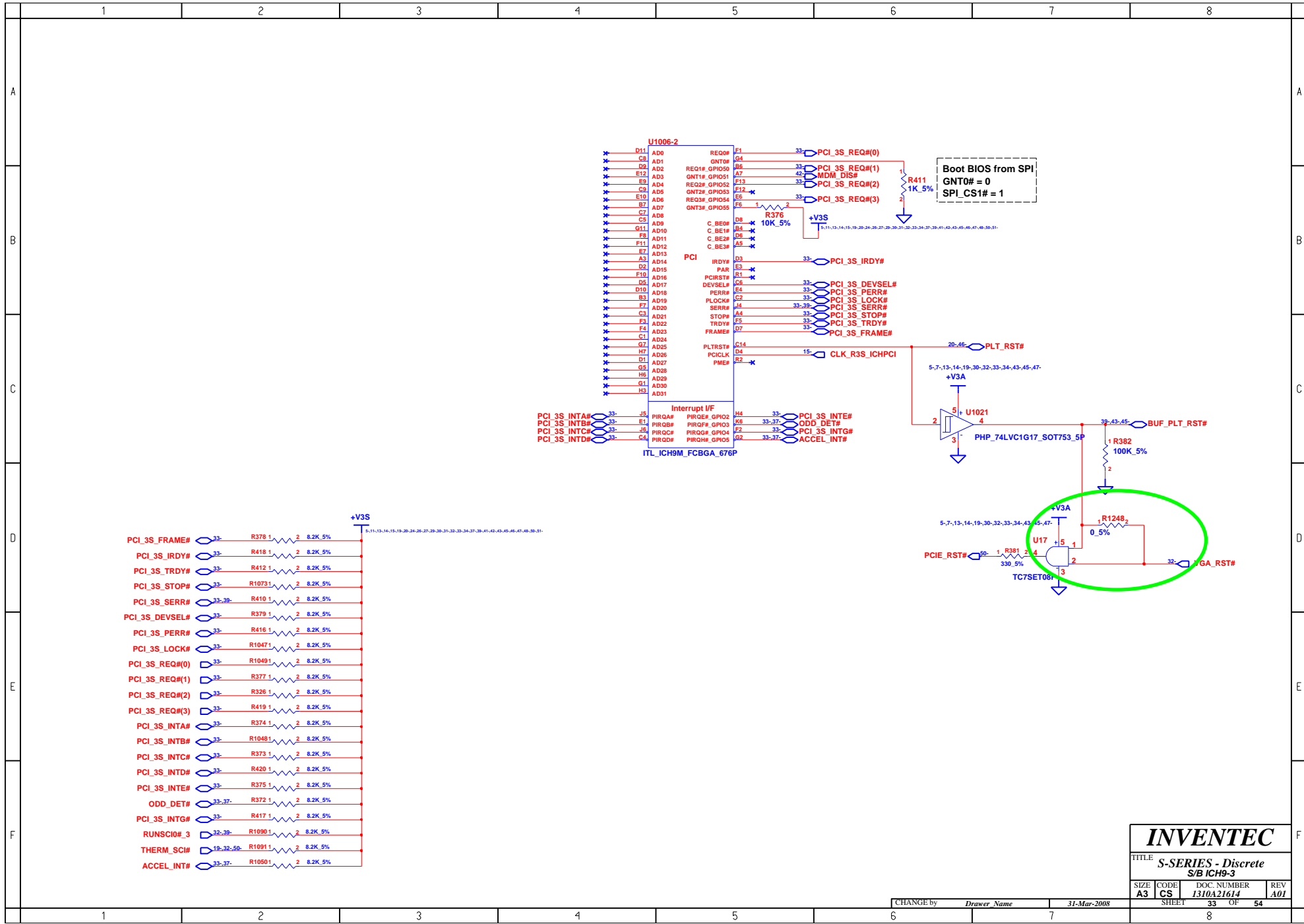
# INVENTEC

TITLE  
S-SERIES - Discrete  
S/B ICH9-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01







Signal	Resistor	Value	Notes
PCI_3S_FRAME#	R376	8.2K	5%
PCI_3S_IRDY#	R418	8.2K	5%
PCI_3S_TRDY#	R412	8.2K	5%
PCI_3S_STOP#	R1073	8.2K	5%
PCI_3S_SERR#	R410	8.2K	5%
PCI_3S_DEVSEL#	R379	8.2K	5%
PCI_3S_PERR#	R416	8.2K	5%
PCI_3S_LOCK#	R1047	8.2K	5%
PCI_3S_REQ#(0)	R1049	8.2K	5%
PCI_3S_REQ#(1)	R377	8.2K	5%
PCI_3S_REQ#(2)	R326	8.2K	5%
PCI_3S_REQ#(3)	R419	8.2K	5%
PCI_3S_INTA#	R374	8.2K	5%
PCI_3S_INTB#	R1048	8.2K	5%
PCI_3S_INTC#	R373	8.2K	5%
PCI_3S_INTD#	R420	8.2K	5%
PCI_3S_INTE#	R375	8.2K	5%
ODD_DET#	R372	8.2K	5%
PCI_3S_INTG#	R417	8.2K	5%
RUNSCIO#_3	R1090	8.2K	5%
THERM_SCI#	R1091	8.2K	5%
ACCEL_INT#	R1050	8.2K	5%

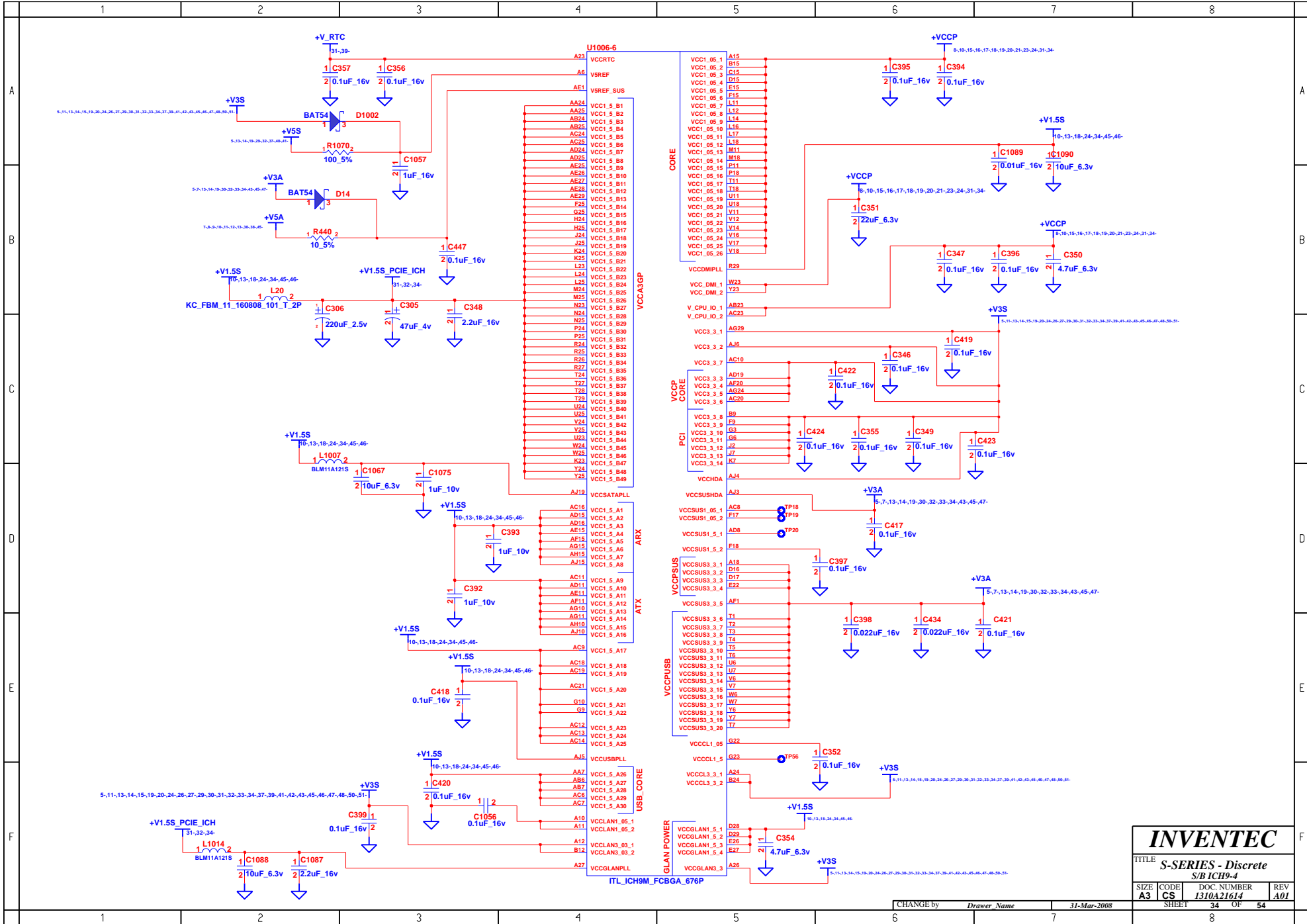
Boot BIOS from SPI  
 GNT0# = 0  
 SPI\_CS1# = 1

+V3A  
 5-7-13-14-19-30-32-33-34-43-45-47-

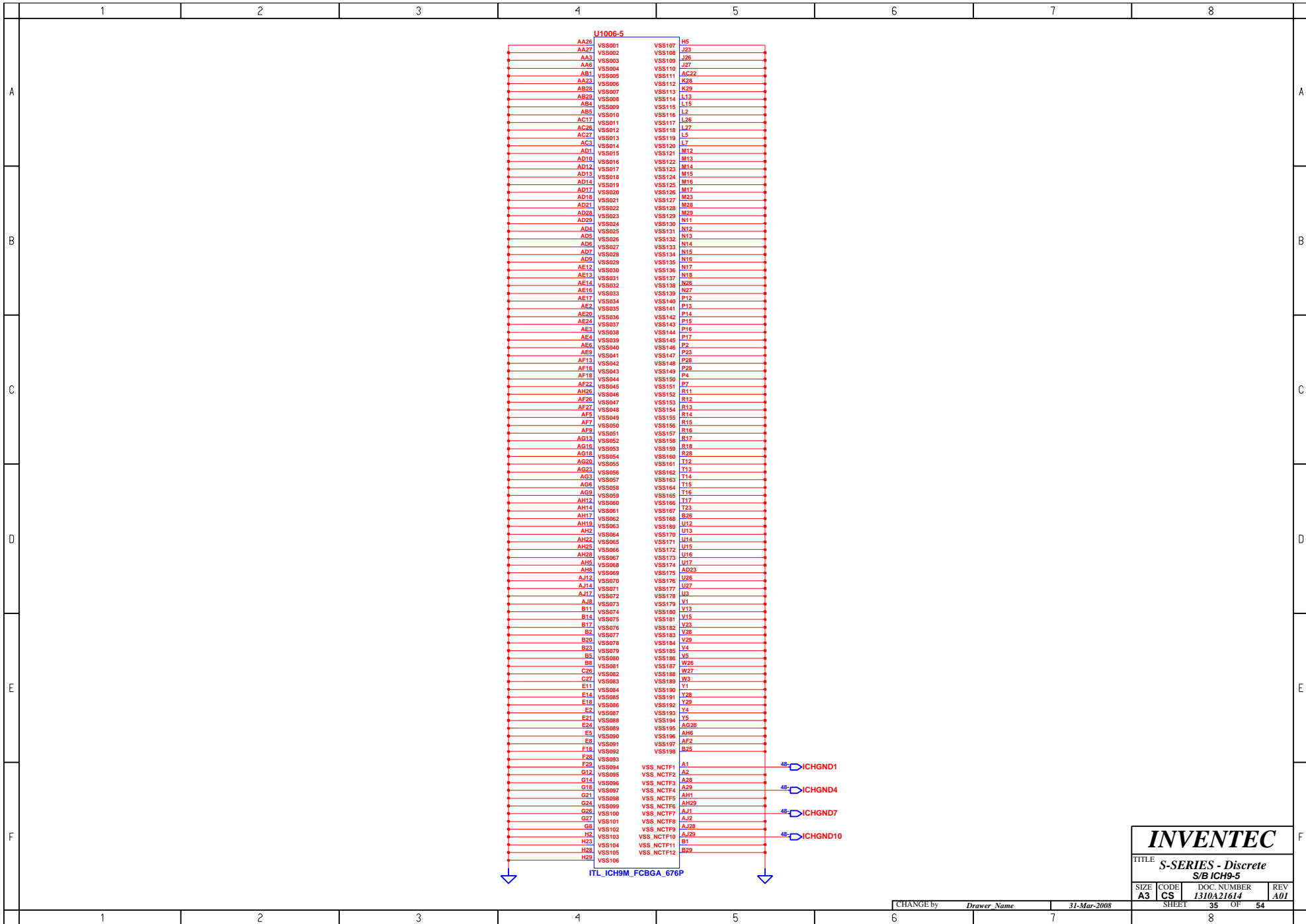
+V3A  
 5-7-13-14-19-30-32-33-34-43-45-47-

**INVENTEC**  
 TITLE S-SERIES - Discrete  
 S/B ICH9-3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01



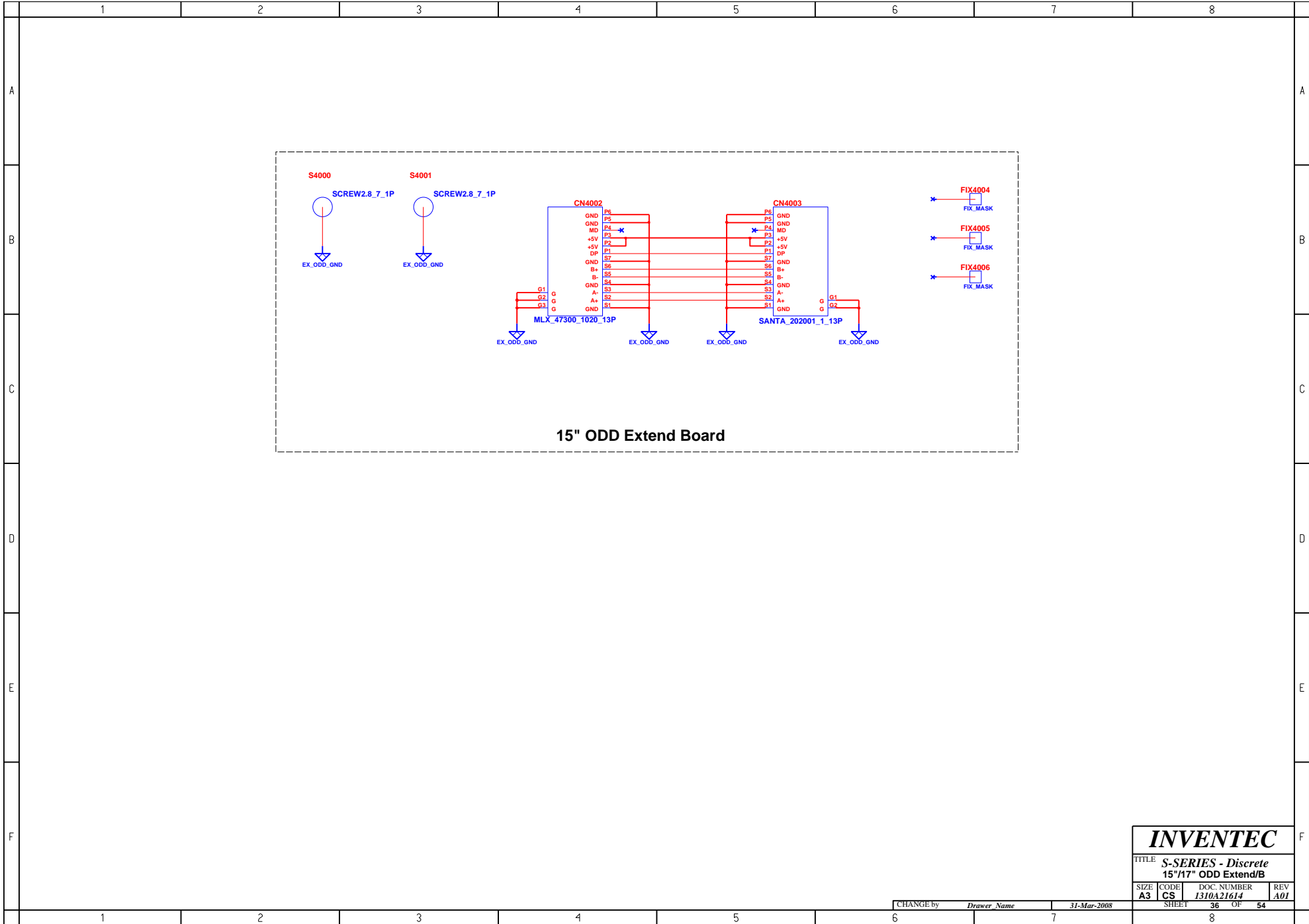
<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete</b> <b>S/B ICH9-d</b>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
CHANGE by <i>Drawer Name</i>		31-Mar-2008	SHEET <b>34</b> OF <b>54</b>



**INVENTEC**  
 TITLE *S-SERIES - Discrete*  
*S/B ICH9-5*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01

CHANGE by *Drawer Name* 31-Mar-2008 SHEET 35 OF 54



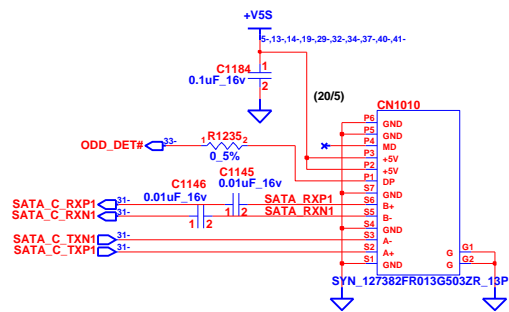
**INVENTEC**

TITLE *S-SERIES - Discrete*  
**15"17" ODD Extend/B**

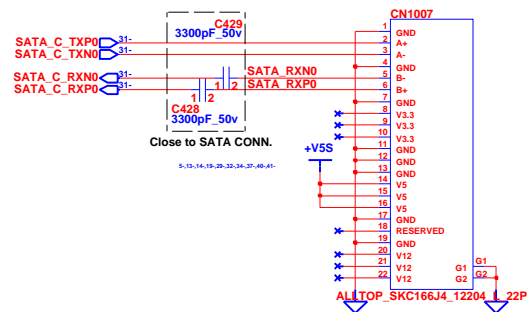
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <i>1310A21614</i>	REV <b>A01</b>
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CHANGE by *Drawer Name* 31-Mar-2008

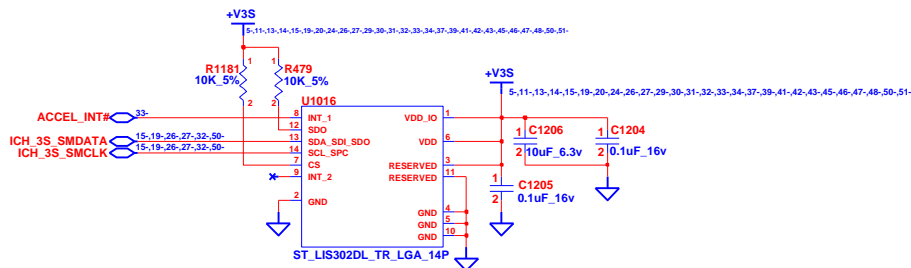
SHEET 36 OF 54



SATA ODD



SATA HDD



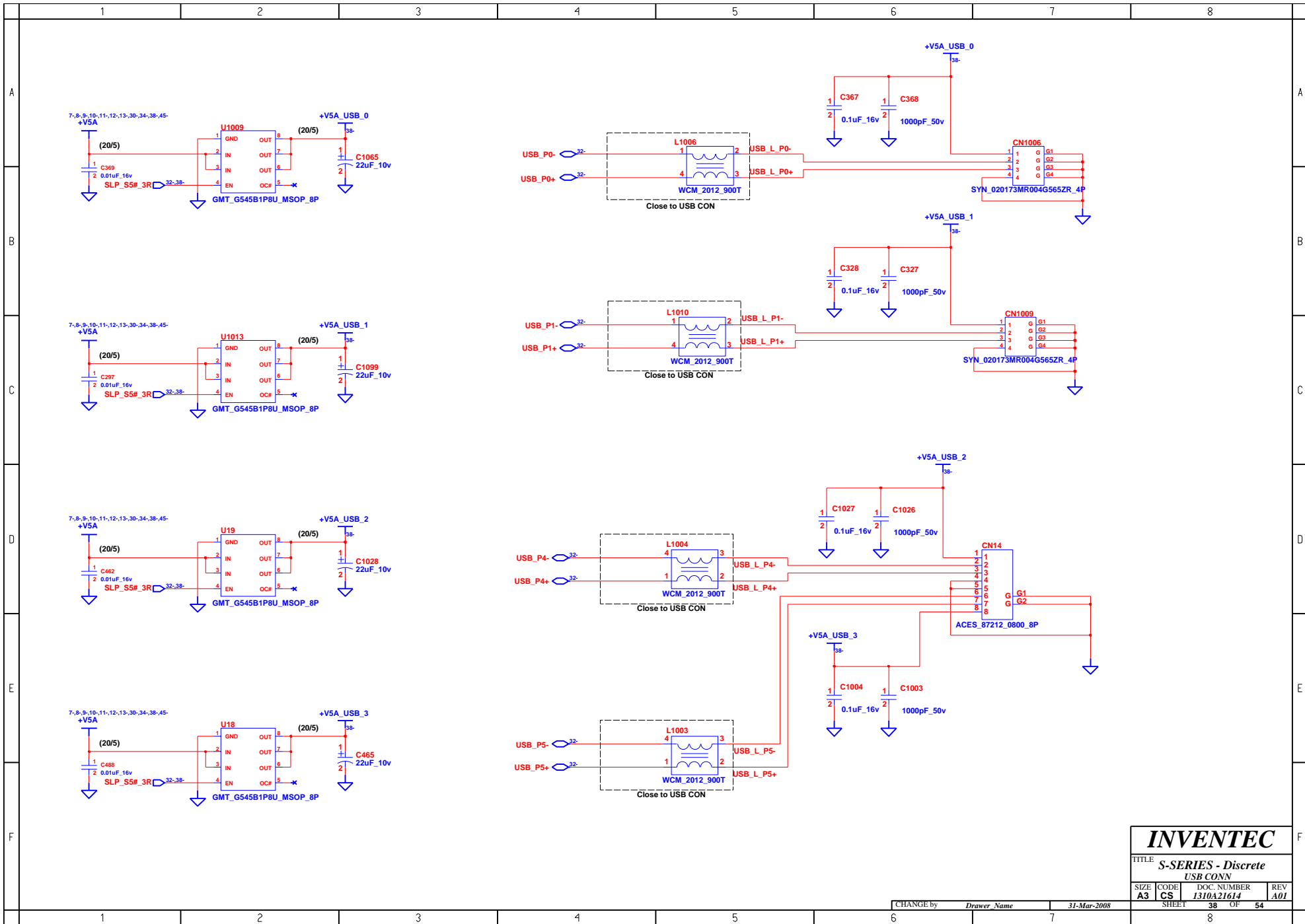
Accelerometer

**INVENTEC**

TITLE			
S-SERIES - Discrete			
HDD & ODD CONN & Accelerometer			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01

CHANGE by *Drawer Name* 31-Mar-2008

SHEET 37 OF 54



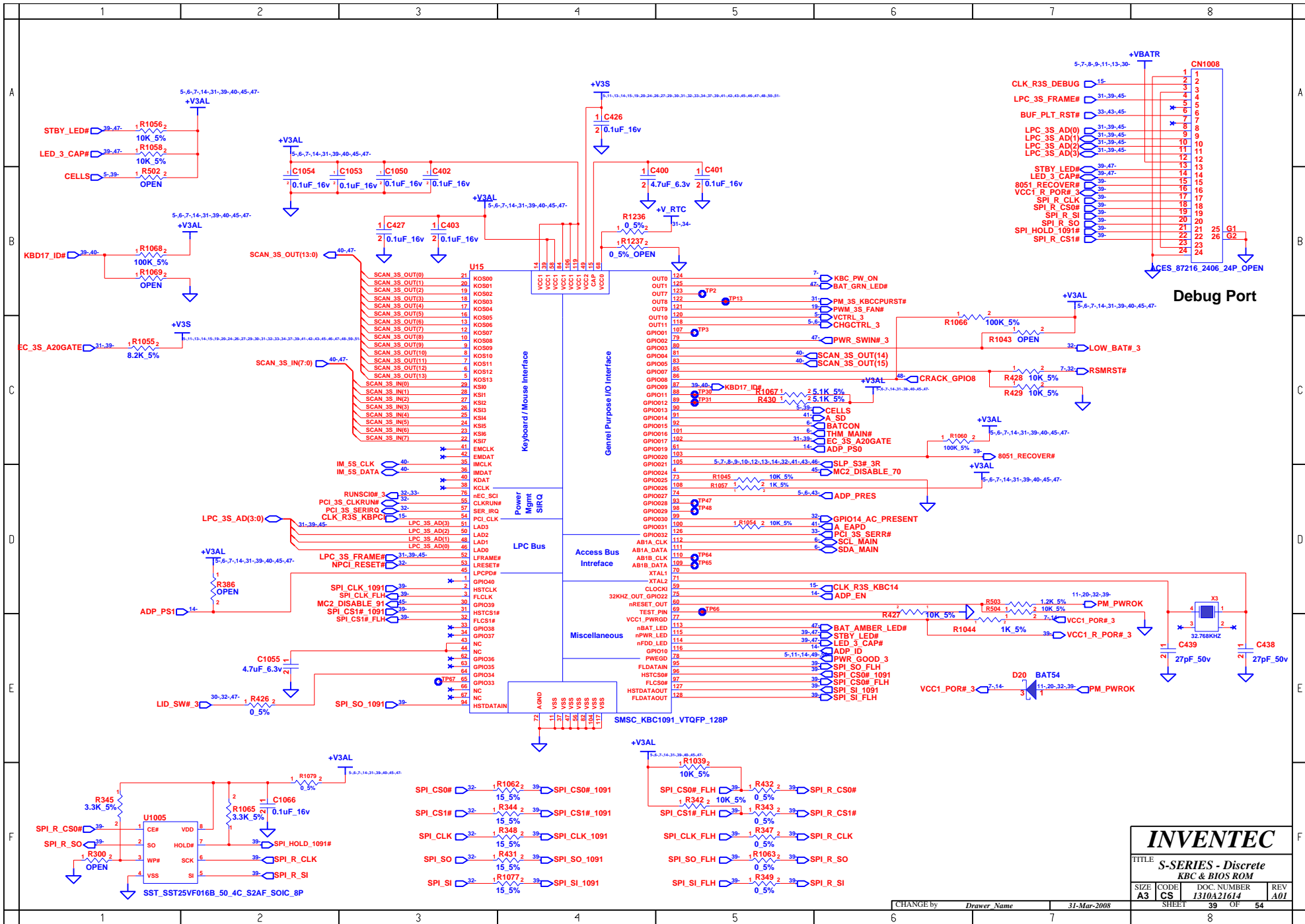
# INVENTEC

TITLE  
**S-SERIES - Discrete**  
**USB CONN**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
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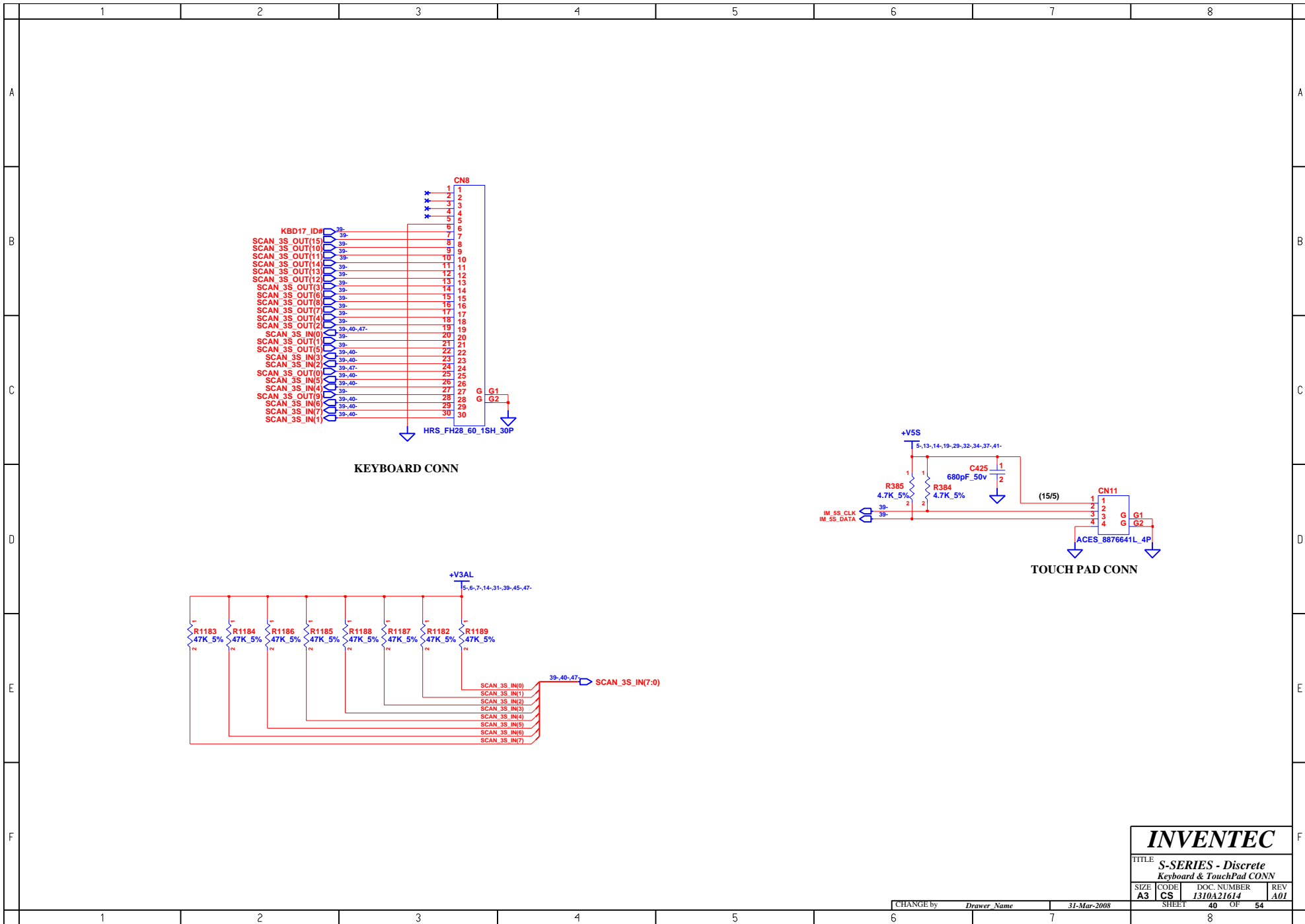
CHANGE by *Drawer Name* 31-Mar-2008

SHEET 38 OF 54



**INVENTEC**  
 TITLE: S-SERIES - Discrete  
 KBC & BIOS ROM

SIZE: A3 CS    CODE:    DOC NUMBER: 1310A21614    REV: A01



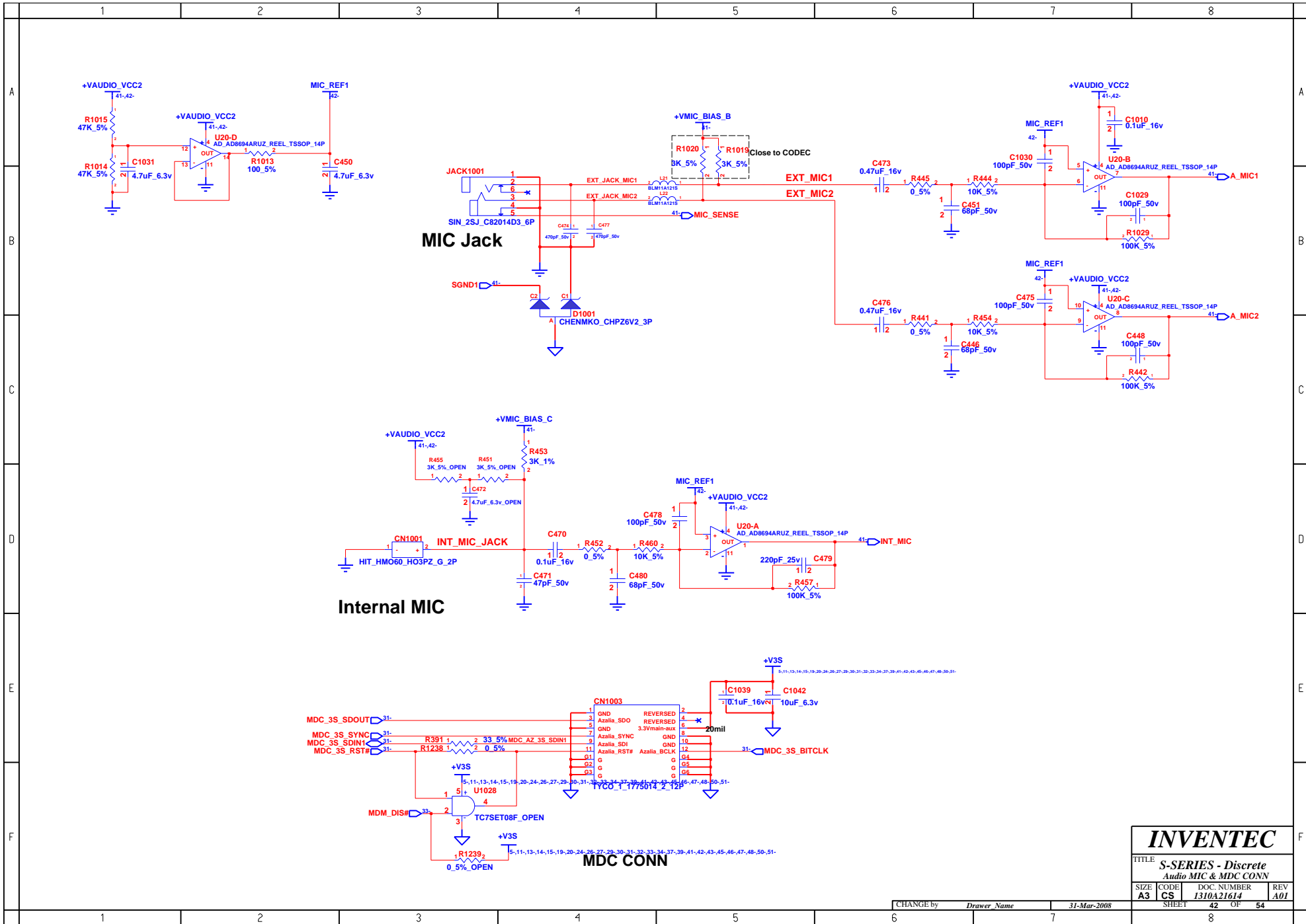
# INVENTEC

TITLE  
**S-SERIES - Discrete**  
 Keyboard & TouchPad CONN

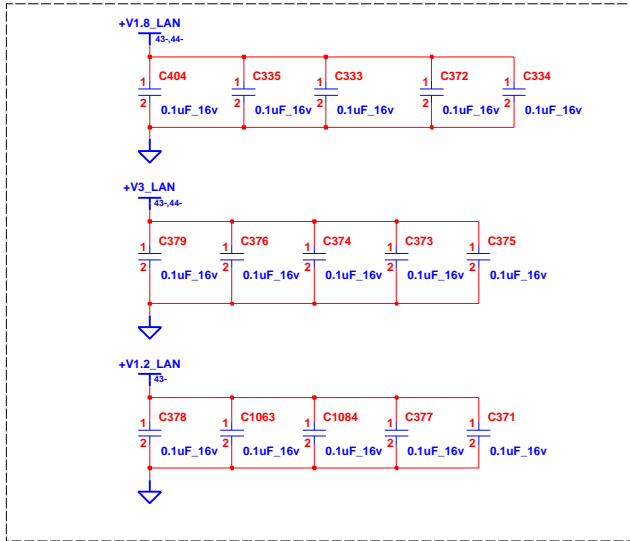
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
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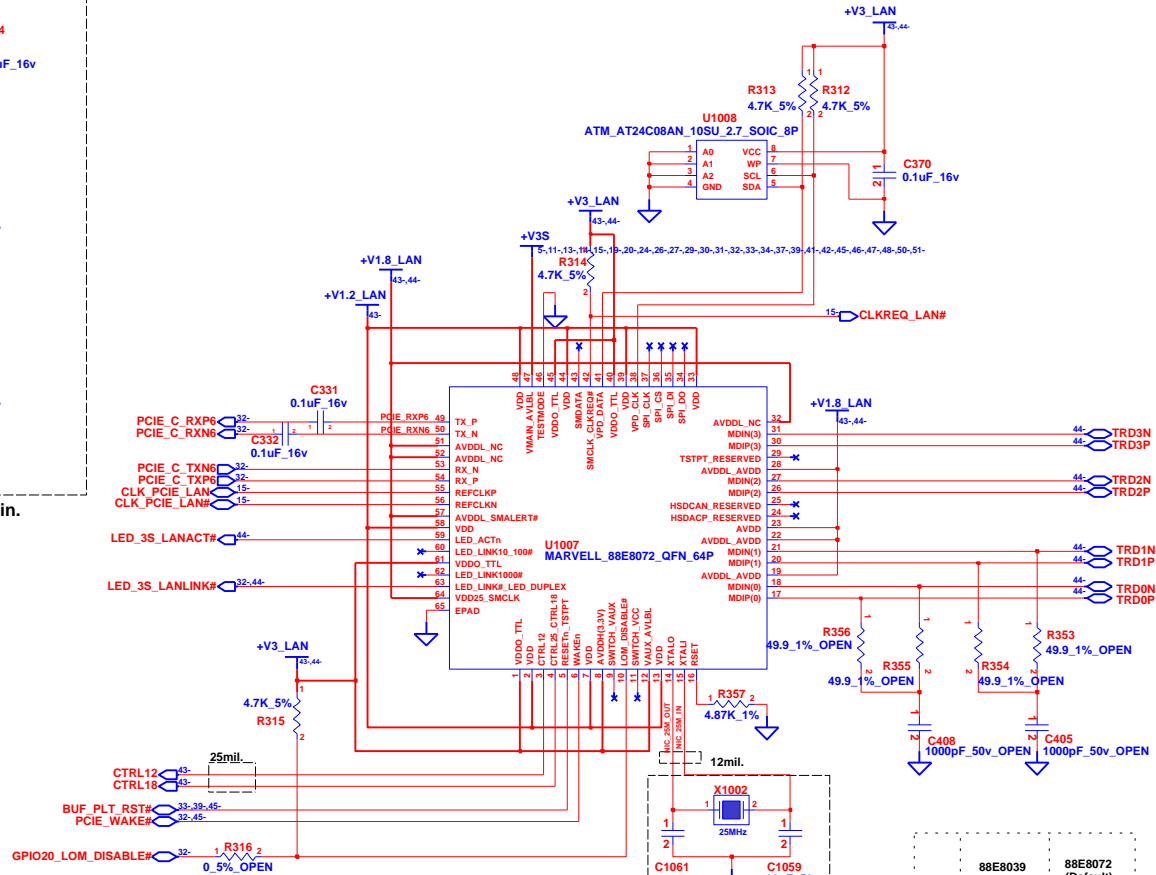




<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete</b> Audio MIC & MDC CONN			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC NUMBER <b>I310A21614</b>	REV <b>A01</b>
CHANGE by <i>Drawer Name</i>		31-Mar-2008	SHEET 42 OF 54

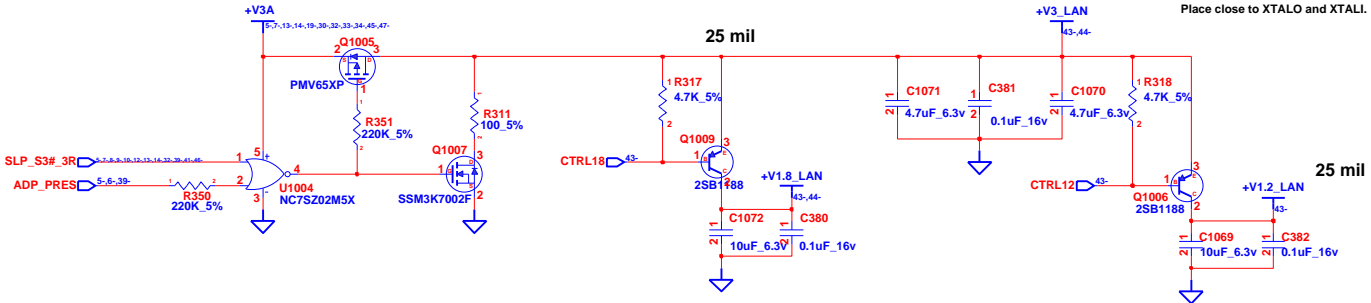


Place bypass cap as close as possible with every power pin.



Place close to XTALO and XTALI.

	88E8039	88E8072 (Default)
R356	49.9_1%	NI
R355	49.9_1%	NI
R354	49.9_1%	NI
R353	49.9_1%	NI
C408	1000p_50V	NI
C405	1000p_50V	NI
R357	2K_1%	4.87K_1%



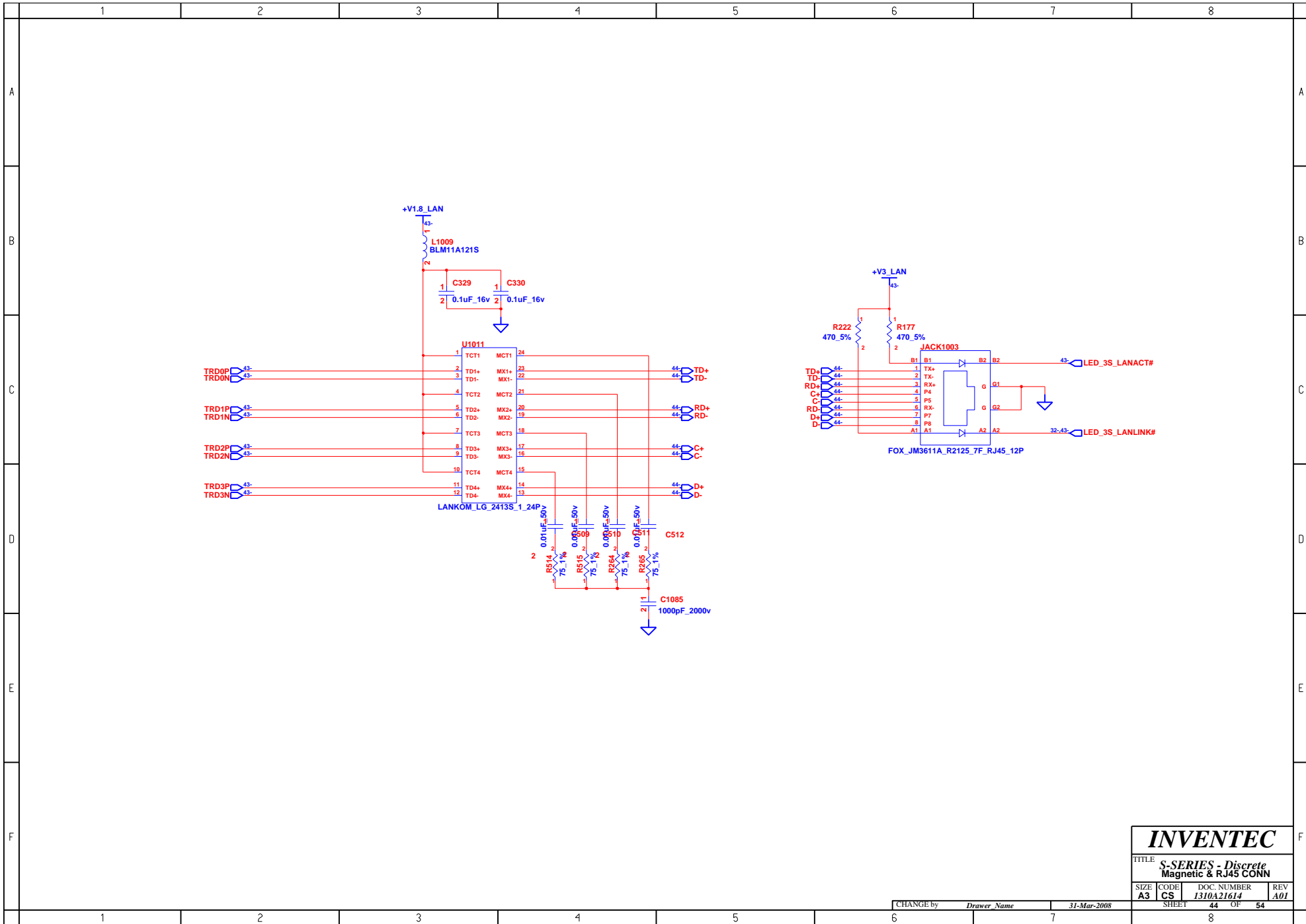
# INVENTEC

TITLE: S-SERIES - Discrete  
Giga LAN Controller

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01

CHANGE by Drawer Name 31-Mar-2008

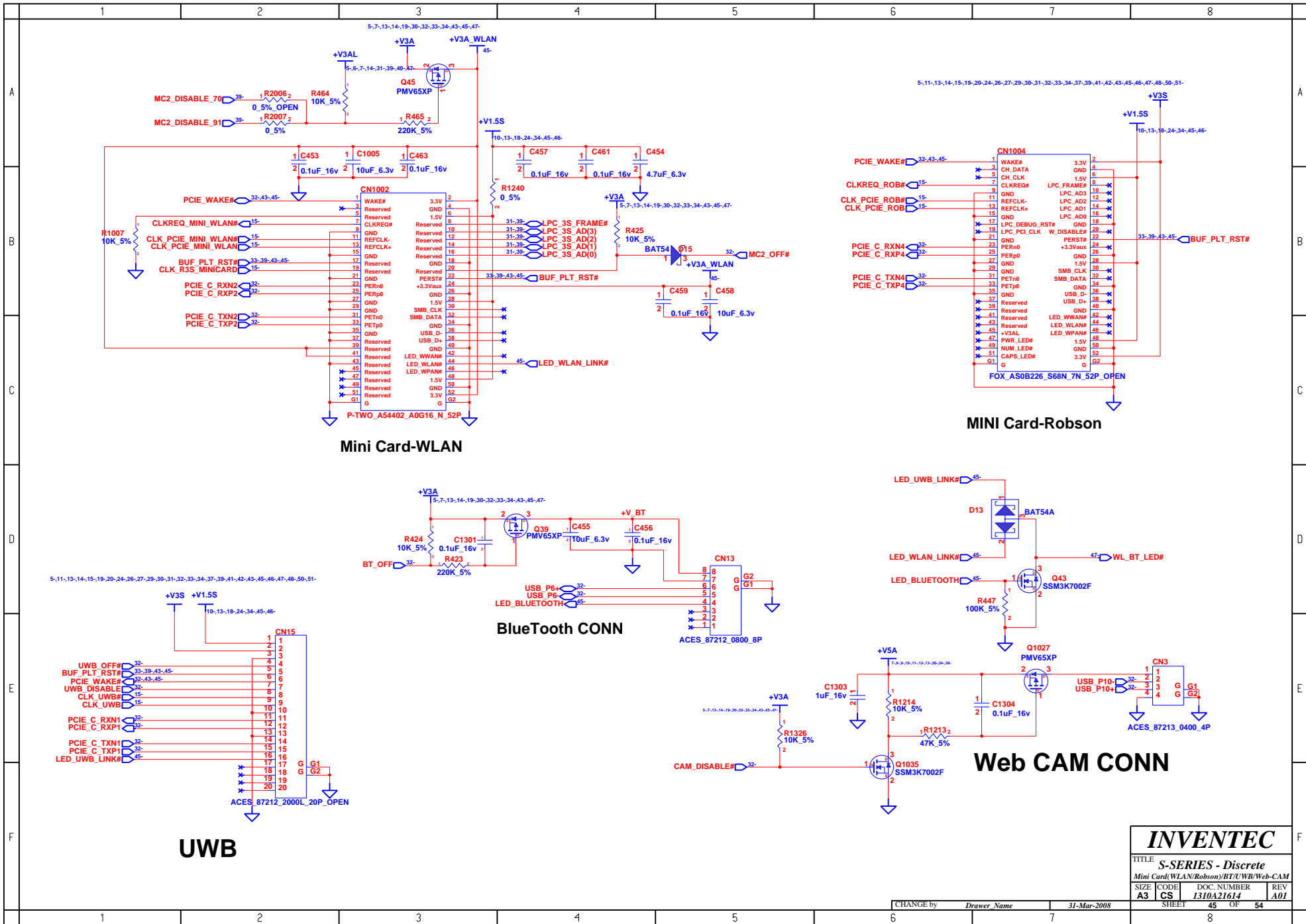
SHEET 43 OF 54



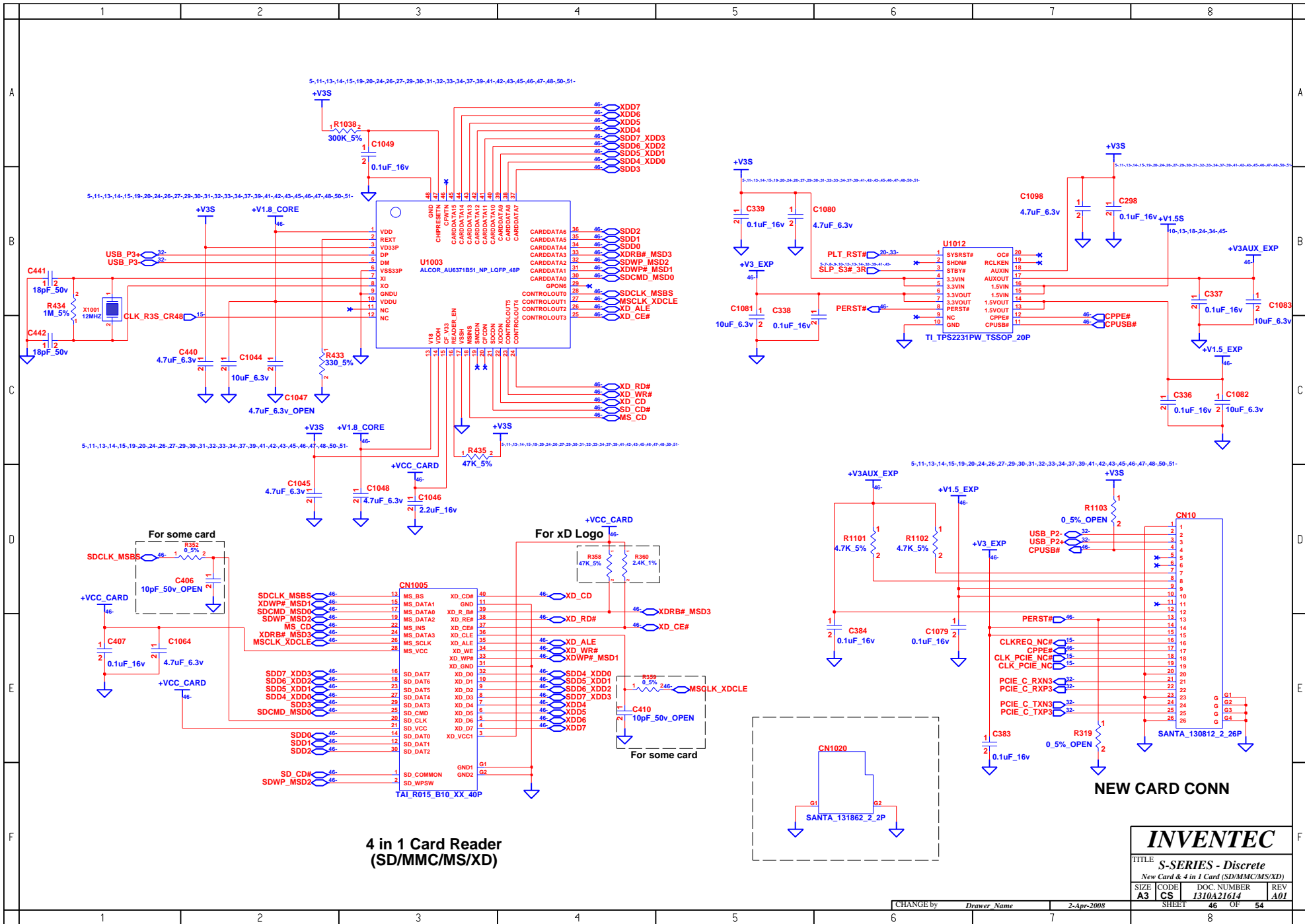
**INVENTEC**

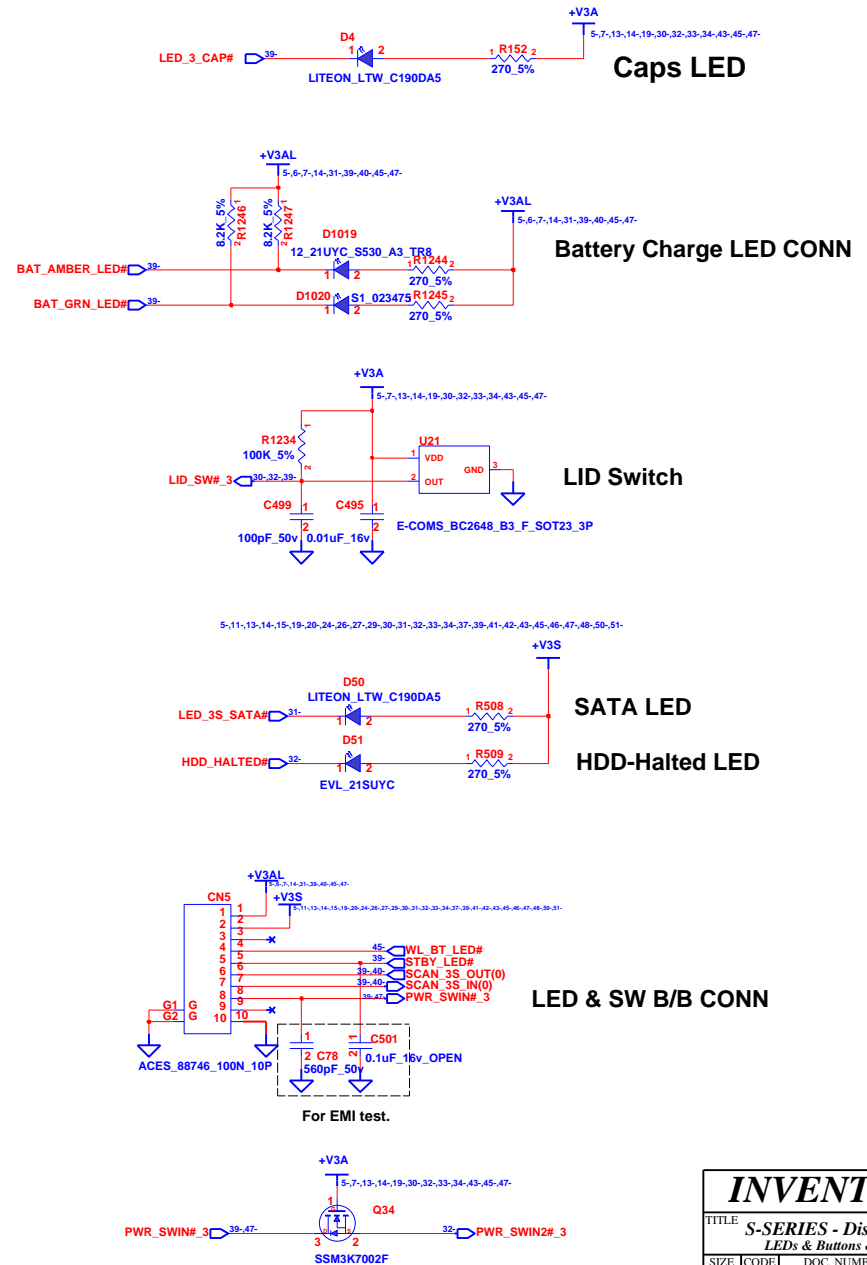
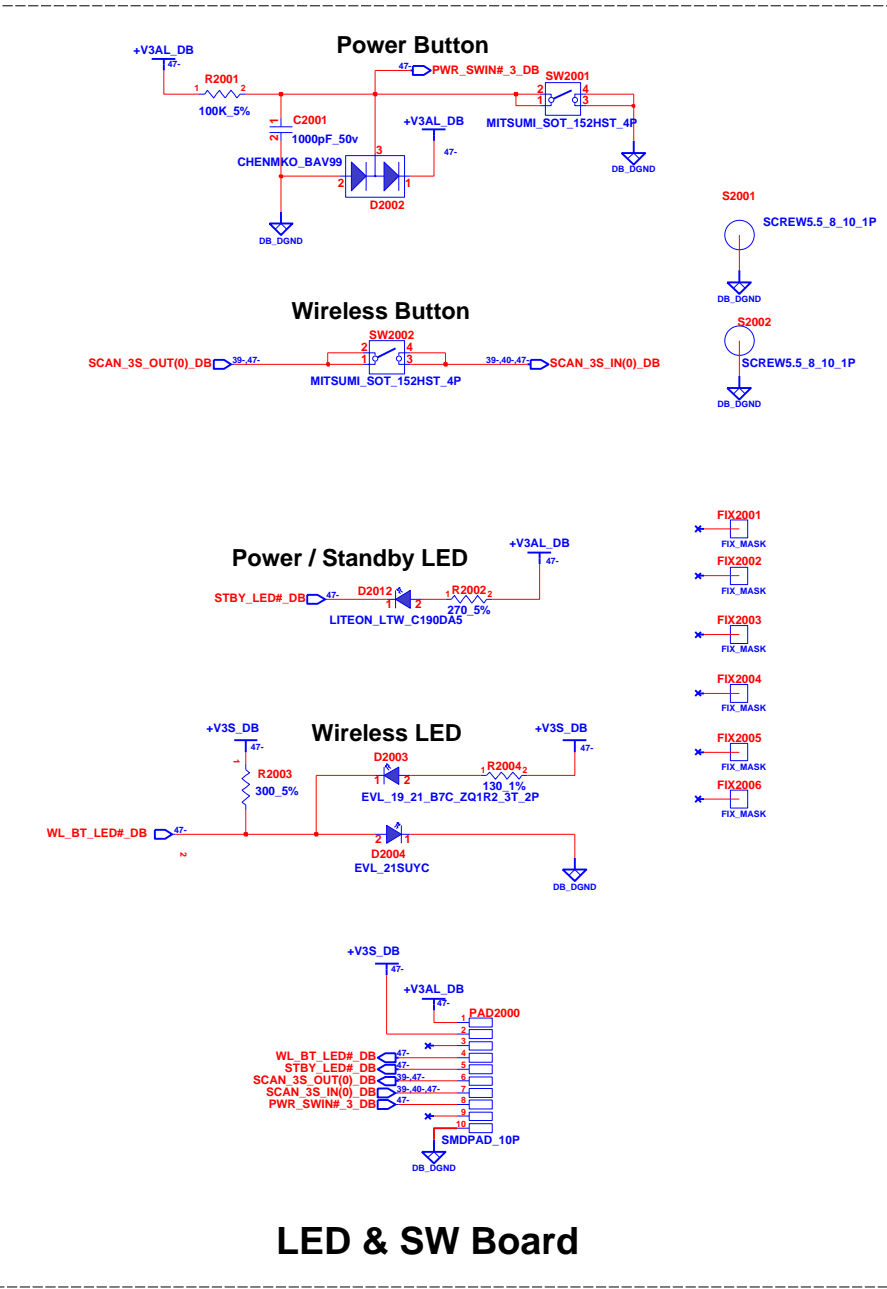
TITLE  
**S-SERIES - Discrete  
 Magnetic & RJ45 CONN**

SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
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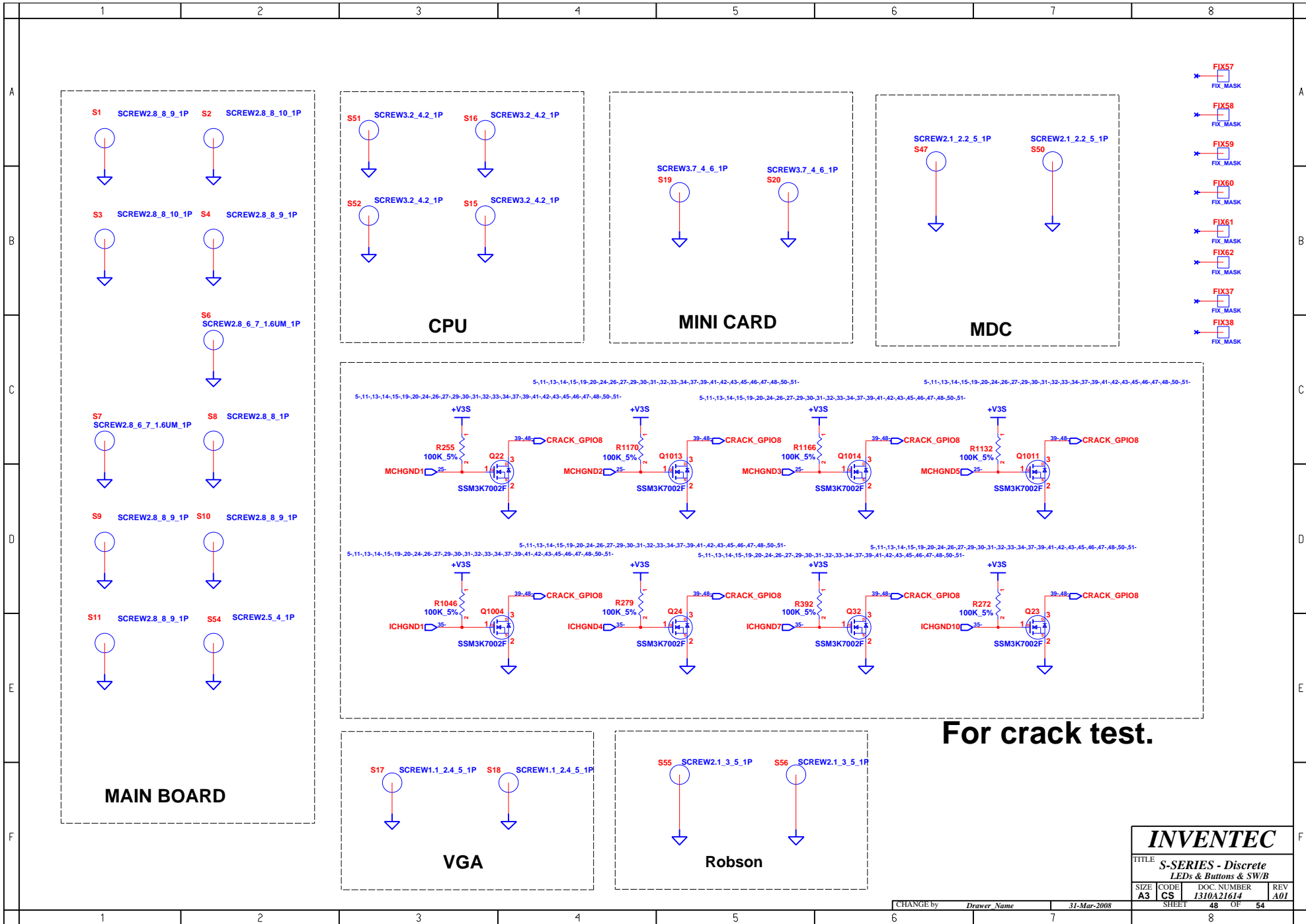


<b>INVENTEC</b>			
TITLE <i>S-SERIES - Discrete</i>			
Mini Card(WLAN/Robson)/BT/UWB/Web-CAM			
SIZE A3	CODE CS	DOC. NUMBER 1310A21614	REV A01
CHANGE by <i>Drawer Name</i>		31-Mar-2008	
SHEET 1		45 Of 54	





<b>INVENTEC</b>			
TITLE: S-SERIES - Discrete LEDs & Buttons & SW/B			
SIZE: A3	CODE: CS	DOC NUMBER: 1310A21614	REV: A01
CHANGE by: Drawer Name		31-Mar-2008	
SHEET: 47		OF: 54	



**For crack test.**

<b>INVENTEC</b>			
TITLE <i>S-SERIES - Discrete LEDs &amp; Buttons &amp; SW/B</i>			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC NUMBER <b>1310A21614</b>	REV <b>A01</b>
CHANGE by <i>Drawer Name</i>		31-Mar-2008	
SHEET		48 OF 54	



STRAPS	PIN	Description of default settings	
TX_PWRS_ENB	GPIO0	PCIe full TX output swing.	1
TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enabled.	1
BIF_DEBUG_ACCESS	GPIO4	Debug signals muxed out.	0
ROMIDCFG(0:3)	GPIO[11:13,9]	Memory aperture type	X X X X

X = DESIGN DEPENDANT  
 0 = DO NOT INSTALL RESISTOR  
 1 = INSTALL 10K RESISTOR

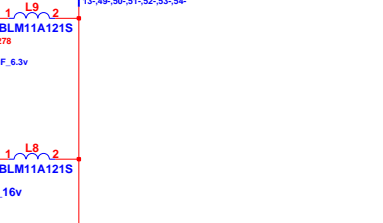
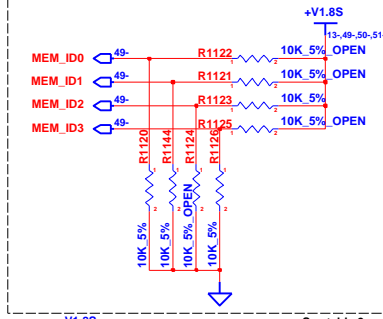
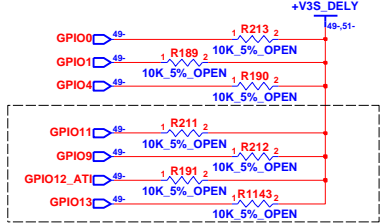
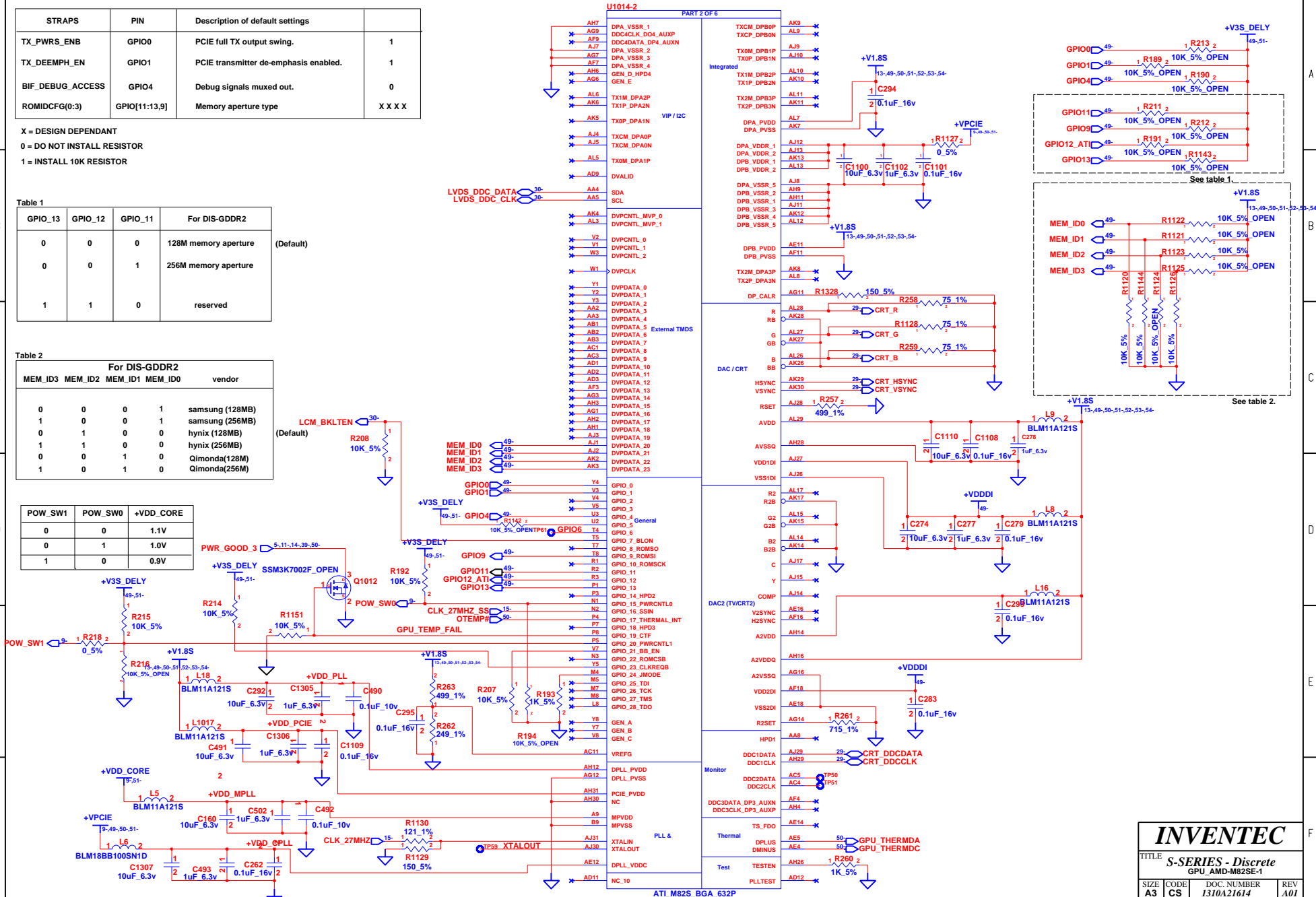
Table 1

GPIO_13	GPIO_12	GPIO_11	For DIS-GDDR2
0	0	0	128M memory aperture (Default)
0	0	1	256M memory aperture
1	1	0	reserved

Table 2

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	vendor
0	0	0	1	samsung (128MB)
1	0	0	1	samsung (256MB)
0	1	0	0	hynix (128MB)
1	1	0	0	hynix (256MB)
0	0	1	0	Qimonda(128MB)
1	0	1	0	Qimonda(256M)

POW_SW1	POW_SW0	+VDD_CORE
0	0	1.1V
0	1	1.0V
1	0	0.9V

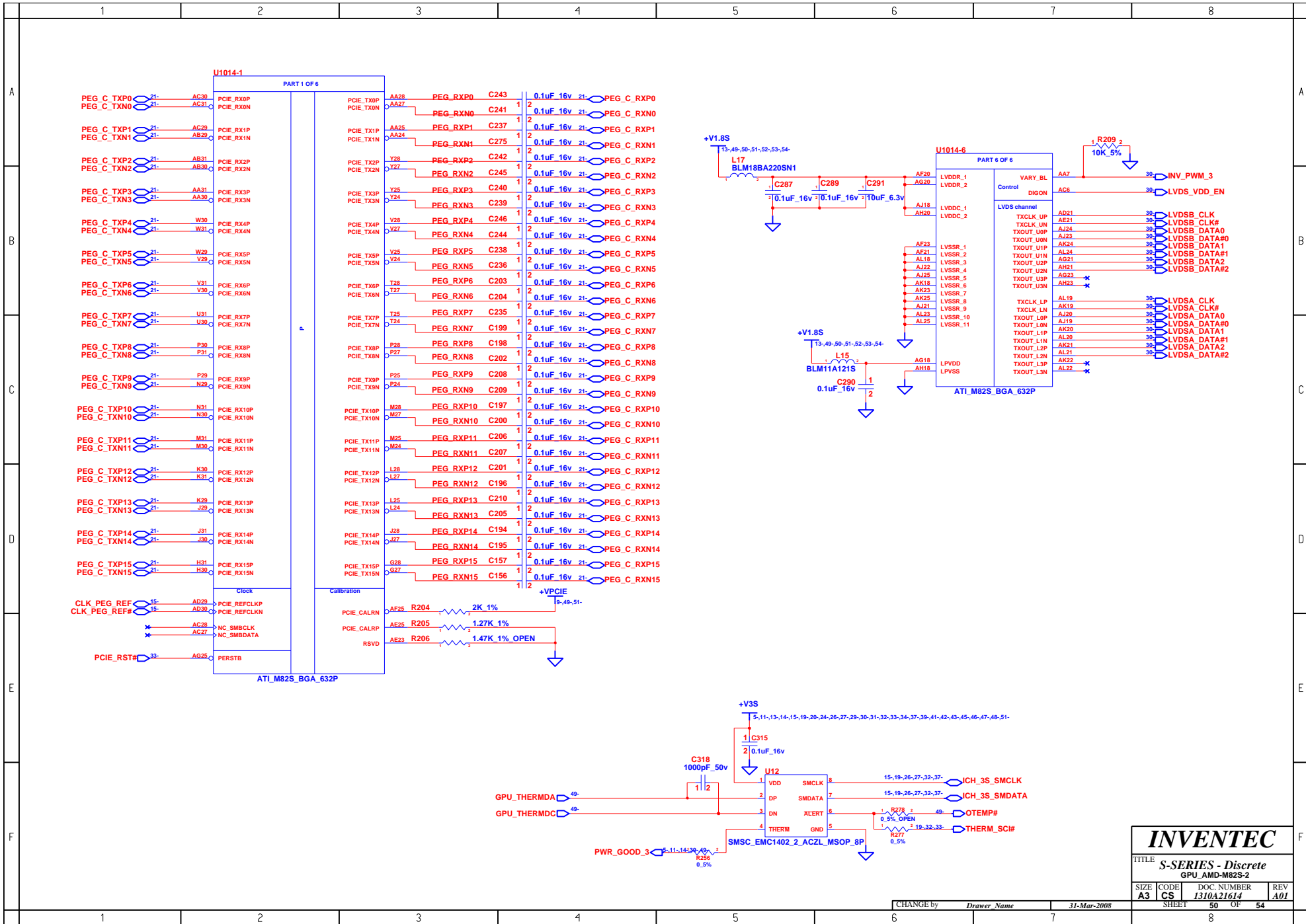


**INVENTEC**

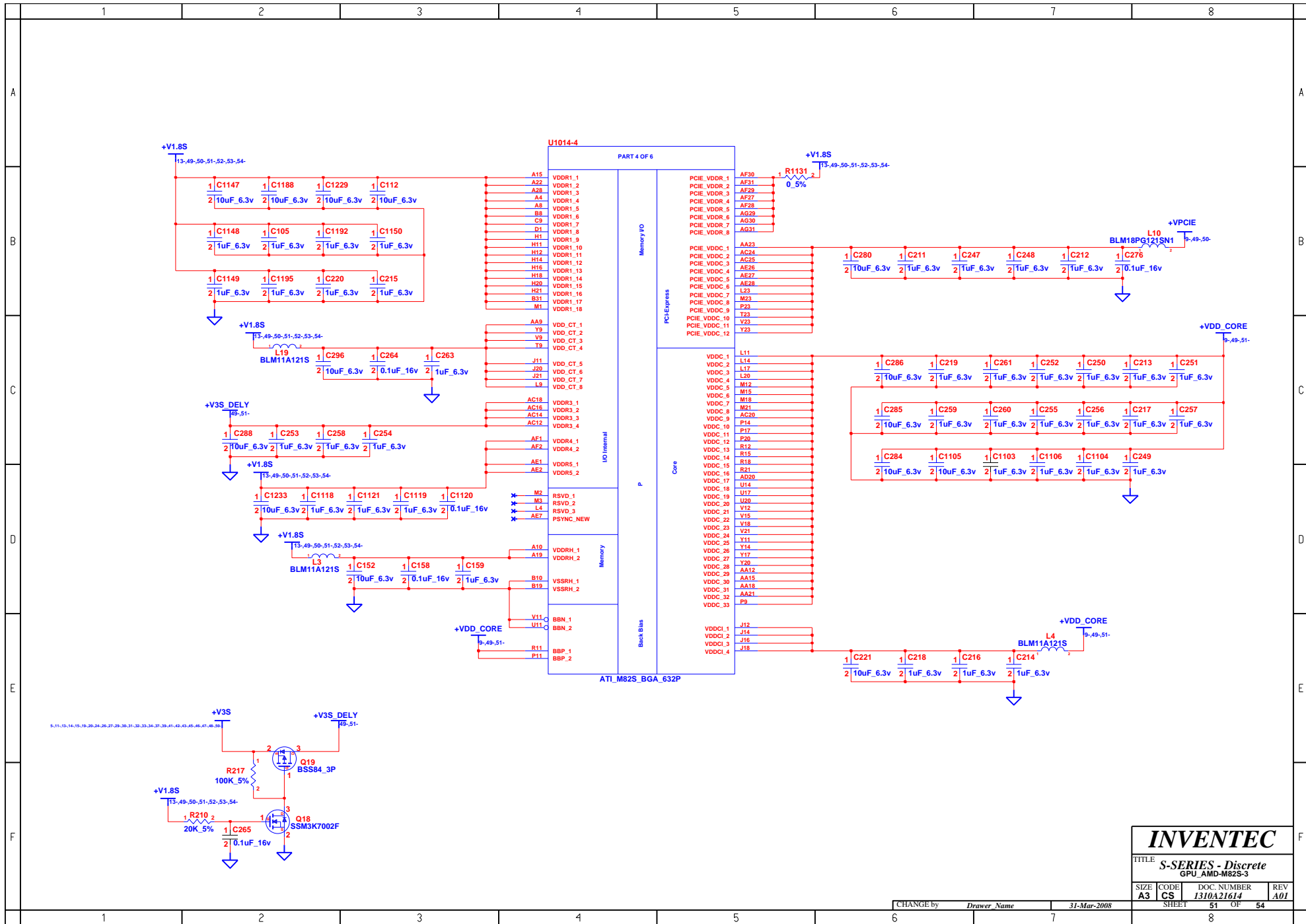
TITLE: S-SERIES - Discrete GPU\_AMD-M82SE-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01

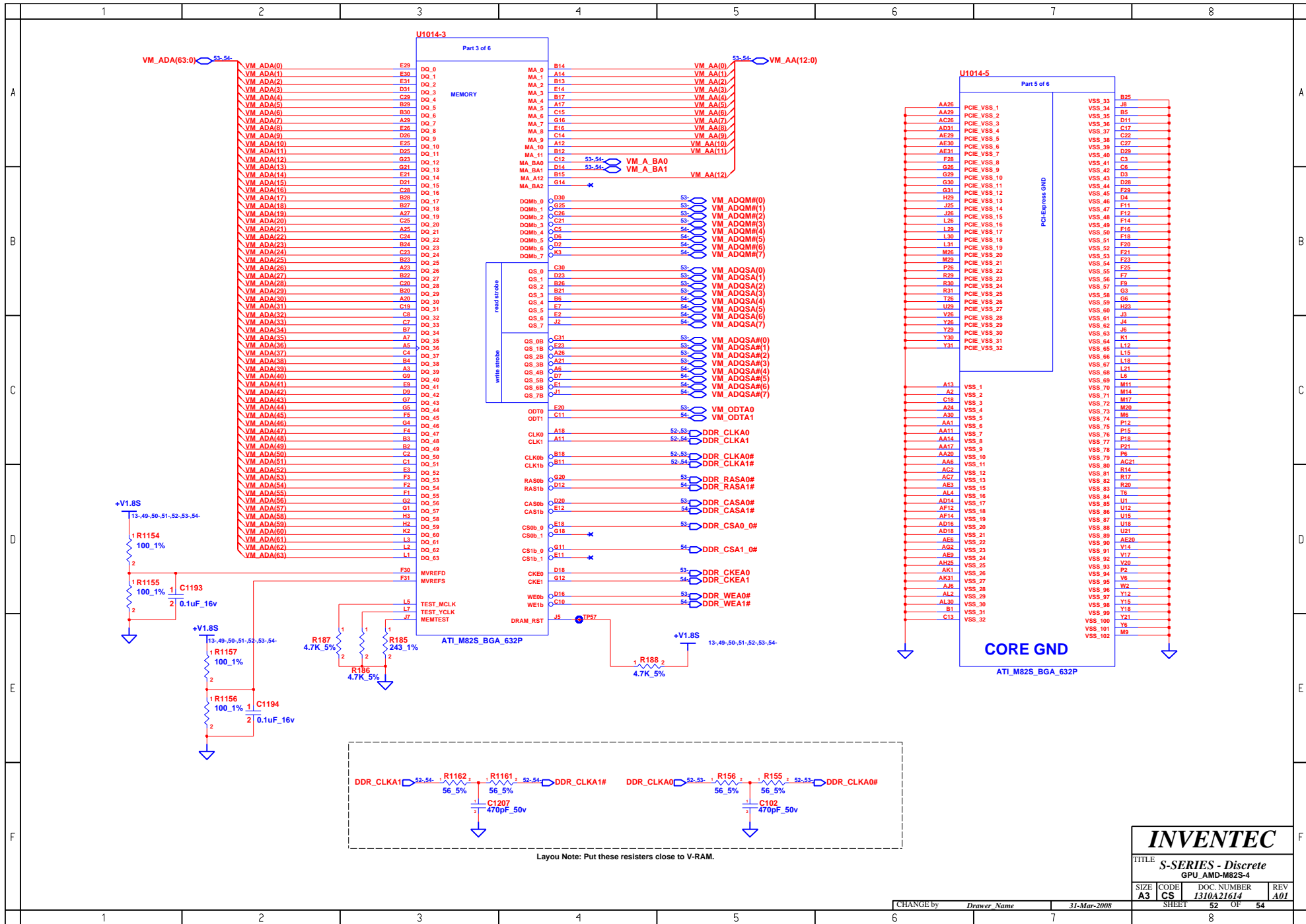
SHEET 49 OF 54



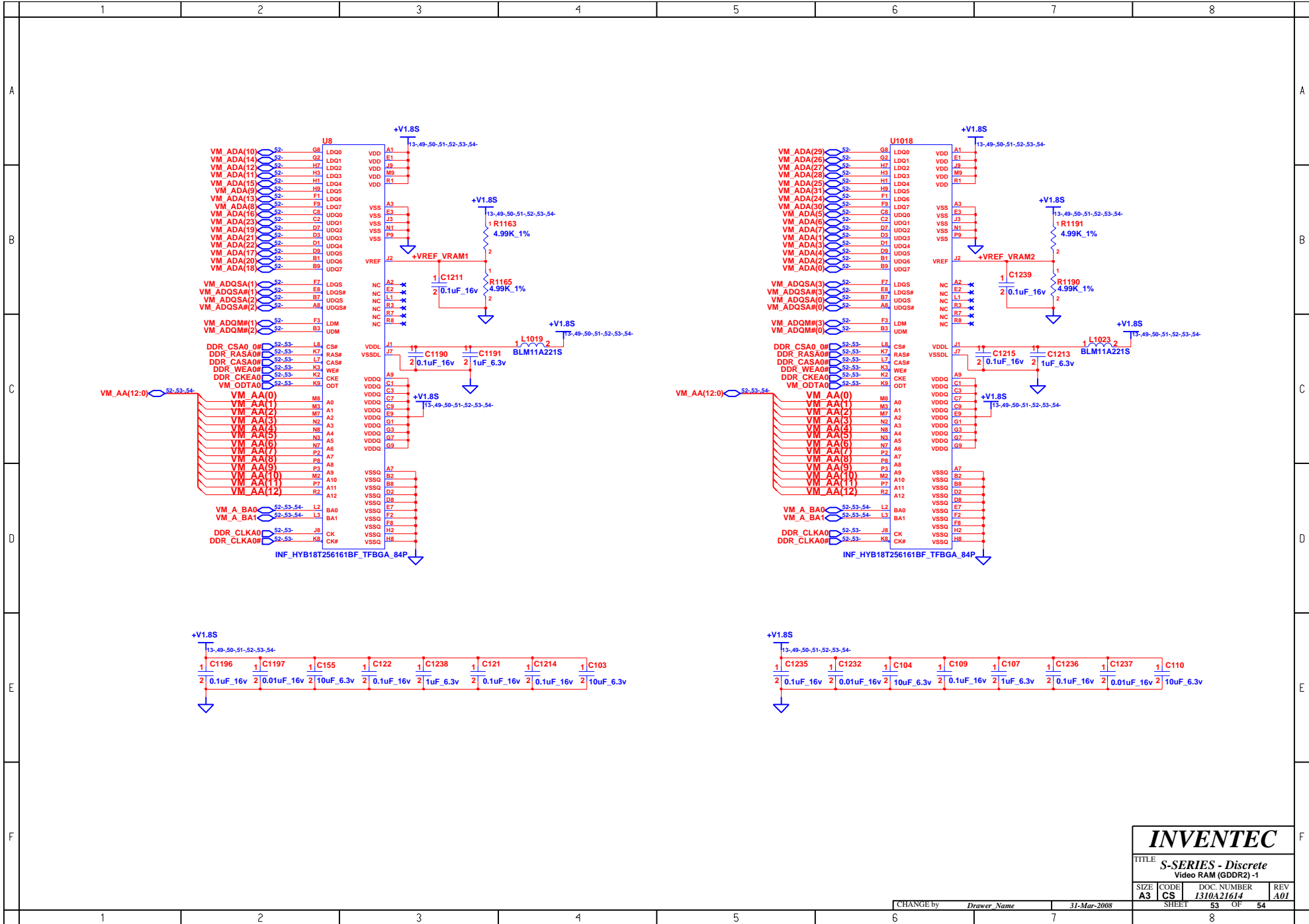
<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete</b> GPU_AMD-M825-2			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC NUMBER <b>1310A21614</b>	REV <b>A01</b>
CHANGE by <i>Drawer Name</i>		31-Mar-2008	
SHEET <b>50</b>		OF <b>54</b>	



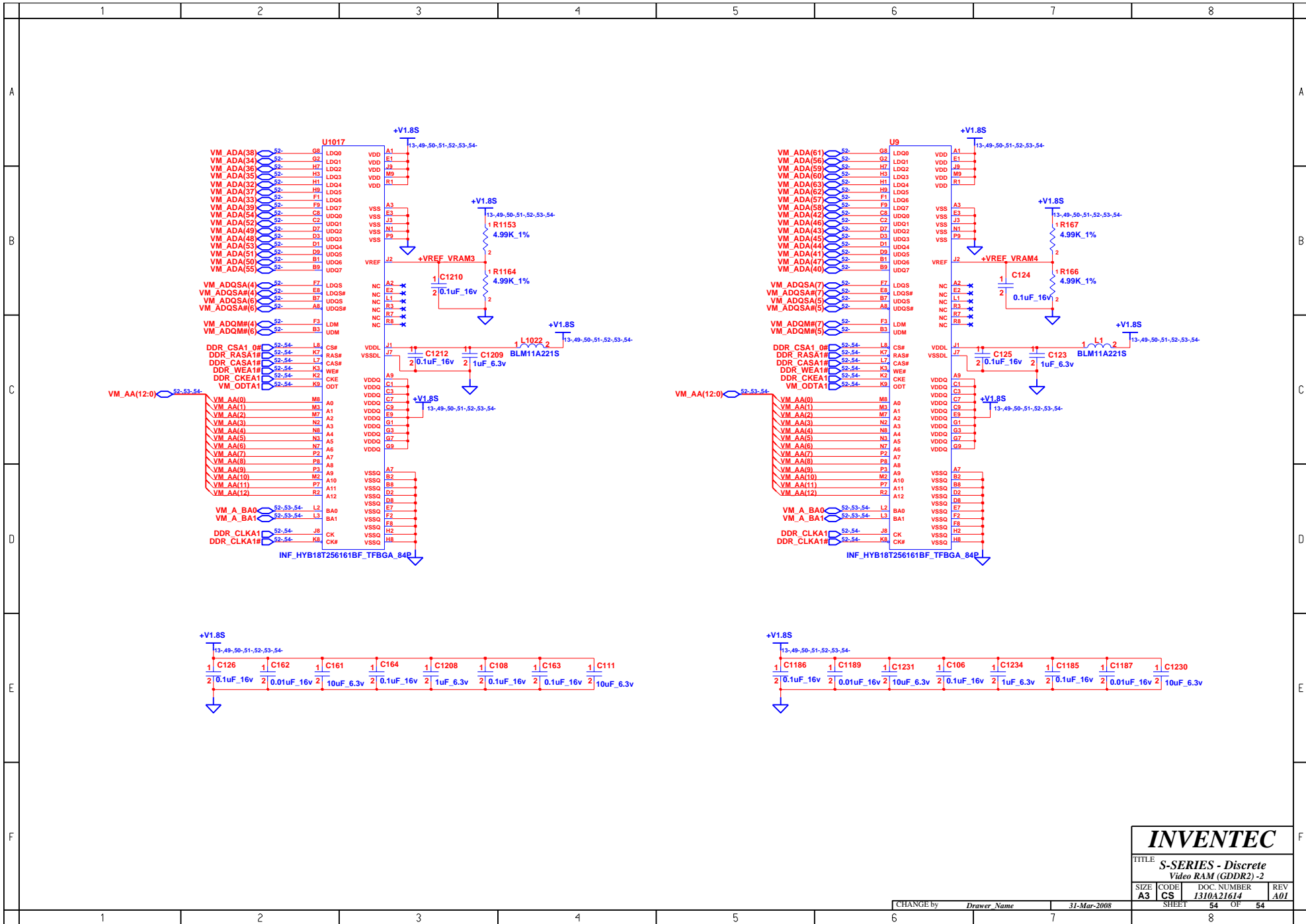
<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete</b>			
GPU_AMD-M82S-3			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A21614	A01
CHANGE by		Drawer Name	31-Mar-2008
SHEET		51	OF 54



<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete</b> GPU_AMD-M82S-4			
SIZE <b>A3</b>	CODE <b>CS</b>	DOC. NUMBER <b>1310A21614</b>	REV <b>A01</b>
CHANGE by <i>Drawer Name</i>		31-Mar-2008	
SHEET		52 OF 54	



<b>INVENTEC</b>			
TITLE <b>S-SERIES - Discrete</b>			
Video RAM (GDDR2) -1			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01
CHANGE by		Drawer Name	31-Mar-2008
SHEET		53	OF 54



# INVENTEC

TITLE  
**S-SERIES - Discrete**  
 Video RAM (GDDR2) -2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A21614	A01

CHANGE by *Drawer Name* 31-Mar-2008

SHEET 54 OF 54