1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

GILA
EVT1

11/21/03

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

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13*	11	SMU	
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22	17	U3LITE CORE	
23	18	SHASTA CORE	
24	19	U3LITE MISC	
25*	20	SHASTA SERIAL	
26	21	PULSAR POWER	
27	22	PULSAR CLOCKS	
28*	23	U3LITE APPLE PI	PROCESSOR
29	24	NEO APPLE PI	
30	25	CPU STRAPS	
31	26	NEO POWER & BYPASS	
32	27	CPU BYPASS	
33	28	CPU VREG	
34	29	CPU VREG	
35	30	CPU VREG OUTPUT CAPS	
36	31	CPU DIODE CONDITIONER	
37*	32	U3LITE MEMORY	MEMORY
38	33	SERIES TERMINATION	
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45	36	PARALLEL TERMINATION	
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50	40	GPU VREG	
51	41	EXTERNAL TMDS TRANSMITTER	
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54	44	GRAPHICS DDR SDRAM A	
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59	49	EXT VGA & TMDS	
60*	50	U3LITE HYPERTRANSPORT	HT
62*	51	SHASTA HYPERTRANSPORT	
64	52	HYPERTRANSPORT LA CONNECTORS	
74*	53	SHASTA PCI	PCI
75*	54	BOOT ROM	
76	55	AIRPORT EXTREME	
77*	56	USB2 PCI	
80*	57	SHASTA DISK	DISK
83	58	DISK CONNECTORS	
84*	59	SHASTA ETHERNET	ETHERNET
87	60	ETHERNET PHY & CONNECTORS	
88*	61	SHASTA FIREWIRE	FIREWIRE
90	62	FIREWIRE A PHY & CONNECTORS	
91*	63	USB HOST INTERFACE	USB
92	64	USB DEVICE INTERFACE	
94	65	MODEM CONNECTOR	MODEM
95*	66	AUDIO CODEC, LINE IN, MIC IN	AUDIO
96*	67	HEADPHONE / LINE OUT	
97*	68	SPEAKER AMP	
98*	69	AUDIO CONNECTORS	
99*	70	AUDIO POWER SUPPLIES	

* PAGES WHERE MASTER PAGE IS IN A DIFFERENT SCHEMATIC

DIMENSIONS ARE IN MILLIMETERS
XX ± ____
X.XX ± ____
X.XXX ± ____
ANGLES ± ____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCH,MLB,GILA

DRAWING NUMBER 051-6482 REV. 13

SHT 1 OF 99

FREQUENCIES LISTED ARE MAXIMUM DATA TRANSFER RATES SUPPORTED BY U3LITE

U2900
CPU
NEO 10S
PAGE 29

32-BIT
APPLE PI
ELASTIC INTERFACE
1.2V/900MHZ

U1300
SMU
PAGE 13

U1301
RTC
PAGE 13

J5900, J5901
J5902, J5903
17",20" INVERTER
TMDS
EXT VGA
PAGE 59

U5400, U5401
FRAME
BUFFER A
PAGE 54

64-BIT
FRAME BUFFER
2.6V/540MHZ

U4900
GPU
NV18B/NV34
PAGE 49

32-BIT
8X AGP
0.8V/533MHZ
4X = 1.5V
I/O = 1.5V

APPLE PI
PAGE 28

AGP
PAGE 48

U3
U3LITE
CORE
PAGE 22

MAIN MEMORY
PAGE 37

64/128-BIT
MAIN MEMORY
2.6V/400MHZ
333MHZ SUPPORTED

SERIES
TERM
PAGE 38

J4000
J4001
DIMMS
PAGE 40

PARALLEL
TERM
PAGES 44&45

64-BIT
FRAME BUFFER
2.6V/540MHZ

U5500, U5501
FRAME
BUFFER B
PAGE 55

MISC
PAGE 24

HYPERTRANSPORT
PAGE 60

8-BIT
HYPERTRANSPORT
1.2V/400MHZ
CONTROL = 2.5V

U2600
PULSAR
POWER
PAGE 26
CLOCKS
PAGE 27

I2C
PAGE 18

J6400
J6401
J6402
HT
DEBUG
PAGE 64

J9210/J9220/J9230
USB
CONNECTORS
PAGE 92

J9400
MICRODASH MODEM
CONNECTOR
PAGE 94

To Shasta
SCCA

J9240
BLUETOOTH
CONNECTOR
PAGE 92

USB
PAGE 91

U7700
USB 2.0
uPD720101
PCI
PAGE 77

U7500
BOOTROM
PAGE 75

J7600
AIRPORT
EXTREME
CONNECTOR
PAGE 76

EDUCATION: NOT USED
GOOD,BETTER,BEST: HARD DRIVE

JXXXX
SATA
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

HYPERTRANSPORT
PAGE 62

U2300

PCI
PAGE 74

32-bit PCI (5V-3.3V/33MHz)

SATA
PAGE 80
SATA1

FOR DEVELOPMENT ONLY

J8302
SATA DEV
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

SATA2

SHASTA

GPIO/PCI64
PAGE 25

EDUCATION: HARD DRIVE
GOOD,BETTER,BEST: OPTICAL

J8301
UATA
CONNECTOR
PAGE 83

UATA/133
3.3V/133MHZ

UATA
PAGE 80

CORE
PAGE 23

NCS
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J9401
CTL-LESS /
SOFT MODEM
CONNECTOR
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ETHERNET
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FIREWIRE
PAGE 88

I2S
PAGE 25
SCCA
I2S1
SCCB
I2S2
I2S0

GMII (3.3V/125MHz) 8-BIT TX & 8-BIT RX

1394 PHY (3.3V/98MHz)

U9500
AUDIO CODEC
PCM3052
PAGE 95

S/PDIF

OPTICAL OUT

J9803
COMBO OUT
CONNECTOR
PAGE 98

LINE OUT
AMP
PAGE 97

LINE OUT

SPEAKER
AMP
PAGE 97

J9801
SPEAKER
CONNECTOR
PAGE 98

LINE IN
AMP
PAGE 97

U8700
10/100 ETHERNET
BCM5221
PAGE 87

U9000
FIREWIRE A
802A
PAGE 90
0 1

4 Diff pairs

2 Diff pairs

J8700
ETHERNET
CONNECTOR
PAGE 87

J9000, J9001
FIREWIRE A
CONNECTORS
PAGE 90

J9800
LINE IN
CONNECTOR
PAGE 98

J9802
MIC
CONNECTOR
PAGE 98

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE NONE

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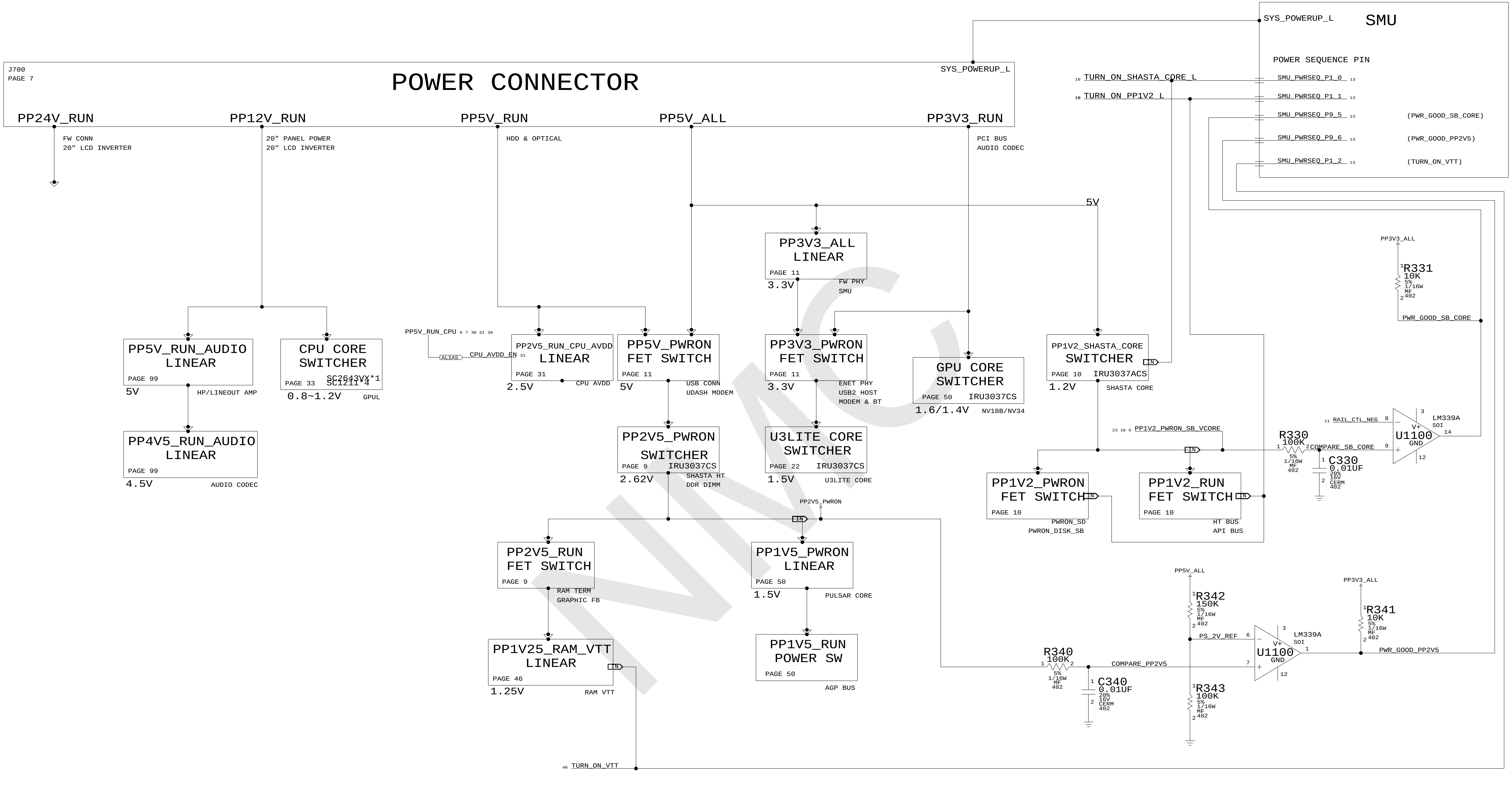

SMU
SYS_POWERUP_L
POWER SEQUENCE PIN
TURN_ON_SHASTA_CORE_L
TURN_ON_PP1V2_L
SMU_PWRSEQ_P1_0
SMU_PWRSEQ_P1_1
SMU_PWRSEQ_P9_5
SMU_PWRSEQ_P9_6
SMU_PWRSEQ_P1_2
(PWR_GOOD_SB_CORE)
(PWR_GOOD_PP2V5)
(TURN_ON_VTT)
J700
PAGE 7
POWER CONNECTOR
PP24V_RUN
PP12V_RUN
PP5V_RUN
PP5V_ALL
PP3V3_RUN
FW CONN
20" LCD INVERTER
20" PANEL POWER
20" LCD INVERTER
HDD & OPTICAL
PCI BUS
AUDIO CODEC
5V
PP3V3_ALL LINEAR
PAGE 11
3.3V
FW PHY
SMU
PP5V_RUN_AUDIO LINEAR
PAGE 99
5V
HP/LINEOUT AMP
CPU CORE SWITCHER
PAGE 33
SC2643VX*1
SC1211*4
0.8~1.2V
GPUL
PP5V_RUN_CPU
CPU_AVDD_EN
ALIAS
PP2V5_RUN_CPU_AVDD LINEAR
PAGE 31
2.5V
CPU AVDD
PP5V_PWRON FET SWITCH
PAGE 11
5V
USB CONN
UDASH MODEM
PP3V3_PWRON FET SWITCH
PAGE 11
3.3V
ENET PHY
USB2 HOST
MODEM & BT
GPU CORE SWITCHER
PAGE 50
IRU3037CS
1.6/1.4V
NV18B/NV34
PP1V2_SHASTA_CORE SWITCHER
PAGE 10
IRU3037ACS
1.2V
SHASTA CORE
PP4V5_RUN_AUDIO LINEAR
PAGE 99
4.5V
AUDIO CODEC
PP2V5_PWRON SWITCHER
PAGE 9
IRU3037CS
2.62V
SHASTA HT
DDR DIMM
U3LITE CORE SWITCHER
PAGE 22
IRU3037CS
1.5V
U3LITE CORE
PP1V2_PWRON_SB_VCORE
PP1V2_PWRON FET SWITCH
PAGE 10
PWRON_SD
PWRON_DISK_SB
PP1V2_RUN FET SWITCH
PAGE 10
HT BUS
API BUS
PP3V3_ALL
R331
10K
PWR_GOOD_SB_CORE
RAIL_CTL_NEG
LM339A
SOI
U1100
R330
100K
COMPARE_SB_CORE
C330
0.01UF
PP2V5_PWRON
PP2V5_RUN FET SWITCH
PAGE 9
RAM TERM
GRAPHIC FB
PP1V5_PWRON LINEAR
PAGE 50
1.5V
PULSAR CORE
PP1V25_RAM_VTT LINEAR
PAGE 46
1.25V
RAM VTT
PP1V5_RUN POWER SW
PAGE 50
AGP BUS
PP5V_ALL
R342
150K
PS_2V_REF
R341
10K
PWR_GOOD_PP2V5
R340
100K
COMPARE_PP2V5
C340
0.01UF
R343
100K
TURN_ON_VTT

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE NONE	SHT 3 OF 99	

DATE	DESCRIPTION
10/08/03	PROTO RELEASE (REV 09)
10/13/03	CHANGED ALL 4 NB AVDDS TO PP1V5_PWRON_NB_AVDD RAIL TERMINATION FOR VSP CLOCK NOW TRACKS PP1V2_HT RAIL TERMINATION FOR NB CLOCK NOW TRACKS PP1V2_EI_NB RAIL TERMINATION FOR CPU CLOCK NOW TRACKS PP1V2_EI_CPU RAIL NO STUFFED R1303 BECAUSE WHITE LED IS ACTIVE HIGH ADDED 5 PULLDOWNS FOR CPU VID SIGNALS UNCONNECTED THERMAL PAD FOR U9600 HEADPHONE AMP CHECKIN 09001
10/14/03	ADDED 4 SMT NUTS U3600 PIN 6 TO PP5V_RUN CHECKIN 09002
10/15/03	SWAPPED EI_CPU_TO_NB_AD17 WITH EI_CPU_TO_NB_AD24 ON J1400 BOM CHANGES FOR R2910, R5727, R9139, R9810 MAIN PROTO RELEASE (REV 10)
11/03/03	REPINNED J9240 BLUETOOTH CONNECTOR MANY MIN_NECK_WIDTH UPDATES DC-DC UPDATES ON PAGES 9,10,22,33,34,50 NEW CONNECTORS FOR MODEM AND PATA ADDED GAP FILLER CHANGED PART NUMBER OF NV18B MOVED SERIES TERM FOR PULSAR CLOCKS TO LOGIC ANALYZER PAGE ADDED NET_SPACING_TYPE=PROC_DIFF TO TDIODE_POS, TDIODE_NEG, KPVDD2, AND KPGND2 CHANGED PULSAR 2.2UF CAPS TO 10% MASTER PAGE SYNC CHECKIN 10001
11/04/03	NEW AIRPORT CONNECTOR ADDED LEDS FOR 5V ALL RAIL AND PANEL POWER CHANGED DS870X TO LED870X TO FOLLOW CONVENTION REPLACED POWER CONNECTOR MASTER PAGE SYNC RELEASE REV 11
11/10/03	J8301 PATA CONNECTOR ROTATED 180 DEGREES MIN_LINE_WIDTH AND MIN_NECK_WIDTH UPDATES THROUGHOUT ADDED EMI-SPRING AND TIED TO GND_CHASSIS_MODEM UPDATED CRYSTAL CONSTRAINTS FIREWIRE NET NAME CHANGES TO MATCH NAMING CONVENTION CHANGED Q1001 TO NTD60N02R CHANGED PULSAR SERIES TERM R2707, R2719, R2701, R2761, R2779 TO 0 OHM CHANGED ZH700 AND ZH701 TO HOL-315R138 CHANGED 20" INVERTER TO 518-0141 CHANGED U3LITE P/N TO V1.1 MASTER PAGE SYNC CHECKIN 11001
11/11/03	PLL-LOCK LED CHANGED TO GREEN SMU PART# UPDATED DC/DC NET NAME FIXES ON PAGES 9,10,22 ADDED SERIAL SIGNALS TO AIRPORT CARD FOR NEW MARTY CARD PULSAR SERIES TERM - CHANGED R2705,R2711,R2702 TO 0 OHM. R2770 -> 20 OHM CHANGED SHASTA P/N TO V1.1 UPDATED POWER SEQUENCING TO MATCH SMU PINOUT 1.4 NO_TEST UPDATES ADDED 6 OUTPUT CAPS (124-0322) TO CPU VCORE VREG MASTER PAGE SYNC CHECKIN 11002 - EVT DESIGN REVIEW
11/13/03	CHANGED CRYSTAL Y5700 TO 197S0026 LED3002, LED3600, AND LED800 CHANGED TO D3002, D3610, AND D810 P/N 378S0042 CPU POWER SUPPLY FETS - VISHAY USED ON SAMSUNG BOMS AND ON SEMI ON HYNIX BOMS CHANGED INPUT CAPS TO 124-0323 INPUT AND OUTPUT CERM CAPS MARKED AS CRITICAL NEW LARGER CAP FOR VTT VREG. C4609 CHANGED TO 128S0022. C4608 NOSTUFFED BOMOPTIONS AND SCHEMATIC CLEANUP TO AGP (BUSY, STOP, TYPEDET, GCDET) CHANGED 20" INVERTER DECOUPLING TO TWO 1UF 1210 CAPS ADDED MORE POWER AND GROUND SHORTS FOR AUDIO ADDED NET_SPACING_TYPE=PROC_DIFF TO DIFF PAIRS THAT DIDN'T HAVE IT MASTER PAGE SYNC RELEASE REV 12
11/14/03	CHANGED PCI_CLK33M_SB_EXT NET NAME ON PAGE 27 FOR REUSE. ALIAS ADDED ON PAGE 8 ADDED ECSET FOR PLS_EXTCLK NET. DROPPED PROP DELAY FROM OTHER CRYSTALS ALIASED PP5V_AUDIO TO PP5V_RUN RAIL ADDED CIRCUIT SO 5V RAIL TO 17" INVERTER COMES UP AFTER 12V R2742 CHANGED TO 806 OHM MASTER PAGE SYNC CHECKIN 12001
11/15/03	CHANGED J8303 TO 5 PIN CONNECTOR CHANGED MICRODASH MODEM HEIGHT AND CHANGED TO DEVELOPMENT BOM OPTION
11/17/03	PIN SWAPPED L5908 FOR ROUTING STUFFED TMDS INDUCTORS AND NOSTUFFED 0 OHM RESISTORS CHANGED MODEM STANDOFFS TO 862-0035 AND ADDED ELECTRICAL CONNECTIONS ADDED TWO MORE SMT NUTS FOR CPU HEATSINK CHANGED LED700,701,702,5900,8301,8700,8701,8702 AND D3001 TO 378S0045 MASTER PAGE SYNC CHECKIN 12002
11/17/03	NO_TEST, FUNC_TEST UPDATES CHECKIN 12003
11/18/03	CHASSIS MODEM NO LONGER TIES TO REST OF CHASSIS ADDED CAPS TO GROUND FOR CPU HEATSINK SMT NUTS CHANGED CRYSTAL FILTERING FOR PULSAR MOVED RAM_CKE SIGNALS TO 62 OHM VTT PARALLEL TERM WITH 4.7K PULL-DOWN ADDED POWER SEQUENCING FOR VTT VREG MASTER PAGE SYNC CHECKIN 12004
11/19/03	STUFFING CHANGES FOR ETHERNET RESET CHANGED XW3302 TO LAYER 6 SHORT POWER BUTTON CONNECTOR SYMBOL UPDATED UPDATED CRITICAL LIST CHANGE Y5700 TO 4 PIN CRYSTAL CHECKIN 12005
11/20/03	CHANGED R2700 TO 22OHM AND NOSTUFFED CPU VID SET TO 1.475V J1400 CHANGED TO NOSTUFF CHANGED HALF OF DIMM AND VTT DECOUPLING TO 1UF EVT1 RELEASE (REV 13)

REVISION HISTORY

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6482 | REV. 13

SCALE NONE | SHT 4 OF 99

	NO_TEST=TRUE	TP_BUF_RST	57
	NO_TEST=YES	TP_DFPCLK	58
L3	NO_TEST=YES	TP_DFPCLK_L	58
L4	NO_TEST=TRUE	TP_DFPD0	58
L5	NO_TEST=TRUE	TP_DFPD1	58
L6	NO_TEST=TRUE	TP_DFPD2	58
L7	NO_TEST=YES	TP_DFPD3	58
L8	NO_TEST=TRUE	TP_DFPD5	58
L9	NO_TEST=YES	TP_DFPD6	58
L10	NO_TEST=YES	TP_EXT_TMDS_CKM	58
L20	NO_TEST=TRUE	TP_EXT_TMDS_CKP	58
L20	NO_TEST=YES	TP_EXT_TMDS_D0M	58
L20	NO_TEST=YES	TP_EXT_TMDS_D0P	58
L20	NO_TEST=YES	TP_EXT_TMDS_D1M	58
L30	NO_TEST=YES	TP_EXT_TMDS_D1P	58
L20	NO_TEST=YES	TP_EXT_TMDS_D2M	58
L30	NO_TEST=YES	TP_EXT_TMDS_D2P	58
L30	NO_TEST=TRUE	TP_FBBCS1_L	52
L31	NO_TEST=TRUE	TP_GPU_INTB_L	49
L31	NO_TEST=TRUE	TP_GPU_THERMA	58
L31	NO_TEST=TRUE	TP_GPU_THERMC	58
L31	NO_TEST=TRUE	TP_IFP1VREF	58
L31	NO_TEST=TRUE	TP_NVAGP_TDO	49
L32	NO_TEST=YES	TP_TMDS_TXD3M	58
L31	NO_TEST=YES	TP_TMDS_TXD3P	58
L32	NO_TEST=TRUE	TP_TMDS_TXD7M	58
L32	NO_TEST=YES	TP_TMDS_TXD7P	58
L32	NO_TEST=TRUE	TP_VIPHCLK	57
L33	NO_TEST=YES	TP_FRWRLPS	58
L33	NO_TEST=TRUE	TP_AGP_MB_AGP8X_DET_L	48
L33	NO_TEST=TRUE	TP_ATTENTION	29
L34	NO_TEST=TRUE	TP_ENET_CLK125M_GTX	87
L33	NO_TEST=TRUE	TP_ENET_TXD<7>	87
L34	NO_TEST=TRUE	TP_ENET_TXD<4>	87
L34	NO_TEST=TRUE	TP_ENET_TXD<5>	87
L34	NO_TEST=TRUE	TP_FW_CLK98M_LCLK	90
L34	NO_TEST=TRUE	TP_AFN	29
L34	NO_TEST=TRUE	TP_PSRO1	29
L34	NO_TEST=TRUE	TP_PSRO2	29
L34	NO_TEST=TRUE	TP_PSYNCOUT	29
L34	NO_TEST=TRUE	TP_USB2_PWREN<2>	92
L35	NO_TEST=TRUE	TP_USB2_PWREN<3>	92
L34	NO_TEST=TRUE	TP_USB2_PWREN<4>	92
L35	NO_TEST=TRUE	TP_PROC_TRIGGER_OUT	14 29
L35	NO_TEST=TRUE	TP_NEC_AMC	77
L35	NO_TEST=TRUE	TP_NEC_NANDTEST	77
L35	NO_TEST=TRUE	TP_NEC_NTEST1	77
L35	NO_TEST=TRUE	TP_NEC_SMC	77
L35	NO_TEST=TRUE	TP_NEC_SMI_L	77
L36	NO_TEST=TRUE	TP_NEC_SRCLK	77
L35	NO_TEST=TRUE	TP_NEC_SRDATA	77
L36	NO_TEST=TRUE	TP_NEC_SRMOD	77
L36	NO_TEST=TRUE	TP_NEC_TEB	77
L36	NO_TEST=TRUE	TP_NEC_TEST	77
L36	NO_TEST=TRUE	TP_PLS_CLK_66M_0	27
L36	NO_TEST=TRUE	TP_PLS_CLK_66M_1	27
L37	NO_TEST=TRUE	TP_PLS_REF_CML	27
L37	NO_TEST=TRUE	TP_PLS_TEST1	27
L37	NO_TEST=TRUE	TP_PLS_TEST2	27
L37	NO_TEST=TRUE	TP_PLS_TEST3	27
L37	NO_TEST=TRUE	TP_SB_FSTEST	25
L37	NO_TEST=TRUE	TP_SB_PLLTEST	25
L37	NO_TEST=TRUE	TP_VREF_CG	48
L37	NO_TEST=TRUE	TP_SB_NC_P7	91
L38	NO_TEST=TRUE	TP_SB_NC_P8	91
L37	NO_TEST=TRUE	TP_SB_NC_R3	91
L38	NO_TEST=TRUE	TP_SB_NC_R4	91
L38	NO_TEST=TRUE	TP_SB_NC_R5	91
L38	NO_TEST=TRUE	TP_SB_NC_R6	91
L38	NO_TEST=TRUE	TP_SB_NC_R7	91
L38	NO_TEST=TRUE	TP_SB_NC_R8	91
L38	NO_TEST=TRUE	TP_SB_NC_T1	91
L38	NO_TEST=TRUE	TP_SB_NC_T2	91
L38	NO_TEST=TRUE	TP_SB_NC_T3	91
L39	NO_TEST=TRUE	TP_SB_NC_T4	91
L38	NO_TEST=TRUE	TP_SB_NC_T5	91
L39	NO_TEST=TRUE	TP_SB_NC_T6	91
L39	NO_TEST=TRUE	TP_SB_NC_T7	91
L39	NO_TEST=TRUE	TP_SB_NC_T8	91
L39	NO_TEST=TRUE	TP_SB_NC_U1	91
L39	NO_TEST=TRUE	TP_SB_NC_U2	91
L39	NO_TEST=TRUE	TP_SB_NC_U3	91
L39	NO_TEST=TRUE	TP_SB_NC_U4	91
L39	NO_TEST=TRUE	TP_SB_NC_U5	91
L39	NO_TEST=TRUE	TP_SB_NC_U6	91
L40	NO_TEST=TRUE	TP_SB_NC_V1	91
L40	NO_TEST=TRUE	TP_SB_NC_V2	91
L40	NO_TEST=TRUE	TP_SB_NC_V3	91
L40	NO_TEST=TRUE	TP_SB_NC_V4	91
L40	NO_TEST=TRUE	TP_SB_NC_W1	91
L40	NO_TEST=TRUE	TP_SB_NC_W3	91
L40	NO_TEST=TRUE	TP_SB_NC_Y1	91
L40	NO_TEST=TRUE	TP_SB_NC_Y3	91
L40	NO_TEST=TRUE	TP_SATA_CLK25M	27
L42	NO_TEST=TRUE	TP_ENET_TCK	87
L42	NO_TEST=TRUE	TP_USB2_PWREN<0>	92
L42	NO_TEST=TRUE	TP_USB2_PWREN<1>	92
L43	NO_TEST=TRUE	TP_DUMMY_A	24
L43	NO_TEST=TRUE	TP_DUMMY_B	24
L43	NO_TEST=TRUE	TP_RAM_CKE_R<2>	37
L43	NO_TEST=TRUE	TP_RAM_CKE_R<3>	37
L43	NO_TEST=TRUE	TP_RAM_CKE_R<6>	37
L43	NO_TEST=TRUE	TP_RAM_CKE_R<7>	37
L43	NO_TEST=TRUE	TP_RAM_CS_L_R<10>	37
L43	NO_TEST=TRUE	TP_RAM_CS_L_R<11>	37
L43	NO_TEST=TRUE	TP_RAM_CS_L_R<2>	37
L43	NO_TEST=TRUE	TP_RAM_CS_L_R<3>	37
L44	NO_TEST=TRUE	TP_RAM_MUXEN0	37
L44	NO_TEST=TRUE	TP_RAM_MUXEN4	37
L44	NO_TEST=TRUE	TP_NB_PM_SLEEP0	24
L44	NO_TEST=TRUE	TP_J4000_SJRESET_L	40
L44	NO_TEST=TRUE	TP_J4001_SJRESET_L	40
L44	NO_TEST=TRUE	TP_CMP_SPARE	36
L44	NO_TEST=TRUE	TP_ENET_TXD<6>	87
L78	NO_TEST=TRUE	U2100_UNUSED	21

90	IN	FW_VP_PORT1	FUNC_TEST=TRUE
90	IN	FW_TPO1P	FUNC_TEST=TRUE
90	IN	FW_TPO1N	FUNC_TEST=TRUE
90	IN	FW_TPI1P	FUNC_TEST=TRUE
90	IN	FW_TPI1N	FUNC_TEST=TRUE
90	IN	FW_VP_PORT2	FUNC_TEST=TRUE
90	IN	FW_TPO2P	FUNC_TEST=TRUE
90	IN	FW_TPO2N	FUNC_TEST=TRUE
90	IN	FW_TPI2P	FUNC_TEST=TRUE
90	IN	FW_TPI2N	FUNC_TEST=TRUE
90	IN	FW_VGND	FUNC_TEST=TRUE
77 76 75 74	IN	PCI_AD<31..0>	FUNC_TEST=TRUE
77 76 74	IN	PCI_CBE_L<3..0>	FUNC_TEST=TRUE
8	IN	PCI_CLK33M_AIRPORT	FUNC_TEST=TRUE
76 74	IN	PCI_SLOTA_REQ_L	FUNC_TEST=TRUE
76 74	IN	PCI_SLOTA_GNT_L	FUNC_TEST=TRUE
76 25	IN	PCI_SLOTA_INT_L	FUNC_TEST=TRUE
77 76 75 74 51 49	IN	PCI_RESET_L	FUNC_TEST=TRUE
77 76 74	IN	PCI_FRAME_L	FUNC_TEST=TRUE
77 76 74	IN	PCI_TRDY_L	FUNC_TEST=TRUE
77 76 74	IN	PCI_IRDY_L	FUNC_TEST=TRUE
77 76 74	IN	PCI_STOP_L	FUNC_TEST=TRUE
77 76 74	IN	PCI_DEVSEL_L	FUNC_TEST=TRUE
77 76 74	IN	PCI_PAR	FUNC_TEST=TRUE
76	IN	PCI_SLOTA_IDSEL	FUNC_TEST=TRUE
76 75 74	IN	ROM_CS_L	FUNC_TEST=TRUE
76 75 74	IN	ROM_OE_L	FUNC_TEST=TRUE
76 75 74	IN	ROM_WE_L	FUNC_TEST=TRUE
76 75	IN	ROM_ONBOARD_CS_L	FUNC_TEST=TRUE
76	IN	AIRPORT_CLKRUN_L_PD	FUNC_TEST=TRUE
92	IN	USB_BT_N	FUNC_TEST=TRUE
92	IN	USB_BT_P	FUNC_TEST=TRUE
92	IN	USB2_PORT1_N_F	FUNC_TEST=TRUE
92	IN	USB2_PORT1_P_F	FUNC_TEST=TRUE
92	IN	USB2_PORT2_N_F	FUNC_TEST=TRUE
92	IN	USB2_PORT2_P_F	FUNC_TEST=TRUE
92	IN	USB2_PORT3_N_F	FUNC_TEST=TRUE
92	IN	USB2_PORT3_P_F	FUNC_TEST=TRUE
92	IN	PP5V_USB2_PORT1_F	FUNC_TEST=TRUE
92	IN	PP5V_USB2_PORT2_F	FUNC_TEST=TRUE
92	IN	PP5V_USB2_PORT3_F	FUNC_TEST=TRUE
94 76 25	IN	I2S1_DEV_TO_SB_DTI 2 TEST POINTS	FUNC_TEST=TRUE
94 25	IN	I2S1_SYNC 2 TEST POINTS	FUNC_TEST=TRUE
94 25	IN	I2S1_BITCLK 2 TEST POINTS	FUNC_TEST=TRUE
94 25	IN	I2S1_MCLK 2 TEST POINTS	FUNC_TEST=TRUE
94 76 25	IN	I2S1_SB_TO_DEV_DTO 2 TEST POINTS	FUNC_TEST=TRUE
94 25	IN	I2S1_RESET_L 2 TEST POINTS	FUNC_TEST=TRUE
94 25	IN	MODEM_RING2SYS_L 2 TEST POINTS	FUNC_TEST=TRUE
94 18	IN	I2C_UDASH_SDA	FUNC_TEST=TRUE
94 18	IN	I2C_UDASH_SCL	FUNC_TEST=TRUE
94	IN	USB_UDASH_N	FUNC_TEST=TRUE
94	IN	USB_UDASH_P	FUNC_TEST=TRUE
94 25	IN	UDASH_SDOWN	FUNC_TEST=TRUE
94 25	IN	UDASH_RESET_L	FUNC_TEST=TRUE
94	IN	UDASH_I2C_A1_PU	FUNC_TEST=TRUE
59	IN	PPVCC_TMDS	FUNC_TEST=TRUE
59	IN	PP3V3_DDC	FUNC_TEST=TRUE
59	IN	TD0M	FUNC_TEST=TRUE
59	IN	TD0P	FUNC_TEST=TRUE
59	IN	TD1M	FUNC_TEST=TRUE
59	IN	TD1P	FUNC_TEST=TRUE
59	IN	TD2M	FUNC_TEST=TRUE
59	IN	TD2P	FUNC_TEST=TRUE
59	IN	TCKM	FUNC_TEST=TRUE
59	IN	TCKP	FUNC_TEST=TRUE
59	IN	TMDS_DDC_DAT	FUNC_TEST=TRUE
59	IN	TMDS_DDC_CLK	FUNC_TEST=TRUE
59 7	IN	GND_CHASSIS_TMDS	FUNC_TEST=TRUE
59	IN	FILT_ANALOG_RED	FUNC_TEST=TRUE
59	IN	FILT_ANALOG_GRN	FUNC_TEST=TRUE
59	IN	FILT_ANALOG_BLU	FUNC_TEST=TRUE
59 57 56	IN	ANALOG_HSYNC_L	FUNC_TEST=TRUE
59 57 56	IN	ANALOG_VSYNC_L	FUNC_TEST=TRUE
59	IN	VGA_IIC_CLK	FUNC_TEST=TRUE
59	IN	VGA_IIC_DAT	FUNC_TEST=TRUE
59 58	IN	MON_DETECT	FUNC_TEST=TRUE
59	IN	DDC_VCC_5	FUNC_TEST=TRUE
59	IN	PP24V_INV	FUNC_TEST=TRUE
59	IN	GND_20_INV	FUNC_TEST=TRUE
59	IN	INV_20_LCD_PWM	FUNC_TEST=TRUE
59	IN	INV_20_CUR_HI_F	FUNC_TEST=TRUE
59	IN	PP12V_INV	FUNC_TEST=TRUE
59	IN	GND_17_INV	FUNC_TEST=TRUE
59	IN	PP5V_AGP_RL	FUNC_TEST=TRUE
59	IN	INV_17_LCD_PWM_F	FUNC_TEST=TRUE
59	IN	LAMP_STS_F	FUNC_TEST=TRUE
59	IN	INV_17_CUR_HI_F	FUNC_TEST=TRUE
33 8	IN	CPU_VID_R<5..0>	FUNC_TEST=TRUE
36	IN	KPVDD2_FMAX	FUNC_TEST=TRUE
36	IN	KPGND2_FMAX	FUNC_TEST=TRUE
36	IN	TDIODE_POS_FMAX	FUNC_TEST=TRUE
36	IN	TDIODE_NEG_FMAX	FUNC_TEST=TRUE
36 33	IN	CORE_ISNS_M	FUNC_TEST=TRUE
36 33	IN	CORE_ISNS_P	FUNC_TEST=TRUE

PP12V_RUN PP5V_RUN PP24V_RUN PP5V_ALL PP3V3_RUN

	IN	PP12V_RUN 10 TEST POINTS	FUNC_TEST=TRUE
11 7	IN	PP5V_ALL 5 TEST POINTS	FUNC_TEST=TRUE
13	IN	PP5V_RUN 5 TEST POINTS	FUNC_TEST=TRUE
11	IN	PP3V3_RUN 5 TEST POINTS	FUNC_TEST=TRUE
	IN	PP24V_RUN 5 TEST POINTS	FUNC_TEST=TRUE
83 7	IN	PP5V_DISK 5 TEST POINTS	FUNC_TEST=TRUE
83 7	IN	PP12V_DISK 5 TEST POINTS	FUNC_TEST=TRUE
	IN	GND 12 TEST POINTS	FUNC_TEST=TRUE

PP2V5_RUN PP5V_PWRON PP1V2_PWRON PP1V5_RUN PP3V3_PWRON

	IN	PP2V5_RUN	FUNC_TEST=TRUE
	IN	PP1V5_RUN	FUNC_TEST=TRUE
18 13	IN	PP5V_PWRON	FUNC_TEST=TRUE
27 18 13	IN	PP3V3_PWRON	FUNC_TEST=TRUE
	IN	PP1V2_PWRON	FUNC_TEST=TRUE
23 10 9	IN	PP1V2_PWRON_SB_VCORE	FUNC_TEST=TRUE
	IN	PP3V3_ALL_SMU	FUNC_TEST=TRUE
36 31 30 7 3	IN	PP5V_RUN_CPU	FUNC_TEST=TRUE
22 7	IN	PPVCORE_NB	FUNC_TEST=TRUE
36 35 34 33 32 31 29 7	IN	PPVCORE_CPU	FUNC_TEST=TRUE
34 33	IN	PP12V_CPU	FUNC_TEST=TRUE
33	IN	VCORE_SENSE_GND	FUNC_TEST=TRUE
33	IN	VCORE_SENSE_VOUT	FUNC_TEST=TRUE
13 8 7	IN	SMU_MANUAL_RESET_L 2 TEST POINTS	FUNC_TEST=TRUE
13 7	IN	SYS_POWER_BUTTON_L 2 TEST POINTS	FUNC_TEST=TRUE
7	IN	POWER_BUTTON_L	FUNC_TEST=TRUE
7	IN	RESET_BUTTON_L	FUNC_TEST=TRUE
13 8	IN	SMU_RESET_L	FUNC_TEST=TRUE
33 13 11 10 7	IN	SYS_POWERUP_L	FUNC_TEST=TRUE
50 46 27 11 10 9 8	IN	SYS_SLEEP	FUNC_TEST=TRUE
13 8	IN	SYS_POWERFAIL_L	FUNC_TEST=TRUE
13	IN	EXT_POWER_BUTTON_L	FUNC_TEST=TRUE
9	IN	U900_FEEDBACK	FUNC_TEST=TRUE
22	IN	U2200_FEEDBACK	FUNC_TEST=TRUE
59 57	IN	ANALOG_RED	FUNC_TEST=TRUE
59 57	IN	ANALOG_GRN	FUNC_TEST=TRUE
59 57	IN	ANALOG_BLU	FUNC_TEST=TRUE
	IN	AUDIO_LI_DETECT_L	FUNC_TEST=TRUE
98 25	IN	AUDIO_LO_DET_L	FUNC_TEST=TRUE
75	IN	ROM_WP_L	FUNC_TEST=TRUE
83 80	IN	UATA_DD<15..0>	FUNC_TEST=TRUE
83 80	IN	UATA_DA<2..0>	FUNC_TEST=TRUE
83 80	IN	UATA_CS0_L	FUNC_TEST=TRUE
83 80	IN	UATA_CS1_L	FUNC_TEST=TRUE
83 80	IN	UATA_RESET_L	FUNC_TEST=TRUE
83	IN	UATA_DSTROBE_R	FUNC_TEST=TRUE
83 80	IN	UATA_HSTROBE	FUNC_TEST=TRUE
83 80 66	IN	UATA_STOP	FUNC_TEST=TRUE
83	IN	UATA_DMARQ_R	FUNC_TEST=TRUE
83 80	IN	UATA_DMACK_L	FUNC_TEST=TRUE
83	IN	UATA_INTRQ_R	FUNC_TEST=TRUE
83	IN	UATA_IOCS16_PU	FUNC_TEST=TRUE
83	IN	UATA_CSEL_PD	FUNC_TEST=TRUE
36 31	IN	TDIODE_NEG	FUNC_TEST=TRUE
76	IN	TP_AIRPORT_PME_L	FUNC_TEST=TRUE
76	IN	TP_AIRPORT_RF_DISABLE	FUNC_TEST=TRUE

FUNC TEST

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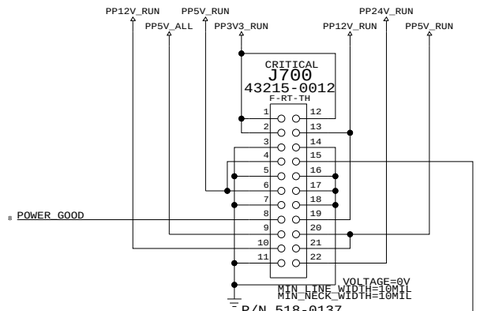
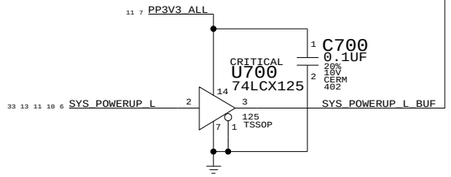
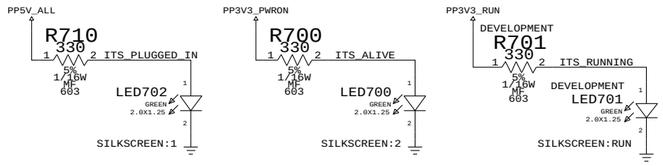
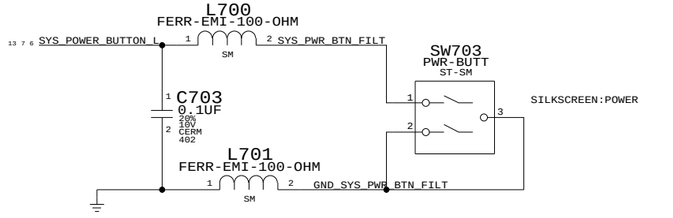
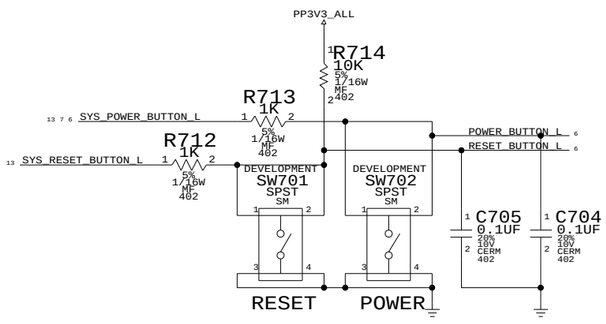
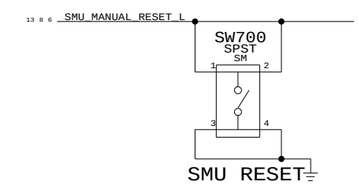






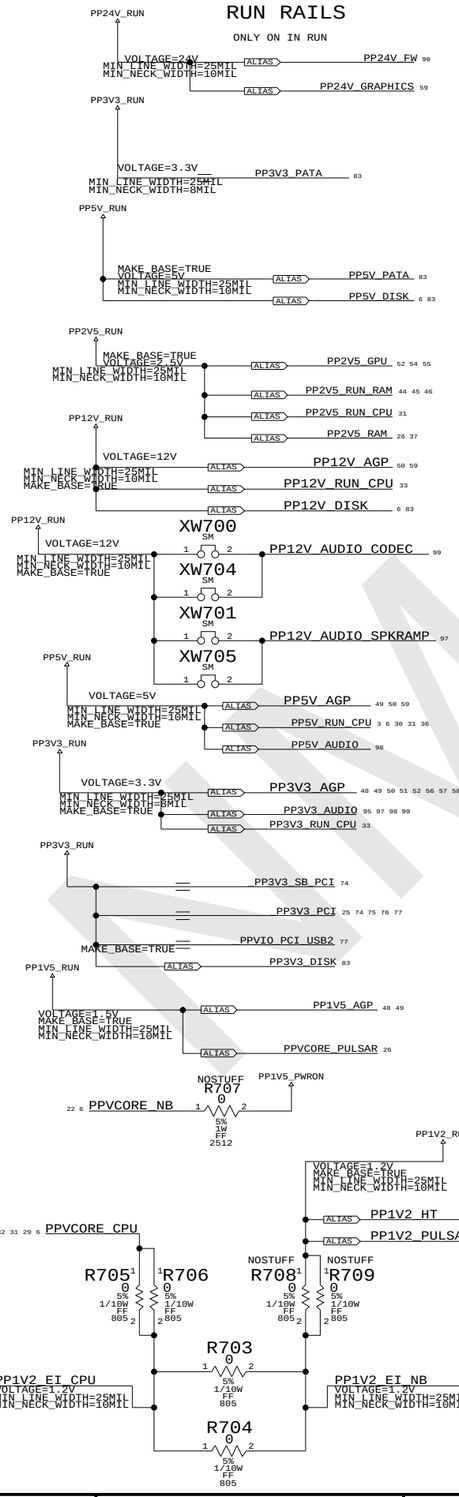






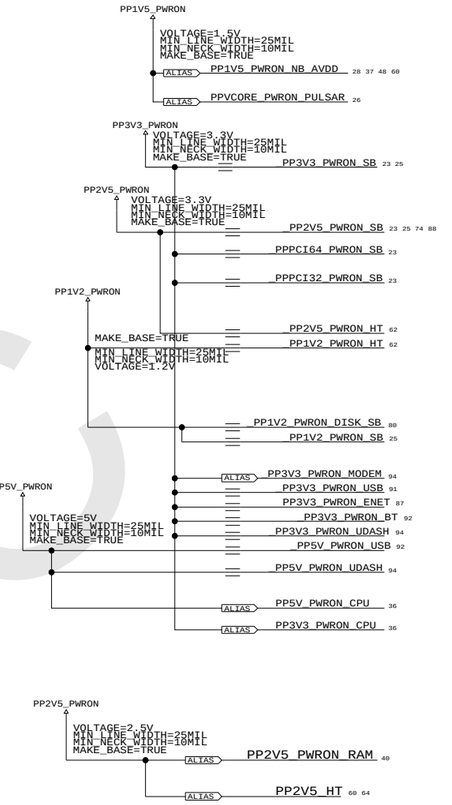
RUN RAILS

ONLY ON IN RUN



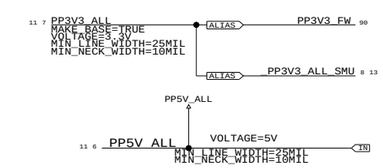
PWRON RAILS

ON IN RUN AND SLEEP

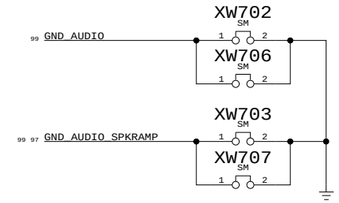


ALL RAILS

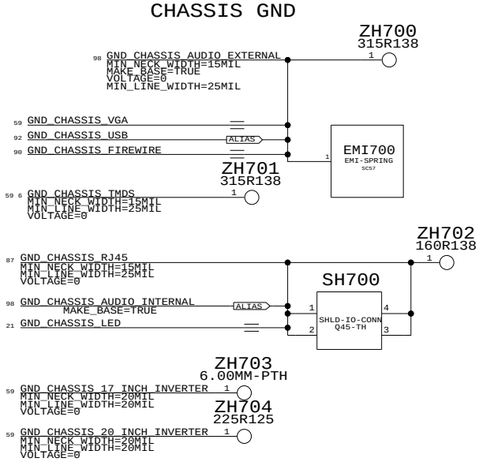
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



GND RAILS

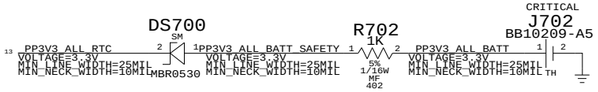


CHASSIS GND



RTC BATTERY

ALWAYS ON (TRICKLE)



POWER CONN / ALIAS

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D	051-6482	13
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PCI CLOCKS

TP_NB_THMI — MAKE_BASE=TRUE — ALIAS — NB_THMI (24)
TP_THMO — MAKE_BASE=TRUE — ALIAS — NB_THMO (24)

PCI_CLK33M_USB2 — MAKE_BASE=TRUE — PCI_CLK33M_USB2 (77)
PCI_CLK_GP0 (27)
TP_PCI_CLK_GP1 — MAKE_BASE=TRUE — ALIAS — PCI_CLK_GP1 (27)
6 PCI_CLK33M_AIRPORT — MAKE_BASE=TRUE — PCI_CLK33M_AIRPORT (76)
PCI_CLK_P3 (27)
TP_PCI_CLK_P4 — MAKE_BASE=TRUE — ALIAS — PCI_CLK_P4 (27)
74 27 PCI_CLK33M_SB_EXT — MAKE_BASE=TRUE — ALIAS — PCI_CLK_P1 (27)

SMU

TP_SMU_CHARGE_BATT — MAKE_BASE=TRUE — ALIAS — SMU_CHARGE_BATT (13)
NO_TEST=TRUE
TP_ALS0_OUT — MAKE_BASE=TRUE — ALIAS — ALS0_OUT (13)
TP_ALS1_OUT — MAKE_BASE=TRUE — ALIAS — ALS1_OUT (13)
TP_ALS_GAIN_BOOST — MAKE_BASE=TRUE — ALIAS — ALS_GAIN_BOOST (13)
TP_SMU_ADAPTER_ID — MAKE_BASE=TRUE — ALIAS — SMU_ADAPTER_ID (13)
TP_ACCEL_LOWPWR_L — MAKE_BASE=TRUE — ALIAS — ACCEL_LOWPWR_L (13)
TP_SMU_PWRSEQ_P1_3 — MAKE_BASE=TRUE — ALIAS — SMU_PWRSEQ_P1_3 (13)
TP_SMU_PWRSEQ_P1_4 — MAKE_BASE=TRUE — ALIAS — SMU_PWRSEQ_P1_4 (13)
13 TP_SMU_SPARE_P10_0 — MAKE_BASE=TRUE — ALIAS — SMU_SPARE_P10_0
TP_ACCEL_INT_L — MAKE_BASE=TRUE — ALIAS — ACCEL_INT_L (13)

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S2784	1	PROCESSOR	CBGA-576-1MM	IC,MPU,NEO,10S,REV2,1.8GHZ,70C	1.8GHZ	1.15V	45W	?	U2900	NEO_REV2_1_8GHZ
337S2785	1	PROCESSOR	CBGA-576-1MM	IC,MPU,NEO,10S,REV2,2.0GHZ,70C	2.0GHZ	1.15V	65W	?	U2900	NEO_REV2_2_0GHZ
337S2786	1	PROCESSOR	CBGA-576-1MM	IC,MPU,NEO,10S,REV3,1.8GHZ,70C	1.8GHZ	1.15V	45W	?	U2900	NEO_REV3_1_8GHZ
337S2787	1	PROCESSOR	CBGA-576-1MM	IC,MPU,NEO,10S,REV3,2.0GHZ,70C	2.0GHZ	1.15V	65W	?	U2900	NEO_REV3_2_0GHZ

PP2V5_PWRON
R870 4.7K 5% 1/16W MF 402
24 13 SMU_WARM_RESET_L
U700 74LCX125 TSSOP — SYS_WARM_RESET_L (24 25 74 77 87)
13 SMU_SLEEP
U700 74LCX125 TSSOP — SYS_SLEEP (6 9 10 11 27 46 50)
U700 74LCX125 TSSOP

MISC PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
	062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE VPP1		
	820-1540	1	PCB,FAB,MLB	MLB1	
	825-2029	1	LBL,SER #,INP DEV	LBL1	
	051-6482	1	PCB,SCHEM,MLB	SCH1	
	341T1366	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
CRITICAL	742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT700	
	875-1614	1	GAP FILLER	GAP2900	
	341T1395	1	PURCH ASSY, SMU BIG	U1300	
CRITICAL	875-1752	1	GPU GAP PAD	PAD4900	
CRITICAL	452-0678	6	CPU HEATSINK SCREW	SRW800,SRW801,SRW802,SRW803,SRW804,SRW805	
CRITICAL	870-1177	6	CPU HEATSINK SPRING	SPR800,SPR801,SPR802,SPR803,SPR804,SPR805	
CRITICAL	730-0291	1	CPU HEATSINK	HS2900	

NEED TO ADD THERMAL GREASE TO MLB BOM

ALTERNATE FOR SERIAL NUMBER LABEL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
825-2808	825-2029	COMMON	LBL1	BAR CODE LABEL

CPU VID<0:5>

VID SET TO 1.475V TO ACHIEVE 1.45V AT PROCESSOR

PP3V3_RUN
R814 10K, R816 10K, R817 10K, R808 10K, NOSTUFF R809 10K, R804 10K (5% 1/16W MF 402)
13 CPU_VID<0> — NOSTUFF R819 0 — CPU_VID_R<0> (6 33)
13 CPU_VID<1> — NOSTUFF R820 0 — CPU_VID_R<1> (6 33)
13 CPU_VID<2> — NOSTUFF R821 0 — CPU_VID_R<2> (6 33)
13 CPU_VID<3> — NOSTUFF R822 0 — CPU_VID_R<3> (6 33)
13 CPU_VID<4> — NOSTUFF R823 0 — CPU_VID_R<4> (6 33)
13 CPU_VID<5> — NOSTUFF R824 0 — CPU_VID_R<5> (6 33)
NOSTUFF J803 BM12B-SRSS-TB F-ST-SM
R832 10K, R831 10K, R830 10K, R829 10K, R827 10K, R811 20K (NOSTUFF, 5% 1/16W MF 402)

NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

DOWNLOAD CONNECTOR

PP3V3_ALL
DEVELOPMENT J802 ST-HDR-RI-TEMP TH 998-0269
SMU_BOOT_SCLK
SMU_BOOT_CE
SMU_BOOT_CNVSS
R826 100 5% 1/16W MF 402
J802_2 — SMU_BOOT_BUSY (13)
SMU_BOOT_RXD (13)
J802_6 — (SMU_BOOT_EPM)
SMU_MANUAL_RESET_L (6 7 8 13)
SMU_BOOT_TXD (13)
DEVELOPMENT R806 10K, R807 10K, R805 0, R803 10K (5% 1/16W MF 402)

SMU ANALOG VREF

13 PP3V3_ALL_SMU_AVCC
NOSTUFF R818 200 1% 1/16W MF 402
NOSTUFF C801 2.2UF 20% 10V CERM 805
PPVREF_SMU (13)
R802 0 5% 1/16W MF 402 — PPVREF_SMU_ADC_REF (36)
NOSTUFF VR801 2.5V SOT-23
NOSTUFF C802 0.47UF 20% 16V CERM 603
GND_SMU_AVSS (13 33 36)
R828 0 5% 1/16W MF 402 — GND_SMU_AVSS_DAGND (36)

POWER_FAIL_L CONNECTION

PP3V3_ALL
R812 10K 5% 1/16W MF 402
SYS_POWERFAIL_L (6 13)
7 POWER_GOOD — R813 47 5% 1/16W MF 402

CPU HEATSINK SMT NUTS

SDF800 HSK-NUT-6.5MM TH — HS_SDF800 (1) — C880 0.01UF 20% 16V CERM 402
SDF801 HSK-NUT-6.5MM TH — HS_SDF801 (1) — C881 0.01UF 20% 16V CERM 402
SDF802 HSK-NUT-6.5MM TH — HS_SDF802 (1) — C882 0.01UF 20% 16V CERM 402
SDF803 HSK-NUT-6.5MM TH — HS_SDF803 (1) — C883 0.01UF 20% 16V CERM 402
SDF804 HSK-NUT-6.5MM TH — HS_SDF804 (1) — C884 0.01UF 20% 16V CERM 402
SDF805 HSK-NUT-6.5MM TH — HS_SDF805 (1) — C885 0.01UF 20% 16V CERM 402

CHEAPER SMU RESET

13 7 PP3V3_ALL_SMU
NOSTUFF R815 1K 5% 1/16W MF 402
NOSTUFF D800 1N914 SOT23
NOSTUFF R810 0 5% 1/16W MF 402
13 8 7 6 SMU_MANUAL_RESET_L — SMU_RESET_L (6 13)
NOSTUFF C800 1UF 10% 6.3V CERM 402

PULSAR ERROR_L LED

PP3V3_RUN
DEVELOPMENT R801 4.7K 5% 1/16W MF 402
DEVELOPMENT R800 330 5% 1/16W MF 402
ERROR_LED
DEVELOPMENT D810 RED SM
27 CLOCK_ERROR_L

SHASTA JTAG PULL DOWN

25 JTAG_SB_TRST_L
R825 10K 5% 1/16W MF 402
THESE PINS HAVE INTERNAL PULLUPS
TP_JTAG_SB_TCK — MAKE_BASE=TRUE — ALIAS — JTAG_SB_TCK (25)
TP_JTAG_SB_TDI — MAKE_BASE=TRUE — ALIAS — JTAG_SB_TDI (25)
TP_JTAG_SB_TDO — MAKE_BASE=TRUE — ALIAS — JTAG_SB_TDO (25)
TP_JTAG_SB_TMS — MAKE_BASE=TRUE — ALIAS — JTAG_SB_TMS (25)

DEVELOPMENT J800 U.FL-R_SMT F-ST-SM
24 NB_PMR_OBSV
518S0104

SIGNAL ALIAS

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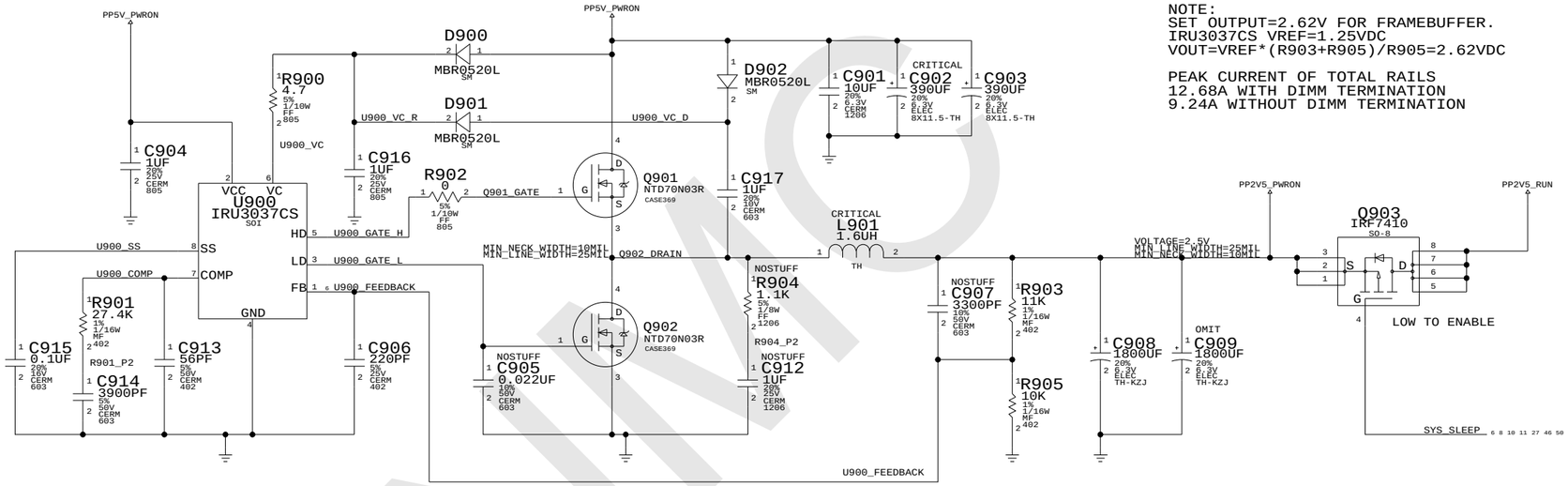
2.5V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=2.62V FOR FRAMEBUFFER.
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R903+R905)/R905=2.62VDC

PEAK CURRENT OF TOTAL RAILS
12.68A WITH DIMM TERMINATION
9.24A WITHOUT DIMM TERMINATION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
124-0324	1	CAP,AL ELEC,1500UF,6.3V	C909	17_INCH_LCD
124-0322	1	CAP,AL ELEC,1800UF,6.3V	C909	20_INCH_LCD

2.5V VREG

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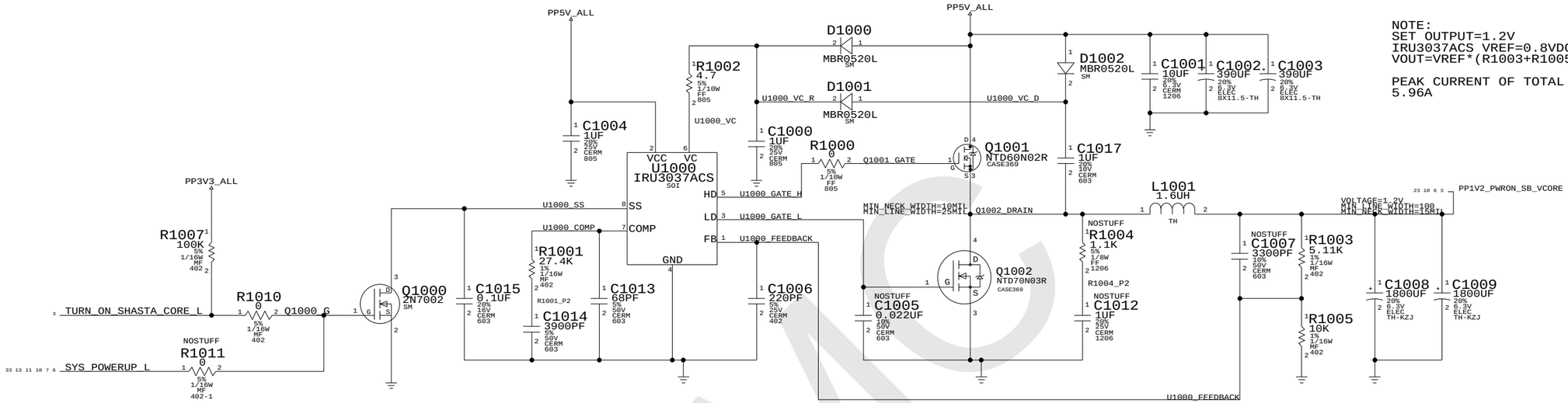
SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE: NONE

SHT 9 OF 99

SHASTA CORE VOLTAGE REGULATOR

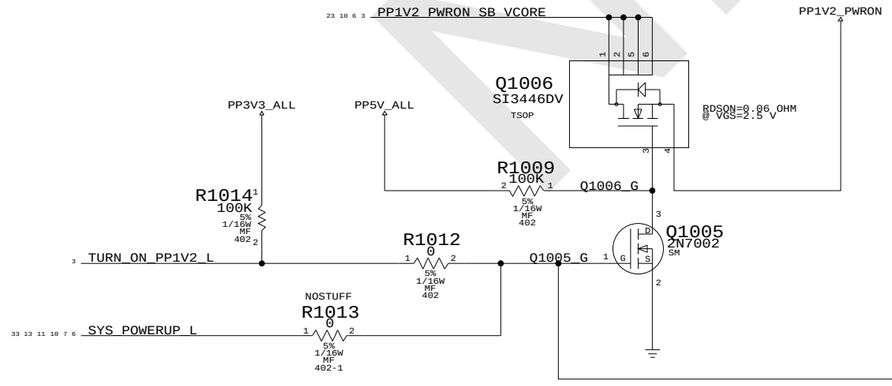


NOTE:
SET OUTPUT=1.2V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.206VDC

PEAK CURRENT OF TOTAL RAILS
5.96A

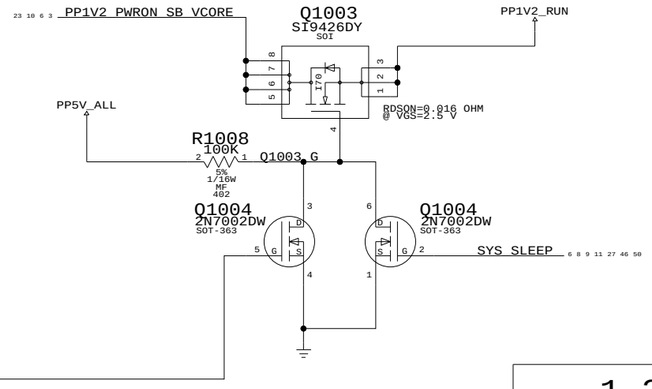
PP1V2_PWRON FET SWITCH

PEAK CURRENT 0.6A



PP1V2_RUN FET SWITCH

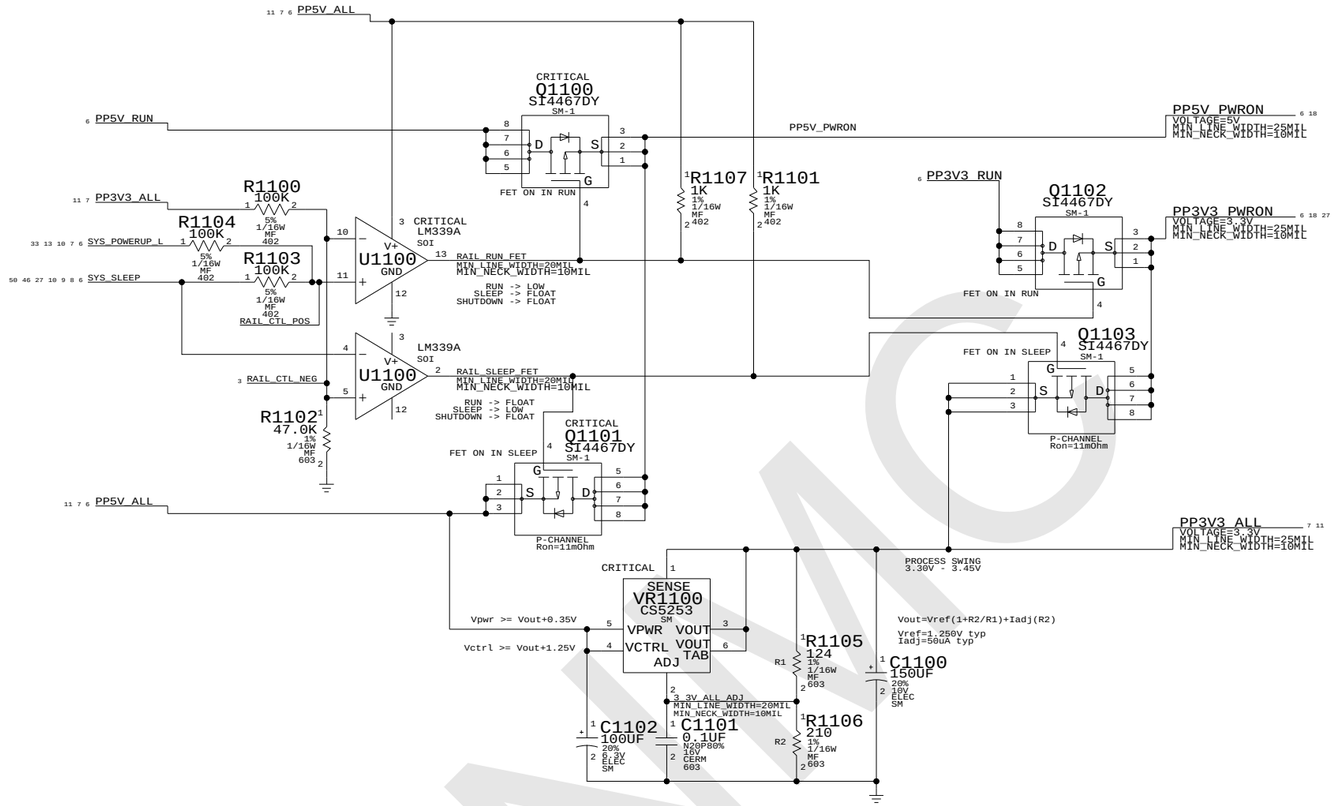
PEAK CURRENT 4.43A



1.2V VREG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 10 OF 99	



5V & 3.3V VREGS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT
NONE	11 OF 99

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	15 MIL SPACING		SMU_CLK10M_XIN 13
	15 MIL SPACING		SMU_CLK10M_XOUT 13
	15 MIL SPACING		SMU_CLK10M_XOUT_R 13
RTC_CLK32K_XTAL	15 MIL SPACING		RTC_CLK32K_X1 13
	15 MIL SPACING		RTC_CLK32K_X2 13

Page Notes

Power aliases required by this page:
- _PP3V3_ALL_SMU
- _PP3V3_ALL_RTC
- _PP3V3_PWRON_SMU
- _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

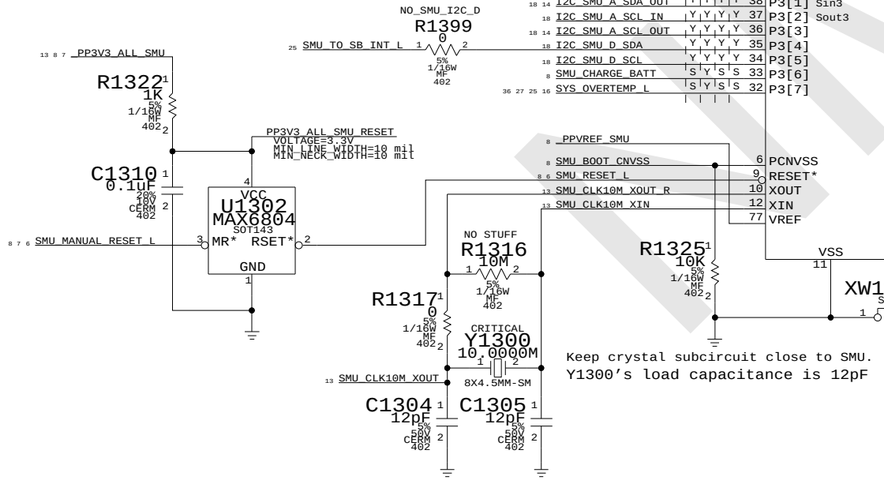
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

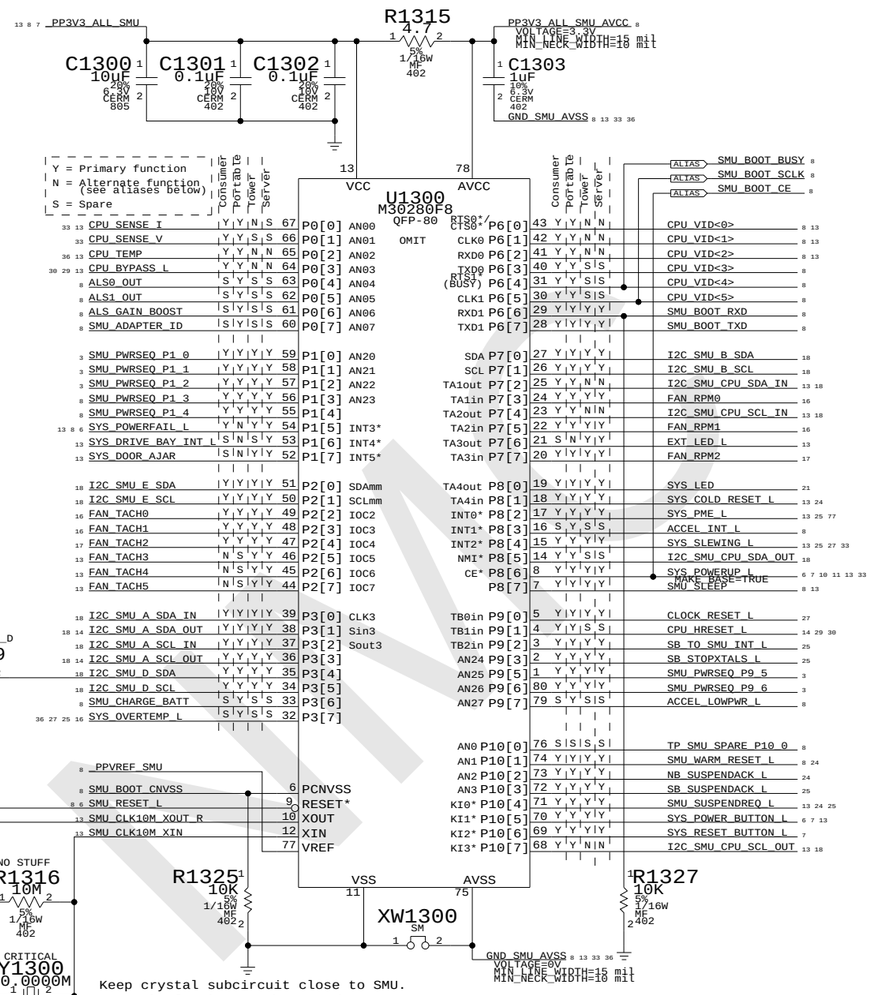
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.4.

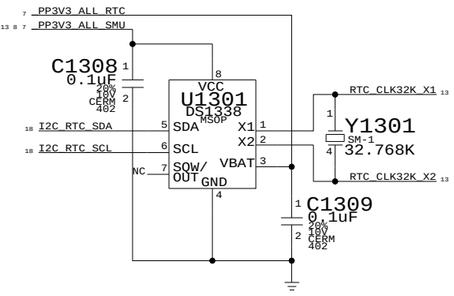
Undervoltage Reset Circuit



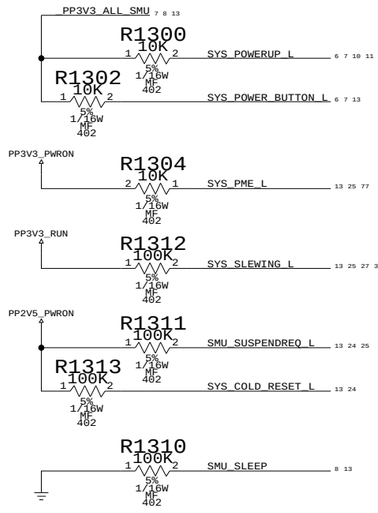
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Consumer

	Port		
13 FAN_TACH3	2.5 (ALTAS)	SYS_LED_RED	21
13 FAN_TACH4	2.6 (ALTAS)	SYS_LED_GREEN	21
13 FAN_TACH5	2.7 (ALTAS)	SYS_LED_BLUE	21

Portable

	Port		
13 8 6 SYS_POWERFAIL_L	1.5 (ALTAS)	SMU_ACIN	
13 SYS_DRIVE_BAY_INT_L	1.6 (ALTAS)	SMU_BATT_DET_L	
13 SYS_DOOR_AJAR	1.7 (ALTAS)	SYS_LID_OPEN	
13 EXT_LED_L	7.6 (ALTAS)	SYS_KBDLED	

Tower & Server

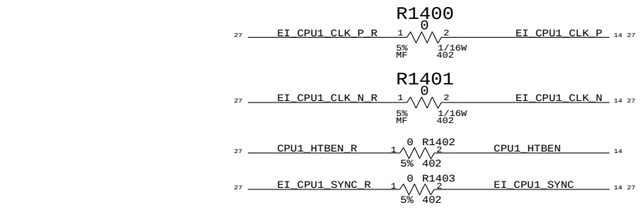
	Port		
33 13 CPU_SENSE_I	0.0 (ALTAS)	SYS_SLOT_PWR	
36 13 CPU_TEMP	0.2 (ALTAS)	FAN_TACH6	
30 29 13 CPU_BYPASS_L	0.3 (ALTAS)	FAN_TACH7	
13 8 CPU_VID<0>	6.0 (ALTAS)	FAN_RPM3	
13 8 CPU_VID<1>	6.1 (ALTAS)	FAN_RPM4	
13 8 CPU_VID<2>	6.2 (ALTAS)	FAN_RPM5	
18 13 I2C_SMU_CPU_SDA_IN	7.2 (ALTAS)	FAN_PWM6	
18 13 I2C_SMU_CPU_SCL_IN	7.4 (ALTAS)	FAN_PWM7	
18 13 I2C_SMU_CPU_SCL_OUT	10.7 (ALTAS)	EXT_POWER_BUTTON_L 6	

Master: Link

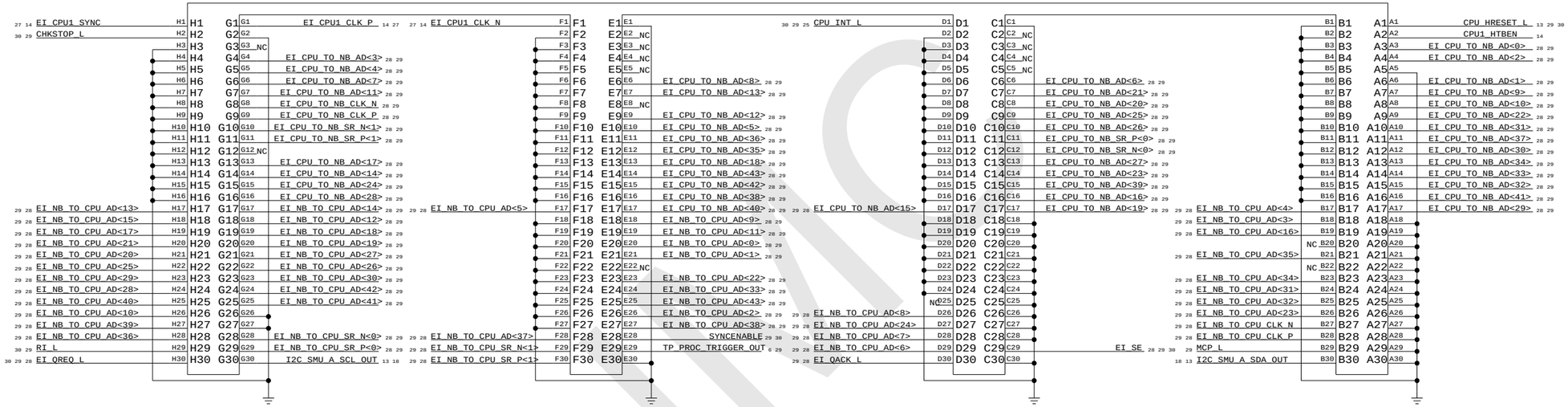
System Management Unit

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 13 OF 99	



NOSTUFF



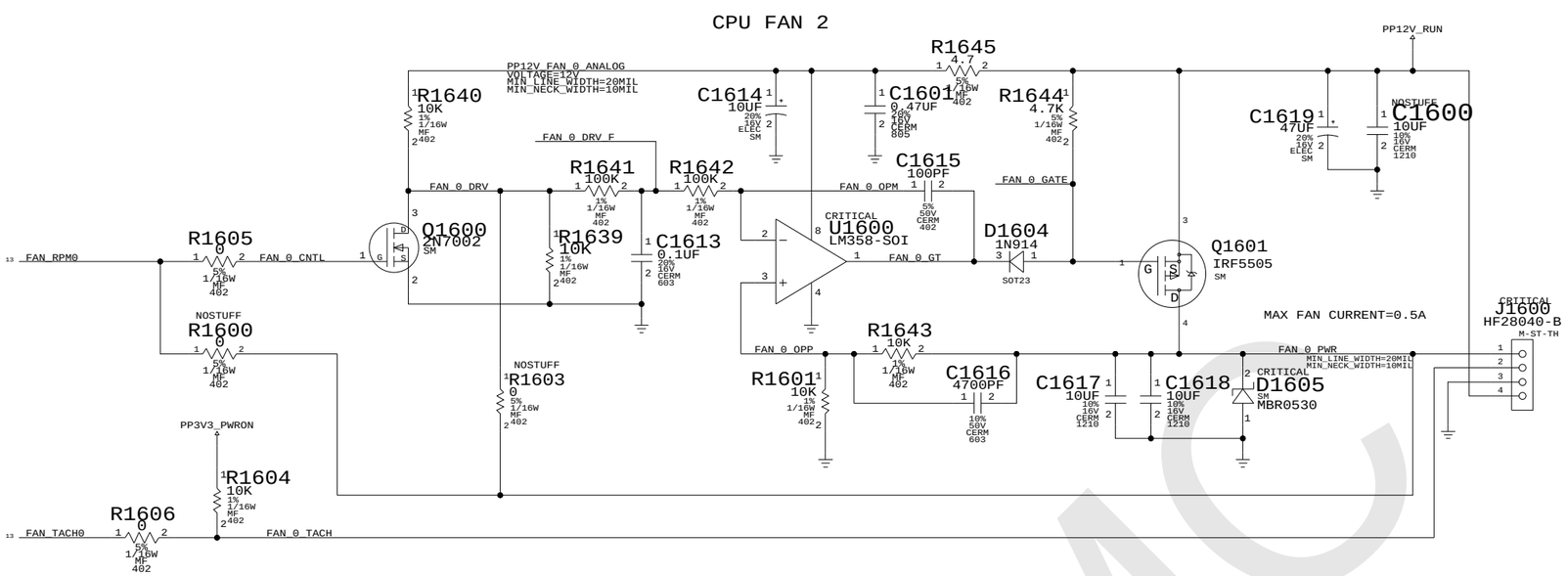
CPU LOGIC ANALYZER

APPLE COMPUTER INC.

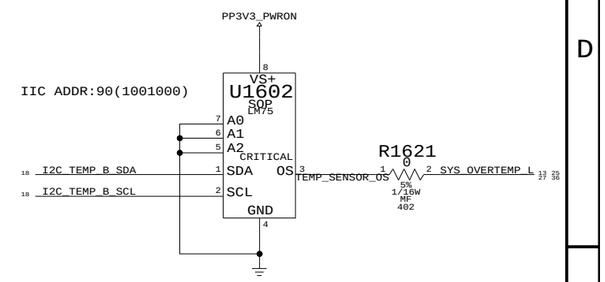
SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT
NONE	14 OF 99

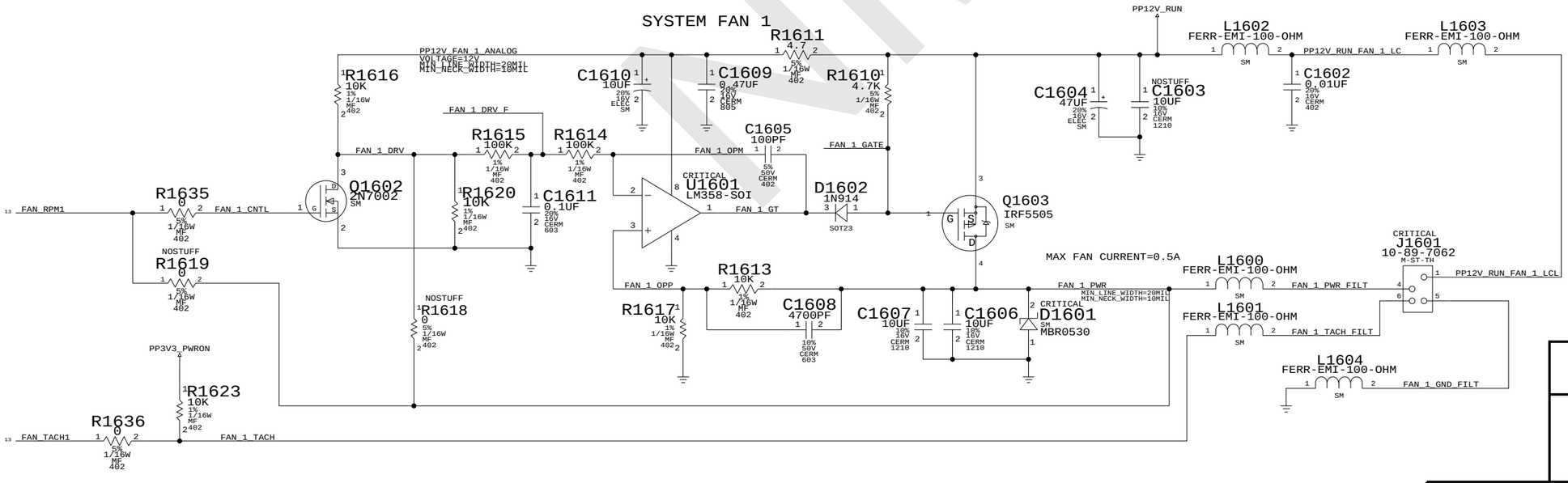
FAN 0 - Q37 STYLE CPU FAN CONTROL CIRCUIT



SYSTEM TEMP SENSOR



FAN 1 - Q37 STYLE CPU FAN CONTROL CIRCUIT

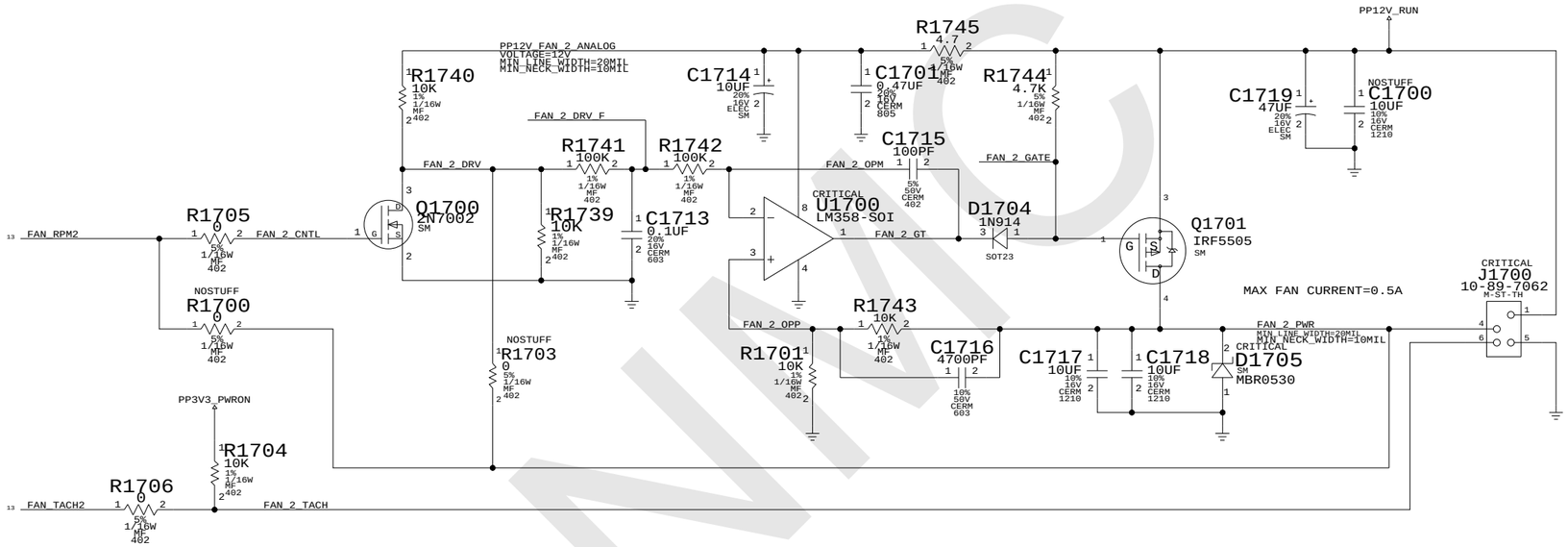


Q37/Q16 FAN CONTROL

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 16 OF 99	

FAN 2 - Q37 STYLE SYSTEM FAN CONTROL CIRCUIT



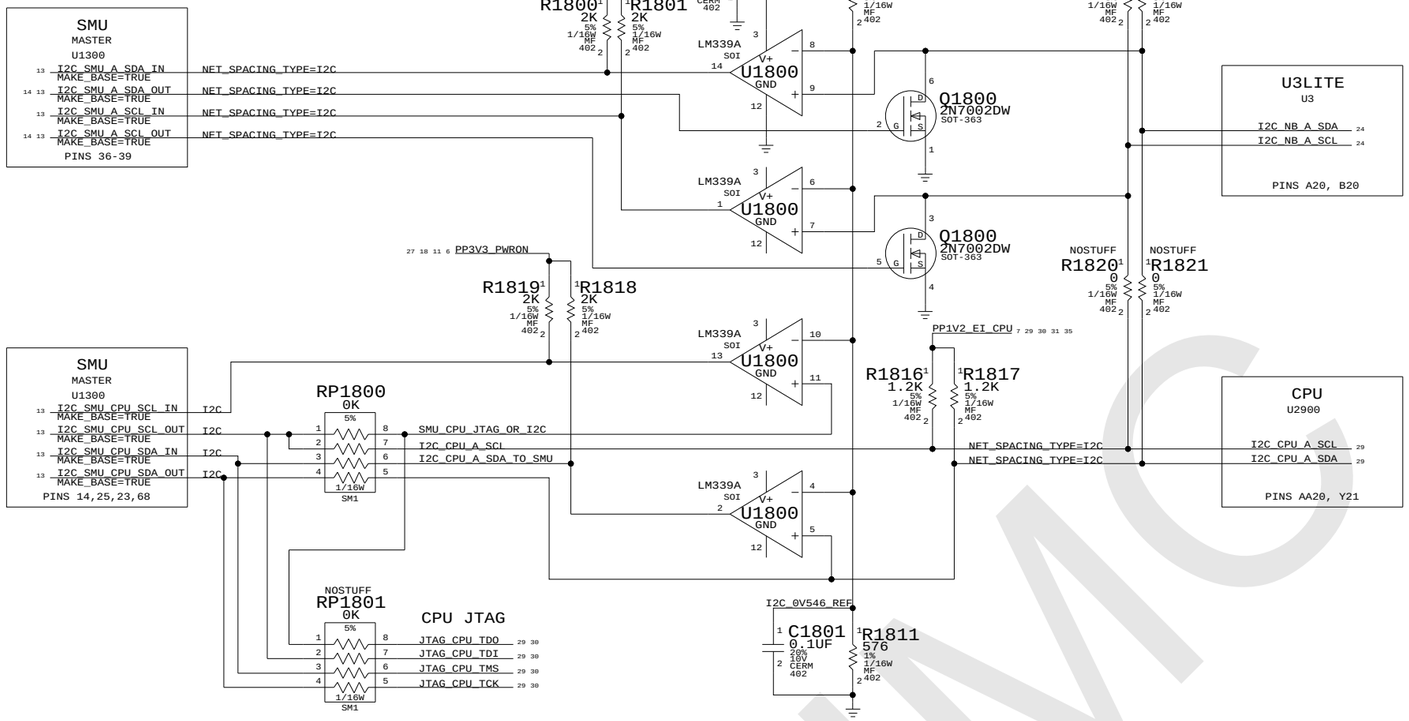
CPU FAN CONNECTOR

APPLE COMPUTER INC.

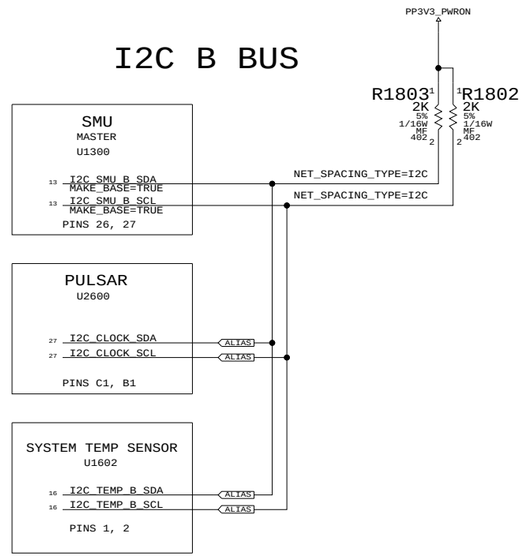
SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT
NONE	17 OF 99

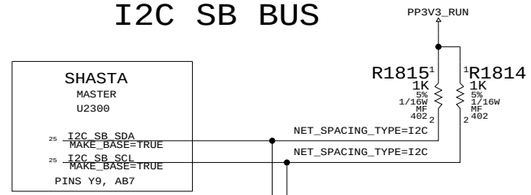
I2C A BUS



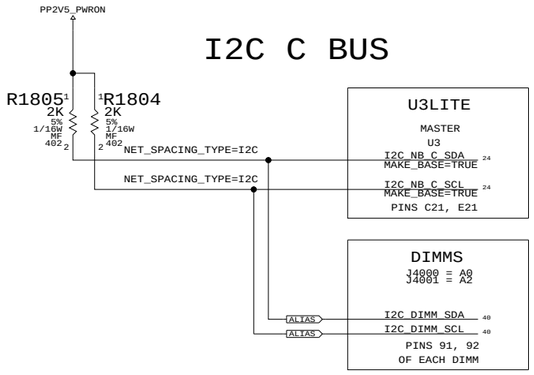
I2C B BUS



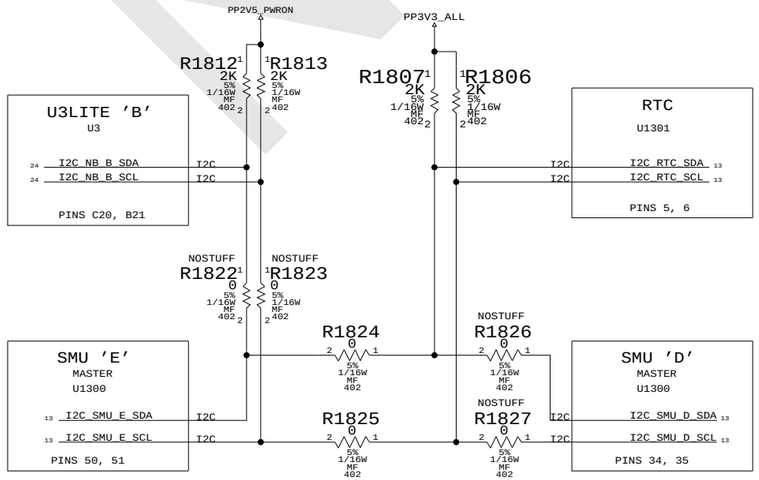
I2C SB BUS



I2C C BUS



I2C D & E BUS



I2C CONNECTIONS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 18 OF 99	

TOTAL CURRENT EXCLUDING LEDS CURRENT < 170 MICRO AMPS

PLACE THESE PARTS CLOSE TO SMU IC

PP5V_PWRON

RGB_LED R2109 953K 1% 1/16W MF 402

RGB_LED R2101 0 5% 1/16W MF 402

SYS_LED_GREEN MAKE_BASE=TRUE

PWM INPUT FROM SMU

G_PWM_IN_H

RGB_LED U2100 LP324 TSSOP

G_BASE_DRV

G_PWM_DC

RGB_LED R2104 953K 1% 1/16W MF 402

RGB_LED C2104 0.022UF 20% 16V CERM 402

RGB_LED C2106 0.47UF 20% 10V CERM 603

RGB_LED R2105 200K 1% 1/16W MF 402

RGB_LED R2112 1K 1% 1/16W MF 402

G_IN_OFFSET

5MV INPUT OFFSET

100% DUTY CYCLE OF 3V-PP PWM = 0.5V

RGB_LED C2105 220PF 5% 25V CERM 402

GND_CHASSIS_LED 7 21

G_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED L2100 400-OHM-EMI SM-1

G_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED Q2102 2N3904 SM

G_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED R2100 25.5 1% 1/16W MF 402

CHANGE R2100 VALUE TO SET LED CURRENT

MAX LED CURRENT = 0.5 / R

RGB_LED LED2100 LATBG66B AMB-GRN-BLUE PLCC

AMB GRN BLUE

RGB_LED L2104 400-OHM-EMI SM-1

RGB_LED_A MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED C2107 220PF 5% 25V CERM 402

RGB_LED C2108 220PF 5% 25V CERM 402

RGB_LED C2109 220PF 5% 25V CERM 402

RGB_LED C2103 0.1UF 20% 10V CERM 402

RGB_LED U2100 LP324 TSSOP

U2100_UNUSED

PLACE THESE PARTS CLOSE TO SMU IC

PP5V_PWRON

RGB_LED R2102 953K 1% 1/16W MF 402

RGB_LED R2115 0 5% 1/16W MF 402

SYS_LED_RED MAKE_BASE=TRUE

PWM INPUT FROM SMU

R_PWM_IN_H

RGB_LED U2100 LP324 TSSOP

R_BASE_DRV

R_PWM_DC

RGB_LED R2110 953K 1% 1/16W MF 402

RGB_LED C2101 0.022UF 20% 16V CERM 402

RGB_LED C2112 0.47UF 20% 10V CERM 603

RGB_LED R2111 200K 1% 1/16W MF 402

RGB_LED R2114 1K 1% 1/16W MF 402

R_IN_OFFSET

R_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED L2101 400-OHM-EMI SM-1

R_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED Q2108 2N3904 SM

R_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED R2113 25.5 1% 1/16W MF 402

PLACE THESE PARTS CLOSE TO SMU IC

PP5V_PWRON

RGB_LED R2118 953K 1% 1/16W MF 402

RGB_LED R2130 0 5% 1/16W MF 402

SYS_LED_BLUE MAKE_BASE=TRUE

PWM INPUT FROM SMU

B_PWM_IN_H

RGB_LED U2100 LP324 TSSOP

B_BASE_DRV

B_PWM_DC

RGB_LED R2116 953K 1% 1/16W MF 402

RGB_LED C2102 0.022UF 20% 16V CERM 402

RGB_LED C2118 0.47UF 20% 10V CERM 603

RGB_LED R2117 200K 1% 1/16W MF 402

RGB_LED R2127 1K 1% 1/16W MF 402

B_IN_OFFSET

B_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED L2102 400-OHM-EMI SM-1

B_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED Q2114 2N3904 SM

B_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

RGB_LED R2126 25.5 1% 1/16W MF 402

PLACE THESE PARTS CLOSE TO SMU IC

NOSTUFF Q2100 FDV302P SOT-23

PP3V3_PWRON

NOSTUFF R2119 953K 1% 1/16W MF 402

SYS_LED_H

WHITE_LED R2106 1K 5% 1/16W MF 402

SYS_GATE

WHITE_LED R2129 4.7K 5% 1/16W MF 402

NOSTUFF R2132 1K 5% 1/16W MF 402

SYS_LED

PWM INPUT FROM SMU

SYS_LED_IN

WHITE_LED R2107 0 5% 1/16W MF 402

(STUFF WHEN SYS_LED_L = ACTIVE HIGH)
(AND NO STUFF R2132, R2119 & Q2100)

LED2101

WHITE SM6

SYS_DRV_A MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

PP5V_PWRON

WHITE_LED L2105 400-OHM-EMI SM-1

WHITE_LED C2111 220PF 5% 25V CERM 402

WHITE_LED C2110 220PF 5% 25V CERM 402

GND_CHASSIS_LED 7 21

SYS_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

WHITE_LED L2103 400-OHM-EMI SM-1

SYS_LED_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

WHITE_LED R2103 100 1% 1/16W MF 402

SYS_LED_DRV_C MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

WHITE_LED Q2101 FDV301N SM

INDICATOR LED

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE: NONE

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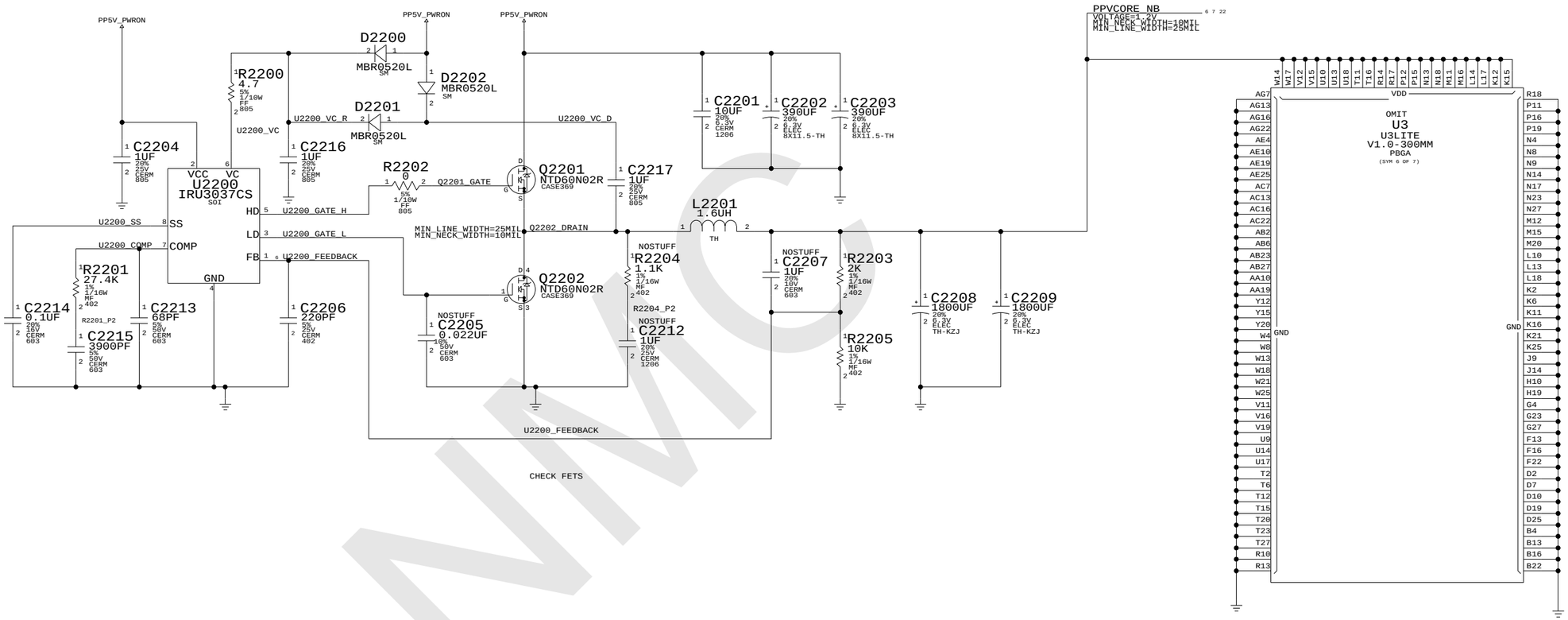
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0284	1	IC,U3LITE,V1.1,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0282	343S0284		U3	U3L,V1.1,200MM,PBGA

NOTE:
SET OUTPUT=1.5VDC FOR U3LITE CORE
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R2203+R2205)/R2205=1.5VDC

7.73A OF PEAK CURRENT DRAW ON PCORE_NB



22 7 6 PPVCORE_NB

C2222 0.1UF
C2223 0.1UF
C2225 0.1UF
C2227 0.1UF
C2228 0.1UF
C2229 0.1UF
C2230 0.1UF
C2231 0.1UF
C2232 0.1UF
C2233 0.1UF
C2234 0.1UF
C2235 0.1UF
C2236 0.1UF
C2237 0.1UF
C2238 0.1UF
C2239 0.1UF
C2240 0.1UF
C2242 0.1UF
C2243 0.1UF
C2244 0.1UF
C2245 0.1UF
C2246 0.1UF
C2247 0.1UF

U3LITE CORE POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 22 OF 99	

VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
3.3V	25MIL	10MIL	PPPCI64_PWRON_SB 7 23
3.3V	25MIL	10MIL	PPPCI32_PWRON_SB 7 23
3.3V	25MIL	10MIL	PP3V3_PWRON_SB 7 23 25
2.5V	25MIL	10MIL	PP2V5_PWRON_SB 7 23 25 74 88
1.2V	100	15MIL	PP1V2_PWRON_SB_VCORE 3 6 10 23

Page Notes

Power aliases required by this page:
- _PPPCI64_PWRON_SB (to 5V or 3.3V)
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
- (NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

neoBorg Implementation

Master power enable signal (from PMU) connects directly to SBVCORE supply (SBVCORE_RUN). Supply asserts PGOOD (SBVCORE_PGOOD) when ready, which acts as the power enable signal for the rest of the neoBorg components.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

23 10 6 3 PP1V2_PWRON_SB_VCORE

C2300 C2301 C2302 C2303 C2304
C2305 C2306 C2307 C2308 C2309
C2310 C2311 C2312 C2313 C2314

25 23 7 PP3V3_PWRON_SB

C2320 C2321 C2322 C2323 C2324
C2325 C2326 C2327 C2328 C2329
C2330 C2331 C2332 C2333 C2334
C2335 C2336 C2337 C2338 C2339

All: 0.1uF 20% 10V CERM 402

VDDC: H15 H8 J12 J15 K8 L15 L8 M15 N8 P15 R10 R12 R9 T10 T15

VDDO33: AA1 AA2 AA3 AB10 AB2 AB6 B1 B2 B5 D1 F4 F8 H1 L7 M1 R2 U12 U9 V7 W4

GND: A1 A2 A22 A5 AA10 AA6 AB1 AB22 C19 D2 E22 F3 F7 H2 H9 J10 J11 J13 J14 J16

GND: J22 K10 K11 K12 K13 K7 K9 L10 L11 L12 L13 L14 L16 L9 M10 M11 M12 M13 M14

OMIT

U2300
SHASTA
V1.0
BGA
(1 OF 8)

POWER

Shasta max (est 06/30/03) current:

DIGITAL	- 1.2V -	950 mA	(1175 mW)
ANALOG12	- 1.2V -	600 mA	(760 mW)
VDDPs	- 2.5V -	100 mA	(250 mW)
I/O 2.5	- 2.5V -	20 mA	(60 mW)
I/O 3.3	- 3.3V -	220 mA	(770 mW)
Total:			3015 mW

VDDO25: D19 G15

VIO1: H18 H17 K21

VIO2: L21 W22 Y19

VDDP_KL: V8

W5 W19 U22 U13 U10 T12 R19 P9 P4 P14 P13 P12 P10 N9 N22 N13 N12 N11 N10 M2

PP2V5_PWRON_SB 7 23 25 74 88

C2350 C2351 (0.1uF 20% 10V CERM 402)

PPPCI64_PWRON_SB 7 23

C2355 C2356 C2357 (0.1uF 20% 10V CERM 402)

For PCI_AD<63..32>

PPPCI32_PWRON_SB 7 23

C2360 C2361 C2362 (0.1uF 20% 10V CERM 402)

For PCI_AD<31..0>

PP2V5_PWRON_SB 7 23 25 74 88

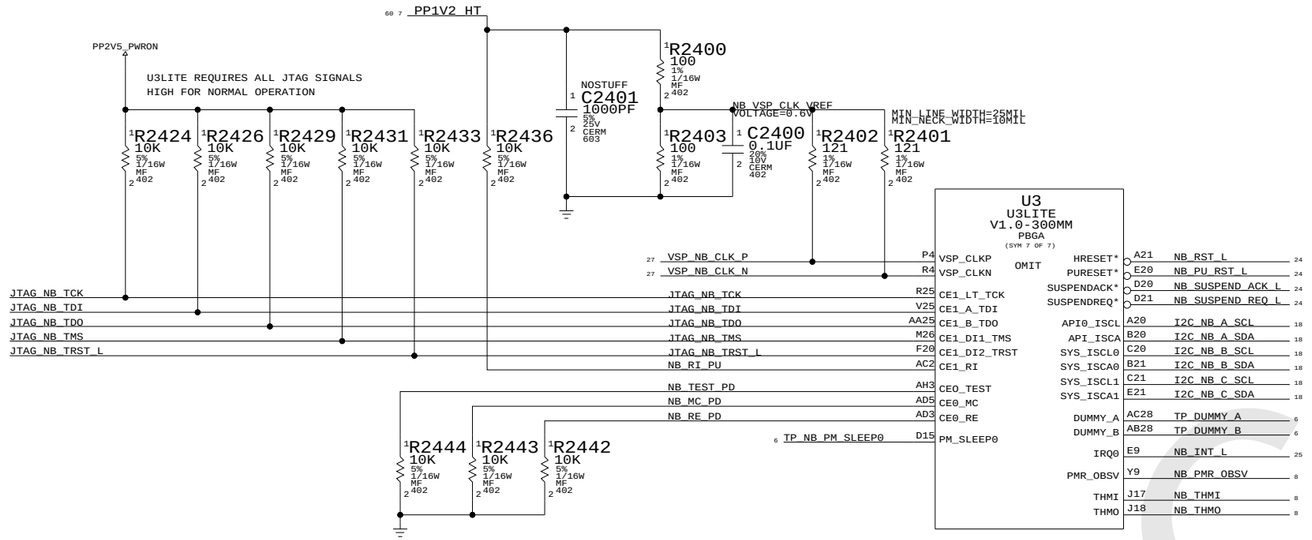
C2365 (0.1uF 20% 10V CERM 402)

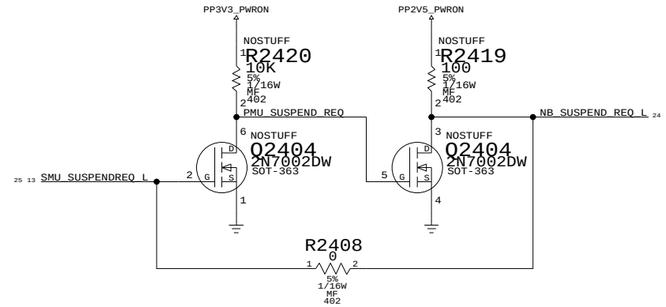
DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:04 2003

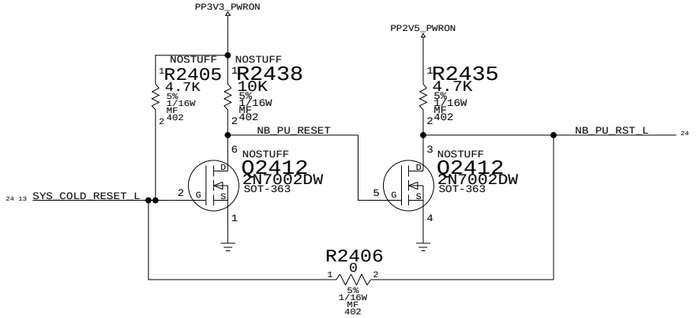
Shasta Core

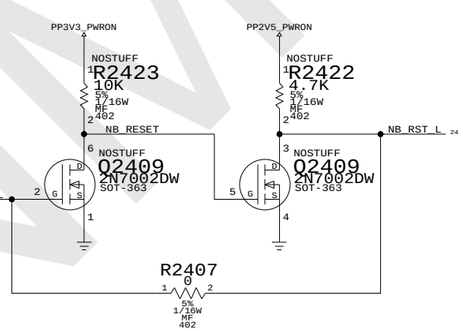
APPLE COMPUTER INC.

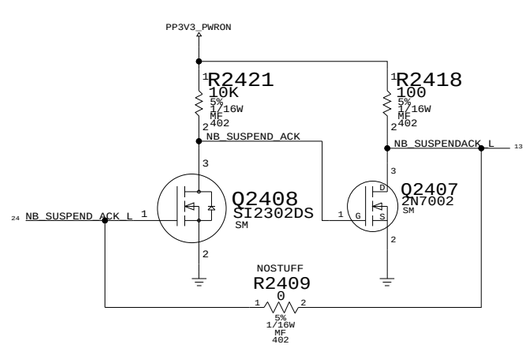
SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 23 OF 99	











ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_RESET	10 MIL SPACING		SYS_COLD_RESET_L 13 24
SMU_RESET	10 MIL SPACING		SYS_WARM_RESET_L 8 25 74 77 87

MASTER: GILA

U3LITE MISC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE: NONE

SHT 24 OF 99

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I2S0_TO_SB			I2S0_DEV_TO_SB_DTI 25 95
I2S0_TO_DEV			I2S0_SB_TO_DEV_DTO 25 95
I2S0_TO_DEV			I2S0_MCLK 25 95
I2S0_BIDIR			I2S0_BITCLK 25 95
I2S0_BIDIR			I2S0_SYNC 25 95
I2S1_TO_SB			I2S1_DEV_TO_SB_DTI 6 25 76 94
I2S1_TO_DEV			I2S1_SB_TO_DEV_DTO 6 25 76 94
I2S1_TO_DEV			I2S1_MCLK 6 25 94
I2S1_BIDIR			I2S1_BITCLK 6 25 94
I2S1_BIDIR			I2S1_SYNC 6 25 94
I2S2_TO_SB			I2S2_DEV_TO_SB_DTI 25 99
I2S2_TO_DEV			I2S2_SB_TO_DEV_DTO 25 99
I2S2_TO_DEV			I2S2_MCLK 25 99
I2S2_BIDIR			I2S2_BITCLK 25 99
I2S2_BIDIR			I2S2_SYNC 25 99
SB_CLK18M_XTAL	15_MIL_SPACING		SB_CLK18M_XTALI 25
	15_MIL_SPACING		SB_CLK18M_XTALO 25
	15_MIL_SPACING		SB_CLK18M_XTALO_R 25
SB_CLK25M_ATA	15_MIL_SPACING		SB_CLK25M_ATA 25 27

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- PCI_64BIT
  Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs

NorthBridge / SouthBridge MPIC Routing

PP3V3_RUN
R2576 10K 5% 1/16W MF 402
To SouthBridge -> NB_TO_SB_INT 25
-> From NorthBridge NB_INT_L 24
MPIC_SB R2575 10K 5% 1/16W MF 402
NB_INT_L_R
MPIC_SB Q2576 2N3904 SM
MPIC_NB R2579 0 5% 1/16W MF 402
MPIC_SB R2578 0 5% 1/16W MF 402
<- To CPU CPU_INT_L 29 14 38
From SouthBridge <- SB_INT_L 25

PP3V3_PCI 7 74 75 76 77
R2550 10K 5% 1/16W MF 402 — PCI_SLOTE_REQ_L 25
R2551 10K — PCI_SLOTE_GNT_L 25
R2552 10K — PCI_SLOTF_REQ_L 25
R2553 10K — PCI_SLOTF_GNT_L 25
R2556 10K — PCI_SLOTA_INT_L 6 25 76
R2557 10K — PCI_SLOTD_INT_L 25
R2558 10K — PCI_SLOTE_INT_L 25
R2559 10K — PCI_SLOTG_INT_L 25 77

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:05 2003

PCI 32-bit select

1 = 32-bit PCI & GPIOs
0 = 64-bit PCI & XGC
(Internal pull-up)

PCI_64BIT R2501 4.7K 5% 1/16W MF 402
R2580 4.7K 5% 1/16W MF 402

CRITICAL Y2590 18.432M 8X4.5MM-SM
SB_CLK18M_XTALO 25
R2590 200 1% 1/16W MF 402
C2590 22pF 5% 50V CERM 402
C2591 22pF 5% 50V CERM 402

PP2V5_PWRON_SB 88 74 23 7
L2500 FERR-EMI-600-OHM SM
PP2V5_PWRON_SB_XTAL18VDD VOLTAGE=2.5V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=15 mil
C2500 10uF 20% 6.3V CERM 1206
C2501 0.001uF 10% 50V CERM 402
L2510 FERR-EMI-600-OHM SM
PP2V5_PWRON_SB_XTALVDD VOLTAGE=2.5V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=15 mil
C2510 10uF 20% 6.3V CERM 1206
C2511 0.001uF 10% 50V CERM 402

Re-pin within each RPAK as necessary
DO NOT swap between RPAKs

I2S0: Audio DAC
I2S1: Soft Modem
I2S2: S/P-DIF

I2S0_DEV_TO_SB_DTI	RP2510	(I2S0_DEV_TO_SB_DTI)	W7	I2S0DTI_H
I2S0_SB_TO_DEV_DTO		I2S0_SB_TO_DEV_DTO_R	Y5	I2S0DTO_H
I2S0_MCLK		I2S0_MCLK_R	U8	I2S0MCLK_H
I2S0_BITCLK		I2S0_BITCLK_R	AA4	I2S0BITCLK_H
I2S0_SYNC		I2S0_SYNC_R	Y6	I2S0SYNC_H
I2S1_DEV_TO_SB_DTI	RP2520	(I2S1_DEV_TO_SB_DTI)	V10	I2S1DTI_H
I2S1_SB_TO_DEV_DTO		I2S1_SB_TO_DEV_DTO_R	AB5	I2S1DTO_H
I2S1_MCLK		I2S1_MCLK_R	V9	I2S1MCLK_H
I2S1_BITCLK		I2S1_BITCLK_R	AA8	I2S1BITCLK_H
I2S1_SYNC		I2S1_SYNC_R	AA7	I2S1SYNC_H
I2S1_RESET_L		(I2S1_RESET_L)	V5	GPIO_H_0
I2S2_DEV_TO_SB_DTI	RP2530	(I2S2_DEV_TO_SB_DTI)	AA5	I2S2DTI_H
I2S2_SB_TO_DEV_DTO		I2S2_SB_TO_DEV_DTO_R	Y8	I2S2DTO_H
I2S2_MCLK		I2S2_MCLK_R	Y7	I2S2MCLK_H
I2S2_BITCLK		I2S2_BITCLK_R	AB4	I2S2BITCLK_H
I2S2_SYNC		I2S2_SYNC_R	W9	I2S2SYNC_H
I2S2_RESET_L		(I2S2_RESET_L)	Y2	GPIO_H_1

AUDIO GPIO - see note on right

SB_INT_L	AB3	GPIO_H_2
MODEM_RING2SYS_L	W8	GPIO_H_3
SB_PCI_SEL32BIT	W6	PCI_SEL32BIT_H
I2C_SB_SCL	Y9	I2CCLK_H
I2C_SB_SDA	AB7	I2CDATA_H
SYS_WARM_RESET_L	E9	RESET_L
SB_STOPXTALS_L	W10	STOPXTALS_L
SMU_SUSPENDREQ_L	U11	SUSPENDREQ_L
SB_SUSPENDACK_L	V11	SUSPENDACK_L
SYS_PME_L	W18	PCI1PME_L
TP_SB_WATCHDOG	V12	INTRWD_H
JTAG_SB_TDI	AA11	TDI
JTAG_SB_TDO	W11	TDO
JTAG_SB_TCK	AB11	TCK
JTAG_SB_TMS	Y11	TMS
JTAG_SB_TRST_L	W12	TRST_L
SB_TEST_MODE_PD	A3	TEST_MODE_H
TP_SB_PLLTEST	U14	PLLTEST
TP_SB_FSTEST	V14	FSTEST
SB_CLK18M_XTALI	W13	XTAL_18_I
SB_CLK18M_XTALO_R	V13	XTAL_18_O
SB_CLK25M_ATA	U15	XTALI
	NC V15	XTALO

I2S0 | I2S1 (SCCA) | I2S2 (SCCB) | GPIO | I2C | PWR_MGT | TEST | XTALS | PCI | XGI

PP3V3_PWRON_SB 25 23 7
NO STUFF R2500 4.7K 5% 1/16W MF 402

PP1V2_PWRON_SB_PLL45VDD VOLTAGE=1.2V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=15 mil
L2520 FERR-EMI-600-OHM SM — PP1V2_PWRON_SB 7
C2521 0.001uF 10% 50V CERM 402
C2520 10uF 20% 6.3V CERM 1206
PP1V2_PWRON_SB_PLL49VDD VOLTAGE=1.2V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=15 mil
L2530 FERR-EMI-600-OHM SM
C2531 0.001uF 10% 50V CERM 402
C2530 10uF 20% 6.3V CERM 1206
PP3V3_PWRON_SB 7 23 25
C2540 0.1uF 20% 10V CERM 402

XTAL_VDD W14 | XTAL_18_VDD Y13 | PLL_45_VDD AA13 | PLL_49_VDD Y12 | VIO_PME W17

U2300 SHASTA V1.0 BGA (2 OF 8) OMIT

GPIO

PCI1REQ_3_L	U17	PCI_SLOTE_REQ_L	25
PCI1GNT_3_L	AA19	PCI_SLOTE_GNT_L	25
PCI1REQ_4_L	AB21	PCI_SLOTF_REQ_L	25
PCI1GNT_4_L	AA20	PCI_SLOTF_GNT_L	25
PCI1REQ_5_L	U16	SB_TO_SMU_INT_L	13 25
PCI1GNT_5_L	Y20	CPU_SRESET_L	25 29 30
PCI1AD_32_H	D18	SB_GPIO12	25
PCI1AD_33_H	A20	SYS_OVERTEMP_L	13 16 25 27 36
PCI1AD_34_H	F18	UDASH_SDOWN	6 94
PCI1AD_35_H	F17	UDASH_RESET_L	6 25 94
PCI1AD_36_H	G16	AGP_INT_L	49
PCI1AD_37_H	F16	PCI_SLOTA_INT_L	6 25 76
PCI1AD_38_H	A21	PCI_SLOTB_INT_L	25
PCI1AD_39_H	B21	PCI_SLOTC_INT_L	25
PCI1AD_40_H	C20	PCI_SLOTD_INT_L	25
PCI1AD_41_H	G17	PCI_SLOTE_INT_L	25
PCI1AD_42_H	G18	PCI_SLOTF_INT_L	25
PCI1AD_43_H	E19	SB_GPIO23	25
PCI1AD_44_H	F19	SB_GPIO24	25
PCI1AD_45_H	D20	SB_GPIO25	25
PCI1AD_46_H	E20	SB_SATABR_RESET_L	25
PCI1AD_47_H	C21	PCI_SLOTG_INT_L	25 77
PCI1AD_48_H	F20	FW_LOWPWR	25 90
PCI1AD_49_H	G19	ENETFW_RESET	25 87
PCI1AD_50_H	C22	SB_GPIO30	25
PCI1AD_51_H	D21	ENET_ENERGYDET	25 87
PCI1AD_52_H	G20	AUDIO_LO_DET_L	6 98
PCI1AD_53_H	D22	AUDIO_LO_METAL_PLUG_L	98
PCI1AD_54_H	K18	AUDIO_LI_DET_L	98
PCI1AD_55_H	H19	AUDIO_LI_METAL_PLUG_L	99
PCI1AD_56_H	J17	AUDIO_HP_DET_L	99
PCI1AD_57_H	F21	AUDIO_SPKR_DET_L	99
PCI1AD_58_H	G21	AUDIO_LO_MUTE_L	96
PCI1AD_59_H	H20	AUDIO_HP_MUTE_L	99
PCI1AD_60_H	J19	AUDIO_SPKR_MUTE_L	97
PCI1AD_61_H	F22	AUDIO_EXT_MCLK_SEL	99
PCI1AD_62_H	G22	AUDIO_GPIO_11	99
PCI1AD_63_H	H21	AUDIO_GPIO_12	98
PCI1C_BE_4_L	J20	I2S0_RESET_L	95
PCI1C_BE_5_L	H22	SB_GPIO45	25
PCI1C_BE_6_L	K22	SB_GPIO46	25
PCI1C_BE_7_L	K20	SB_GPIO47	25
PCI1REQ64_L	K17	SYS_SLEWING_L	13 25 27 33
PCI1ACK64_L	L17	SB_GPIO49	25
PCI1PAR64_H	E18	SB_GPIO50	25
XGI_CLK_H	Y4	SB_GPIO51	25
XGI_DTO0_H	U7	SB_GPIO52	25
XGI_DTO1_H	T9	NB_TO_SB_INT	25
XGI_DTI_H	W2	SMU_TO_SB_INT_L	13 25

"Slot E" - AD21
"Slot F" - AD22

XTAL_18 GND AB12 | PLL_45 GND AB13 | PLL_49 GND AA12

AUDIO GPIOS
NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

PP3V3_PWRON_SB 25 23 7
R2554 1K 5% 1/16W MF 402 — SB_TO_SMU_INT_L 25 13
R2555 NO STUFF 10K — CPU_SRESET_L 30 29 25
R2560 1K — SYS_OVERTEMP_L 36 27 25 16 13
R2561 10K — UDASH_RESET_L 94 25 6
R2562 NO STUFF 1K — SYS_SLEWING_L 33 27 25 13 (REDUNDANT - NEED TO ADDRESS THIS)
R2563 10K — MODEM_RING2SYS_L 94 25 6
R2564 10K — I2S1_RESET_L 94 25 6
R2565 NO STUFF 10K — SB_SATABR_RESET_L 25 (REDUNDANT - NEED TO ADDRESS THIS)
R2566 10K — FW_LOWPWR 90 25
R2567 10K — ENETFW_RESET 87 25
R2568 10K — ENET_ENERGYDET 87 25

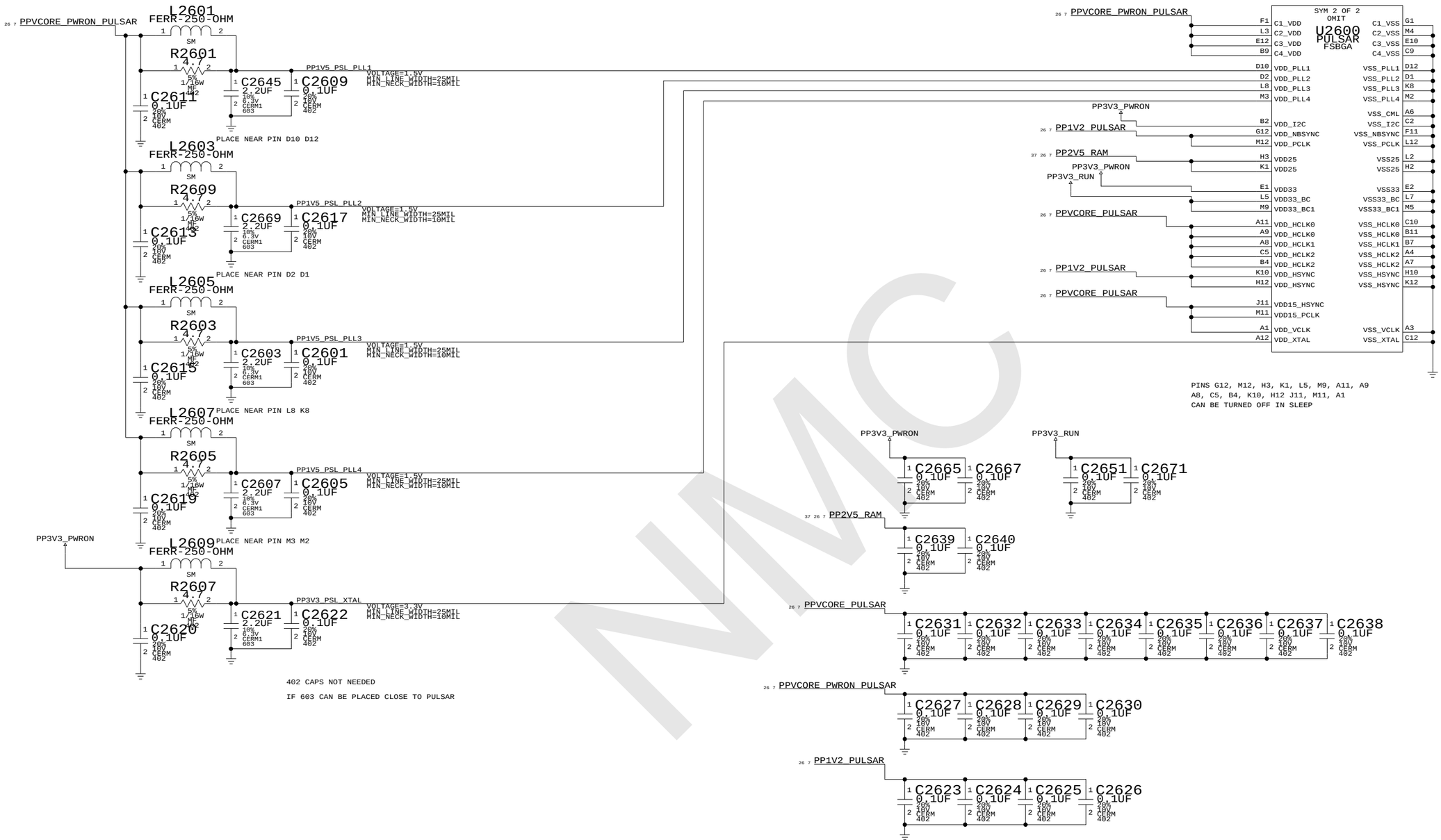
PP3V3_PWRON_SB 25 23 7
RP2550 10K — SB_GPIO12 25
RP2550 10K — PCI_SLOTB_INT_L 25
RP2550 10K — PCI_SLOTC_INT_L 25
RP2551 10K — PCI_SLOTF_INT_L 25
RP2551 10K — SB_GPIO23 25
RP2551 10K — SB_GPIO24 25
RP2550 10K — SB_GPIO25 25
RP2551 10K — SB_GPIO30 25
RP2552 10K — SB_GPIO45 25
RP2552 10K — SB_GPIO46 25
RP2552 10K — SB_GPIO47 25
RP2552 10K — SB_GPIO49 25
RP2553 10K — SB_GPIO50 25
RP2553 10K — SB_GPIO51 25
RP2553 10K — SB_GPIO52 25
RP2553 10K — SMU_TO_SB_INT_L 25 13

Master: Link

Shasta Serial / Misc

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 25 OF 99	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, PBGA	U2600	

MASTER: GILA

PULSAR POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 26 OF 99	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
EI_NB_CLK_P	EI_NB_CLK	CLOCKS	EI_NB_CLK
EI_NB_CLK_N	EI_NB_CLK	CLOCKS	EI_NB_CLK
EI_CPU_SYNC	EI_SYNC	CLOCKS	
EI_NB_SYNC		CLOCKS	
EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS	
VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS	
AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS	
HT_CLK66M_NB	HT_NB_CLK	CLOCKS	
HT_CLK66M_SB	HT_SB_CLK	CLOCKS	
PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS	
PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS	
PLS_EXTCLK	PLS_XTAL	CLOCKS	

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER
ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI_NB_SYNC IS PART OF EI_CPU_SYNC TOPOLOGY

NET SPACING TYPE

SYM 1 OF 2

OMIT
U2600
PULSAR
FSBGA

GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS	
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS	
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS	
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS	
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS	
HCLKN_1	C8	EI_CPU1_CLK_N_R	CLOCKS	14
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS	
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS	
HCLKP_1	B8	EI_CPU1_CLK_P_R	CLOCKS	14
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS	
GPCLK25_0	J3	PLS_CLK_66M_0_R	CLOCKS	
GPCLK25_1	J1	PLS_CLK_66M_1_R	CLOCKS	
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS	
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS	
PCLK33_0	K5	PCI_CLK66M_SB_INT_R	CLOCKS	
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS	
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS	
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS	
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS	
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS	
HTBEN_1	J12	CPU1_HTBEN_R	CLOCKS	14
NBSYNC	F12	EI_NB_SYNC_R	CLOCKS	
HSYNC_0	J10	EI_CPU_SYNC_R	CLOCKS	
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS	14
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS	
REFLCK_1	H1	SATA_CLK25M_R	CLOCKS	
SLEWING*	K9	SLEWING_L_R	CLOCKS	
ERROR*	M8	CLOCK_ERROR_L		8
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS	
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS	

R2701 0 5% 1 2 — 3.3V 33MHZ — PCI_CLK_GP0 — 8
R2761 0 5% 402 — 3.3V 33MHZ — PCI_CLK_GP1 — 8

C2708 0.001UF 50V 10% 2CERM 402 — VSP_NB_CLK_P — 24 27
C2710 0.001UF 50V 10% 2CERM 402 — VSP_NB_CLK_N — 24 27
C2713 0.001UF 50V 10% 2CERM 402 — EI_CPU_CLK_P — 27 29
C2715 0.001UF 50V 10% 2CERM 402 — EI_CPU_CLK_N — 27 29
C2700 0.001UF 50V 10% 2CERM 402 — EI_NB_CLK_P — 27 28
C2702 0.001UF 50V 10% 2CERM 402 — EI_NB_CLK_N — 27 28

R2775 0 5% 402	2.5V	66MHZ	TP_PLS_CLK_66M_0	6
R2776 0 5% 402	2.5V	66MHZ	TP_PLS_CLK_66M_1	6
R2703 20 5% 402	2.5V	66MHZ	HT_CLK66M_NB	27 60
R2709 20 5% 402	2.5V	66MHZ	RAM_CLK66M_NB	37
R2705 0 5% 402	3.3V	66MHZ	PCI_CLK66M_SB_INT	27 74
R2711 0 5% 402	3.3V	33MHZ	PCI_CLK_P1	8
R2707 0 5% 402	3.3V	66MHZ	AGP_CLK66M_GPU	27 49
R2702 0 5% 402	3.3V	33MHZ	PCI_CLK_P3	8
R2779 0 5% 402			PCI_CLK_P4	8
R2715 0 5% 402	1.2V	66MHZ	CPU_HTBEN	29 30
R2768 0 5% 402	1.2V		EI_NB_SYNC	27 28
R2772 0 5% 402	1.2V		EI_CPU_SYNC	27 29
R2770 20 5% 402	2.5V	25MHZ	SB_CLK25M_ATA	25
R2700 22 5% 402	2.5V	25MHZ	TP_SATA_CLK25M	6
R2717 0 5% 402	1.2V	66MHZ	HT_CLK66M_SB	27 62
R2719 0 5% 402	1.5V	66MHZ	AGP_CLK66M_NB	27 48

R2720 0 5% 402 — SYS_SLEWING_L — 13 25 33

18 I2C_CLOCK_SCL — C1 SCLK
18 I2C_CLOCK_SDA — B1 SDATA
13 CLOCK_RESET_L — R2704 0 5% 402 — PLS_RESET_L — D3 RESET*
PLS_X_IN — C11 XIN
PLS_X_OUT — B12 XOUT
NOSTUFF R2738 1K 5% 402 — PLS_X_ADDRSEL — E3 ADDRSEL
6 TP_PLS_TEST1 — K3 TEST1
6 TP_PLS_TEST2 — E11 TEST2
6 TP_PLS_TEST3 — D11 TEST3
R2706 249 1% — PLS_SCAN_MODE — M1 SCAN_MODE
R2744 681 1% — PLS_REF15 — G11 REF15
R2740 1K 1% — PLS_REF25 — J2 REF25
R2746 1K 1% — PLS_REF33 — M6 REF33
6 TP_PLS_REF_CML — A5 REF_CML
R2742 806 1% — PLS_PRES_CML — B6 PRES_CML
36 25 16 13 SYS_OVERTEMP_L — R2748 0 5% 1/16W MF 402 — PLS_FORCE_P0_L_R — F2 FORCESPO*
C3 PD
50 46 11 10 9 8 6 SYS_SLEEP (SLEEP) — R2750 0 5% — PLS_POWER_DOWN
R2724 1K 5% NOSTUFF

0=IIC ADDR D2/D3
1=IIC ADDR D4/D5

18 11 6 PP3V3_PWRON — R2722 1K 5% 1/16W MF 402 NOSTUFF

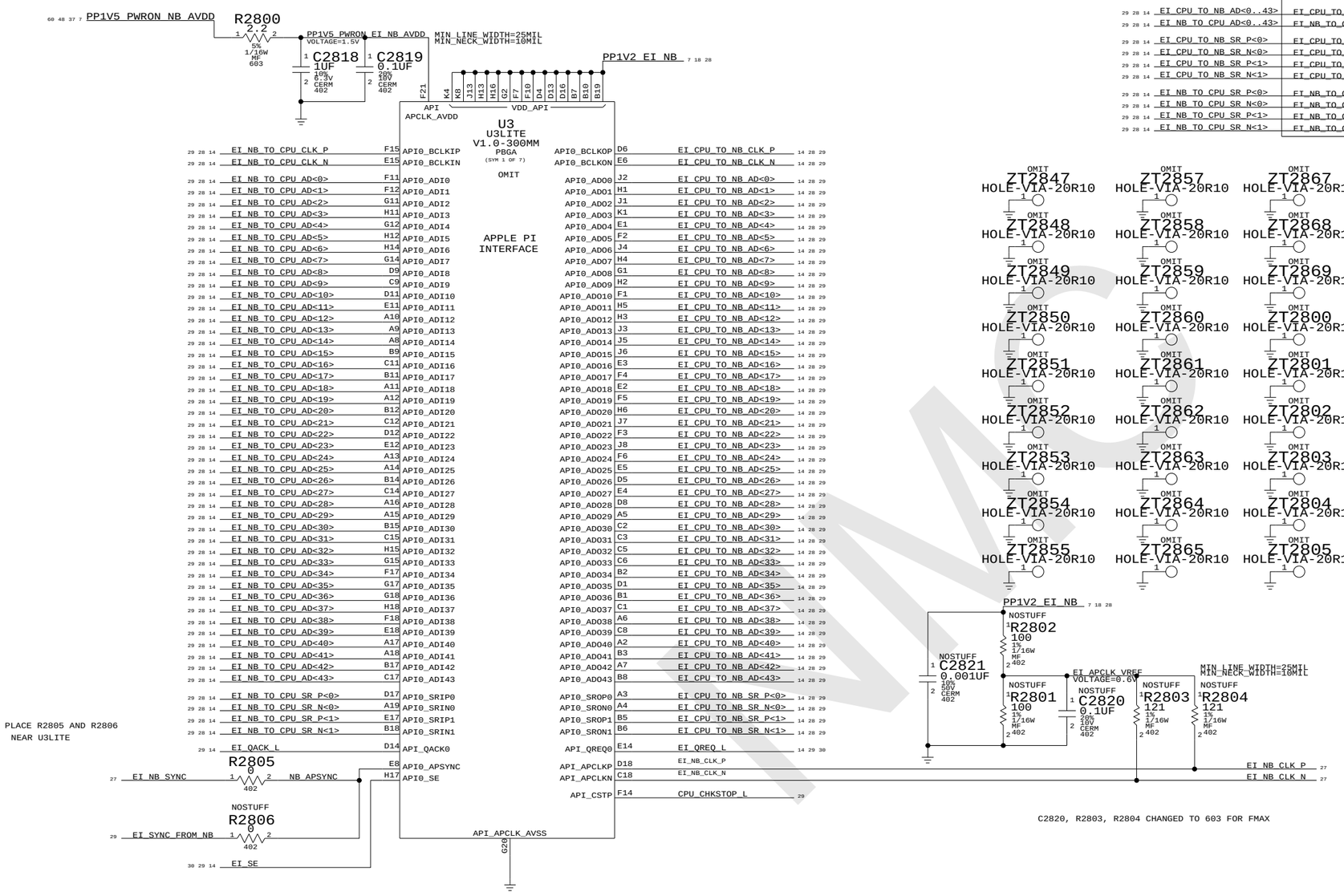
7 PLS_EXTCLK — R2752 0 5% 1/16W MF 402 NO STUFF
R2754 0 5% 1/16W MF 402
R2758 330K 5% 1/16W MF 402 NO STUFF
R2756 0 5% 1/16W MF 402
R2762 24 5% 1/16W MF 402 NOSTUFF
R2764 24 5% 1/16W MF 402 NOSTUFF
PLS_INTERM
J2700 U.FL-R_SMT F-ST-SM NOSTUFF
CRITICAL Y2701 25.0000M 8X4.5MM-SM
PLS_X_IN_B — PLS_X_OUT_B
C2707 33PF 5% 50V CERM 402
C2705 33PF 5% 50V CERM 402

MASTER: GILA

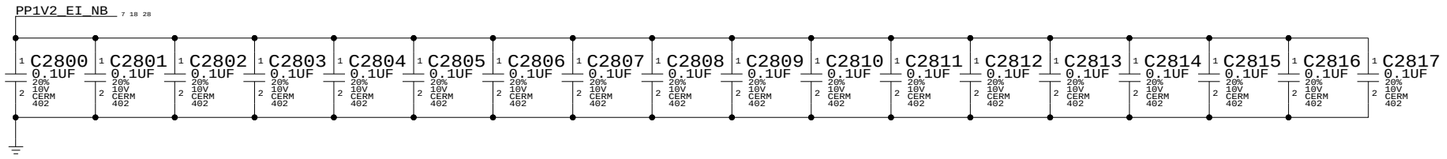
PULSAR CLOCKS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 27 OF 99	



	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_AD	
EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_AD	
EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1
EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1
EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1
EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1



MASTER: NEOBORG U3LITE

U3LITE APPLE PI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 28 OF 99	

PLACE AT PROCESSOR PINS.

PLACE NEAR PROCESSOR.

27 EI_CPU_CLK_P

27 EI_CPU_CLK_N

NOSTUFF R2903 46.4 1% 1/16W MF 402

NOSTUFF R2901 46.4 1% 1/16W MF 402

NOSTUFF C2901 0.22UF 20% 6.3V X5R 402

35 31 30 29 18 7 PP1V2_EI_CPU

NOSTUFF R2909 100 1% 1/16W MF 402

NOSTUFF R2907 100 1% 1/16W MF 402

SYSCLK_TERM VOLTAGE=0.6V

SYSCLK* SYSCLK

(SEE TABLE) OMIT CRITICAL

U2900 GPUL (1 OF 3) CBGA

28 14	EI_NB_TO_CPU_CLK_P	E24	EI_CLKI	EI_CLK	G23
28 14	EI_NB_TO_CPU_CLK_N	D24	EI_CLKI*	EI_CLK*	G22
28 14	EI_NB_TO_CPU_AD<0>	H25	EI_AD10	EI_AD0	B5
28 14	EI_NB_TO_CPU_AD<1>	J25	EI_AD11	EI_AD1	C5
28 14	EI_NB_TO_CPU_AD<2>	H27	EI_AD12	EI_AD2	E1
28 14	EI_NB_TO_CPU_AD<3>	J27	EI_AD13	EI_AD3	L1
28 14	EI_NB_TO_CPU_AD<4>	C13	EI_AD14	EI_AD4	K1
28 14	EI_NB_TO_CPU_AD<5>	A18	EI_AD15	EI_AD5	K4
28 14	EI_NB_TO_CPU_AD<6>	K28	EI_AD16	EI_AD6	E2
28 14	EI_NB_TO_CPU_AD<7>	H28	EI_AD17	EI_AD7	E3
28 14	EI_NB_TO_CPU_AD<8>	J28	EI_AD18	EI_AD8	B6
28 14	EI_NB_TO_CPU_AD<9>	G28	EI_AD19	EI_AD9	A6
28 14	EI_NB_TO_CPU_AD<10>	F28	EI_AD110	EI_AD10	F2
28 14	EI_NB_TO_CPU_AD<11>	G29	EI_AD111	EI_AD11	G3
28 14	EI_NB_TO_CPU_AD<12>	H29	EI_AD112	EI_AD12	G4
28 14	EI_NB_TO_CPU_AD<13>	K29	EI_AD113	EI_AD13	H3
28 14	EI_NB_TO_CPU_AD<14>	B18	EI_AD114	EI_AD14	H4
28 14	EI_NB_TO_CPU_AD<15>	B15	EI_AD115	EI_AD15	D11
28 14	EI_NB_TO_CPU_AD<16>	A14	EI_AD116	EI_AD16	E12
28 14	EI_NB_TO_CPU_AD<17>	C15	EI_AD117	EI_AD17	E13
28 14	EI_NB_TO_CPU_AD<18>	B15	EI_AD118	EI_AD18	E14
28 14	EI_NB_TO_CPU_AD<19>	A16	EI_AD119	EI_AD19	C11
28 14	EI_NB_TO_CPU_AD<20>	C16	EI_AD120	EI_AD20	D1
28 14	EI_NB_TO_CPU_AD<21>	E26	EI_AD121	EI_AD21	E1
28 14	EI_NB_TO_CPU_AD<22>	E25	EI_AD122	EI_AD22	E2
28 14	EI_NB_TO_CPU_AD<23>	B22	EI_AD123	EI_AD23	E3
28 14	EI_NB_TO_CPU_AD<24>	B24	EI_AD124	EI_AD24	A2
28 14	EI_NB_TO_CPU_AD<25>	F26	EI_AD125	EI_AD25	A3
28 14	EI_NB_TO_CPU_AD<26>	B25	EI_AD126	EI_AD26	A4
28 14	EI_NB_TO_CPU_AD<27>	B26	EI_AD127	EI_AD27	B4
28 14	EI_NB_TO_CPU_AD<28>	C14	EI_AD128	EI_AD28	D12
28 14	EI_NB_TO_CPU_AD<29>	C17	EI_AD129	EI_AD29	D13
28 14	EI_NB_TO_CPU_AD<30>	B16	EI_AD130	EI_AD30	B3
28 14	EI_NB_TO_CPU_AD<31>	B20	EI_AD131	EI_AD31	C4
28 14	EI_NB_TO_CPU_AD<32>	B28	EI_AD132	EI_AD32	C1
28 14	EI_NB_TO_CPU_AD<33>	A28	EI_AD133	EI_AD33	C2
28 14	EI_NB_TO_CPU_AD<34>	C18	EI_AD134	EI_AD34	A1
28 14	EI_NB_TO_CPU_AD<35>	C19	EI_AD135	EI_AD35	C3
28 14	EI_NB_TO_CPU_AD<36>	A20	EI_AD136	EI_AD36	F4
28 14	EI_NB_TO_CPU_AD<37>	A26	EI_AD137	EI_AD37	F1
28 14	EI_NB_TO_CPU_AD<38>	A24	EI_AD138	EI_AD38	B2
28 14	EI_NB_TO_CPU_AD<39>	A22	EI_AD139	EI_AD39	C6
28 14	EI_NB_TO_CPU_AD<40>	A12	EI_AD140	EI_AD40	A10
28 14	EI_NB_TO_CPU_AD<41>	A17	EI_AD141	EI_AD41	C10
28 14	EI_NB_TO_CPU_AD<42>	C12	EI_AD142	EI_AD42	A8
28 14	EI_NB_TO_CPU_AD<43>	A19	EI_AD143	EI_AD43	A9
28 14	EI_NB_TO_CPU_SR_P<0>	L2	EI_SR10	EI_SRO0	L3
28 14	EI_NB_TO_CPU_SR_N<0>	K2	EI_SR10*	EI_SRO0*	L2
28 14	EI_NB_TO_CPU_SR_P<1>	L1	EI_SR11	EI_SRO1	M1
28 14	EI_NB_TO_CPU_SR_N<1>	L2	EI_SR11*	EI_SRO1*	M2
28 14	EI_QACK_L	V2	QACK*	QREQ*	AB12
30 29 14	CHKSTOP_L	R28	CHKSTOP*	INT*	AB15
30 29 27	CPU_HTBEN	AB17	TBEN		
6	TP_PSYNCOUT	AB16	APSYNCOUT	APSYNCIN	AA10
30 14 13	CPU_HRESET_L	V26	HRESET*	IIC_SCL	AA20
30 25	CPU_SRESET_L	AB2	SRESET*	IIC_SDA	AA21
30	PROC_THERM_INT_L	V28	THERM_INT*	I2CGO	N22
30	PROCID0	L26	PROCID0	CKTERMDIS	AA14
30	PROCID1	M26	PROCID1	EI_DISABLE	J29
30	PROCID2	R26	PROCID2	BUSCFG0	AA19
30 28 14	EI_SE	N25	TRIGGER_IN	BUSCFG1	AC19
14 6	TP_PROC_TRIGGER_OUT	N26	TRIGGER_OUT	BUSCFG2	AB19
6	TP_AFN	AA12	AFN	ATTENTION	AB12
30	AVPRESET_L	W27	AVPRESET*	GPUL_DBG	AA22
30	BIMODE_L	AC25	BIMODE*	JTAGMODE	AA
30	C1UNDGLOBAL	AC23	C1UNDGLOBAL	TCK	AB21
30	C2UNDGLOBAL	AC24	C2UNDGLOBAL	TDI	AB23
30	DI2_L	V24	DI2*	TDO	AB24
30	LSSDMODE	AB6	LSSDMODE	TMS	AA22
30	LSSDSCANENABLE	V29	LSSDSCANENABLE	TRST*	W29
30	LSSDSTOPC2ENABLE	AB5	LSSDSTOPC2ENABLE	BYPASS*	Y24
30	LSSDSTOPC2STARENABLE	AB4	LSSDSTOPC2STARENABLE	PLLLOCK	T28
30	LSSDSTOPENABLE	AB13	LSSDSTOPENABLE	PLLMULT	AA8
29 14	MCP_L	AB14	MCP*	PLLRANGE0	AB7
6	TP_PSRO1	V22	PSRO1	PLLRANGE1	AA9
6	TP_PSRO2	V5	PSRO2	PLLTEST	V22
30	PULSESEL0	AC26	PULSESEL0	PLLTESTOUT	T19
30	PULSESEL1	AB11	PULSESEL1	SPARE	AA13
30	PULSESEL2	AC16	PULSESEL2		
30	RAMSTOPENABLE	AB3	RAMSTOPENABLE		
30 14	RI_L	AC1	RI*		
30 14	SYNCENABLE	AA25	SYNCENABLE*		

28 14	EI_CPU_TO_NB_CLK_P	14 28	EI_CPU_TO_NB_AD<0>	14 28	EI_CPU_TO_NB_AD<32>	14 28
28 14	EI_CPU_TO_NB_CLK_N	14 28	EI_CPU_TO_NB_AD<1>	14 28	EI_CPU_TO_NB_AD<33>	14 28
			EI_CPU_TO_NB_AD<2>	14 28	EI_CPU_TO_NB_AD<34>	14 28
			EI_CPU_TO_NB_AD<3>	14 28	EI_CPU_TO_NB_AD<35>	14 28
			EI_CPU_TO_NB_AD<4>	14 28	EI_CPU_TO_NB_AD<36>	14 28
			EI_CPU_TO_NB_AD<5>	14 28	EI_CPU_TO_NB_AD<37>	14 28
			EI_CPU_TO_NB_AD<6>	14 28	EI_CPU_TO_NB_AD<38>	14 28
			EI_CPU_TO_NB_AD<7>	14 28	EI_CPU_TO_NB_AD<39>	14 28
			EI_CPU_TO_NB_AD<8>	14 28	EI_CPU_TO_NB_AD<40>	14 28
			EI_CPU_TO_NB_AD<9>	14 28	EI_CPU_TO_NB_AD<41>	14 28
			EI_CPU_TO_NB_AD<10>	14 28	EI_CPU_TO_NB_AD<42>	14 28
			EI_CPU_TO_NB_AD<11>	14 28	EI_CPU_TO_NB_AD<43>	14 28
			EI_CPU_TO_NB_AD<12>	14 28		
			EI_CPU_TO_NB_AD<13>	14 28		
			EI_CPU_TO_NB_AD<14>	14 28		
			EI_CPU_TO_NB_AD<15>	14 28		
			EI_CPU_TO_NB_AD<16>	14 28		
			EI_CPU_TO_NB_AD<17>	14 28		
			EI_CPU_TO_NB_AD<18>	14 28		
			EI_CPU_TO_NB_AD<19>	14 28		
			EI_CPU_TO_NB_AD<20>	14 28		
			EI_CPU_TO_NB_AD<21>	14 28		
			EI_CPU_TO_NB_AD<22>	14 28		
			EI_CPU_TO_NB_AD<23>	14 28		
			EI_CPU_TO_NB_AD<24>	14 28		
			EI_CPU_TO_NB_AD<25>	14 28		
			EI_CPU_TO_NB_AD<26>	14 28		
			EI_CPU_TO_NB_AD<27>	14 28		
			EI_CPU_TO_NB_AD<28>	14 28		
			EI_CPU_TO_NB_AD<29>	14 28		
			EI_CPU_TO_NB_AD<30>	14 28		
			EI_CPU_TO_NB_AD<31>	14 28		
			EI_CPU_TO_NB_SR_P<0>	14 28		
			EI_CPU_TO_NB_SR_N<0>	14 28		
			EI_CPU_TO_NB_SR_P<1>	14 28		
			EI_CPU_TO_NB_SR_N<1>	14 28		
			EI_QREQ_L	14 28 30		
			CPU_INT_L	14 25 30		
			CPU_APSYNC			
			I2C_CPU_A_SCL	18		
			I2C_CPU_A_SDA	18		
			I2CGO	30		
			CKTERMDIS_L	30		
			EI_DISABLE	30		
			BUSCFG0	30		
			BUSCFG1	30		
			BUSCFG2	30		
			TP_ATTENTION	6		
			GPUL_DBG	30		
			JTAGMODE_SPARE2	30		
			JTAG_CPU_TCK	18 30		
			JTAG_CPU_TDI	18 30		
			JTAG_CPU_TDO	18 30		
			JTAG_CPU_TMS	18 30		
			JTAG_CPU_TRST_L	18 30		
			CPU_BYPASS_L	13 30		
			PLLLOCK	30		
			PLLMULT	30		
			PLLRANGE0	30		
			PLLRANGE1	30		
			PLLTEST	30		
			PLLTESTOUT	30		
			CPU_SPARE	30		

MATCH TO SYSCLK

R2910 0 5% 1/16W MF 402 — EI_CPU_SYNC 27

NOSTUFF R2911 0 5% 1/16W MF 402 — EI_SYNC_FROM_NB 28

PROCESSOR IIC ADDRESS: 80,84

36 35 34 33 32 31 7 6 PPVCORE_CPU

MORE PROCESSOR DECOUPLING ON PAGES 31 & 32

C2953	C2947	C2945	C2939	C2937	C2928	C2924	C2920	C2914	C2912
C2954	C2948	C2946	C2940	C2938	C2929	C2925	C2921	C2915	C2913
C2955	C2951	C2949	C2943	C2941	C2930	C2926	C2922	C2918	C2916
C2956	C2952	C2950	C2944	C2942	C2931	C2927	C2923	C2919	C2917
C2900	C2960	C2959	C2958	C2957	C2936	C2935	C2934	C2933	C2932
C2911	C2910	C2909	C2908	C2907	C2906	C2905	C2904	C2903	C2902

All: 1UF 10% 6.3V CERM 402

NOSTUFF R2905 49.9 1% 1/16W MF 402 — 30 29 27 CPU_HTBEN

PLACE BY PROCESSOR PIN.

35 31 30 29 18 7 PP1V2_EI_CPU

R2906 1K 5% 1/16W MF 402

R2908 1K 5% 1/16W MF 402

R2902 0 5% 1/16W MF 402 — 28 CPU_CHKSTOP_L

NOSTUFF R2904 0 5% 1/16W MF 402

CHKSTOP_L 14 29 30

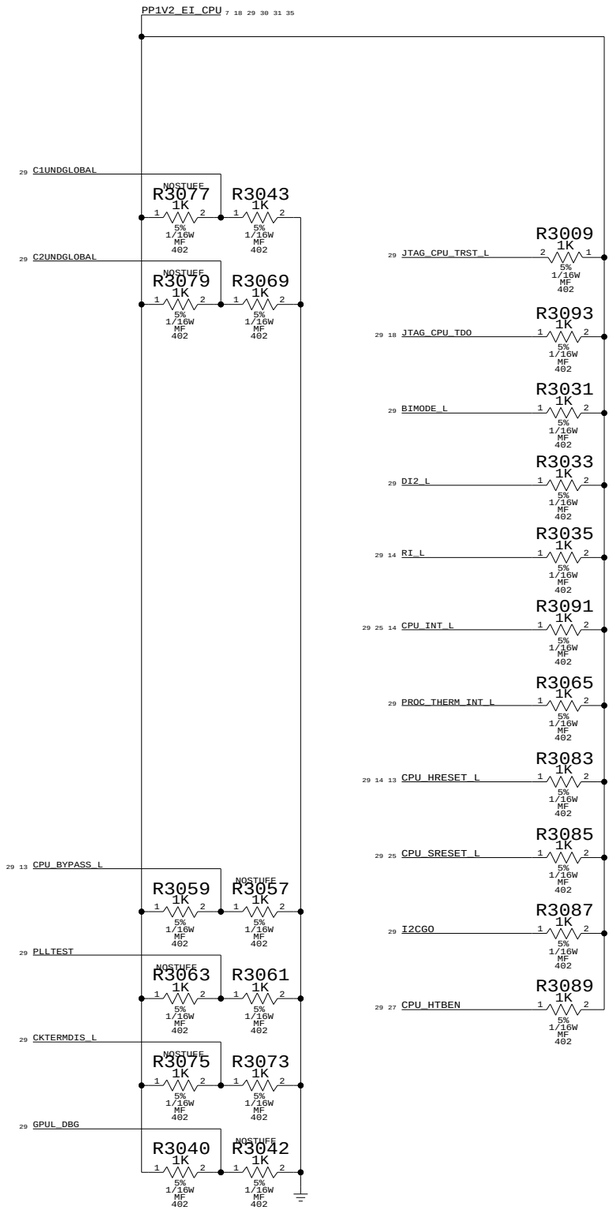
MCP_L 14 29

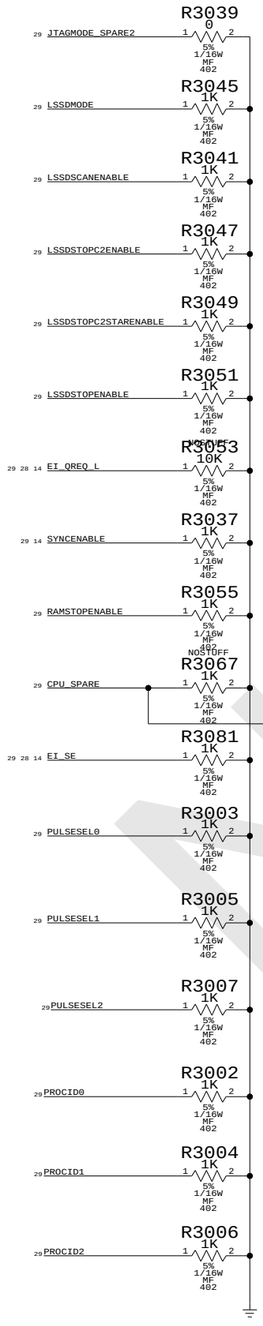
PROCESSOR LOGIC I/O

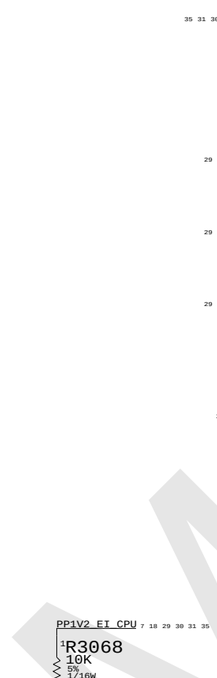
APPLE COMPUTER INC.

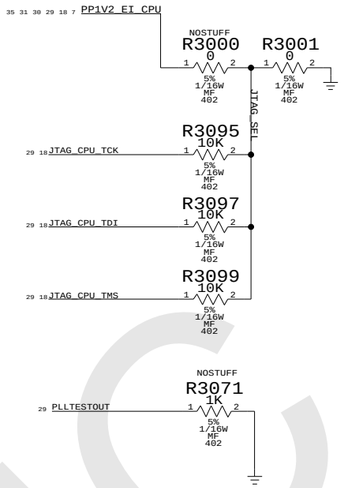
SIZE D | DRAWING NUMBER 051-6482 | REV. 13

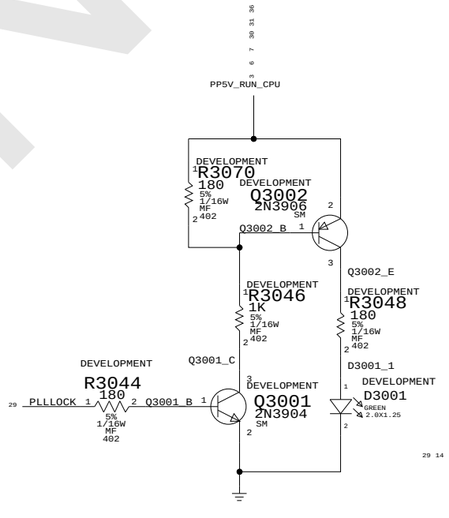
SCALE NONE | SHT 29 OF 99

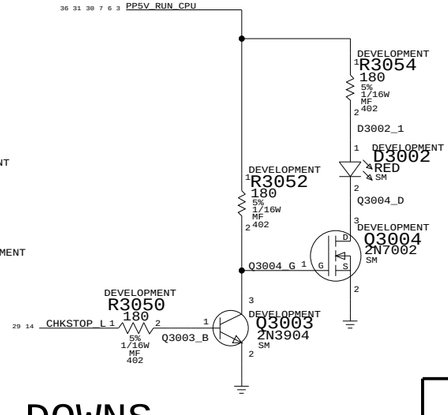


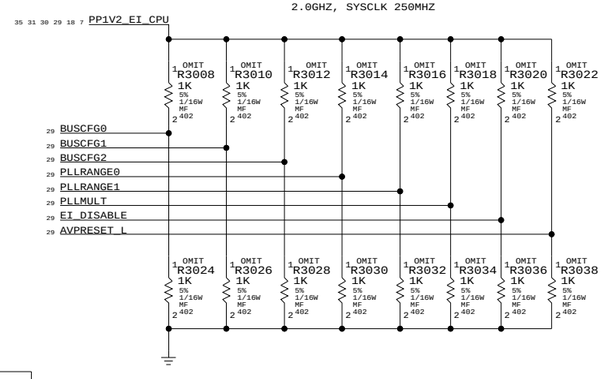












SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	NOSTUFF	SYSCLK * 12
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018		SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028		PROC / 2
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	NOSTUFF	PROC / 3
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF	PROC / 12
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036		
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	NOSTUFF	900 TO 1800 MHZ
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	NOSTUFF	1.8 TO 3.6 GHZ
*	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032		1.2 TO 2.4 GHZ
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022		AVPRESET OFF
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION

CPU SPEED 1.8GHZ, SYSCLK 225MHZ
2.0GHZ, SYSCLK 250MHZ

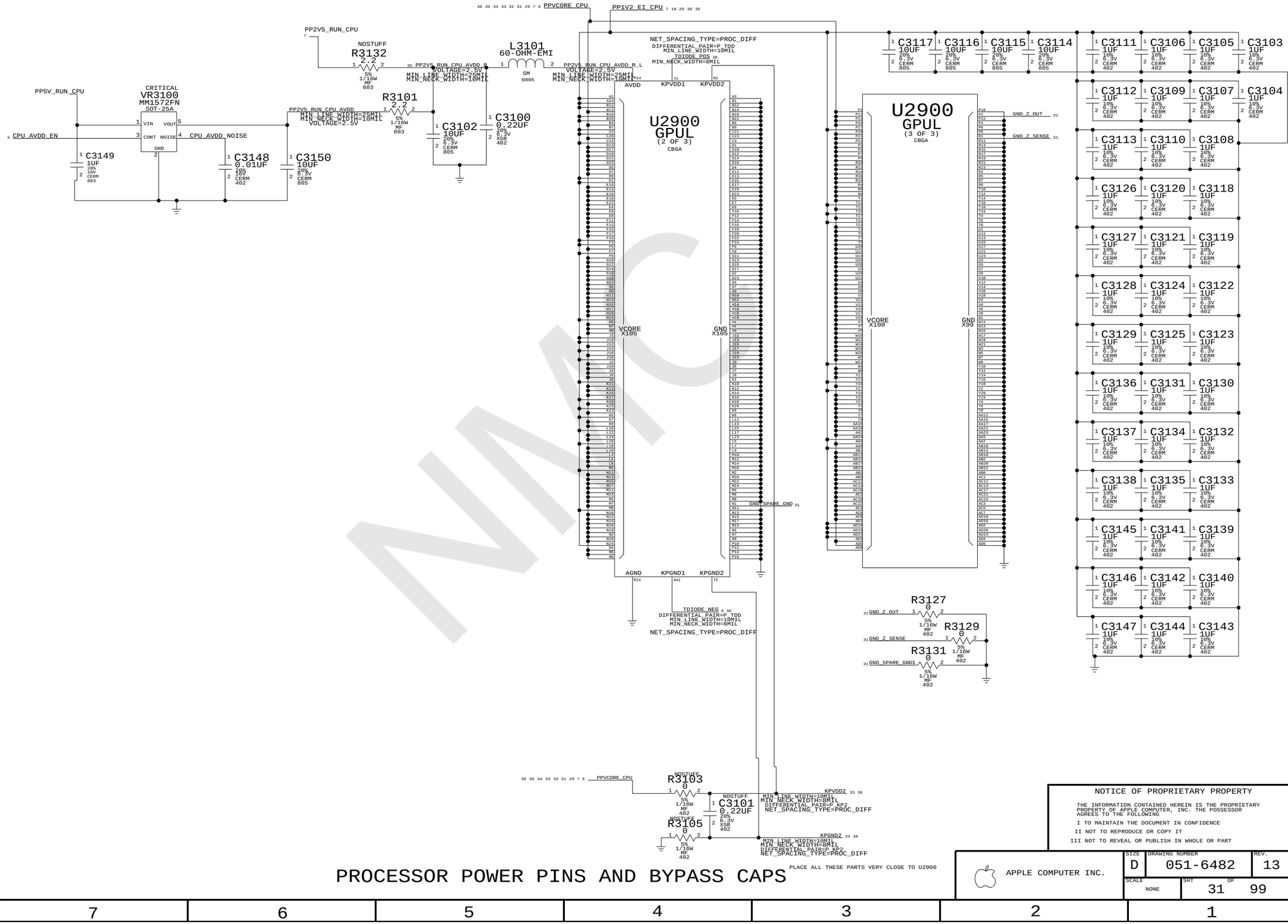
MASTER: GILA

CPU STRAPS

PROCESSOR PULL-UPS AND -DOWNS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 30 OF 99	



PROCESSOR POWER PINS AND BYPASS CAPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT	OF
NONE	31	99

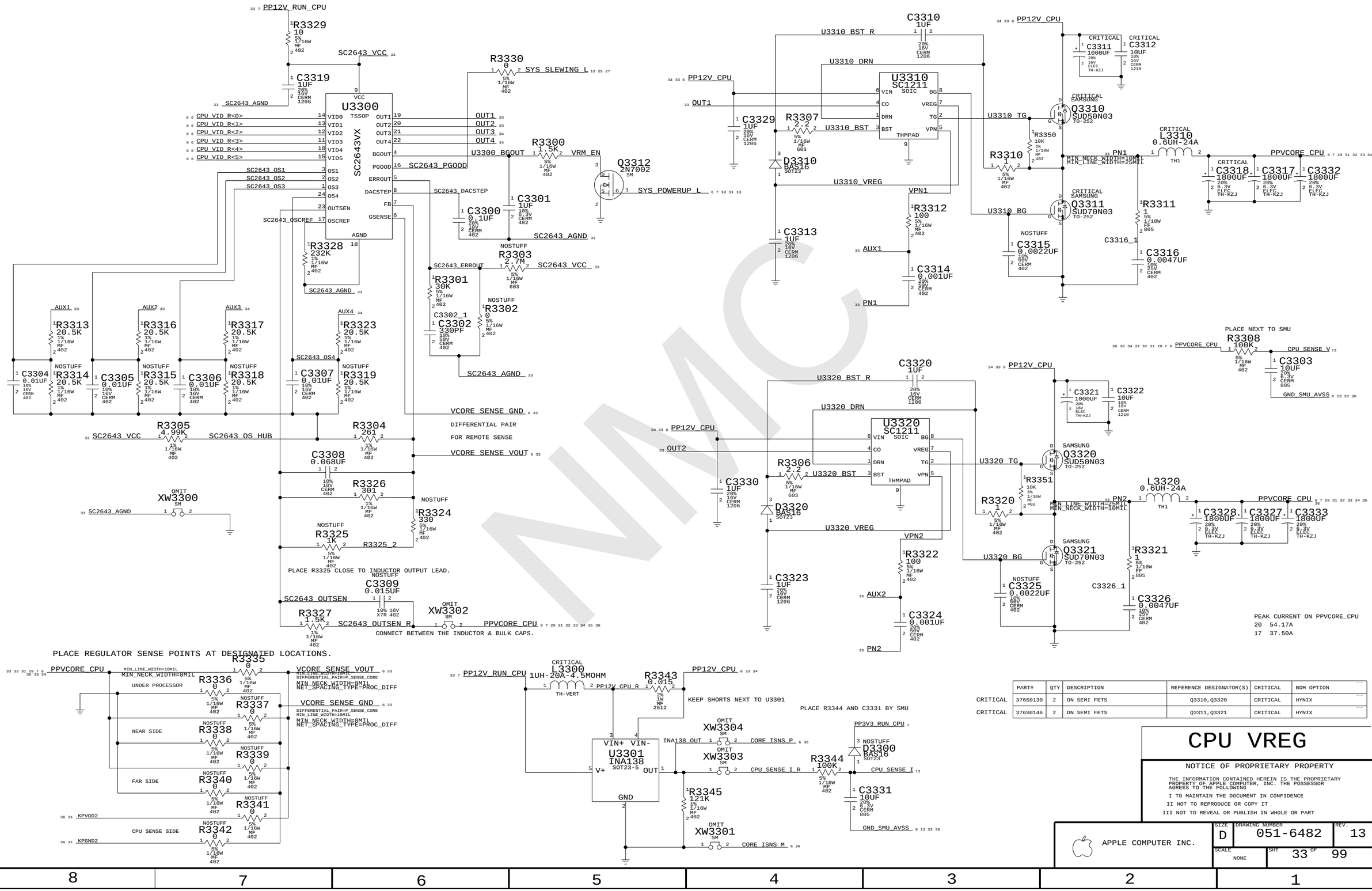
36 35 34 33 31 29 7 6 PPVCORE_CPU

C3222 1UF 10% 6.3V CERM 402	C3221 1UF 10% 6.3V CERM 402	C3220 1UF 10% 6.3V CERM 402	C3219 1UF 10% 6.3V CERM 402	C3218 1UF 10% 6.3V CERM 402	C3217 1UF 10% 6.3V CERM 402	C3216 1UF 10% 6.3V CERM 402	C3215 1UF 10% 6.3V CERM 402	C3212 1UF 10% 6.3V CERM 402	C3200 1UF 10% 6.3V CERM 402
C3293 1UF 10% 6.3V CERM 402	C3268 1UF 10% 6.3V CERM 402	C3261 1UF 10% 6.3V CERM 402	C3259 1UF 10% 6.3V CERM 402	C3235 1UF 10% 6.3V CERM 402	C3232 1UF 10% 6.3V CERM 402	C3226 1UF 10% 6.3V CERM 402	C3224 1UF 10% 6.3V CERM 402	C3245 1UF 10% 6.3V CERM 402	C3223 1UF 10% 6.3V CERM 402
C3294 1UF 10% 6.3V CERM 402	C3269 1UF 10% 6.3V CERM 402	C3264 1UF 10% 6.3V CERM 402	C3260 1UF 10% 6.3V CERM 402	C3236 1UF 10% 6.3V CERM 402	C3233 1UF 10% 6.3V CERM 402	C3227 1UF 10% 6.3V CERM 402	C3225 1UF 10% 6.3V CERM 402	C3256 1UF 10% 6.3V CERM 402	C3234 1UF 10% 6.3V CERM 402
C3295 1UF 10% 6.3V CERM 402	C3271 1UF 10% 6.3V CERM 402	C3265 1UF 10% 6.3V CERM 402	C3262 1UF 10% 6.3V CERM 402	C3239 1UF 10% 6.3V CERM 402	C3237 1UF 10% 6.3V CERM 402	C3230 1UF 10% 6.3V CERM 402	C3228 1UF 10% 6.3V CERM 402	C3289 1UF 10% 6.3V CERM 402	C3267 1UF 10% 6.3V CERM 402
C3296 1UF 10% 6.3V CERM 402	C3270 1UF 10% 6.3V CERM 402	C3266 1UF 10% 6.3V CERM 402	C3263 1UF 10% 6.3V CERM 402	C3240 1UF 10% 6.3V CERM 402	C3238 1UF 10% 6.3V CERM 402	C3231 1UF 10% 6.3V CERM 402	C3229 1UF 10% 6.3V CERM 402	C3201 1UF 10% 6.3V CERM 402	C3278 1UF 10% 6.3V CERM 402
C3297 1UF 10% 6.3V CERM 402	C3282 1UF 10% 6.3V CERM 402	C3276 1UF 10% 6.3V CERM 402	C3272 1UF 10% 6.3V CERM 402	C3252 1UF 10% 6.3V CERM 402	C3250 1UF 10% 6.3V CERM 402	C3243 1UF 10% 6.3V CERM 402	C3241 1UF 10% 6.3V CERM 402	C3206 1UF 10% 6.3V CERM 402	C3204 1UF 10% 6.3V CERM 402
C3298 1UF 10% 6.3V CERM 402	C3281 1UF 10% 6.3V CERM 402	C3277 1UF 10% 6.3V CERM 402	C3273 1UF 10% 6.3V CERM 402	C3253 1UF 10% 6.3V CERM 402	C3251 1UF 10% 6.3V CERM 402	C3244 1UF 10% 6.3V CERM 402	C3242 1UF 10% 6.3V CERM 402	C3207 1UF 10% 6.3V CERM 402	C3205 1UF 10% 6.3V CERM 402
C3299 1UF 10% 6.3V CERM 402	C3284 1UF 10% 6.3V CERM 402	C3279 1UF 10% 6.3V CERM 402	C3274 1UF 10% 6.3V CERM 402	C3257 1UF 10% 6.3V CERM 402	C3254 1UF 10% 6.3V CERM 402	C3248 1UF 10% 6.3V CERM 402	C3246 1UF 10% 6.3V CERM 402	C3210 1UF 10% 6.3V CERM 402	C3208 1UF 10% 6.3V CERM 402
C3202 1UF 10% 6.3V CERM 402	C3283 1UF 10% 6.3V CERM 402	C3280 1UF 10% 6.3V CERM 402	C3275 1UF 10% 6.3V CERM 402	C3258 1UF 10% 6.3V CERM 402	C3255 1UF 10% 6.3V CERM 402	C3249 1UF 10% 6.3V CERM 402	C3247 1UF 10% 6.3V CERM 402	C3211 1UF 10% 6.3V CERM 402	C3209 1UF 10% 6.3V CERM 402
C3203 1UF 10% 6.3V CERM 402	C3292 1UF 10% 6.3V CERM 402	C3291 1UF 10% 6.3V CERM 402	C3290 1UF 10% 6.3V CERM 402	C3288 1UF 10% 6.3V CERM 402	C3287 1UF 10% 6.3V CERM 402	C3286 1UF 10% 6.3V CERM 402	C3285 1UF 10% 6.3V CERM 402	C3214 1UF 10% 6.3V CERM 402	C3213 1UF 10% 6.3V CERM 402

PROC DECOUPLING

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE NONE	SHT 32 OF 99	

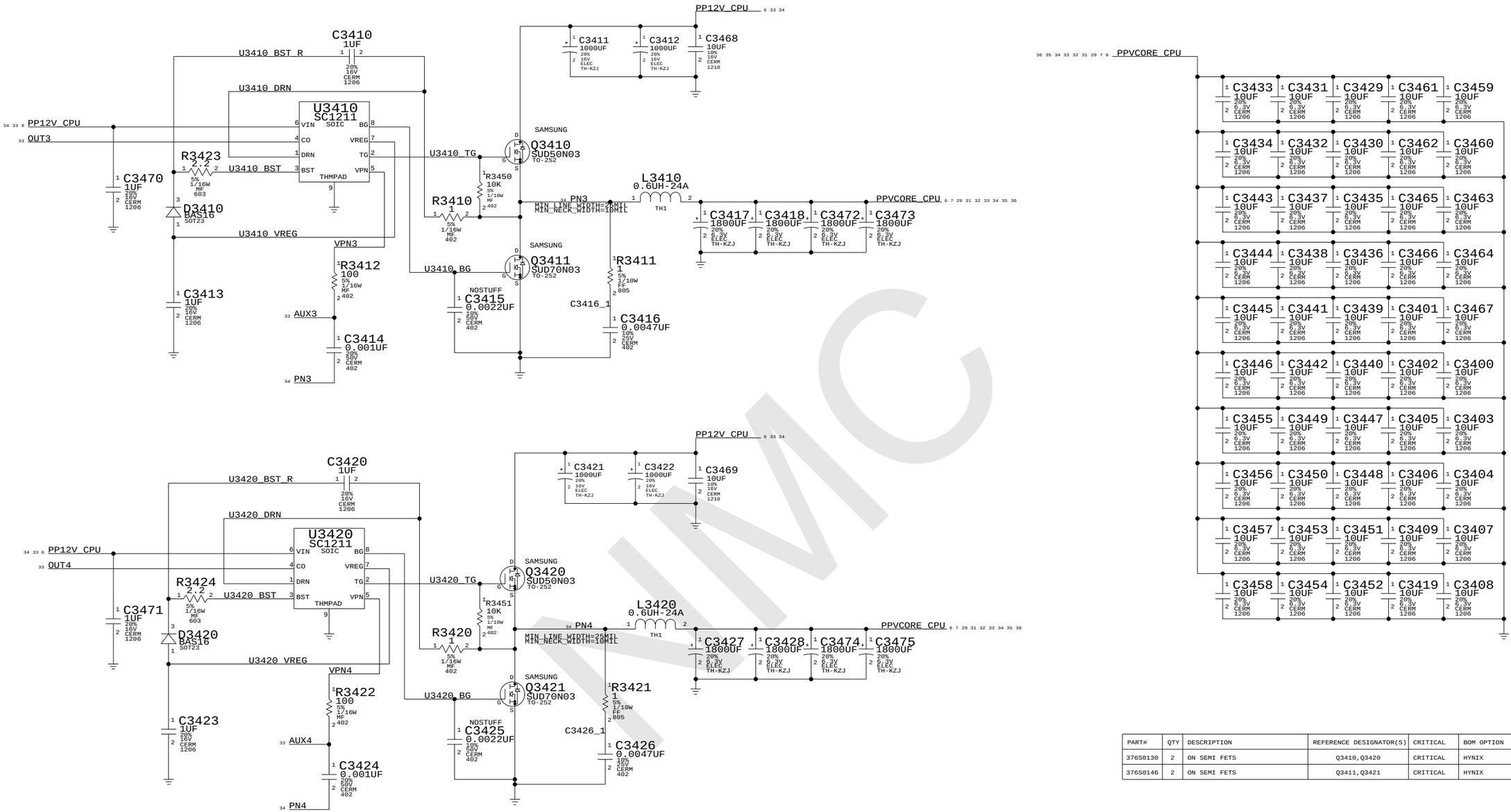


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
CRITICAL	376S0130	2	ON SEMI FETS	Q3310,Q3320	CRITICAL	HYNIX
CRITICAL	376S0146	2	ON SEMI FETS	Q3311,Q3321	CRITICAL	HYNIX

CPU VREG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 33 OF 99	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0130	2	ON SEMI FETS	Q3410,Q3420	CRITICAL	HYNIX
376S0146	2	ON SEMI FETS	Q3411,Q3421	CRITICAL	HYNIX

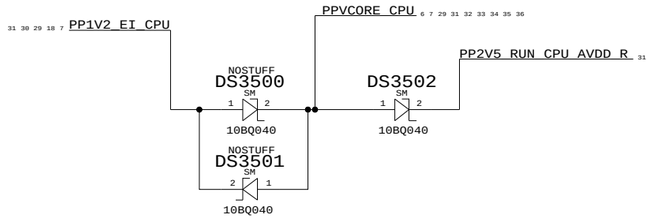
CPU VREG

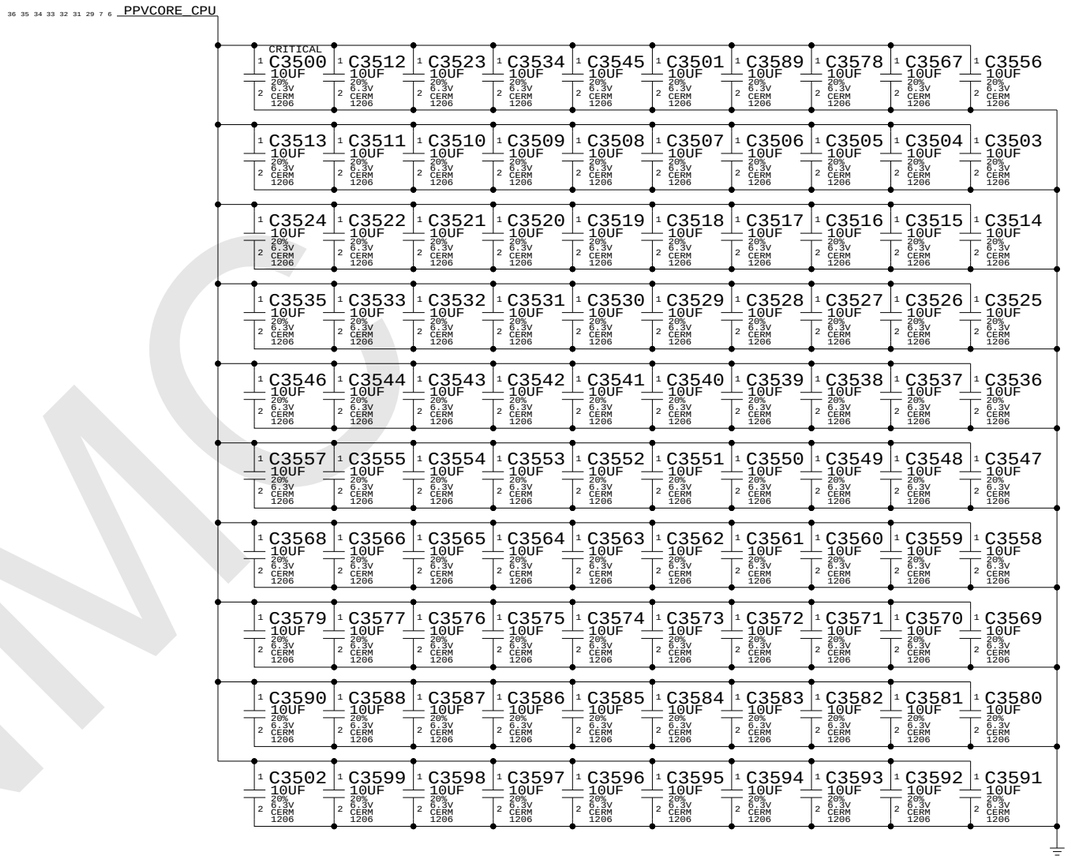
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE: NONE

SHT 34 OF 99





CPU VREG OUTPUT CAPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 35 OF 99	

POWER MONITOR

PP5V_PWRON_CPU
R3602 2 5% 1/16W MF 603
C3603 2.2UF 20% 10V CERM 805
C3604 2.2UF 20% 10V CERM 805
C3605 2.2UF 20% 10V CERM 805
C3600 2.2UF 20% 10V CERM 805
MIN_LINE_WIDTH=15MIL
MIN_NECK_WIDTH=10MIL
DAVDD
XW3601 SM OMIT
DAGND
XW3600 MUST BE PLACED CLOSE TO SMU

THESE SIGNALS HAVE A MIN_LINE_WIDTH=10MIL AND MIN_NECK_WIDTH=8MIL

100UA CURRENT SOURCE
R3606 10K 0.1% 1/16W FF 603
R3603 10K 0.1% 1/16W FF 603
TD_CURRENT
U3601 LMV2011 SOT23-5
R3604 20K 0.1% 1/16W FF 603
ADC_REF
R3607 20K 0.1% 1/16W FF 603
R3605 10K 0.1% 1/16W FF 603
DAGND
BUFFER
U3602 LMV2011 SOT23-5
R3608 12.7K 1% 1/16W MF 603
TD_BUFFERED
MIN_LINE_WIDTH=10MIL
MIN_NECK_WIDTH=8MIL
C3607 10UF 20% 6.3V CERM 805
R3609 10K 0.1% 1/16W FF 603
R3611 158K 1% 1/16W MF 603
R3612 36.5K 0.5% 1/16W FF 603
U3603 LMV2011 SOT23-5
R3610 10K 0.1% 1/16W FF 603
R3613 36.5K 0.5% 1/16W FF 603
R3614 158K 1% 1/16W MF 603
C3608 10UF 20% 6.3V CERM 805
TDIODE_POS
TDIODE_NEG
C3610 0.0022UF 10% 50V CERM 402
C3606 0.0022UF 10% 50V CERM 402
PPVCORE_CPU
NOSTUFF R3616 1K 1% 1/16W MF 402
R3615 0 5% 1/16W MF 402
CPU_TEMP_R
R3628 100K 5% 1/16W MF 402
CPU_TEMP
MIN_LINE_WIDTH=10MIL
MIN_NECK_WIDTH=8MIL
C3613 10UF 20% 6.3V CERM 805
GND_SMU_AVSS
NEED TO CONNECT TO P65 OF 80PIN SMU OR PIN 49 OF 64PIN SMU

PP5V_RUN_CPU
DEVELOPMENT
R3600 100 5% 1/16W MF 402
LED3600P1
D3610 RED SM
LED3600P2
C3609 2.2UF 20% 10V CERM 805
U3600 LM393 SOI
U3600P3
SYS_OVERTEMP_L
TP_CMP_SPARE
GND
Q3600 2N3906 SM
Q3600_B
R3627 1K 5% 1/16W MF 402
ADC_REF
R3618 1K 0.1% 1/16W FF 603
R3617 10K 0.1% 1/16W FF 603
DAGND

CHANNEL | SOURCE | VOLT SCALE | COUNT SCALE
0 | U21 TEMPERATURE | - | 0.25 C/CNT
1 | PROC TEMPERATURE | 50C/V | 0.125 C/CNT
2 | 12V CURRENT | 5A/V | 0.01221A/CNT
3 | PROC VOLTAGE | 1V/V | 0.00244V/CNT

PP3V3_PWRON_CPU
R3601 200 1% 1/16W MF 603
C3601 2.2UF 20% 10V CERM 805
ADC_REF
MIN_LINE_WIDTH=10MIL
MIN_NECK_WIDTH=8MIL
R3690 0 5% 1/16W MF 402
PPVREF_SMU_ADC_REF
D3600 2.5V SSOT-23
C3602 0.47UF 20% 10V CERM 603
R3691 0 5% 1/16W MF 402
GND_SMU_AVSS_DAGND
NEEDED FOR FMAX

NOSTUFF J3600 BM12B-SRSS-TB F-ST-SM
PLACE CLOSE TO U2900
XW3611 SM OMIT
XW3612 SM OMIT
XW3613 SM OMIT
XW3614 SM OMIT
KPVDD2_FMAX
KPGND2_FMAX
TDIODE_POS_FMAX
TDIODE_NEG_FMAX
CORE_ISNS_M
CORE_ISNS_P
DIFFERENTIAL_PAIR=KP2_FMAX
DIFFERENTIAL_PAIR=TDIODE
DIFFERENTIAL_PAIR=CORE_ISNS
MIN_LINE_WIDTH=10MIL
MIN_NECK_WIDTH=8MIL
NET_SPACING_TYPE=PROC_DIFF

NOSTUFF R3620 51 5% 1/16W MF 402
CPU_TEMP
FMAX_P
FMAX_M
NO_TEST
DIFFERENTIAL_PAIR=P_FMAX
NET_SPACING_TYPE=PROC_DIFF
NOSTUFF R3619 0 5% 1/10W FF 805
NOSTUFF R3621 51 5% 1/16W MF 402
PLACE AT BOARD EDGE

SHAMPOO IS BETTER!!

CPU DIODE CONDITIONER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 36 OF 99	

U3LITE'S MAIN MEMORY INTERFACE CAN BE TURNED OFF IN SLEEP

U3TWINS DO NOT HAVE MASKS

37 26 7 PP2V5_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 2 OF 7) OMIT

MEMORY DATA INTERFACE

RAM_DQ_R<0>	AF20	DDR_DQ0	DDR_DQ64	AG27	RAM_DQ_R<64>		
RAM_DQ_R<1>	AH22	DDR_DQ1	DDR_DQ65	AF24	RAM_DQ_R<65>		
RAM_DQ_R<2>	AH21	DDR_DQ2	DDR_DQ66	AE24	RAM_DQ_R<66>		
RAM_DQ_R<3>	AG21	DDR_DQ3	DDR_DQ67	AG26	RAM_DQ_R<67>		
RAM_DQ_R<4>	AB20	DDR_DQ4	DDR_DQ68	AF26	RAM_DQ_R<68>		
RAM_DQ_R<5>	AC21	DDR_DQ5	DDR_DQ69	AD24	RAM_DQ_R<69>		
RAM_DQ_R<6>	AD23	DDR_DQ6	DDR_DQ70	AD25	RAM_DQ_R<70>		
RAM_DQ_R<7>	AD21	DDR_DQ7	DDR_DQ71	AG28	RAM_DQ_R<71>		
RAM_DQ_R<8>	AH26	DDR_DQ8	DDR_DQ72	AF28	RAM_DQ_R<72>		
RAM_DQ_R<9>	AH25	DDR_DQ9	DDR_DQ73	AE28	RAM_DQ_R<73>		
RAM_DQ_R<10>	AH24	DDR_DQ10	DDR_DQ74	AD26	RAM_DQ_R<74>		
RAM_DQ_R<11>	AH23	DDR_DQ11	DDR_DQ75	AF27	RAM_DQ_R<75>		
RAM_DQ_R<12>	AH27	DDR_DQ12	DDR_DQ76	AC26	RAM_DQ_R<76>		
RAM_DQ_R<13>	AG24	DDR_DQ13	DDR_DQ77	AC25	RAM_DQ_R<77>		
RAM_DQ_R<14>	AF23	DDR_DQ14	DDR_DQ78	AC27	RAM_DQ_R<78>		
RAM_DQ_R<15>	AH28	DDR_DQ15	DDR_DQ79	AD27	RAM_DQ_R<79>		
RAM_DQ_R<16>	U25	DDR_DQ16	DDR_DQ80	AA27	RAM_DQ_R<80>		
RAM_DQ_R<17>	AA23	DDR_DQ17	DDR_DQ81	AA26	RAM_DQ_R<81>		
RAM_DQ_R<18>	Y22	DDR_DQ18	DDR_DQ82	AA24	RAM_DQ_R<82>		
RAM_DQ_R<19>	AA22	DDR_DQ19	DDR_DQ83	AA28	RAM_DQ_R<83>		
RAM_DQ_R<20>	U24	DDR_DQ20	DDR_DQ84	Y26	RAM_DQ_R<84>		
RAM_DQ_R<21>	V23	DDR_DQ21	DDR_DQ85	Y25	RAM_DQ_R<85>		
RAM_DQ_R<22>	V22	DDR_DQ22	DDR_DQ86	Y28	RAM_DQ_R<86>		
RAM_DQ_R<23>	U22	DDR_DQ23	DDR_DQ87	Y24	RAM_DQ_R<87>		
RAM_DQ_R<24>	P25	DDR_DQ24	DDR_DQ88	V26	RAM_DQ_R<88>		
RAM_DQ_R<25>	R22	DDR_DQ25	DDR_DQ89	V27	RAM_DQ_R<89>		
RAM_DQ_R<26>	R21	DDR_DQ26	DDR_DQ90	V24	RAM_DQ_R<90>		
RAM_DQ_R<27>	U23	DDR_DQ27	DDR_DQ91	W28	RAM_DQ_R<91>		
RAM_DQ_R<28>	P26	DDR_DQ28	DDR_DQ92	U27	RAM_DQ_R<92>		
RAM_DQ_R<29>	R24	DDR_DQ29	DDR_DQ93	V28	RAM_DQ_R<93>		
RAM_DQ_R<30>	P24	DDR_DQ30	DDR_DQ94	T28	RAM_DQ_R<94>		
RAM_DQ_R<31>	P23	DDR_DQ31	DDR_DQ95	U26	RAM_DQ_R<95>		
RAM_DQ_R<32>	M25	DDR_DQ32	DDR_DQ96	R27	RAM_DQ_R<96>		
RAM_DQ_R<33>	M23	DDR_DQ33	DDR_DQ97	R26	RAM_DQ_R<97>		
RAM_DQ_R<34>	P21	DDR_DQ34	DDR_DQ98	R28	RAM_DQ_R<98>		
RAM_DQ_R<35>	P22	DDR_DQ35	DDR_DQ99	P27	RAM_DQ_R<99>		
RAM_DQ_R<36>	M24	DDR_DQ36	DDR_DQ100	M28	RAM_DQ_R<100>		
RAM_DQ_R<37>	L22	DDR_DQ37	DDR_DQ101	N28	RAM_DQ_R<101>		
RAM_DQ_R<38>	L23	DDR_DQ38	DDR_DQ102	L28	RAM_DQ_R<102>		
RAM_DQ_R<39>	J23	DDR_DQ39	DDR_DQ103	P28	RAM_DQ_R<103>		
RAM_DQ_R<40>	D23	DDR_DQ40	DDR_DQ104	L25	RAM_DQ_R<104>		
RAM_DQ_R<41>	D24	DDR_DQ41	DDR_DQ105	L26	RAM_DQ_R<105>		
RAM_DQ_R<42>	C26	DDR_DQ42	DDR_DQ106	L27	RAM_DQ_R<106>		
RAM_DQ_R<43>	C27	DDR_DQ43	DDR_DQ107	K28	RAM_DQ_R<107>		
RAM_DQ_R<44>	A22	DDR_DQ44	DDR_DQ108	H27	RAM_DQ_R<108>		
RAM_DQ_R<45>	A25	DDR_DQ45	DDR_DQ109	H28	RAM_DQ_R<109>		
RAM_DQ_R<46>	C24	DDR_DQ46	DDR_DQ110	J27	RAM_DQ_R<110>		
RAM_DQ_R<47>	C23	DDR_DQ47	DDR_DQ111	L24	RAM_DQ_R<111>		
RAM_DQ_R<48>	B24	DDR_DQ48	DDR_DQ112	J25	RAM_DQ_R<112>		
RAM_DQ_R<49>	B23	DDR_DQ49	DDR_DQ113	J24	RAM_DQ_R<113>		
RAM_DQ_R<50>	A23	DDR_DQ50	DDR_DQ114	J26	RAM_DQ_R<114>		
RAM_DQ_R<51>	A24	DDR_DQ51	DDR_DQ115	G28	RAM_DQ_R<115>		
RAM_DQ_R<52>	A27	DDR_DQ52	DDR_DQ116	H25	RAM_DQ_R<116>		
RAM_DQ_R<53>	A28	DDR_DQ53	DDR_DQ117	H24	RAM_DQ_R<117>		
RAM_DQ_R<54>	B28	DDR_DQ54	DDR_DQ118	F27	RAM_DQ_R<118>		
RAM_DQ_R<55>	A26	DDR_DQ55	DDR_DQ119	H26	RAM_DQ_R<119>		
RAM_DQ_R<56>	F24	DDR_DQ56	DDR_DQ120	E28	RAM_DQ_R<120>		
RAM_DQ_R<57>	J22	DDR_DQ57	DDR_DQ121	E27	RAM_DQ_R<121>		
RAM_DQ_R<58>	E23	DDR_DQ58	DDR_DQ122	F26	RAM_DQ_R<122>		
RAM_DQ_R<59>	H23	DDR_DQ59	DDR_DQ123	E26	RAM_DQ_R<123>		
RAM_DQ_R<60>	J21	DDR_DQ60	DDR_DQ124	D28	RAM_DQ_R<124>		
RAM_DQ_R<61>	H21	DDR_DQ61	DDR_DQ125	C28	RAM_DQ_R<125>		
RAM_DQ_R<62>	G21	DDR_DQ62	DDR_DQ126	E25	RAM_DQ_R<126>		
RAM_DQ_R<63>	H22	DDR_DQ63	DDR_DQ127	E24	RAM_DQ_R<127>		

60 48 28 7 PP1V5_PWRON_NB_AVDD

R3702 2.2 5% 1/16W MF 603

PP1V5_PWRON_RAM_NB_AVDD VOLTAGE=1.5V

C3745 1UF 10% 6.3V CERM 402

C3744 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

PP2V5_RAM 7 26 37

U3 U3LITE V1.0-300MM PBGA (SYM 3 OF 7) OMIT

MEMORY CONTROL INTERFACE

27 RAM_CLK66M_NB	AC20	DDR_CLKP		
RAM_CLK_A_P_R	AA12	DDR_CK_A		
RAM_CLK_A_N_R	AB12	DDR_CK_AN		
RAM_CLK_B_P_R	AB14	DDR_CK_B		
RAM_CLK_B_N_R	AA14	DDR_CK_BN		
RAM_CLK_C_P_R	AE15	DDR_CK_C		
RAM_CLK_C_N_R	AE14	DDR_CK_CN		
RAM_CLK_D_P_R	AC14	DDR_CK_D		
RAM_CLK_D_N_R	AD14	DDR_CK_DN		
RAM_CLK_E_P_R	AD15	DDR_CK_E		
RAM_CLK_E_N_R	AC15	DDR_CK_EN		
RAM_CLK_F_P_R	AA15	DDR_CK_F		
RAM_CLK_F_N_R	AB15	DDR_CK_FN		
RAM_CKE_R<0>	AC17	DDR_CKE0		
RAM_CKE_R<1>	AD17	DDR_CKE1		
TP_RAM_CKE_R<2>	AE17	DDR_CKE2		
TP_RAM_CKE_R<3>	AF17	DDR_CKE3		
RAM_CKE_R<4>	AB17	DDR_CKE4		
RAM_CKE_R<5>	AA17	DDR_CKE5		
TP_RAM_CKE_R<6>	AB18	DDR_CKE6		
TP_RAM_CKE_R<7>	AA18	DDR_CKE7		
	Y21	DDR_VREF0		
	U21	DDR_VREF1		
	L21	DDR_VREF2		
	H20	DDR_VREF3		
	AA21	DDR_VREF4		
	M21	DDR_VREF5		
	V21	DDR_VREF6		
	J20	DDR_VREF7		
	AE21	DDR_RAS	RAM_RAS_L_R	
	AD20	DDR_CAS	RAM_CAS_L_R	
	AC23	DDR_WE	RAM_WE_L_R	
	AF21	DDR_BA0	RAM_BA_R<0>	
	AE20	DDR_BA1	RAM_BA_R<1>	
	AH16	DDR_MUXEN0	TP_RAM_MUXEN0	6
	AH18	DDR_MUXEN4	TP_RAM_MUXEN4	6
	AG12	DDR_MAD0	RAM_A_R<0>	
	AH13	DDR_MAD1	RAM_A_R<1>	
	AH14	DDR_MAD2	RAM_A_R<2>	
	AH15	DDR_MAD3	RAM_A_R<3>	
	AF12	DDR_MAD4	RAM_A_R<4>	
	AE12	DDR_MAD5	RAM_A_R<5>	
	AD12	DDR_MAD6	RAM_A_R<6>	
	AC12	DDR_MAD7	RAM_A_R<7>	
	AG15	DDR_MAD8	RAM_A_R<8>	
	AF15	DDR_MAD9	RAM_A_R<9>	
	AF14	DDR_MAD10	RAM_A_R<10>	
	AG14	DDR_MAD11	RAM_A_R<11>	
	AH17	DDR_MAD12	RAM_A_R<12>	
	AG17	DDR_MAD13	RAM_A_R<13>	
	AF18	DDR_CS0	RAM_CS_L_R<0>	
	AE18	DDR_CS1	RAM_CS_L_R<1>	
	AG20	DDR_CS2	TP_RAM_CS_L_R<2>	6
	AH20	DDR_CS3	TP_RAM_CS_L_R<3>	6
	AC18	DDR_CS8	RAM_CS_L_R<8>	
	AD18	DDR_CS9	RAM_CS_L_R<9>	
	AG18	DDR_CS10	TP_RAM_CS_L_R<10>	6
	AH19	DDR_CS11	TP_RAM_CS_L_R<11>	6
	AC24	DDR_DQSP0	RAM_DQS_R<0>	
	AG23	DDR_DQSP1	RAM_DQS_R<1>	
	Y23	DDR_DQSP2	RAM_DQS_R<2>	
	R23	DDR_DQSP3	RAM_DQS_R<3>	
	M22	DDR_DQSP4	RAM_DQS_R<4>	
	B26	DDR_DQSP5	RAM_DQS_R<5>	
	B27	DDR_DQSP6	RAM_DQS_R<6>	
	F23	DDR_DQSP7	RAM_DQS_R<7>	
	AE23	DDR_DQSP8	RAM_DQS_R<8>	
	AD28	DDR_DQSP9	RAM_DQS_R<9>	
	Y27	DDR_DQSP10	RAM_DQS_R<10>	
	U28	DDR_DQSP11	RAM_DQS_R<11>	
	M27	DDR_DQSP12	RAM_DQS_R<12>	
	J28	DDR_DQSP13	RAM_DQS_R<13>	
	F28	DDR_DQSP14	RAM_DQS_R<14>	
	F25	DDR_DQSP15	RAM_DQS_R<15>	

DDR_CLK_AVSS

AA20

CLK<A..C> GO TO J4000

CLK<D..F> GO TO J4001

CKE<1..0> GO TO J4000

CKE<5..4> GO TO J4001

RAS / CAS / WE / BA<1..0> GO TO BOTH DIMMS

ADDRESS LINES GO TO BOTH DIMMS

CS<1..0> GO TO J4000

CS<9..8> GO TO J4001

DQS<7..0> GO TO J4000

DQS<15..8> GO TO J4001

PP2V5_RAM 7 26 37

R3700 1K 1% 1/16W MF 402

R3701 1K 1% 1/16W MF 402

PP1V25_RAM_VREF_NB VOLTAGE=1.25V

C3730 0.1UF 20% 10V CERM 402

C3746 0.1UF 20% 10V CERM 402

C3747 0.1UF 20% 10V CERM 402

C3748 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

PP2V5_RAM 7 26 37

C3700 C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 C3709 C3710 C3711 C3712 C3713 C3714 C3731 C3732 C3733 C3734 C3735 C3736 C3737 0.1UF 20% 10V CERM 402

PP2V5_RAM 7 26 37

C3715 C3716 C3717 C3718 C3719 C3720 C3721 C3722 C3724 C3725 C3726 C3727 C3728 C3729 C3743 C3742 C3740 C3739 C3738 0.1UF 20% 10V CERM 402

MASTER: NEOBORG U3LITE

U3LITE MEMORY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 37 OF 99	

ALL R PACKS ARE 15 OHM 1/16W 5%

38 37	RAM_DQ_R<7>	RP3836	4	5	15	RAM_DQ<7>	38 40 44
38 37	RAM_DQ_R<2>	RP3836	1	8	15	RAM_DQ<2>	38 40 44
38 37	RAM_DQ_R<0>	RP3836	3	6	15	RAM_DQ<0>	38 40 44
38 37	RAM_DQ_R<3>	RP3836	2	7	15	RAM_DQ<3>	38 40 44
38 37	RAM_DQ_R<1>	RP3816	1	8	15	RAM_DQ<1>	38 40 44
38 37	RAM_DQ_R<4>	RP3816	2	7	15	RAM_DQ<4>	38 40 44
38 37	RAM_DQ_R<6>	RP3816	4	5	15	RAM_DQ<6>	38 40 44
38 37	RAM_DQ_R<5>	RP3816	3	6	15	RAM_DQ<5>	38 40 44
38 37	RAM_DQ_R<9>	RP3835	4	5	15	RAM_DQ<9>	38 40 44
38 37	RAM_DQ_R<10>	RP3801	1	8	15	RAM_DQ<10>	38 40 44
38 37	RAM_DQ_R<11>	RP3801	3	6	15	RAM_DQ<11>	38 40 44
38 37	RAM_DQ_R<14>	RP3801	4	5	15	RAM_DQ<14>	38 40 44
38 37	RAM_DQ_R<12>	RP3835	2	7	15	RAM_DQ<12>	38 40 44
38 37	RAM_DQ_R<13>	RP3801	2	7	15	RAM_DQ<13>	38 40 44
38 37	RAM_DQ_R<15>	RP3835	1	8	15	RAM_DQ<15>	38 40 44
38 37	RAM_DQ_R<8>	RP3835	3	6	15	RAM_DQ<8>	38 40 44
38 37	RAM_DQ_R<17>	RP3822	1	8	15	RAM_DQ<17>	38 40 44
38 37	RAM_DQ_R<22>	RP3822	4	5	15	RAM_DQ<22>	38 40 44
38 37	RAM_DQ_R<19>	RP3822	2	7	15	RAM_DQ<19>	38 40 44
38 37	RAM_DQ_R<18>	RP3822	3	6	15	RAM_DQ<18>	38 40 44
38 37	RAM_DQ_R<20>	RP3823	3	6	15	RAM_DQ<20>	38 40 44
38 37	RAM_DQ_R<16>	RP3823	4	5	15	RAM_DQ<16>	38 40 44
38 37	RAM_DQ_R<21>	RP3823	2	7	15	RAM_DQ<21>	38 40 44
38 37	RAM_DQ_R<23>	RP3823	1	8	15	RAM_DQ<23>	38 40 44
38 37	RAM_DQ_R<30>	RP3808	3	6	15	RAM_DQ<30>	38 40 44
38 37	RAM_DQ_R<26>	RP3824	2	7	15	RAM_DQ<26>	38 40 44
38 37	RAM_DQ_R<24>	RP3808	1	8	15	RAM_DQ<24>	38 40 44
38 37	RAM_DQ_R<27>	RP3824	1	8	15	RAM_DQ<27>	38 40 44
38 37	RAM_DQ_R<28>	RP3808	4	5	15	RAM_DQ<28>	38 40 44
38 37	RAM_DQ_R<31>	RP3808	2	7	15	RAM_DQ<31>	38 40 44
38 37	RAM_DQ_R<29>	RP3824	4	5	15	RAM_DQ<29>	38 40 44
38 37	RAM_DQ_R<25>	RP3824	3	6	15	RAM_DQ<25>	38 40 44
38 37	RAM_DQ_R<32>	RP3826	4	5	15	RAM_DQ<32>	38 40 44
38 37	RAM_DQ_R<35>	RP3807	2	7	15	RAM_DQ<35>	38 40 44
38 37	RAM_DQ_R<38>	RP3826	2	7	15	RAM_DQ<38>	38 40 44
38 37	RAM_DQ_R<37>	RP3807	4	5	15	RAM_DQ<37>	38 40 44
38 37	RAM_DQ_R<39>	RP3826	3	6	15	RAM_DQ<39>	38 40 44
38 37	RAM_DQ_R<33>	RP3807	3	6	15	RAM_DQ<33>	38 40 44
38 37	RAM_DQ_R<34>	RP3807	1	8	15	RAM_DQ<34>	38 40 44
38 37	RAM_DQ_R<36>	RP3826	1	8	15	RAM_DQ<36>	38 40 44
38 37	RAM_DQ_R<47>	RP3811	2	7	15	RAM_DQ<47>	38 40 44
38 37	RAM_DQ_R<46>	RP3811	1	8	15	RAM_DQ<46>	38 40 44
38 37	RAM_DQ_R<43>	RP3814	2	7	15	RAM_DQ<43>	38 40 44
38 37	RAM_DQ_R<41>	RP3814	1	8	15	RAM_DQ<41>	38 40 44
38 37	RAM_DQ_R<45>	RP3811	4	5	15	RAM_DQ<45>	38 40 44
38 37	RAM_DQ_R<42>	RP3814	3	6	15	RAM_DQ<42>	38 40 44
38 37	RAM_DQ_R<40>	RP3814	4	5	15	RAM_DQ<40>	38 40 44
38 37	RAM_DQ_R<44>	RP3811	3	6	15	RAM_DQ<44>	38 40 44
38 37	RAM_DQ_R<51>	RP3830	4	5	15	RAM_DQ<51>	38 40 44
38 37	RAM_DQ_R<50>	RP3830	2	7	15	RAM_DQ<50>	38 40 44
38 37	RAM_DQ_R<49>	RP3830	1	8	15	RAM_DQ<49>	38 40 44
38 37	RAM_DQ_R<48>	RP3830	3	6	15	RAM_DQ<48>	38 40 44
38 37	RAM_DQ_R<52>	RP3812	2	7	15	RAM_DQ<52>	38 40 44
38 37	RAM_DQ_R<53>	RP3812	3	6	15	RAM_DQ<53>	38 40 44
38 37	RAM_DQ_R<54>	RP3812	4	5	15	RAM_DQ<54>	38 40 44
38 37	RAM_DQ_R<55>	RP3812	1	8	15	RAM_DQ<55>	38 40 44
38 37	RAM_DQ_R<56>	RP3813	1	8	15	RAM_DQ<56>	38 40 44
38 37	RAM_DQ_R<63>	RP3831	4	5	15	RAM_DQ<63>	38 40 44
38 37	RAM_DQ_R<59>	RP3813	2	7	15	RAM_DQ<59>	38 40 44
38 37	RAM_DQ_R<61>	RP3831	2	7	15	RAM_DQ<61>	38 40 44
38 37	RAM_DQ_R<57>	RP3831	3	6	15	RAM_DQ<57>	38 40 44
38 37	RAM_DQ_R<60>	RP3831	1	8	15	RAM_DQ<60>	38 40 44
38 37	RAM_DQ_R<58>	RP3813	3	6	15	RAM_DQ<58>	38 40 44
38 37	RAM_DQ_R<62>	RP3813	4	5	15	RAM_DQ<62>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

38 37	RAM_CKE_R<4>	RP3841	3	6	15	RAM_CKE<4>	38 40 45
38 37	RAM_CKE_R<5>	RP3841	4	5	15	RAM_CKE<5>	38 40 45
38 37	RAM_CKE_R<0>	RP3841	2	7	15	RAM_CKE<0>	38 40 44
38 37	RAM_CKE_R<1>	RP3841	1	8	15	RAM_CKE<1>	38 40 44
38 37	RAM_CS_L_R<8>	RP3842	1	8	15	RAM_CS_L<8>	38 40 45
38 37	RAM_CS_L_R<9>	RP3842	2	7	15	RAM_CS_L<9>	38 40 45
38 37	RAM_CS_L_R<1>	RP3842	3	6	15	RAM_CS_L<1>	38 40 44
38 37	RAM_CS_L_R<0>	RP3842	4	5	15	RAM_CS_L<0>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

38 37	RAM_A_R<11>	RP3832	3	6	15	RAM_A<11>	38 40 44
38 37	RAM_A_R<1>	RP3832	4	5	15	RAM_A<1>	38 40 44
38 37	RAM_A_R<10>	RP3832	2	7	15	RAM_A<10>	38 40 45
38 37	RAM_WE_L_R	RP3800	4	5	15	RAM_WE_L	38 40 45
38 37	RAM_A_R<4>	RP3833	3	6	15	RAM_A<4>	38 40 44
38 37	RAM_A_R<6>	RP3833	2	7	15	RAM_A<6>	38 40 44
38 37	RAM_A_R<7>	RP3833	1	8	15	RAM_A<7>	38 40 44
		RP3834	1	8	15		
38 37	RAM_A_R<12>	RP3800	3	6	15	RAM_A<12>	38 40 44
38 37	RAM_A_R<2>	RP3834	2	7	15	RAM_A<2>	38 40 44
38 37	RAM_A_R<0>	RP3833	4	5	15	RAM_A<0>	38 40 44
38 37	RAM_A_R<5>	RP3832	1	8	15	RAM_A<5>	38 40 44
38 37	RAM_A_R<13>	RP3800	2	7	15	RAM_A<13>	38 40 44
38 37	RAM_A_R<3>	RP3800	1	8	15	RAM_A<3>	38 40 44
38 37	RAM_CAS_L_R	RP3804	1	8	15	RAM_CAS_L	38 40 45
38 37	RAM_BA_R<0>	RP3804	4	5	15	RAM_BA<0>	38 40 45
38 37	RAM_BA_R<1>	RP3804	2	7	15	RAM_BA<1>	38 40 45
38 37	RAM_RAS_L_R	RP3804	3	6	15	RAM_RAS_L	38 40 45
38 37	RAM_A_R<9>	RP3834	3	6	15	RAM_A<9>	38 40 44
38 37	RAM_A_R<8>	RP3834	4	5	15	RAM_A<8>	38 40 44

38 37	RAM_DQ_R<68>	RP3818	2	7	15	RAM_DQ<68>	38 40 45
38 37	RAM_DQ_R<65>	RP3805	2	7	15	RAM_DQ<65>	38 40 45
38 37	RAM_DQ_R<70>	RP3818	4	5	15	RAM_DQ<70>	38 40 45
38 37	RAM_DQ_R<66>	RP3805	1	8	15	RAM_DQ<66>	38 40 45
38 37	RAM_DQ_R<71>	RP3818	3	6	15	RAM_DQ<71>	38 40 45
38 37	RAM_DQ_R<64>	RP3805	4	5	15	RAM_DQ<64>	38 40 45
38 37	RAM_DQ_R<67>	RP3805	3	6	15	RAM_DQ<67>	38 40 45
38 37	RAM_DQ_R<69>	RP3818	1	8	15	RAM_DQ<69>	38 40 45
38 37	RAM_DQ_R<74>	RP3817	3	6	15	RAM_DQ<74>	38 40 45
38 37	RAM_DQ_R<73>	RP3802	4	5	15	RAM_DQ<73>	38 40 45
38 37	RAM_DQ_R<72>	RP3817	2	7	15	RAM_DQ<72>	38 40 45
38 37	RAM_DQ_R<75>	RP3817	4	5	15	RAM_DQ<75>	38 40 45
38 37	RAM_DQ_R<78>	RP3802	2	7	15	RAM_DQ<78>	38 40 45
38 37	RAM_DQ_R<79>	RP3817	1	8	15	RAM_DQ<79>	38 40 45
38 37	RAM_DQ_R<77>	RP3802	1	8	15	RAM_DQ<77>	38 40 45
38 37	RAM_DQ_R<76>	RP3802	3	6	15	RAM_DQ<76>	38 40 45
38 37	RAM_DQ_R<87>	RP3806	2	7	15	RAM_DQ<87>	38 40 45
38 37	RAM_DQ_R<86>	RP3821	1	8	15	RAM_DQ<86>	38 40 45
38 37	RAM_DQ_R<81>	RP3821	4	5	15	RAM_DQ<81>	38 40 45
38 37	RAM_DQ_R<80>	RP3821	2	7	15	RAM_DQ<80>	38 40 45
38 37	RAM_DQ_R<84>	RP3806	1	8	15	RAM_DQ<84>	38 40 45
38 37	RAM_DQ_R<85>	RP3806	3	6	15	RAM_DQ<85>	38 40 45
38 37	RAM_DQ_R<83>	RP3821	3	6	15	RAM_DQ<83>	38 40 45
38 37	RAM_DQ_R<82>	RP3806	4	5	15	RAM_DQ<82>	38 40 45
38 37	RAM_DQ_R<91>	RP3819	3	6	15	RAM_DQ<91>	38 40 45
38 37	RAM_DQ_R<93>	RP3819	1	8	15	RAM_DQ<93>	38 40 45
38 37	RAM_DQ_R<94>	RP3803	2	7	15	RAM_DQ<94>	38 40 45
38 37	RAM_DQ_R<90>	RP3819	4	5	15	RAM_DQ<90>	38 40 45
38 37	RAM_DQ_R<88>	RP3803	4	5	15	RAM_DQ<88>	38 40 45
38 37	RAM_DQ_R<89>	RP3819	2	7	15	RAM_DQ<89>	38 40 45
38 37	RAM_DQ_R<92>	RP3803	3	6	15	RAM_DQ<92>	38 40 45
38 37	RAM_DQ_R<95>	RP3803	1	8	15	RAM_DQ<95>	38 40 45
38 37	RAM_DQ_R<98>	RP3820	4	5	15	RAM_DQ<98>	38 40 45
38 37	RAM_DQ_R<96>	RP3820	3	6	15	RAM_DQ<96>	38 40 45
38 37	RAM_DQ_R<103>	RP3820	2	7	15	RAM_DQ<103>	38 40 45
38 37	RAM_DQ_R<97>	RP3820	1	8	15	RAM_DQ<97>	38 40 45
38 37	RAM_DQ_R<100>	RP3825	2	7	15	RAM_DQ<100>	38 40 45
38 37	RAM_DQ_R<99>	RP3825	3	6	15	RAM_DQ<99>	38 40 45
38 37	RAM_DQ_R<102>	RP3825	1	8	15	RAM_DQ<102>	38 40 45
38 37	RAM_DQ_R<101>	RP3825	4	5	15	RAM_DQ<101>	38 40 45
38 37	RAM_DQ_R<111>	RP3809	1	8	15	RAM_DQ<111>	38 40 45
38 37	RAM_DQ_R<106>	RP3809	3	6	15	RAM_DQ<106>	38 40 45
38 37	RAM_DQ_R<105>	RP3809	2	7	15	RAM_DQ<105>	38 40 45
38 37	RAM_DQ_R<108>	RP3829	2	7	15	RAM_DQ<108>	38 40 45
38 37	RAM_DQ_R<107>	RP3829	4	5	15	RAM_DQ<107>	38 40 45
38 37	RAM_DQ_R<110>	RP3829	3	6	15	RAM_DQ<110>	38 40 45
38 37	RAM_DQ_R<104>	RP3809	4	5	15	RAM_DQ<104>	38 40 45
38 37	RAM_DQ_R<109>	RP3829	1	8	15	RAM_DQ<109>	38 40 45
38 37	RAM_DQ_R<119>	RP3828	4	5	15	RAM_DQ<119>	38 40 45
38 37	RAM_DQ_R<112>	RP3815	2	7	15	RAM_DQ<112>	38 40 45
38 37	RAM_DQ_R<117>	RP3815	1	8	15	RAM_DQ<117>	38 40 45
38 37	RAM_DQ_R<118>	RP3828	1	8	15	RAM_DQ<118>	38 40 45
38 37	RAM_DQ_R<113>	RP3815	3	6	15	RAM_DQ<113>	38 40 45
38 37	RAM_DQ_R<115>	RP3828	3	6	15	RAM_DQ<115>	38 40 45
38 37	RAM_DQ_R<116>	RP3828	2	7	15	RAM_DQ<116>	38 40 45
38 37	RAM_DQ_R<114>	RP3815	4	5	15	RAM_DQ<114>	38 40 45
38 37	RAM_DQ_R<121>	RP3827	3	6	15	RAM_DQ<121>	38 40 45
38 37	RAM_DQ_R<124>	RP3827	2	7	15	RAM_DQ<124>	38 40 45
38 37	RAM_DQ_R<120>	RP3827	4	5	15	RAM_DQ<120>	38 40 45
38 37	RAM_DQ_R<123>	RP3810	2	7	15	RAM_DQ<123>	38 40 45
38 37	RAM_DQ_R<125>	RP3827	1	8	15	RAM_DQ<125>	38 40 45
38 37	RAM_DQ_R<122>	RP3810	4	5	15	RAM_DQ<122>	38 40 45
38 37	RAM_DQ_R<126>	RP3810	1	8	15	RAM_DQ<126>	38 40 45
38 37	RAM_DQ_R<115>	RP3828	3	6	15	RAM_DQ<115>	38 40 45
38 37	RAM_DQ_R<116>	RP3828	2	7	15	RAM_DQ<116>	38 40 45
38 37	RAM_DQ_R<127>	RP3810	3	6	15	RAM_DQ<127>	38 40 45

THE FOLLOWING ARE 0402 5% RESISTORS

38 37	RAM_CLK_A_P_R	R3816	1	2	15	RAM_CLK_A_P	38 40
38 37	RAM_CLK_A_N_R	R3817	1	2	15	RAM_CLK_A_N	38 40
38 37	RAM_CLK_B_P_R	R3818	1	2	15	RAM_CLK_B_P	38 40
38 37	RAM_CLK_B_N_R	R3819	1	2	15	RAM_CLK_B_N	38 40
38 37	RAM_CLK_C_P_R	R3820	1	2	15	RAM_CLK_C_P	38 40
38 37	RAM_CLK_C_N_R	R3821	1	2	15	RAM_CLK_C_N	38 40
38 37	RAM_CLK_D_P_R	R3822	1	2	15	RAM_CLK_D_P	38 40
38 37	RAM_CLK_D_N_R	R3823	1	2	15	RAM_CLK_D_N	38 40
38 37	RAM_CLK_E_P_R	R3824	1	2	15	RAM_CLK_E_P	38 40
38 37	RAM_CLK_E_N_R	R3825	1	2	15	RAM_CLK_E_N	38 40
38 37	RAM_CLK_F_P_R	R3826	1	2	15	RAM_CLK_F_P	38 40
38 37	RAM_CLK_F_N_R	R3827	1	2	15	RAM_CLK_F_N	38 40

38 37	RAM_DQS_R<0>	R3800	1	2	15	RAM_DQS<0>	38 40 44
38 37	RAM_DQS_R<1>	R3801	1	2	15	RAM_DQS<1>	38 40 44
38 37	RAM_DQS_R<2>	R3802	1	2	15	RAM_DQS<2>	38 40 44
38 37	RAM_DQS_R<3>	R3803	1	2	15	RAM_DQS<3>	38 40 44
38 37	RAM_DQS_R<4>	R3804	1	2	15	RAM_DQS<4>	38 40 44
38 37	RAM_DQS_R<5>	R3805	1	2	15	RAM_DQS<5>	38 40 44
38 37	RAM_DQS_R<6>	R3806	1	2	15	RAM_DQS<6>	38 40 44
38 37	RAM_DQS_R<7>	R3807	1	2	15	RAM_DQS<7>	38 40 44
38 37	RAM_DQS_R<8>	R3808	1	2	15	RAM_DQS<8>	38 40 45
38 37	RAM_DQS_R<9>	R3809	1	2	15	RAM_DQS<9>	38 40 45
38 37	RAM_DQS_R<10>	R3810	1	2	15	RAM_DQS<10>	38 40 45
38 37	RAM_DQS_R<11>	R3811	1	2	15	RAM_DQS<11>	38 40 45
38 37	RAM_DQS_R<12>	R3812	1	2	15	RAM_DQS<12>	38 40 45
38 37	RAM_DQS_R<13>	R3813	1	2	15	RAM_DQS<13>	38 40 45
38 37	RAM_DQS_R<14>	R3814	1	2	15	RAM_DQS<14>	38 40 45
38 37	RAM_DQS_R<15>	R3815	1	2	15	RAM_DQS<15>	38 40 45

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
38 37 RAM_CLK_A_P_R			RAM_CLK	RAM_CLK_A_R	2006
38 37 RAM_CLK_A_N_R			RAM_CLK	RAM_CLK_A_R	2007
38 37 RAM_CLK_B_P_R			RAM_CLK	RAM_CLK_B_R	2008
38 37 RAM_CLK_B_N_R			RAM_CLK	RAM_CLK_B_R	2009
38 37 RAM_CLK_C_P_R			RAM_CLK	RAM_CLK_C_R	2010
38 37 RAM_CLK_C_N_R			RAM_CLK	RAM_CLK_C_R	2011
38 37 RAM_CLK_D_P_R			RAM_CLK	RAM_CLK_D_R	2012
38 37 RAM_CLK_D_N_R			RAM_CLK	RAM_CLK_D_R	2013
38 37 RAM_CLK_E_P_R			RAM_CLK	RAM_CLK_E_R	2014
38 37 RAM_CLK_E_N_R			RAM_CLK	RAM_CLK_E_R	2015
38 37 RAM_CLK_F_P_R			RAM_CLK	RAM_CLK_F_R	2016
38 37 RAM_CLK_F_N_R			RAM_CLK	RAM_CLK_F_R	2017
40 38 RAM_CLK_A_P	RAM_CLK0		RAM_CLK	RAM_CLK_A	2018
40 38 RAM_CLK_A_N	RAM_CLK0		RAM_CLK	RAM_CLK_A	2019
40 38 RAM_CLK_B_P	RAM_CLK0		RAM_CLK	RAM_CLK_B	2020
40 38 RAM_CLK_B_N	RAM_CLK0		RAM_CLK	RAM_CLK_B	2021
40 38 RAM_CLK_C_P	RAM_CLK0		RAM_CLK	RAM_CLK_C	2022
40 38 RAM_CLK_C_N	RAM_CLK0		RAM_CLK	RAM_CLK_C	2023
40 38 RAM_CLK_D_P	RAM_CLK1		RAM_CLK	RAM_CLK_D	2024
40 38 RAM_CLK_D_N	RAM_CLK1		RAM_CLK	RAM_CLK_D	2025
40 38 RAM_CLK_E_P	RAM_CLK1		RAM_CLK	RAM_CLK_E	2026
40 38 RAM_CLK_E_N	RAM_CLK1		RAM_CLK	RAM_CLK_E	2027
40 38 RAM_CLK_F_P	RAM_CLK1		RAM_CLK	RAM_CLK_F	2028
40 38 RAM_CLK_F_N	RAM_CLK1		RAM_CLK	RAM_CLK_F	2029
38 37 RAM_CKE_R<1..0>			RAM_CAD		2030
38 37 RAM_CKE_R<5..4>			RAM_CAD		2031
44 40 38 RAM_CKE<0>	RAM_CKECS0		RAM_CAD		2034
44 40 38 RAM_CKE<1>	RAM_CKECS0		RAM_CAD		2035
45 40 38 RAM_CKE<4>	RAM_CKECS1		RAM_CAD		2036
45 40 38 RAM_CKE<5>	RAM_CKECS1		RAM_CAD		2037
38 37 RAM_CS_L_R<1..0>			RAM_CAD		2038
38 37 RAM_CS_L_R<9..8>			RAM_CAD		2041
44 40 38 RAM_CS_L<0>	RAM_CKECS0		RAM_CAD		2043
44 40 38 RAM_CS_L<1>	RAM_CKECS0		RAM_CAD		2042
45 40 38 RAM_CS_L<8>	RAM_CKECS1		RAM_CAD		2040
45 40 38 RAM_CS_L<9>	RAM_CKECS1		RAM_CAD		2044
38 37 RAM_DQS_R<15..0>			RAM_CAD		2005
38 37 RAM_DQ_R<127..0>			RAM_CAD		2004
45 44 40 38 RAM_DQ<127..0>			RAM_CAD		2003
44 40 38 RAM_DQS<0>	RAM_DQS0		RAM_CAD		2046
44 40 38 RAM_DQ<7..0>	RAM_DQS0		RAM_CAD		2045
44 40 38 RAM_DQS<1>	RAM_DQS1		RAM_CAD		2051
44 40 38 RAM_DQ<15..8>	RAM_DQS1		RAM_CAD		2052
44 40 38 RAM_DQS<2>	RAM_DQS2		RAM_CAD		2053
44 40 38 RAM_DQ<23..16>	RAM_DQS2		RAM_CAD		2054
44 40 38 RAM_DQS<3>	RAM_DQS3		RAM_CAD		2055
44 40 38 RAM_DQ<31..24>	RAM_DQS3		RAM_CAD		2056
44 40 38 RAM_DQS<4>	RAM_DQS4		RAM_CAD		2057
44 40 38 RAM_DQ<39..32>	RAM_DQS4		RAM_CAD		2058
44 40 38 RAM_DQS<5>	RAM_DQS5		RAM_CAD		2059
44 40 38 RAM_DQ<47..40>	RAM_DQS5		RAM_CAD		2060
44 40 38 RAM_DQS<6>	RAM_DQS6		RAM_CAD		2061
44 40 38 RAM_DQ<55..48>	RAM_DQS6		RAM_CAD		2062
44 40 38 RAM_DQS<7>	RAM_DQS7		RAM_CAD		2063
44 40 38 RAM_DQ<63..56>	RAM_DQS7		RAM_CAD		2064
45 40 38 RAM_DQS<8>	RAM_DQS8		RAM_CAD		2065
45 40 38 RAM_DQ<71..64>	RAM_DQS8		RAM_CAD		2067
45 40 38 RAM_DQS<9>	RAM_DQS9		RAM_CAD		2066
45 40 38 RAM_DQ<79..72>	RAM_DQS9		RAM_CAD		2068
45 40 38 RAM_DQS<10>	RAM_DQS10		RAM_CAD		2070
45 40 38 RAM_DQ<87..80>	RAM_DQS10		RAM_CAD		2069
45 40 38 RAM_DQS<11>	RAM_DQS11		RAM_CAD		2072
45 40 38 RAM_DQ<95..88>	RAM_DQS11		RAM_CAD		2071
45 40 38 RAM_DQS<12>	RAM_DQS12		RAM_CAD		2073
45 40 38 RAM_DQ<103..96>	RAM_DQS12		RAM_CAD		2075
45 40 38 RAM_DQS<13>	RAM_DQS13		RAM_CAD		2074
45 40 38 RAM_DQ<111..104>	RAM_DQS13		RAM_CAD		2077
45 40 38 RAM_DQS<14>	RAM_DQS14		RAM_CAD		2076
45 40 38 RAM_DQ<119..112>	RAM_DQS14		RAM_CAD		2078
45 40 38 RAM_DQS<15>	RAM_DQS15		RAM_CAD		2080
45 40 38 RAM_DQ<127..120>	RAM_DQS15		RAM_CAD		2079
38 37 RAM_A_R<13..0>			RAM_CAD		2090
38 37 RAM_BA_R<1..0>			RAM_CAD		2091
38 37 RAM_RAS_L_R			RAM_CAD		2097
38 37 RAM_CAS_L_R			RAM_CAD		2098
38 37 RAM_WE_L_R			RAM_CAD		2099
45 44 40 38 RAM_A<13..0>	RAM_A_CTL		RAM_CAD		2000
45 40 38 RAM_BA<1..0>	RAM_A_CTL		RAM_CAD		2001
45 40 38 RAM_RAS_L	RAM_A_CTL		RAM_CAD		2093
45 40 38 RAM_CAS_L	RAM_A_CTL		RAM_CAD		2092
45 40 38 RAM_WE_L	RAM_A_CTL		RAM_CAD		2101

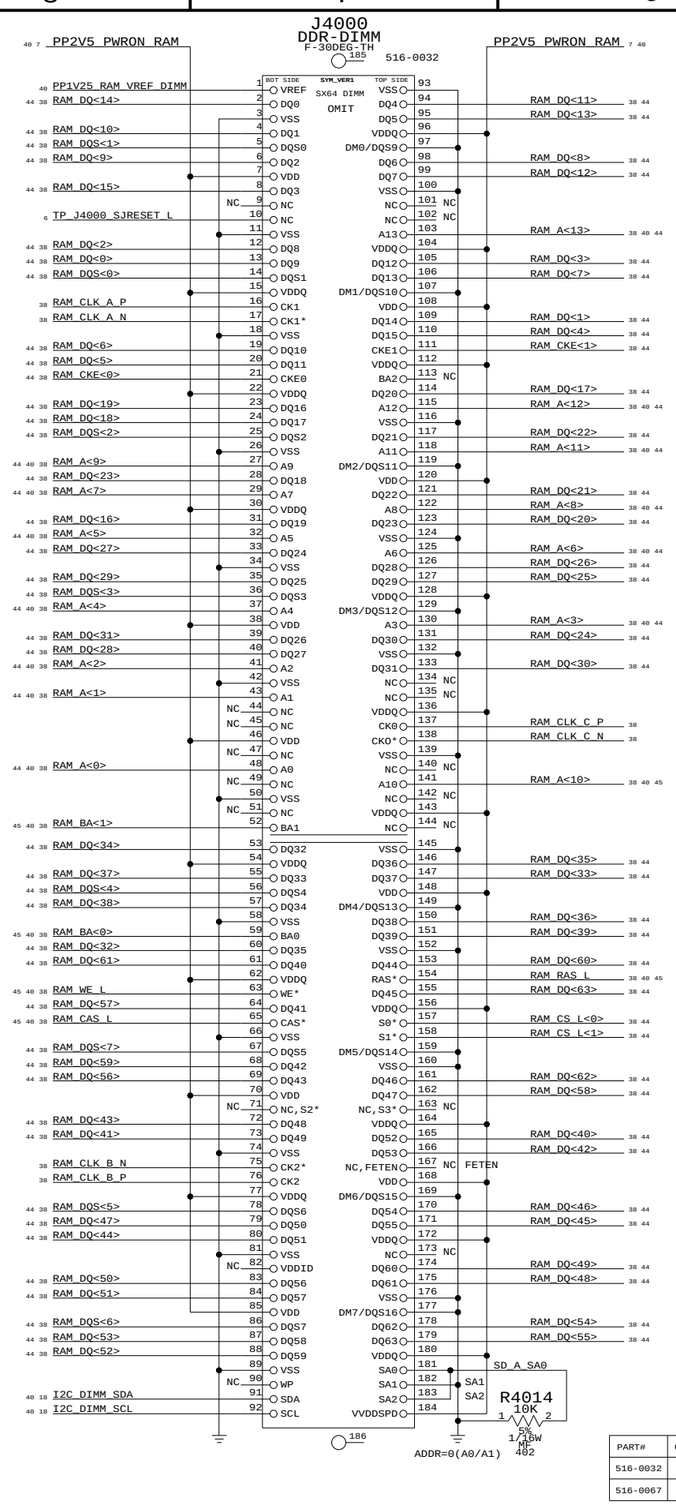
RAM_CLK PRIMARY SPACING SET TO 5MIL
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

RAM_CAD SPACING IS 10MIL

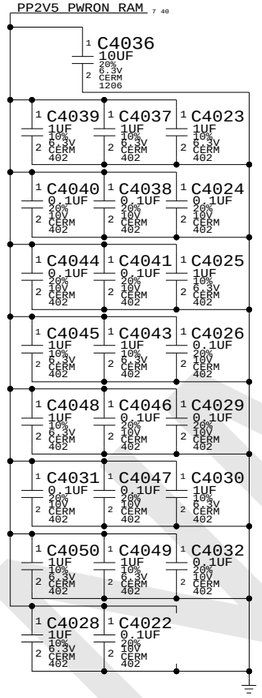
SERIES TERM

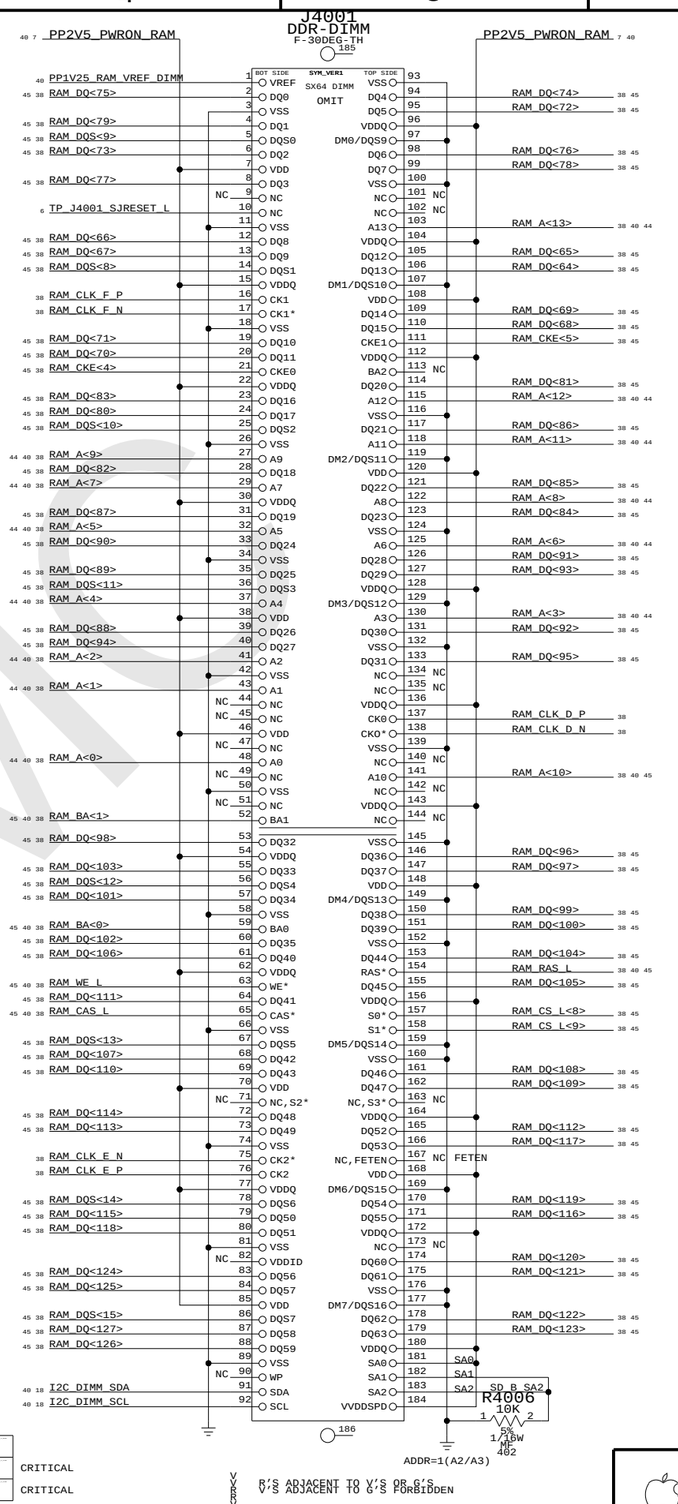
APPLE COMPUTER INC.

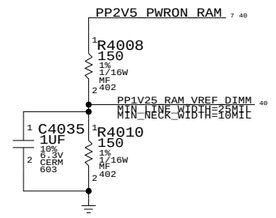
SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 38 OF 99	

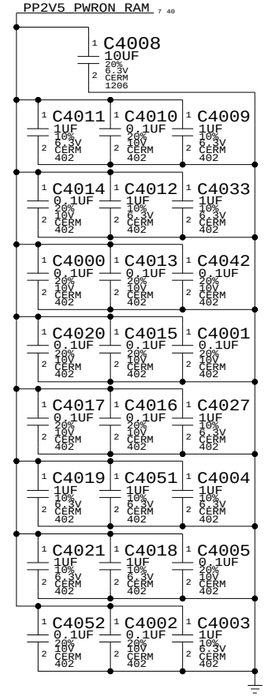


PIN 82:
NC: VDD & VDDQ ARE THE SAME
GND: VDD & VDDQ ARE DIFFERENT









PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
516-0032	2	CONN,DDR DIMM 30 DEG	J4000,J4001	17_INCH_LCD
516-0067	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD

CRITICAL
CRITICAL

D'S ADJACENT TO V'S OR G'S
V'S ADJACENT TO G'S FORBIDDEN

DIMMS

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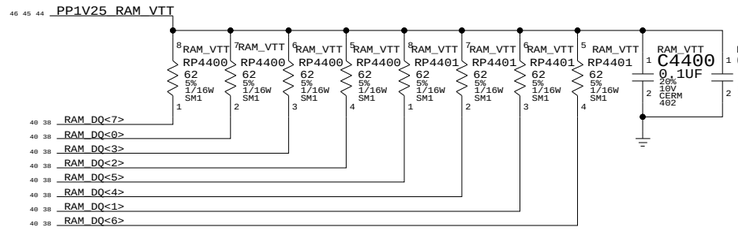
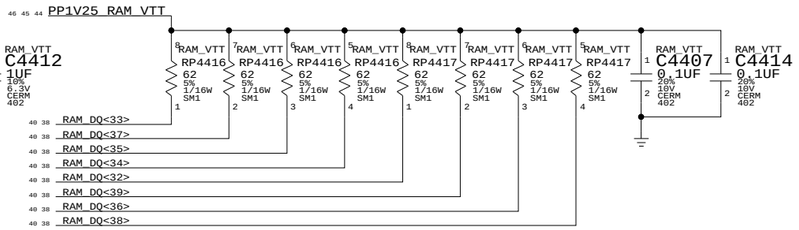
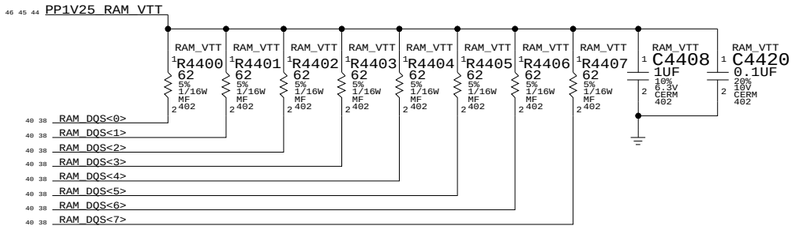
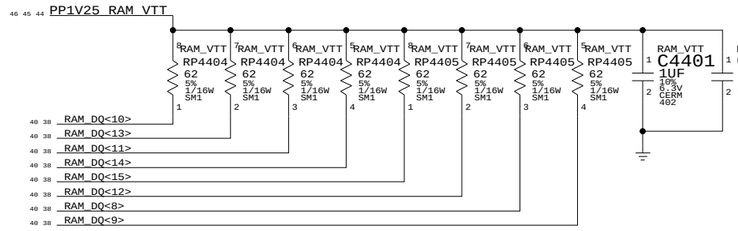
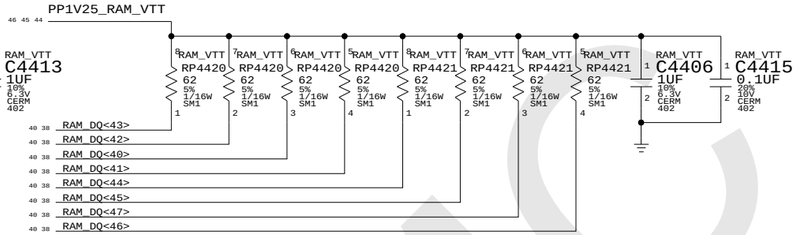
SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 40 OF 99	

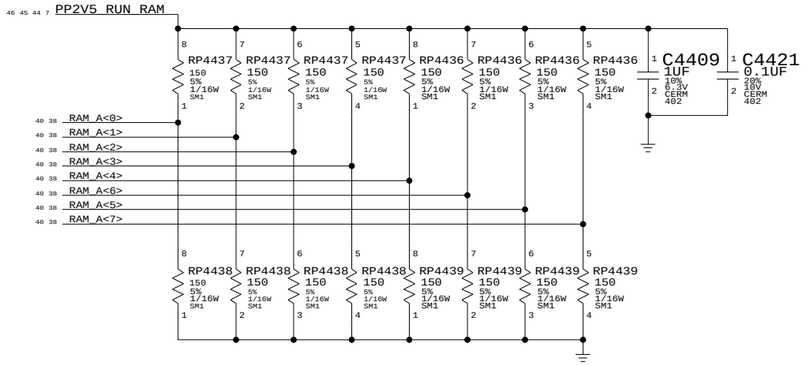


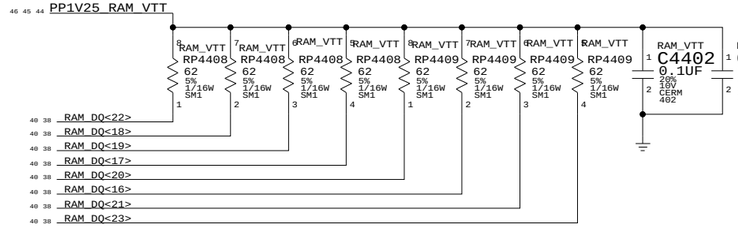


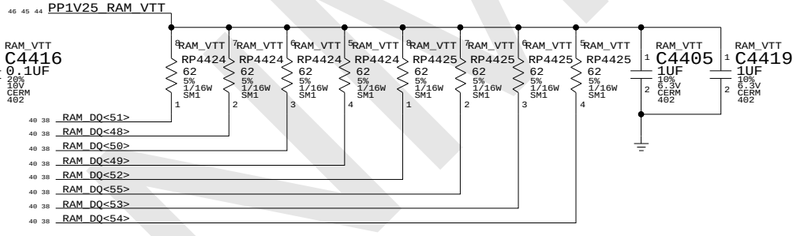


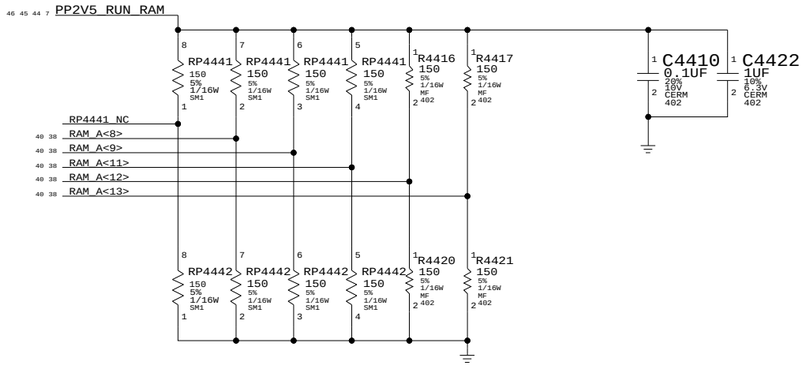


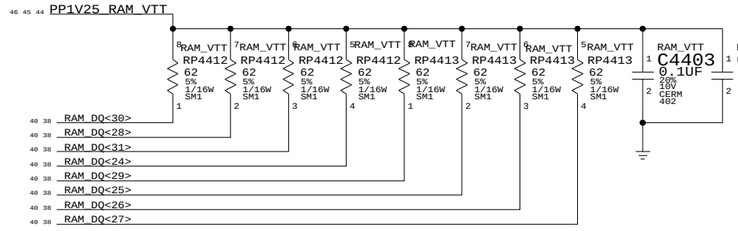


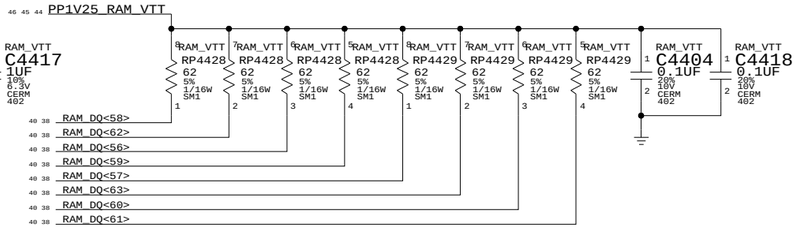


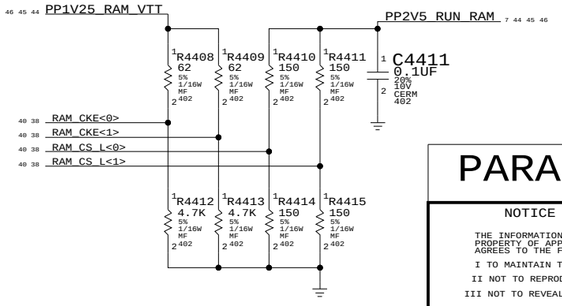












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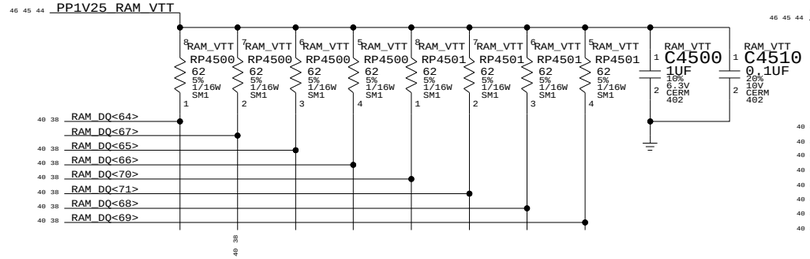
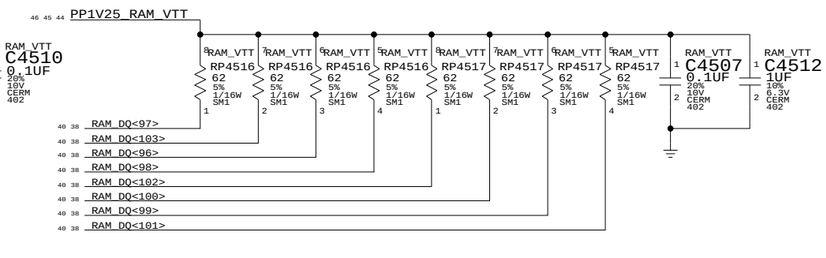
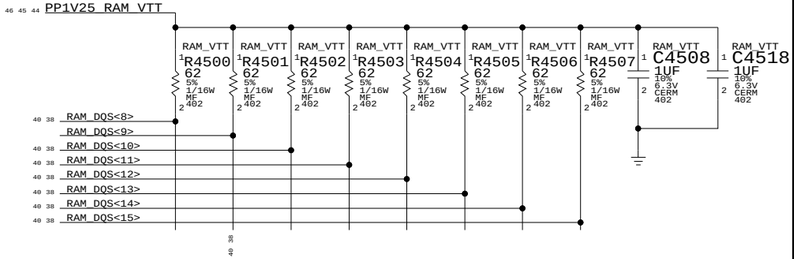
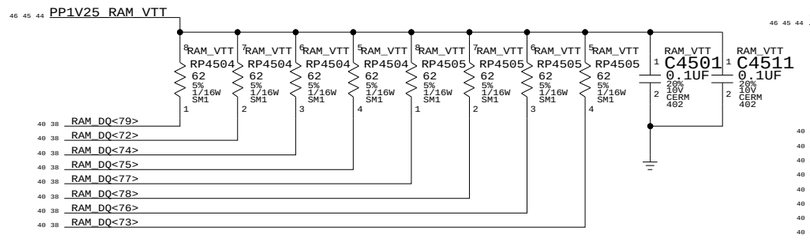
APPLE COMPUTER INC.

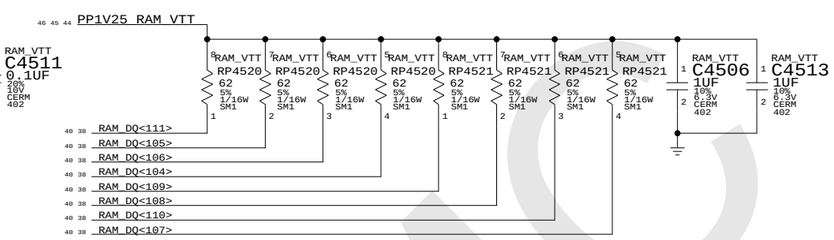
SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 44 OF 99	

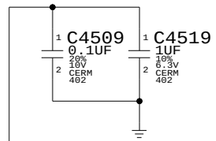


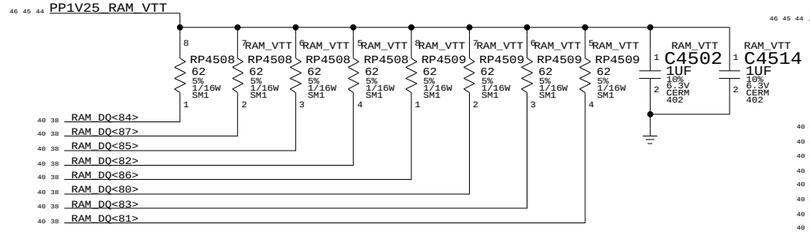


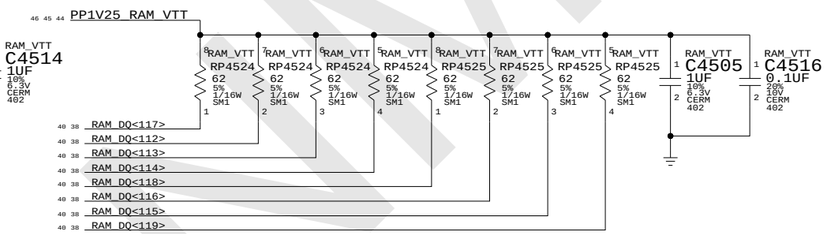


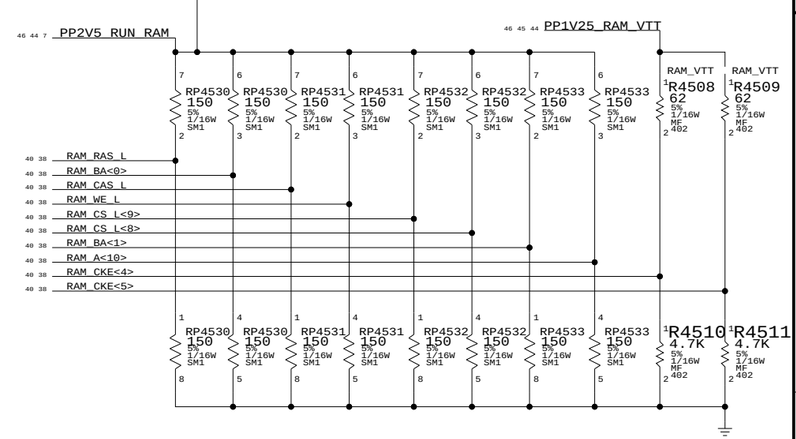


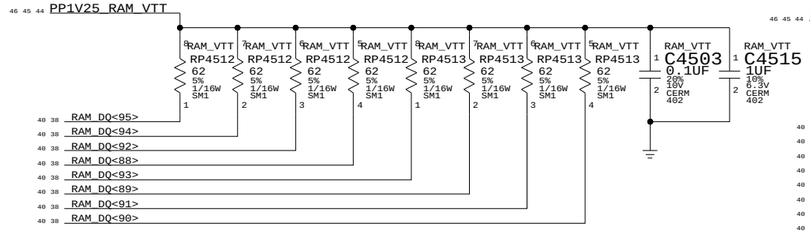


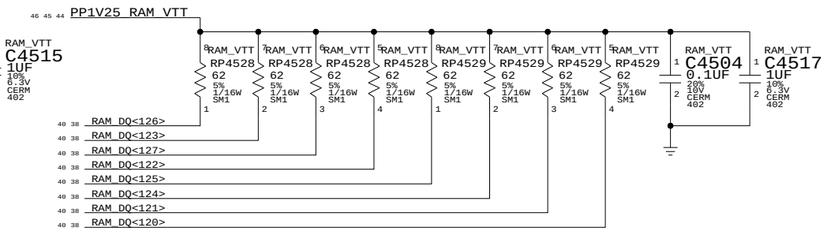








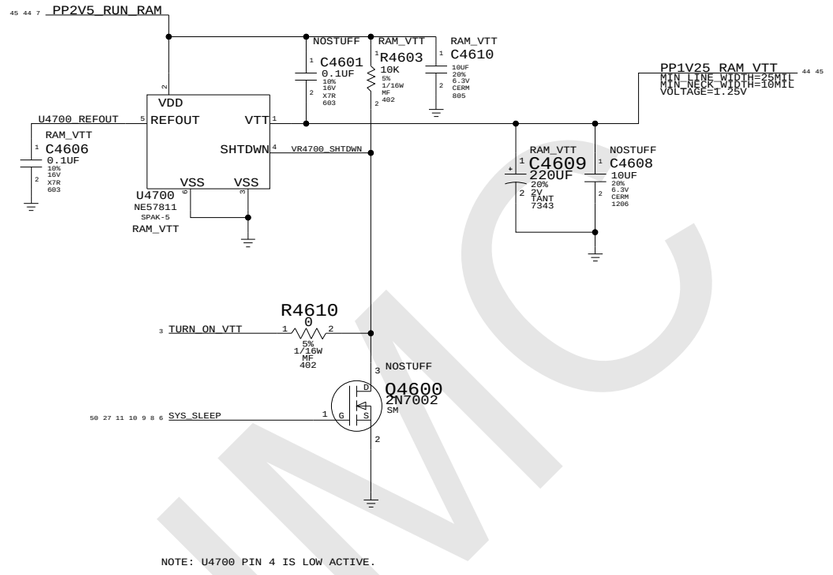




PARALLEL TERM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 45 OF 99	



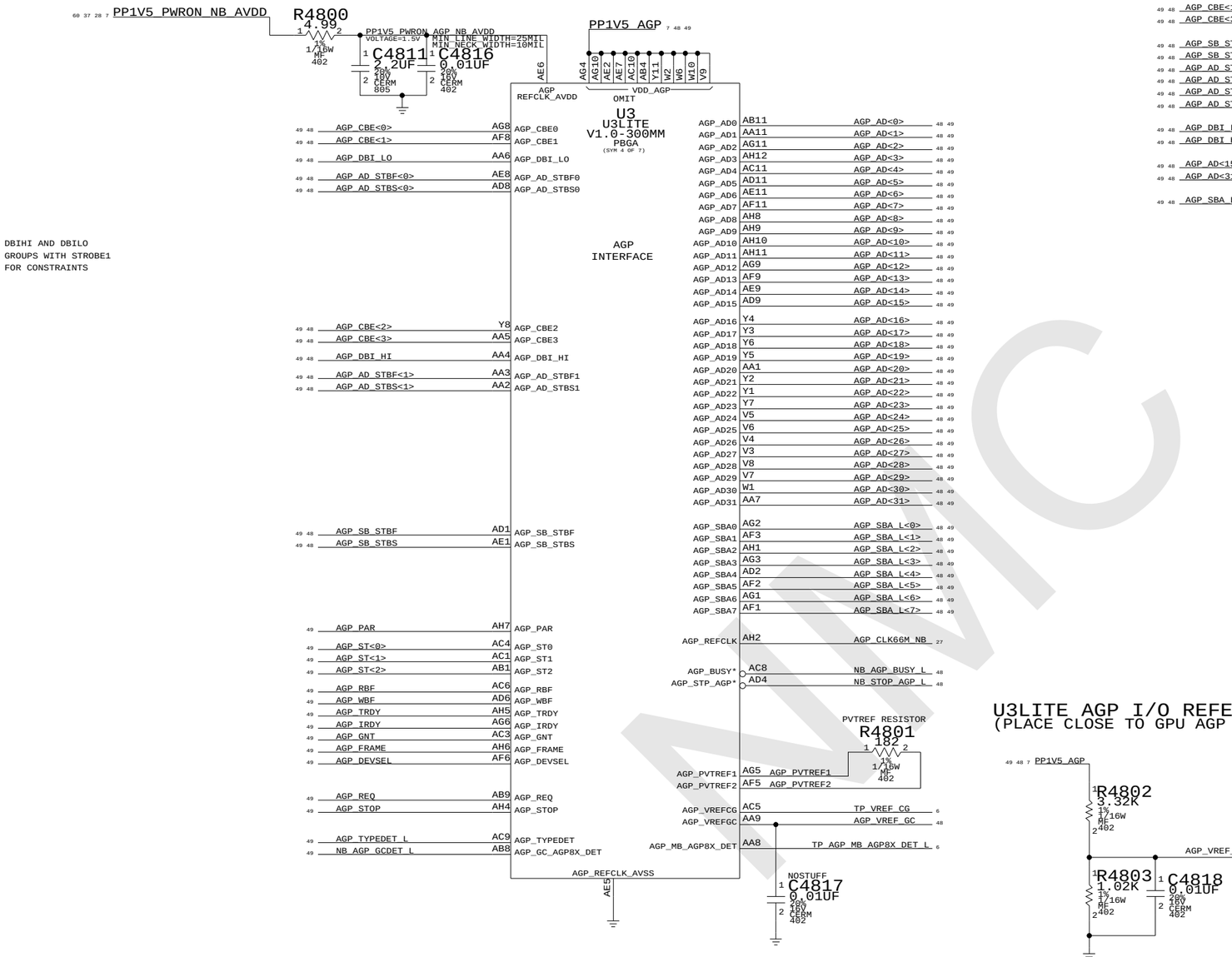
NOTE: U4700 PIN 4 IS LOW ACTIVE.

MEM TERM VREGS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT
NONE	46 OF 99

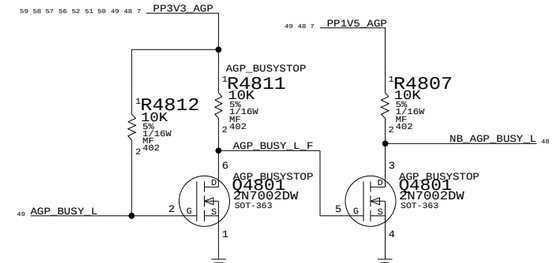


ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
AGP_CBE<1..0>	AGP_AD_0	AGP_DATA		146
AGP_CBE<3..2>	AGP_AD_1	AGP_DATA		148
AGP_SB_STBF	AGP_SB_STBS	AGP_STROBE	AGP_SB_STB	140
AGP_SB_STBS	AGP_SB_STBS	AGP_STROBE	AGP_SB_STB	160
AGP_AD_STBF<0>	AGP_AD_STB_0	AGP_STROBE	AGP_AD_STB0	153
AGP_AD_STBS<0>	AGP_AD_STB_0	AGP_STROBE	AGP_AD_STB0	152
AGP_AD_STBF<1>	AGP_AD_STB_1	AGP_STROBE	AGP_AD_STB1	155
AGP_AD_STBS<1>	AGP_AD_STB_1	AGP_STROBE	AGP_AD_STB1	154
AGP_DBI_LO	AGP_AD_0	AGP_DATA		165
AGP_DBI_HI	AGP_AD_STB_1	AGP_DATA		166
AGP_AD<15..0>	AGP_AD_0	AGP_DATA		167
AGP_AD<31..16>	AGP_AD_1	AGP_DATA		168
AGP_SBA_L<7..0>	AGP_SBA	AGP_DATA		159

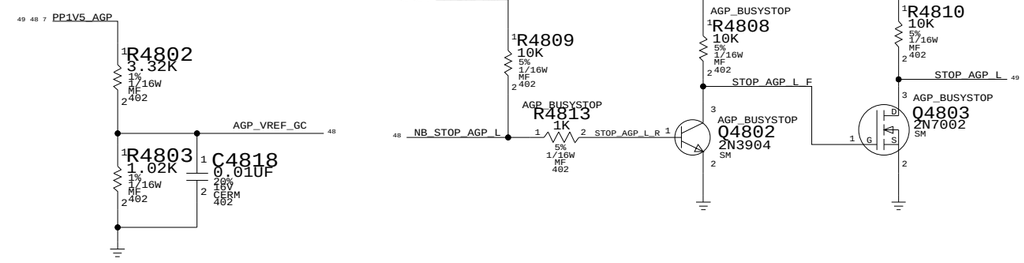
DBI_HI IS NOT A STROBE BUT SHARES THE SAME TOPOLOGY AS A STROBE

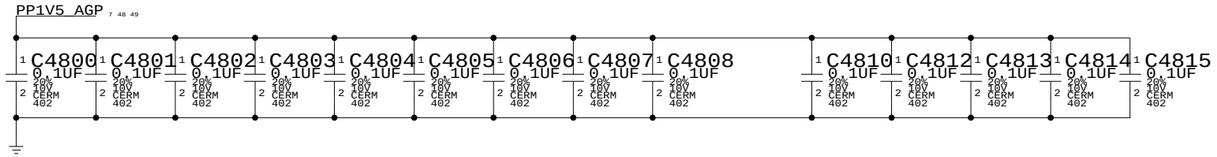
LEVEL SHIFTER FOR U3LITE & NVIDIA AGP BUS.

AGP BUSY AND STOP NOT USED IN THIS DESIGN



U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)





MASTER: GILA

U3LITE AGP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 48 OF 99	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0155	1	IC,NV18B,GRAPHIC CTRL	U4900	NV18B
338S0113	1	IC,NV34,GRAPHIC CTRL	U4900	NV34

NVIDIA RECOMMENDS A WIDER RANGE OF CAP VALUES, EMC LIKES ONE VALUE

U4900
NV18B
BGA
(1 OF 5)
OMIT

AGP_AD<0>	AJ28	PCIAD0
AGP_AD<1>	AK28	PCIAD1
AGP_AD<2>	AH27	PCIAD2
AGP_AD<3>	AK27	PCIAD3
AGP_AD<4>	AJ27	PCIAD4
AGP_AD<5>	AH26	PCIAD5
AGP_AD<6>	AJ26	PCIAD6
AGP_AD<7>	AH25	PCIAD7
AGP_AD<8>	AH23	PCIAD8
AGP_AD<9>	AJ23	PCIAD9
AGP_AD<10>	AH22	PCIAD10
AGP_AD<11>	AJ22	PCIAD11
AGP_AD<12>	AJ21	PCIAD12
AGP_AD<13>	AK21	PCIAD13
AGP_AD<14>	AH20	PCIAD14
AGP_AD<15>	AJ20	PCIAD15
AGP_AD<16>	AG26	PCIAD16
AGP_AD<17>	AE24	PCIAD17
AGP_AD<18>	AG25	PCIAD18
AGP_AD<19>	AG24	PCIAD19
AGP_AD<20>	AF24	PCIAD20
AGP_AD<21>	AG23	PCIAD21
AGP_AD<22>	AE22	PCIAD22
AGP_AD<23>	AF22	PCIAD23
AGP_AD<24>	AE21	PCIAD24
AGP_AD<25>	AG20	PCIAD25
AGP_AD<26>	AG19	PCIAD26
AGP_AD<27>	AF19	PCIAD27
AGP_AD<28>	AE19	PCIAD28
AGP_AD<29>	AF18	PCIAD29
AGP_AD<30>	AG18	PCIAD30
AGP_AD<31>	AE18	PCIAD31

		AGP 2X,4X : AGP 8X
AGP_CBE<0>	AJ24	PCIC0/BE0* : C0*/BE0
AGP_CBE<1>	AH19	PCIC1/BE1* : C1*/BE1
AGP_CBE<2>	AF25	PCIC2/BE2* : C2*/BE2
AGP_CBE<3>	AG22	PCIC3/BE3* : C3*/BE3
AGP_CLK66M_GPU	AG12	PCICLK : CLK
NV_PCIRST_L	AF15	PCIRST* : RST*
AGP_GNT	AE15	PCIGNT* : GNT
AGP_REQ	AF13	PCIREQ* : REQ
AGP_FRAME	AK16	PCIFRAME* : FRAME
AGP_IRDY	AG16	PCIIRDY* : IRDY
AGP_TRDY	AJ17	PCITRDY* : TRDY
AGP_DEVSEL	AJ16	PCIDEVSEL* : DEVSEL
AGP_STOP	AH17	PCISTOP* : STOP
AGP_PAR	AK18	PCIPAR : PAR
AGP_INT_L	AG15	PCIINTA* : INTA
TP_GPU_INTB_L	AE10	NC_PCIINTB* : INTB
AGP_RBF	AG14	AGPRBF* : RBF
AGP_WBF	AG17	AGPWBF* : WBF
AGP_DBI_HI	AJ18	AGPPIPE* : DBI_HI
AGP_DBI_LO	AJ19	<RESRVD> : DBI_LO
AGP_ST<0>	AG13	AGPST0 : ST0
AGP_ST<1>	AE16	AGPST1 : ST1
AGP_ST<2>	AE13	AGPST2 : ST2
AGP_AD_STBF<0>	AK24	AGPADSTBF0 : ADSTBF0
AGP_AD_STBS<0>	AJ25	AGPADSTBS0* : ADSTBS0
AGP_AD_STBF<1>	AG21	AGPADSTBF1 : ADSTBF1
AGP_AD_STBS<1>	AF21	AGPADSTBS1* : ADSTBS1
AGP_SB_STBF	AK13	AGPSBSTBF : SBSTBF
AGP_SB_STBS	AJ13	AGPSBSTBS* : SBSTBS
AGP_SBA_L<0>	AJ11	AGPSBA0 : SBA0*
AGP_SBA_L<1>	AH11	AGPSBA1 : SBA1*
AGP_SBA_L<2>	AJ12	AGPSBA2 : SBA2*
AGP_SBA_L<3>	AH12	AGPSBA3 : SBA3*
AGP_SBA_L<4>	AJ14	AGPSBA4 : SBA4*
AGP_SBA_L<5>	AH14	AGPSBA5 : SBA5*
AGP_SBA_L<6>	AJ15	AGPSBA6 : SBA6*
AGP_SBA_L<7>	AH15	AGPSBA7 : SBA7*
GPU_MBDET_L	AF16	<RESRVD> : MBDET*
AGP_BUSY_L	AF12	AGPBUSY* : BUSY*
STOP_AGP_L	AG11	AGPSTOP* : STOP*
GPU_AGP_VREF	AK29	AGPVREF : AGPVREF

PP1V5_AGP	AE14, AE11, AE17, AE20, AE23, AD11, AD14, AD23, AD20, AD17
AGPVDDQ	
VDD	AA17, AA18, L20, Y20, L13, Y13, N20, P20, U20, V20, L11, N11, P11, U11, V11, Y11, L14, Y14, L17, Y17, L18, Y18
VDD33	H6, AC6, U7, G14, U6, AD15, H7, AD16, AD19, AD22, AC7, AD12, P24
PPVCORE_GPU	
VD50CLAMP0	N4
VD50CLAMP1	AE9
AGP_PLLVDD	AE12
AGPCALPD	AA13
AGPCALPU	AA14
TESTMODE	AE5
NC	A1, AK30, G6, R7, T7

OUTPUT DRIVER BYPASS

C4912 0.01UF, C4911 0.01UF, C4904 0.1UF, C4905 0.1UF, C4906 0.1UF, C4913 0.1UF, C4907 0.1UF, C4908 0.1UF, C4909 0.1UF, C4910 0.1UF
10% 16V CERM 402

CORE BYPASS

C4914 0.01UF, C4915 0.01UF, C4916 0.1UF, C4917 0.1UF, C4918 0.1UF, C4919 0.1UF, C4920 0.1UF, C4921 0.1UF, C4922 0.1UF, C4923 0.1UF, C4924 0.1UF
20% 10V CERM 402

C4925 0.01UF 10% 16V CERM 402; C4926 0.01UF 10% 16V CERM 402; C4927 0.1UF, C4928 0.1UF, C4929 0.1UF, C4930 0.1UF, C4931 0.1UF, C4932 0.1UF
20% 10V CERM 402

C4961 10UF 20% 6.3V CERM 805; C4960 10UF 20% 6.3V CERM 805; C4902 10UF, C4900 10UF, C4903 10UF, C4901 10UF 20% 6.3V CERM 805; C4933 0.1UF, C4934 0.1UF, C4935 0.1UF
20% 10V CERM 402

PP3V3_AGP 59 58 57 56 52 51 50 49 48 7

NV34 L4901 1000-OHM-EMI SM

AGP_PLLVDD — VOLTAGE=3.3V MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

PP3V3_AGP 7 48 49 50 51 52 56 57 58 59

NV34 C4959 4.7UF 20% 6.3V CERM 805; NV34 C4956 0.1UF 20% 10V CERM 402; NV34 C4955 0.001UF 10% 50V CERM 402

I/O BYPASS

C4936 0.01UF, C4942 0.01UF, C4938 0.1UF, C4939 0.1UF, C4941 0.1UF, C4937 0.1UF
10% 16V CERM 402

C4943 10UF 20% 6.3V CERM 805; C4944 0.01UF, C4945 0.01UF 10% 16V CERM 402; C4946 0.1UF, C4947 0.1UF, C4949 0.1UF, C4950 0.1UF, C4951 0.1UF, C4952 0.1UF
20% 10V CERM 402

PP5V_AGP 7 50 59

C4953 0.1UF, C4954 0.1UF 20% 10V CERM 402

50 OHM TO VDDQ — AGPCALPD
50 OHM TO GND — AGPCALPU
GPU_50PULLUP
GPU_50PULLDWN
10K OHM TO GND — TESTMODE
GPU_TMODE

R4901 10K 5% 1/16W MF 402
R4900 49.9 1% 1/16W MF 402
R4902 49.9 1% 1/16W MF 402 — PP1V5_AGP 7 48 49

R4906 3.32K 1% 1/16W MF 402 — PP1V5_AGP 49 48 7
R4907 1.02K 1% 1/16W MF 402
C4957 0.01UF 20% 10V CERM 402
GPU_AGP_VREF 49 — VOLTAGE=1.35V MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

PP3V3_AGP 59
NV34 R4910 10K 5% 1/16W MF 402
NV34 R4911 10K 5% 1/16W MF 402

R4905 1K — NVAGP_TRST_L
R4904 1K — NVAGP_TCLK
TP_NVAGP_TDO 6
TP_NVAGP_TDI
TP_NVAGP_TMS

C2 TCLK, C1 TMS, D1 TDI, E2 TDO, D2 TRST*

TP_GPU<0> TP_GPU<1> TP_GPU<2> TP_GPU<3> TP_GPU<4> — NO TEST

BOUNDRY SCAN AVAILABLE ONLY ON NV3X SERIES

R4912 0 5% 1/16W MF 402 — PCI_RESET_L 77 76 75 74 51 6

PP3V3_AGP 7 48 49 50 51 52 56 57 58 59

R4908 4.99K 1% 1/16W MF 402 — AGP_INT_L 25 49

48 NB_AGP_GCDET_L
48 AGP_TYPEDET_L

R4913 0 5% 1/16W MF 402
R4909 10K 5% 1/16W MF 402

DOES HOOP UP AGP_BUSY_L &
STOP_AGP_L TO 3.3V OR 1.5V?

AGP VERSION SELECT
(LOW = AGP V3.X)
(HIGH = AGP V2.X)

R4903 0 5% 1/16W MF 402

GPU AGP I/O REFERENCE
(PLACE CLOSE TO U3LITE AGP BALLS)

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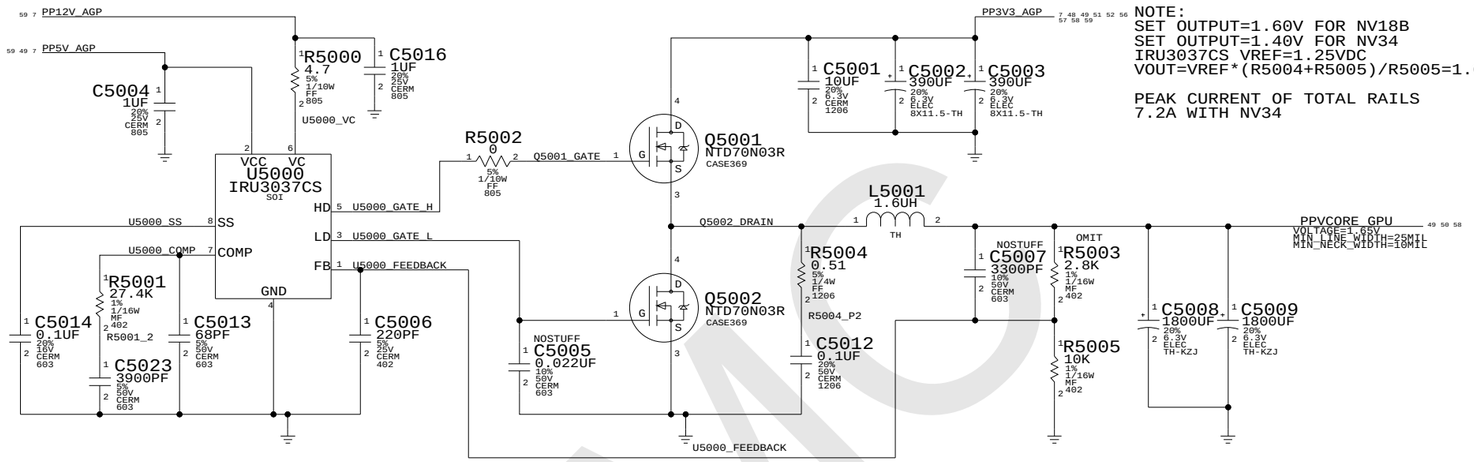
NVIDIA AGP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 49 OF 99	

PPVOCRE_GPU	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
1.60VDC	114S2803	1	RES,2.8K OHM,1/16W,1%,0402	R5003	NV18B
1.40VDC	114S1213	1	RES,1.21K OHM,1/16W,1%,0402	R5003	NV34

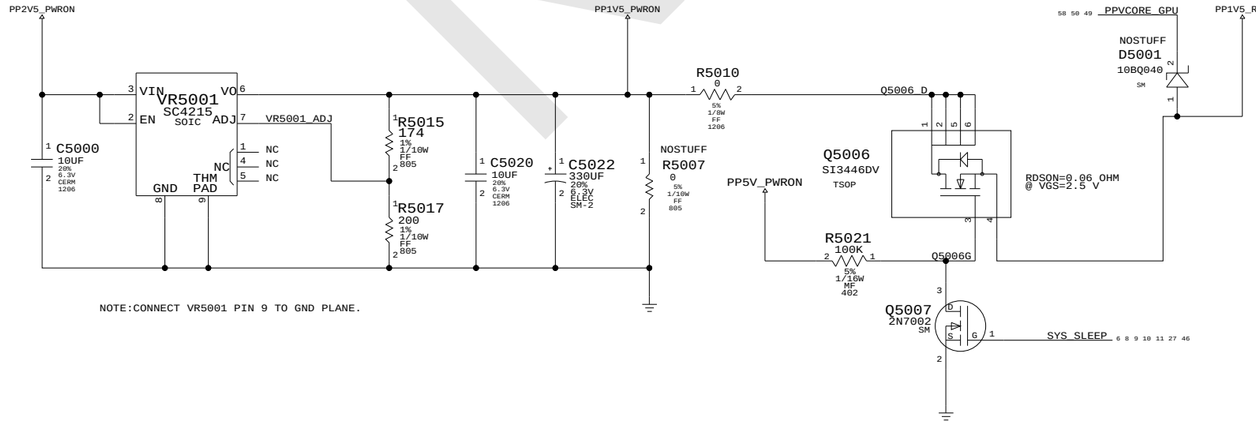
GPU VCORE VREG



NOTE:
SET OUTPUT=1.60V FOR NV18B
SET OUTPUT=1.40V FOR NV34
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R5004+R5005)/R5005=1.60(OR 1.40) VDC

PEAK CURRENT OF TOTAL RAILS
7.2A WITH NV34

AGP 1.5V VREG



NOTE:CONNECT VR5001 PIN 9 TO GND PLANE.

NOTE:
SET OUTPUT=1.5V
SC4215 VREF=0.8VDC
VOUT=VREF*(R5015+R5017)/R5017=1.5 VDC

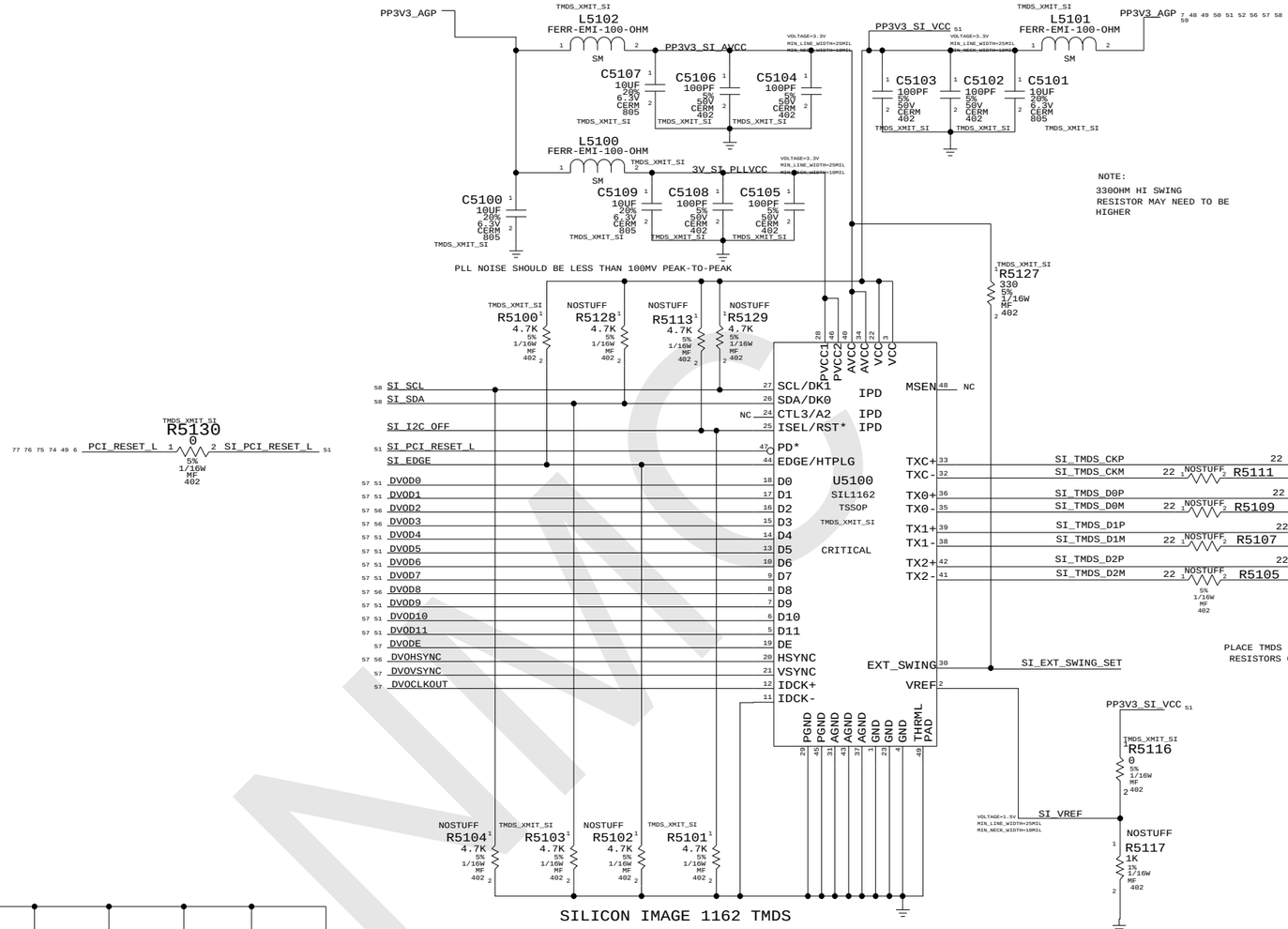
PEAK CURRENT OF TOTAL RAILS
0.95A

GRAPHICS VREGS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT	OF
NONE	50	99

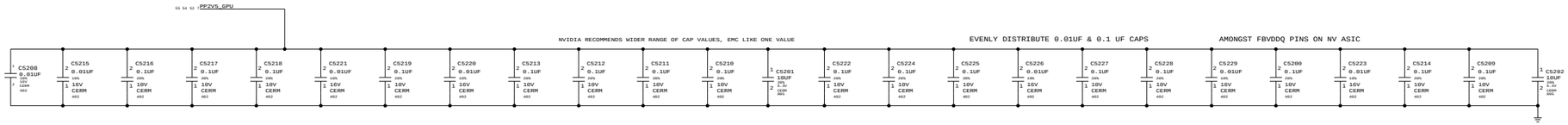


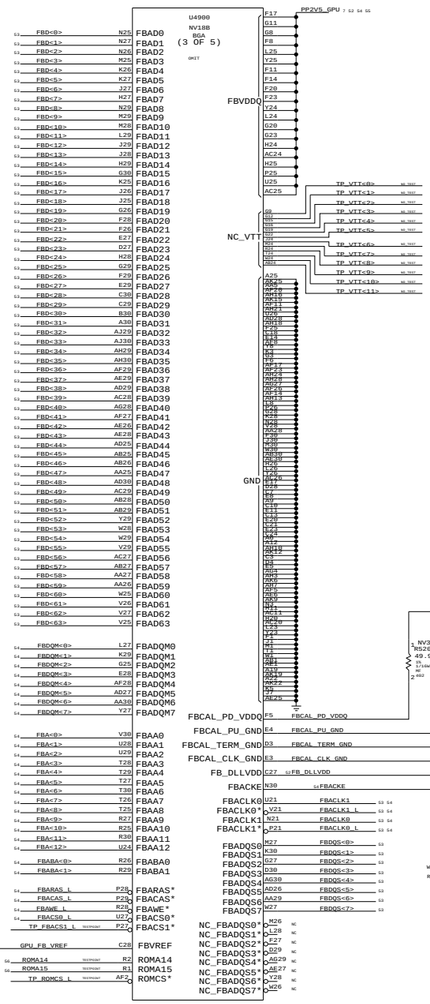
EXTERNAL TMDS TRANSMITTER

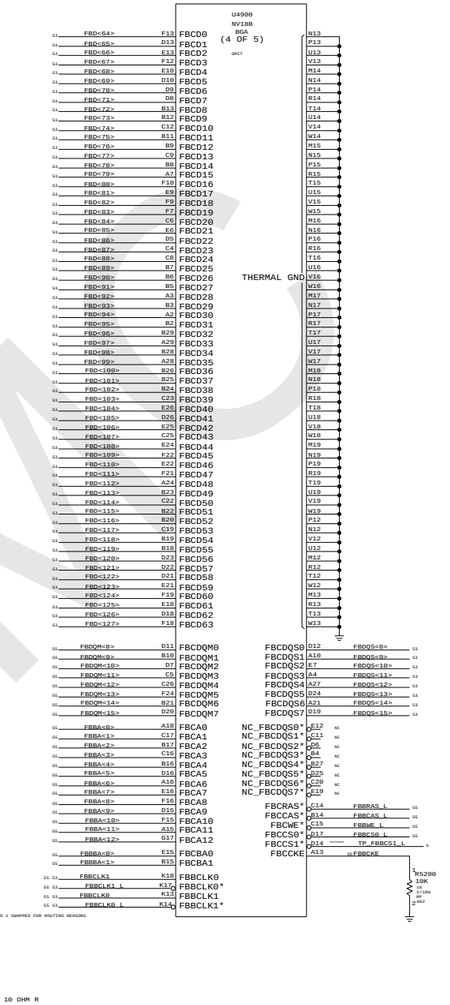
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 51 OF 99	

DRAWING







NVIDIA FRAME BUFFER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
E	051-6482	13
SCALE: NONE	SHT 52 OF 99	

PLACE R'S CLOSE TO MEMORY

FBD<31>	15	1	8	RP5320	RFBD<31>	
FBD<30>	15	2	7	RP5320	RFBD<30>	
FBD<29>	15	3	6	RP5320	RFBD<29>	
FBD<28>	15	4	5	RP5320	RFBD<28>	
FBD<27>	15	1	8	RP5321	RFBD<27>	
FBD<26>	15	2	7	RP5321	RFBD<26>	
FBD<25>	15	3	6	RP5321	RFBD<25>	
FBD<24>	15	4	5	RP5321	RFBD<24>	
FBD<0>	15	1	8	RP5322	RFBD<0>	
FBD<1>	15	2	7	RP5322	RFBD<1>	
FBD<2>	15	3	6	RP5322	RFBD<2>	
FBD<3>	15	4	5	RP5322	RFBD<3>	
FBD<17>	15	1	8	RP5323	RFBD<17>	
FBD<16>	15	2	7	RP5323	RFBD<16>	
FBD<18>	15	3	6	RP5323	RFBD<18>	
FBD<19>	15	4	5	RP5323	RFBD<19>	
FBD<15>	15	1	8	RP5324	RFBD<15>	
FBD<14>	15	2	7	RP5324	RFBD<14>	
FBD<13>	15	3	6	RP5324	RFBD<13>	
FBD<12>	15	4	5	RP5324	RFBD<12>	
FBD<10>	15	1	8	RP5325	RFBD<10>	
FBD<11>	15	2	7	RP5325	RFBD<11>	
FBD<9>	15	3	6	RP5325	RFBD<9>	
FBD<8>	15	4	5	RP5325	RFBD<8>	
FBD<5>	15	1	8	RP5326	RFBD<5>	
FBD<6>	15	2	7	RP5326	RFBD<6>	
FBD<4>	15	3	6	RP5326	RFBD<4>	
FBD<7>	15	4	5	RP5326	RFBD<7>	
FBD<20>	15	1	8	RP5327	RFBD<20>	
FBD<21>	15	2	7	RP5327	RFBD<21>	
FBD<22>	15	3	6	RP5327	RFBD<22>	
FBD<23>	15	4	5	RP5327	RFBD<23>	

FBD<32>	15	3	6	RP5328	RFBD<32>	
FBD<33>	15	4	5	RP5328	RFBD<33>	
FBD<34>	15	1	8	RP5328	RFBD<34>	
FBD<35>	15	2	7	RP5328	RFBD<35>	
FBD<36>	15	4	5	RP5316	RFBD<36>	
FBD<37>	15	3	6	RP5316	RFBD<37>	
FBD<38>	15	2	7	RP5316	RFBD<38>	
FBD<39>	15	1	8	RP5316	RFBD<39>	
FBD<40>	15	2	7	RP5329	RFBD<40>	
FBD<41>	15	1	8	RP5329	RFBD<41>	
FBD<42>	15	3	6	RP5329	RFBD<42>	
FBD<43>	15	4	5	RP5329	RFBD<43>	
FBD<44>	15	1	8	RP5330	RFBD<44>	
FBD<45>	15	2	7	RP5330	RFBD<45>	
FBD<46>	15	4	5	RP5330	RFBD<46>	
FBD<47>	15	3	6	RP5330	RFBD<47>	
FBD<48>	15	4	5	RP5331	RFBD<48>	
FBD<49>	15	3	6	RP5331	RFBD<49>	
FBD<50>	15	1	8	RP5331	RFBD<50>	
FBD<51>	15	2	7	RP5331	RFBD<51>	
FBD<52>	15	4	5	RP5300	RFBD<52>	
FBD<53>	15	3	6	RP5300	RFBD<53>	
FBD<54>	15	2	7	RP5300	RFBD<54>	
FBD<55>	15	1	8	RP5300	RFBD<55>	
FBD<56>	15	1	8	RP5301	RFBD<56>	
FBD<57>	15	2	7	RP5301	RFBD<57>	
FBD<58>	15	4	5	RP5301	RFBD<58>	
FBD<59>	15	3	6	RP5301	RFBD<59>	
FBD<60>	15	1	8	RP5302	RFBD<60>	
FBD<61>	15	3	6	RP5302	RFBD<61>	
FBD<62>	15	2	7	RP5302	RFBD<62>	
FBD<63>	15	4	5	RP5302	RFBD<63>	

PLACE R'S CLOSE TO GPU

FBACLK1 — R5316 100 1% 1/10W MF 402 — PLACE 100OHM TERM AT RAM — FBACLK1_L

FBACLK0 — R5317 100 1% 1/10W MF 402 — PLACE 100OHM TERM AT RAM — FBACLK0_L

FBBCLK1 — R5318 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM — FBBCLK1_L

FBBCLK0 — R5319 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM — FBBCLK0_L

FBD<64>	GPU128BIT	15	1	8	RP5310	RFBD<64>
FBD<65>	GPU128BIT	15	2	7	RP5310	RFBD<65>
FBD<66>	GPU128BIT	15	3	6	RP5310	RFBD<66>
FBD<67>	GPU128BIT	15	4	5	RP5310	RFBD<67>
FBD<84>	GPU128BIT	15	1	8	RP5309	RFBD<84>
FBD<85>	GPU128BIT	15	2	7	RP5309	RFBD<85>
FBD<86>	GPU128BIT	15	3	6	RP5309	RFBD<86>
FBD<87>	GPU128BIT	15	4	5	RP5309	RFBD<87>
FBD<72>	GPU128BIT	15	4	5	RP5319	RFBD<72>
FBD<73>	GPU128BIT	15	3	6	RP5319	RFBD<73>
FBD<75>	GPU128BIT	15	2	7	RP5319	RFBD<75>
FBD<74>	GPU128BIT	15	1	8	RP5319	RFBD<74>
FBD<68>	GPU128BIT	15	1	8	RP5308	RFBD<68>
FBD<70>	GPU128BIT	15	2	7	RP5308	RFBD<70>
FBD<69>	GPU128BIT	15	3	6	RP5308	RFBD<69>
FBD<71>	GPU128BIT	15	4	5	RP5308	RFBD<71>
FBD<80>	GPU128BIT	15	1	8	RP5307	RFBD<80>
FBD<81>	GPU128BIT	15	2	7	RP5307	RFBD<81>
FBD<82>	GPU128BIT	15	3	6	RP5307	RFBD<82>
FBD<83>	GPU128BIT	15	4	5	RP5307	RFBD<83>
FBD<76>	GPU128BIT	15	4	5	RP5317	RFBD<76>
FBD<77>	GPU128BIT	15	3	6	RP5317	RFBD<77>
FBD<78>	GPU128BIT	15	2	7	RP5317	RFBD<78>
FBD<79>	GPU128BIT	15	1	8	RP5317	RFBD<79>
FBD<91>	GPU128BIT	15	1	8	RP5318	RFBD<91>
FBD<90>	GPU128BIT	15	2	7	RP5318	RFBD<90>
FBD<89>	GPU128BIT	15	3	6	RP5318	RFBD<89>
FBD<88>	GPU128BIT	15	4	5	RP5318	RFBD<88>
FBD<95>	GPU128BIT	15	1	8	RP5303	RFBD<95>
FBD<94>	GPU128BIT	15	2	7	RP5303	RFBD<94>
FBD<93>	GPU128BIT	15	3	6	RP5303	RFBD<93>
FBD<92>	GPU128BIT	15	4	5	RP5303	RFBD<92>

FBD<96>	GPU128BIT	15	4	5	RP5315	RFBD<96>
FBD<97>	GPU128BIT	15	3	6	RP5315	RFBD<97>
FBD<98>	GPU128BIT	15	2	7	RP5315	RFBD<98>
FBD<99>	GPU128BIT	15	1	8	RP5315	RFBD<99>
FBD<100>	GPU128BIT	15	4	5	RP5314	RFBD<100>
FBD<101>	GPU128BIT	15	3	6	RP5314	RFBD<101>
FBD<102>	GPU128BIT	15	2	7	RP5314	RFBD<102>
FBD<103>	GPU128BIT	15	1	8	RP5314	RFBD<103>
FBD<104>	GPU128BIT	15	1	8	RP5312	RFBD<104>
FBD<105>	GPU128BIT	15	2	7	RP5312	RFBD<105>
FBD<106>	GPU128BIT	15	3	6	RP5312	RFBD<106>
FBD<107>	GPU128BIT	15	4	5	RP5312	RFBD<107>
FBD<108>	GPU128BIT	15	1	8	RP5313	RFBD<108>
FBD<109>	GPU128BIT	15	2	7	RP5313	RFBD<109>
FBD<110>	GPU128BIT	15	3	6	RP5313	RFBD<110>
FBD<111>	GPU128BIT	15	4	5	RP5313	RFBD<111>
FBD<112>	GPU128BIT	15	4	5	RP5311	RFBD<112>
FBD<113>	GPU128BIT	15	3	6	RP5311	RFBD<113>
FBD<114>	GPU128BIT	15	2	7	RP5311	RFBD<114>
FBD<115>	GPU128BIT	15	1	8	RP5311	RFBD<115>
FBD<116>	GPU128BIT	15	4	5	RP5306	RFBD<116>
FBD<117>	GPU128BIT	15	3	6	RP5306	RFBD<117>
FBD<118>	GPU128BIT	15	2	7	RP5306	RFBD<118>
FBD<119>	GPU128BIT	15	1	8	RP5306	RFBD<119>
FBD<120>	GPU128BIT	15	1	8	RP5304	RFBD<120>
FBD<121>	GPU128BIT	15	2	7	RP5304	RFBD<121>
FBD<122>	GPU128BIT	15	4	5	RP5304	RFBD<122>
FBD<123>	GPU128BIT	15	3	6	RP5304	RFBD<123>
FBD<124>	GPU128BIT	15	1	8	RP5305	RFBD<124>
FBD<125>	GPU128BIT	15	3	6	RP5305	RFBD<125>
FBD<126>	GPU128BIT	15	2	7	RP5305	RFBD<126>
FBD<127>	GPU128BIT	15	4	5	RP5305	RFBD<127>

PLACE THESE R CLOSE TO SGRAM

FBDQS<0>	R5301	15	RFBDQS<0>
FBDQS<1>	R5302	15	RFBDQS<1>
FBDQS<2>	R5300	15	RFBDQS<2>
FBDQS<3>	R5303	15	RFBDQS<3>
FBDQS<4>	R5307	15	RFBDQS<4>
FBDQS<5>	R5305	15	RFBDQS<5>
FBDQS<6>	R5306	15	RFBDQS<6>
FBDQS<7>	R5304	15	RFBDQS<7>

(1% 1/16W MF 402)

PLACE THESE R CLOSE TO SGRAM

FBDQS<8>	R5308	15	RFBDQS<8>
FBDQS<9>	R5314	15	RFBDQS<9>
FBDQS<10>	R5309	15	RFBDQS<10>
FBDQS<11>	R5315	15	RFBDQS<11>
FBDQS<12>	R5310	15	RFBDQS<12>
FBDQS<13>	R5313	15	RFBDQS<13>
FBDQS<14>	R5311	15	RFBDQS<14>
FBDQS<15>	R5312	15	RFBDQS<15>

(GPU128BIT; 1% 1/16W MF 402)

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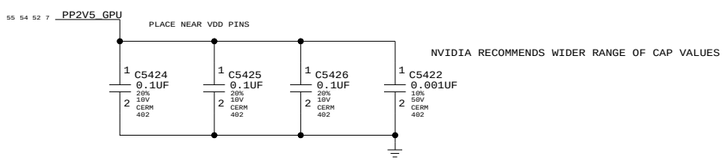
FB TERMINATION

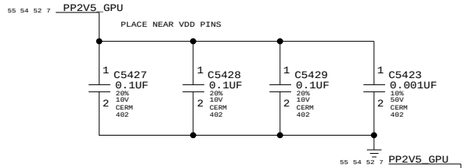
APPLE COMPUTER INC.

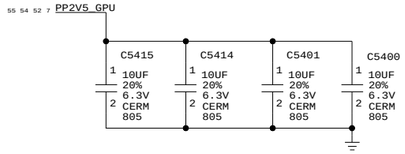
SIZE	DRAWING NUMBER	REV.
D	051-6482	13

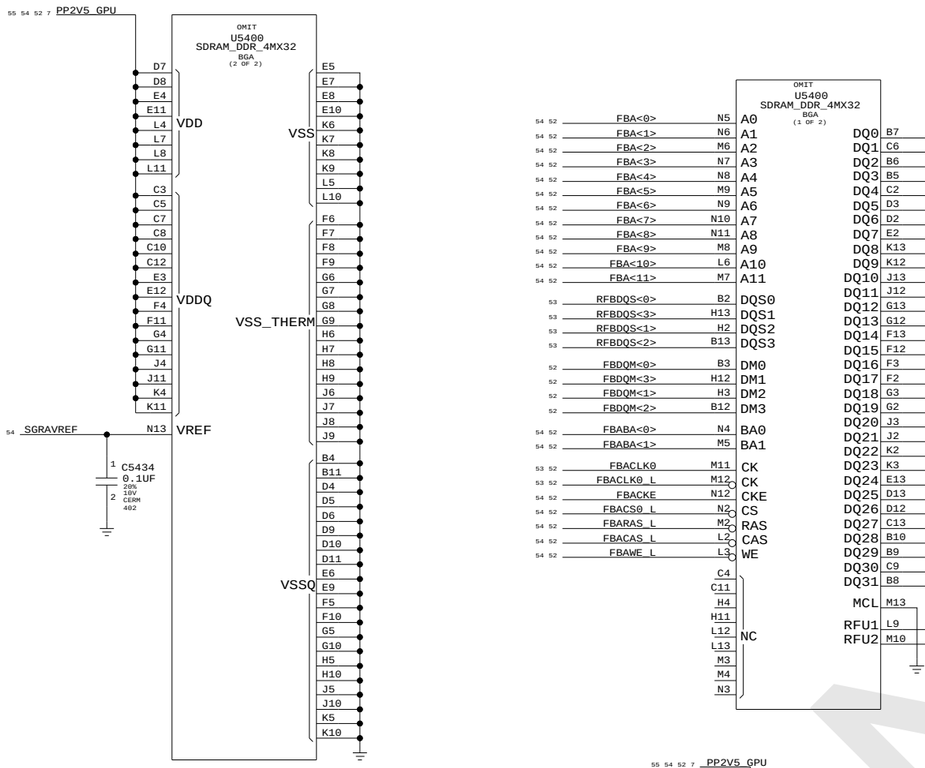
SCALE: NONE — SHT 53 OF 99

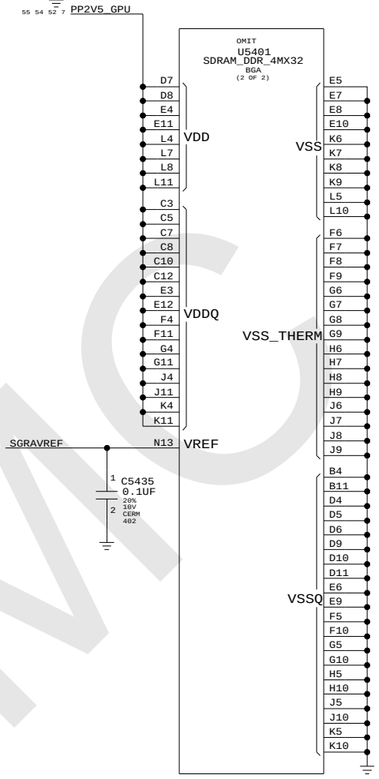


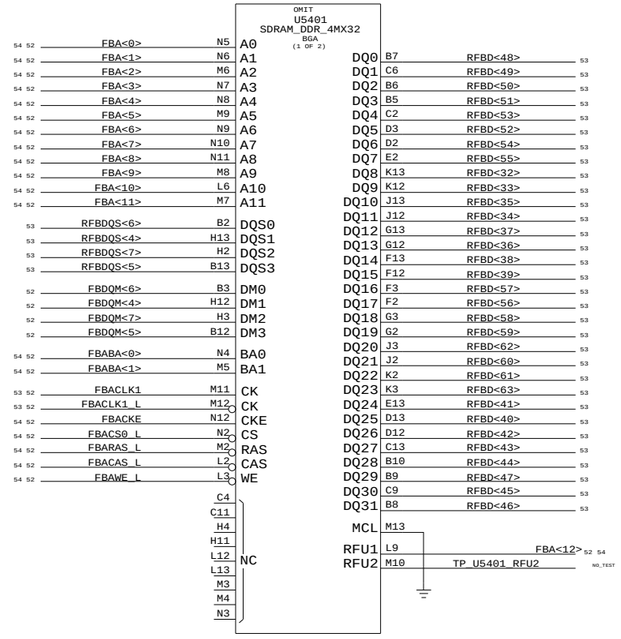
NVIDIA RECOMMENDS WIDER RANGE OF CAP VALUES

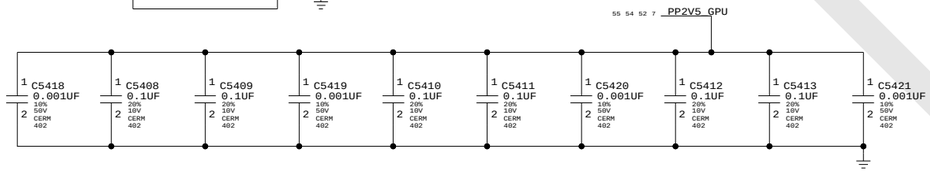


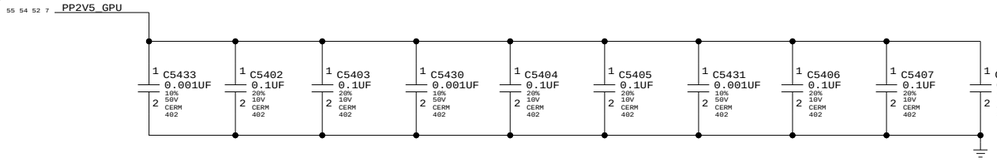






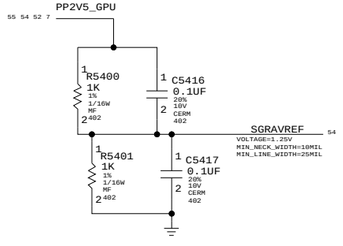






EVENLY PLACE 0.1UF CAP & 0.01UF CAPS

DDR SDRAM A VREF



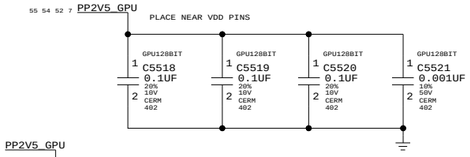
SGRAM0 & SGRAM1 MEMORY SUPPORT

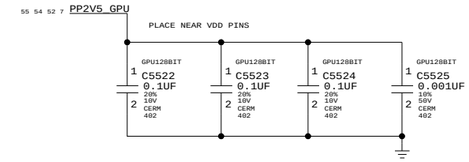
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	SAMSUNG
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX

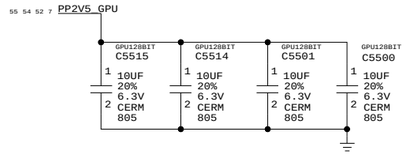
GPU DDR SDRAM A

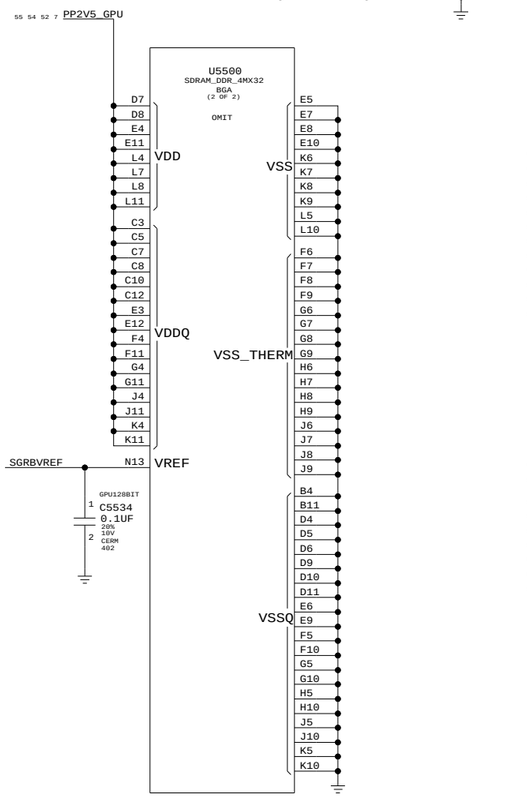
APPLE COMPUTER INC.

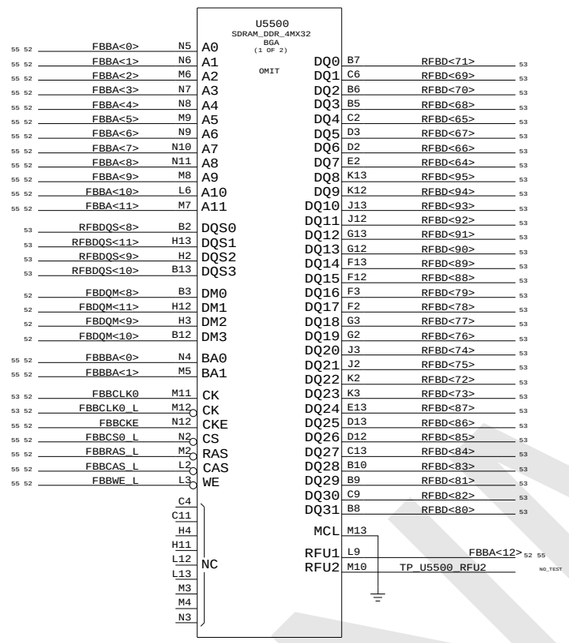
SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 54 OF 99	

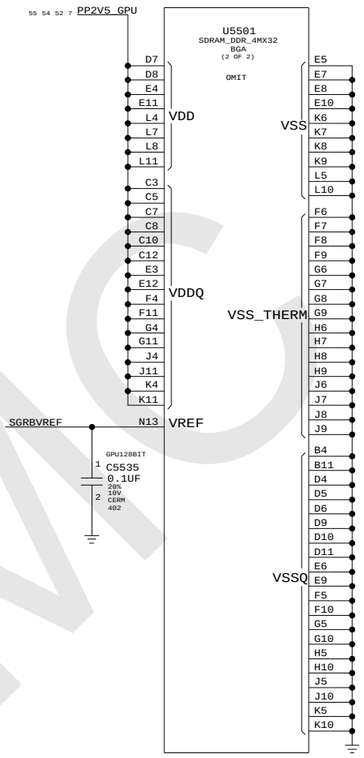


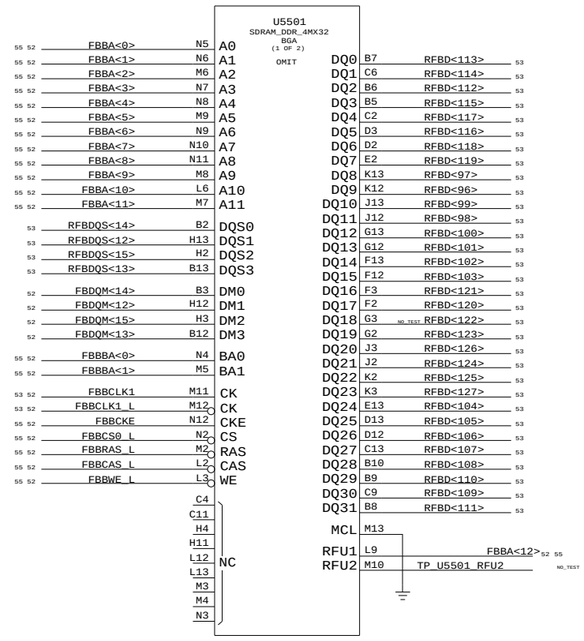


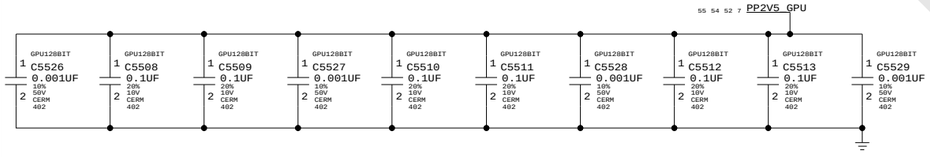


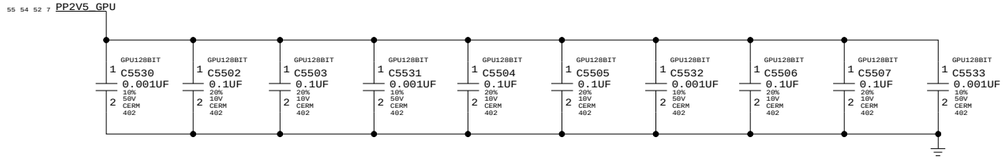






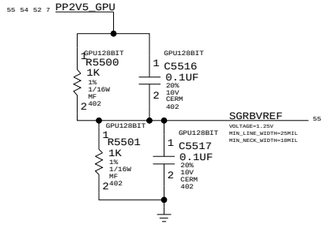






DDR SDRAM B VREF

EVENLY PLACE 0.1UF CAP & 0.01 UF CAPS



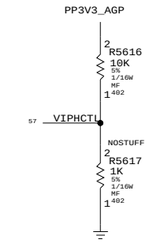
SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	GPU128BIT_SAMSUNG
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	GPU128BIT_HYNIX

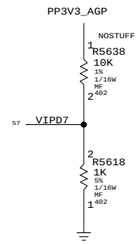
GPU DDR SDRAM B

APPLE COMPUTER INC.

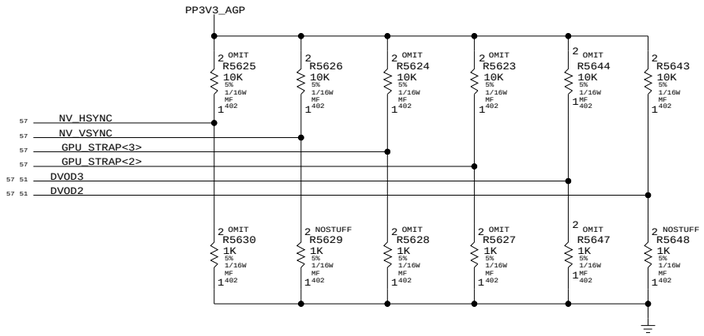
SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 55 OF 99	



(5) HOST MODE
[0] = [VIPHCTL]
0 = PCI MODE
* 1 = AGP MODE

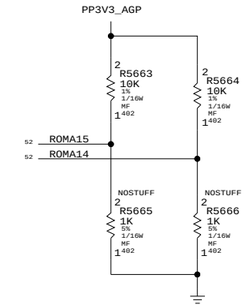


(6) AGP SIDEBAND
[0] = [VIPD7]
* 0 = ENABLE AGP SIDEBAND
1 = DISABLE AGP SIDEBAND

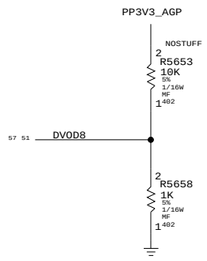


(8) FRAME BUFFER MEMORY SPEED
[5..0] = [NV11_HSYNC,NV11_VSYNC,GPU_STRAP<3>,GPU_STRAP<2>,DVOD3,DVOD2]

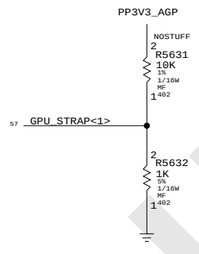
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
110111 = 270MHZ SAMSUNG (NV18B)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5623		270MHZ_SAM_18
116S1104	1	RES,10K-OHM,1/16W,5%	R5644		270MHZ_SAM_18
116S1103	1	RES,1K-OHM,1/16W,5%	R5628		270MHZ_SAM_18
110011 = 270MHZ HYNIX (NV18B)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5644		270MHZ_HYN_18
116S1103	2	RES,1K-OHM,1/16W,5%	R5628,R5627		270MHZ_HYN_18
111101 = 270MHZ SAMSUNG (NV34)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5624		270MHZ_SAM_34
116S1104	1	RES,10K-OHM,1/16W,5%	R5623		270MHZ_SAM_34
116S1103	1	RES,1K-OHM,1/16W,5%	R5647		270MHZ_SAM_34
111100 = 270MHZ HYNIX (NV34)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5624,R5623		270MHZ_HYN_34
116S1103	2	RES,1K-OHM,1/16W,5%	R5630,R5647		270MHZ_HYN_34



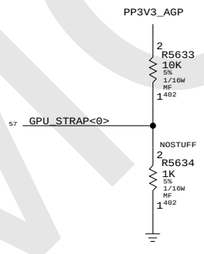
(1) ROM TYPE (OVERRIDDEN IF STRAP1 = 0)
[1..0] = [ROMA15,ROMA14]
00 = PARALLEL
01 = SERIAL AT25F
10 = SERIAL SST45VF
* 11 = SERIAL FUTURE



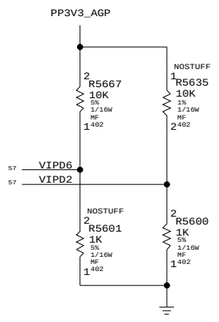
FAST WRITE SUPPORT
0=ENABLE
1=DISABLE



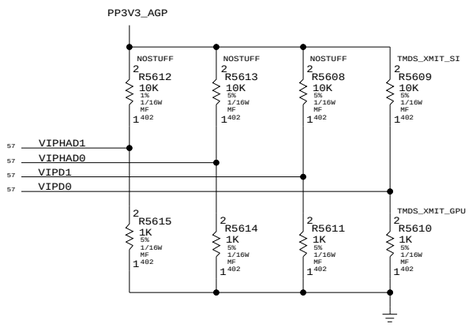
(9) SUB-VENDOR
[0] = [GPU_STRAP<1>]
* 0 = SYSTEM BIOS (VENDOR & SUBSYSTEM ID=0X0000)
1 = ADAPTER CARD VGA BIOS (VENDOR & SUBSYSTEM ID=0X54-0X57)



(10) PCI ADDRESS BUS
[0] = [GPU_STRAP<0>]
0 = REVERSED
* 1 = NORMAL

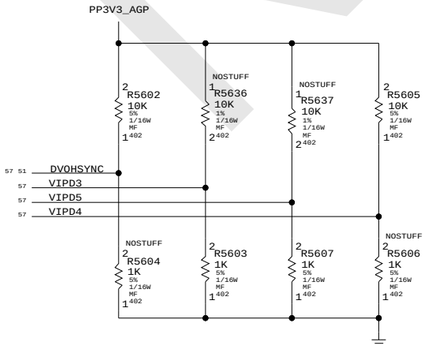


(2) CRYSTAL FREQUENCY SELECT
[1..0] = [VIPD6,VIPD2]
00 = 13.5MHZ
01 = 14.38MHZ
* 10 = 27MHZ
11 = {UNDEFINED}

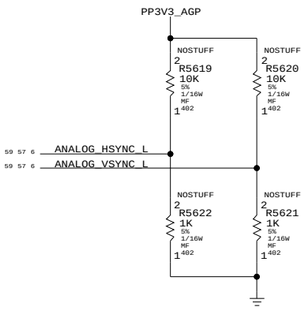


(4) USER DEFINED STRAPS
[3..0] = [VIPHAD1,VIPHAD0,VIPD1,VIPD0]

THESE BITS ARE UNDEFINED BUT THEY
MUST BE KEPT LOW DURING RESET



(3) PCI DEVICE ID
[3..0] = [DVOHSYNC,VIPD3,VIPD5,VIPD4]
0010 = 0X112 GEFORCE2 GO
0011 = 0X113 QUADRO2 GO
0100 = 0X114 NV17M
0000 = 0X110 GEFORCE2GO MX (NV11B)
* 1001 = NV18B,NV31,NV34



(7) TV MODE
[1..0] = [ANALOG_HSYNC*,ANALOG_VSYNC*]
00 = SECAM
01 = NTSC
10 = PAL
11 = DISABLED

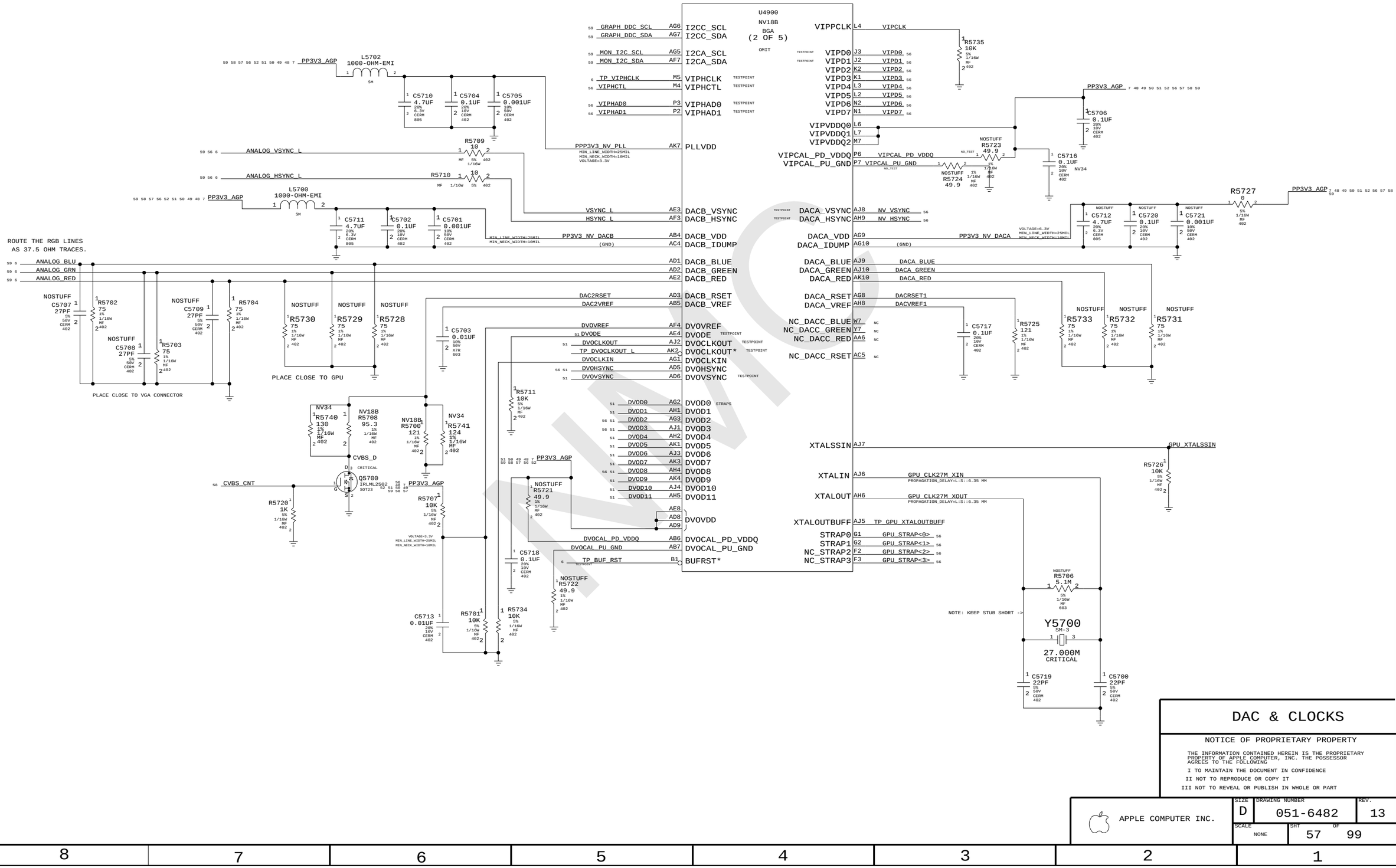
(THESE RESISTORS ARE ALL NOSTUFF)

NVIDIA STRAPS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6482 | REV. 13

SCALE NONE | SHT 56 OF 99


U4900
NV18B
BGA
(2 OF 5)
OMIT
I2CC_SCL
I2CC_SDA
I2CA_SCL
I2CA_SDA
VIPHCLK
VIPHCTL
VIPHAD0
VIPHAD1
PLLVDD
VSYNC_L
HSYNC_L
DACB_VSYNC
DACB_HSYNC
DACB_VDD
DACB_IDUMP
DACB_BLUE
DACB_GREEN
DACB_RED
DACB_RSET
DACB_VREF
DAC2RSET
DAC2VREF
DVOVREF
DVODE
DVOCLKOUT
DVOCLKOUT*
DVOCLKIN
DVOHSYNC
DVOVSYNC
DVOD0
DVOD1
DVOD2
DVOD3
DVOD4
DVOD5
DVOD6
DVOD7
DVOD8
DVOD9
DVOD10
DVOD11
DVOVDD
DVOCAL_PD_VDDQ
DVOCAL_PU_GND
BUFRST*
VIPPCLK
VIPD0
VIPD1
VIPD2
VIPD3
VIPD4
VIPD5
VIPD6
VIPD7
VIPVDDQ0
VIPVDDQ1
VIPVDDQ2
VIPCAL_PD_VDDQ
VIPCAL_PU_GND
DACA_VSYNC
DACA_HSYNC
DACA_VDD
DACA_IDUMP
DACA_BLUE
DACA_GREEN
DACA_RED
DACA_RSET
DACA_VREF
NC_DACC_BLUE
NC_DACC_GREEN
NC_DACC_RED
NC_DACC_RSET
XTALSSIN
XTALIN
XTALOUT
XTALOUTBUFF
STRAP0
STRAP1
NC_STRAP2
NC_STRAP3
PP3V3_AGP
L5702
1000-OHM-EMI
L5700
1000-OHM-EMI
PPP3V3_NV_PLL
PP3V3_NV_DACB
PP3V3_NV_DACA
ANALOG_VSYNC_L
ANALOG_HSYNC_L
ANALOG_BLU
ANALOG_GRN
ANALOG_RED
ROUTE THE RGB LINES
AS 37.5 OHM TRACES.
PLACE CLOSE TO VGA CONNECTOR
PLACE CLOSE TO GPU
GRAPH_DDC_SCL
GRAPH_DDC_SDA
MON_I2C_SCL
MON_I2C_SDA
TP_VIPHCLK
VIPHCTL
VIPHAD0
VIPHAD1
DVOVDDE
TP_DVOCLKOUT_L
DVOCLKIN
DVOHSYNC
DVOVSYNC
DVOD0
DVOCAL_PD_VDDQ
DVOCAL_PU_GND
TP_BUF_RST
VIPCLK
VIPD0
VIPD1
VIPD2
VIPD3
VIPD4
VIPD5
VIPD6
VIPD7
VIPCAL_PD_VDDQ
VIPCAL_PU_GND
DACA_VSYNC
DACA_HSYNC
DACA_VDD
DACA_IDUMP
DACA_BLUE
DACA_GREEN
DACA_RED
DACRSET1
DACVREF1
PP3V3_NV_DACA
GPU_XTALSSIN
GPU_CLK27M_XIN
GPU_CLK27M_XOUT
TP_GPU_XTALOUTBUFF
GPU_STRAP<0>
GPU_STRAP<1>
GPU_STRAP<2>
GPU_STRAP<3>
CVBS_D
CVBS_CNT
Q5700
IRLML2502
SOT23
CRITICAL
NOTE: KEEP STUB SHORT ->
Y5700
SM-3
27.000M
CRITICAL
R5735 10K
R5727 0
R5726 10K
R5706 5.1M
R5723 49.9
R5724 49.9
R5722 49.9
R5721 0.001UF
R5720 0.1UF
R5712 4.7UF
R5733 75
R5732 75
R5731 75
R5725 121
R5717 0.1UF
R5716 0.1UF
R5706 0.1UF
R5711 10K
R5734 10K
R5701 10K
R5713 0.01UF
R5703 0.01UF
R5718 0.1UF
R5719 22PF
R5700 22PF
R5740 130
R5708 95.3
R5700 121
R5741 124
R5720 1K
R5707 10K
R5709 10
R5710 10
R5702 75
R5704 75
R5730 75
R5729 75
R5728 75
R5708 75
R5709 27PF
R5710 27PF
R5707 27PF
R5708 27PF
C5710 4.7UF
C5704 0.1UF
C5705 0.001UF
C5711 4.7UF
C5702 0.1UF
C5701 0.001UF
C5703 0.01UF
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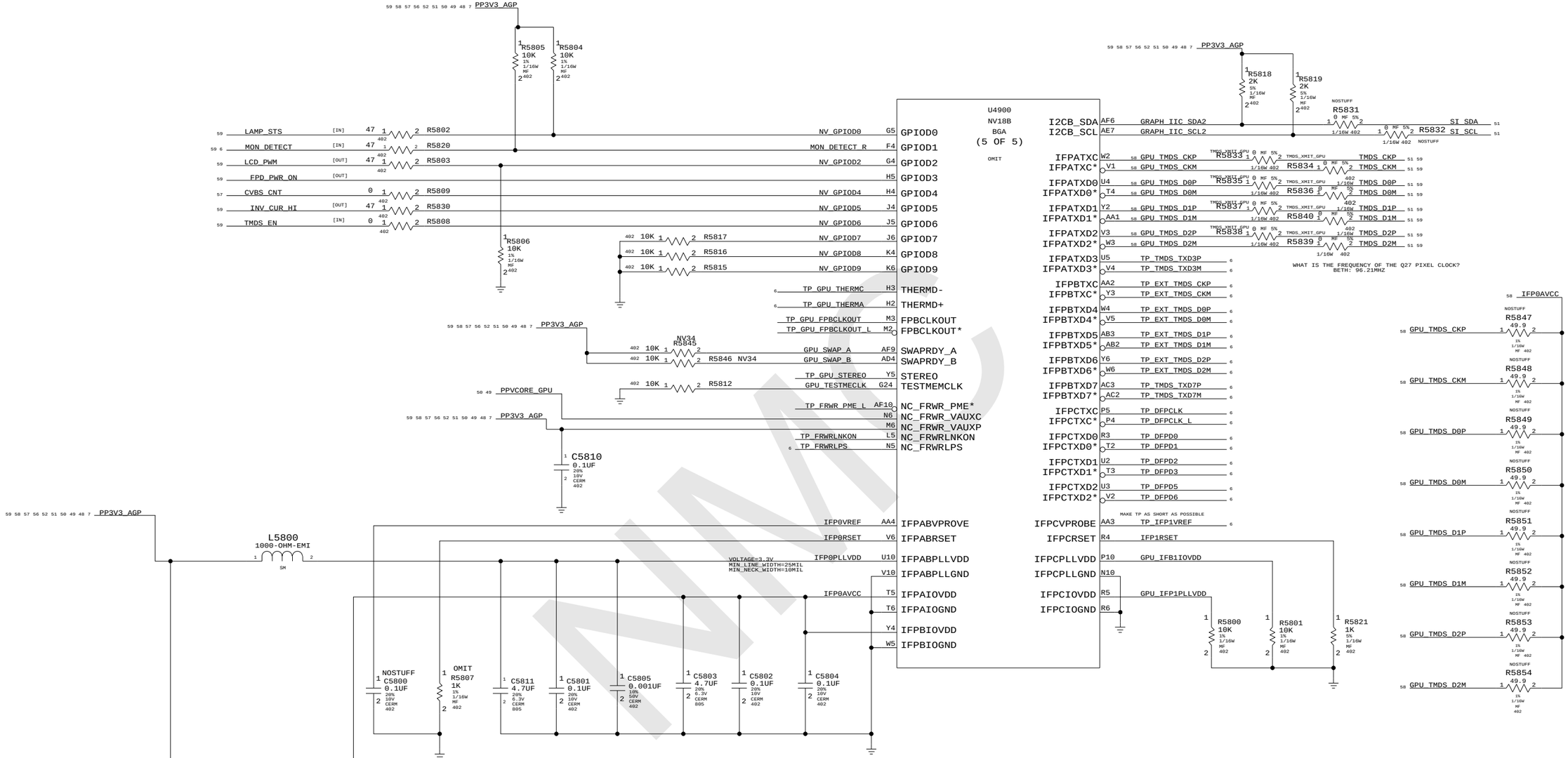
DAC & CLOCKS
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6482
REV. 13
SCALE NONE
SHT 57 OF 99



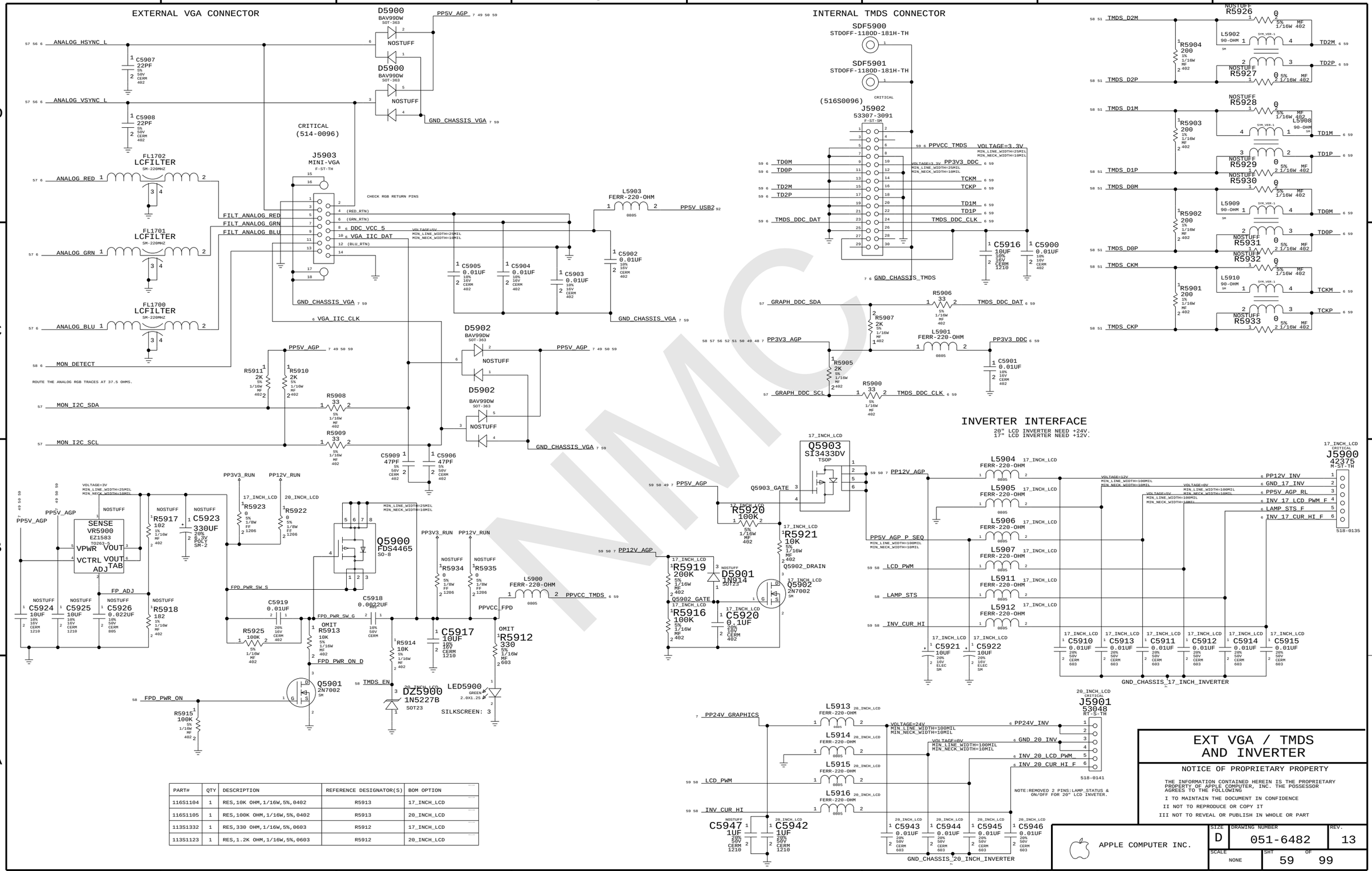
GPU TMDS SWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1003	1	RES,1K OHM,1%,1/16W,0402	R5807	17_INCH_LCD
114S1503	1	RES,1.5K OHM,1%,1/16W,0402	R5807	20_INCH_LCD

DVI AND STRAPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 58 OF 99	

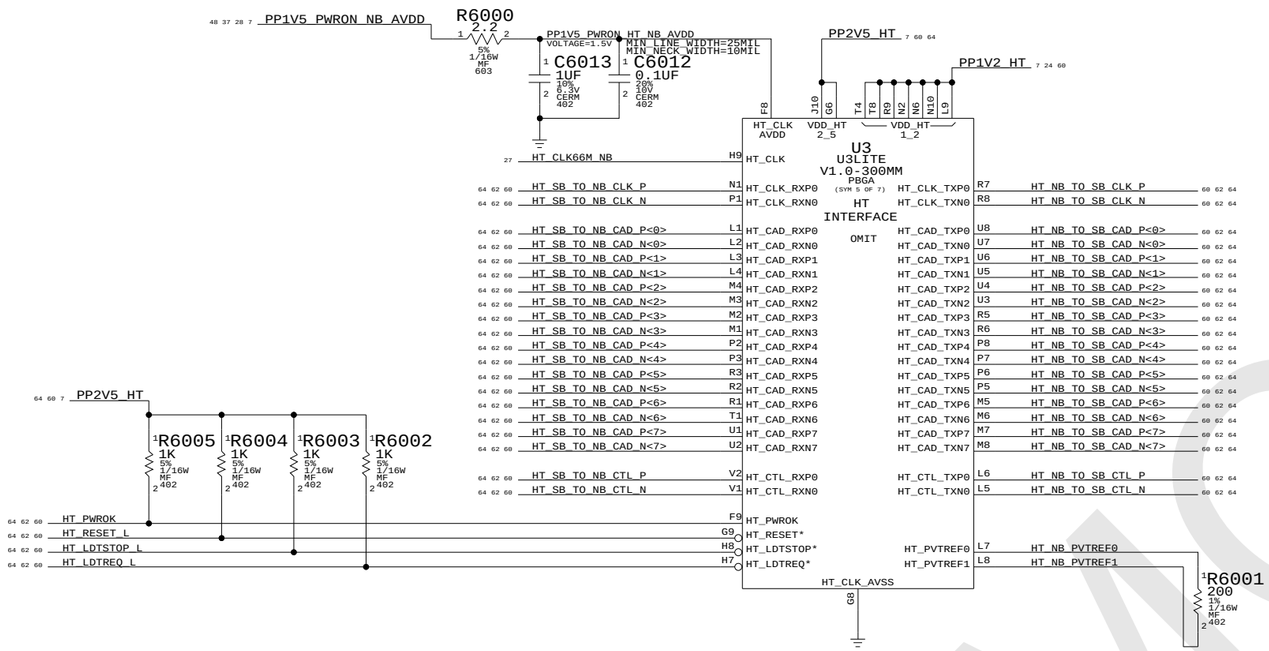


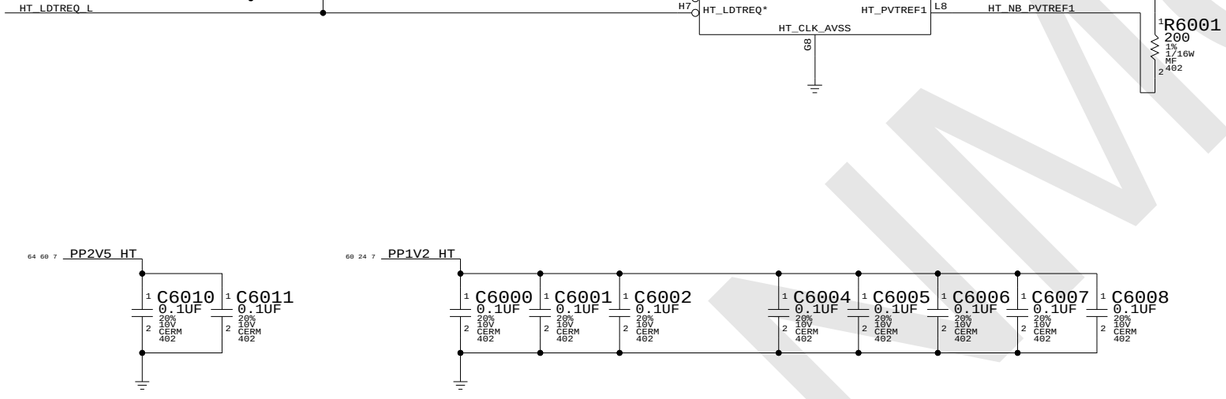
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,10K OHM,1/16W,5%,0402	R5913	17_INCH_LCD
116S1105	1	RES,100K OHM,1/16W,5%,0402	R5913	20_INCH_LCD
113S1332	1	RES,330 OHM,1/16W,5%,0603	R5912	17_INCH_LCD
113S1123	1	RES,1.2K OHM,1/16W,5%,0603	R5912	20_INCH_LCD

EXT VGA / TMDS AND INVERTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 59 OF 99	





	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CLK	146
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CLK	147
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CTL	183
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CTL	182
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD0	151
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD0	150
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD1	152
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD1	153
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD2	154
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD2	155
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD3	156
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD3	157
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD4	158
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD4	159
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD5	160
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD5	161
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD6	162
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD6	163
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD7	164
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_1V2	HT_NB_TO_SB_CAD7	165
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CLK	148
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CLK	149
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CTL	184
HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CTL	185
HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD0	166
HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD0	167
HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD1	168
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD1	169
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD2	170
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD2	171
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD3	172
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD3	173
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD4	174
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD4	175
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD5	176
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD5	177
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD6	178
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD6	179
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD7	180
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_1V2	HT_SB_TO_NB_CAD7	181
HT_PWROK	HT_PWROK	HT_2V5		186
HT_RESET_L	HT_CTL	HT_2V5		187
HT_LDTSTOP_L	HT_CTL	HT_2V5		188
HT_LDTREQ_L	HT_CTL	HT_2V5		189

HT_1V2

5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5

4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERENCE DOES NOT NEED TO BE SPECIFIED
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

MASTER: NEOBORG U3LITE

U3LITE HT

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 60 OF 99	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	15 MIL SPACING	

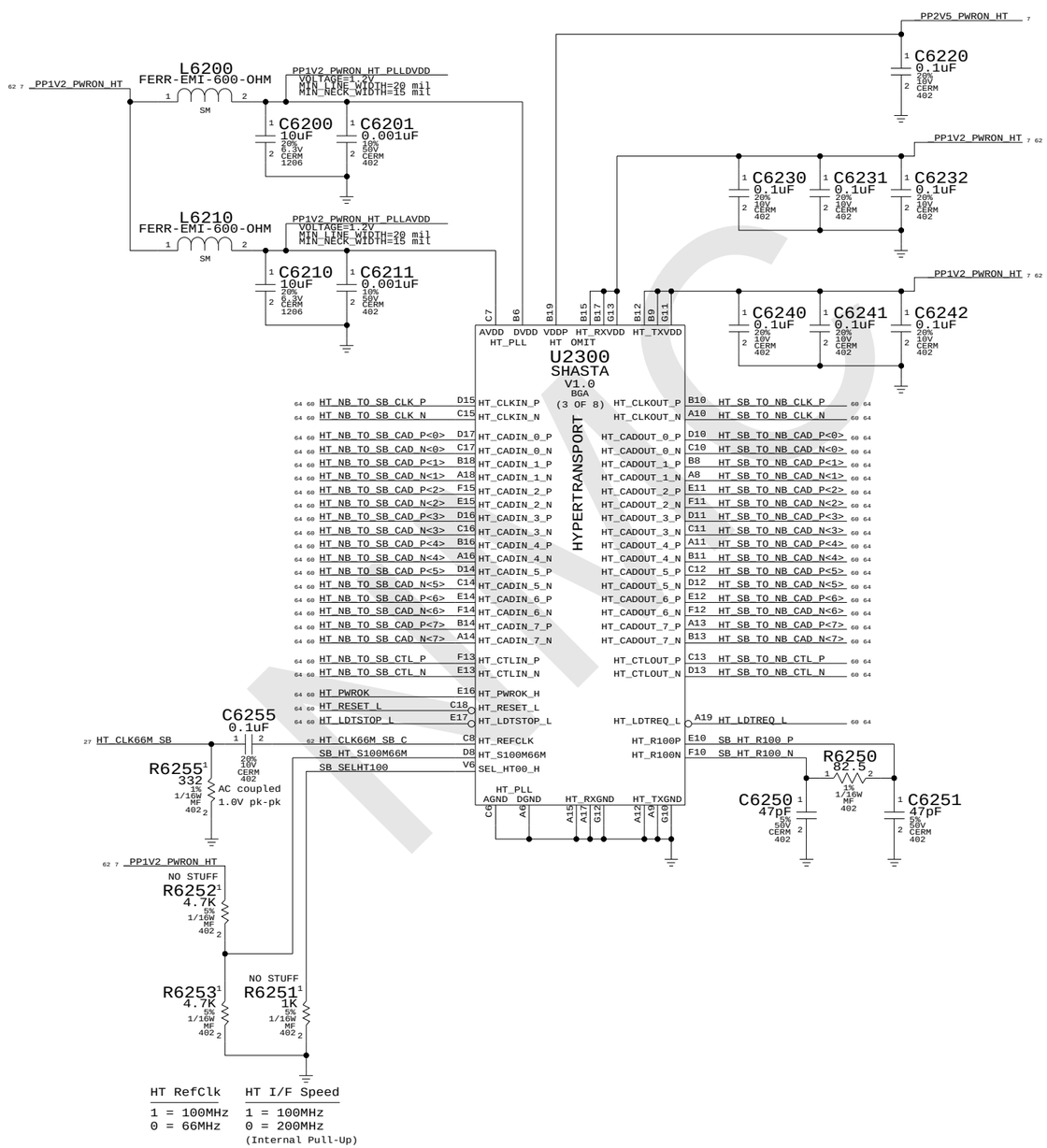
HT_CLK66M_SB_C 62

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_HT
- _PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:31 2003

Master: Fizzy

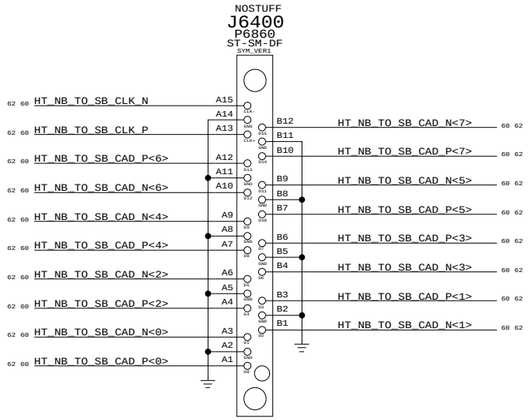
Shasta HyperTransport

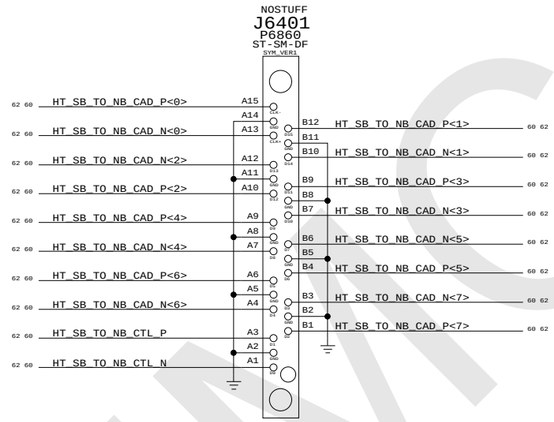
APPLE COMPUTER INC.

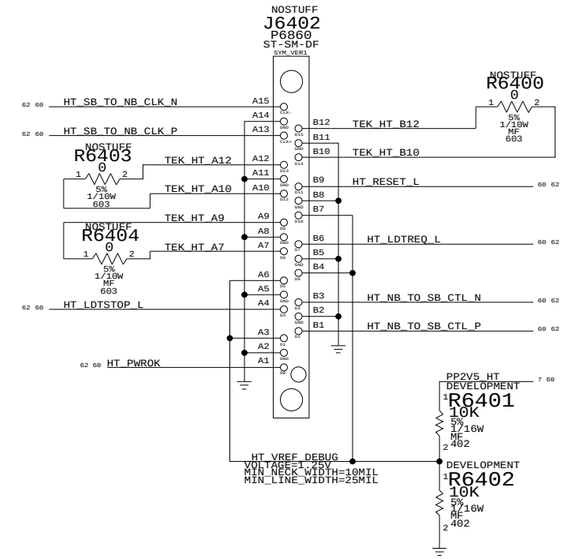
SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 62 OF 99	

SAME CONNECTORS & PINOUT AS

Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2







MASTER: GILA

HT DEBUG CONN

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE: NONE

SHT 64 OF 99

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_AD		PCI_AD<31..28>
PCI_AD27		PCI_AD<27>
PCI_AD		PCI_AD<26..24>
PCI_AD23		PCI_AD<23>
PCI_AD22		PCI_AD<22>
PCI_AD21		PCI_AD<21>
PCI_AD20		PCI_AD<20>
PCI_AD		PCI_AD<19..18>
PCI_AD17		PCI_AD<17>
PCI_AD		PCI_AD<16..0>
PCI		PCI_CBE_L<3..0>
PCI		PCI_PAR
PCI_CTL		PCI_DEVSEL_L
PCI_CTL		PCI_FRAME_L
PCI_CTL		PCI_IRDY_L
PCI_CTL		PCI_TRDY_L
PCI_CTL		PCI_STOP_L

Page Notes

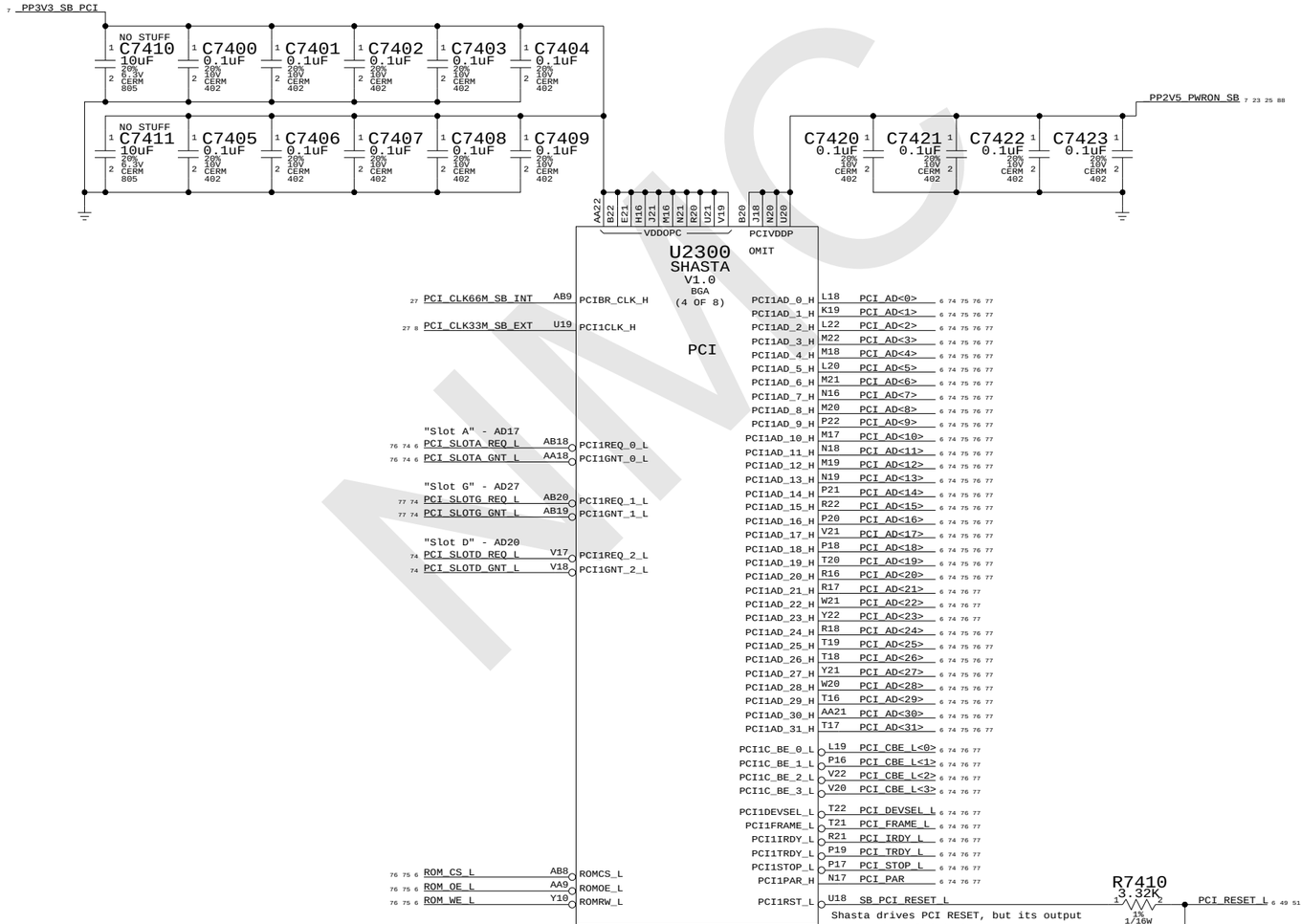
Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_SB_PCI (can be _PP3V3_PCI)
- _PP2V5_PWRON_SB

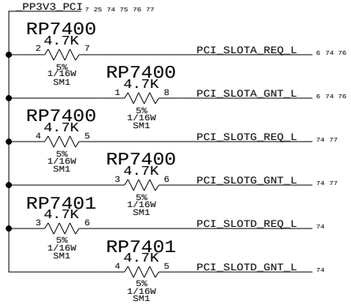
Signal aliases required by this page:
(NONE)

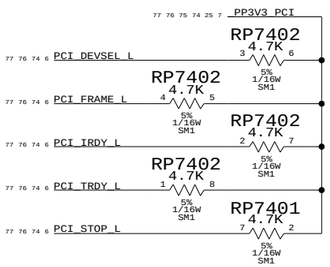
BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)







Master: Link

Shasta PCI Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 74 OF 99	

_DRAWING
TITLE=LINK
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:32 2003

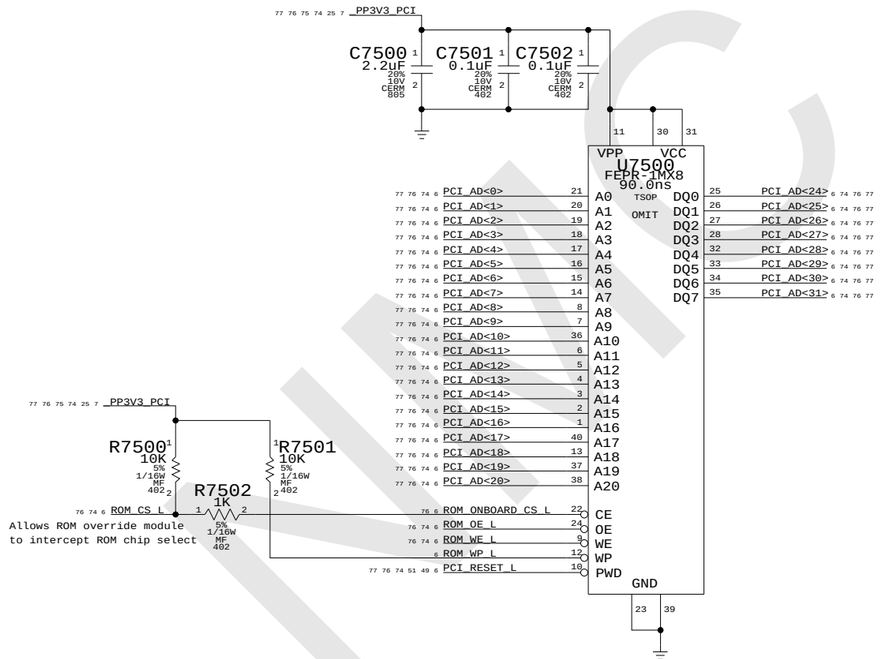
Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



Master: Fizzy

BootROM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE: NONE

SHT 75 OF 99

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:32 2003

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

_PCI_CLK33M_AIRPORT 8 76

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

77 75 74 25 7 _PP3V3_PCI

NO STUFF C7600 1 2 10UF 20% 6.3V CERM 1206
NO STUFF C7601 1 2 10UF 20% 6.3V CERM 1206
C7602 1 2 0.1UF 20% 10V CERM 402
C7603 1 2 0.1UF 20% 10V CERM 402

CRITICAL
J7600
RCPT-CARD-EDGE
F-ST-TH1

SIDE-A		SIDE-B	
77 75 74 51 49 6 PCI_RESET_L	1	2	
6 TP_AIRPORT_RF_DISABLE	3	4	PCI_CLK33M_AIRPORT 8 76
74 6 PCI_SLOTA_REQ_L	5	6	
	7	8	PCI_SLOTA_GNT_L 6 74
77 75 74 6 PCI_AD<31>	9	10	TP_AIRPORT_PME_L 6
	11	12	PCI_SLOTA_INT_L 6 25
77 75 74 6 PCI_AD<29>	13	14	PCI_AD<30> 6 74 75 77
77 75 74 6 PCI_AD<27>	15	16	
77 75 74 6 PCI_AD<25>	17	18	PCI_AD<28> 6 74 75 77
	19	20	PCI_AD<26> 6 74 75 77
77 74 6 PCI_CBE_L<3>	21	22	PCI_AD<24> 6 74 75 77
	23	24	6 PCI_SLOTA_IDSEL
77 74 6 PCI_AD<23>	25	26	
77 74 6 PCI_AD<21>	27	28	PCI_AD<22> 6 74 77
77 75 74 6 PCI_AD<19>	29	30	PCI_AD<20> 6 74 75 77
	31	32	PCI_PAR 6 74 77
77 76 75 74 6 PCI_AD<17>	33	34	PCI_AD<18> 6 74 75 77
	35	36	PCI_AD<16> 6 74 75 77
77 74 6 PCI_CBE_L<2>	37	38	
77 74 6 PCI_IRDY_L	39	40	PCI_FRAME_L 6 74 77
	41	42	PCI_TRDY_L 6 74 77
6 AIRPORT_CLKRUN_L_PD	43	44	PCI_STOP_L 6 74 77
	45	46	PCI_DEVSEL_L 6 74 77
77 74 6 PCI_CBE_L<1>	47	48	
77 75 74 6 PCI_AD<14>	49	50	PCI_AD<15> 6 74 75 77
	51 KEY	52	PCI_AD<13> 6 74 75 77
77 75 74 6 PCI_AD<12>	53	54	PCI_AD<11> 6 74 75 77
77 75 74 6 PCI_AD<10>	55	56	
75 74 6 ROM_WE_L	57	58	PCI_AD<9> 6 74 75 77
77 75 74 6 PCI_AD<8>	59	60	PCI_CBE_L<0> 6 74 77
77 75 74 6 PCI_AD<7>	61	62	ROM_OE_L 6 74 75
	63	64	PCI_AD<6> 6 74 75 77
77 75 74 6 PCI_AD<5>	65	66	
75 6 ROM_ONBOARD_CS_L	67	68	PCI_AD<4> 6 74 75 77
77 75 74 6 PCI_AD<3>	69	70	PCI_AD<2> 6 74 75 77
	71	72	PCI_AD<0> 6 74 75 77
77 75 74 6 PCI_AD<1>	73	74	
75 74 6 ROM_CS_L	75	76 NC	RESERVED FOR USB_DP AND USB_DN
	NC 77	78 NC	
	NC 79	80	
	NC 81	82 NC	
	NC 83	84 NC	
	85	86 NC	
	NC 87	88 NC	
	89	90 NC	RESERVED FOR RADIO_IO
	NC 91	92 NC	
	NC 93	94 NC	
	NC 95	96 NC	
	NC 97	98 NC	
	NC 99	100 NC	

516-0069

R7600 1 2 22 5% 1/16W MF 402
PCI_AD<17> 6 74 75 76 77

DEVELOPMENT
R7610 1 2 0 5% 1/16W MF 402
94 25 6 I2S1_DEV_TO_SB_DTI
SCC_RXDA
I2S1_DEV_TO_SB_DTI_J

DEVELOPMENT
R7611 1 2 0 5% 1/16W MF 402
94 25 6 I2S1_SB_TO_DEV_DTO
SCC_TXDA
I2S1_SB_TO_DEV_DTO_J

R7601 1 2 10K 5% 1/16W MF 402

PLACE R7610 AND R7611 CLOSE TO J9400

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:33 2003

AirPort Extreme

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 76 OF 99	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	

PCI_CLK33M_USB2 8 77

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

7 _PPVIO_PCI_USB2

C7703 0.1uF 20% 10V CERM 402

VDD_PCI

CRITICAL
U7700
NEC_uPD720101_USB2
FBGA

76 75 74 6 PCI_AD<0>	M5	AD0	
76 75 74 6 PCI_AD<1>	P5	AD1	
76 75 74 6 PCI_AD<2>	N5	AD2	
76 75 74 6 PCI_AD<3>	P4	AD3	
76 75 74 6 PCI_AD<4>	N4	AD4	
76 75 74 6 PCI_AD<5>	M3	AD5	
76 75 74 6 PCI_AD<6>	N3	AD6	
76 75 74 6 PCI_AD<7>	M1	AD7	
76 75 74 6 PCI_AD<8>	L2	AD8	
76 75 74 6 PCI_AD<9>	L1	AD9	
76 75 74 6 PCI_AD<10>	K2	AD10	
76 75 74 6 PCI_AD<11>	L3	AD11	
76 75 74 6 PCI_AD<12>	K1	AD12	
76 75 74 6 PCI_AD<13>	K3	AD13	
76 75 74 6 PCI_AD<14>	J2	AD14	
76 75 74 6 PCI_AD<15>	J1	AD15	
76 75 74 6 PCI_AD<16>	F2	AD16	
76 75 74 6 PCI_AD<17>	E3	AD17	
76 75 74 6 PCI_AD<18>	E1	AD18	
76 75 74 6 PCI_AD<19>	D3	AD19	
76 75 74 6 PCI_AD<20>	D1	AD20	
76 74 6 PCI_AD<21>	D2	AD21	
76 74 6 PCI_AD<22>	C2	AD22	
76 74 6 PCI_AD<23>	C1	AD23	
76 75 74 6 PCI_AD<24>	B4	AD24	
76 75 74 6 PCI_AD<25>	A4	AD25	
76 75 74 6 PCI_AD<26>	B5	AD26	
76 75 74 6 PCI_AD<27>	C4	AD27	
76 75 74 6 PCI_AD<28>	A5	AD28	
76 75 74 6 PCI_AD<29>	C5	AD29	
76 75 74 6 PCI_AD<30>	B6	AD30	
76 75 74 6 PCI_AD<31>	A6	AD31	
76 74 6 PCI_CBE_L<0>	M2	CBE0	
76 74 6 PCI_CBE_L<1>	J3	CBE1	
76 74 6 PCI_CBE_L<2>	F1	CBE2	
76 74 6 PCI_CBE_L<3>	C3	CBE3	
76 74 6 PCI_PAR	J4	PAR	
76 74 6 PCI_FRAME_L	F3	FRAME	
76 74 6 PCI_IRDY_L	F4	IRDY	
76 74 6 PCI_TRDY_L	G1	TRDY	
76 74 6 PCI_STOP_L	G3	STOP	
PCI_SLOTG_IDSEL	B3	IDSEL	
76 74 6 PCI_DEVSEL_L	G2	DEVSEL	
74 PCI_SLOTG_REQ_L	C6	REQ	
74 PCI_SLOTG_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR OD	
NEC_INTA_L	C7	INTA OD	
NEC_INTB_L	B7	INTB OD	
NEC_INTC_L	A7	INTC OD	
77 8 _PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST(CHIP RESET)	
NEC_CRUN_L_PD	N6	CRUN	
NEC_PME_L	D9	PME OD	
NEC_VCCRST_L	C9	VCCRST(PCI RESET)	
6 TP_NEC_SMI_L	L6	SMI OD	
NEC_LEGC_PD	L7	LEGC	
IPD NTEST1	M8	TP_NEC_NTEST1	6
IPD SMC	M7	TP_NEC_SMC	6
IPD TEB	N7	TP_NEC_TEB	6
IPD AMC	P7	TP_NEC_AMC	6
IPD TEST	L8	TP_NEC_TEST	6
NANDTEST	M10	TP_NEC_NANDTEST	6
SRCLK	M9	TP_NEC_SRCLK	6
SRDTA	N9	TP_NEC_SRDATA	6
IPD SRMOD	P9	TP_NEC_SRMOD	6

R7714 22 5% 1/16W MF 402

76 75 74 25 7 PP3V3_PCI

R7716 10K 5% 1/16W MF 402

R7713 10K 5% 1/16W MF 402

25 PCI_SLOTG_INT_L — RP7703 47 5% 1/16W SM1

RP7703 47 5% 1/16W SM1

RP7703 47 5% 1/16W SM1

87 74 25 24 8 SYS_WARM_RESET_L — RP7702 47 5% 1/16W SM1

25 13 SYS_PME_L — RP7702 47 5% 1/16W SM1

76 75 74 51 49 6 PCI_RESET_L — RP7702 47 5% 1/16W SM1

RP7702 & RP7703 required to facilitate NAND-tree testing

R7715 4.7K 5% 1/10W MF 402

RP7703 47 5% 1/16W SM1

Master: Fizzy

USB 2.0 PCI Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 77 OF 99	

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:33 2003

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_P1_C
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_N1_C
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_P1
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_N1
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_P2_C
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_N2_C
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_P2
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_N2
UATA_DD			UATA_DD<15..8>
UATA_DD7			UATA_DD<7>
UATA_DD			UATA_DD<6..0>
UATA_HOST			UATA_DA<2..0>
UATA_HOST			UATA_CS0_L
UATA_HOST			UATA_CS1_L
UATA_HOST			UATA_HSTROBE
UATA_HOST			UATA_STOP
UATA_HOST_R			UATA_DMACK_L
UATA_HOST_R			UATA_RESET_L
UATA_DEV_R_C			UATA_DSTROBE
UATA_DEV_R			UATA_DMARQ
UATA_DEV_R			UATA_INTRQ

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

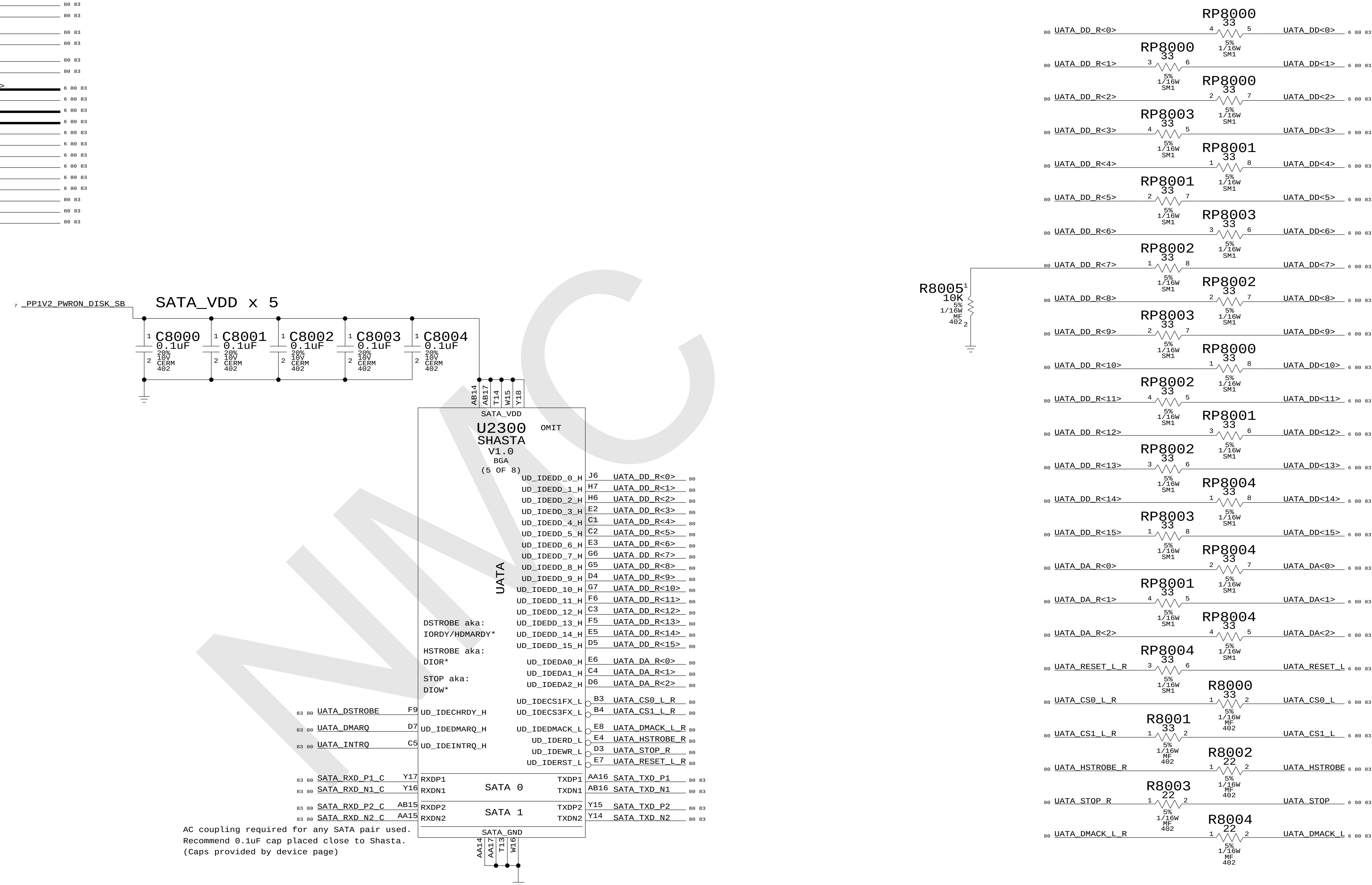
BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line: 15 mils
Length Tolerance: 50 mils
Primary Max Sep: 10 mils outer
Primary Max Sep: 9 mils inner
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

UATA Termination



Master: Link

Shasta Disk

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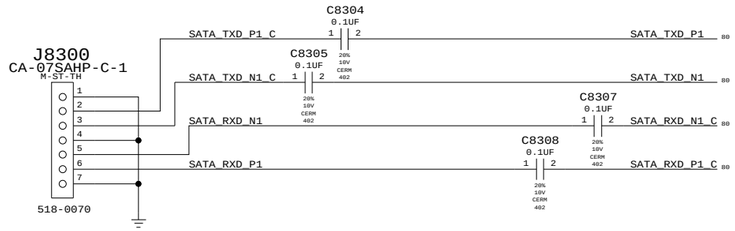
APPLE COMPUTER INC.

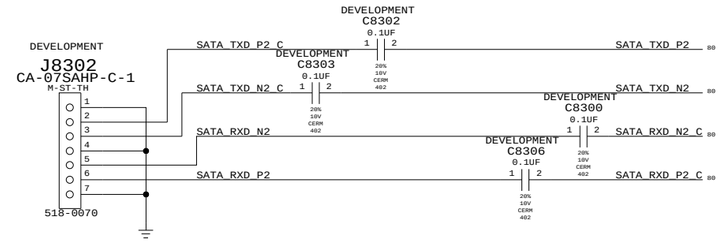
SIZE D | DRAWING NUMBER 051-6482 | REV. 13
SCALE NONE | SHT 80 OF 99

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:34 2003

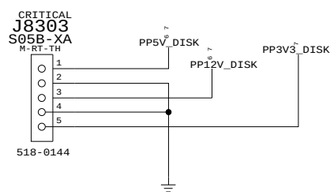
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
UATA_DD<15..8>	UATA_DD		
UATA_DD<7>	UATA_DD7		
UATA_DD<6..0>	UATA_DD		
UATA_DA<2..0>	UATA_HOST		
UATA_CS0_L	UATA_HOST		
UATA_CS1_L	UATA_HOST		
UATA_HSTROBE	UATA_HOST		
UATA_STOP	UATA_HOST		
UATA_DMACK_L	UATA_HOST_R		
UATA_RESET_L	UATA_HOST_R		
UATA_DSTROBE	UATA_DEV_R_C		
UATA_DMARQ	UATA_DEV_R		
UATA_INTRQ	UATA_DEV_R		

SATA CONNECTORS

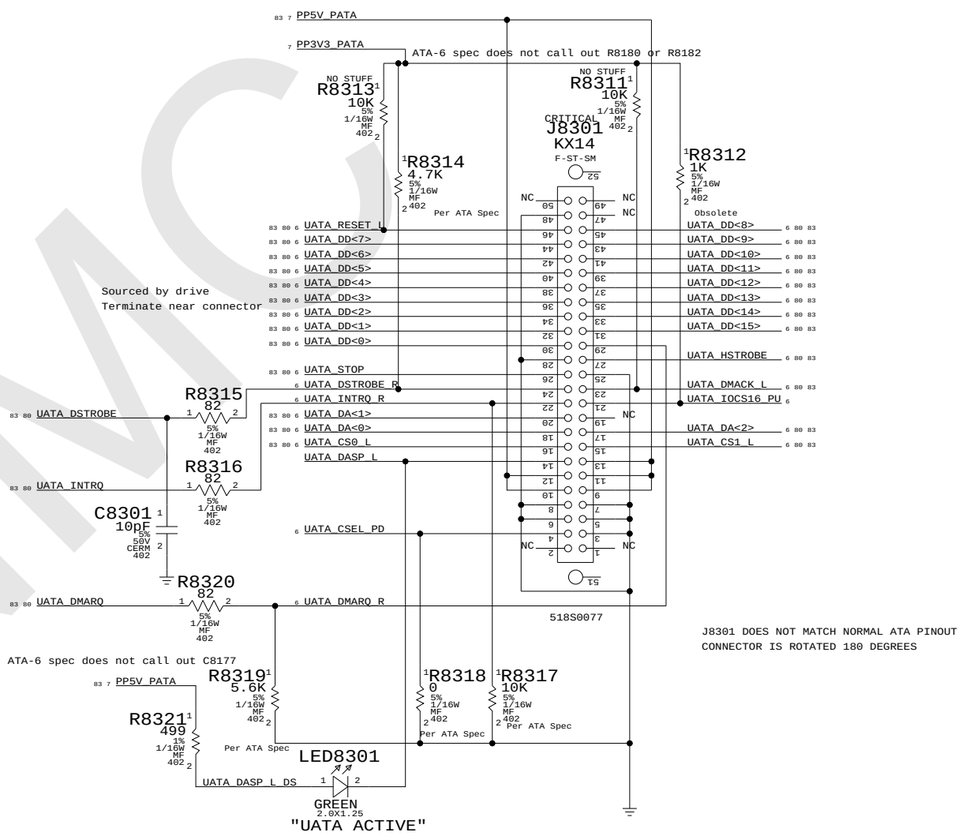




HD POWER



PATA CONNECTOR



DISK CONNECTORS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT	OF
NONE	83	99

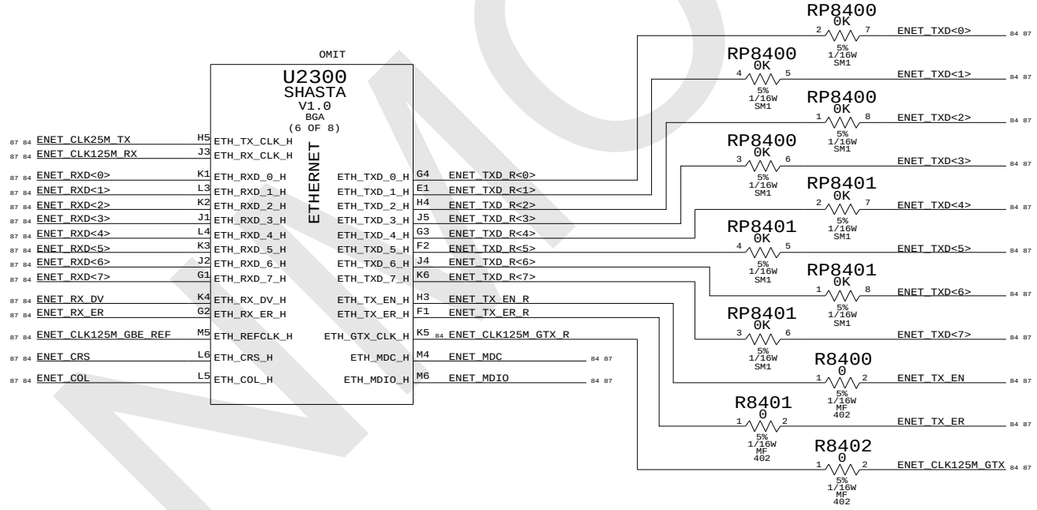
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_RX_CLK	10 MIL		ENET_CLK25M_TX 84 87
ENET_RX_CLK	10 MIL		ENET_CLK125M_RX 84 87
ENET_GBE_REF	15 MIL SPACING		ENET_CLK125M_GBE_REF 84 87
ENET_TX_CLK	15 MIL SPACING		ENET_CLK125M_GTX 84 87
	15 MIL SPACING		ENET_CLK125M_GTX_R 84
ENET_RX			ENET_RXD<7..0> 84 87
ENET_RX_CTL			ENET_RX_DV 84 87
ENET_RX_CTL			ENET_RX_ER 84 87
ENET_TX			ENET_TXD<7..0> 84 87
ENET_TX_CTL			ENET_TX_EN 84 87
ENET_TX_CTL			ENET_TX_ER 84 87
ENET_RX_CTL			ENET_CRS 84 87
ENET_RX_CTL			ENET_COL 84 87
ENET_MDC			ENET_MDC 84 87
ENET_MDIO			ENET_MDIO 84 87

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:35 2003

Master: Link

Shasta Ethernet

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 84 OF 99	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_MDI_TX	ENET	ENET_MDI_TD	ENET_TDP 87
ENET_MDI_TX	ENET	ENET_MDI_TD	ENET_TDN 87
ENET_MDI_RX	ENET	ENET_MDI_RD	ENET_RDP 87
ENET_MDI_RX	ENET	ENET_MDI_RD	ENET_RDN 87
ENET_XTAL	15 MIL SPACING		ENET_CLK25M_XIN 87
	15 MIL SPACING		ENET_CLK25M_XOUT 87

ETHERNET ROUTING PRIORITY:
1. DECOUPLING CAPS
2. TX TERMINATION - LOCATE NEAR PHY
3. RX TERMINATION - LOCATE NEAR PHY

ROUTE TD OVER 2.5V PLANE (BOTTOM LAYER) ONLY
ROUTE RD OVER GROUND PLANE (TOP LAYER) ONLY

ALL DIFFERENTIAL SIGNALS SHOULD BE CLOSE, PARALLEL, MATCHED LENGTHS, WITH MINIMUM VIA COUNT, AND SHORT IF POSSIBLE

CLEAR OUT ALL PLANES BETWEEN MIDDLE OF TRANSFORMER AND CONNECTOR

PP2V5_ENET
VOLTAGE=2.5V
MIN_LINE_WIDTH=50MIL
MIN_NECK_WIDTH=10MIL
C8703 0.1UF 20% 10V CERM 402
C8704 0.01UF 20% 16V CERM 402
C8702 0.1UF 20% 10V CERM 402
C8705 0.01UF 20% 16V CERM 402
C8712 2.2UF 20% 10V CERM 805

87 7 PP3V3_PWRON_ENET

ENET_DVDD
VOLTAGE=2.5V
MIN_LINE_WIDTH=25MIL
MIN_NECK_WIDTH=10MIL
C8711 2.2UF 20% 10V CERM 805
C8716 0.1UF 20% 10V CERM 402
C8708 0.01UF 20% 16V CERM 402
C8715 0.1UF 20% 10V CERM 402
C8709 0.01UF 20% 16V CERM 402

NOTE: PLACE R3128, R3100, RP 3101 CLOSE TO PHY

U8700
FLAS-1
TRANSC_BCM5221
CRITICAL

REGVDD 3
REGAVDD 20
DVDD1 2
DVDD2 55
AVDD1 27
AVDD2 28
OVDD1 1
OVDD2 46
REFCLK 4 (NC)
BIASVDD 22
OVDD/NC 8

(PLACE R3126, R3127 R3117, R3118 CLOSE TO PHY)
C8710 0.01UF 20% 16V CERM 402
R8701 49.9 1% 1/10W MF 402
R8700 49.9 1% 1/10W MF 402

TD+ 31
TD- 30
RD+ 26
RD- 25
SD+ 21
SD- 19 NC

PP3V3_PWRON_ENET 87
R8712 10K 5% 1/16W MF 402
R8713 10K 5% 1/16W MF 402
R8703 49.9 1% 1/10W MF 402
R8702 49.9 1% 1/10W MF 402

FDX 39 ENET_5221_FDX 87
F100/JTAG_TCK 37 TP_ENET_TCK 6
ANEN/JTAG_TRST 38 ANEN
TESTEN 15 ENET_5221_TESTEN 87
MII_EN 18 MII_EN
LOW_PWR 16 ENET_5221_LOW_PWR 87

ENERGY_DET 17 ENET_ENERGYDET 25
RDAC 23

LNKLED/JTAG_TDI* 35 ENET_TDI 87
SPDLED/JTAG_TMS* 36 ENET_TMS 87
XMTLED* 34 XMIT_LED 87
RCVLED/JTAG_TDO* 33 TP_ENET_TDO

R8704 10K 5% 1/16W MF 402
R8704 PULLDOWN ENABLES AUTO-MDI/MDIX

OGND1 40
OGND2 45
OGND3/JTAG_EN 64
DGND1 54
DGND2 63
AGND1 29
AGND2 32
PLLGND 7
BIASGND 24

ENET_RDAC_PD
R8705 1.27K 1% 1/16W MF 402

RP8702 10K 5%
87 ENET_5221_FDX
87 ENET_5221_TESTEN
87 ENET_5221_LOW_PWR
87 OGND3_JTAG_EN

C8722 0.1UF 20% 10V CERM 402

(514-0083)
CRITICAL
J8700
RJ45
MJ-R0018
F-ST-TH

PRIMARY
SYM_VER-3
ENET_TDP 1
ENET_TDN 3
ENET_RDP 4
ENET_RDN 6
9 10 11 12
GND_CHASSIS_RJ45
RJ45 CHIP SIDE

1CT:1CT TX-SIDE
1CT:1CT RX-SIDE
SECONDARY
J1 J2 J3 J4 J5 J6 J7 J8
RJ45 CABLE SIDE
75 OHM 75 OHM 75 OHM 75 OHM
SHIELD 1000PF, 2000V

C8706 0.01UF 20% 16V CERM 402
C8707 0.01UF 20% 16V CERM 402
C8714 0.01UF 20% 16V CERM 402
C8721 0.1UF 20% 10V CERM 402

I237 MAKE_BASE=TRUE
84 ENET_CLK25M_TX
CLK_ENET_LINK_TX NET_SPACING_TYPE=10 MIL
R8706 33 5% 1/16W MF 402
CLKENET_PHY_TX NET_SPACING_TYPE=10 MIL 53
TXC

84 ENET_TXD<0> 57 TXD0
84 ENET_TXD<1> 58 TXD1
84 ENET_TXD<2> 59 TXD2
84 ENET_TXD<3> 60 TXD3

I238 MAKE_BASE=TRUE
84 ENET_CLK125M_RX
CLK_ENET_LINK_RX NET_SPACING_TYPE=10 MIL
84 ENET_TX_EN 56 TXEN
84 ENET_TX_ER 52 TXER

R8707 33 5% 1/16W MF 402
CLKENET_PHY_RX NET_SPACING_TYPE=10 MIL 50 RXC

RP8700 33 5% SM1
84 ENET_RXD<0> 1 8 ENET_PHY_RXD<0> 48 RXD0
84 ENET_RXD<1> 2 7 ENET_PHY_RXD<1> 47 RXD1
84 ENET_RXD<2> 3 6 ENET_PHY_RXD<2> 44 RXD2
84 ENET_RXD<3> 4 5 ENET_PHY_RXD<3> 43 RXD3

R8709 33 5% 1/16W MF 402
84 ENET_RX_DV
ENET_PHY_RX_DV 49 RXDV
ENET_PHY_RX_ER 51 RXER

RP8701 33 1/16W 5%
84 ENET_RX_ER
ENET_PHY_CRS 62 CRS
84 ENET_CRS
ENET_PHY_COL 61 COL
84 ENET_COL
ETHPHYRESET_L 8 RESET*
84 ENET_MDC 42 MDC
41 MDIO
NET_SPACING_TYPE=10 MIL

D8700 1N914 SOT23
77 74 25 24 8 SYS_WARM_RESET_L

SHASTA SIGNAL IS ACTIVE HIGH
90 ENETFW_RESET_L
R8711 0 5% 1/16W MF 402
Q8700 2N7002 SM NOSTUFF
R8719 1K 5% 1/16W MF 402
PP3V3_PWRON_ENET 87
R8708 1.5K 1% 1/16W MF 603
C8723 1UF 20% 10V CERM 603
(PLACE Y8700 CRYSTAL CLOSE TO PHY)
ENETFW_RESET 25

84 ENET_MDIO 6 XTALI
5 XTALO
NC 10 PHYAD0
NC 11 PHYAD1
NC 12 PHYAD2
NC 13 PHYAD3
NC 14 PHYAD4
PHY ADDRESS 00000

ADD DUAL LAYOUT SUPPORT FOR ALTERNATE CRYSTAL
87 ENET_CLK25M_XIN
CRITICAL
Y8700 25.0000M 8X4.5MM-SM
87 ENET_CLK25M_XOUT
C8701 27PF 5% 50V CERM 603
C8700 27PF 5% 50V CERM 603

87 OGND3_JTAG_EN

NOTE: LINK SUPPORT FOR GIGABIT ETHERNET PULLED DOWN OR ALIASED TO TEST POINTS HERE.

84 ENET_RXD<4> I228 ENET_RXD_PD MAKE_BASE=TRUE
84 ENET_RXD<5> I229
84 ENET_RXD<6> I230
84 ENET_RXD<7> I231
R8799 10K 1% 1/16W MF 402

84 ENET_CLK125M_GBE_REF
R8798 10K 1% 1/16W MF 402

84 ENET_TXD<4> I232 TP_ENET_TXD<4> 6 MAKE_BASE=TRUE
84 ENET_TXD<5> I233 TP_ENET_TXD<5> 6 MAKE_BASE=TRUE
84 ENET_TXD<6> I234 TP_ENET_TXD<6> 6 MAKE_BASE=TRUE
84 ENET_TXD<7> I235 TP_ENET_TXD<7> 6 MAKE_BASE=TRUE
84 ENET_CLK125M_GTX I236 TP_ENET_CLK125M_GTX 6 MAKE_BASE=TRUE

87 PP3V3_PWRON_ENET
C8720 4.7UF 20% 10V CERM 1206
C8719 0.1UF 20% 10V CERM 402
C8718 0.1UF 20% 10V CERM 402
C8717 0.1UF 20% 10V CERM 402
C8713 10UF 20% 6.3V CERM 1206
KEEP ALL CAPS CLOSE TO TRANSCEIVER ON THIS PAGE

87 PP3V3_PWRON_ENET
DEVELOPMENT
R8718 4.7K 5% 1/16W MF 603
R8717 330 5% 1/16W MF 603
DS3P1 DEVELOPMENT LED8702 GREEN 2.0X1.25 10/100
R8716 330 5% 1/16W MF 603
DS1P1 DEVELOPMENT LED8701 GREEN 2.0X1.25 XMIT
R8715 330 5% 1/16W MF 603
DS2P1 DEVELOPMENT LED8700 GREEN 2.0X1.25 LINK
R8714 4.7K 5% 1/16W MF 603
87 ENET_TMS
87 XMIT_LED
87 ENET_TDI

ETHERNET PHY

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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6482
REV. 13
SCALE NONE
SHT 87 OF 99
DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
FW			FW_DATA<7..0>	88 90
FW			FW_CTL<1..0>	88 90
FW_LPS			FW_LPS	88 90
FW_LREQ			FW_LREQ	88 90
FW_PINT			FW_PINT	88 90
FW_LCLK	15_MIL_SPACING		FW_CLK98M_LCLK	88 90
FW_PCLK	15_MIL_SPACING		FW_CLK98M_PCLK	88 90
	15_MIL_SPACING		FW_CLK98M_LCLK_R	88

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

74 25 23 7 _PP2V5_PWRON_SB

C8800 0.1uF 20% 10V CERM 402
C8801 0.1uF 20% 10V CERM 402
C8802 0.1uF 20% 10V CERM 402

N5 J7 A4 FWVDDP

U2300 SHASTA V1.0 BGA (7 OF 8) OMIT

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	88 90
PHY_DATA_1_H	P5	FW_DATA<1>	88 90
PHY_DATA_2_H	N1	FW_DATA<2>	88 90
PHY_DATA_3_H	M7	FW_DATA<3>	88 90
PHY_DATA_4_H	N6	FW_DATA<4>	88 90
PHY_DATA_5_H	L1	FW_DATA<5>	88 90
PHY_DATA_6_H	M3	FW_DATA<6>	88 90
PHY_DATA_7_H	L2	FW_DATA<7>	88 90
PHY_CTL_0_H	N2	FW_CTL<0>	88 90
PHY_CTL_1_H	N3	FW_CTL<1>	88 90
PHY_LPS_H	P6	FW_LPS	88 90
PHY_LREQ_H	P1	FW_LREQ	88 90
PHY_LCLK_H	R1	FW_CLK98M_LCLK_R	88
PHY_LINKON_L	N7	FW_LINKON	90
PHY_SCLK_H	P2	FW_CLK98M_PCLK	90 88
PHY_PINT_L	P3	FW_PINT	90 88

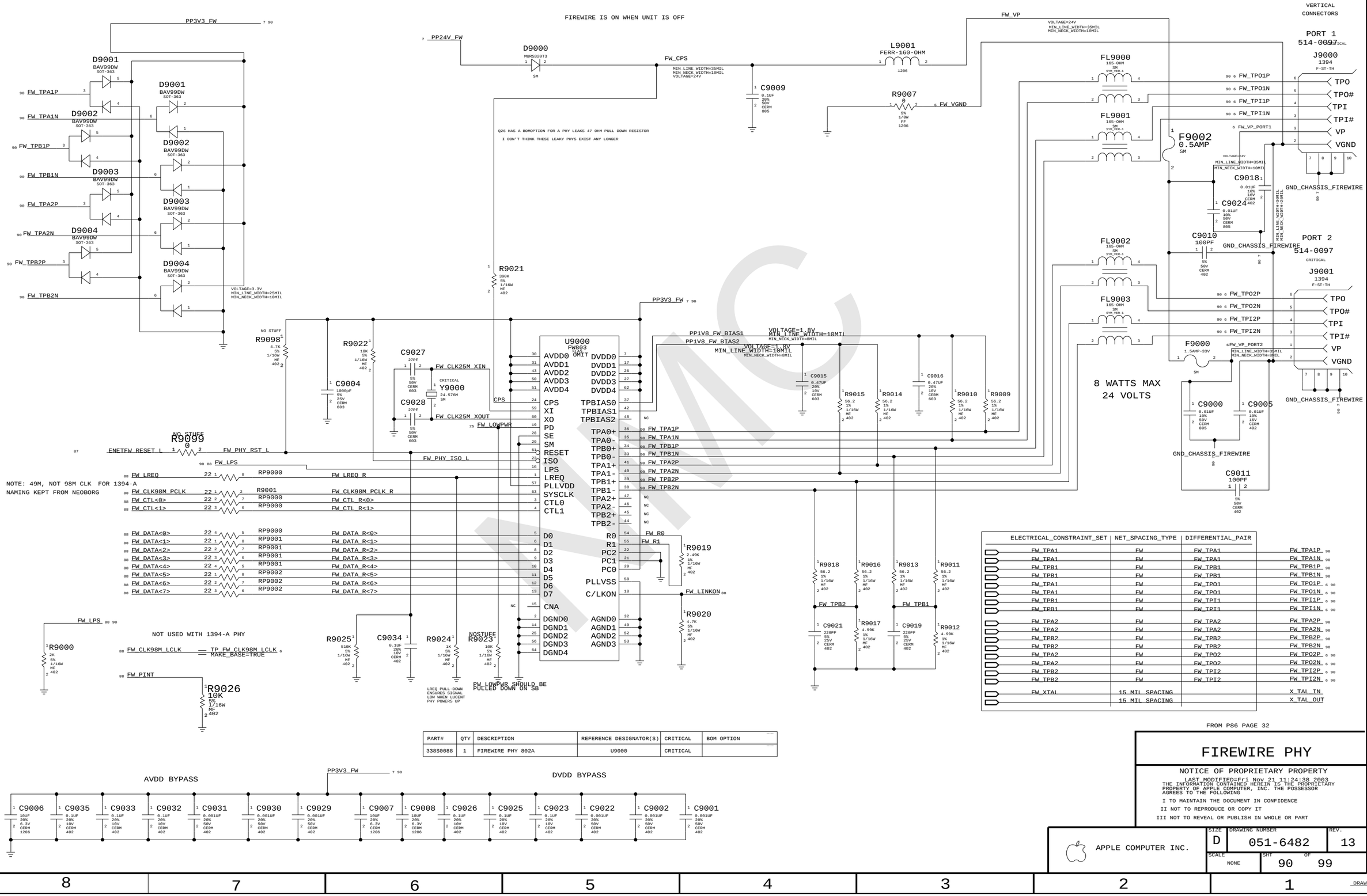
R8800 22 5% 1/16W MF 402
1 2 FW_CLK98M_LCLK 88 90

Shasta FireWire

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 88 OF 99	

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:36 2003



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0088	1	FIREWIRE PHY 802A	U9000	CRITICAL	

FIREWIRE PHY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 90 OF 99	

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2_0	USB2_P<0>
USB2_0	USB2	USB2_0	USB2_N<0>
USB2_1	USB2	USB2_1	USB2_P<1>
USB2_1	USB2	USB2_1	USB2_N<1>
USB2_2	USB2	USB2_2	USB2_P<2>
USB2_2	USB2	USB2_2	USB2_N<2>
USB2_3	USB2	USB2_3	USB2_P<3>
USB2_3	USB2	USB2_3	USB2_N<3>
USB2_4	USB2	USB2_4	USB2_P<4>
USB2_4	USB2	USB2_4	USB2_N<4>
USB2_NEC_XTAL	15_MIL_SPACING		NEC_CLK30M_XT1
	15_MIL_SPACING		NEC_CLK30M_XT2
	15_MIL_SPACING		NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300 SHASTA V1.0 BGA (8 OF 8) OMIT

NC0 P7 TP_SB_NC_P7
NC1 P8 TP_SB_NC_P8
NC2 R3 TP_SB_NC_R3
NC3 R4 TP_SB_NC_R4
NC4 R5 TP_SB_NC_R5
NC5 R6 TP_SB_NC_R6
NC6 R7 TP_SB_NC_R7
NC7 R8 TP_SB_NC_R8
NC8 T1 TP_SB_NC_T1
NC9 T2 TP_SB_NC_T2
NC10 T3 TP_SB_NC_T3
NC11 T4 TP_SB_NC_T4
NC12 T5 TP_SB_NC_T5
NC13 T6 TP_SB_NC_T6
NC14 T7 TP_SB_NC_T7
NC15 T8 TP_SB_NC_T8
NC16 U1 TP_SB_NC_U1
NC17 U2 TP_SB_NC_U2
NC18 U3 TP_SB_NC_U3
NC19 U4 TP_SB_NC_U4
NC20 U5 TP_SB_NC_U5
NC21 U6 TP_SB_NC_V1
NC22 V1 TP_SB_NC_V2
NC23 V2 TP_SB_NC_V3
NC24 V3 TP_SB_NC_V4
NC25 V4 TP_SB_NC_W1
NC26 W1 TP_SB_NC_W3
NC27 W3 TP_SB_NC_Y1
NC28 Y1 TP_SB_NC_Y3
NC29 Y3

91 7 _PP3V3_PWRON_USB
L9135 FERR-EMI-100-OHM SM
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=10 mil
R9135 4.7 5% 1/16W MF 603
C9135 10uF 20% 6.3V CERM 805
C9136 0.1uF 20% 10V CERM 402
C9137 0.1uF 20% 10V CERM 402

C9120 10uF 20% 6.3V CERM 805
C9121 C9122 C9123 C9124 C9125 C9126 C9127 C9128 C9129 C9130 0.1uF 20% 10V CERM 402

P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 → VDD
M10 N12 → AVDD

CRITICAL
U7700 NEC_uPD720101_USB2 FBGA

R9100 R9101 R9102 R9103 R9104 R9105 R9106 R9107 R9108 R9109 36 1% 1/16W MF 402

RSDM1 M14 USB_NEC_N<0>
DM1 M13 (USB2_N<0>) — USB2_N<0> 91 92
DP1 L14 (USB2_P<0>) — USB2_P<0> 91 92
RSDP1 K13 USB_NEC_P<0>

RSDM2 K14 USB_NEC_N<1>
DM2 K12 (USB2_N<1>) — USB2_N<1> 91 92
DP2 J14 (USB2_P<1>) — USB2_P<1> 91 92
RSDP2 J12 USB_NEC_P<1>

RSDM3 H11 USB_NEC_N<2>
DM3 G11 (USB2_N<2>) — USB2_N<2> 91 92
DP3 G13 (USB2_P<2>) — USB2_P<2> 91 92
RSDP3 G14 USB_NEC_P<2>

RSDM4 F12 USB_NEC_N<3>
DM4 F14 (USB2_N<3>) — USB2_N<3> 91 94
DP4 E12 (USB2_P<3>) — USB2_P<3> 91 94
RSDP4 E14 USB_NEC_P<3>

RSDM5 E13 USB_NEC_N<4>
DM5 D14 (USB2_N<4>) — USB2_N<4> 91 92
DP5 C13 (USB2_P<4>) — USB2_P<4> 91 92
RSDP5 C14 USB_NEC_P<4>

91 7 _PP3V3_PWRON_USB
R9110 10K 5% 1/16W MF 402
RP9110 10K 5% 1/16W SM1

92 USB2_OC<0> (USB2_OC<0>) B12 OCI1
92 USB2_OC<1> (USB2_OC<1>) B11 OCI2
92 USB2_OC<2> (USB2_OC<2>) B10 OCI3
94 USB2_OC<3> (USB2_OC<3>) A10 OCI4
92 USB2_OC<4> (USB2_OC<4>) B9 OCI5

92 USB2_PWREN<0> C12 PPON1
92 USB2_PWREN<1> A11 PPON2
92 USB2_PWREN<2> C11 PPON3
92 USB2_PWREN<3> C10 PPON4
92 USB2_PWREN<4> A9 PPON5

91 7 _PP3V3_PWRON_USB
R9140 1.5K 5% 1/16W MF 402
R9141 1.5K 5% 1/16W MF 402
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

91 NEC_CLK30M_XT1 L9 XT1/SCLK
91 NEC_CLK30M_XT2_R P8 XT2
R9145 100 5% 1/16W MF 402
CRITICAL
Y9145 30.0000M 8X4.5MM-SM
NEC_CLK30M_XT2 91
C9145 27pF 5% 50V CERM 402
C9146 27pF 5% 50V CERM 402
Y9145 LOAD CAPACITANCE IS 16pF

VSS
B1 N2 P10 M3 H5 B5 A2 D2 M2 N4 B13 M11 L12 H12 D12 G4 J11 F11 D8
R9139 0 5% 1/16W MF 603
AVSS AVSS(R)
P1 M1 N1
Tie to GND at ball N11
GND_NEC_AVSS_R VOLTAGE=0V MIN_LINE_WIDTH=20 mil MIN_NECK_WIDTH=10 mil

RREF P11 NEC_RREF_PD
R9138 9.09K 1% 1/16W MF 402

DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:24:39 2003

Master: Fizzy

USB Host Interfaces

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 91 OF 99	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2_PORT1_P_F
	USB2	USB2_PORT1_F	USB2_PORT1_N_F
	USB2	USB2_PORT2_F	USB2_PORT2_P_F
	USB2	USB2_PORT2_F	USB2_PORT2_N_F
	USB2	USB2_PORT3_F	USB2_PORT3_P_F
	USB2	USB2_PORT3_F	USB2_PORT3_N_F

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

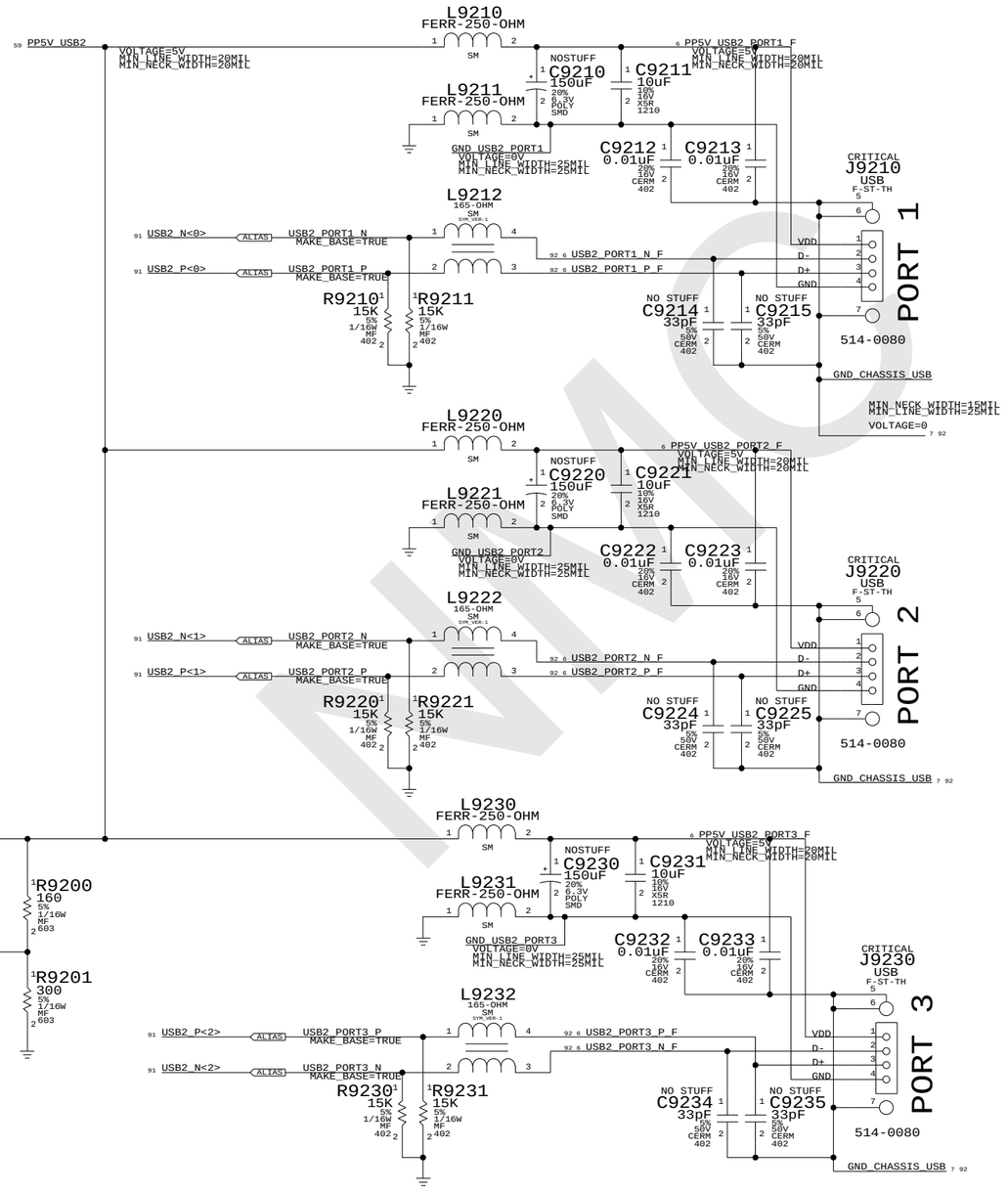
NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

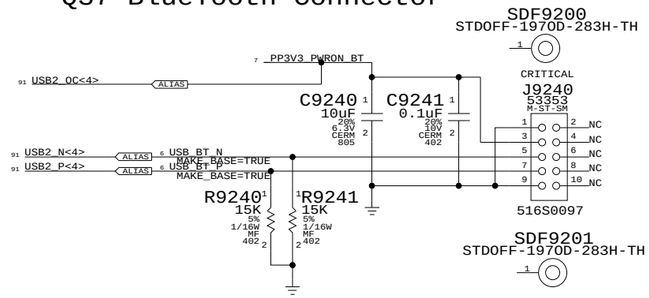
NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

- USB2_PWREN<0> → TP_USB2_PWREN<0> MAKE_BASE=TRUE
- USB2_PWREN<1> → TP_USB2_PWREN<1> MAKE_BASE=TRUE
- USB2_PWREN<2> → TP_USB2_PWREN<2> MAKE_BASE=TRUE
- USB2_PWREN<3> → TP_USB2_PWREN<3> MAKE_BASE=TRUE
- USB2_PWREN<4> → TP_USB2_PWREN<4> MAKE_BASE=TRUE

External USB Ports



Q37 BlueTooth Connector



USB Device Interfaces

NOTICE OF PROPRIETARY PROPERTY

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II NOT TO REPRODUCE OR COPY IT

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 92 OF 99	

_DRAWING
TITLE=FIZZY
ABBREV=DRAWING
LAST_MODIFIED=Fri Nov 21 11:23:57 2003

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_MODEM
  Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NEED TO PICK A MODEM TO STUFF FOR EVT

AND THE CORRESPONDING STANDOFF

Q52 Modem Connector

SDF9400
STDOFF-4MM-9MMH-TH

CRITICAL
J9401
C104A-H9.0
F-ST-SM

7 _PP3V3_PWRON_MODEM

NC	35		
NC	31	32	NC
NC	1	2	NC
	3	4	NC
NC	5	6	MODEM_RING2SYS_L 6 25 94
NC	7	8	
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
	15	16	NC
	17	18	NC
	19	20	
NC	21	22	I2S1_SYNC 6 25 94
94 76 25 6 I2S1_SB_TO_DEV_DTO	23	24	I2S1_DEV_TO_SB_DTI 6 25 76 94
94 25 6 I2S1_RESET_L	25	26	
	27	28	
94 25 6 I2S1_MCLK	29	30	I2S1_BITCLK 6 25 94
NC	33	34	NC
NC	36		

516S0116

SDF9401
STDOFF-4MM-9MMH-TH

GND_CHASSIS_MODEM 1

NOSTUFF
EMI9400
EMI-SPRING
S8-100G

From Intel Mobile Audio/Modem
Daughter Card Specification
Rev 1.0, February 22, 1999

1 - MONO_OUT/PC_BEEP	2 - AUDIO_PWRON
3 - GND	4 - MONO_PHONE
5 - AUXA_RIGHT	6 - RESERVED
7 - AUXA_LEFT	8 - GND
9 - CD_GND	10 - 5Vmain
11 - CD_RIGHT	12 - RESERVED
13 - CD_LEFT	14 - RESERVED
15 - GND	16 - PRIMARY_DN
17 - 3.3Vaux	18 - 5Vd
19 - GND	20 - GND
21 - 3.3Vmain	22 - AC97_SYNC
23 - AC97_SDATA_OUT	24 - AC97_SDATA_INB
25 - AC97_RESET#	26 - AC97_SDATA_INA
27 - GND	28 - GND
29 - AC97_MSTRCLK	30 - AC97_BITCLK

MicroDash Modem Connector

SOFT MODEM IS PLAN OF RECORD
MICRODASH MODEM CONNECTOR LEFT ON FOR DEVELOPMENT PURPOSES ONLY

NOSTUFF
SDF9402
STDOFF-5MM-5.5MMH-TH

91 USB2_OC<3> ALIAS

7 _PP3V3_PWRON_UDASH

DEVELOPMENT C9400 4.7uF 20% 10V CERM 1206
DEVELOPMENT C9401 0.1uF 20% 10V CERM 402
DEVELOPMENT R9400 10K 5% 1/16W MF 402
NOSTUFF R9401 10K 5% 1/16W MF 402
DEVELOPMENT R9402 10K 5% 1/16W MF 402

DEVELOPMENT
J9400
5047
F-ST-SM

(+3.3V)	1	2	(+3.3V)
(GND)	3	4	(RST*) UDASH_RESET_L 6 25
(SDOWN)	5	6	(RTS*) I2S1_MCLK 6 25 94
(GND)	7	8	(DTR*) I2S1_RESET_L 6 25 94
(RXD)	9	10	(GND)
(GPIO*)	11	12	(TXD*) I2S1_SB_TO_DEV_DTO 6 25 76 94
(GND)	13	14	(TRXC) I2S1_BITCLK 6 25 94
(RING*)	15	16	(GND)
(HOOK)	NC 17	18	(D-) USB_UDASH_N 6 MAKE_BASE=TRUE
(GND)	19	20	(D+) USB_UDASH_P 6 MAKE_BASE=TRUE
(SCL)	21	22	(GND)
(GND)	23	24	(SDA) I2C_UDASH_SDA 6 18
(A0)	25	26	(A1) UDASH_I2C_A1_PU 6
(SNDIN)	NC 27	28	(+5V)
(SNDOUT)	NC 29	30	(+5V) PP5V_PWRON_UDASH 7

516S0121

25 6 UDASH_SDOWN
Default to Modem On
94 76 25 6 I2S1_DEV_TO_SB_DTI
94 25 6 I2S1_SYNC
94 25 6 MODEM_RING2SYS_L
MODEM_RING2SYS_L SHOULD BE PULLED UP ON SB
18 6 I2C_UDASH_SCL

ALIAS USB2_N<3> 91
ALIAS USB2_P<3> 91

DEVELOPMENT R9404 15K 5% 1/16W MF 402
DEVELOPMENT R9403 15K 5% 1/16W MF 402

DEVELOPMENT C9402 0.1uF 20% 10V CERM 402
DEVELOPMENT C9403 10uF 20% 6.3V CERM 1206

NOSTUFF
J9402
013-0001-333
RJ11-ST-TH

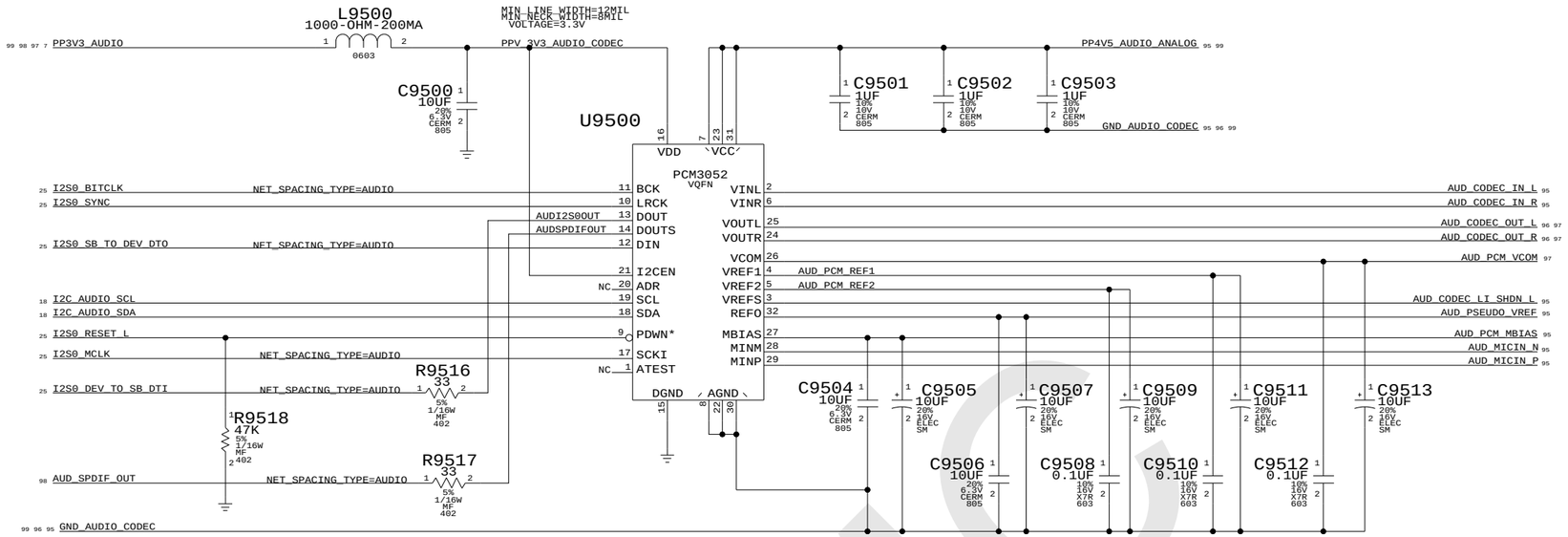
Modem Interface

APPLE COMPUTER INC.

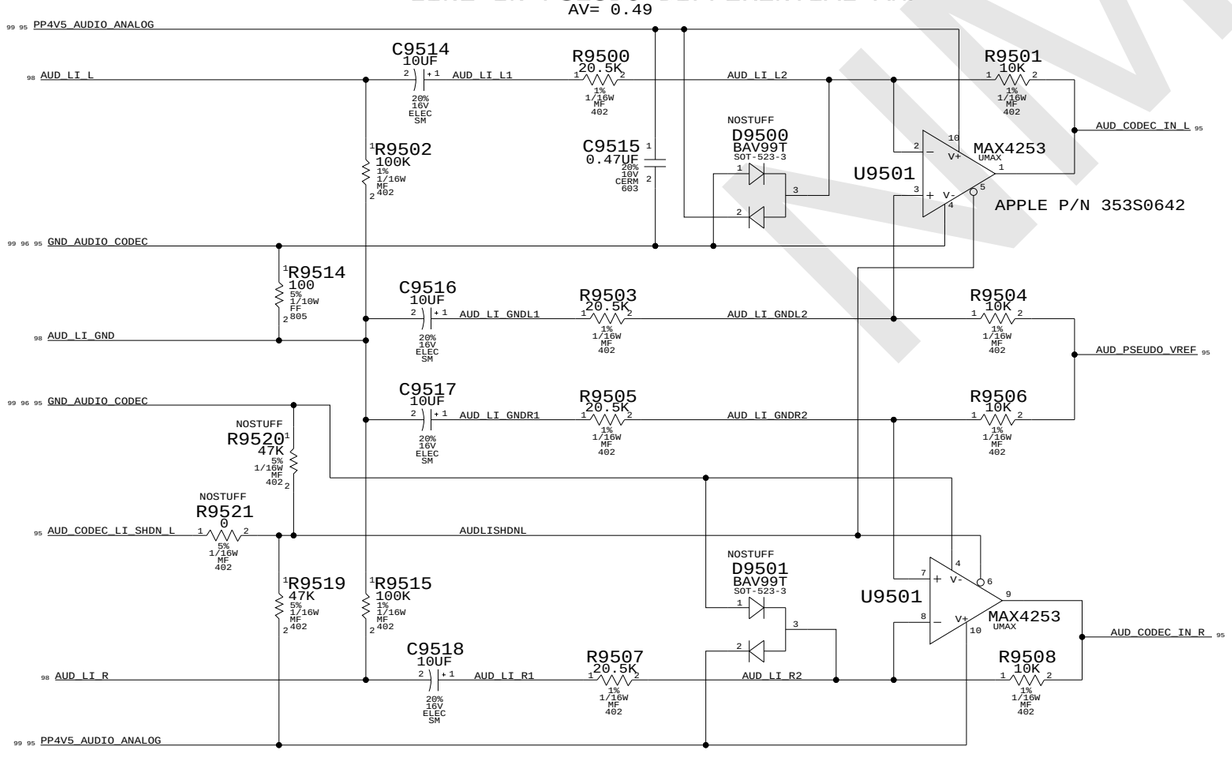
SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT	OF
NONE	94	99

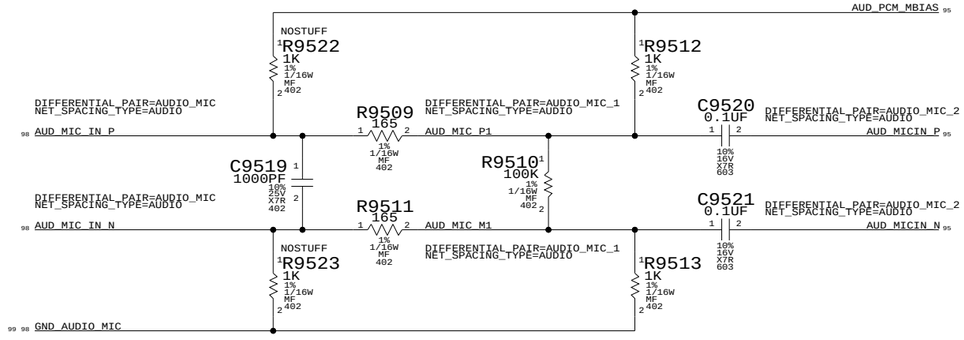
AUDIO CODEC
APPLE P/N 353S0655



LINE IN PSEUDO-DIFFERENTIAL AMP
AV= 0.49



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: CODEC, LINE INPUT

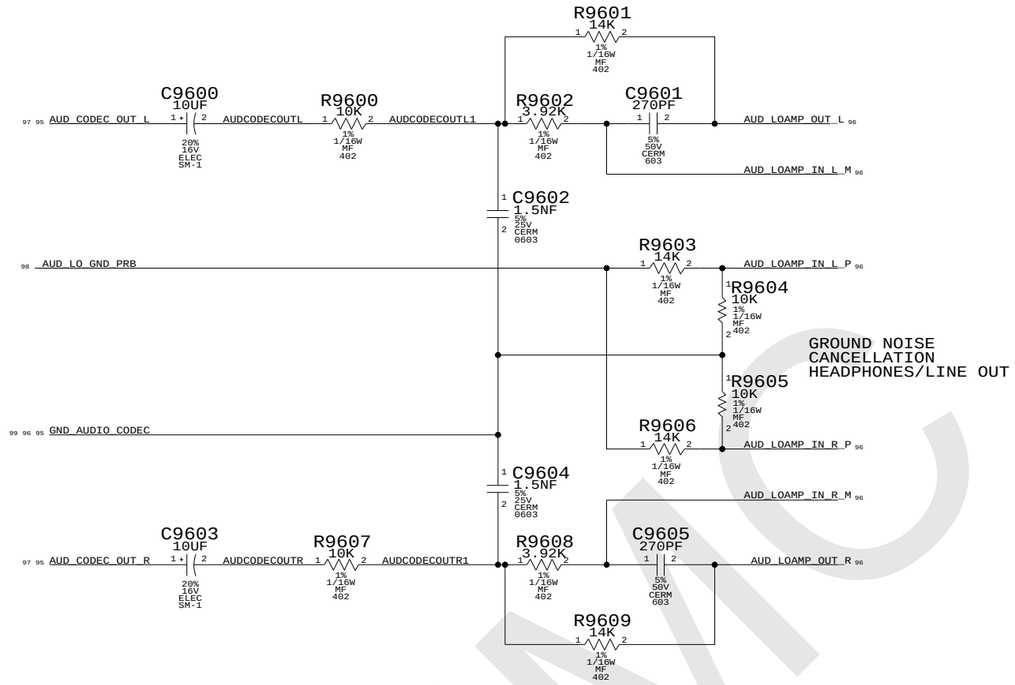
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT	OF
NONE	95	99

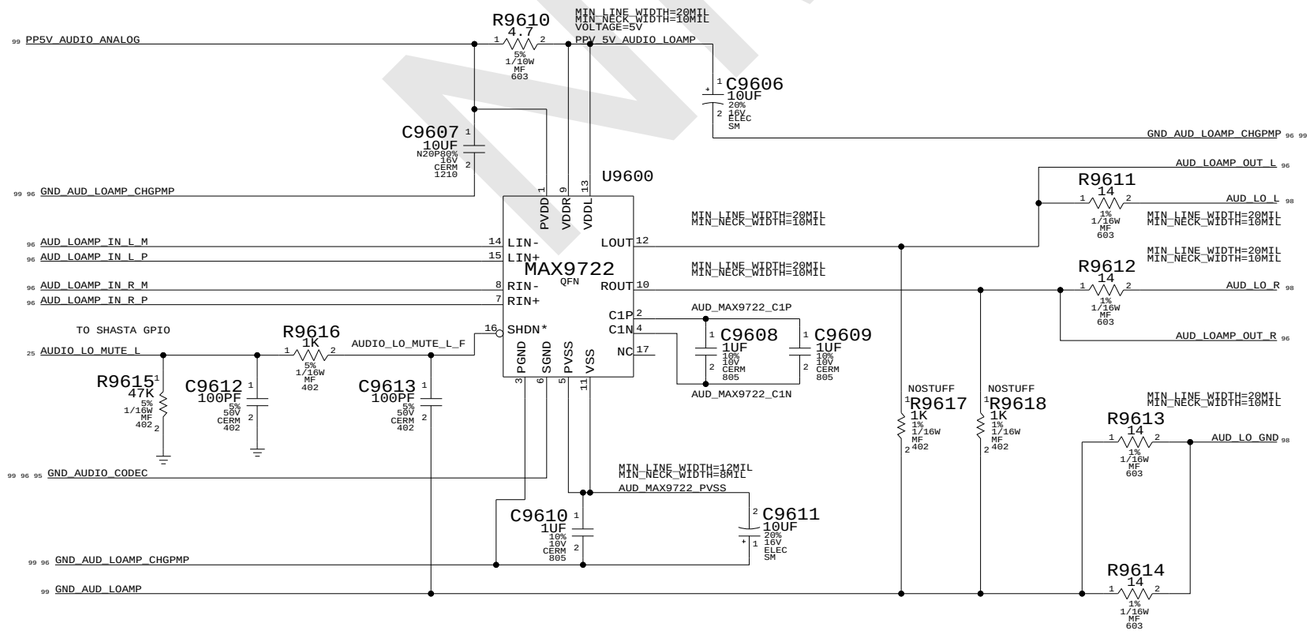
CODEC OUTPUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



HEADPHONES/LINE OUT AMP

APPLE P/N 353S0697



AUDIO:HEADPHONES / LINE OUT

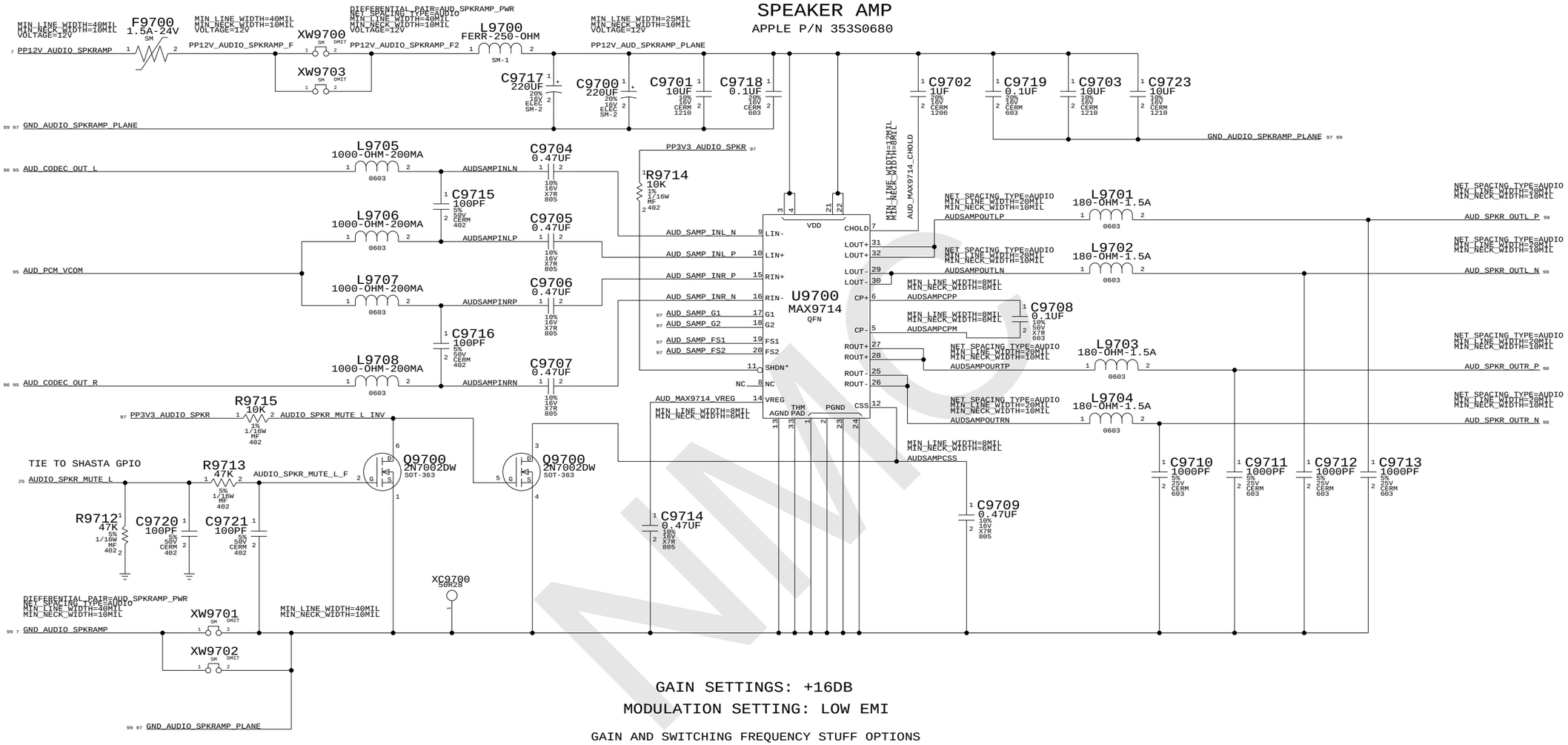
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE	SHT	OF
NONE	96	99

SPEAKER AMP

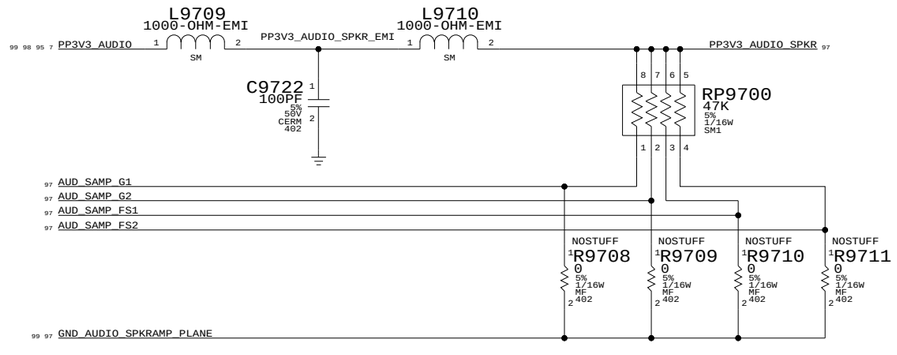
APPLE P/N 353S0680



GAIN SETTINGS: +16DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13

SCALE: NONE

SHT 97 OF 99

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0169	5	FLTR,EMI,FERR BD,180 OHM,1.5A	R9822,R9823,R9824,R9825	R9837
155S0093	31	FLTR,EMI,FERR BD,100 OHM.0603	R9814,R9815,R9816,R9817	R9818,R9819,R9820,R9821,R9826,R9827,R9828,R9829,R9830,R9831,R9843,R9844,R9832,R9833,R9834,R9835,R9836,R9845,R9846,R9838,R9839,R9840,R9841,R9842,R9810,R9848,R9849

LINE IN JACK

APPLE P/N 514-0098

CRITICAL
J9800
AUDIO_JACK
F-ST-TH

MIN_LINE_WIDTH=8MIL MIN_NECK_WIDTH=6MIL
AUD_LI_L_JACK — R9814 0 OMIT — MIN_LINE_WIDTH=8MIL MIN_NECK_WIDTH=6MIL — AUD_LI_L_EMI — R9818 0 OMIT — MIN_LINE_WIDTH=8MIL MIN_NECK_WIDTH=6MIL — AUD_LI_L 95

AUD_LI_DET_JACK — R9815 0 OMIT — AUD_LI_DET_EMI — R9819 0 OMIT — AUD_LI_DET_H 98

AUD_LI_R_JACK — R9816 0 OMIT — AUD_LI_R_EMI — R9820 0 OMIT — AUD_LI_R 95

AUD_LI_GND_JACK — R9817 0 OMIT — AUD_LI_GND_EMI — R9821 0 OMIT — AUD_LI_GND 95

98 7 GND_CHASSIS_AUDIO_EXTERNAL

MIN_LINE_WIDTH=8MIL MIN_NECK_WIDTH=6MIL
98 AUD_LI_GND_EMI

98 7 GND_CHASSIS_AUDIO_EXTERNAL

C9800 100PF 5% 50V CERM 402
C9801 100PF 5% 50V CERM 402
C9802 100PF 5% 50V CERM 402
C9803 100PF 5% 50V CERM 402

DZ9800
14V-15A
0405

SPEAKER CABLE CONNECTOR

APPLE P/N 518-0138

97 AUD_SPKR_OUTR_P — R9822 0 OMIT — AUD_SPKR_OUTR_P_CONN — NET_SPACING_TYPE=AUDIO MIN_LINE_WIDTH=20MIL MIN_NECK_WIDTH=12MIL — CRITICAL J9801 10-89-7082 M-ST-TH — AUD_SPKR_OUTR_N_CONN — R9824 0 OMIT — AUD_SPKR_OUTR_N 97

97 AUD_SPKR_OUTL_N — R9823 0 OMIT — AUD_SPKR_OUTL_N_CONN — R9825 0 OMIT — AUD_SPKR_OUTL_P 97

99 98 97 95 7 PP3V3_AUDIO — R9813 47K

25 AUDIO_GPIO_12 — SPEAKER TYPE DETECT TO SHASTA GPIO

L9800 1000-OHM-200MA 0603

AUDIO_GPIO_12_CONN

C9819 1000PF 5% 25V CERM 603
C9825 1000PF 5% 25V CERM 603
C9826 1000PF 5% 25V CERM 603
C9827 1000PF 5% 25V CERM 603

NOSTUFF C9804 1000PF 5% 25V CERM 603
NOSTUFF C9805 1000PF 5% 25V CERM 603
NOSTUFF C9806 1000PF 5% 25V CERM 603
NOSTUFF C9807 1000PF 5% 25V CERM 603

98 7 GND_CHASSIS_AUDIO_INTERNAL

LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED

99 98 97 95 7 PP3V3_AUDIO
R9800 100K 5% 1/16W MF 402
R9801 47K 5% 1/16W MF 402 — TO SHASTA GPIO — AUDIO_LI_DET_L 25
98 AUD_LI_DET_H — R9802 47K 5% 1/16W MF 402 — AUDLINDETH
Q9800 2N7002 SM
C9808 0.1UF 20% 10V CERM 402

MIC CABLE CONNECTOR

APPLE P/N 518-0034

99 95 GND_AUDIO_MIC — R9826 0 OMIT — GND_AUDIO_MIC_EMI — R9829 0 OMIT — GND_AUDIO_MIC_CONN
95 AUD_MIC_IN_P — R9827 0 OMIT — AUD_MIC_IN_P_EMI — R9830 0 OMIT — AUD_MIC_IN_P_CONN
95 AUD_MIC_IN_N — R9828 0 OMIT — AUD_MIC_IN_N_EMI — R9831 0 OMIT — AUD_MIC_IN_N_CONN

CRITICAL J9802 HF28 M-ST-TH

C9820 1000PF 10% 25V X7R 402
C9821 1000PF 10% 25V X7R 402
C9822 1000PF 10% 25V X7R 402

98 7 GND_CHASSIS_AUDIO_INTERNAL

LINE OUT PLUG DETECTS

AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED

99 98 97 95 7 PP3V3_AUDIO
R9803 100K 5% 1/16W MF 402
R9804 47K 5% 1/16W MF 402 — TO SHASTA GPIO — AUDIO_LO_DET_L 6 25
Q9801 2N7002DW SOT-363
98 AUD_LO_DET1 — R9805 47K — AUD_LO_DET1_1
C9809 0.1UF 20% 10V CERM 402

99 98 97 95 7 PP3V3_AUDIO
R9806 100K 5% 1/16W MF 402
R9807 47K 5% 1/16W MF 402 — TO SHASTA GPIO
NOTE: NET NAME WILL CHANGE TO AUDIO_LO_OPTICAL_PLUG_L / AUDIO_LO_METAL_PLUG_L 25
Q9801 2N7002DW SOT-363
98 AUD_LO_DET2 — R9808 47K — AUD_LO_DET2_1
NOSTUFF R9809 100K 5% 1/16W MF 402
C9810 0.1UF 20% 10V CERM 402

PLACE NEAR J9801 — XC9800 SOR28
PLACE NEAR J700 — XC9801 SOR28

LINE OUT JACK

APPLE P/N 514-0116

CRITICAL
J9803
AUDIO-JCK-SPDIF
F-ST-TH

95 AUD_SPDIF_OUT — R9843 0 OMIT — AUD_SPDIF_OUT_EMI — R9845 0 OMIT — AUD_SPDIF_OUT_JACK
7 PP5V_AUDIO — R9844 0 OMIT — MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL — PP5V_AUDIO_SPDIF_EMI — R9846 0 OMIT — MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL — PP5V_AUDIO_SPDIF_JACK
98 AUD_LO_DET1 — R9832 0 OMIT — AUD_LO_DET1_EMI — R9838 0 OMIT — AUD_LO_DET1_JACK
96 AUD_LO_R — R9833 0 OMIT — MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL — AUD_LO_R_EMI — R9839 0 OMIT — AUD_LO_R_JACK
96 AUD_LO_L — R9834 0 OMIT — MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL — AUD_LO_L_EMI — R9840 0 OMIT — AUD_LO_L_JACK
98 AUD_LO_DET2 — R9835 0 OMIT — AUD_LO_DET2_EMI — R9841 0 OMIT — AUD_LO_DET2_JACK
96 AUD_LO_GND — R9836 0 OMIT — MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL — AUD_LO_GND_EMI — R9842 0 OMIT — AUD_LO_GND_JACK
96 AUD_LO_GND_PRB — R9837 0 OMIT — AUD_LO_GND_PRB_EMI — R9810 0 OMIT — AUD_LO_GND_PRB_JACK

MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL
AUD_LO_GND_JACK
AUD_LO_DET1_JACK
AUD_LO_R_JACK
AUD_LO_L_JACK
AUD_LO_DET2_JACK

VIN VDD GND LED

MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL
AUD_SPDIF_GND

R9812 1 0 5% 1/16W MF 402

98 7 GND_CHASSIS_AUDIO_INTERNAL

C9823 100PF 5% 50V CERM 402
C9824 100PF 5% 50V CERM 402
C9811 100PF 5% 50V CERM 402
C9812 100PF 5% 50V CERM 402
C9813 100PF 5% 50V CERM 402
C9814 100PF 5% 50V CERM 402
C9815 100PF 5% 50V CERM 402
C9816 0.01UF 10% 16V CERM 402
C9817 0.1UF 20% 10V CERM 402
C9818 1UF 10% 10V CERM 805

AUD_LI_GND_EMI 98

DZ9801
14V-15A
0405

NOT USED: R9811, R9848, R9849.

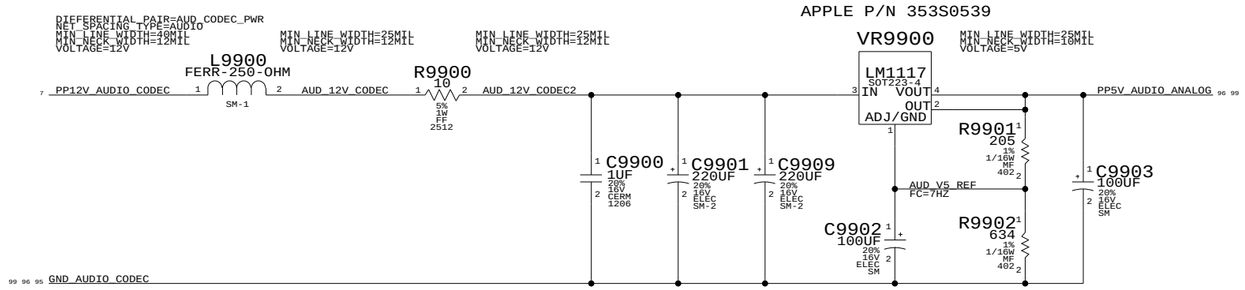
AUDIO: Q45 CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 98 OF 99	

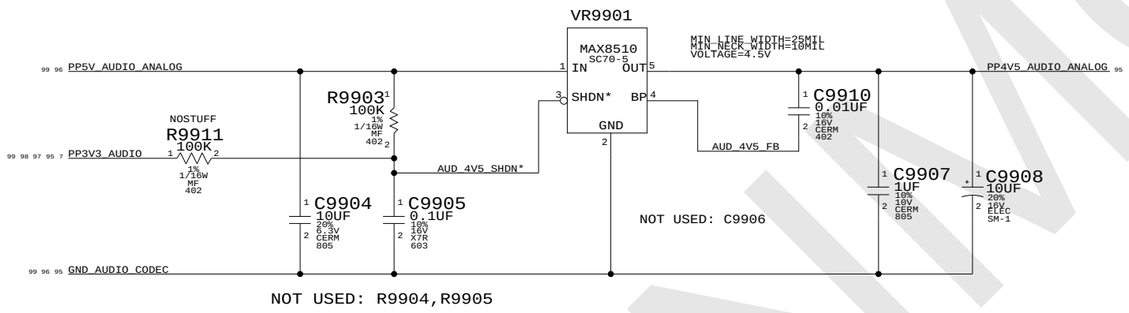
5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP

APPLE P/N 353S0539

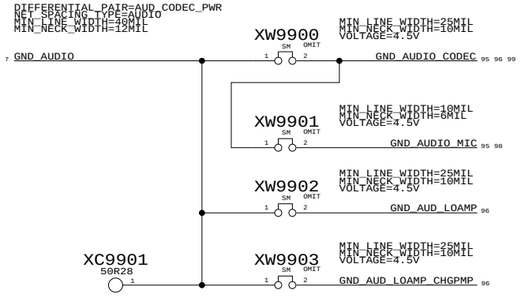


4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

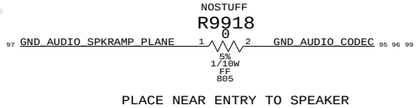
APPLE P/N 353S0733



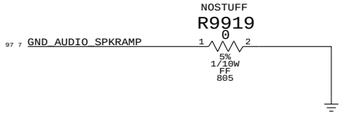
AUDIO GROUND RETURNS



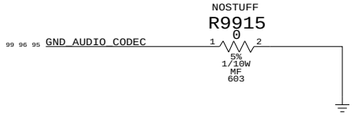
PLACE ACROSS GROUND SPLIT
AT RIGHT SIDE OF C9707



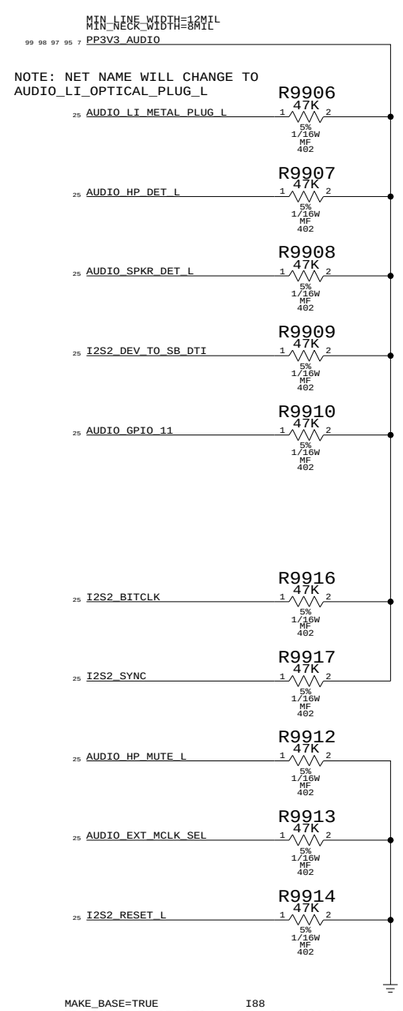
PLACE NEAR ENTRY TO SPEAKER
AMP GROUND PLANE



PLACE ACROSS GROUND SPLIT
AT CODEC U9500



UNUSED GPIO TERMINATIONS



AUDIO: Q45 POWER SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE: NONE	SHT 99 OF 99	