Am3101-1 • Am54/7489-1
Am3101 • Am54/7489

Schottky 64-Bit Write Transparent Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low-power write transparent Schottky RAMs
- Fast "–1" Version: Address access time 35ns
- Standard Version: Address access time 50ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Available with open collector outputs
- Pin compatible replacements for 6560, 93403

FUNCTIONAL DESCRIPTION

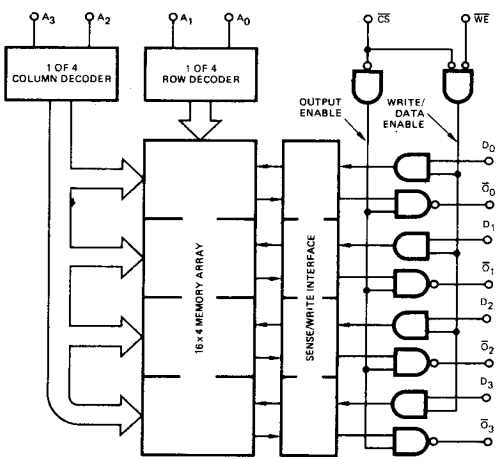
The Am3101-1/3101 and Am54/7489-1/Am54/7489 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word. During the write cycle, the outputs are active and invert the four data inputs, D_0 to D_3.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

When the chip select line is HIGH, the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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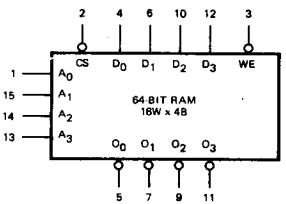
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°
Ambient Temperature with Power Applied	−55 to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} ma
DC Input Voltage	−0.5 to +5.5
Output Current, Into Outputs	20m
DC Input Current	−30 to +5.0m

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Input $\overline{CS}$	Input $\overline{WE}$	Function	Data Output Status $\overline{O}_0-\overline{O}_3$
Low	Low	Write	D_0-D_3 (Inverted)
Low	High	Read	Selected Word (Inverted)
High	Don't Care	Deselect	Output and Write Disabled

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA		0.350	0.45	Volts
			I_{OL} = 20mA		0.380	0.5	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3		−0.015	−0.25	mA
			$\overline{CS}$		−0.030	−0.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V			0.0	10	μA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX	COM'L		75	100	mA
			MIL		75	105	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA			−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} V_{OUT} = 2.4V $V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}			0	40	μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

ITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

: Conditions: See Figures 3 and 4 and Notes 3 and 4

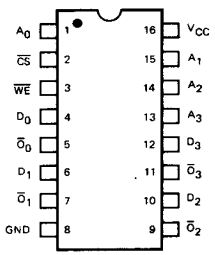
ameters	Description		Am3101-1 • Am54/7489-1 Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Am3101 • Am54/7489 Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$_H(A)$ $_{HL}(A)$	Delay from Address to Output	See Fig. 2	22		35		50	32		50		60	ns
$_{ZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2	14		17		25	20		30		40	ns
$_{ZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1	19		35		50	30		50		60	ns
A)	Setup Time Address (Prior to Initiation of Write)	See Fig. 1	−6.0	0		0		−6.0	0		0		ns
A)	Hold Time Address (After Termination of Write)	See Fig. 1	−2.5	0		0		−2.5	0		0		ns
DI)	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1	18	25		25		24	30		30		ns
DI)	Hold Time Data Input (After Termination of Write)	See Fig. 1	−4.0	0		0		−4.0	0		0		ns
$_W(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	See Fig. 1	18	25		25		24	30		30		ns
$_Z(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)	See Fig. 2	13		17		25	20		30		40	ns
$_H(DI)$ $_{HL}(DI)$	Delay Data Input to Correct Data Output ($\overline{WE} = \overline{CS} = V_{IL}$)	See Fig. 1	18		35		50	30		50		60	ns

es: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. Output is conditioned to data in (inverted) during write to insure correct data is present on all outputs during write and after write is terminated.
3. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30pF$ with both input and output timing referenced to 1.5V.
4. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30pF$; and with both the input and output timing referenced to 1.5V.

3

CONNECTION DIAGRAMS
Top Views

DIP



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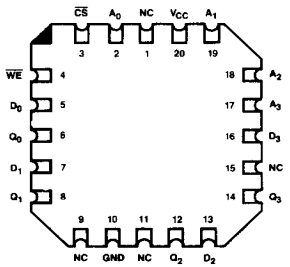
Note: Pin 1 is marked for orientation.

Chip-Pak™



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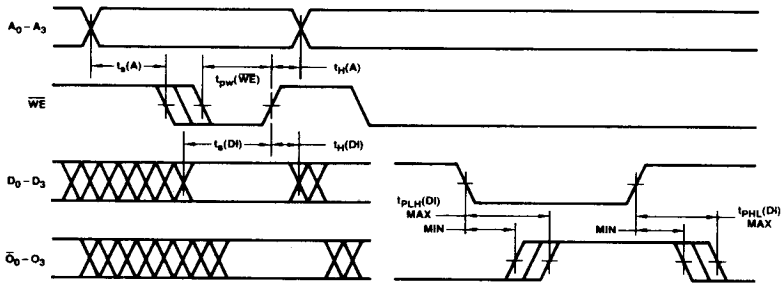
SWITCHING WAVEFORMS

WRITE MODE



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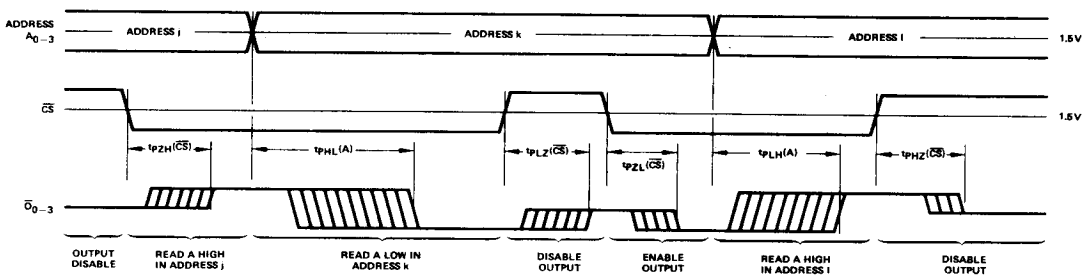
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive while the write enable is ($\overline{WE}$) LOW.

Figure 1

READ MODE



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Switching delays from address and chip select inputs to the data output. A disabled output is HIGH.

Figure 2

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

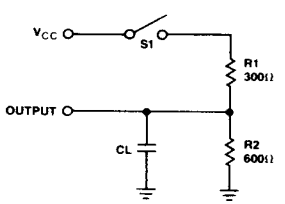

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Figure 3

INPUT PULSES

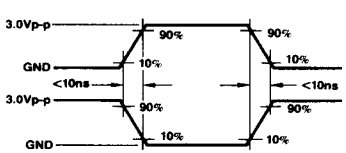

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Figure 4

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM3101-1PC	P-16-1	C-1	COM'L
	AM7489-1N	P-16-1	C-1	
	AM3101-1DC	D-16-1	C-1	
	AM7489-1J	D-16-1	C-1	
	AM3101-1DCB	D-16-1	B-1	
	AM7489-1JB	D-16-1	B-1	
	AM3101-1LC	Consult Factory	C-1	
	AM7489-1LC	Consult Factory	C-1	
	AM3101-1LCB	Consult Factory	B-1	
	AM7489-1LCB	Consult Factory	B-1	
50ns	AM3101-1DM	D-16-1	C-3	MIL
	AM5489-1J	D-16-1	C-3	
	AM3101-1DMB	D-16-1	B-3	
	AM5489-1JB	D-16-1	B-3	
	AM3101-1FM	F-16-1	C-3	
	AM5489-1W	F-16-1	C-3	
	AM3101-1FMB	F-16-1	B-3	
	AM5489-1WB	F-16-1	B-3	
	AM3101-1LM	Consult Factory	C-3	
	AM5489-1LM	Consult Factory	C-3	
	AM3101-1LMB	Consult Factory	B-3	
	AM5489-1LMB	Consult Factory	B-3	
50ns	AM3101PC	P-16-1	C-1	COM'L
	AM7489N	P-16-1	C-1	
	AM3101DC	D-16-1	C-1	
	AM7489J	D-16-1	C-1	
	AM3101DCB	D-16-1	B-1	
	AM7489JB	D-16-1	B-1	
	AM3101LC	Consult Factory	C-1	
	AM7489LC	Consult Factory	C-1	
	AM3101LCB	Consult Factory	B-1	
	AM7489LCB	Consult Factory	B-1	
60ns	AM3101DM	D-16-1	C-3	MIL
	AM5489J	D-16-1	C-3	
	AM3101DMB	D-16-1	B-3	
	AM5489JB	D-16-1	B-3	
	AM3101FM	F-16-1	C-3	
	Am5489W	F-16-1	C-3	
	AM3101FMB	F-16-1	B-3	
	AM5489WB	F-16-1	B-3	
	AM3101LM	Consult Factory	C-3	
	AM5489LM	Consult Factory	C-3	
	AM3101LMB	Consult Factory	B-3	
	AM5489LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.