

# DATA SHEET

Datasheet.Directory

## **PCF8584** I<sup>2</sup>C-bus controller

Product specification  
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**I<sup>2</sup>C-bus controller****PCF8584**

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**1 FEATURES**

- Parallel-bus to I<sup>2</sup>C-bus protocol converter and interface
- Compatible with most parallel-bus microcontrollers/microprocessors including 8049, 8051, 6800, 68000 and Z80
- Both master and slave functions
- Automatic detection and adaption to bus interface type
- Programmable interrupt vector
- Multi-master capability
- I<sup>2</sup>C-bus monitor mode
- Long-distance mode (4-wire)
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range: -40 to +85 °C.

**2 GENERAL DESCRIPTION**

The PCF8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/microprocessors and the serial I<sup>2</sup>C-bus. The PCF8584 provides both master and slave functions.

Communication with the I<sup>2</sup>C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I<sup>2</sup>C-bus specific sequences, protocol, arbitration and timing. The PCF8584 allows parallel-bus systems to communicate bidirectionally with the I<sup>2</sup>C-bus.

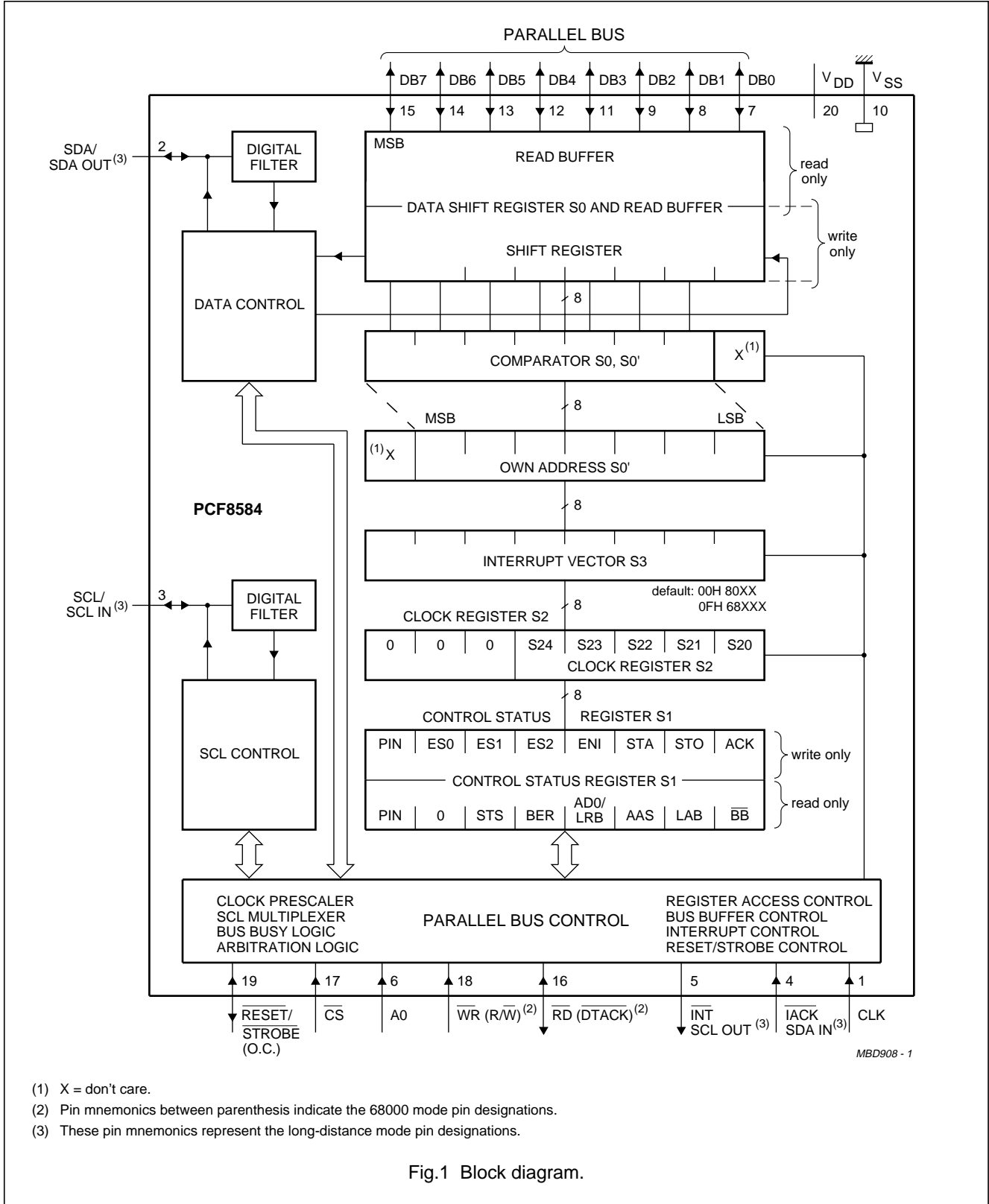
**3 ORDERING INFORMATION**

| TYPE NUMBER | PACKAGE |  |          |
|-------------|---------|--|----------|
|             | NAME    | DESCRIPTION  | VERSION  |
| PCF8584P    | DIP20   | plastic dual in-line package; 20 leads (300 mil)           | SOT146-1 |
| PCF8584T    | SO20    | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |

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4 BLOCK DIAGRAM



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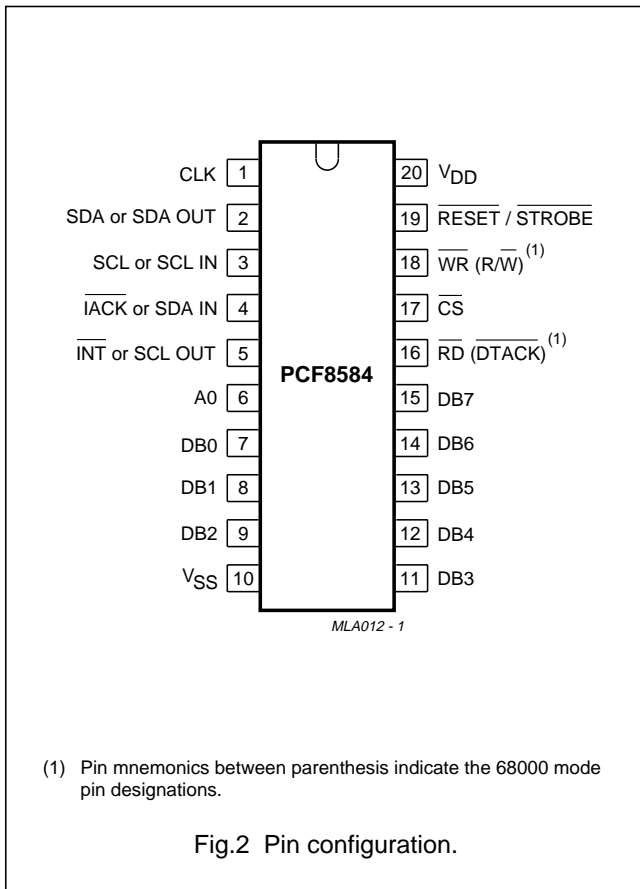
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## 5 PINNING

| SYMBOL   | PIN | I/O   | DESCRIPTION   |
|--|-----|-------|---|
| CLK  | 1   | I     | clock input from microcontroller clock generator (internal pull-up)   |
| SDA or SDA OUT                                       | 2   | I/O   | I <sup>2</sup> C-bus serial data input/output (open-drain). Serial data output in long-distance mode.   |
| SCL or SCL IN  | 3   | I/O   | I <sup>2</sup> C-serial clock input/output (open-drain). Serial clock input in long-distance mode.  |
| $\overline{\text{IACK}}$ or SDA IN                   | 4   | I     | Interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in register S3 will be available at the bus Port if the ENI flag is set. Serial data input in long-distance mode.   |
| $\overline{\text{INT}}$ or SCL OUT                   | 5   | O     | Interrupt output (open-drain); this signal is enabled by the ENI flag in register S1. It is asserted when the PIN flag is reset. (PIN is reset after 1 byte is transmitted or received over the I <sup>2</sup> C-bus). Serial clock output in long-distance mode. |
| A0   | 6   | I     | Register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects register S1, logic 0 selects one of the other registers depending on bits loaded in ESO, ES1 and ES2 of register S1.    |
| DB0  | 7   | I/O   | bidirectional 8-bit bus Port 0  |
| DB1  | 8   | I/O   | bidirectional 8-bit bus Port 1  |
| DB2  | 9   | I/O   | bidirectional 8-bit bus Port 2  |
| V <sub>SS</sub>                                      | 10  | –     | ground  |
| DB3  | 11  | I/O   | bidirectional 8-bit bus Port 3  |
| DB4  | 12  | I/O   | bidirectional 8-bit bus Port 4  |
| DB5  | 13  | I/O   | bidirectional 8-bit bus Port 5  |
| DB6  | 14  | I/O   | bidirectional 8-bit bus Port 6  |
| DB7  | 15  | I/O   | bidirectional 8-bit bus Port 7  |
| $\overline{\text{RD}}$ ( $\overline{\text{DTACK}}$ ) | 16  | I/(O) | $\overline{\text{RD}}$ is the read control input for MAB8049, MAB8051 or Z80-types. $\overline{\text{DTACK}}$ is the data transfer control output for 68000-types (open-drain).   |
| $\overline{\text{CS}}$                               | 17  | I     | chip select input (internal pull-up)  |
| $\overline{\text{WR}}$ (R/ $\overline{\text{W}}$ )   | 18  | I     | $\overline{\text{WR}}$ is the write control input for MAB8048, MAB8051, or Z80-types (internal pull-up). R/ $\overline{\text{W}}$ control input for 68000-types.  |
| $\overline{\text{RESET}}$ /<br>STROBE                | 19  | I/O   | Reset input (open-drain); this input forces the I <sup>2</sup> C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.  |
| V <sub>DD</sub>                                      | 20  | –     | supply voltage  |

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**Table 1** Control signals utilized by the PCF8584 for microcontroller/microprocessor interfacing

| TYPE          | R/W | WR  | R   | DTACK | IACK |
|---------------|-----|-----|-----|-------|------|
| 8048/<br>8051 | no  | yes | yes | no    | no   |
| 68000         | yes | no  | no  | yes   | yes  |
| Z80           | no  | yes | yes | no    | yes  |

The structure of the PCF8584 is similar to that of the I<sup>2</sup>C-bus interface section of the Philips' MABXXX/PCF84(C)XX-series of microcontrollers, but with a modified control structure. The PCF8584 has five internal register locations. Three of these (own address register S0', clock register S2 and interrupt vector S3) are used for initialization of the PCF8584. Normally they are only written once directly after resetting of the PCF8584.

The remaining two registers function as double registers (data buffer/shift register S0, and control/status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. Register S0 is a combination of a shift register and data buffer.

Register S0 performs all serial-to-parallel interfacing with the I<sup>2</sup>C-bus.

Register S1 contains I<sup>2</sup>C-bus status information required for bus access and/or monitoring.

**6 FUNCTIONAL DESCRIPTION**

**6.1 General**

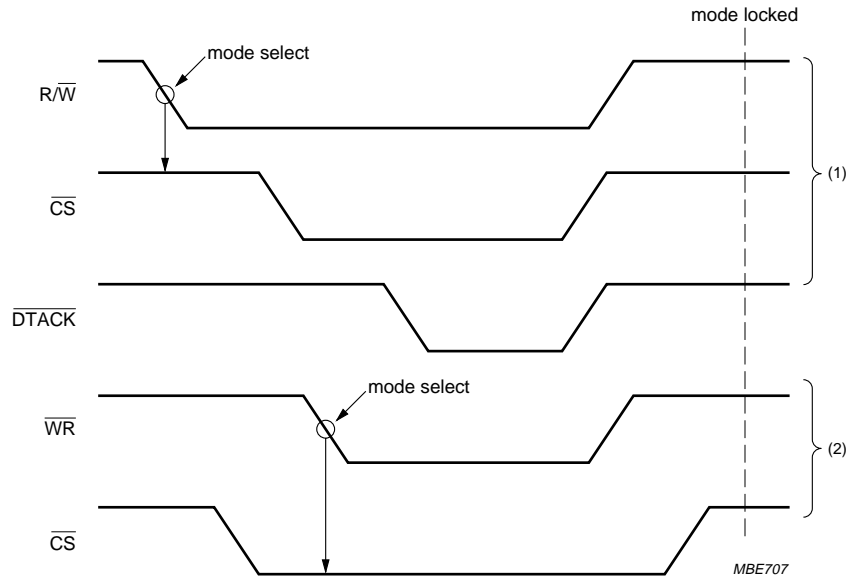
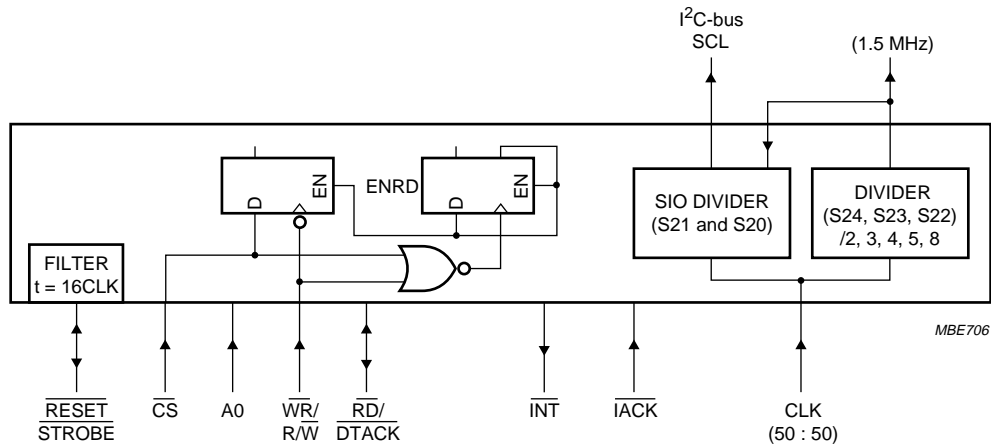
The PCF8584 acts as an interface device between standard high-speed parallel buses and the serial I<sup>2</sup>C-bus. On the I<sup>2</sup>C-bus, it can act either as master or slave. Bidirectional data transfer between the I<sup>2</sup>C-bus and the parallel-bus microcontroller is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. 8048, 8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed (see Section 6.2).

**6.2 Interface Mode Control (IMC)**

Selection of either an 80XX mode or 68000 mode interface is achieved by detection of the first WR-CS signal sequence. The concept takes advantage of the fact that the write control input is common for both types of interfaces. An 80XX-type interface is default. If a HIGH-to-LOW transition of WR (R/W) is detected while CS is HIGH, the 68000-type interface mode is selected and the DTACK output is enabled. Care must be taken that WR and CS are stable after reset.

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- (1) Bus timing; 68000 mode write cycle.
- (2) Bus timing; 80XX mode.

Fig.3 68000/80XX timing sequence utilized by the Interface Mode Control (IMC).

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**6.3 Set-up registers S0', S2 and S3**

Registers S0', S2 and S3 are used for initialization of the PCF8584 (see Fig.5 'Initialization sequence' flowchart).

**6.4 Own address register S0'**

When the PCF8584 is addressed as slave, this register must be loaded with the 7-bit I<sup>2</sup>C-bus address to which the PCF8584 is to respond. During initialization, the own address register S0' must be written to, regardless whether it is later used. The Addressed As Slave (AAS) bit in status register S1 is set when this address is received (the value in S0 is compared with the value in S0'). Note that the S0 and S0' registers are offset by one bit; hence, programming the own address register S0' with a value of 55H will result in the value AAH being recognized as the PCF8584's slave address (see Fig.1).

Programming of S0' is accomplished via the parallel-bus when A0 is LOW, with the appropriate bit combinations set in control status register S1 (S1 is written when pin A0 = HIGH). Bit combinations for accessing all registers are given in Table 5. After reset, S0' has default address 00H (PCF8584 is thus initially in monitor mode, see Section 6.12.3).

**6.5 Clock register S2**

Register S2 provides control over chip clock frequency and SCL clock frequency. S20 and S21 provide a selection of 4 different I<sup>2</sup>C-bus SCL frequencies which are shown in Table 2. Note that these SCL frequencies are only obtained when bits S24, S23 and S22 are programmed to the correct input clock frequency ( $f_{clk}$ ).

**Table 2** Register S2 selection of SCL frequency

| BIT |     | APPROXIMATE SCL<br>FREQUENCY $f_{SCL}$ (kHz) |
|-----|-----|--|
| S21 | S20 |  |
| 0   | 0   | 90   |
| 0   | 1   | 45   |
| 1   | 0   | 11   |
| 1   | 1   | 1.5  |

S22, S23 and S24 are used for control of the internal clock prescaler. Due to the possibility of varying microcontroller clock signals, the prescaler can be programmed to adapt to 5 different clock rates, thus providing a constant internal clock. This is required to provide a stable time base for the SCL generator and the digital filters associated with the I<sup>2</sup>C-bus signals SCL and SDA. Selection for adaption to external clock rates is shown in Table 3.

Programming of S2 is accomplished via the parallel-bus when A0 = LOW, with the appropriate bit combinations set in control status register S1 (S1 is written when A0 = HIGH). Bit combinations for accessing all registers are given in Table 5.

**Table 3** Register S2 selection of clock frequency

| INTERNAL CLOCK FREQUENCY |                  |                  |                 |
|--------------------------|------------------|------------------|-----------------|
| S24                      | S23              | S22              | $f_{clk}$ (MHz) |
| 0                        | X <sup>(1)</sup> | X <sup>(1)</sup> | 3               |
| 1                        | 0                | 0                | 4.43            |
| 1                        | 0                | 1                | 6               |
| 1                        | 1                | 0                | 8               |
| 1                        | 1                | 1                | 12              |

**Note**

1. X = don't care.

**6.6 Interrupt vector S3**

The interrupt vector register provides an 8-bit user-programmable vector for vectored-interrupt microcontrollers. The vector is sent to the bus port (DB7 to DB0) when an interrupt acknowledge signal is asserted and the ENI (enable interrupt) flag is set. Default vector values are:

- Vector is '00H' in 80XX mode
- Vector is '0FH' in 68000 mode.

On reset the PCF8584 is in the 80XX mode, thus the default interrupt vector is '00H'.

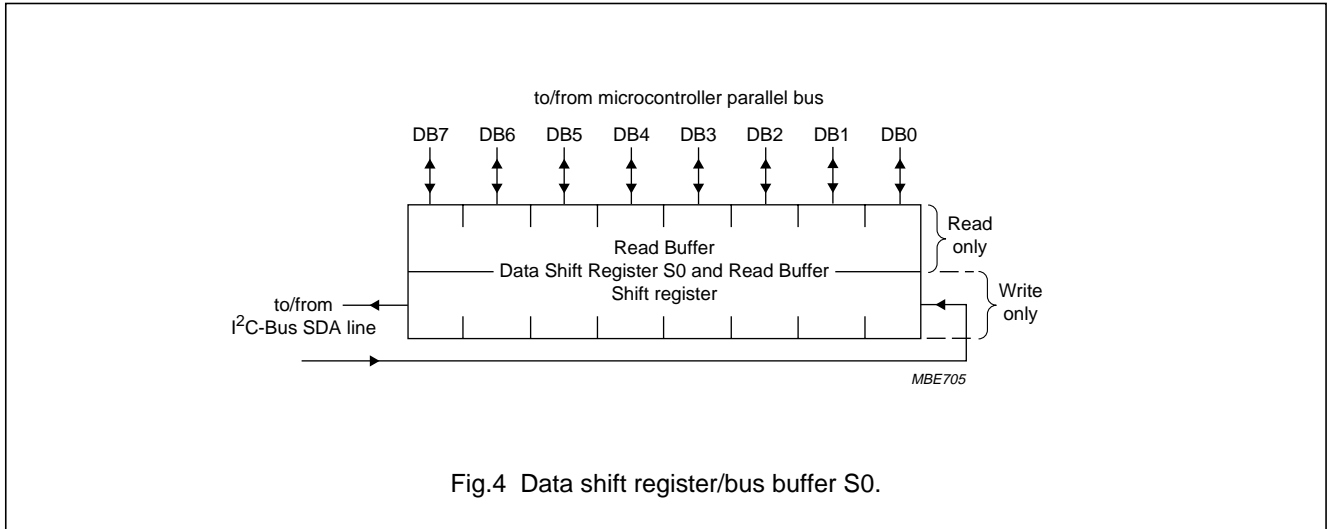
**6.7 Data shift register/read buffer S0**

Register S0 acts as serial shift register and read buffer interfacing to the I<sup>2</sup>C-bus. All read and write operations to/from the I<sup>2</sup>C-bus are done via this register. S0 is a combination of a shift register and a data buffer; parallel data is always written to the shift register, and read from the data buffer. I<sup>2</sup>C-bus data is always shifted in or out of shift register S0.



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In receiver mode the data from the shift register is copied to the read buffer during the acknowledge phase. Further reception of data is inhibited (SCL held LOW) until the S0 read buffer is read (see Section 6.8.1.1).

In the transmitter mode data is transmitted to the I<sup>2</sup>C-bus as soon as it is written to the S0 shift register if the serial I/O is enabled (ESO = 1).

**Remarks:**

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses to the PCF8584 when the I<sup>2</sup>C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. To start a read operation immediately after a write, it is necessary to read the S0 read buffer in order to invoke reception of the first byte ('dummy read' of the address). Immediately after the acknowledgement, this first byte will be transferred from the shift register to the read buffer. The **next** read will then transfer the correct value of the first byte to the microcontroller bus (see Fig.7).

**6.8 Control/status register S1**

Register S1 controls I<sup>2</sup>C-bus operation and provides I<sup>2</sup>C-bus status information. Register S1 is accessed by a HIGH signal on register select input A0. For more efficient communication between microcontroller/processor and the I<sup>2</sup>C-bus, register S1 has separate read and write functions for all bit positions (see Fig.3). The write-only section provides register access control and control over I<sup>2</sup>C-bus signals, while the read-only section provides I<sup>2</sup>C-bus status information.

**Table 4** Control/status register S1

| CONTROL/STATUS         | BITS |                  |     |     |         |     |     |                 | MODE       |
|------------------------|------|------------------|-----|-----|---------|-----|-----|-----------------|------------|
| Control <sup>(1)</sup> | PIN  | ESO              | ES1 | ES2 | ENI     | STA | STO | ACK             | write only |
| Status <sup>(2)</sup>  | PIN  | 0 <sup>(3)</sup> | STS | BER | AD0/LRB | AAS | LAB | $\overline{BB}$ | read only  |

**Notes**

1. For further information see Section 6.8.1.
2. For further information see Section 6.8.2.
3. Logic 1 if not-initialized.

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## 6.8.1 REGISTER S1 CONTROL SECTION

The write-only section of S1 enables access to registers S0, S0', S1, S2 and S3, and controls I<sup>2</sup>C-bus operation; see Table 4.

## 6.8.1.1 PIN (Pending Interrupt Not)

When the PIN bit is written with a logic 1, all status bits are reset to logic 0. This may serve as a software reset function (see Figs 5 to 9). PIN is the only bit in S1 which may be both read and written to. PIN is mostly used as a status bit for synchronizing serial communication, see Section 6.8.2.

## 6.8.1.2 ESO (Enable Serial Output)

ESO enables or disables the serial I<sup>2</sup>C-bus I/O. When ESO is LOW, register access for initialization is possible. When ESO is HIGH, I<sup>2</sup>C-bus communication is enabled; communication with serial shift register S0 is enabled and the S1 bus status bits are made available for reading.

**Table 5** Register access control; ESO = 0 (serial interface off) and ESO = 1 (serial interface on)

| INTERNAL REGISTER ADDRESSING 2-WIRE MODE          |     |     |                          |                                    |
|---|-----|-----|--------------------------|------------------------------------|
| A0  | ES1 | ES2 | $\overline{\text{IACK}}$ | FUNCTION                           |
| <b>ESO = 0; serial interface off</b> (see note 1) |     |     |                          |                                    |
| 1   | 0   | X   | 1 <sup>(2)</sup>         | R/W S1: control                    |
| 0   | 0   | 0   | 1 <sup>(2)</sup>         | R/W S0': (own address)             |
| 0   | 0   | 1   | 1 <sup>(2)</sup>         | R/W S3: (interrupt vector)         |
| 0   | 1   | 0   | 1 <sup>(2)</sup>         | R/W S2: (clock register)           |
| <b>ESO = 1; serial interface on</b>               |     |     |                          |                                    |
| 1   | 0   | X   | 1                        | W S1: control                      |
| 1   | 0   | X   | 1                        | R S1; status                       |
| 0   | 0   | 0   | 1                        | R/W S0: (data)                     |
| 0   | 0   | 1   | 1                        | R/W S3: (interrupt vector)         |
| X   | 0   | X   | 0                        | R S3: (interrupt vector ACK cycle) |

**Notes**

1. With ESO = 0, bits ENI, STA, STO and ACK of S1 can be read for test purposes.
2. 'X' if ENI = 0.

## 6.8.1.3 ES1 and ES2

ES1 and ES2 control selection of other registers for initialization and control of normal operation. After these bits are programmed for access to the desired register (shown in Table 5), the register is selected by a logic LOW level on register select pin A0.

## 6.8.1.4 ENI

This bit enables the external interrupt output  $\overline{\text{INT}}$ , which is generated when the PIN bit is active (logic 0).

**This bit must be set to logic 0 before entering the long-distance mode, and remain at logic 0 during operation in long-distance mode.**

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## 6.8.1.5 STA and STO

These bits control the generation of the I<sup>2</sup>C-bus START condition and transmission of slave address and R/W bit, generation of repeated START condition, and generation of the STOP condition (see Table 7).

**Table 6** Register access control; ESO = 1 (serial interface on) and ES1 = 1; long-distance (4-wire) mode; note 1

| INTERNAL REGISTER ADDRESSING: LONG-DISTANCE (4-WIRE) MODE |     |     |                          |                |
|---|-----|-----|--------------------------|----------------|
| A0  | ES1 | ES2 | $\overline{\text{IACK}}$ | FUNCTION       |
| 1   | 1   | X   | 1                        | W S1: control  |
| 1   | 1   | X   | X                        | R S1; status   |
| 0   | 1   | X   | X                        | R/W S0; (data) |

**Note**

- Trying to read from or write to registers other than S0 and S1 (setting ESO = 0) brings the PCF8584 out of the long-distance mode.

**Table 7** Instruction table for serial bus control

| STA | STO | PRESENT MODE        | FUNCTION                 | OPERATION  |
|-----|-----|---------------------|--------------------------|--|
| 1   | 0   | SLV/REC             | START                    | transmit START + address, remain MST/TRM if R/W = 0;<br>go to MST/REC if R/W = 1 |
| 1   | 0   | MST/TRM             | REPEAT START             | same as for SLV/REC  |
| 0   | 1   | MST/REC;<br>MST/TRM | STOP READ;<br>STOP WRITE | transmit STOP go to SLV/REC mode; note 1   |
| 1   | 1   | MST                 | DATA CHAINING            | send STOP, START and address after last master frame without STOP sent; note 2   |
| 0   | 0   | ANY                 | NOP                      | no operation; note 3   |

**Notes**

- In master receiver mode, the last byte must be terminated with ACK bit HIGH ('negative acknowledge').
- If both STA and STO are set HIGH simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows 'chaining' of transmissions without relinquishing bus control.
- All other STA and STO mode combinations not mentioned in Table 7 are NOPs.

## 6.8.1.6 ACK

This bit must be set normally to a logic 1. This causes the I<sup>2</sup>C-bus controller to send an acknowledge automatically after each byte (this occurs during the 9th clock pulse). The bit must be reset (to logic 0) when the I<sup>2</sup>C-bus controller is operating in master/receiver mode and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the I<sup>2</sup>C-bus, which halts further transmission from the slave device.

## 6.8.2 REGISTER S1 STATUS SECTION

The read-only section of S1 enables access to I<sup>2</sup>C-bus status information; see Table 4.

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### 6.8.2.1 PIN bit

'Pending Interrupt Not' (MSB of register S1) is a status flag which is used to synchronize serial communication and is set to logic 0 whenever the PCF8584 requires servicing. The PIN bit is normally read in polled applications to determine when an I<sup>2</sup>C-bus byte transmission/reception is completed. The PIN bit may also be written, see Section 6.8.1.

Each time a serial data transmission is initiated (by setting the STA bit in the same register), the PIN bit will be set to logic 1 automatically (inactive). When acting as transmitter, PIN is also set to logic 1 (inactive) each time S0 is written. In receiver mode, the PIN bit is automatically set to logic 1 (inactive) each time the data register S0 is read.

After transmission or reception of one byte on the I<sup>2</sup>C-bus (9 clock pulses, including acknowledge), the PIN bit will be automatically reset to logic 0 (active) indicating a complete byte transmission/reception. When the PIN bit is subsequently set to logic 1 (inactive), all status bits will be reset to logic 0. PIN is also set to zero on a BER (bus error) condition.

In polled applications, the PIN bit is tested to determine when a serial transmission/reception has been completed. When the ENI bit (bit 4 of write-only section of register S1) is also set to logic 1 the hardware interrupt is enabled. In this case, the PIN flag also triggers an external interrupt (active LOW) via the  $\overline{\text{INT}}$  output each time PIN is reset to logic 0 (active).

When acting as slave transmitter or slave receiver, while PIN = 0, the PCF8584 will suspend I<sup>2</sup>C-bus transmission by holding the SCL line LOW until the PIN bit is set to logic 1 (inactive). This prevents further data from being transmitted or received until the current data byte in S0 has been read (when acting as slave receiver) or the next data byte is written to S0 (when acting as slave transmitter).

PIN bit summary:

- The PIN bit can be used in polled applications to test when a serial transmission has been completed. When the ENI bit is also set, the PIN flag sets the external interrupt via the  $\overline{\text{INT}}$  output.
- Setting the STA bit (start bit) will set PIN = 1 (inactive).
- In transmitter mode, after successful transmission of one byte on the I<sup>2</sup>C-bus the PIN bit will be automatically reset to logic 0 (active) indicating a complete byte transmission.
- In transmitter mode, PIN is set to logic 1 (inactive) each time register S0 is written.

- In receiver mode, PIN is set to logic 0 (active) on completion of each received byte. Subsequently, the SCL line will be held LOW until PIN is set to logic 1.
- In receiver mode, when register S0 is read, PIN is set to logic 1 (inactive).
- In slave receiver mode, an I<sup>2</sup>C-bus STOP condition will set PIN = 0 (active).
- PIN = 0 if a bus error (BER) occurs.

### 6.8.2.2 STS

When in slave receiver mode, this flag is asserted when an externally generated STOP condition is detected (used only in slave receiver mode).

### 6.8.2.3 BER

Bus error; a misplaced START or STOP condition has been detected. Resets  $\overline{\text{BB}}$  (to logic 1; inactive), sets PIN = 0 (active).

### 6.8.2.4 LRB/AD0

'Last Received Bit' or 'Address 0 (General Call) bit'. This status bit serves a dual function, and is valid only while PIN = 0:

1. LRB holds the value of the last received bit over the I<sup>2</sup>C-bus while AAS = 0 (not addressed as slave). Normally this will be the value of the slave acknowledgement; thus checking for slave acknowledgement is done via testing of the LRB.
2. AD0; when AAS = 1 ('Addressed As Slave' condition), the I<sup>2</sup>C-bus controller has been addressed as a slave. Under this condition, this bit becomes the 'AD0' bit and will be set to logic 1 if the slave address received was the 'general call' (00H) address, or logic 0 if it was the I<sup>2</sup>C-bus controller's own slave address.

### 6.8.2.5 AAS

'Addressed As Slave' bit. Valid only when PIN = 0. When acting as slave receiver, this flag is set when an incoming address over the I<sup>2</sup>C-bus matches the value in own address register S0' (shifted by one bit, see Section 6.4), or if the I<sup>2</sup>C-bus 'General Call' address (00H) has been received ('General Call' is indicated when AD0 status bit is also set to logic 1, see Section 6.8.2.4).

### 6.8.2.6 LAB

'Lost Arbitration' Bit. This bit is set when, in multi-master operation, arbitration is lost to another master on the I<sup>2</sup>C-bus.

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### 6.8.2.7 $\overline{BB}$

'Bus Busy' bit. This is a read-only flag indicating when the I<sup>2</sup>C-bus is in use. A zero indicates that the bus is busy, and access is not possible. This bit is set/reset (logic 1/logic 0) by STOP/START conditions.

### 6.9 Multi-master operation

To avoid conflict between data and repeated START and STOP operations, multi-master systems have some limitations:

- When powering up multiple PCF8584s in multi-master systems, the possibility exists that one node may power up slightly after another node has already begun an I<sup>2</sup>C-bus transmission; the Bus Busy condition will thus not have been detected. To avoid this condition, a delay should be introduced in the initialization sequence of each PCF8584 equal to the longest I<sup>2</sup>C-bus transmission, see flowchart 'PCF8584 initialization' (Fig.5).

### 6.10 Reset

A LOW level pulse on the  $\overline{RESET}$  (CLK must run) input forces the I<sup>2</sup>C-bus controller into a well-defined state. All flags in S1 are reset to logic 0, except the PIN flag and the  $\overline{BB}$  flag, which are set to logic 1. S0' and S3 are set to 00H.

The  $\overline{RESET}$  pin is also used for the  $\overline{STROBE}$  output signal. Both functions are separated on-chip by a digital filter. The reset input signal has to be sufficiently long (minimum 30 clock cycles) to pass through the filter. The  $\overline{STROBE}$  output signal is sufficiently short (8 clock cycles) to be blocked by the filter. For more detailed information on the strobe function see Section 6.12.

### 6.11 Comparison to the MAB8400 I<sup>2</sup>C-bus interface

The structure of the PCF8584 is similar to that of the MAB8400 series of microcontrollers, but with a modified control structure. Access to all I<sup>2</sup>C-bus control and status registers is done via the parallel-bus port in conjunction with register select input A0, and control bits ESO, ES1 and ES2.

### 6.11.1 DELETED FUNCTIONS

The following functions are not available in the PCF8584:

- Always selected (ALS flag)
- Access to the bit counter (BC0 to BC2)
- Full SCL frequency selection (2 bits instead of 5 bits)
- The non-acknowledge mode (ACK flag)
- Asymmetrical clock (ASC flag).

### 6.11.2 ADDED FUNCTIONS

The following functions either replace the deleted functions or are completely new:

- Chip clock prescaler
- Assert acknowledge bit (ACK flag)
- Register selection bits (ES1 and ES2 flags)
- Additional status flags (BER, 'bus error')
- Automatic interface control between 80XX and 68000-type microcontrollers
- Programmable interrupt vector
- Strobe generator
- Bus monitor function
- Long-distance mode [non-I<sup>2</sup>C-bus mode (4-wire); only for communication between parallel-bus processors using the PCF8584 at each interface point].

### 6.12 Special function modes

#### 6.12.1 STROBE

When the I<sup>2</sup>C-bus controller receives its own address (or the '00H' general call address) followed immediately by a STOP condition (i.e. no further data transmitted after the address), a strobe output signal is generated at the  $\overline{RESET}/\overline{STROBE}$  pin (pin 19). The  $\overline{STROBE}$  signal consists of a monostable output pulse (active LOW), 8 clock cycles long (see Fig.9). It is generated after the STOP condition is received, preceded by the correct slave address. This output can be used as a bus access controller for multi-master parallel-bus systems.

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### 6.12.2 LONG-DISTANCE MODE

The long-distance mode provides the possibility of longer-distance serial communication between parallel processors via two I<sup>2</sup>C-bus controllers. This mode is selected by setting ES1 to logic 1 while the serial interface is enabled (ESO = 1).

In this mode the I<sup>2</sup>C-bus protocol is transmitted over 4 unidirectional lines, SDA OUT, SCL IN, SDA IN and SCL IN (pins 2, 3, 4 and 5). These communication lines should be connected to line drivers/receivers (example: RS422) for long-distance applications. Hardware characteristics for long-distance transmission are then given by the chosen standard. Control of data transmission is the same as in normal I<sup>2</sup>C-bus mode. After reading or writing data to shift register S0, long-distance mode must be initialized by setting ESO and ES1 to logic 1. Because the interrupt output INT is not available in this operating mode, synchronization of data transmission/reception must be polled via the PIN bit.

#### Remarks:

Before entering the long-distance mode, ENI must be set to logic 0.

When powering up an PCF8584-node in long-distance mode, the PCF8584 must be isolated from the 4-wire bus via 3-state line drivers/receivers until the PCF8584 is properly initialized for long-distance mode. Failure to implement this precaution will result in system malfunction.

### 6.12.3 MONITOR MODE

When the 7-bit own address register S0' is loaded with all zeros, the I<sup>2</sup>C-bus controller acts as a passive I<sup>2</sup>C monitor. The main features of the monitor mode are:

- The controller is always selected.
- The controller is always in the slave receiver mode.
- The controller never generates an acknowledge.
- The controller never generates an interrupt request.
- A pending interrupt condition does not force SCL LOW.
- $\overline{BB}$  is set to logic 0 after detection of a START condition, and reset to logic 1 after a STOP condition.
- Received data is automatically transferred to the read buffer.
- Bus traffic is monitored by the PIN bit, which is reset to logic 0 after the acknowledge bit of an incoming byte has been received, and is set to logic 1 as soon as the first bit of the next incoming byte is detected. Reading the data buffer S0 sets the PIN bit to logic 1. Data in the read buffer is valid from PIN = 0 and during the next 8 clock pulses (until next acknowledge).
- AAS is set to logic 1 at every START condition, and reset at every 9th clock pulse.

## 7 SOFTWARE FLOWCHART EXAMPLES

### 7.1 Initialization

The flowchart of Fig.5 gives an example of a proper initialization sequence of the PCF8584.

### 7.2 Implementation

The flowcharts (Figs 6 to 9) illustrate proper programming sequences for implementing master transmitter, master receive, and master transmitter, repeated start and master receiver modes in polled applications.

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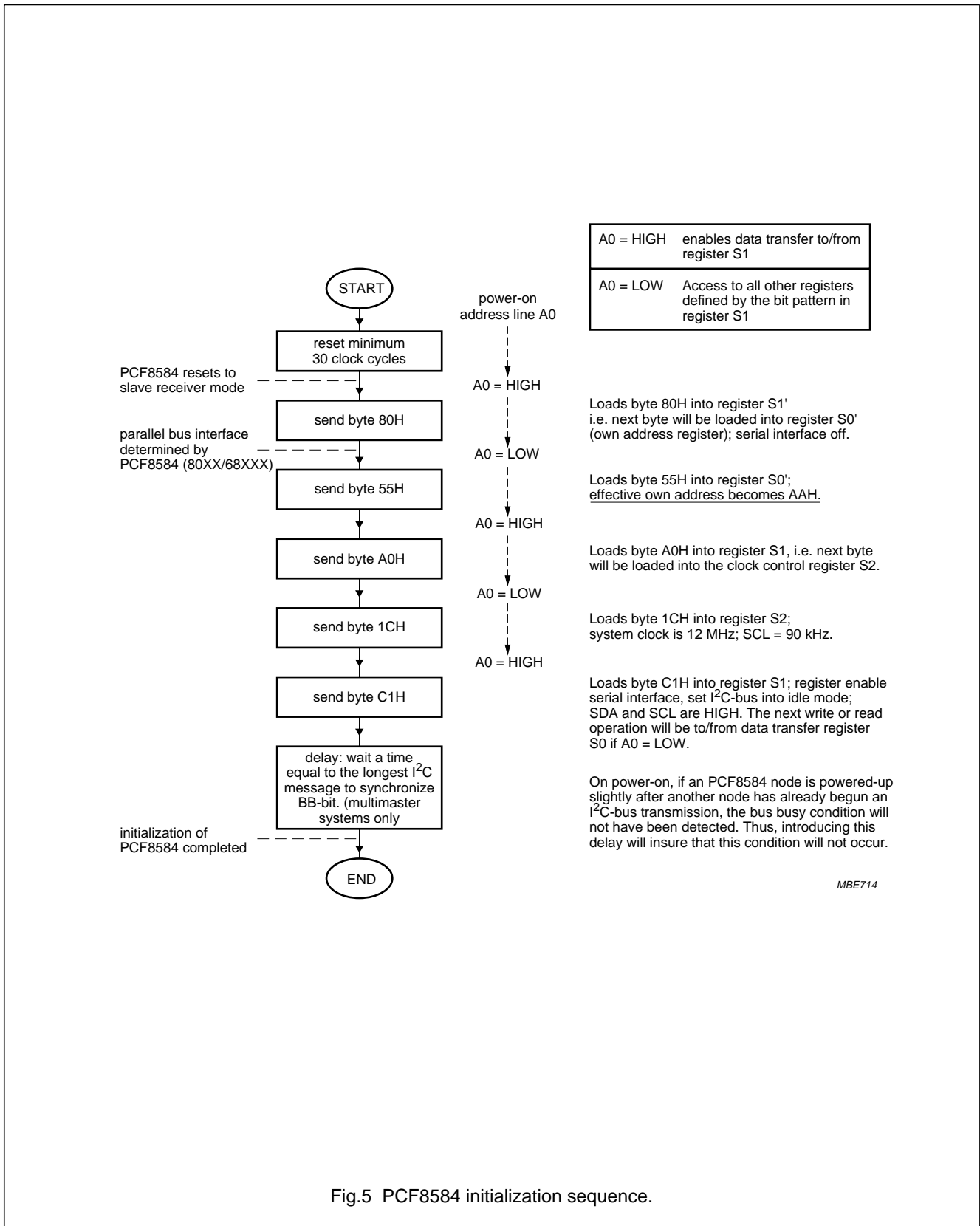


Fig.5 PCF8584 initialization sequence.

I<sup>2</sup>C-bus controller

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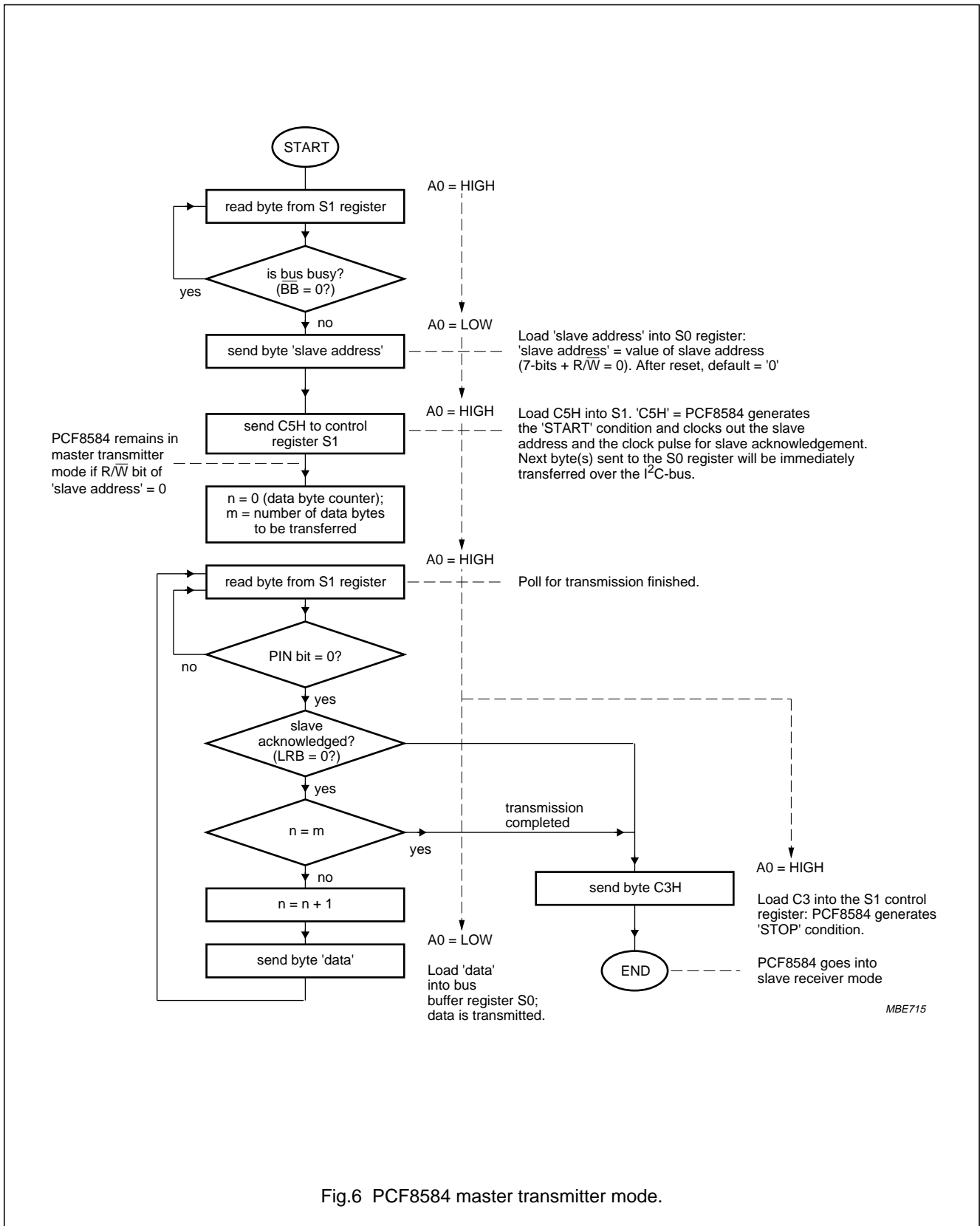
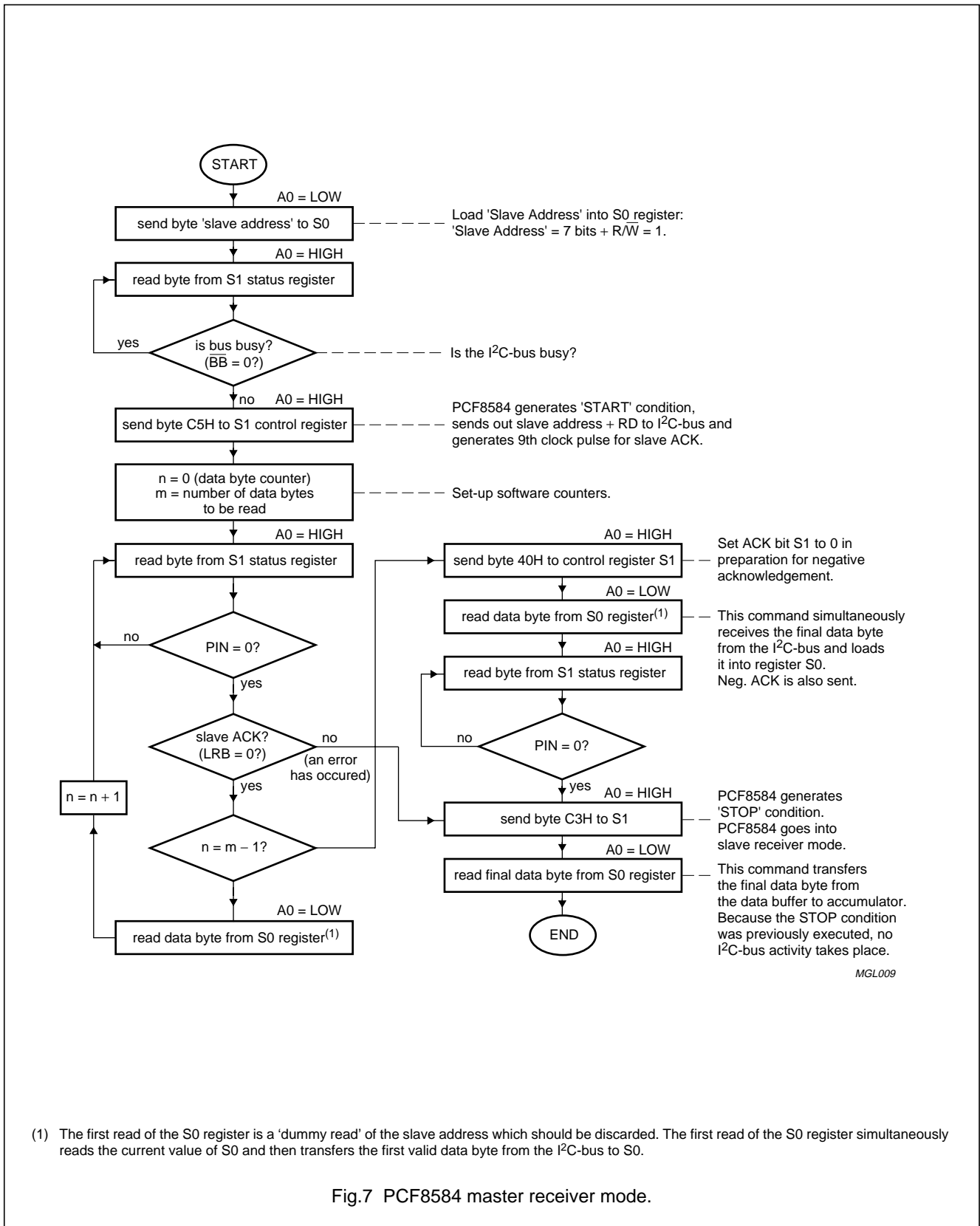


Fig.6 PCF8584 master transmitter mode.



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I<sup>2</sup>C-bus controller

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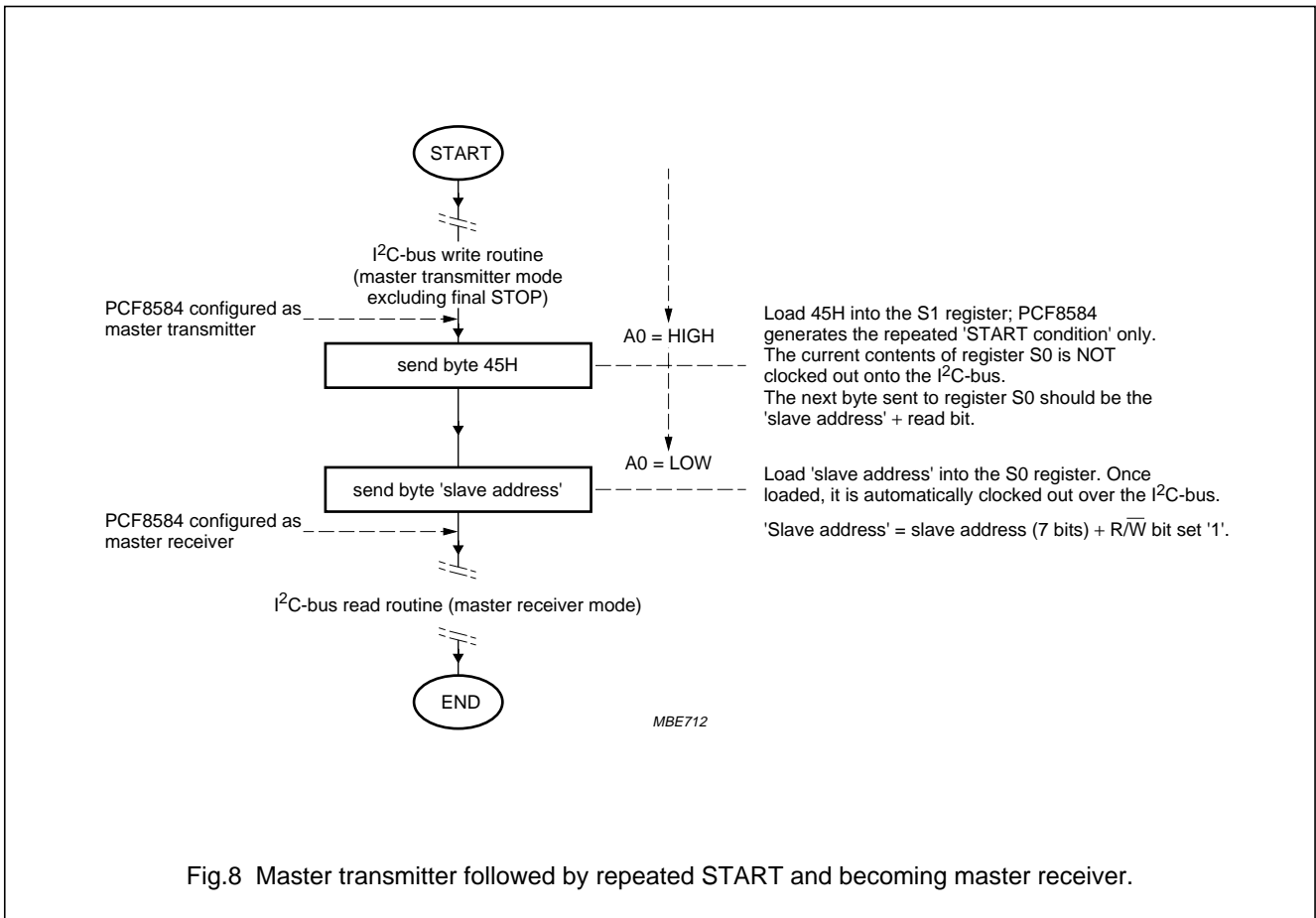


Fig.8 Master transmitter followed by repeated START and becoming master receiver.

I<sup>2</sup>C-bus controller

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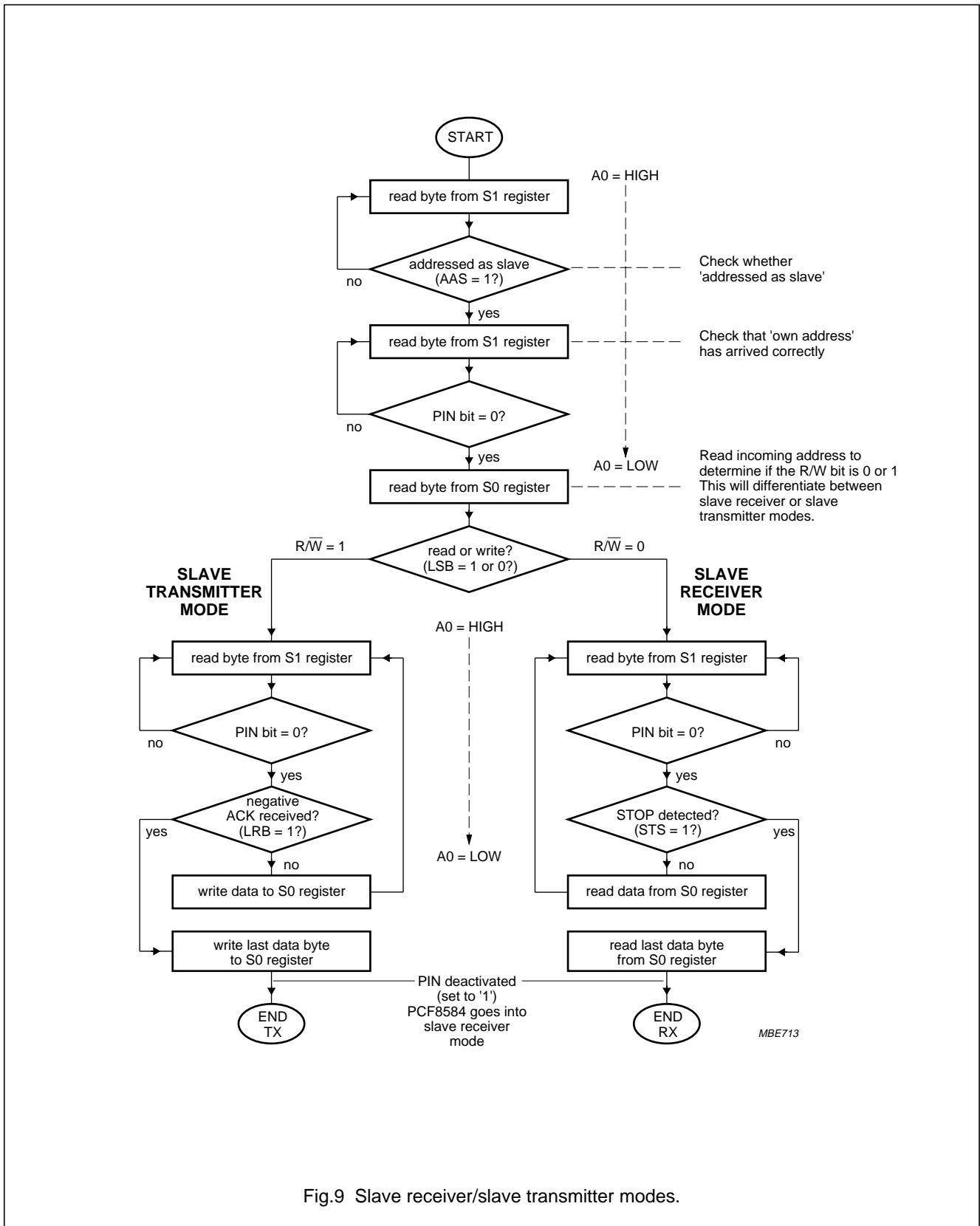


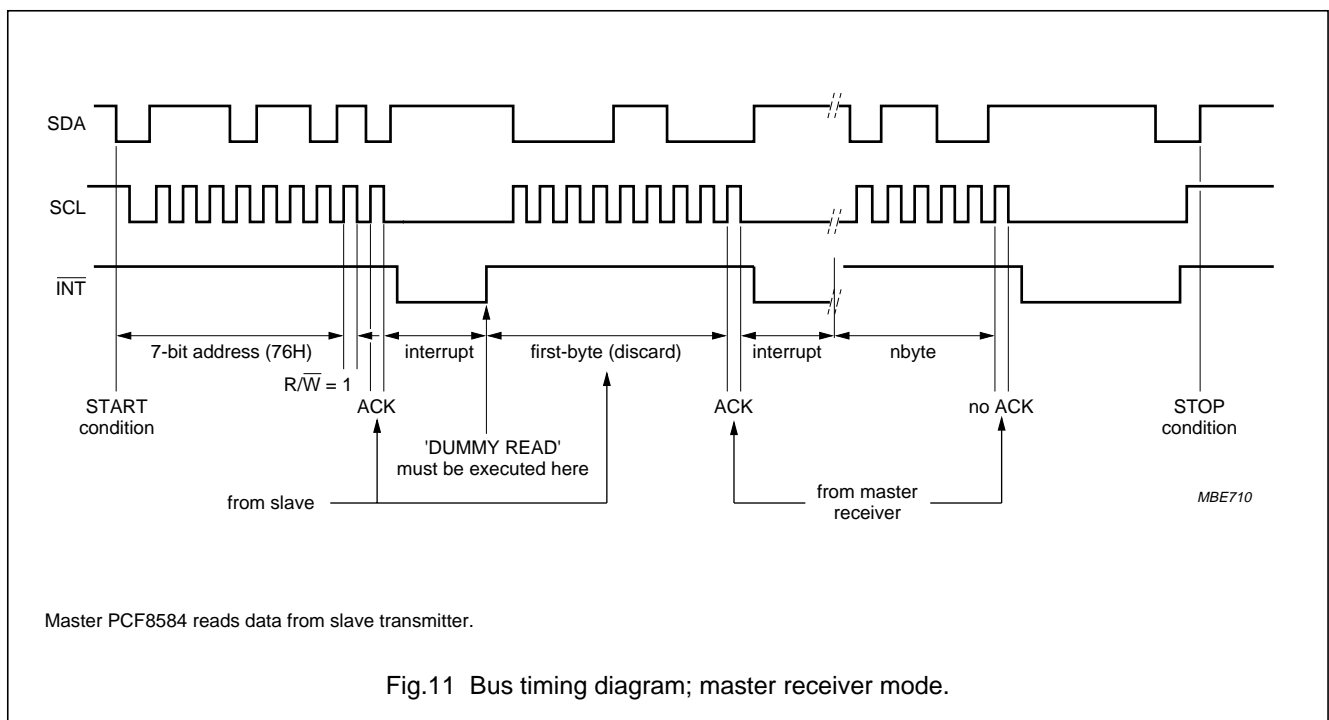
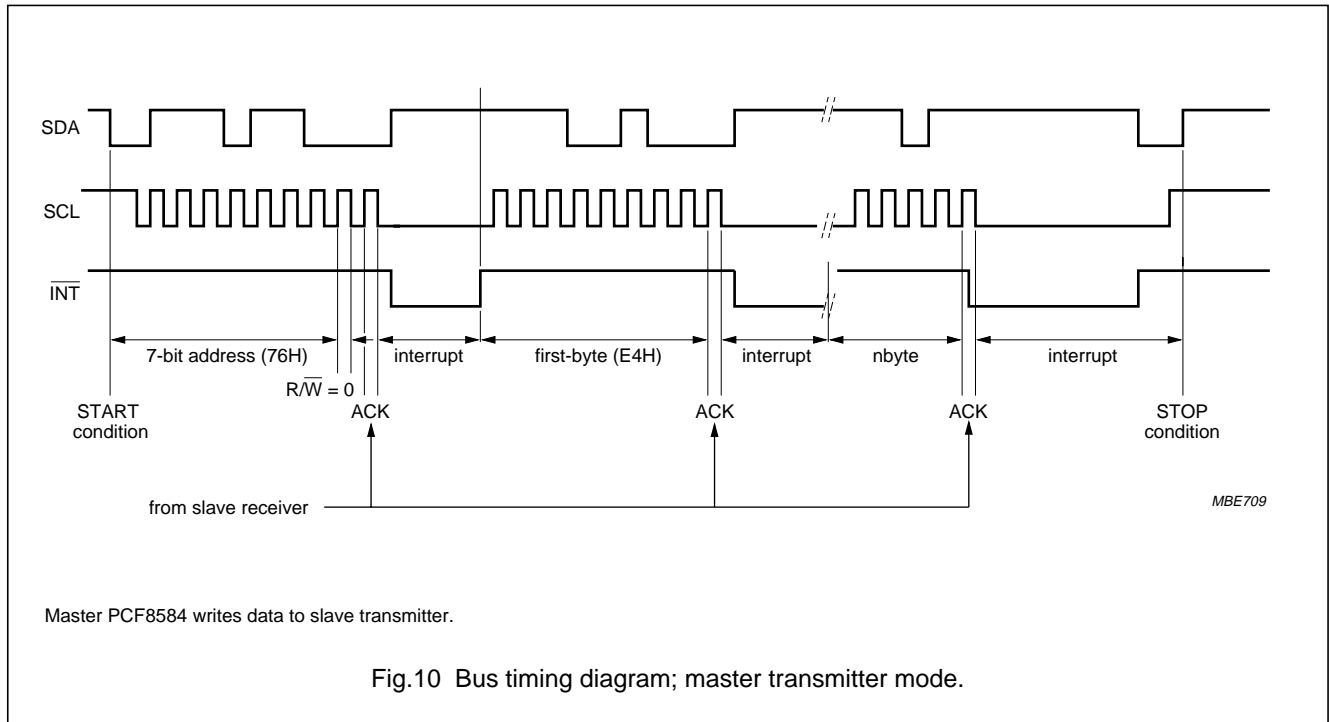
Fig.9 Slave receiver/slave transmitter modes.

I<sup>2</sup>C-bus controller

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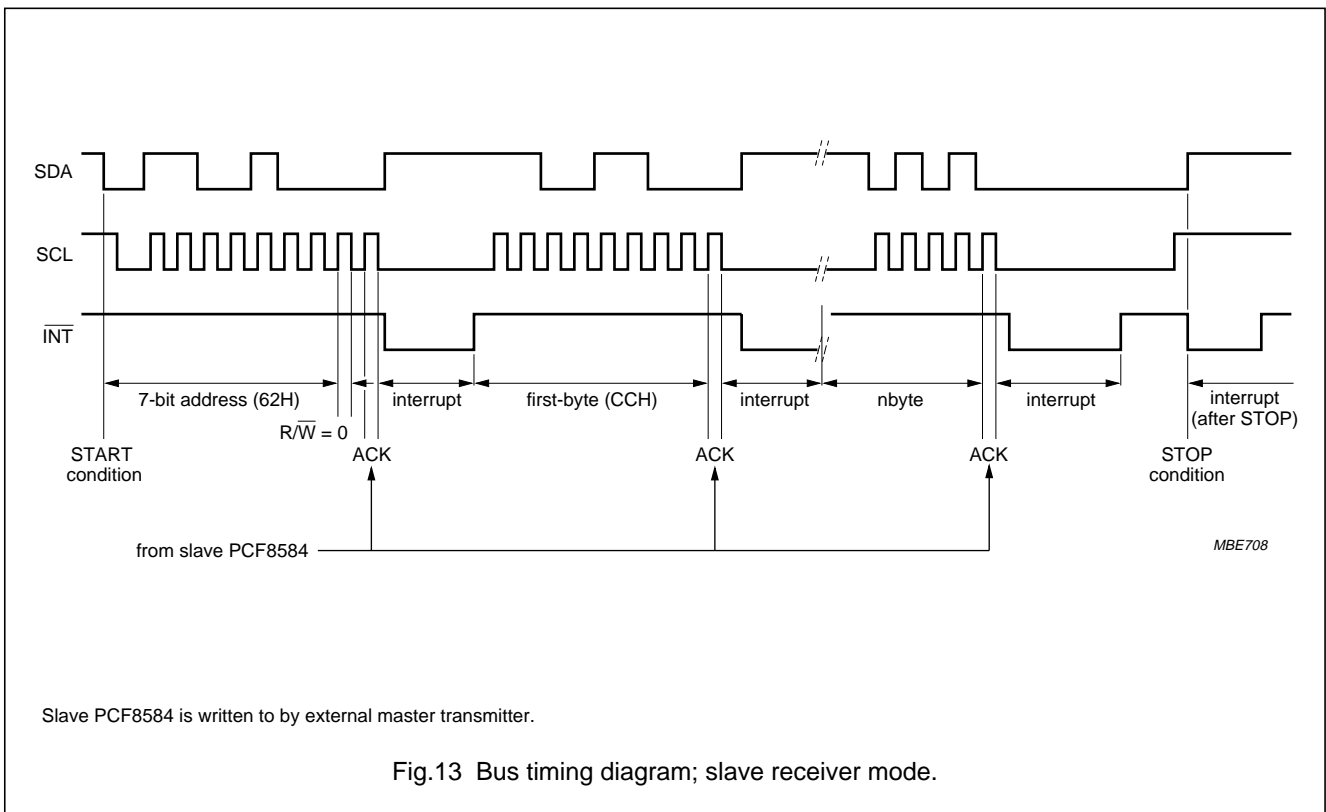
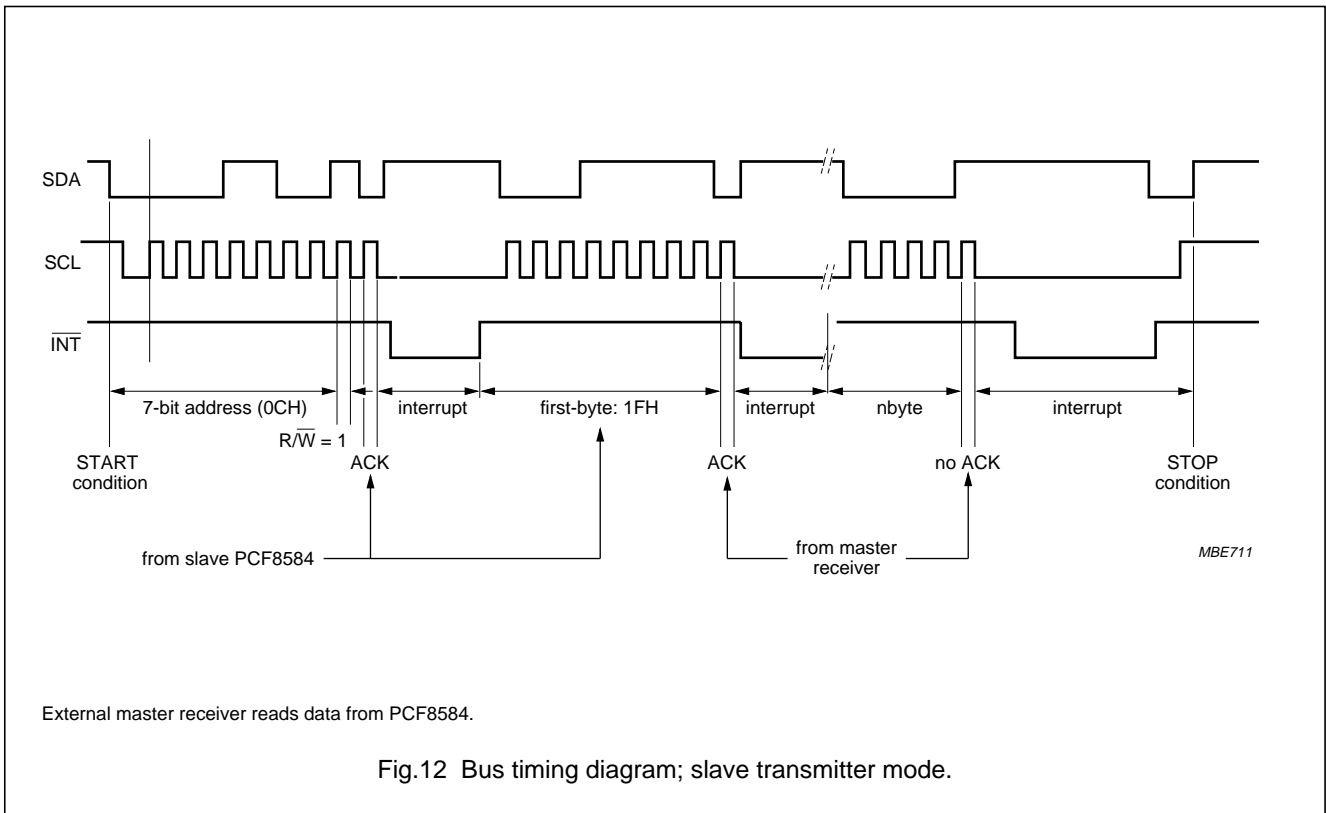
8 I<sup>2</sup>C-BUS TIMING DIAGRAMS

The diagrams (Figs 10 to 13) illustrate typical timing diagrams for the PCF8584 in master/slave functions. For detailed description of the I<sup>2</sup>C-bus protocol, please refer to "The I<sup>2</sup>C-bus and how to use it"; Philips document ordering number 9398 393 40011.



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**9 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL           | PARAMETER                      | MIN. | MAX.                  | UNIT |
|------------------|--------------------------------|------|-----------------------|------|
| V <sub>DD</sub>  | supply voltage                 | -0.3 | +7.0                  | V    |
| V <sub>I</sub>   | voltage range (any input)      | -0.8 | V <sub>DD</sub> + 0.5 | V    |
| I <sub>I</sub>   | DC input current (any input)   | -10  | +10                   | mA   |
| I <sub>O</sub>   | DC output current (any output) | -10  | +10                   | mA   |
| P <sub>tot</sub> | total power dissipation        | -    | 300                   | mW   |
| P <sub>O</sub>   | power dissipation per output   | -    | 50                    | mW   |
| T <sub>amb</sub> | operating ambient temperature  | -40  | +85                   | °C   |
| T <sub>stg</sub> | storage temperature            | -65  | +150                  | °C   |

**10 HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

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**11 DC CHARACTERISTICS** $V_{DD} = 5\text{ V} \pm 10\%$ ;  $T_{amb} = -40$  to  $+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| SYMBOL  | PARAMETER                 | CONDITIONS                                      | MIN.        | TYP. | MAX.        | UNIT             |
|---|---------------------------|---|-------------|------|-------------|------------------|
| <b>Supply</b>   |                           |   |             |      |             |                  |
| $V_{DD}$  | supply voltage            |   | 4.5         | 5.0  | 5.5         | V                |
| $I_{DD}$  | supply current            | standby; note 1                                 | –           | –    | 2.5         | $\mu\text{A}$    |
|   |                           | operating; notes 1 and 2                        | –           | –    | 1.5         | mA               |
| <b>Inputs</b>   |                           |   |             |      |             |                  |
| CLK, $\overline{\text{IACK}}$ , A0, $\overline{\text{CS}}$ , $\overline{\text{WR}}$ , $\overline{\text{RD}}$ , $\overline{\text{RESET}}$ AND D0 to D7 |                           |   |             |      |             |                  |
| $V_{IL}$  | LOW level input voltage   | note 3  | 0           | –    | 0.8         | V                |
| $V_{IH}$  | HIGH level input voltage  | note 3  | 2.0         | –    | $V_{DD}$    | V                |
| <b>SDA AND SCL</b>  |                           |   |             |      |             |                  |
| $V_{IL}$  | LOW level input voltage   | note 4  | 0           | –    | $0.3V_{DD}$ | V                |
| $V_{IH}$  | HIGH level input voltage  | note 4  | $0.7V_{DD}$ | –    | $V_{DD}$    | V                |
| $R_i$   | resistance to $V_{DD}$    | $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; note 5 | 25          | –    | 100         | $\text{k}\Omega$ |
| <b>Outputs</b>  |                           |   |             |      |             |                  |
| $I_{OH}$  | HIGH level output current | $V_{OH} = 2.4\text{ V}$ ; note 6 and 7          | –2.4        | –    | –           | mA               |
| $I_{OL}$  | LOW level output current  | $V_{OL} = 0.4\text{ V}$ ; note 6                | 3.0         | –    | –           | mA               |
| $I_{OL}$  | leakage current           | note 8  | –1          | –    | +1          | $\mu\text{A}$    |

**Notes**

1. Test conditions: 22 k $\Omega$  pull-up resistors on D0 to D7; 10 k $\Omega$  pull-up resistors on SDA, SCL,  $\overline{\text{RD}}$ ;  $\overline{\text{RESET}}$  connected to  $V_{SS}$ ; remaining pins open-circuit.
2. CLK waveform of 12 MHz with 50% duty factor.
3. CLK,  $\overline{\text{IACK}}$ , A0,  $\overline{\text{CS}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{RESET}}$  and D0 to D7 are TTL level inputs.
4. SDA and SCL are CMOS level inputs.
5. CLK,  $\overline{\text{IACK}}$ , A0,  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$ .
6. D0 to D7.
7.  $\overline{\text{DTACK}}$ ,  $\overline{\text{STROBE}}$ .
8. D0 to D7 3-state, SDA, SCL,  $\overline{\text{INT}}$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{RESET}}$ .

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**12 I<sup>2</sup>C-BUS TIMING SPECIFICATIONS**

All the timing limits are valid within the operating supply voltage and ambient temperature range;  $V_{DD} = 5\text{ V} \pm 10\%$ ;  $T_{amb} = -40$  to  $+85\text{ }^{\circ}\text{C}$ ; and refer to  $V_{IL}$  and  $V_{IH}$  with an input voltage of  $V_{SS}$  to  $V_{DD}$ .

| SYMBOL       | PARAMETER                    | MIN. | TYP. | MAX. | UNIT          |
|--------------|------------------------------|------|------|------|---------------|
| $f_{SCL}$    | SCL clock frequency          | –    | –    | 100  | kHz           |
| $t_{SW}$     | tolerable spike width on bus | –    | –    | 100  | ns            |
| $t_{BUF}$    | bus free time                | 4.7  | –    | –    | $\mu\text{s}$ |
| $t_{SU;STA}$ | START condition set-up time  | 4.7  | –    | –    | $\mu\text{s}$ |
| $t_{HD;STA}$ | START condition hold time    | 4.0  | –    | –    | $\mu\text{s}$ |
| $t_{LOW}$    | SCL LOW time                 | 4.7  | –    | –    | $\mu\text{s}$ |
| $t_{HIGH}$   | SCL HIGH time                | 4.0  | –    | –    | $\mu\text{s}$ |
| $t_r$        | SCL and SDA rise time        | –    | –    | 1.0  | $\mu\text{s}$ |
| $t_f$        | SCL and SDA fall time        | –    | –    | 0.3  | $\mu\text{s}$ |
| $t_{SU;DAT}$ | data set-up time             | 250  | –    | –    | ns            |
| $t_{HD;DAT}$ | data hold time               | 0    | –    | –    | ns            |
| $t_{VD;DAT}$ | SCL LOW to data out valid    | –    | –    | 3.4  | $\mu\text{s}$ |
| $t_{SU;STO}$ | STOP condition set-up time   | 4.0  | –    | –    | $\mu\text{s}$ |

**13 PARALLEL INTERFACE TIMING**

All the timing limits are valid within the operating supply voltage and ambient temperature range:  $V_{DD} = 5\text{ V} \pm 10\%$ ;  $T_{amb} = -40$  to  $+85\text{ }^{\circ}\text{C}$ ; and refer to  $V_{IL}$  and  $V_{IH}$  with an input voltage of  $V_{SS}$  to  $V_{DD}$ .  $C_L = 100\text{ pF}$ ;  $R_L = 1.5\text{ k}\Omega$  (connected to  $V_{DD}$ ) for open-drain and high-impedance outputs, where applicable (for measurement purposes only).

| SYMBOL     | PARAMETER   | CONDITIONS            | MIN. | TYP. | MAX. | UNIT |
|------------|---|-----------------------|------|------|------|------|
| $t_r$      | clock rise time                                   | see Fig.14            | –    | –    | 6    | ns   |
| $t_f$      | clock fall time                                   | see Fig.14            | –    | –    | 6    | ns   |
| $t_{CLK}$  | input clock period<br>(50% $\pm 5\%$ duty factor) | see Fig.14            | 83   | –    | 333  | ns   |
| $t_{CLRL}$ | $\overline{CS}$ set-up to $\overline{RD}$ LOW     | see Fig.16 and note 1 | 20   | –    | –    | ns   |
| $t_{CLWL}$ | $\overline{CS}$ set-up to $\overline{WR}$ LOW     | see Fig.15 and note 1 | 20   | –    | –    | ns   |
| $t_{RHCH}$ | $\overline{CS}$ hold from $\overline{RD}$ HIGH    | see Fig.16            | 0    | –    | –    | ns   |
| $t_{WHCH}$ | $\overline{CS}$ hold from $\overline{WR}$ HIGH    | see Fig.15            | 0    | –    | –    | ns   |
| $t_{AVWL}$ | A0 set-up to $\overline{WR}$ LOW                  | see Fig.15            | 10   | –    | –    | ns   |
| $t_{AVRL}$ | A0 set-up to $\overline{RD}$ LOW                  | see Fig.16            | 10   | –    | –    | ns   |
| $t_{WHAI}$ | A0 hold from $\overline{WR}$ HIGH                 | see Fig.15            | 20   | –    | –    | ns   |
| $t_{RHAI}$ | A0 hold from $\overline{RD}$ HIGH                 | see Fig.16            | 10   | –    | –    | ns   |
| $t_{WLWH}$ | $\overline{WR}$ pulse width                       | see Fig.15            | 230  | –    | 1000 | ns   |
| $t_{RLRH}$ | $\overline{RD}$ pulse width                       | see Fig.16            | 230  | –    | 1000 | ns   |
| $t_{DVWH}$ | data set-up before $\overline{WR}$ HIGH           | see Fig.15            | 150  | –    | –    | ns   |
| $t_{RLDV}$ | data valid after $\overline{RD}$ LOW              | see Fig.16            | –    | 160  | 180  | ns   |
| $t_{WHDI}$ | data hold after $\overline{WR}$ HIGH              | see Fig.15            | 20   | –    | –    | ns   |
| $t_{RHDF}$ | data bus floating after $\overline{RD}$<br>HIGH   | see Fig.16            | –    | –    | 150  | ns   |



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| SYMBOL            | PARAMETER   | CONDITIONS            | MIN.               | TYP.                                  | MAX.                    | UNIT |
|-------------------|---|-----------------------|--------------------|---------------------------------------|-------------------------|------|
| t <sub>AVCL</sub> | A0 set-up to $\overline{CS}$ LOW                            | see Figs 17 and 18    | 10                 | –                                     | –                       | ns   |
| t <sub>WLCL</sub> | R/ $\overline{WR}$ set-up to $\overline{CS}$ LOW            | see Fig.17            | 10                 | –                                     | –                       | ns   |
| t <sub>RHCL</sub> | $\overline{R}/\overline{WR}$ set-up to $\overline{CS}$ LOW  | see Fig.18            | 10                 | –                                     | –                       | ns   |
| t <sub>CLDV</sub> | data valid after $\overline{CS}$ LOW                        | see Fig.18 and note 2 | –                  | 160                                   | 180                     | ns   |
| t <sub>CLDL</sub> | $\overline{DTACK}$ LOW after $\overline{CS}$ LOW            | see Figs 17 and 18    | –                  | 2t <sub>CLK</sub> + 75                | 3t <sub>CLK</sub> + 150 | ns   |
| t <sub>CHAI</sub> | A0 hold from $\overline{CS}$ HIGH                           | see Fig.18            | 0                  | –                                     | –                       | ns   |
| t <sub>CHRL</sub> | R/ $\overline{WR}$ hold from $\overline{CS}$ HIGH           | see Fig.18            | 0                  | –                                     | –                       | ns   |
| t <sub>CHWH</sub> | $\overline{R}/\overline{WR}$ hold from $\overline{CS}$ HIGH | see Fig.17            | 0                  | –                                     | –                       | ns   |
| t <sub>CHDF</sub> | data bus float after $\overline{CS}$ HIGH                   | see Fig.18            | –                  | –                                     | 150                     | ns   |
| t <sub>CHDE</sub> | $\overline{DTACK}$ HIGH from $\overline{CS}$ HIGH           | see Figs 17 and 18    | –                  | 100                                   | 120                     | ns   |
| t <sub>CHDI</sub> | data hold after $\overline{CS}$ HIGH                        | see Fig.17            | 0                  | –                                     | –                       | ns   |
| t <sub>DVCL</sub> | data set-up to $\overline{CS}$ LOW                          | see Fig.17            | 0                  | –                                     | –                       | ns   |
| t <sub>ALIE</sub> | $\overline{INT}$ HIGH from $\overline{IACK}$ LOW            | see Figs 19 and 20    | –                  | 130                                   | 180                     | ns   |
| t <sub>ALDV</sub> | data valid after $\overline{IACK}$ LOW                      | see Figs 19 and 20    | –                  | 200                                   | 250                     | ns   |
| t <sub>ALAE</sub> | $\overline{IACK}$ pulse width                               | see Fig.20            | 230                | –                                     | –                       | ns   |
| t <sub>AHDI</sub> | data hold after $\overline{IACK}$ HIGH                      | see Fig.20            | –                  | –                                     | 30                      | ns   |
| t <sub>ALDL</sub> | $\overline{DTACK}$ LOW from $\overline{IACK}$ LOW           | see Fig.20            | –                  | 2t <sub>CLK</sub> + 75                | 3t <sub>CLK</sub> + 150 | ns   |
| t <sub>AHDE</sub> | $\overline{DTACK}$ HIGH from $\overline{IACK}$ HIGH         | see Fig.20            | –                  | 120                                   | 140                     | ns   |
| t <sub>W4</sub>   | $\overline{RESET}$ pulse width                              | see Fig.21            | 30t <sub>CLK</sub> | –                                     | –                       | ns   |
| t <sub>W5</sub>   | $\overline{STROBE}$ pulse width                             | see Fig.22            | 8t <sub>CLK</sub>  | 8t <sub>CLK</sub> + 90                | –                       | ns   |
| t <sub>CLCL</sub> | $\overline{CS}$ LOW   | see Figs 17 and 18    | –                  | t <sub>CLDL</sub> + t <sub>CHDE</sub> | –                       | ns   |

**Notes**

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses when the I<sup>2</sup>C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. Not for S1.

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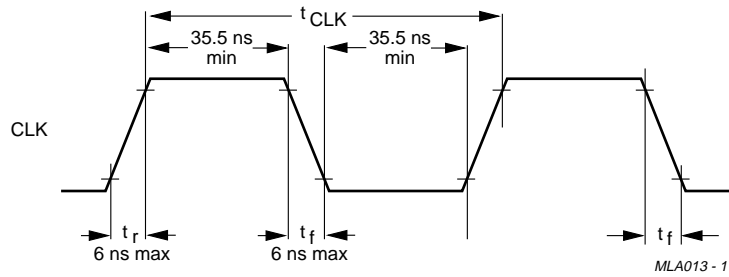


Fig.14 Clock input timing.

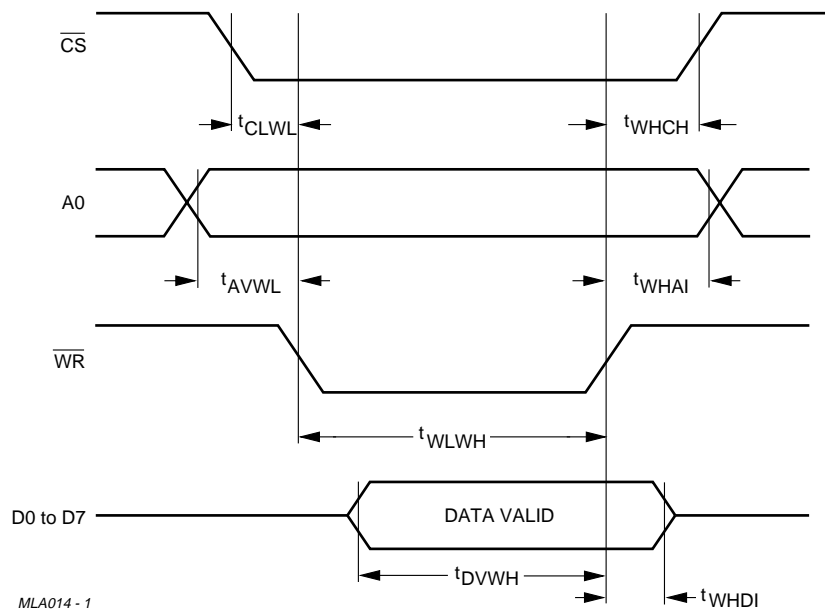


Fig.15 Bus timing (80XX mode); write cycle.

I<sup>2</sup>C-bus controller

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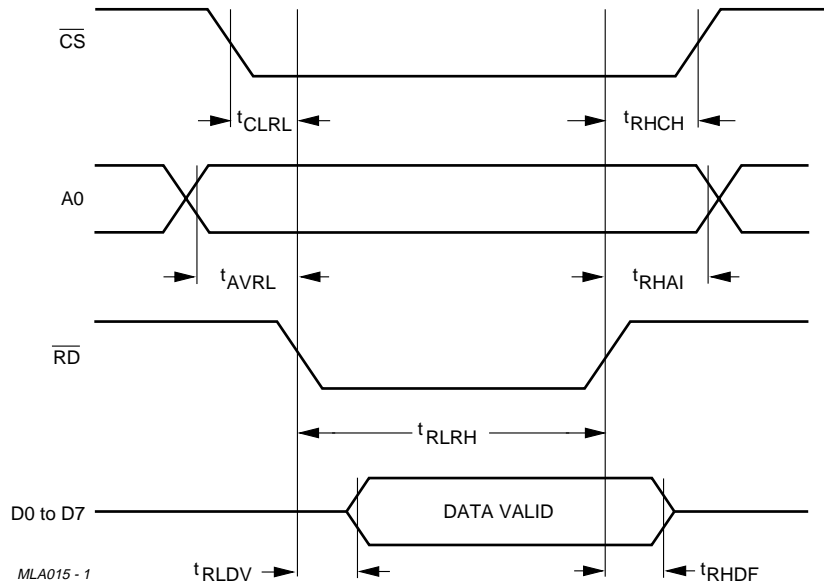


Fig.16 Bus timing (80XX mode); read cycle.

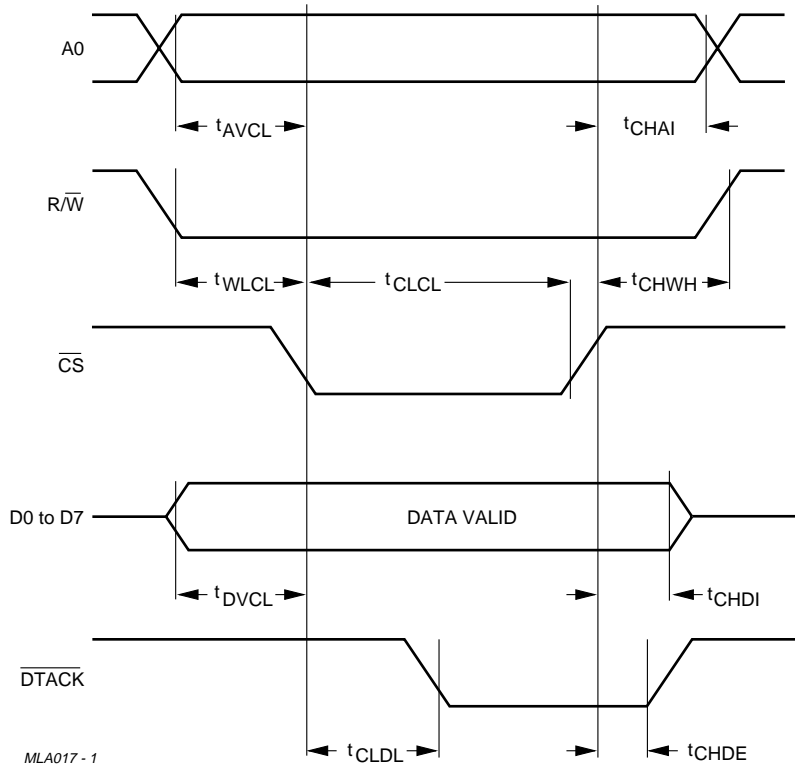
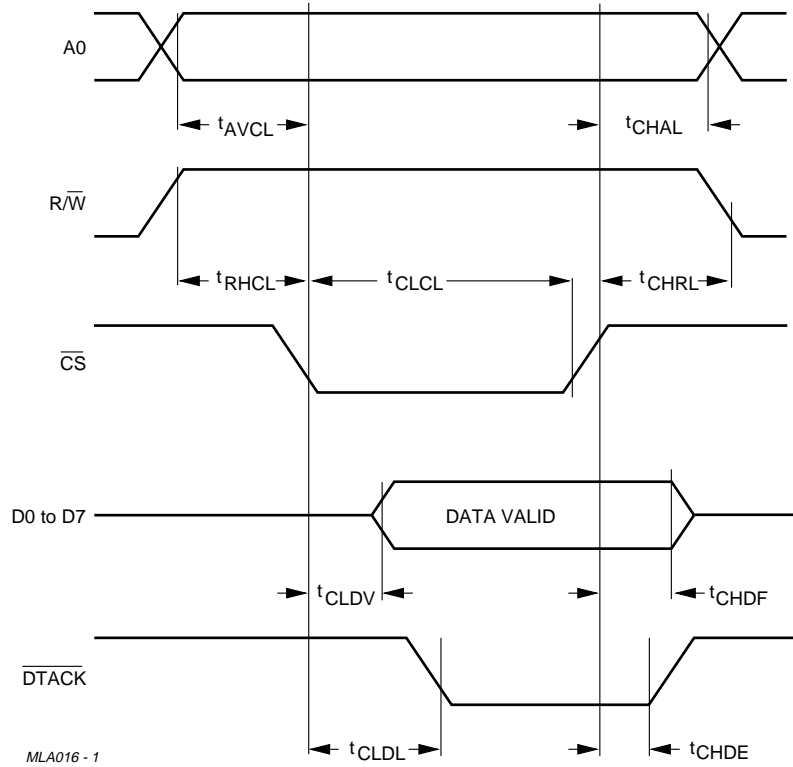


Fig.17 Bus timing (68000 mode); write cycle.

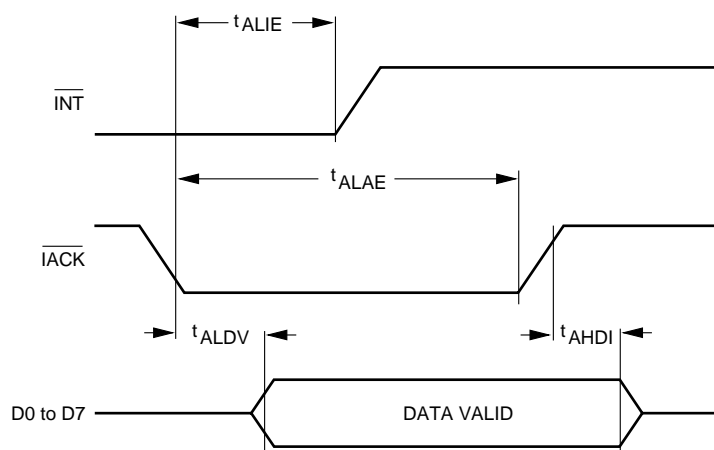
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MLA016 - 1

Fig.18 Bus timing (68000 mode); read cycle.



MLA018 - 1

Fig.19 Interrupt timing (80XX mode).

I<sup>2</sup>C-bus controller

PCF8584

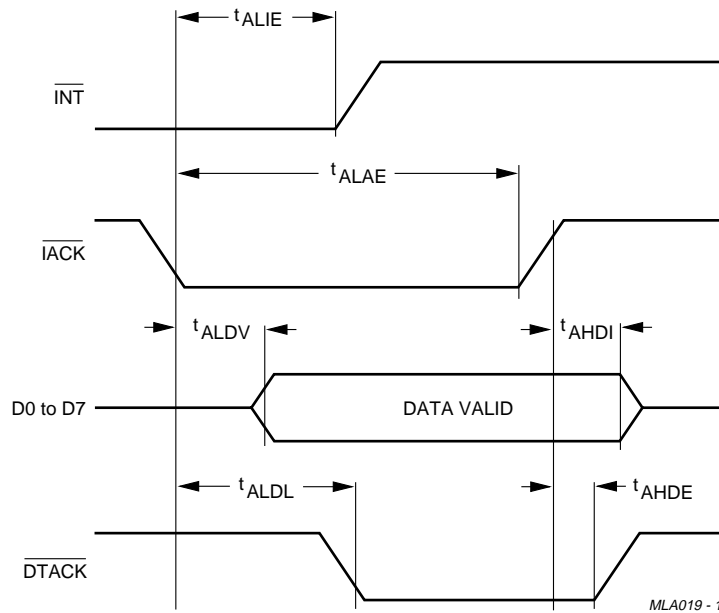


Fig.20 Interrupt timing (68000 mode).

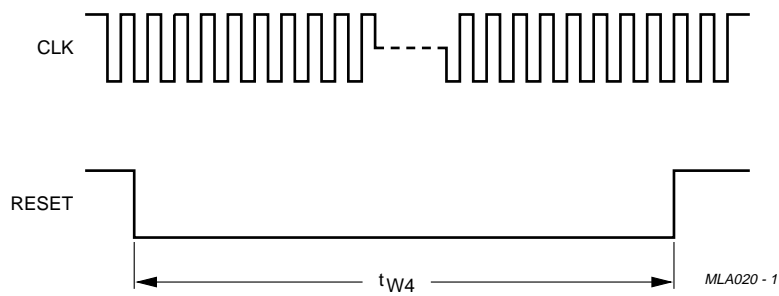


Fig.21 Reset timing.

I<sup>2</sup>C-bus controller

PCF8584

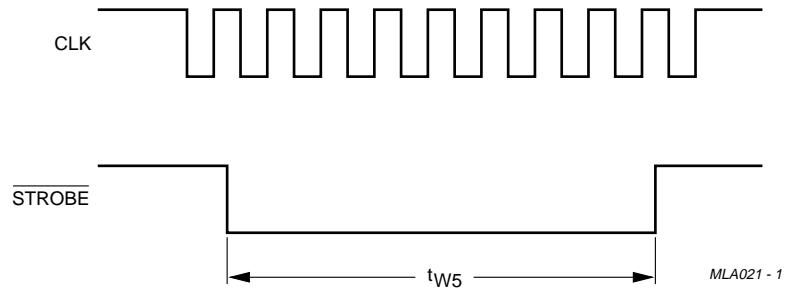


Fig.22 Strobe timing.

I<sup>2</sup>C-bus controller

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14 APPLICATION INFORMATION

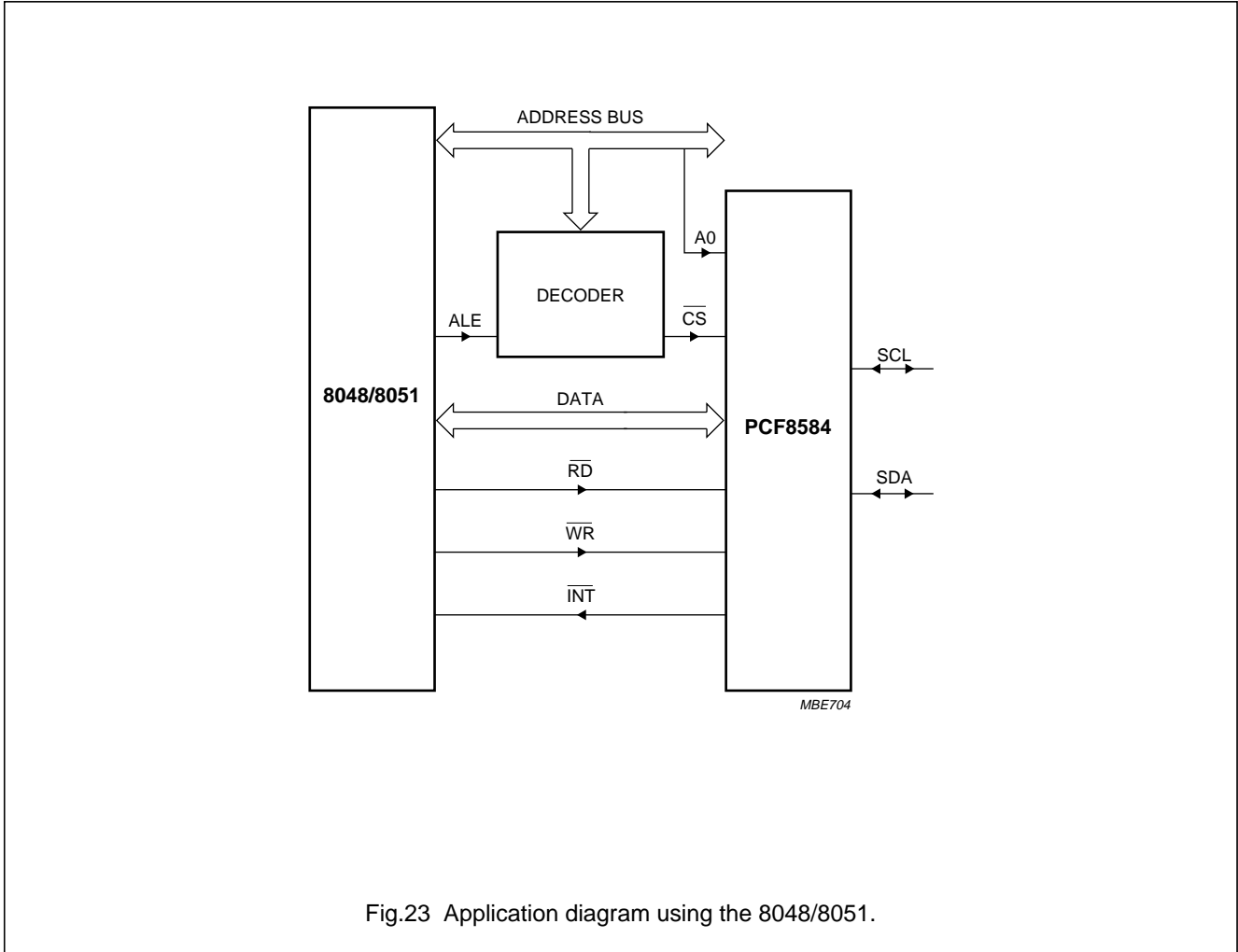


Fig.23 Application diagram using the 8048/8051.

I<sup>2</sup>C-bus controller

PCF8584

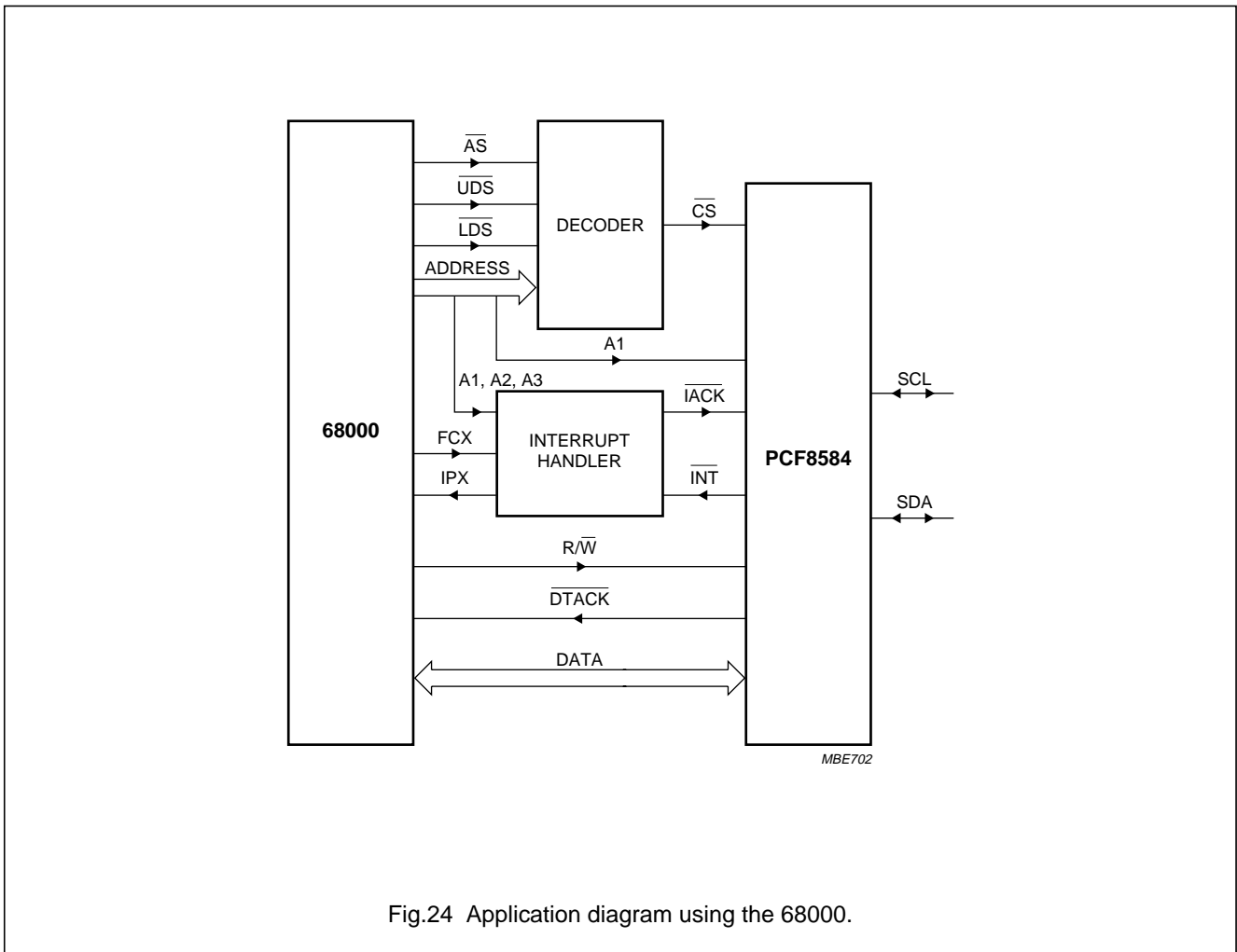
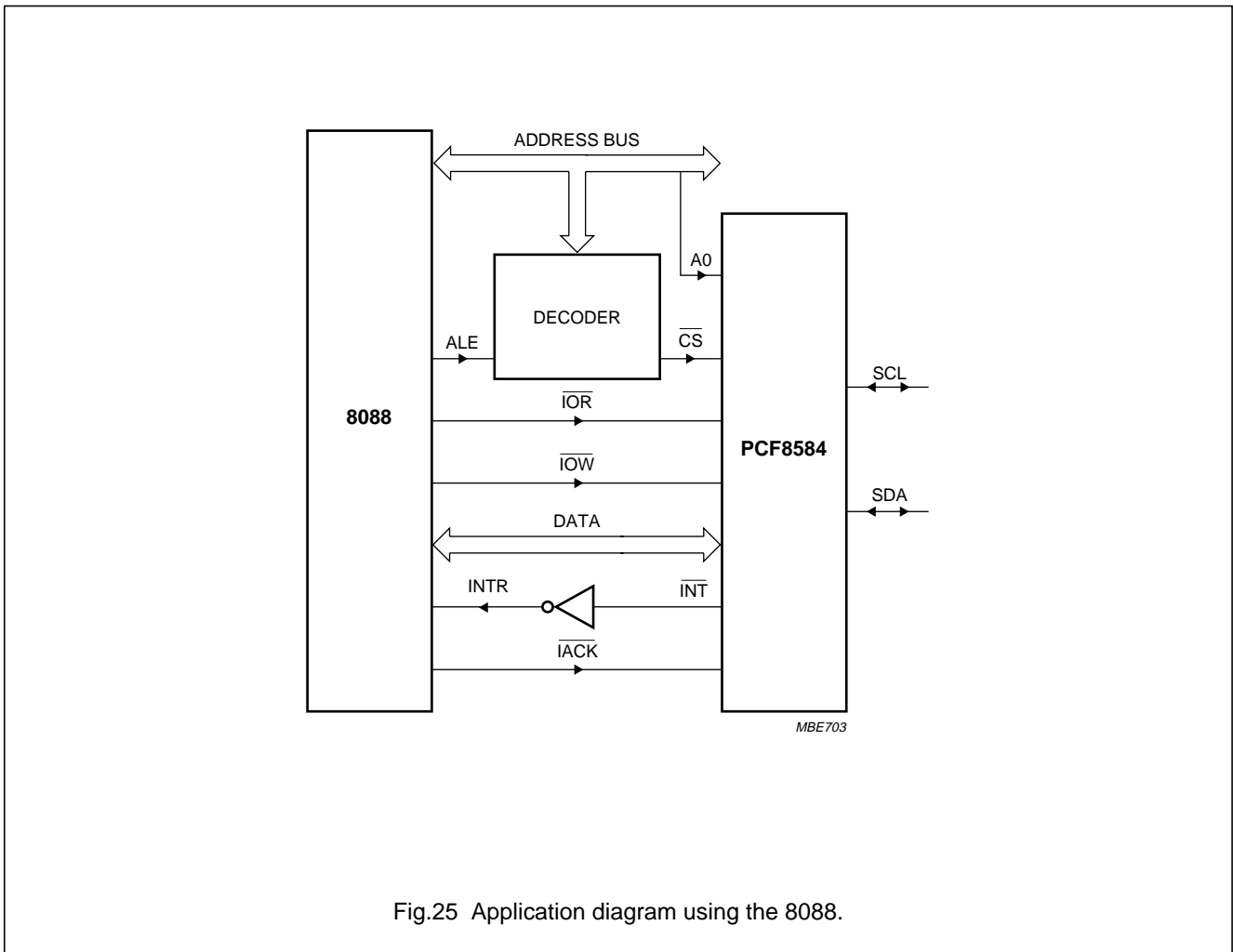


Fig.24 Application diagram using the 68000.



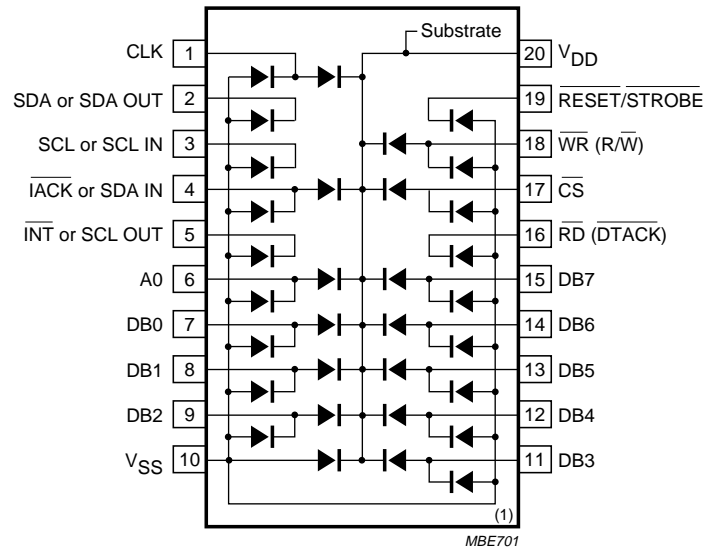
I<sup>2</sup>C-bus controller

PCF8584



I<sup>2</sup>C-bus controller

PCF8584



Maximum forward current: 5 mA; maximum reverse voltage: 5 V.

Fig.26 PCF8584 diode protection.

14.1 Application notes

Additional application notes are available from Philips Semiconductors:

1. AN95068: "C Routines for the PCF8584".
2. AN96040: "Using the PCF8584 with non-specified timings and other frequently asked questions".
3. AN90001: "Interfacing PCF8584 I<sup>2</sup>C-bus controller to 80(C)51 family of microcontrollers".

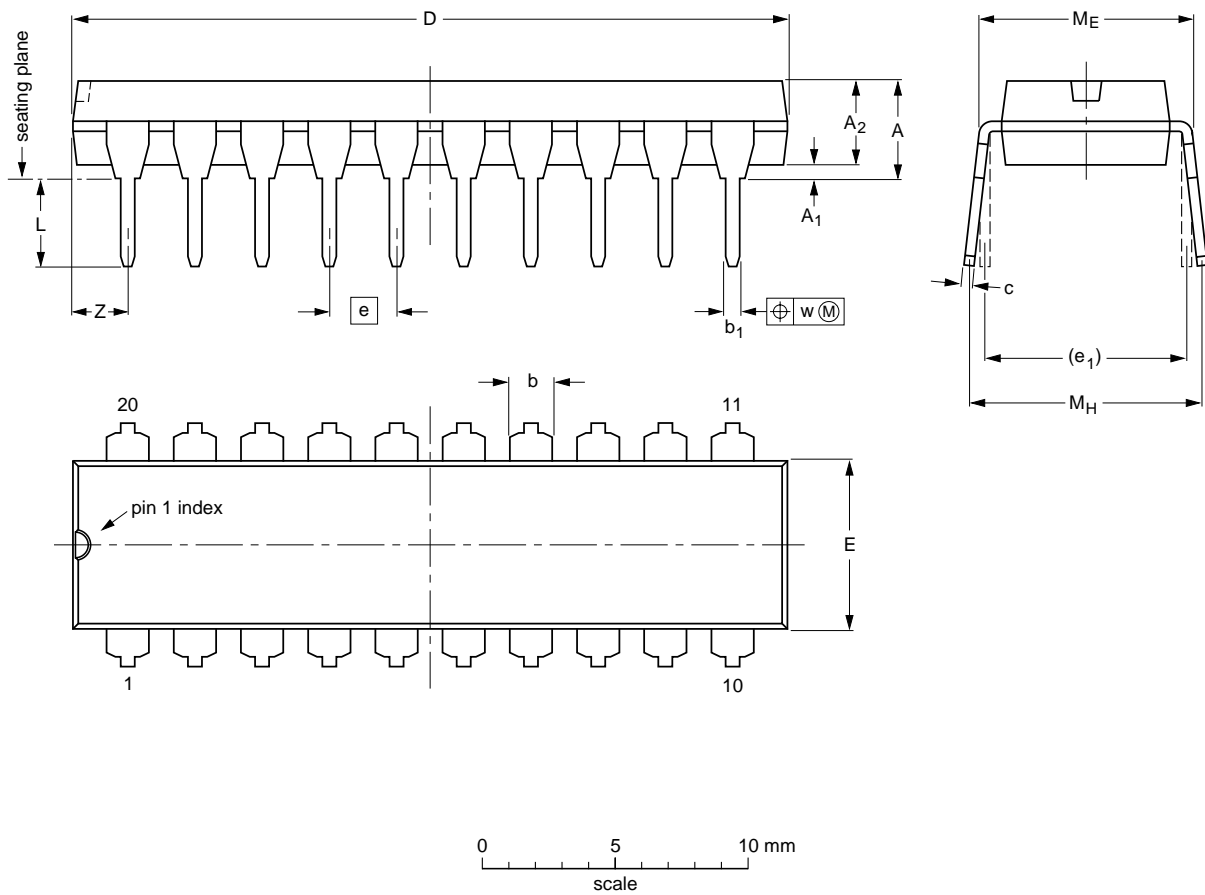
I<sup>2</sup>C-bus controller

PCF8584

15 PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm     | 4.2    | 0.51                | 3.2                 | 1.73<br>1.30   | 0.53<br>0.38   | 0.36<br>0.23   | 26.92<br>26.54   | 6.40<br>6.22     | 2.54 | 7.62           | 3.60<br>3.05 | 8.25<br>7.80   | 10.0<br>8.3    | 0.254 | 2.0                   |
| inches | 0.17   | 0.020               | 0.13                | 0.068<br>0.051 | 0.021<br>0.015 | 0.014<br>0.009 | 1.060<br>1.045   | 0.25<br>0.24     | 0.10 | 0.30           | 0.14<br>0.12 | 0.32<br>0.31   | 0.39<br>0.33   | 0.01  | 0.078                 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

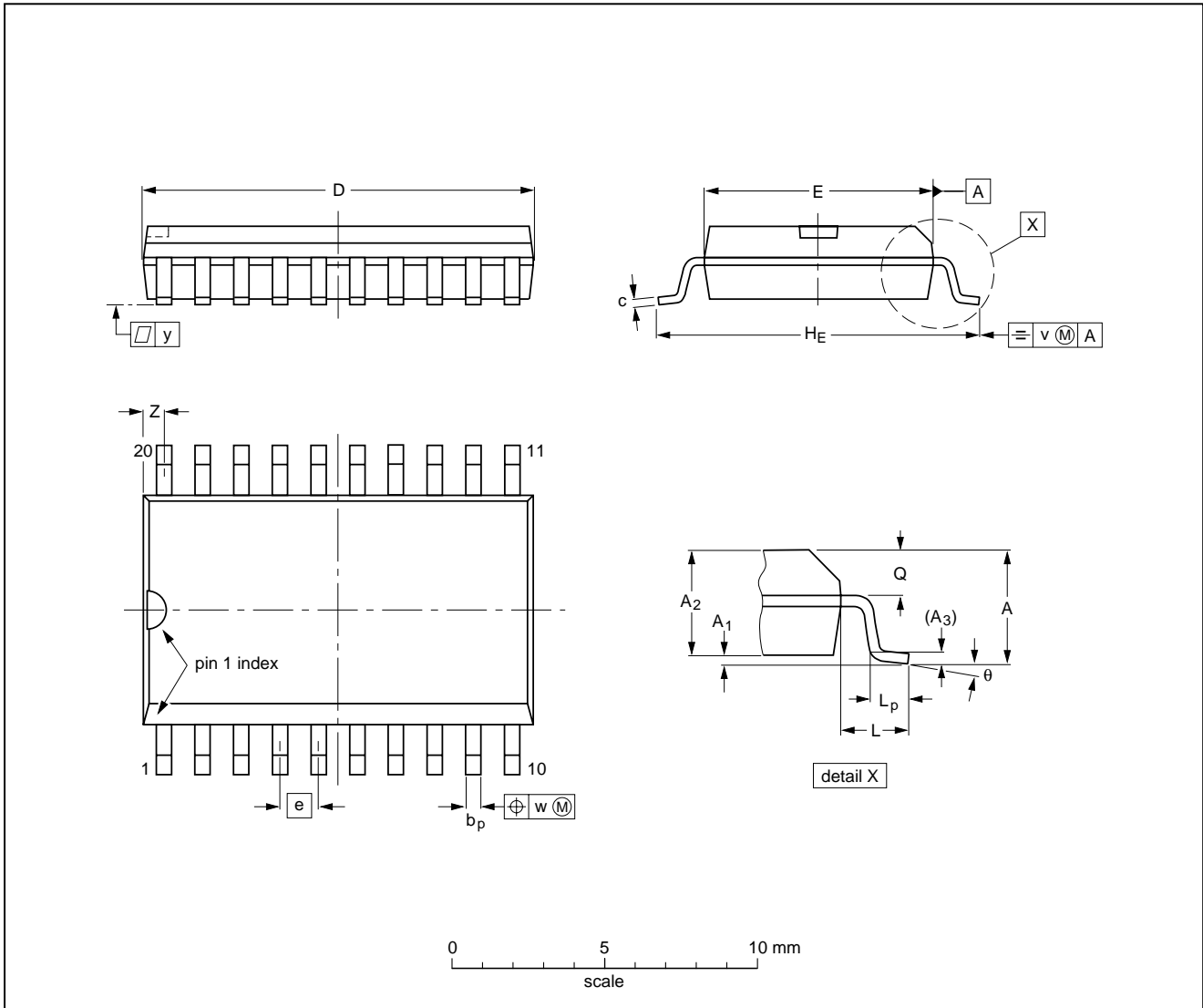
| OUTLINE VERSION | REFERENCES |       |       |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|-------|-------|--|---------------------|----------------------|
|                 | IEC        | JEDEC | EIAJ  |  |                     |                      |
| SOT146-1        |            |       | SC603 |  |                     | 92-11-17<br>95-05-24 |

I<sup>2</sup>C-bus controller

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.30<br>0.10   | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 13.0<br>12.6     | 7.6<br>7.4       | 1.27  | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.10   | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49     | 0.30<br>0.29     | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |                     |                      |
| SOT163-1        | 075E04     | MS-013AC |      |                     | 95-01-24<br>97-05-22 |

## I<sup>2</sup>C-bus controller

## PCF8584

### 16 SOLDERING

#### 16.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### 16.2 DIP

##### 16.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### 16.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### 16.3 SO

##### 16.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### 16.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### 16.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

# I<sup>2</sup>C-bus controller

# PCF8584

## 17 DEFINITIONS

|   |   |
|---|---|
| <b>Data sheet status</b>  |   |
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

## 18 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

## 19 PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

I<sup>2</sup>C-bus controller

PCF8584

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**NOTES**

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