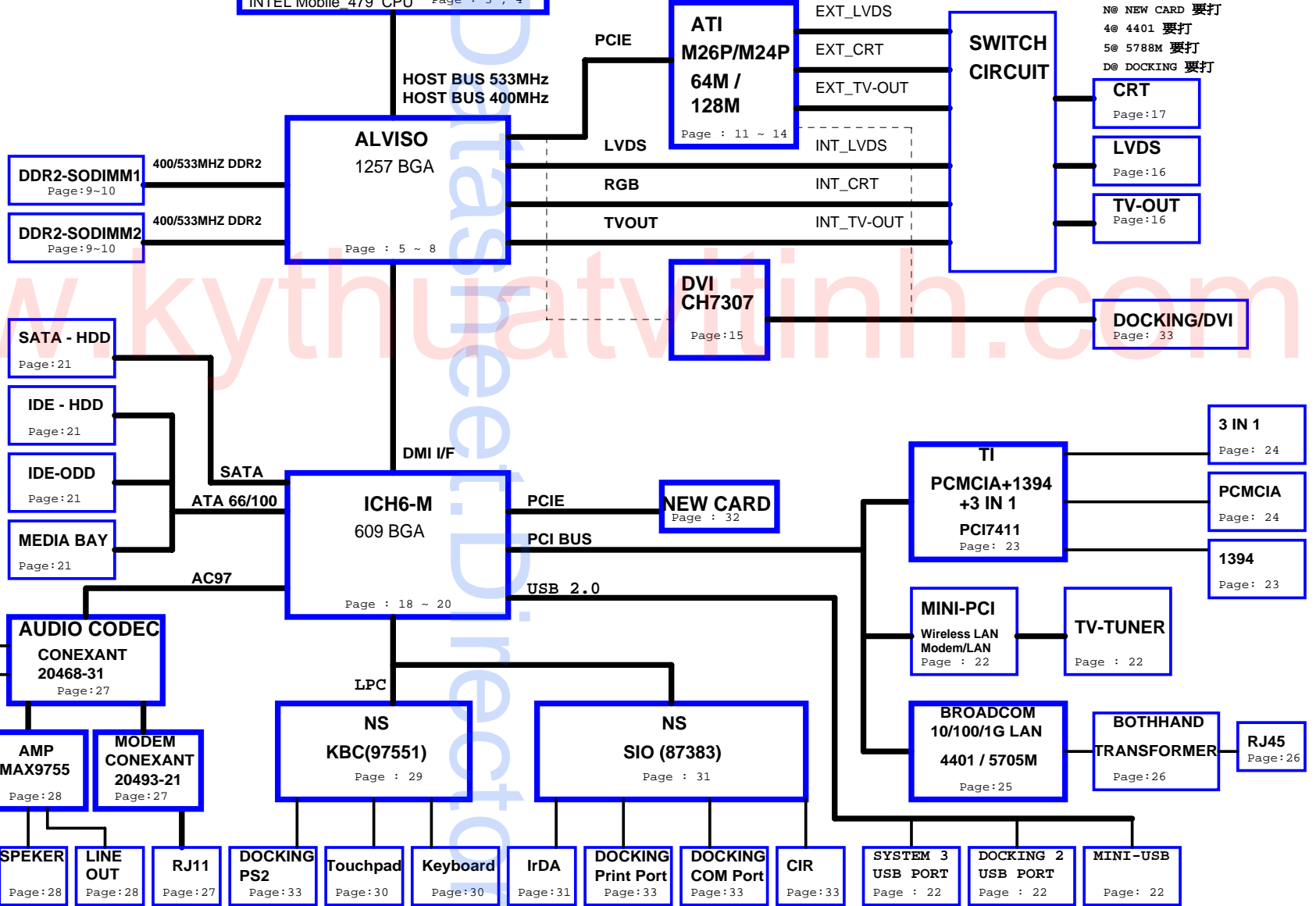


CRANE3 (ZL7)

- BOM MARK
- ED@ INT. VGA WITH DOCK
 - ID@ INT. VGA WITH DOCK
 - ND@ W/O DOCKING要打
 - E@ EXT VGA 要打
 - I@ INTVGA 要打
 - SA@ SATA 要打
 - F@ FIXED ODD要打
 - SW@ SWAPPABLE ODD 要打
 - 3@ 3in1 要打
 - N@ NEW CARD 要打
 - 4@ 4401 要打
 - 5@ 5788M 要打
 - D@ DOCKING 要打



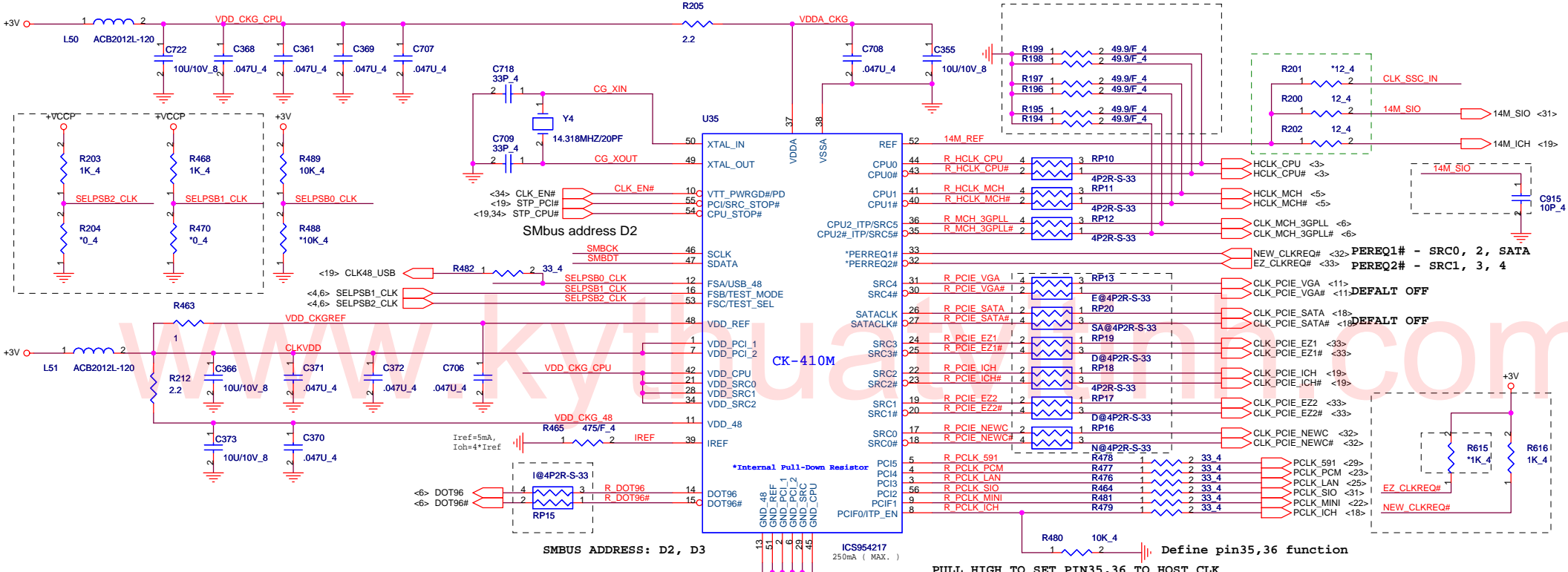
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD24	INTA#	BROADCOM LAN
REQ2# / GNT2#	AD19	INTB# , INTD#	MINI-PCI
REQ1# / GNT1#	AD17	INTC# , INTD# , INTA#	TI 7411
REQ3# / GNT3#	AD18	INTB# , INTD#	MINI-PCI (TV Tuner)

REV.C

PROJECT : ZL7
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	C
Date:	Thursday, June 23, 2005	Sheet 1 of 40

Place these termination to close CK410M.

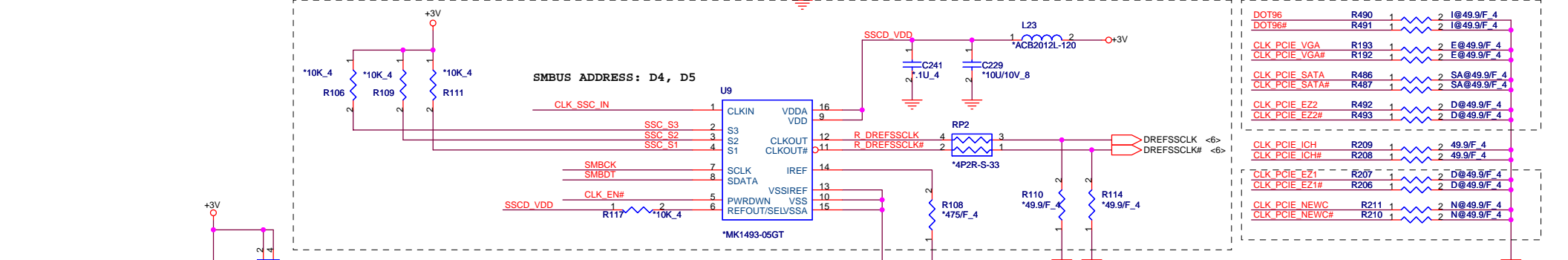


Smbus address D2

SMBUS ADDRESS: D2, D3

CK-410M

Define pin35,36 function
PULL HIGH TO SET PIN35,36 TO HOST CLK



DOTHAN-A 400
DOTHAN-A 533

	FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33	
0	0	1	133	100	33	
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RSVD	100	33	

Place these termination to close CK410M.

QUANTA COMPUTER

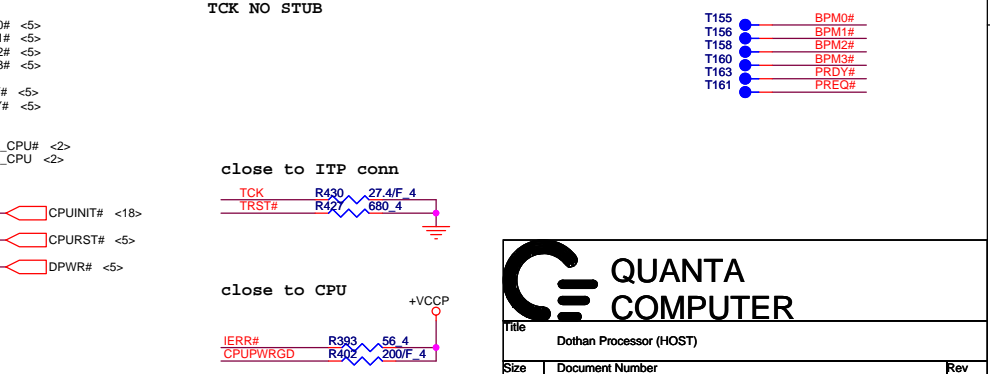
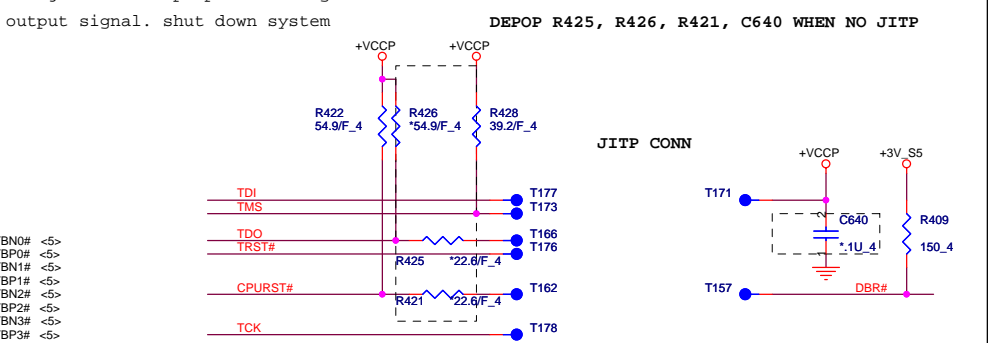
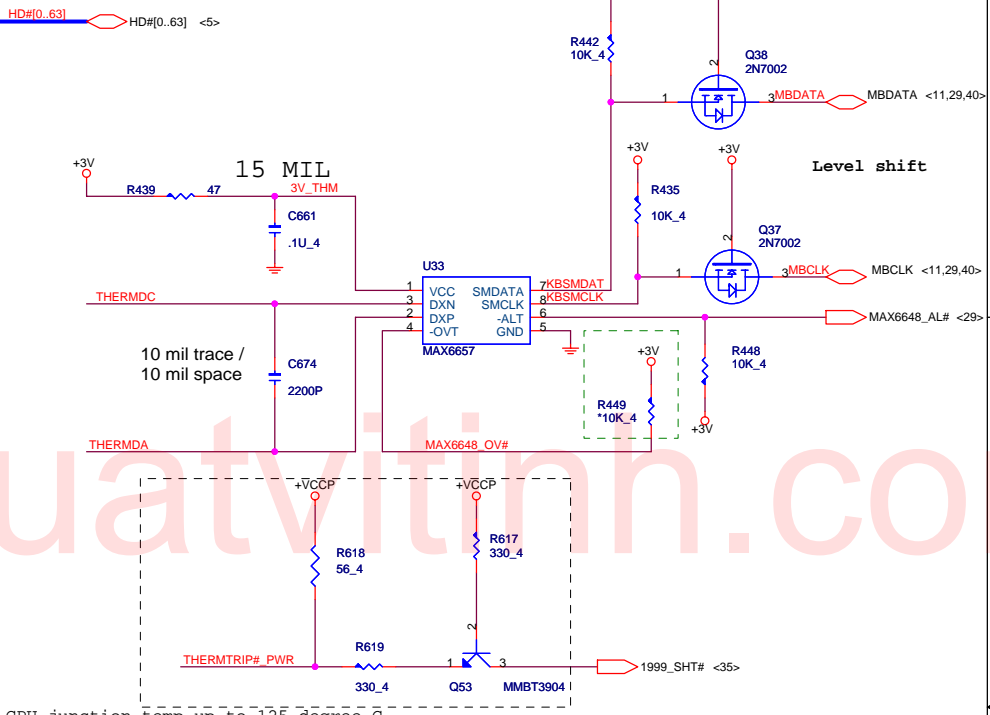
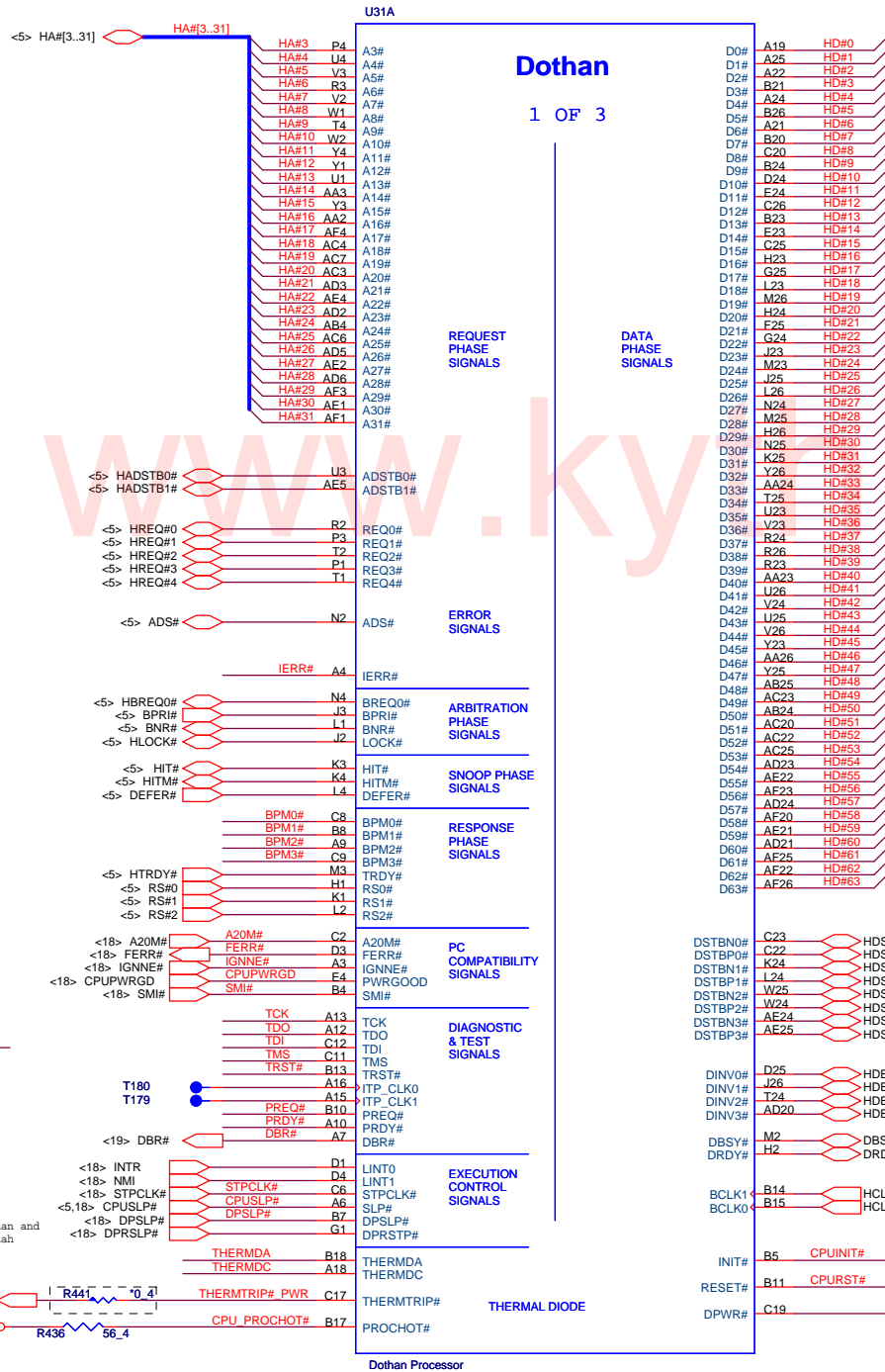
Title: CLOCK GENERATOR

Size: Document Number ZL7

Date: Thursday, June 23, 2005

Sheet 2 of 40

Rev C

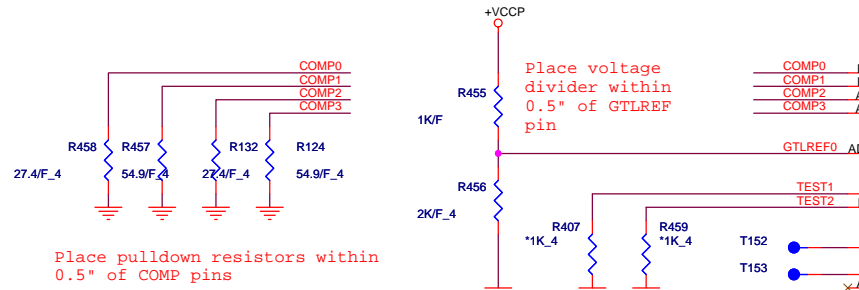


QUANTA COMPUTER

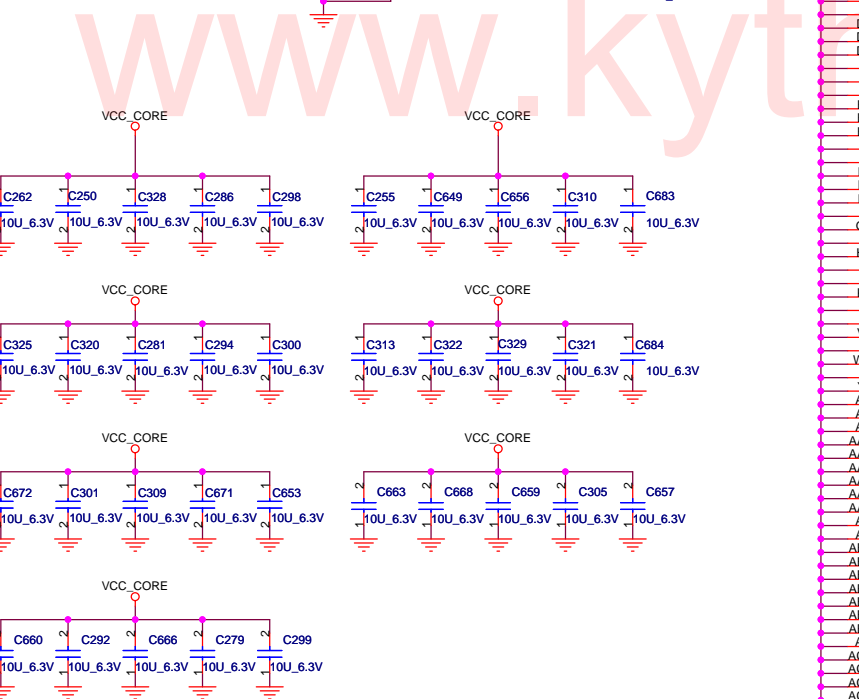
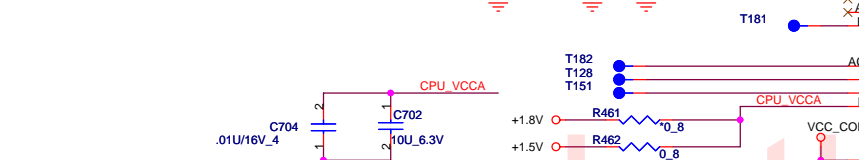
Title: Dothan Processor (HOST)

Size: Document Number ZL7

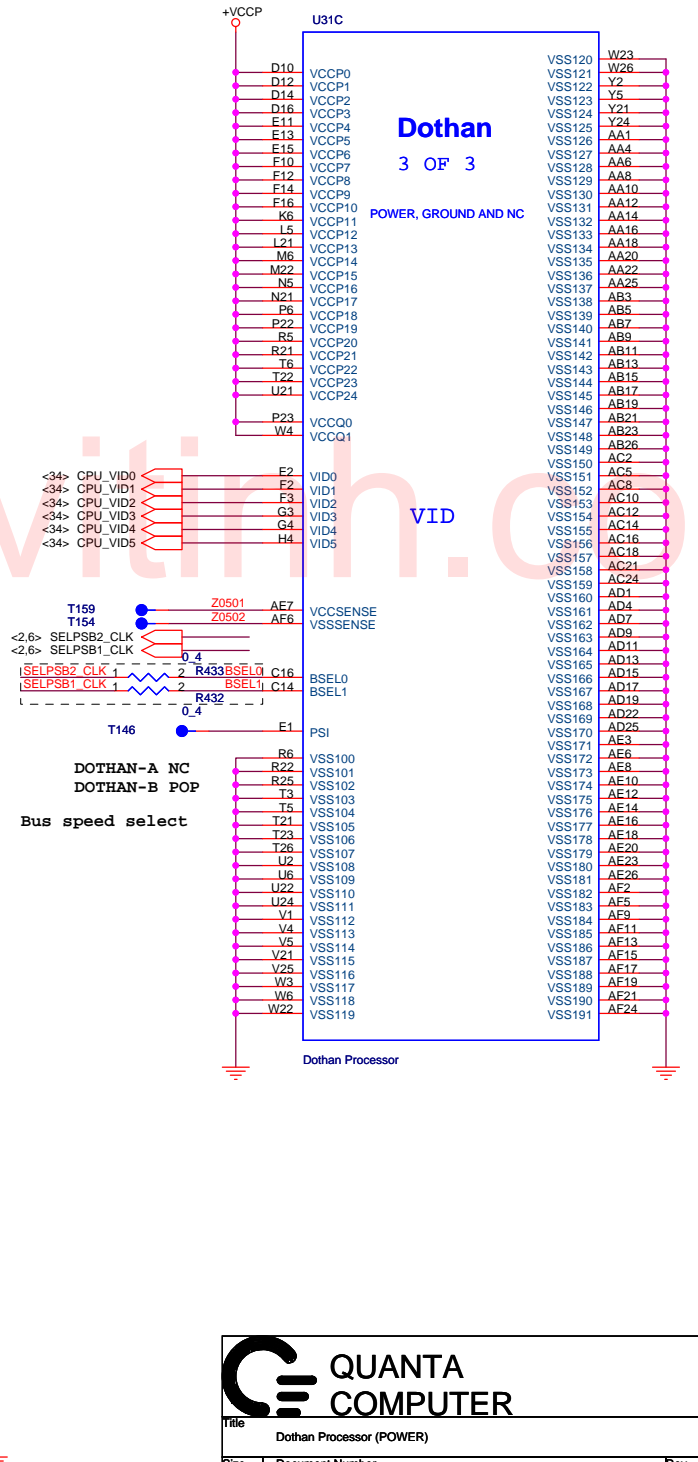
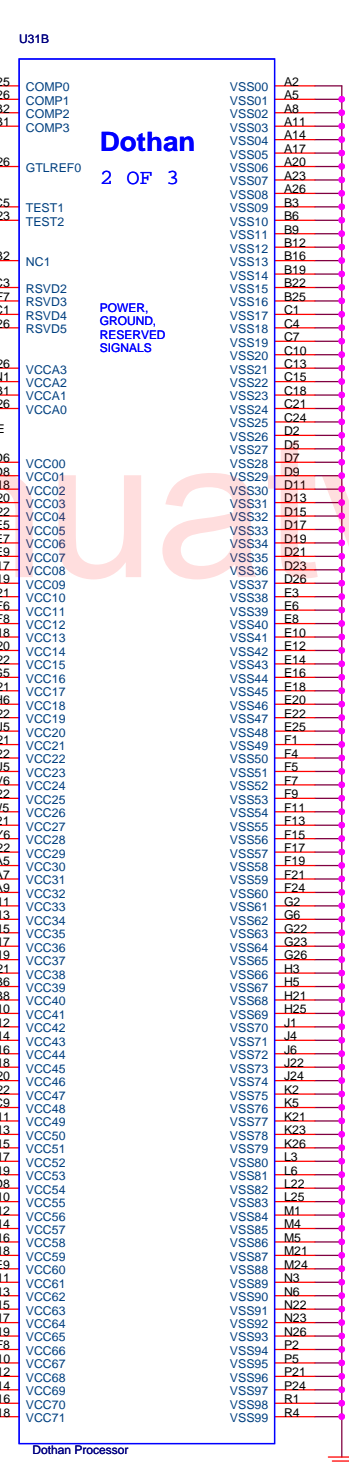
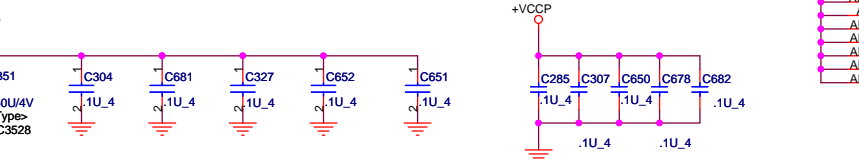
Date: Thursday, June 23, 2005 Sheet 3 of 40 Rev C



Place pull-down resistors within 0.5" of COMP pins



Total caps = 2633 uF
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



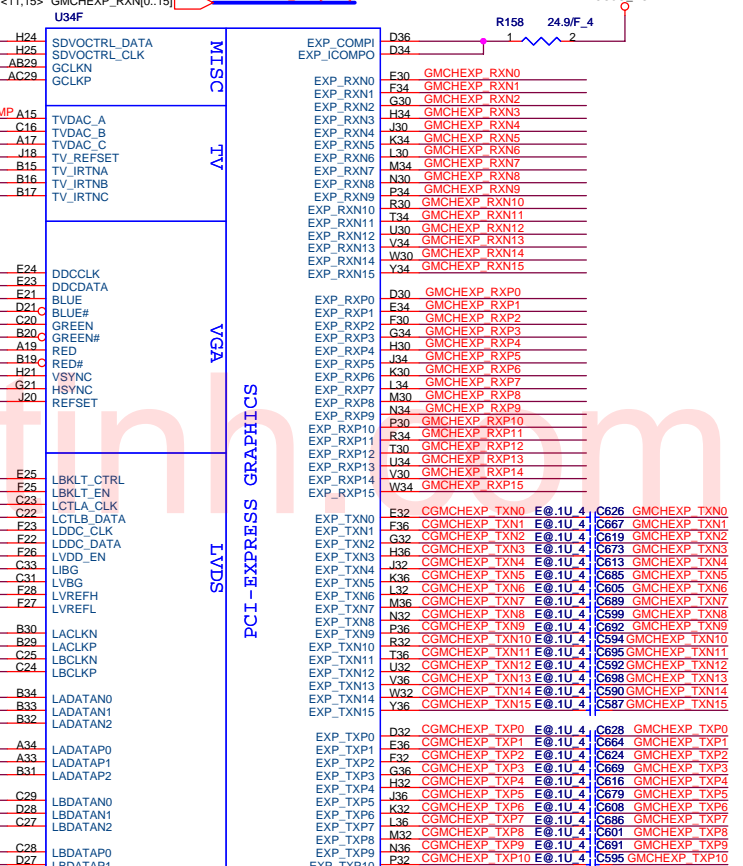
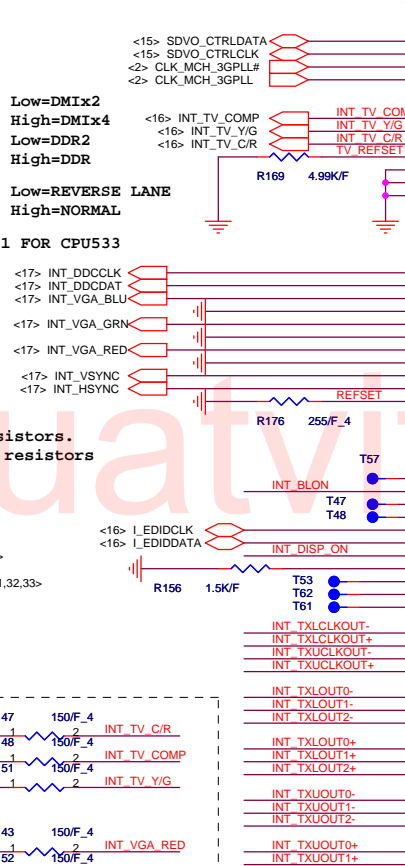
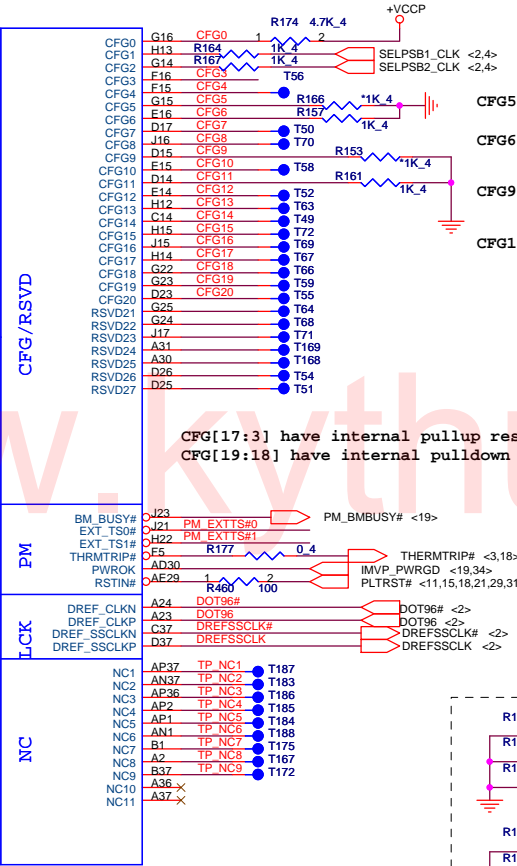
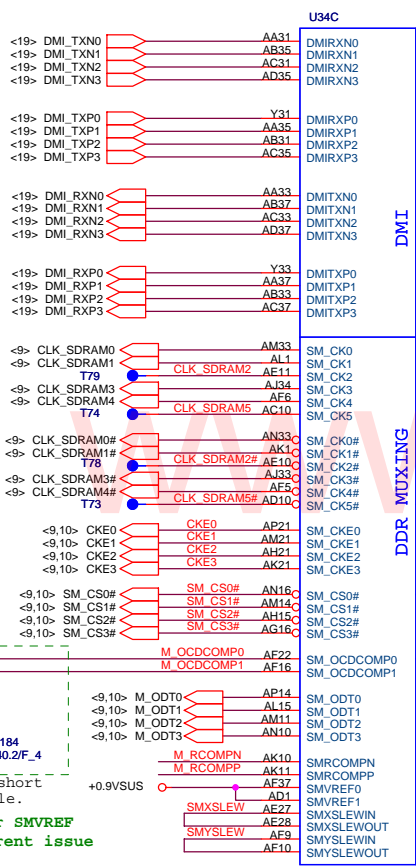
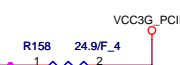
QUANTA COMPUTER

Title: Dothan Processor (POWER)

Size: Document Number ZL7

Date: Thursday, June 23, 2005 Sheet 4 of 40 Rev C

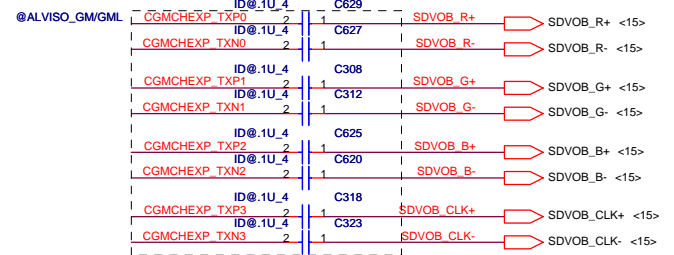
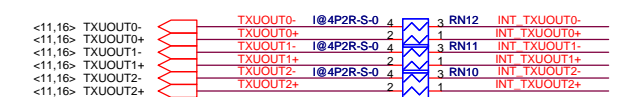
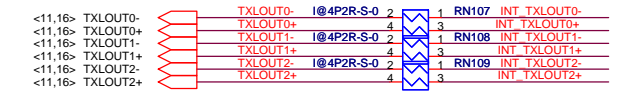
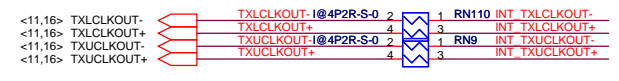
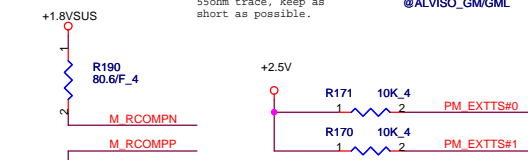
CFG[0:2]=100 FOR FSB 533
CFG[0:2]=101 FOR FSB 400

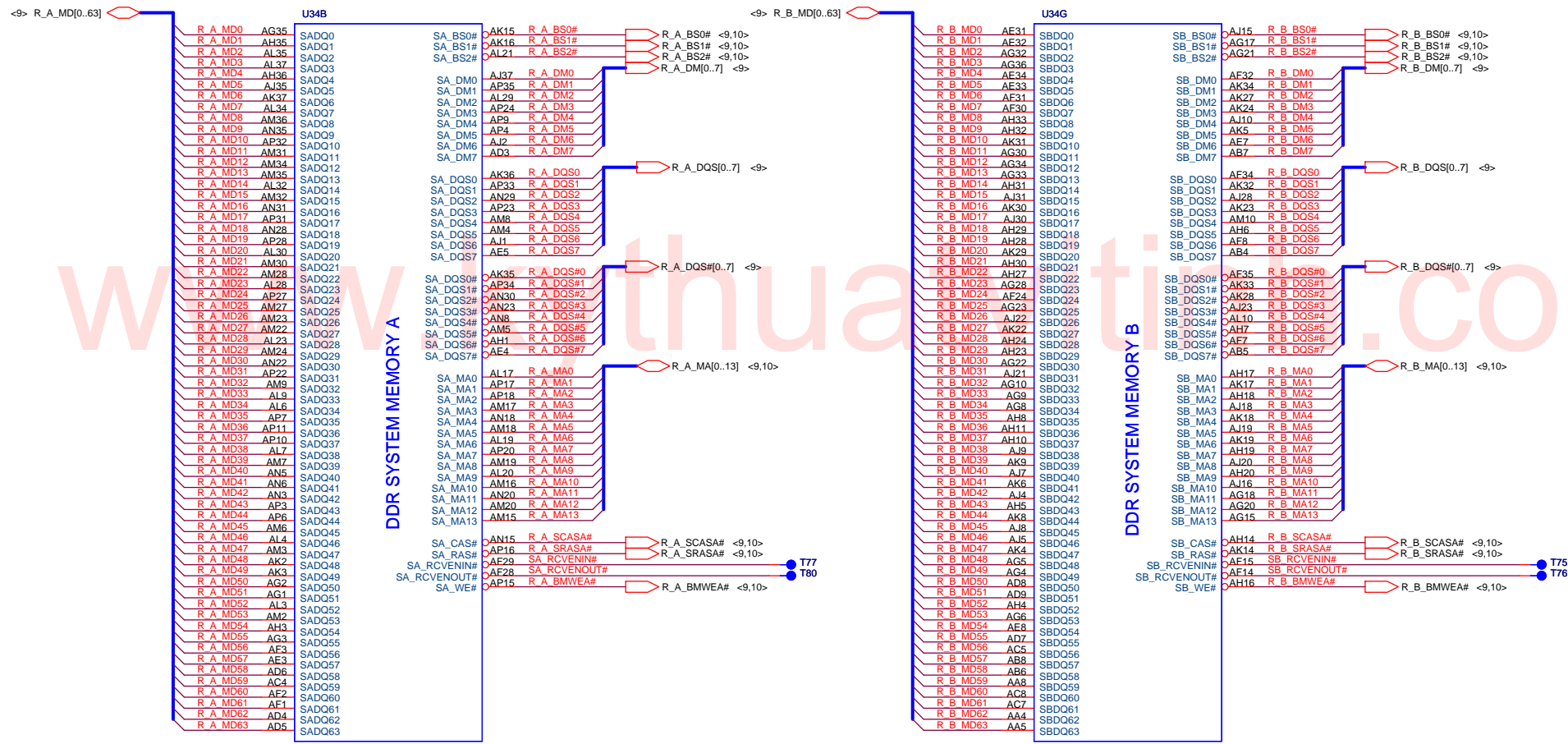


CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors

Route as short as possible.
Depop for SMVREF over current issue

It's point to point, 55ohm trace, keep as short as possible.





@ALVISO_GM/GML

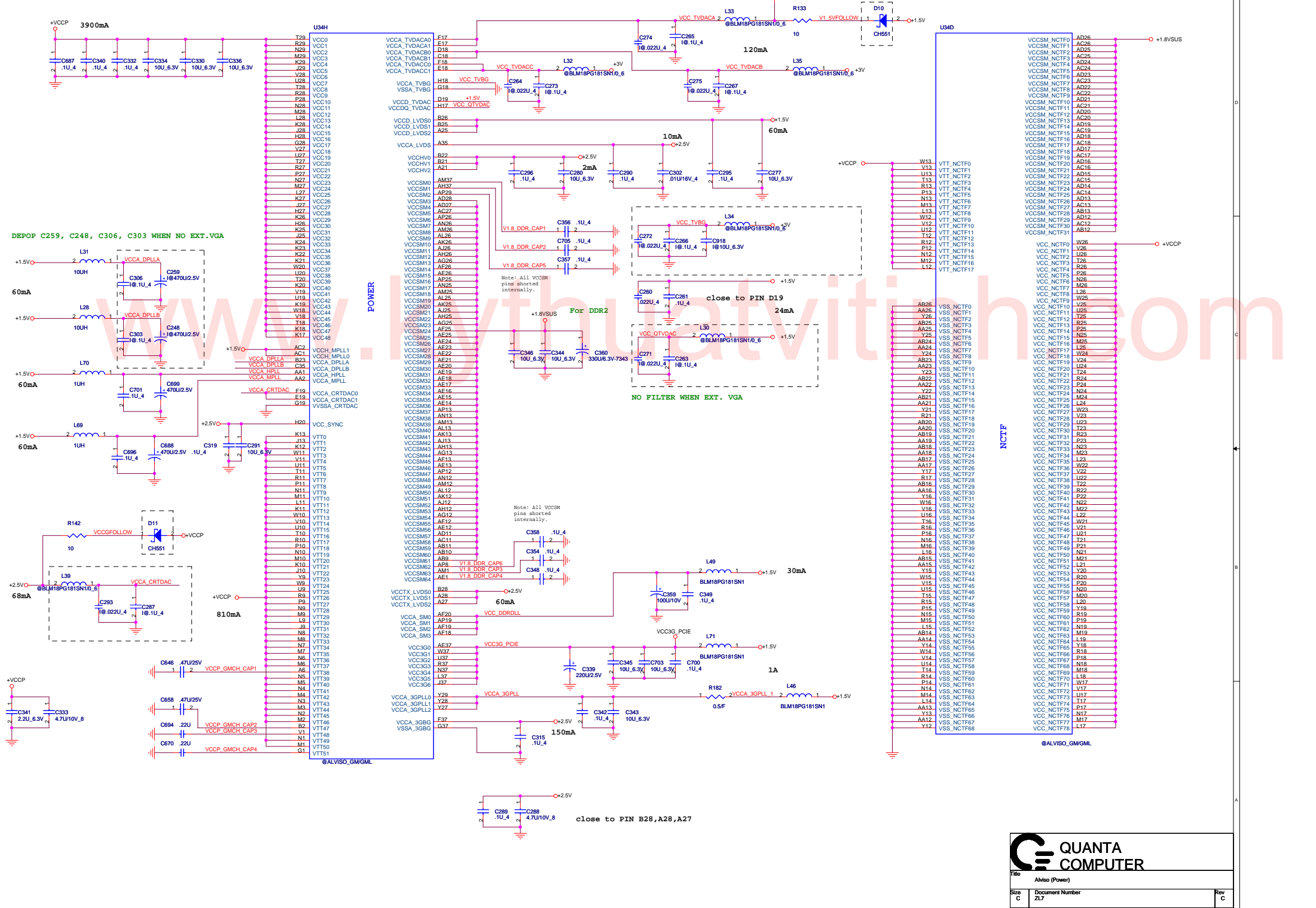
@ALVISO_GM/GML

QUANTA COMPUTER

Title: Alviso (DDR)

Size: Custom	Document Number: ZL7	Rev: C
Date: Thursday, June 23, 2005	Sheet: 7	of 40

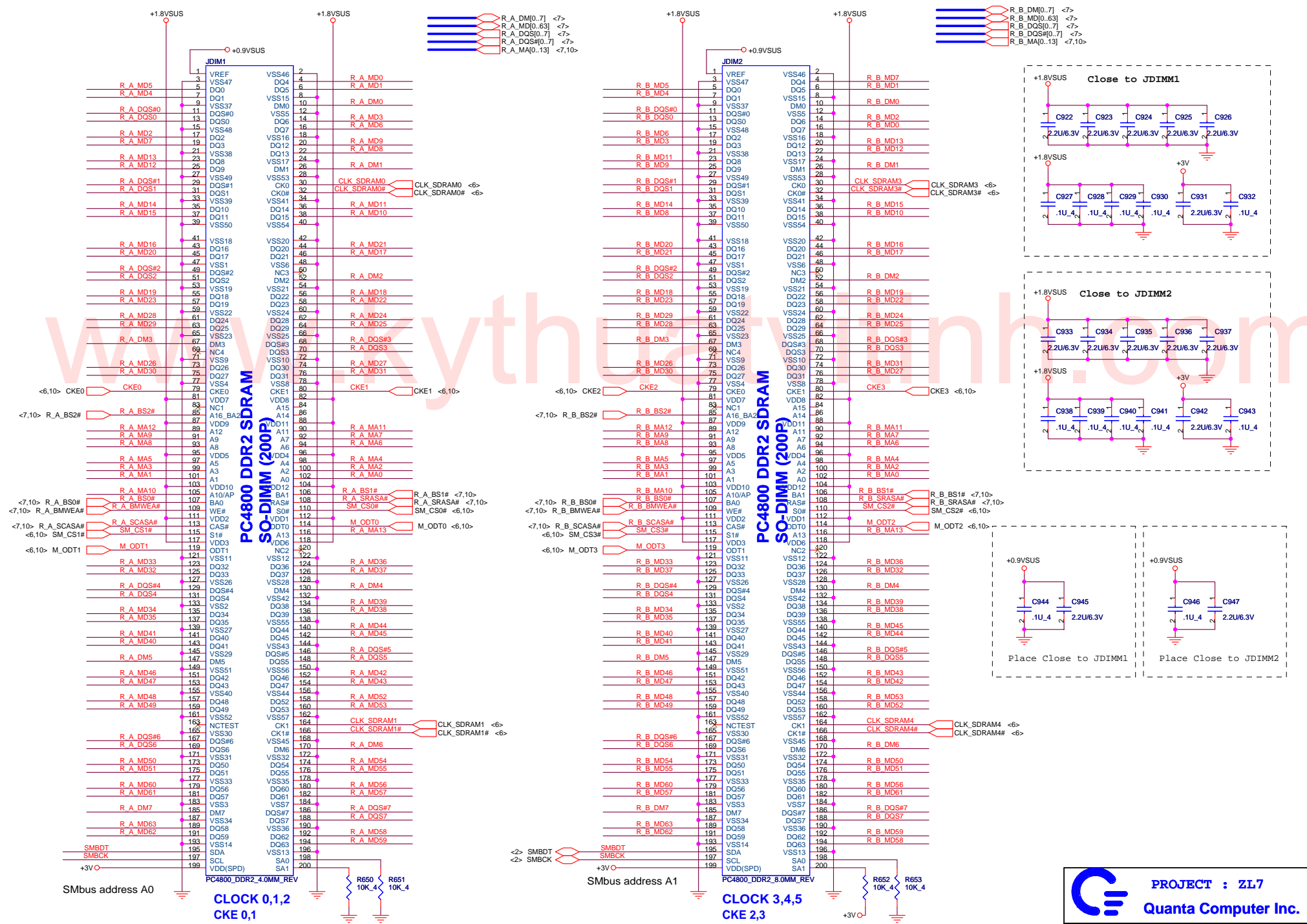
NO FILTER WHEN EXT. VGA



QUANTA COMPUTER

File: **Amiso (Power)**

Size C	Document Number 2L7	Rev C
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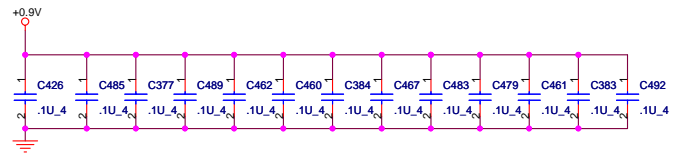
**PC4800 DDR2 SDRAM
SO-DIMM (200P)**

**PC4800 DDR2 SDRAM
SO-DIMM (200P)**

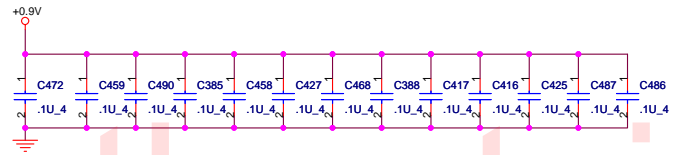
**CLOCK 0,1,2
CKE 0,1**

**CLOCK 3,4,5
CKE 2,3**

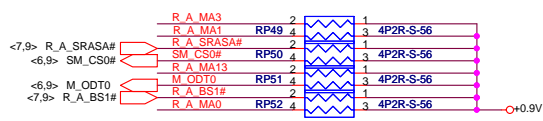
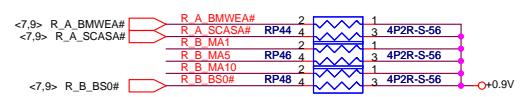
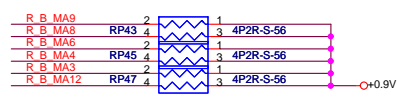
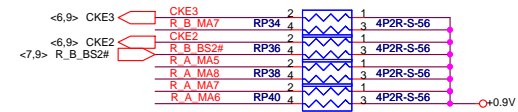
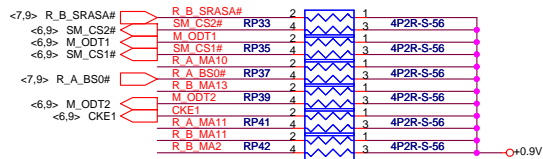
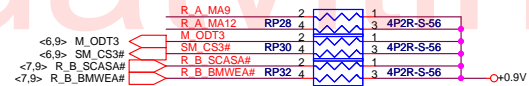
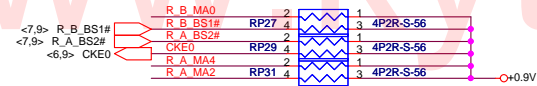




Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



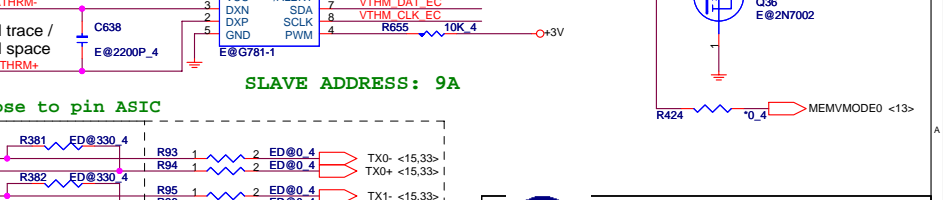
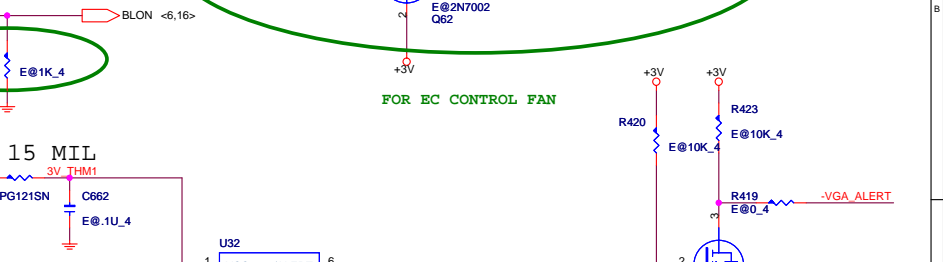
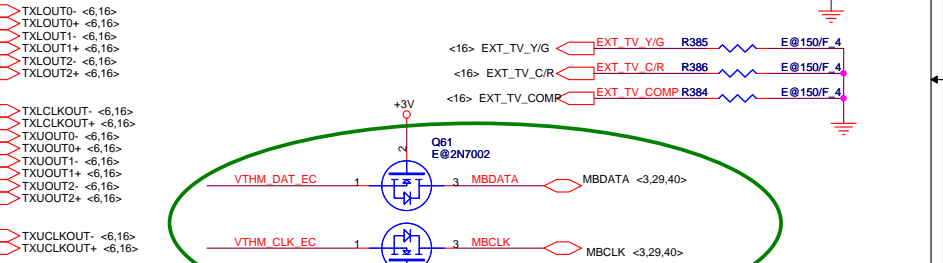
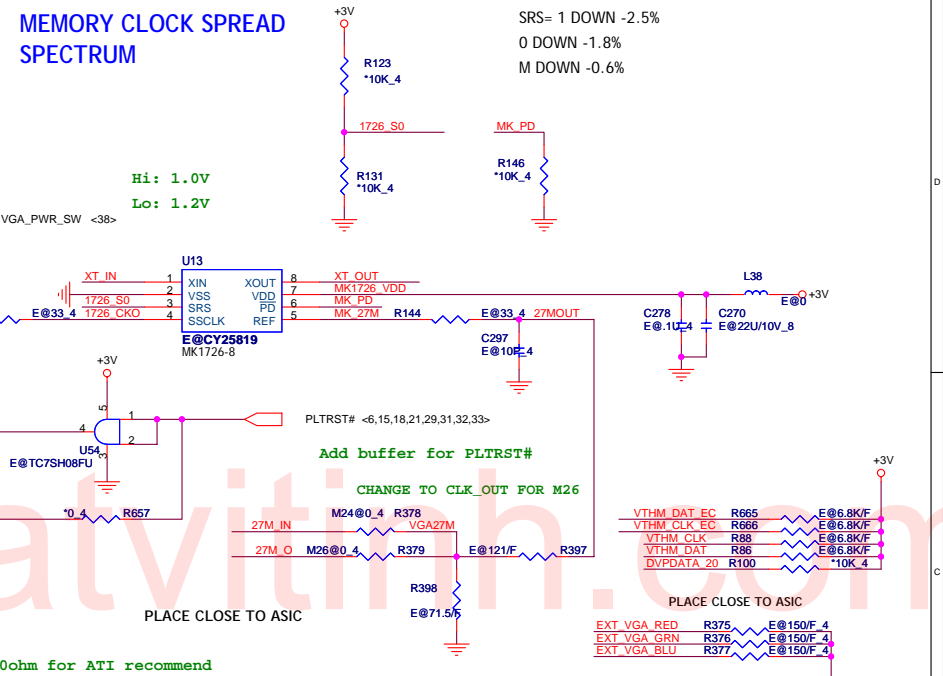
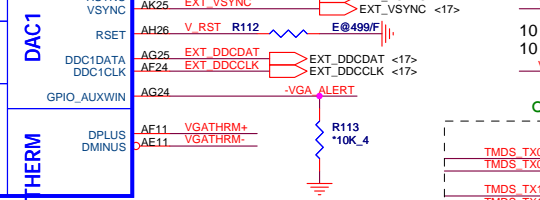
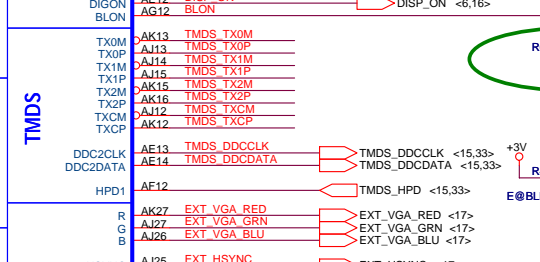
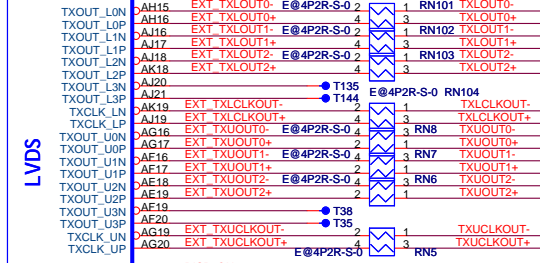
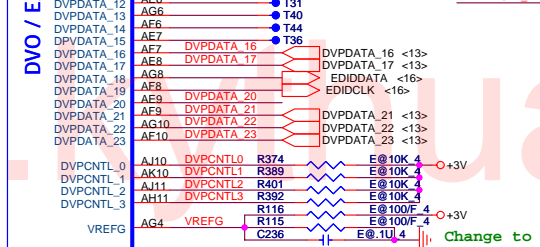
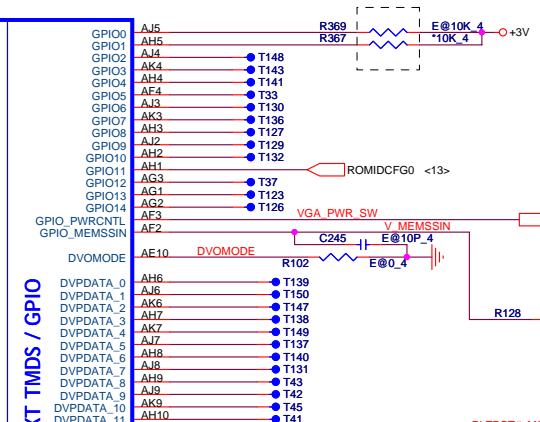
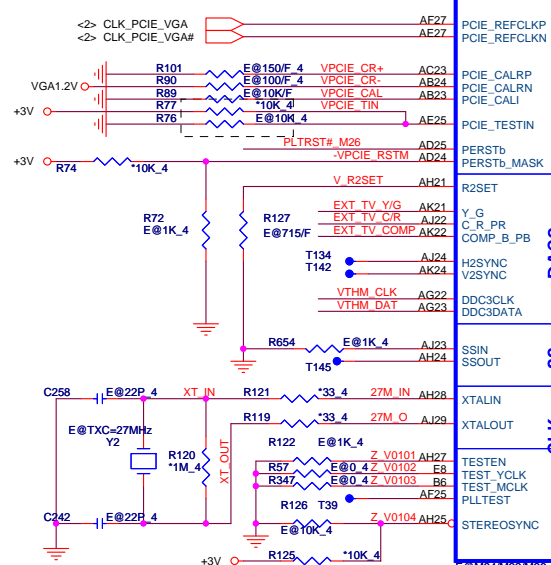
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



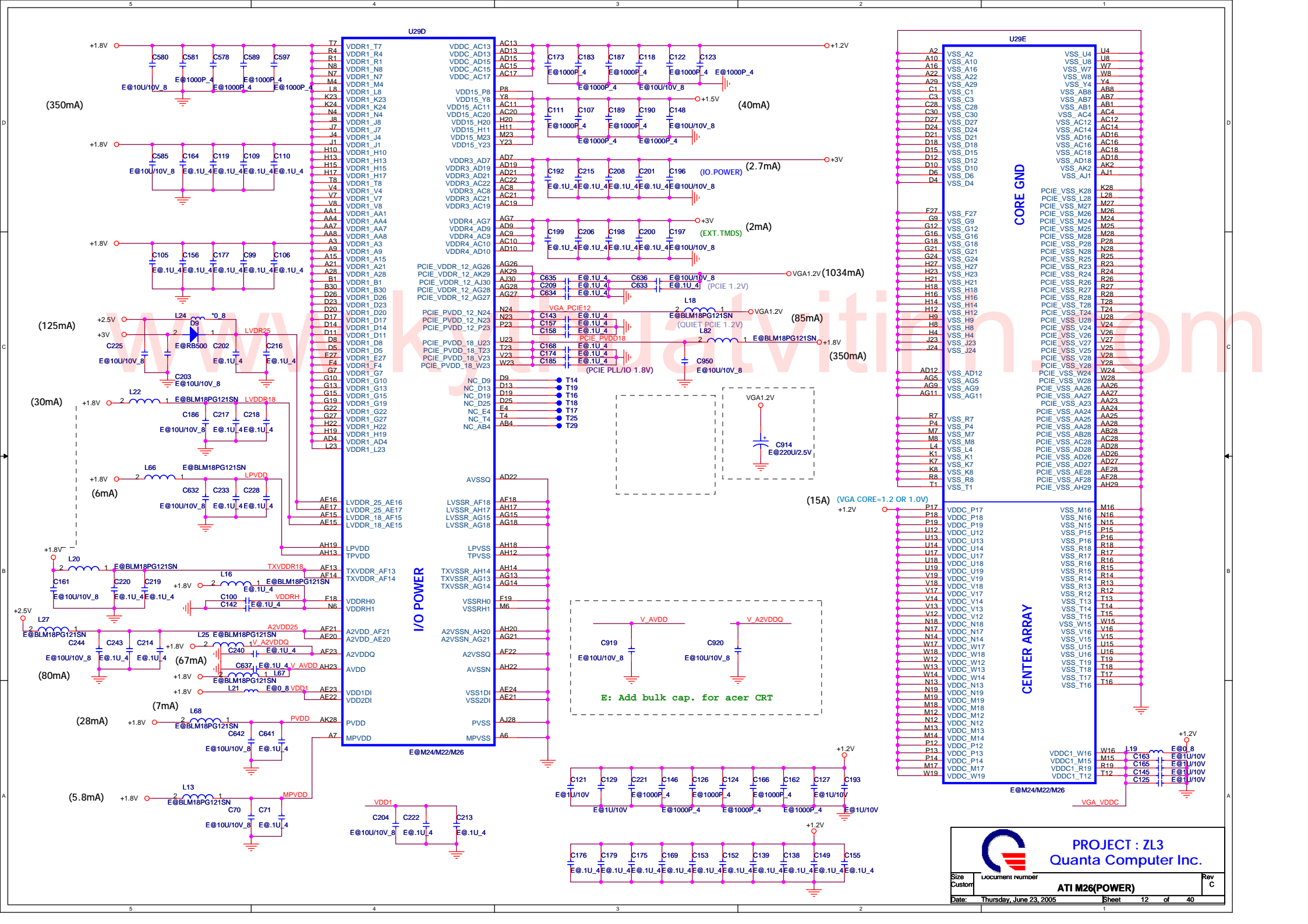
www.kythuatvithinh.com

Signal	Component	Value	Notes
<6> GMCEXP_TXP0[0..15]	GMCEXP_TXP0	AH30	
<6> GMCEXP_TXN0[0..15]	GMCEXP_TXN0	AG30	
<6> GMCEXP_TXP1[0..15]	GMCEXP_TXP1	AG29	
<6> GMCEXP_TXN1[0..15]	GMCEXP_TXN1	AF29	
<6,15> GMCEXP_RXP0[0..15]	GMCEXP_RXP2	AE29	
<6,15> GMCEXP_RXN0[0..15]	GMCEXP_RXN2	AE30	
	GMCEXP_TXP3	AD30	
	GMCEXP_TXN3	AD29	
	GMCEXP_TXP4	AD29	
	GMCEXP_TXN4	AB29	
	GMCEXP_TXP5	AB30	
	GMCEXP_TXN5	AA30	
	GMCEXP_TXP6	AA29	
	GMCEXP_TXN6	Y29	
	GMCEXP_TXP7	W29	
	GMCEXP_TXN7	W30	
	GMCEXP_TXP8	V30	
	GMCEXP_TXN8	V29	
	GMCEXP_TXP9	U29	
	GMCEXP_TXN9	T29	
	GMCEXP_TXP10	T30	
	GMCEXP_TXN10	R30	
	GMCEXP_TXP11	P29	
	GMCEXP_TXN11	P29	
	GMCEXP_TXP12	N29	
	GMCEXP_TXN12	N30	
	GMCEXP_TXP13	M29	
	GMCEXP_TXN13	M30	
	GMCEXP_TXP14	L29	
	GMCEXP_TXN14	K29	
	GMCEXP_TXP15	K30	
	GMCEXP_TXN15	J30	

Signal	Component	Value	Notes
GMCEXP_RXP0	C231	E@1U 4 V	GMCEXP_RXP0
GMCEXP_RXN0	C234	E@1U 4 V	GMCEXP_RXN0
GMCEXP_RXP1	C227	E@1U 4 V	GMCEXP_RXP1
GMCEXP_RXN1	C224	E@1U 4 V	GMCEXP_RXN1
GMCEXP_RXP2	C211	E@1U 4 V	GMCEXP_RXP2
GMCEXP_RXN2	C205	E@1U 4 V	GMCEXP_RXN2
GMCEXP_RXP3	C212	E@1U 4 V	GMCEXP_RXP3
GMCEXP_RXN3	C207	E@1U 4 V	GMCEXP_RXN3
GMCEXP_RXP4	C194	E@1U 4 V	GMCEXP_RXP4
GMCEXP_RXN4	C188	E@1U 4 V	GMCEXP_RXN4
GMCEXP_RXP5	C195	E@1U 4 V	GMCEXP_RXP5
GMCEXP_RXN5	C191	E@1U 4 V	GMCEXP_RXN5
GMCEXP_RXP6	C178	E@1U 4 V	GMCEXP_RXP6
GMCEXP_RXN6	C171	E@1U 4 V	GMCEXP_RXN6
GMCEXP_RXP7	C160	E@1U 4 V	GMCEXP_RXP7
GMCEXP_RXN7	C154	E@1U 4 V	GMCEXP_RXN7
GMCEXP_RXP8	C159	E@1U 4 V	GMCEXP_RXP8
GMCEXP_RXN8	C151	E@1U 4 V	GMCEXP_RXN8
GMCEXP_RXP9	C182	E@1U 4 V	GMCEXP_RXP9
GMCEXP_RXN9	C172	E@1U 4 V	GMCEXP_RXN9
GMCEXP_RXP10	C140	E@1U 4 V	GMCEXP_RXP10
GMCEXP_RXN10	C131	E@1U 4 V	GMCEXP_RXN10
GMCEXP_RXP11	C141	E@1U 4 V	GMCEXP_RXP11
GMCEXP_RXN11	C135	E@1U 4 V	GMCEXP_RXN11
GMCEXP_RXP12	C116	E@1U 4 V	GMCEXP_RXP12
GMCEXP_RXN12	C112	E@1U 4 V	GMCEXP_RXN12
GMCEXP_RXP13	C117	E@1U 4 V	GMCEXP_RXP13
GMCEXP_RXN13	C113	E@1U 4 V	GMCEXP_RXN13
GMCEXP_RXP14	C96	E@1U 4 V	GMCEXP_RXP14
GMCEXP_RXN14	C94	E@1U 4 V	GMCEXP_RXN14
GMCEXP_RXP15	C98	E@1U 4 V	GMCEXP_RXP15
GMCEXP_RXN15	C95	E@1U 4 V	GMCEXP_RXN15



SRS= 1 DOWN -2.5%
 0 DOWN -1.8%
 M DOWN -0.6%



(350mA)

(125mA)

(30mA)

(6mA)

(80mA)

(7mA)

(5.8mA)

(40mA)

(2mA)

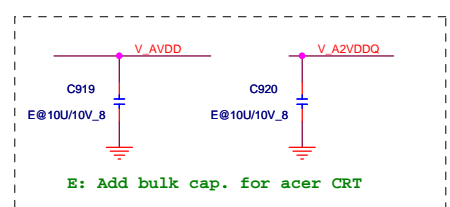
(85mA)

(350mA)

(15A)

CORE GND

CENTER ARRAY

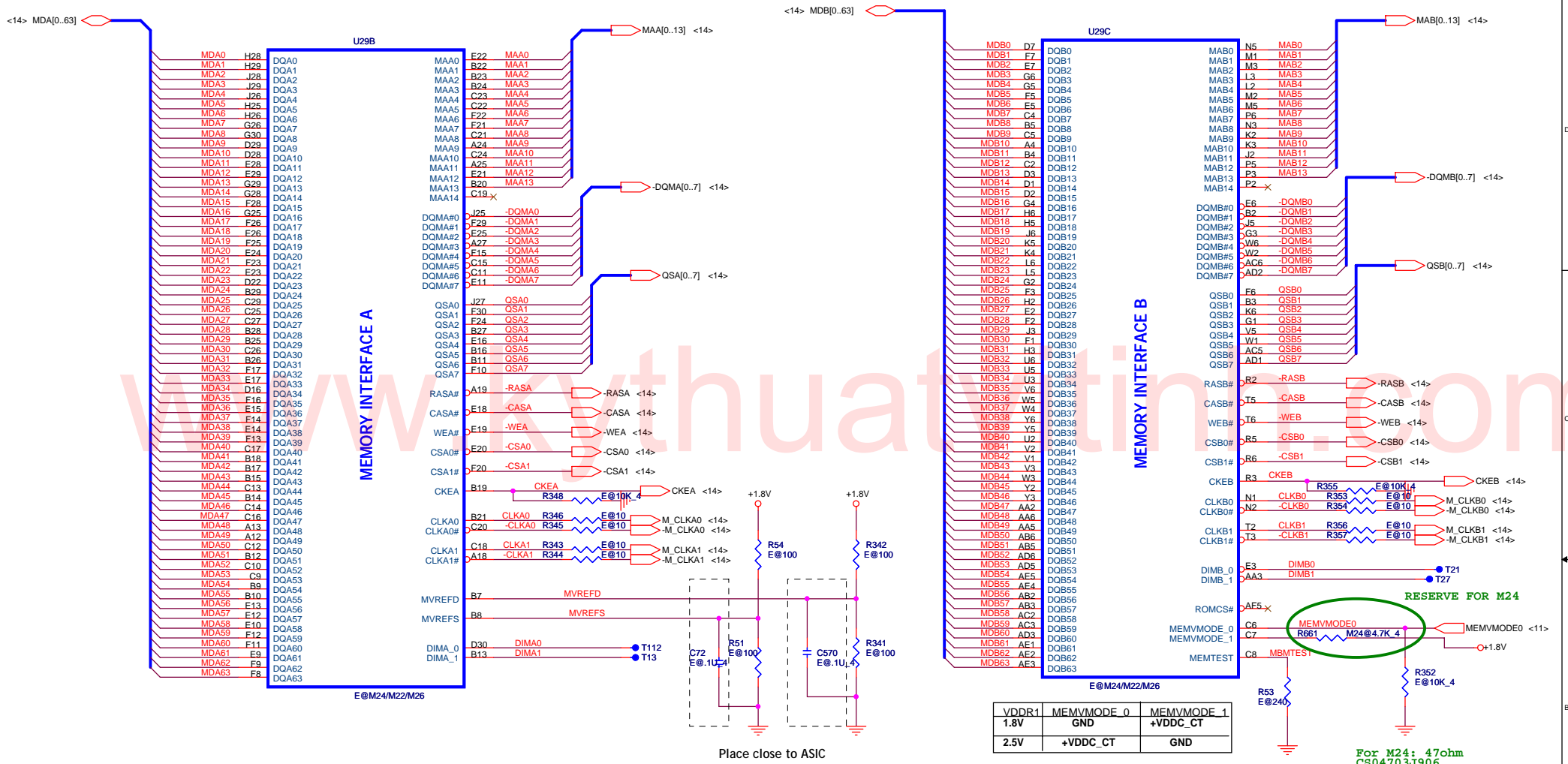


PROJECT : ZL3
Quanta Computer Inc.

ATI M26(Power)

Size: Custom Document number: Rev: C

Date: Thursday, June 23, 2005 Sheet: 12 of 40

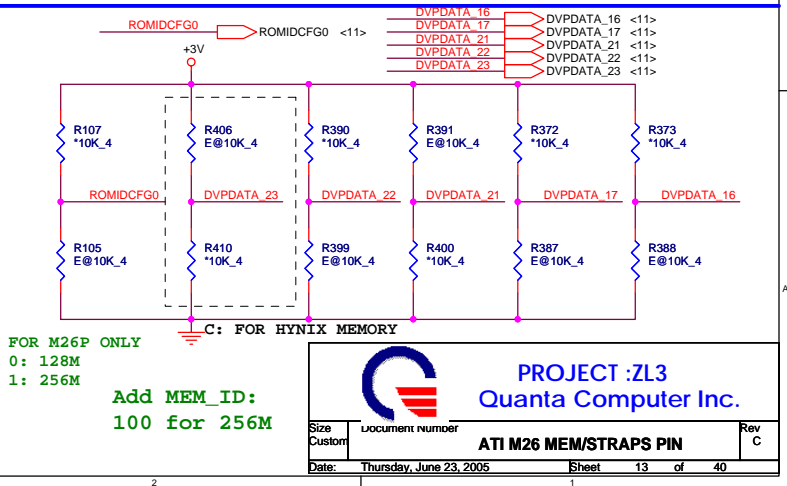


Place close to ASIC

For M24: 470ohm CS04703J906

GPIO_0	PCI-Express Current Calibration Bandgap Backup 0: use reference voltage from Bandgap 1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable 0: Disable PLL force calibration 1: Enable PLL force calibration
GPIO_(3,2)	00: PCI Express 1.0 mode 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration 0: enable 1: disable
GPIO_5	Bypass PCI-Express PLL

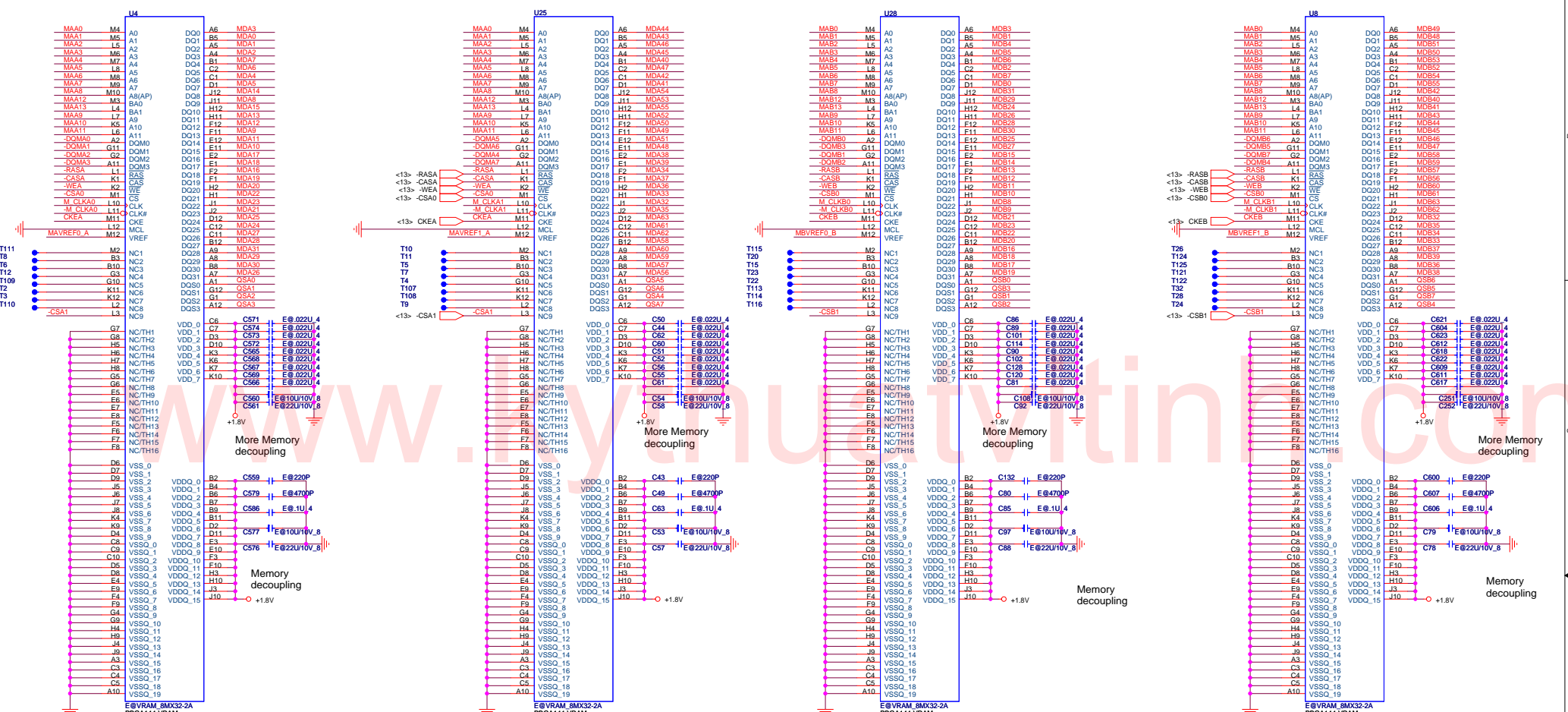
STRAPS PIN	
GPIO_6	PCI-Express transmitter current compensation 0: Normal 1: Inject extra current for output buffer switching
GPIO_8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible
GPIO(9,13:11) INT P/D	ROMIDCFG 0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23 MEM TYPE	DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung



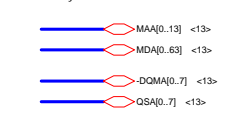
PROJECT :ZL3
Quanta Computer Inc.

Size Custom Document number
Date: Thursday, June 23, 2005 Sheet 13 of 40

ATI M26 MEM/STRAPS PIN Rev C

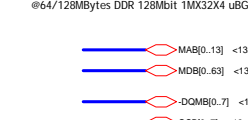


VGA DDR MEMORY A
 @64/128MBytes DDR 128Mbit 1MX32X4 uBGA

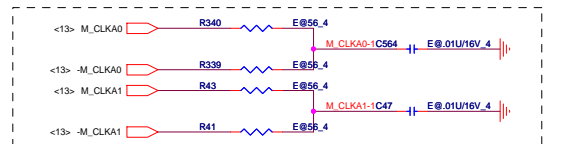


Place close to memory

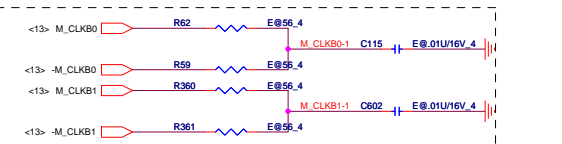
VGA DDR MEMORY B
 @64/128MBytes DDR 128Mbit 1MX32X4 uBGA



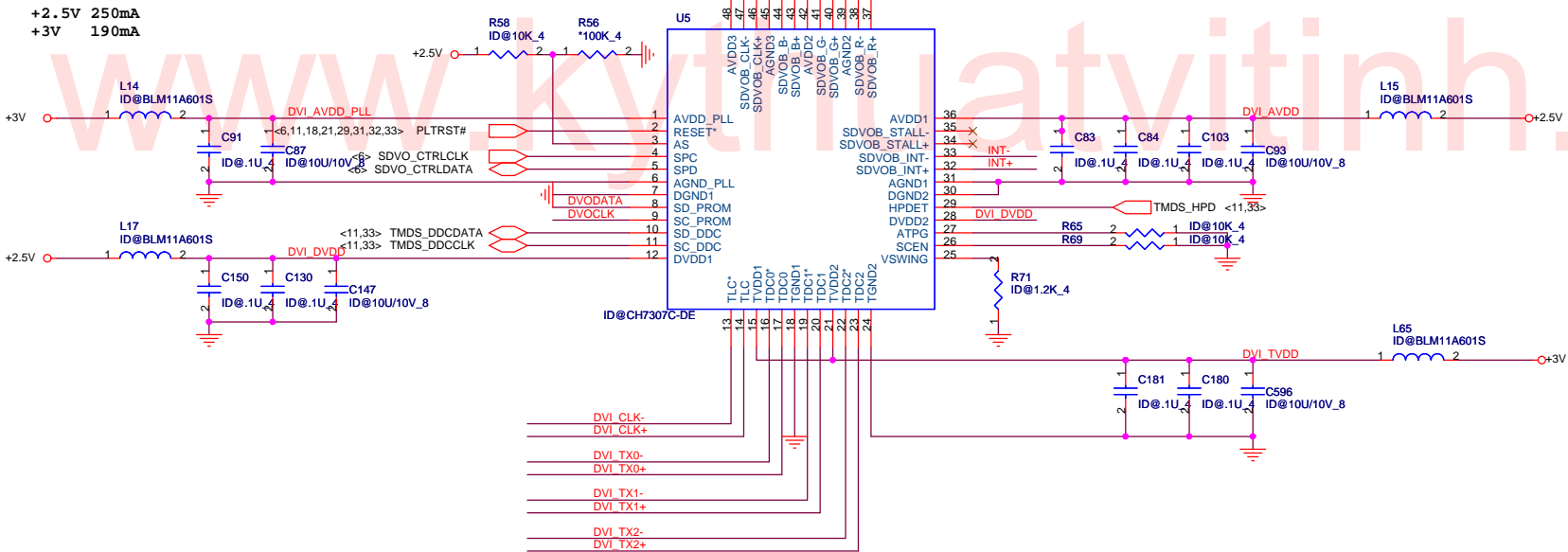
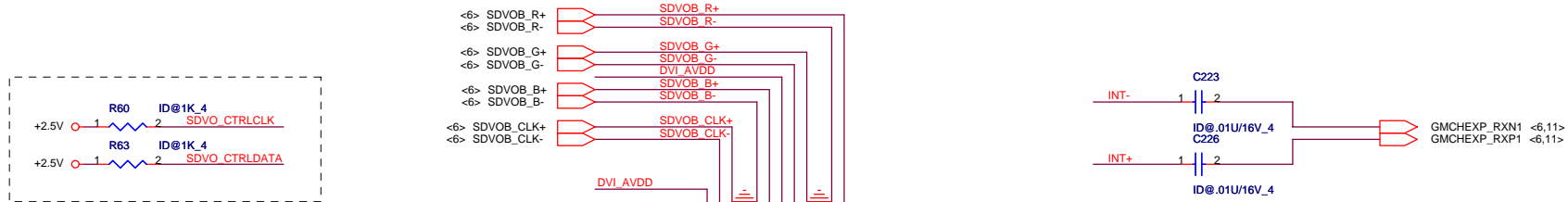
Place close to memory



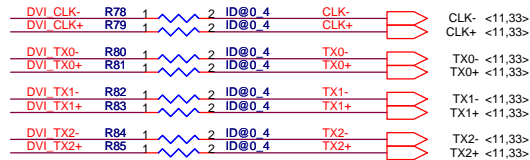
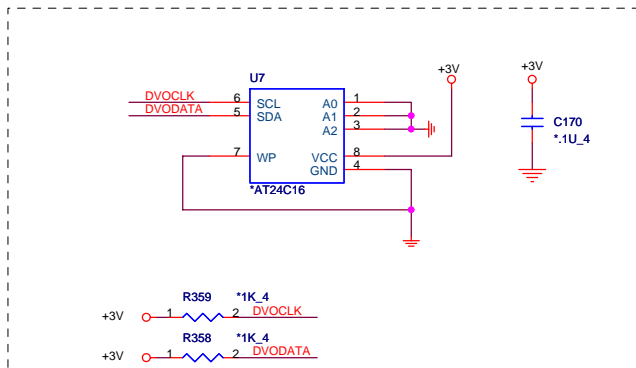
At least a 2.5:1 spacing between the pair
 These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

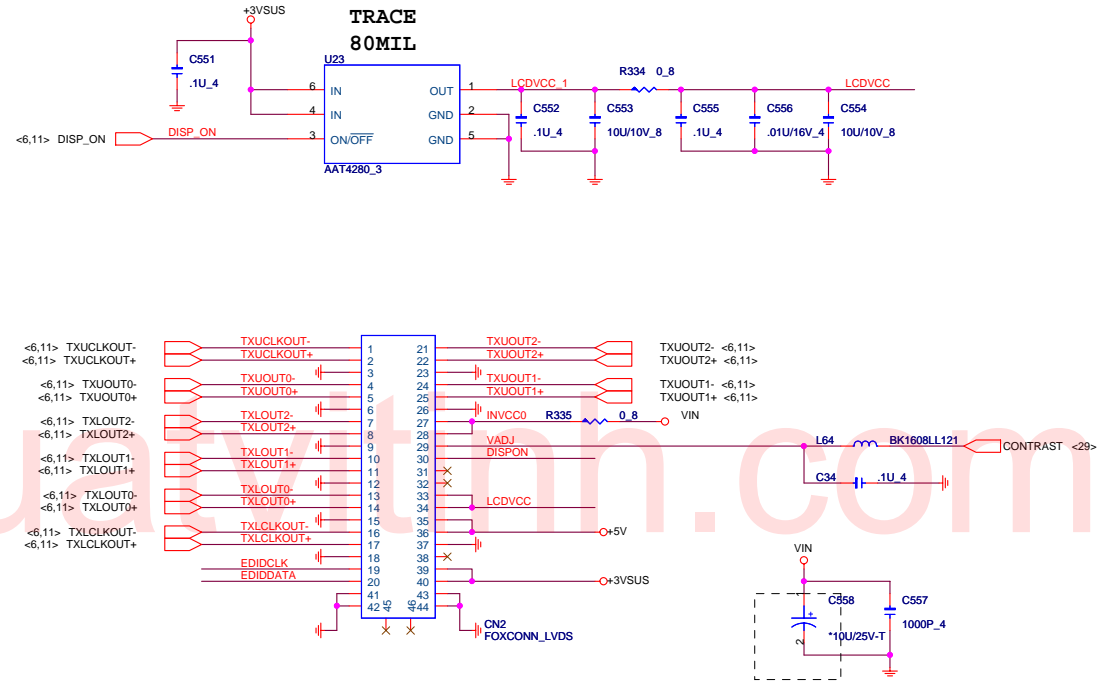
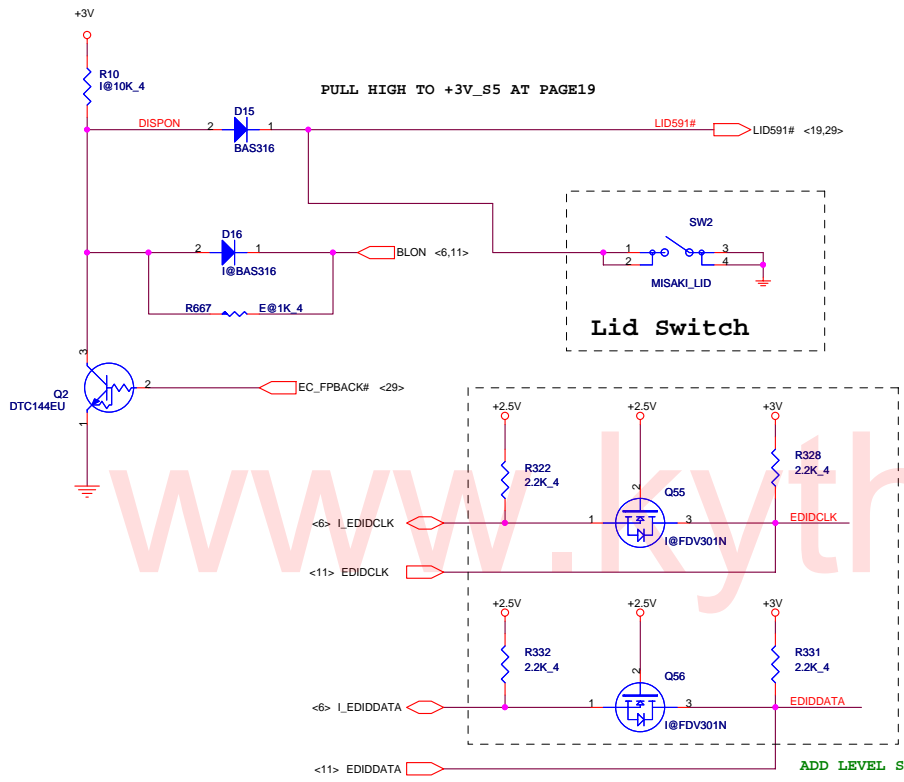


At least a 2.5:1 spacing between the pair
 These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

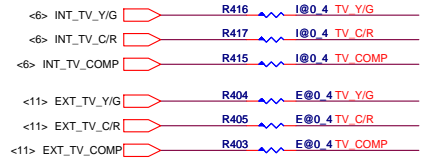
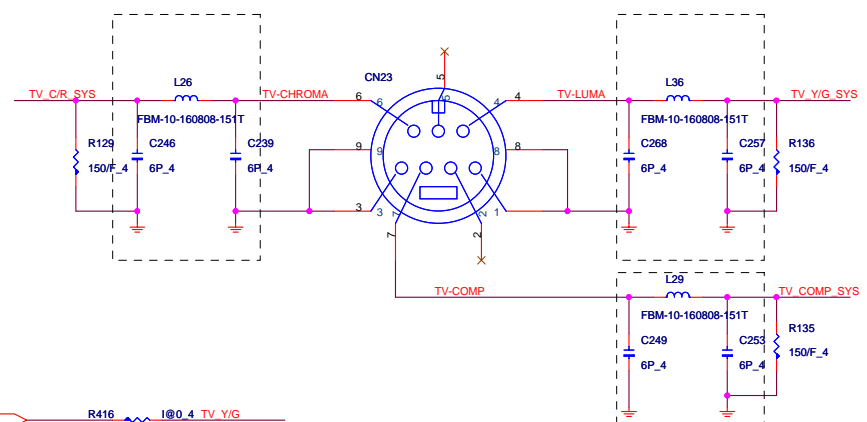
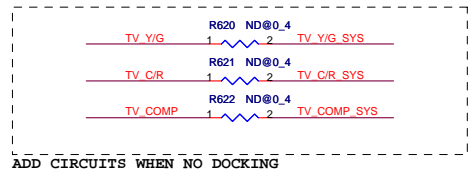
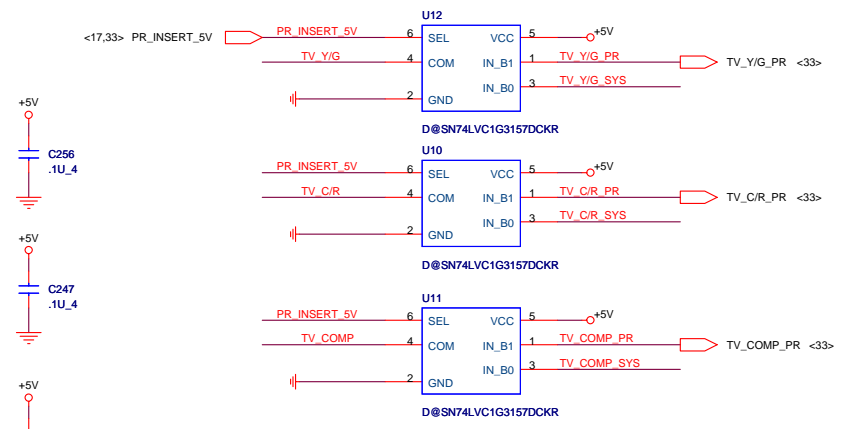


ALWAYS NOT ON, TEST ONLY

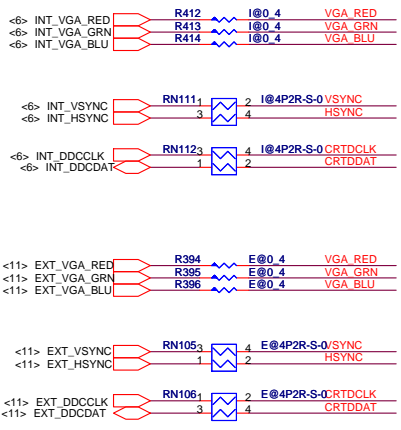




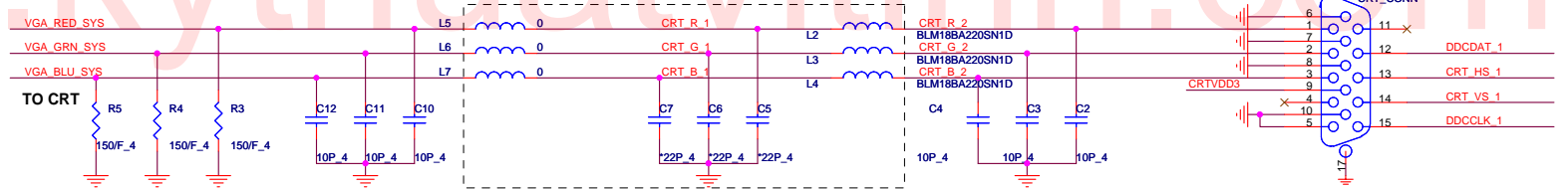
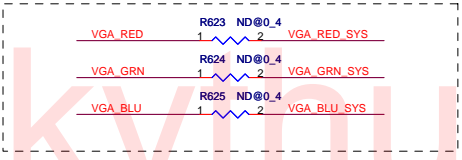
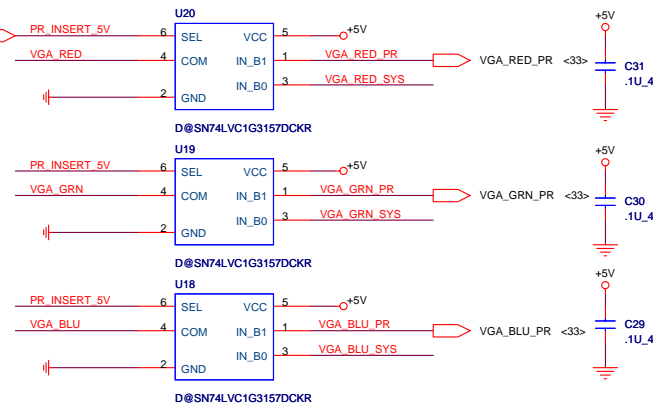
ADD LEVEL SHIFT FOR EDID
Change to FDV301 for Vgs issue



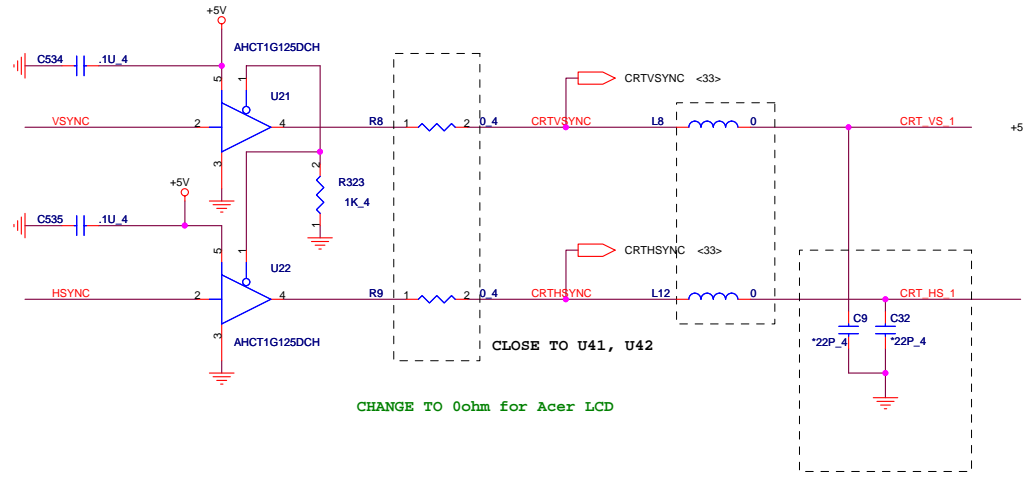
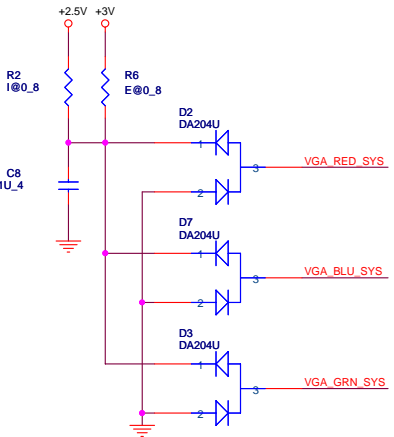
PROJECT : ZL7
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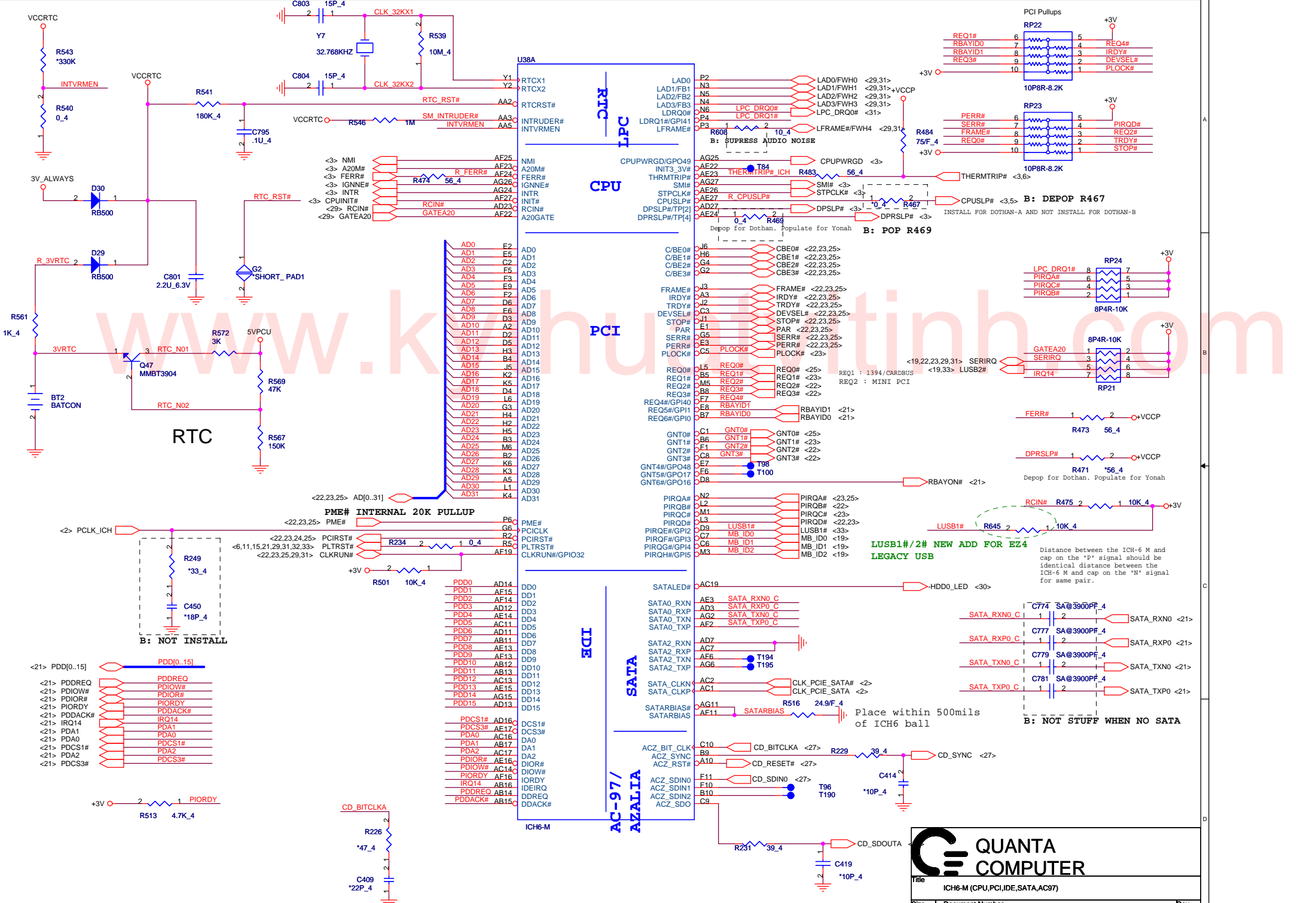
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

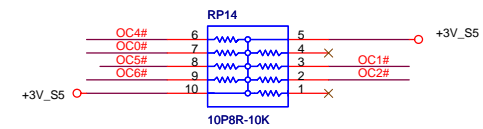
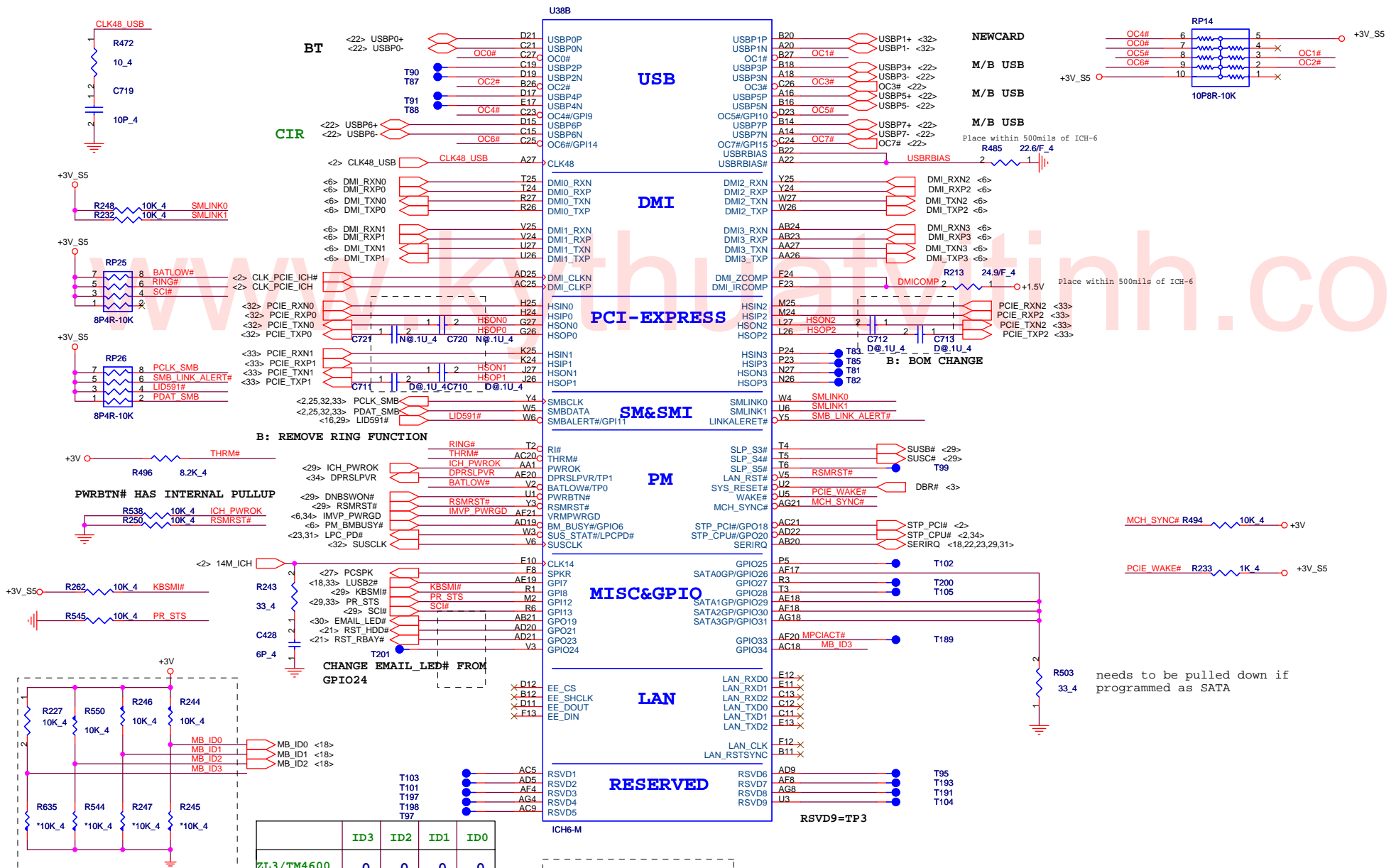


Change to FDV301N for Vgs issue.



CHANGE TO 0ohm for Acer LCD





Place within 500mils of ICH-6
R485 22.0/F_4

Place within 500mils of ICH-6
R213 24.9/F_4

B: REMOVE RING FUNCTION

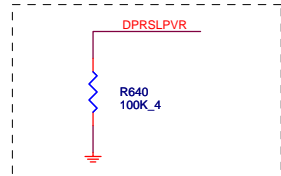
B: BOM CHANGE

MCH SYNC# R494 10K_4 +3V

PCIE_WAKE# R233 1K_4 +3V_S5

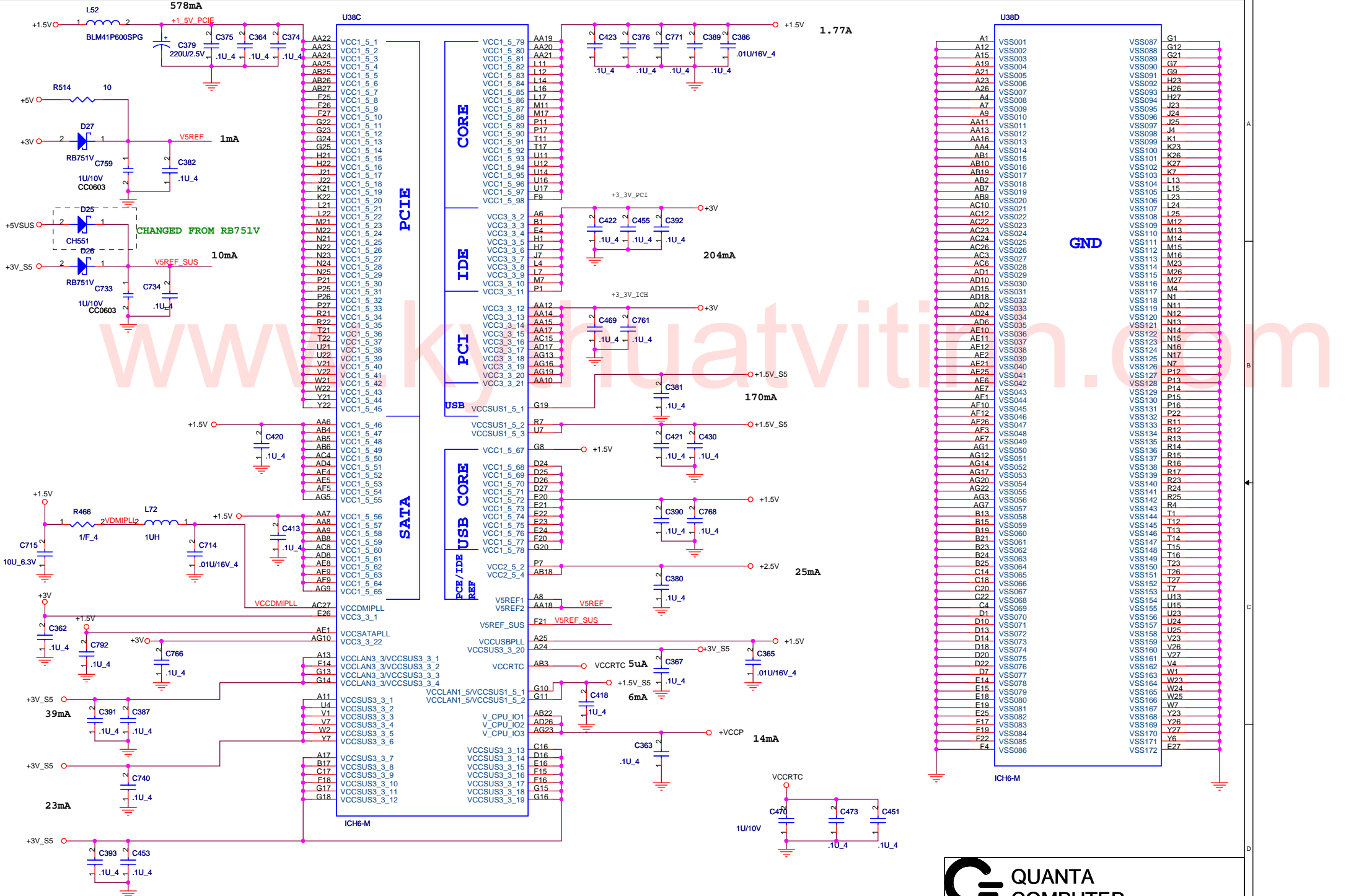
R503 needs to be pulled down if programmed as SATA

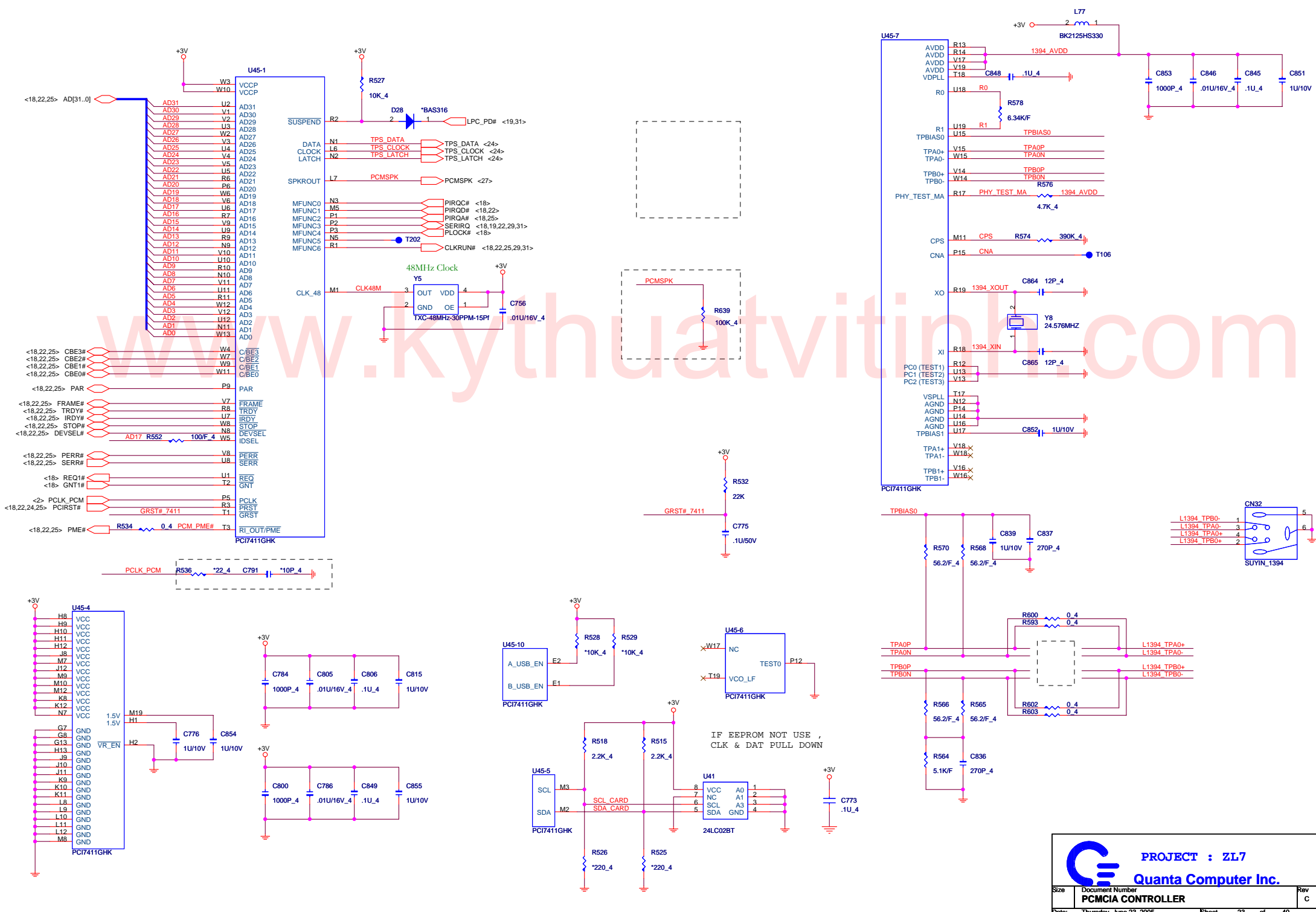
	ID3	ID2	ID1	ID0
ZL3/TM4600	0	0	0	0
ZL3B/TM4100	0	0	1	0
ZL3D/AS1690	0	1	0	0
ZL3F/AS3510	0	1	1	0
ZL3C/EX4100	1	0	1	1

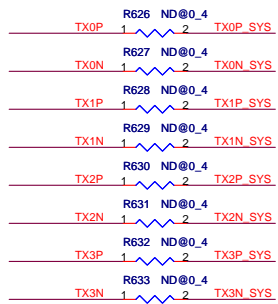
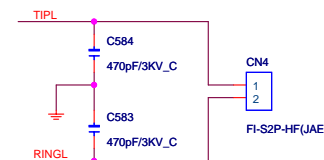
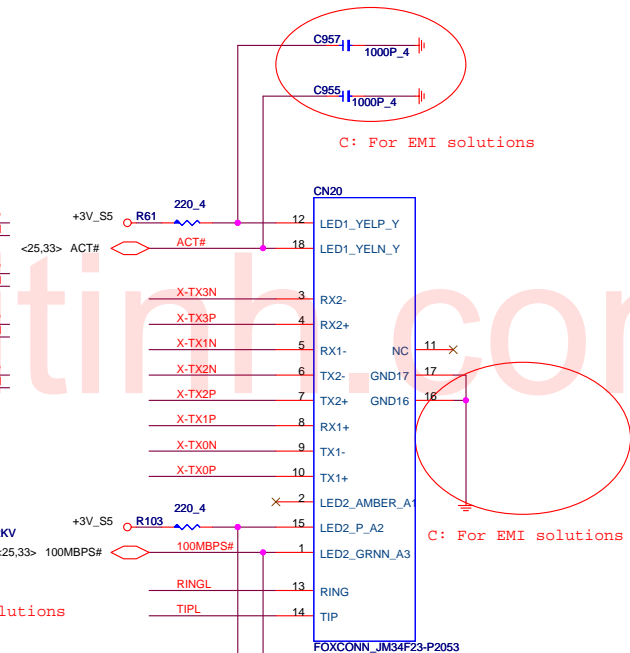
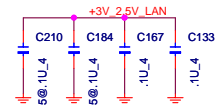
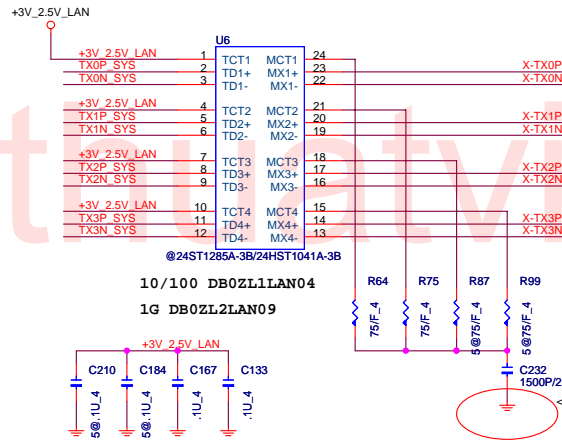
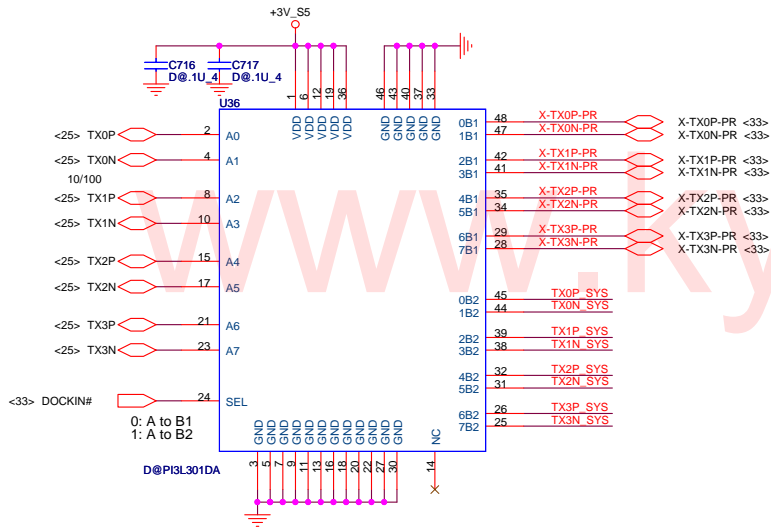


ADD PULLLOW



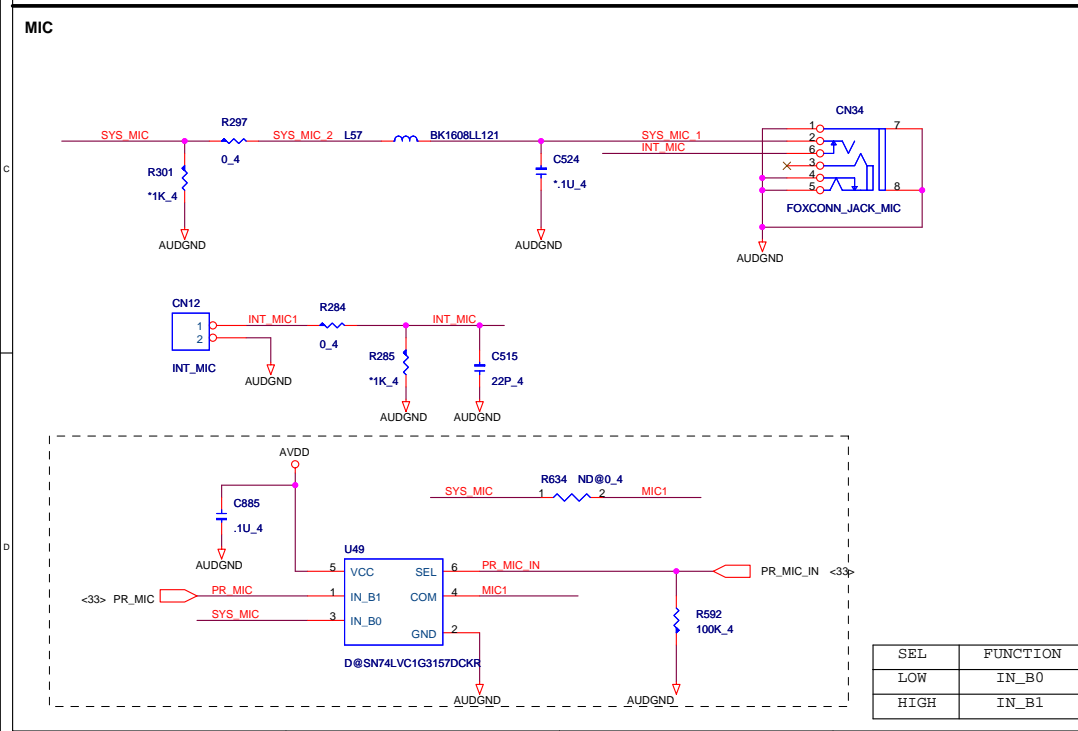
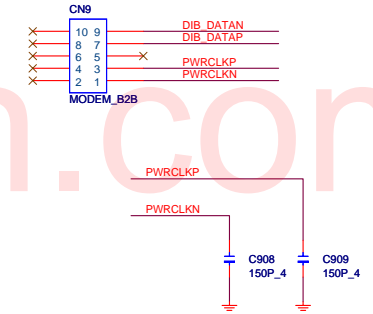
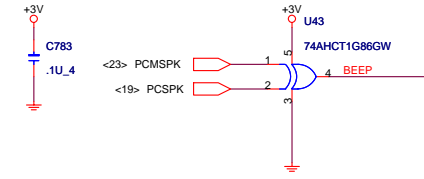
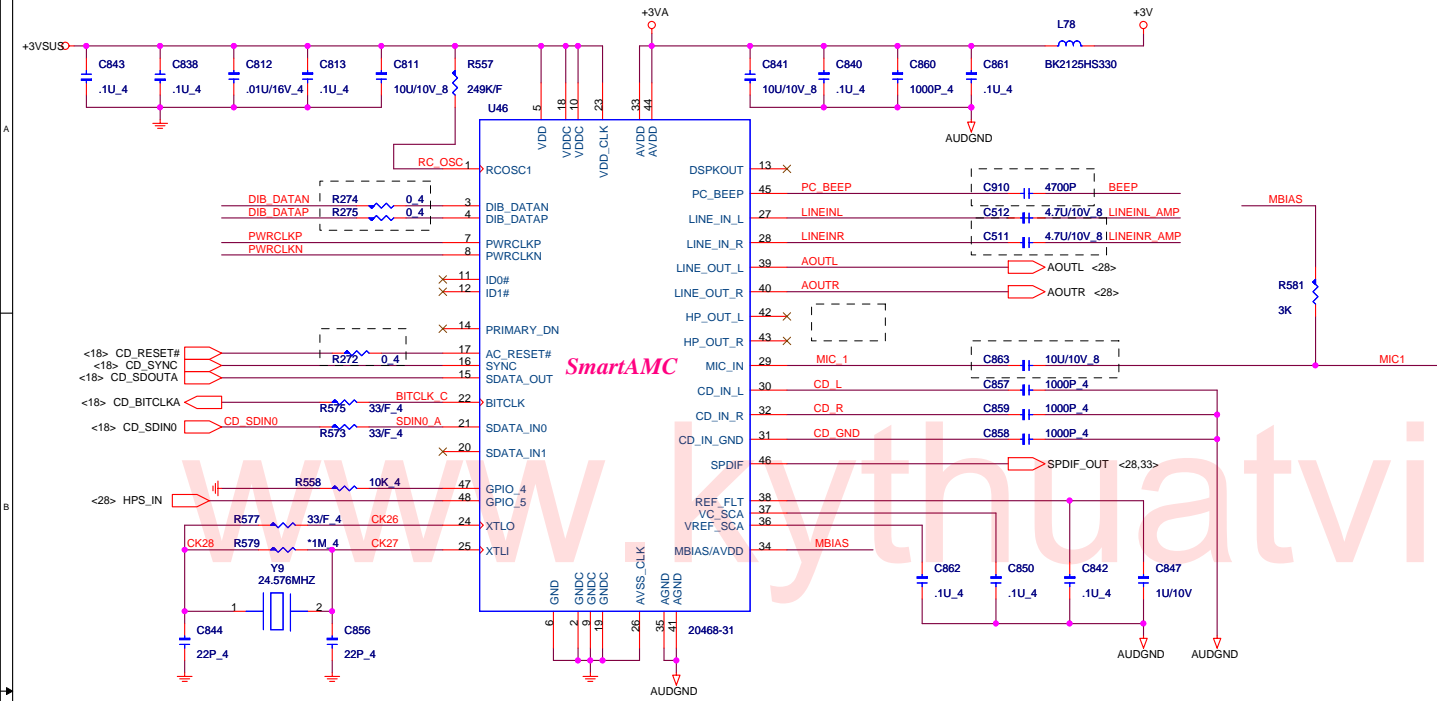




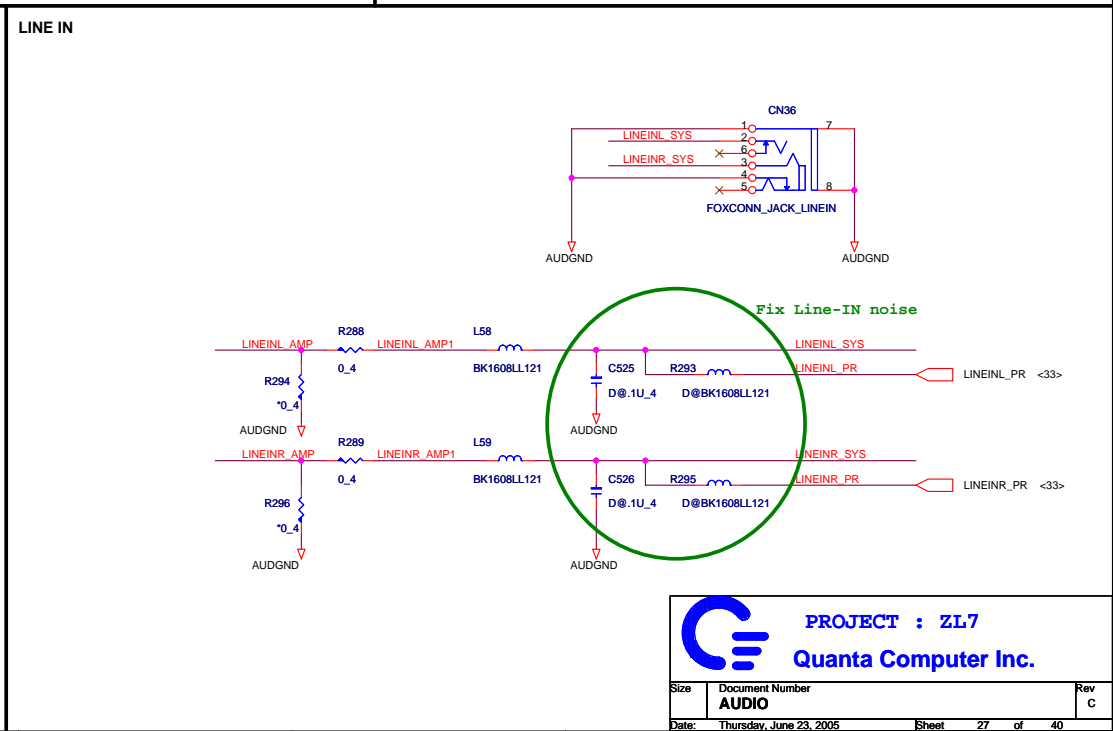


ADD CIRCUITS WHEN NO DOCKING

The AMC20463-004 modem is used for mother board family MBAMC20463-004.



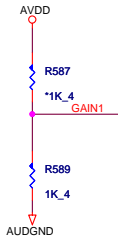
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



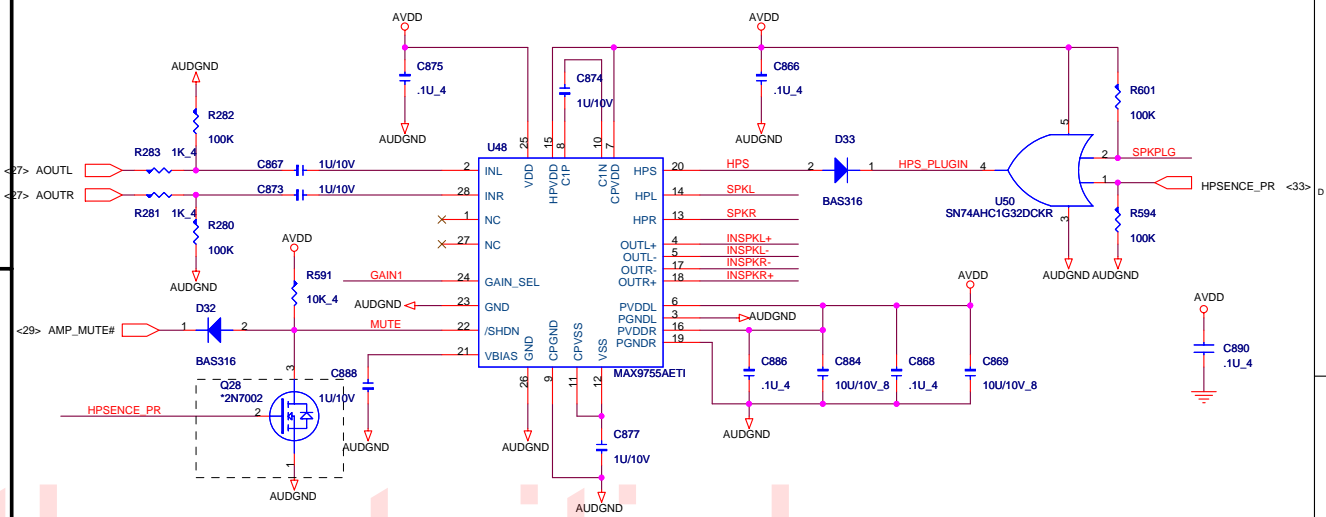
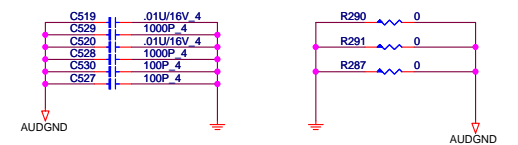
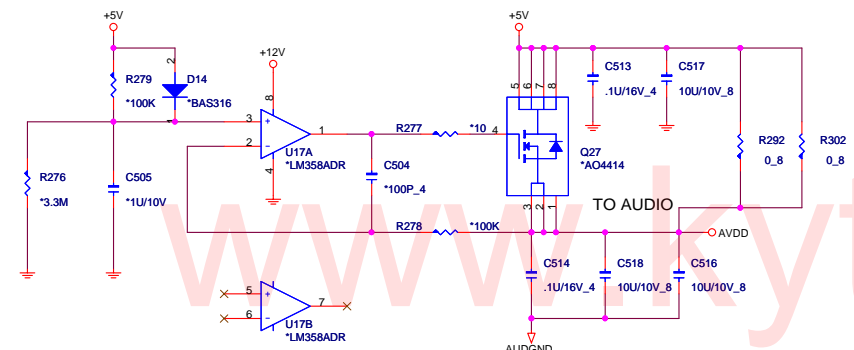
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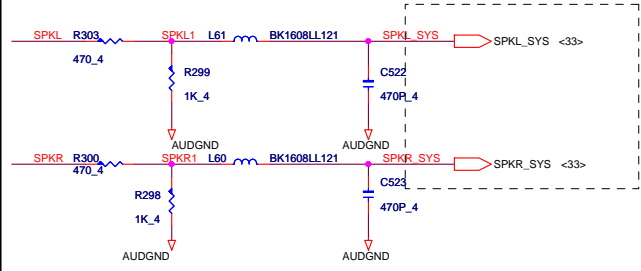
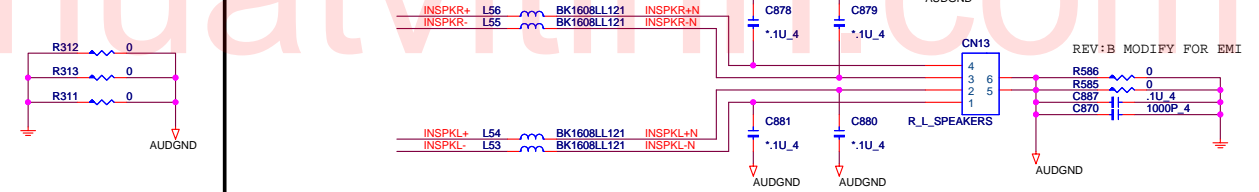
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



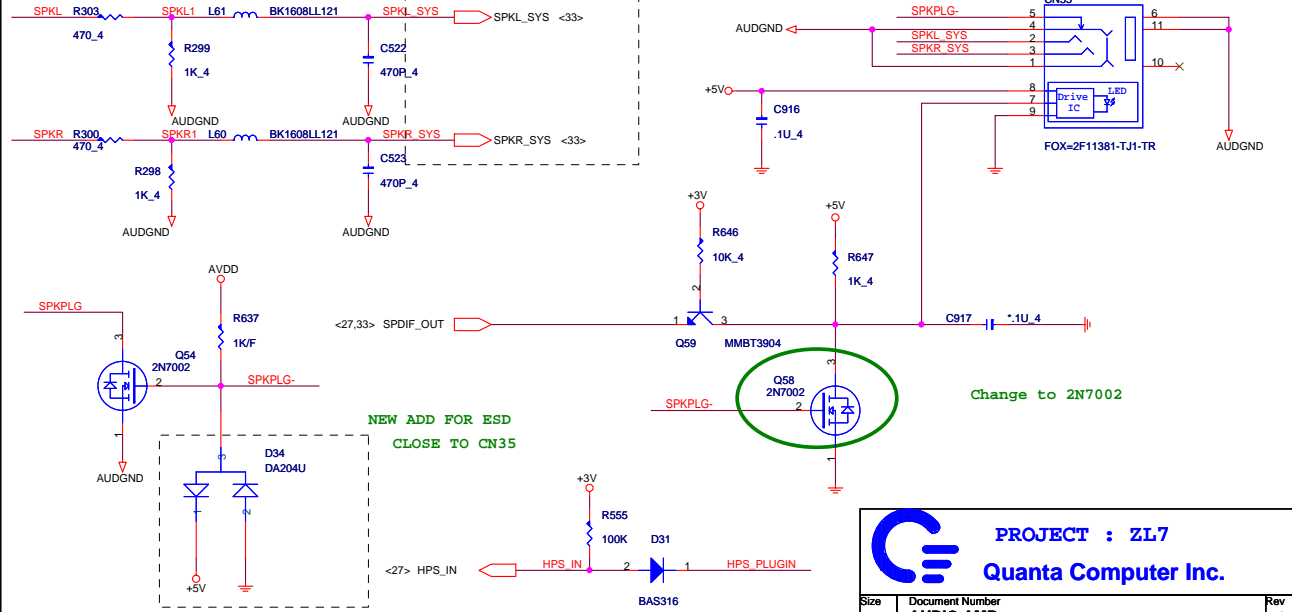
AMP POWER



SPEAKER CON.



LINE OUT&SPDIF

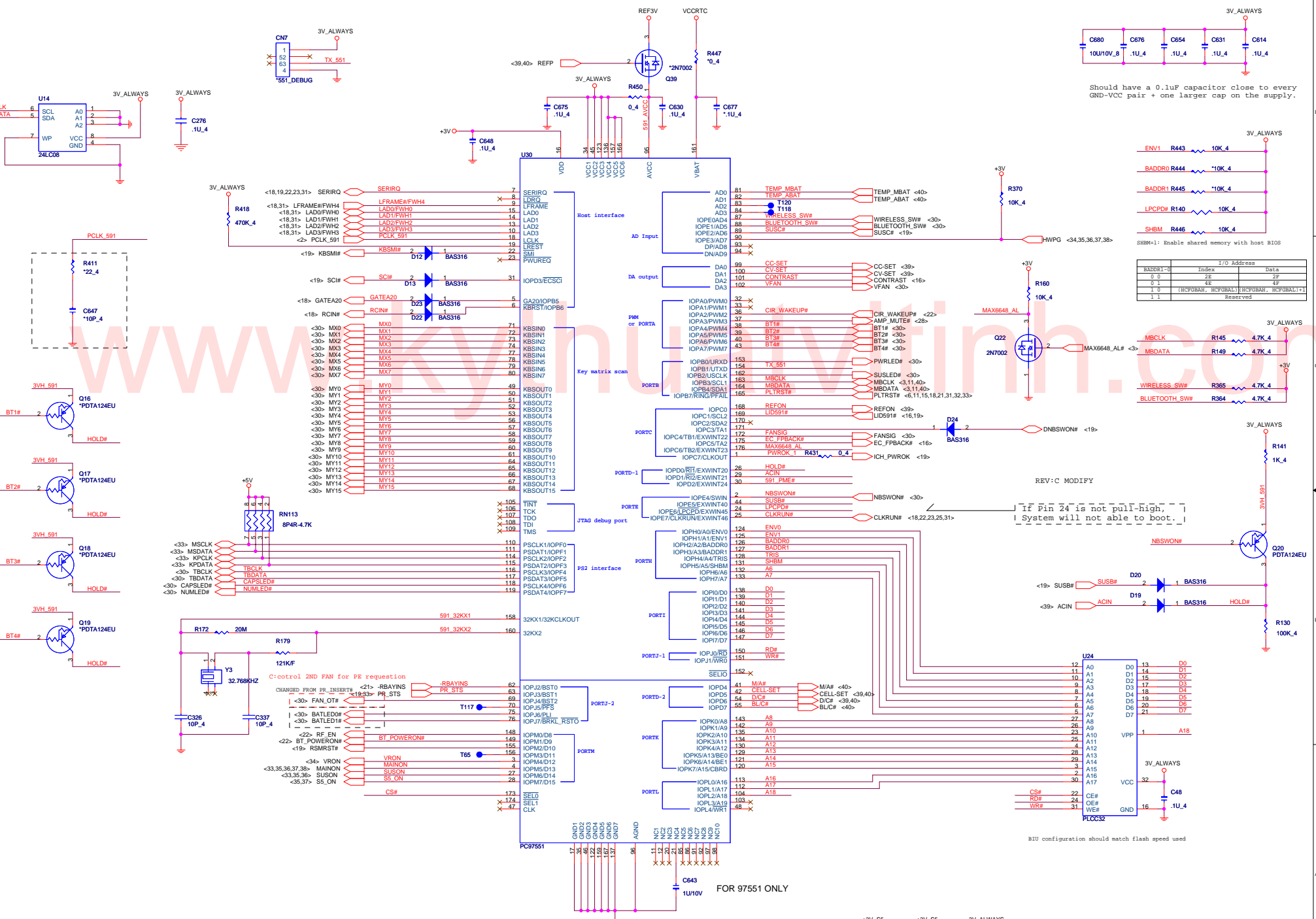


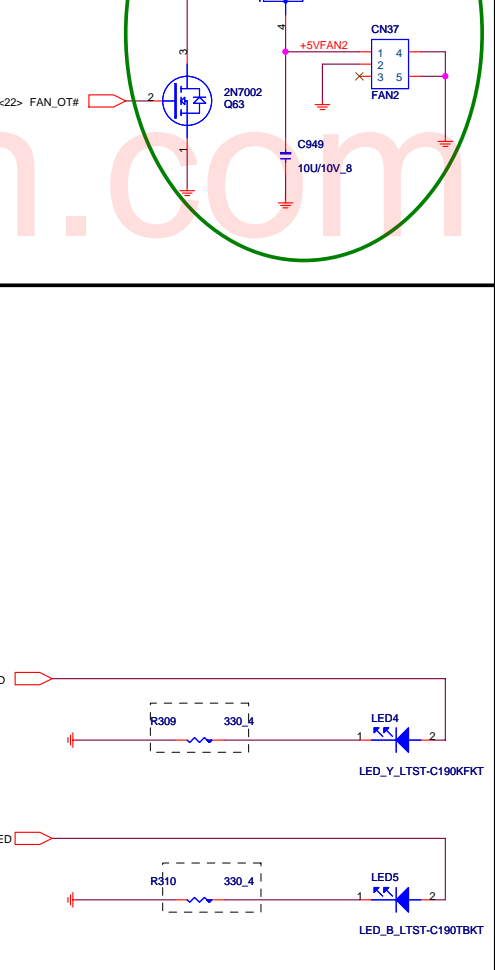
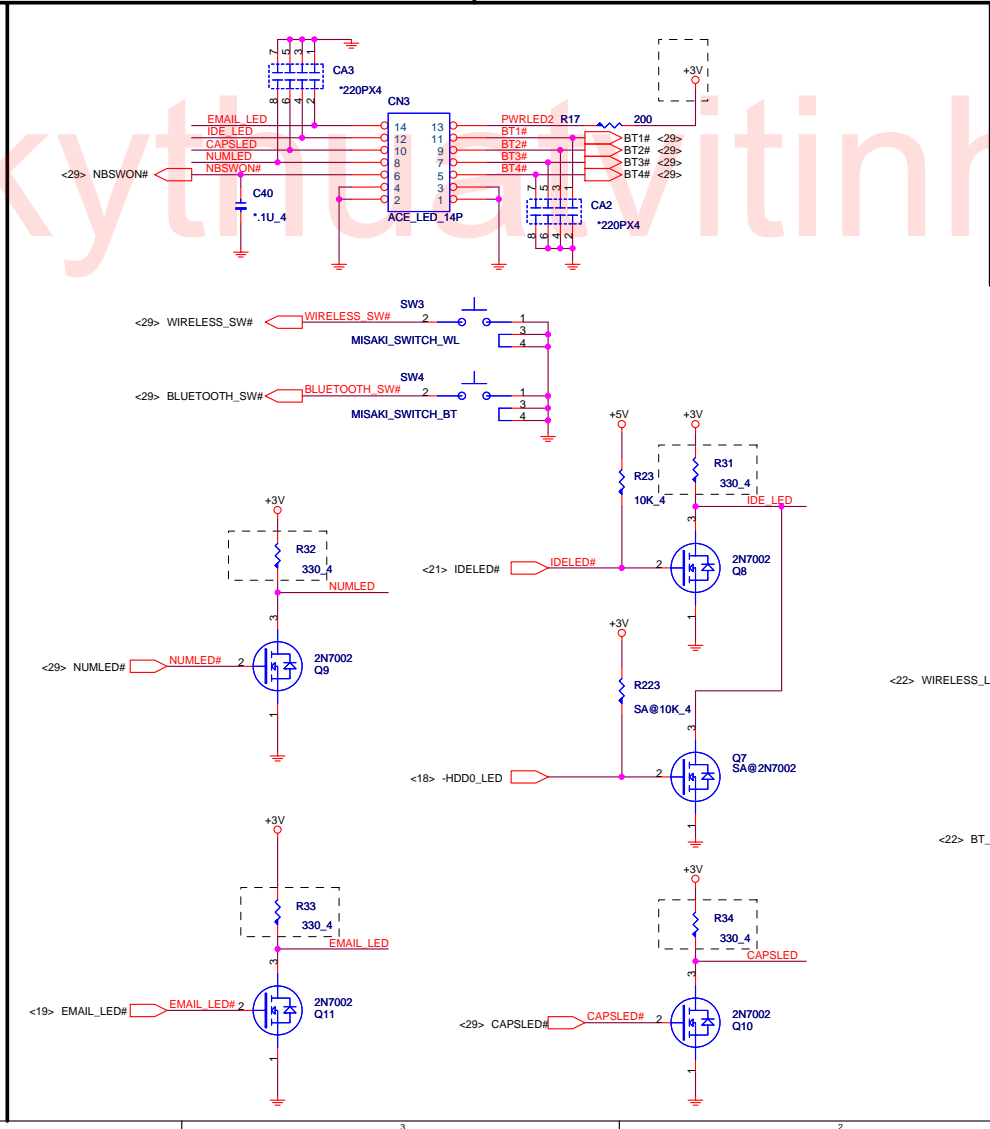
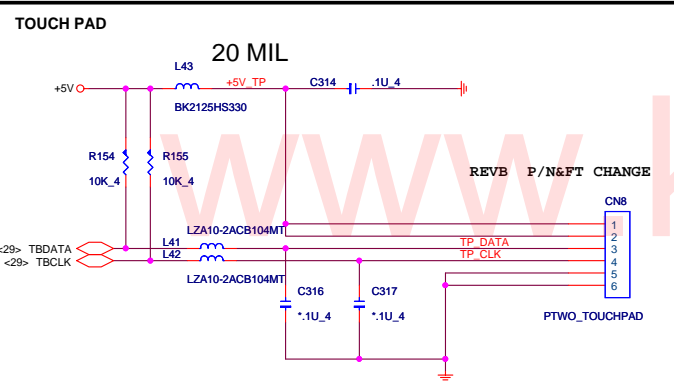
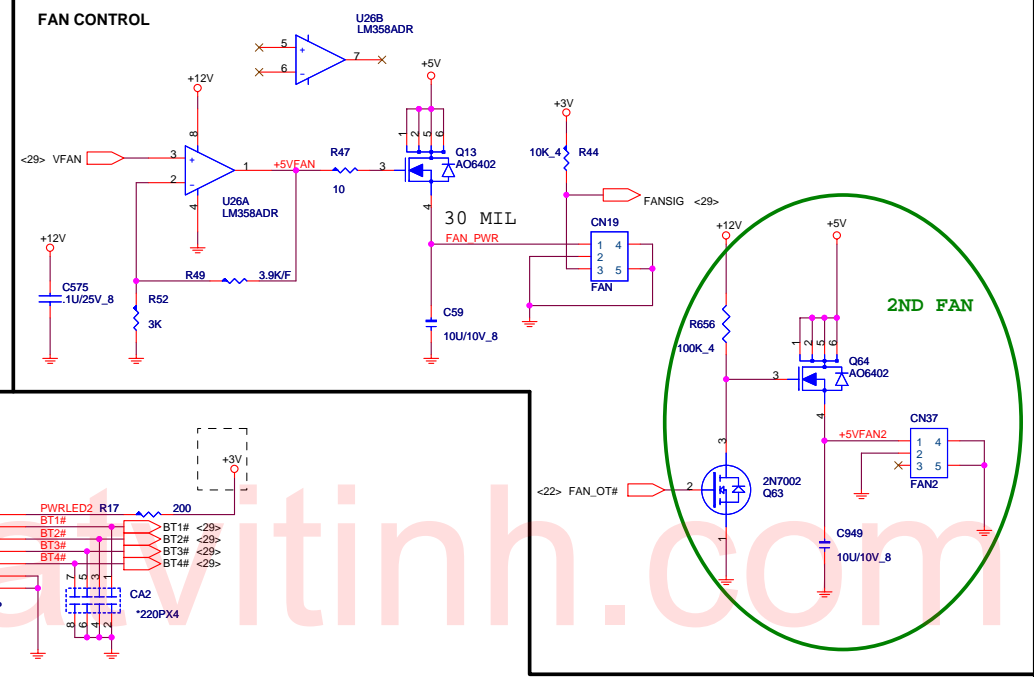
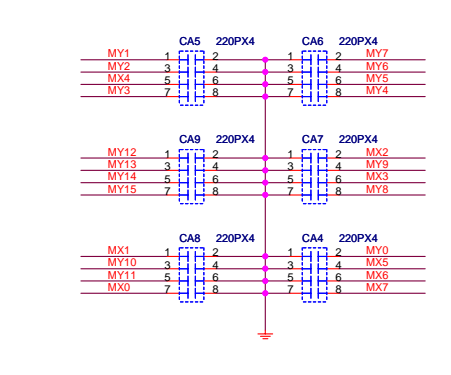
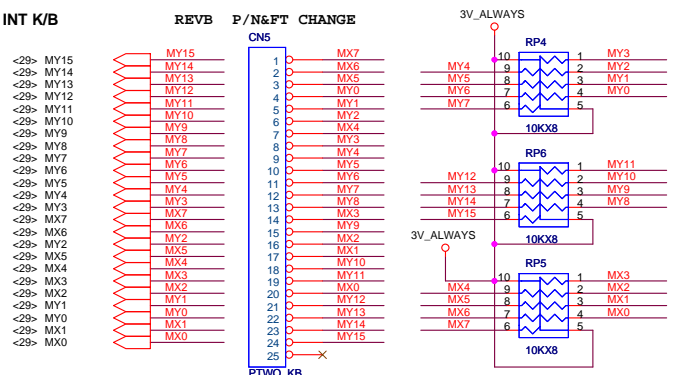
NEW ADD FOR ESD
CLOSE TO CN35

Change to 2N7002

PROJECT : ZL7
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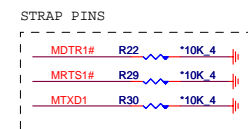
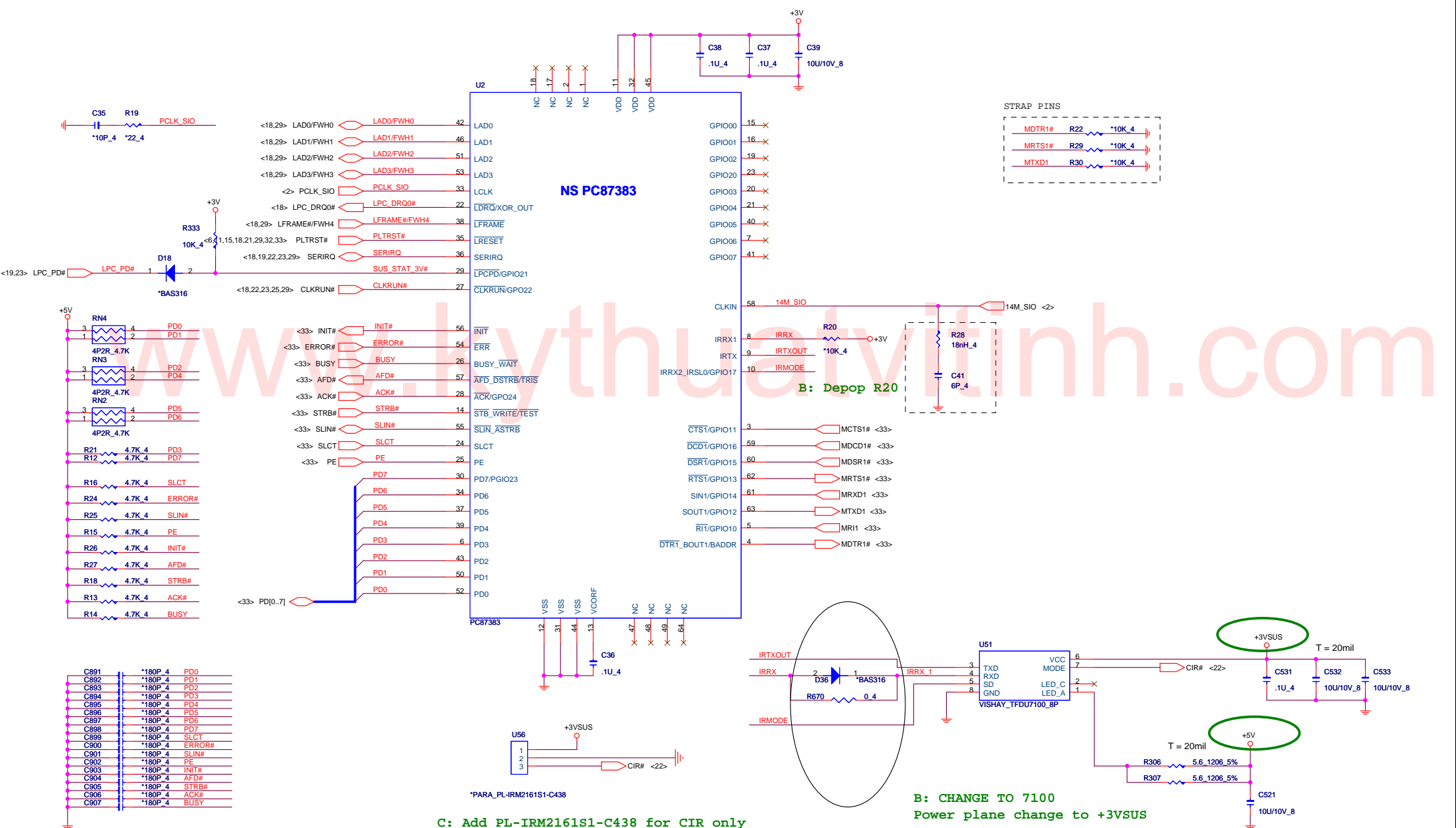
LDRQ#(pin 8) internal is no use





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	T/P,FAN,SWITCH,LED,K/B	C
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B: Depop R20

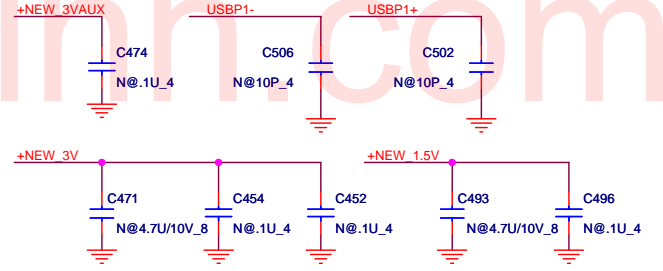
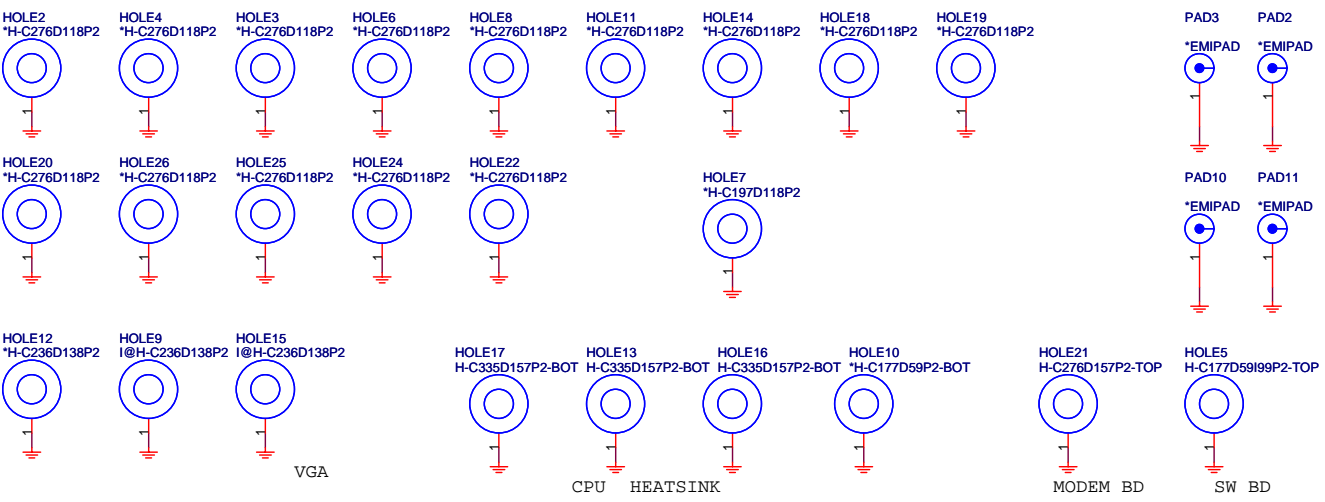
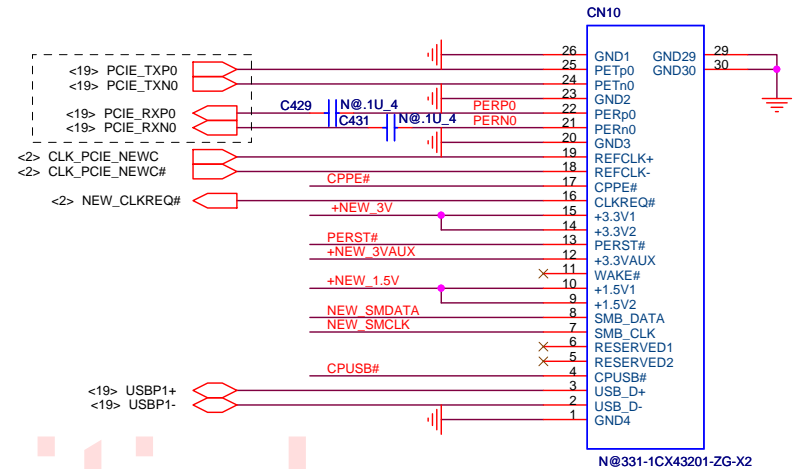
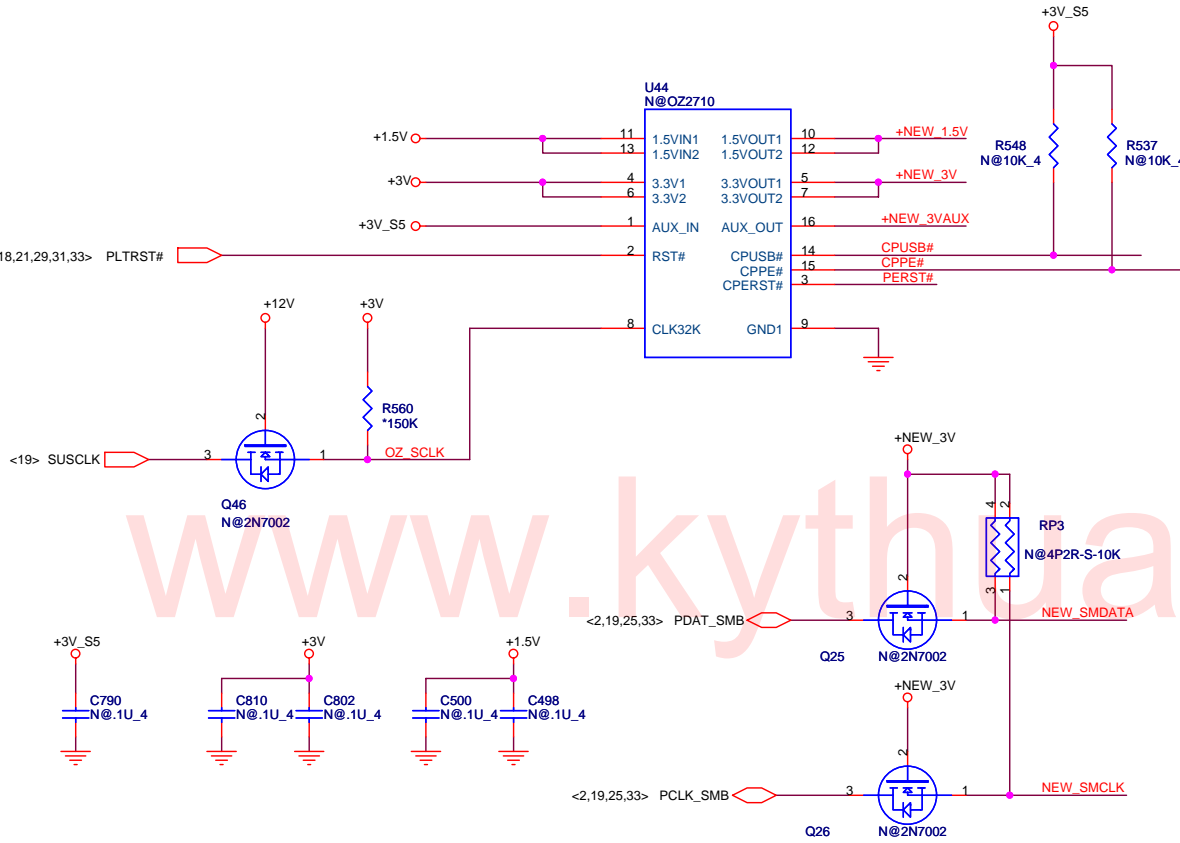
B: CHANGE TO 7100
Power plane change to +3VSUS

C: Add PL-IRM2161S1-C438 for CIR only

*PARA_PL-IRM2161S1-C438

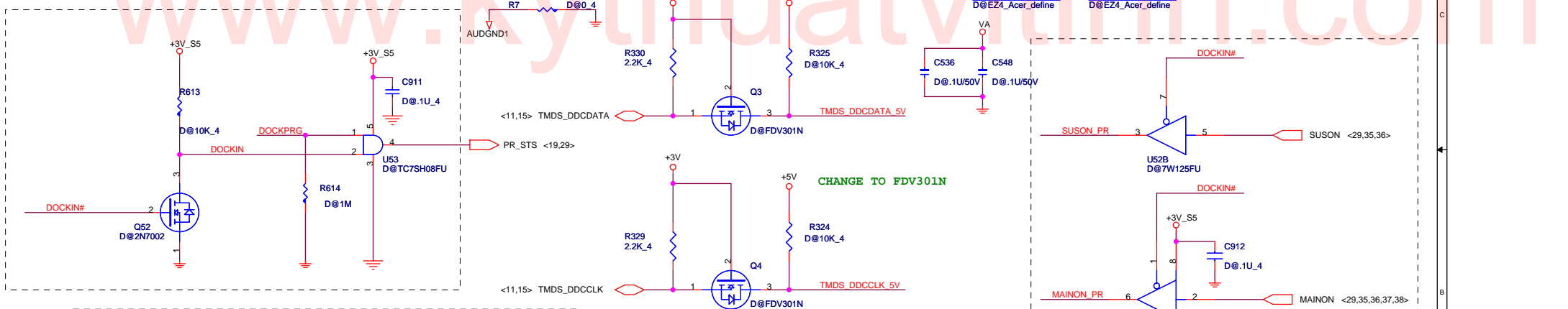
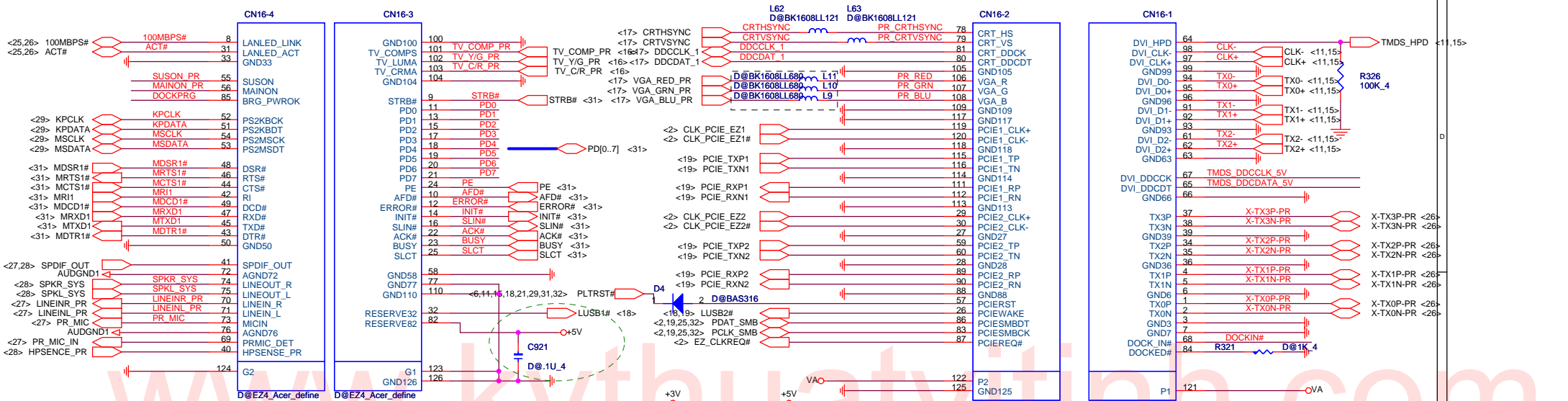
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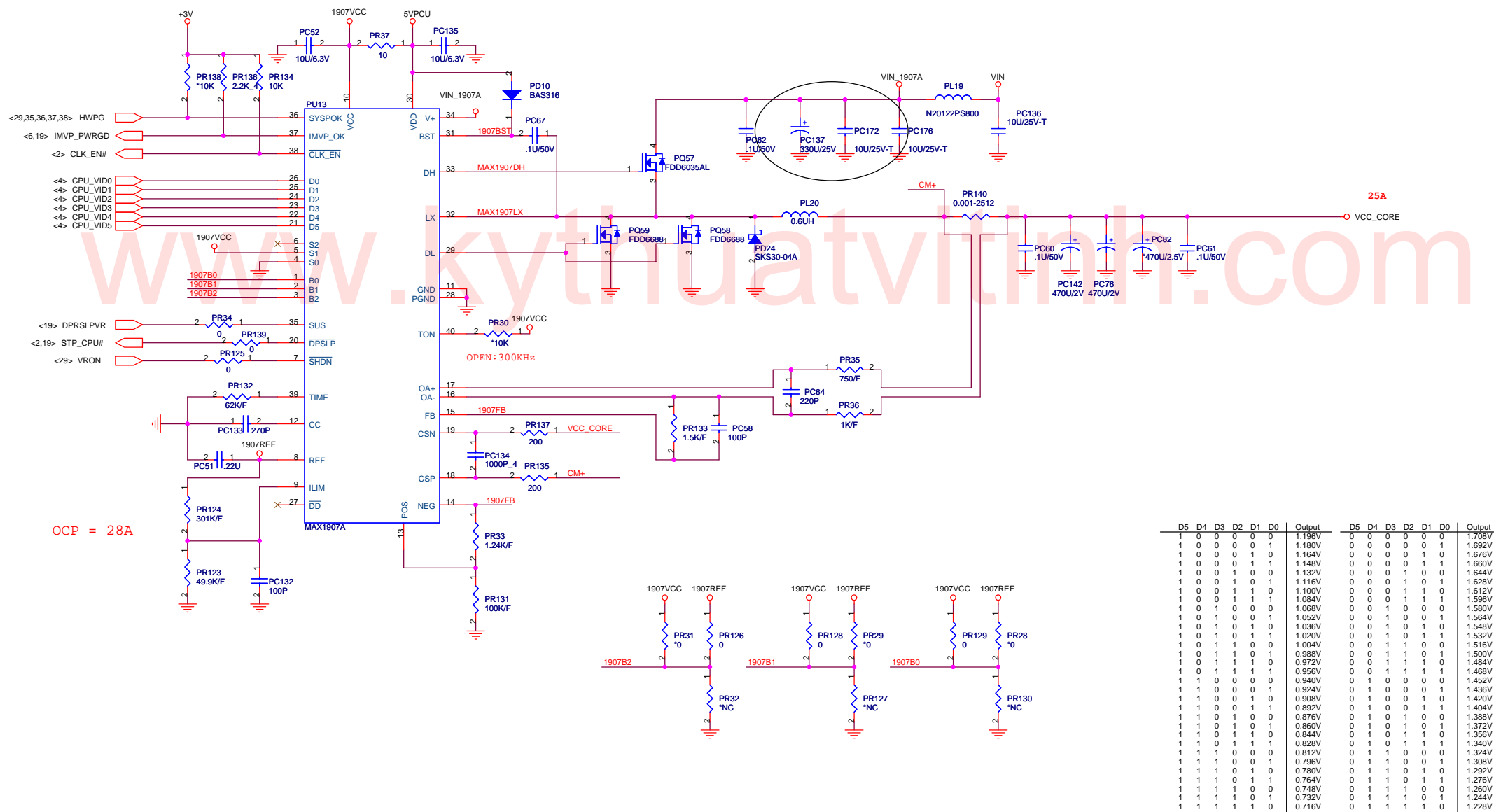
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SPKL_SYS	C543	D@220P_4	PR_CRTHSYNC	C544	*10P_4
SPKR_SYS	C542	D@220P_4	PR_CRTVSYNC	C545	*10P_4
LINEINL_PR	C27	D@220P_4	PR_BLU	C24	D@10P_4
LINEINR_PR	C28	D@220P_4	PR_GRN	C25	D@10P_4
PR_MIC_IN	C13	D@47P_4	PR_RED	C26	D@10P_4
PR_MIC	C23	D@47P_4	CRTVSYNC	C549	*10P_4
100MBPS#	C14	D@1000P_4	CRTHSYNC	C550	*10P_4
ACT#	C17	D@1000P_4	DDCCLK_1	C547	D@10P_4
TV_COMP_PR	C20	D@10P_4	DDCDAT_1	C546	D@10P_4
TV_C/R_PR	C22	D@10P_4	X-TX1P-PR	C16	D@10P_4
TV_Y/G_PR	C21	D@10P_4	X-TX1N-PR	C15	D@10P_4
			X-TX0P-PR	C18	D@10P_4
			X-TX0N-PR	C19	D@10P_4
			X-TX3P-PR	C539	D@10P_4
			X-TX3N-PR	C540	D@10P_4
			X-TX2P-PR	C537	D@10P_4
			X-TX2N-PR	C538	D@10P_4

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OCP = 28A


SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output
✓ OPEN	VCC	GND	0.748V

VCC_BOOT

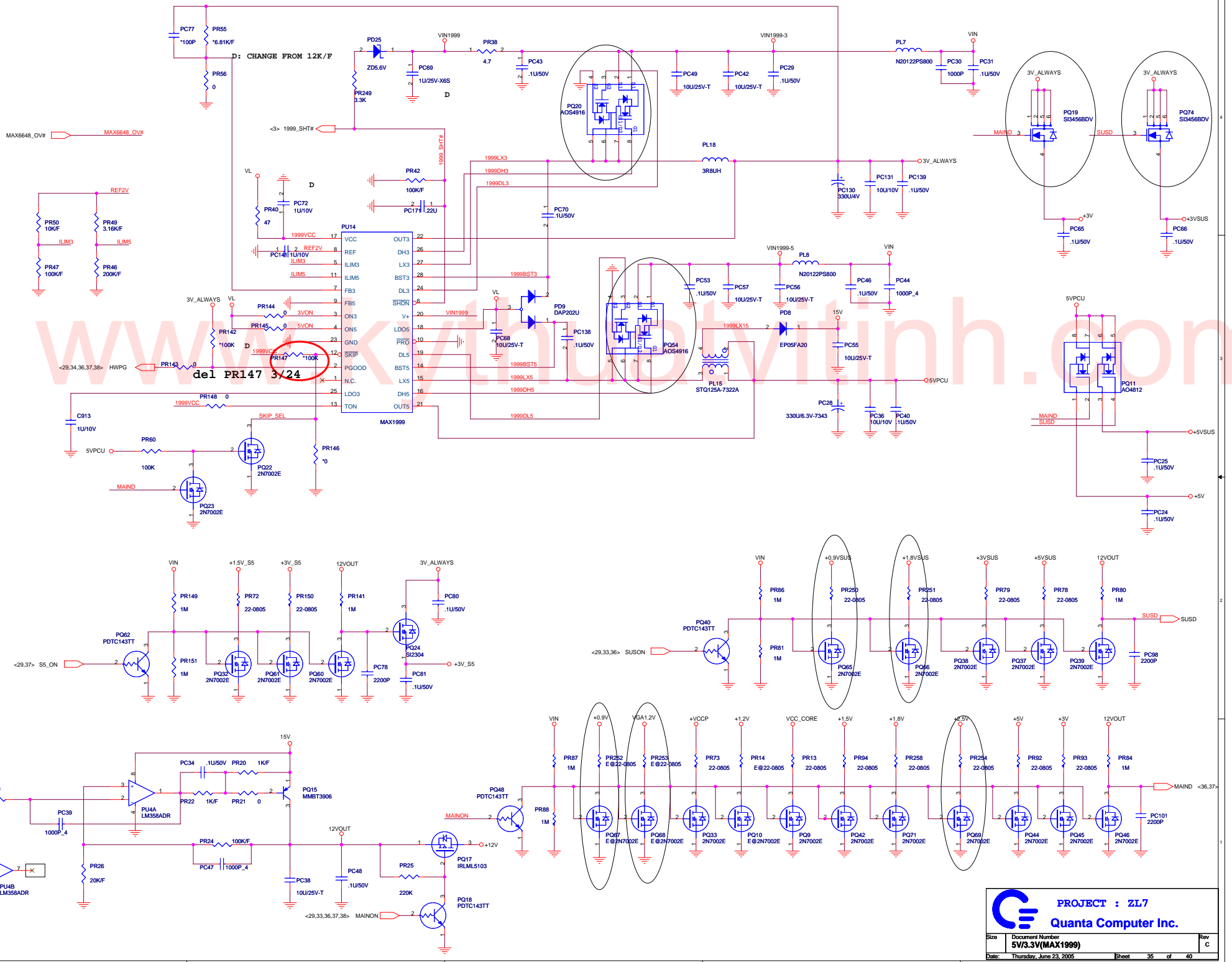
B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
✓ REF	VCC	VCC	1.212V

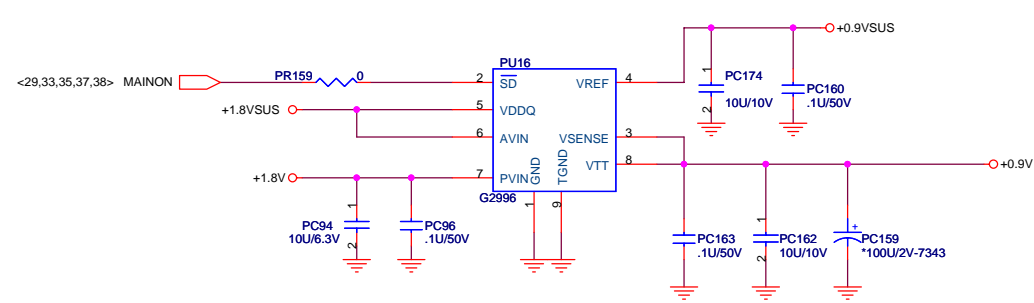
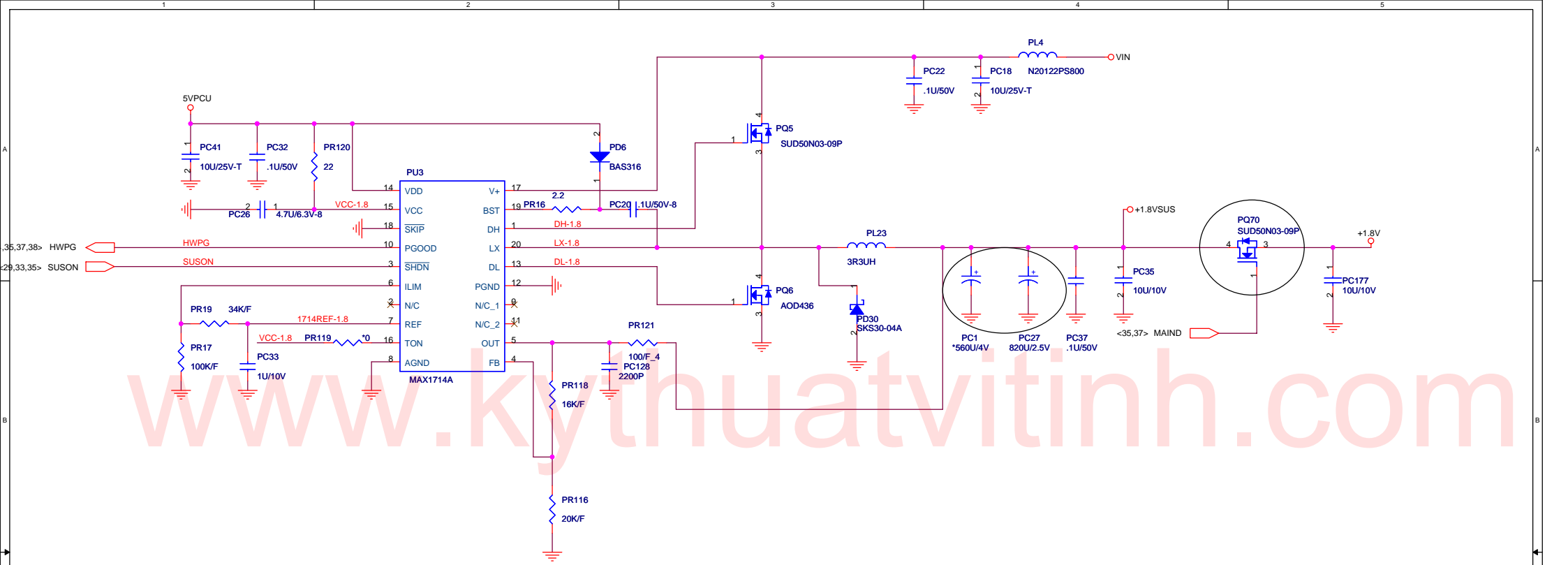
D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	1	0	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	1	0	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	1	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

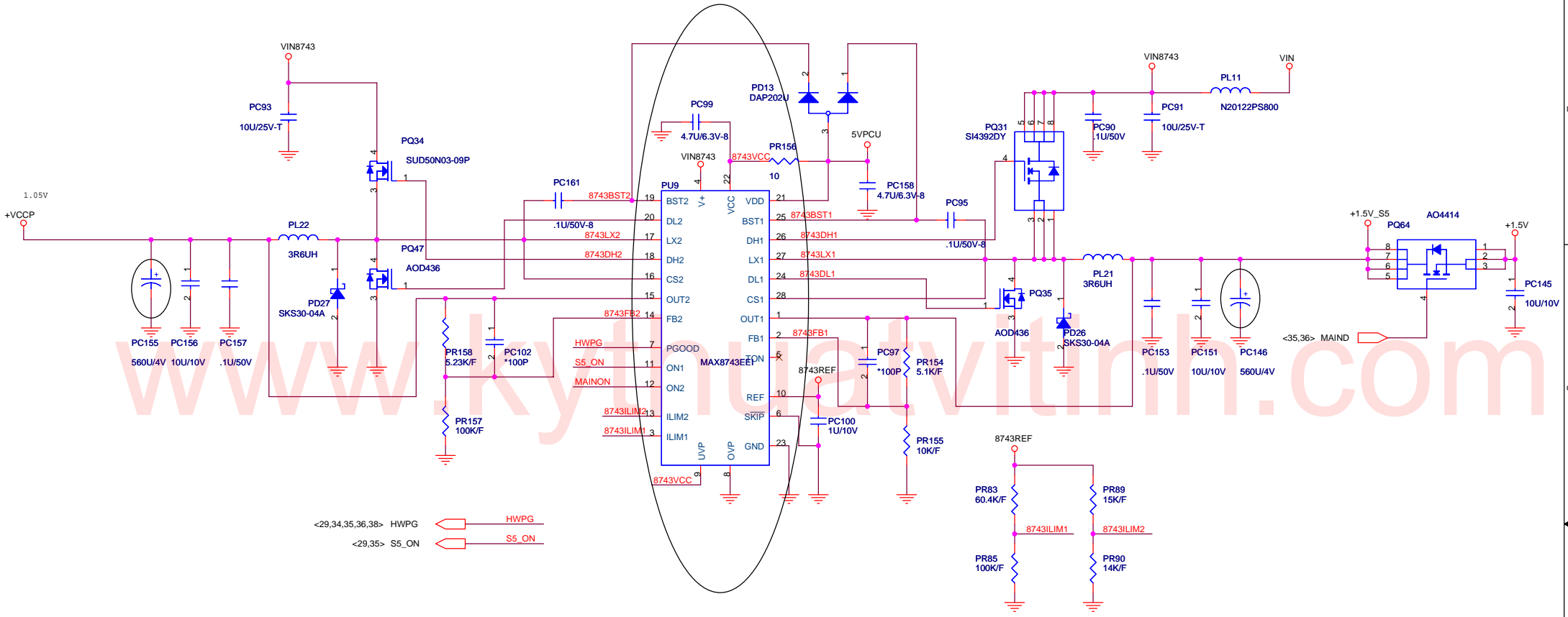


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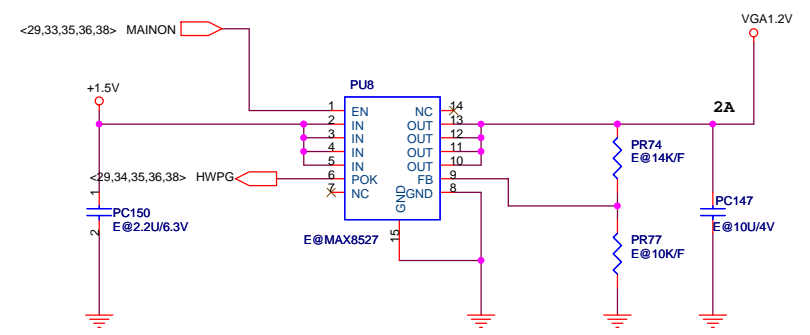
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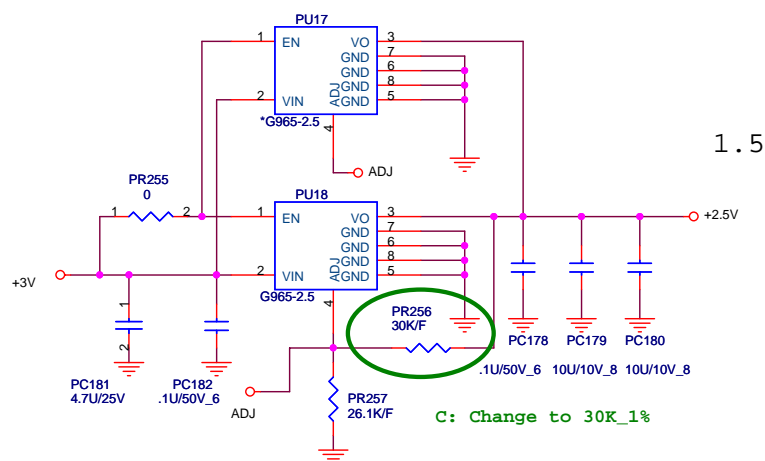
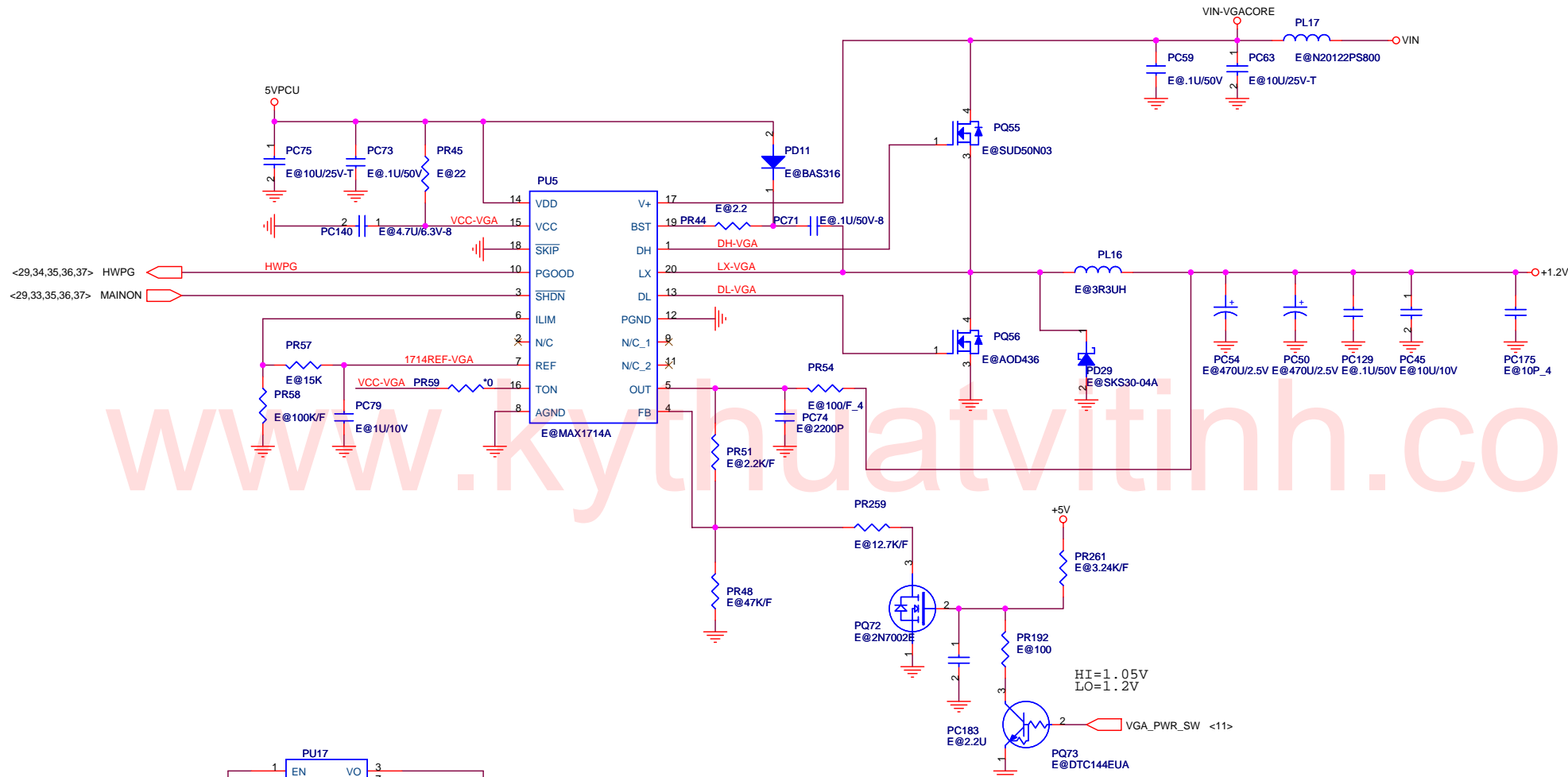






<29,34,35,36,38> HWP
 <29,35> SS_ON

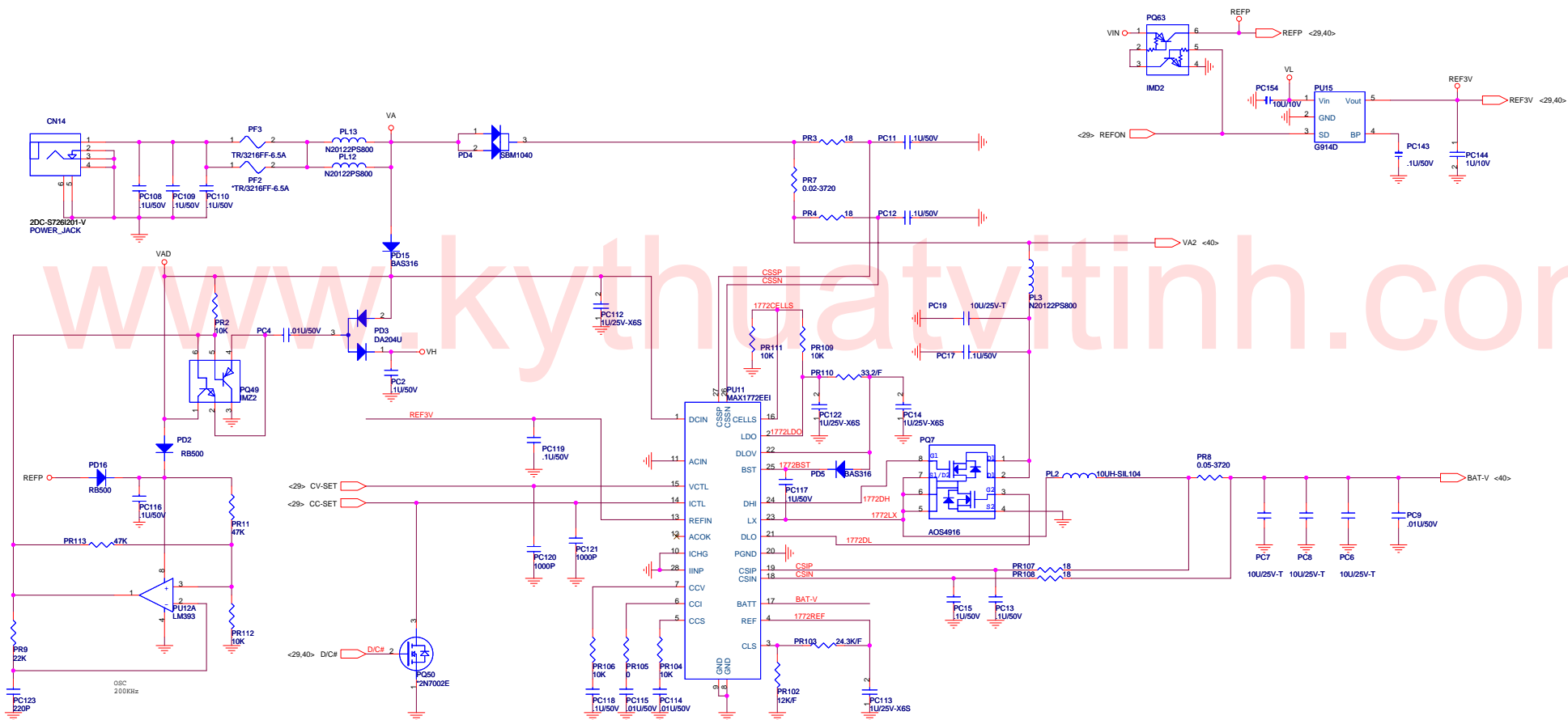




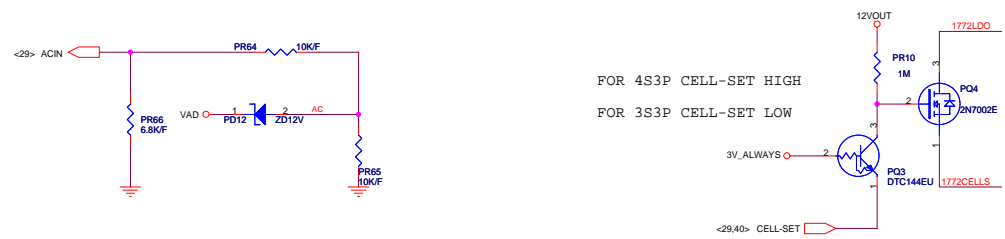
1.5 / 3A

C: Change to 30K_1%

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	+1.2V/+1.8V	C
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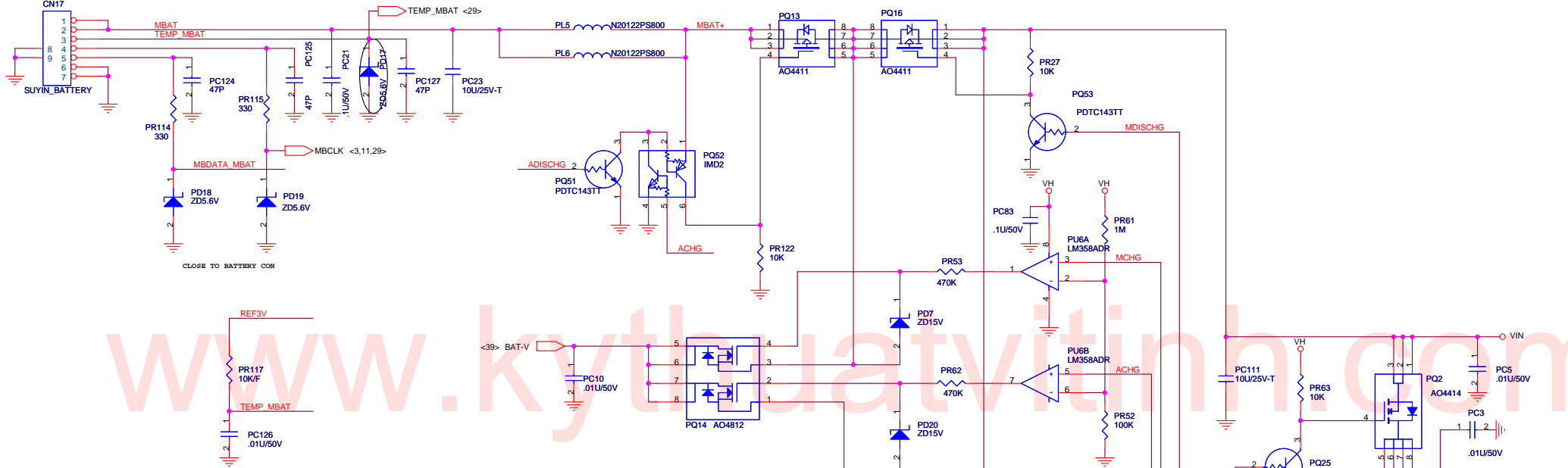


FOR 120W 6.2A

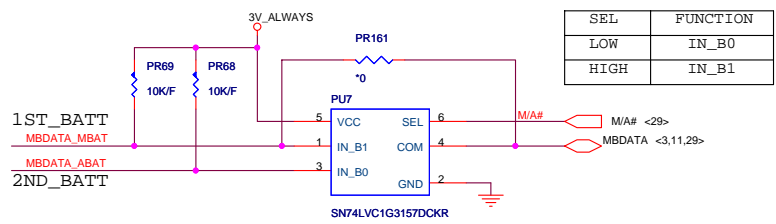
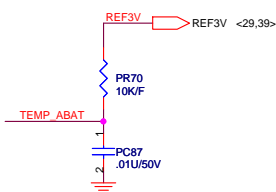
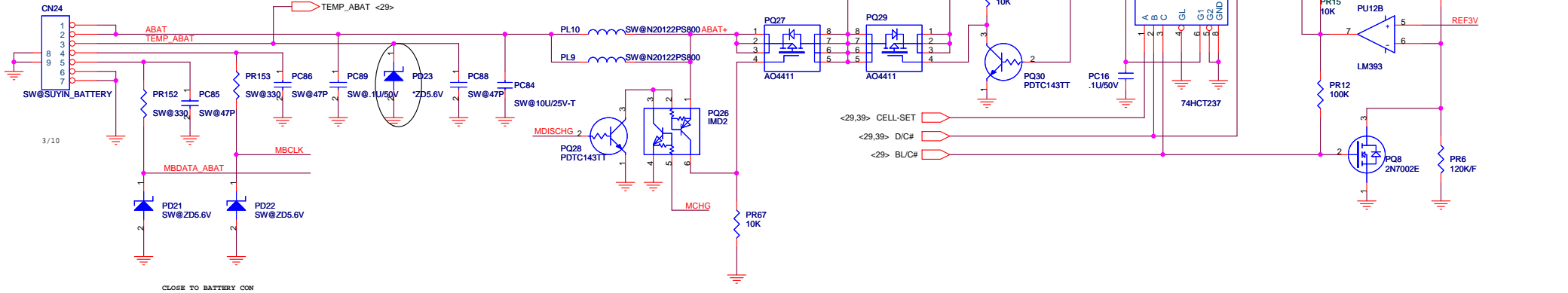


FOR 4S3P CELL-SET HIGH
FOR 3S3P CELL-SET LOW

1ST_BATT_CONN



2ND_BATT_CONN



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

PROJECT : ZL7
Quanta Computer Inc.

Size: Document Number
BATTERY SELECT

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