T-79-07-10

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MC1741S
MC1741SC

ORDERING INFORMATION

Device	Temperature Range	Package
MC1741SG	−55°C to +125°C	Metal Can
MC1741SCD	0°C to +70°C	SO-8
MC1741SCG	0°C to +70°C	Metal Can
MC1741SCP1	0°C to +70°C	Plastic DIP

HIGH SLEW RATE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

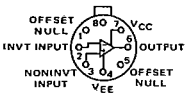
The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

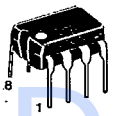
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601-04

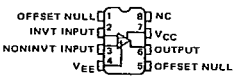


(Top View)



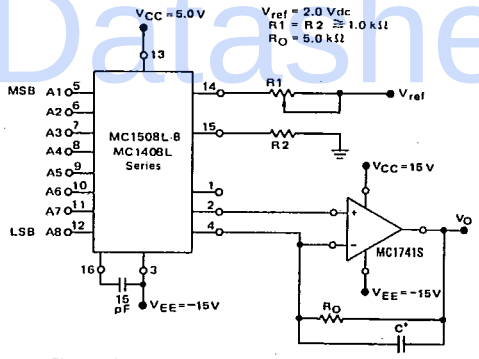
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8



(Top View)

TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Pins not shown are not connected.

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 150 pF).

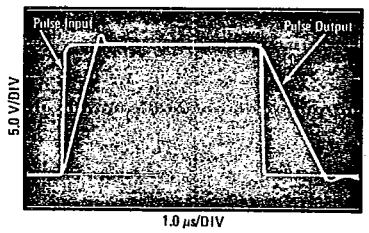
Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

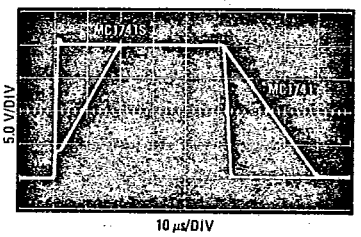
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\,V}{1\,k}(5\,k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\,V\left[\frac{255}{256}\right] = 9.961\,V$$

MC1741S LARGE-SIGNAL TRANSIENT RESPONSE



STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



MC1741S, MC1741SC

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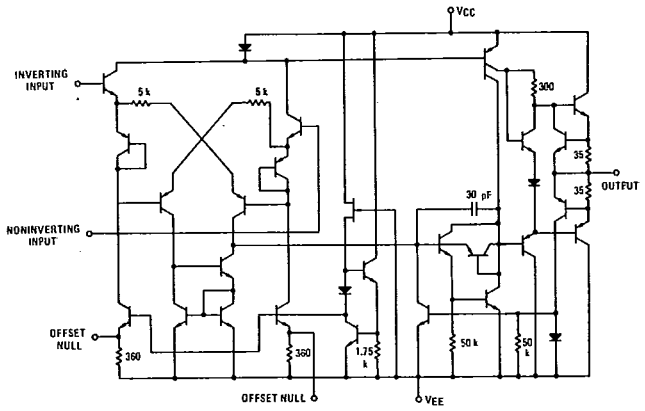
CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		MC1741SC	MC1741S	
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal Voltage	V_{ID}	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	±15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 625 5.0		 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range Metal Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

FIGURE 1 – OFFSET ADJUST CIRCUIT

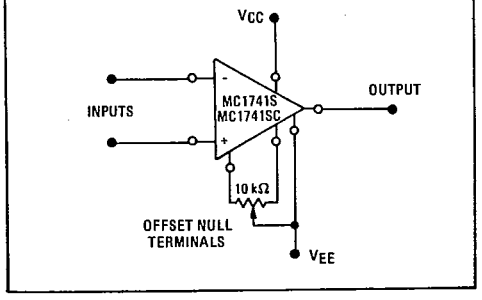
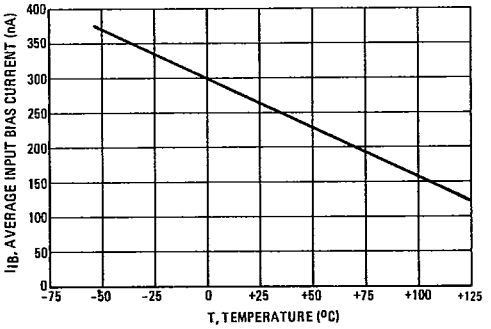


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE



MC1741S, MC1741SC

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ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1741S			MC1741SC			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3) A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)	BW_P	150	200	–	150	200	–	kHz
Large-Signal Transient Response Slew Rate (Figures 10 and 11) V(–) to V(+) V(+) to V(–) Settling Time (Figures 10 and 11) (to within 0.1%)	SR t_{setlg}	 10 10 –	 20 12 3.0	 – – –	 10 10 –	 20 12 3.0	 – – –	 V/μs μs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8) Rise Time Fall Time Propagation Delay Time Overshoot	 t_{TLH} t_{THL} t_{PLH},t_{PHL} OS	 – – – –	 0.25 0.25 0.25 20	 – – – –	 – – – –	 0.25 0.25 0.25 20	 – – – –	 μs μs μs %
Short-Circuit Output Currents	I_{OS}	±10	–	±35	±10	–	±35	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4) V_O = ±10 V, T_A = +25°C V_O = ±10 V, T_A = T_{low}* to T_{high}*	A_{vol}	 50,000 25,000	 200,000 –	 – –	 20,000 15,000	 100,000 –	 – –	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing R_L = 10 kΩ, T_A = T_{low} to T_{high} (MC1741S only) R_L = 2.0 kΩ, T_A = +25°C R_L = 2.0 kΩ, T_A = T_{low} to T_{high}	V_O	 ±12 ±10 ±10	 ±14 ±13 –	 – – –	 ±12 ±10 ±10	 ±14 ±13 –	 – – –	V_{pk}
Input Common-Mode Voltage Range T_A = T_{low} to T_{high} (MC1741S)	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz) T_A = T_{low} to T_{high} (MC1741S)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2) T_A = +25°C and T_{high} T_A = T_{low}	I_{IB}	 – –	 200 500	 500 1500	 – –	 200 –	 500 800	nA
Input Offset Current T_A = +25°C and T_{high} T_A = T_{low}	$\|I_{IO}\|$	 – –	 30 –	 200 500	 – –	 30 –	 200 300	nA
Input Offset Voltage (R_S = ≤10 kΩ) T_A = +25°C T_A = T_{low} to T_{high}	$\|V_{IO}\|$	 – –	 1.0 –	 5.0 6.0	 – –	 2.0 –	 6.0 7.5	mV
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0) T_A = T_{low} to T_{high}	P_C	–	50	85	–	50	85	mW
Positive Voltage Supply Sensitivity (V_{EE} constant) T_A = T_{low} to T_{high} on MC1741S	PSS+	–	2.0	100	–	2.0	150	μV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS-	–	10	150	–	10	150	μV/V

*T_{low} = 0 for MC1741SC
= -55 °C for MC1741S

T_{high} = +70°C for MC1741SC
= +125 °C for MC1741S

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

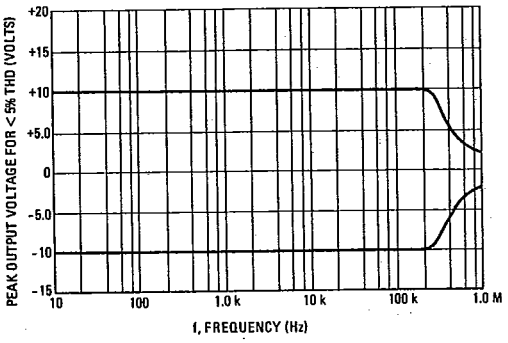


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

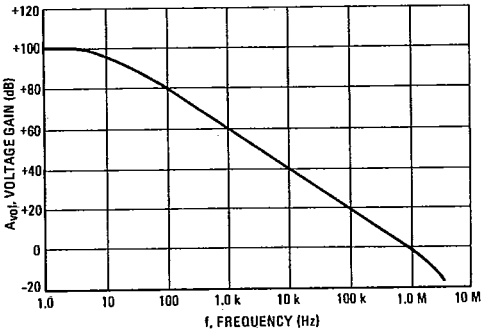


FIGURE 5 – NOISE versus FREQUENCY

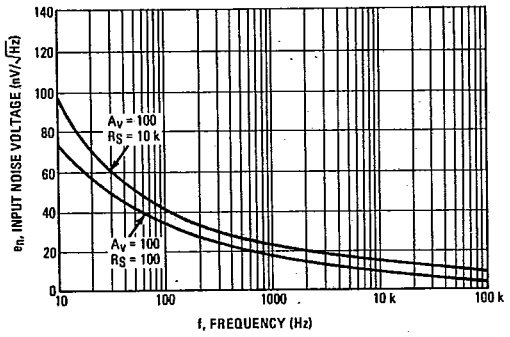


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

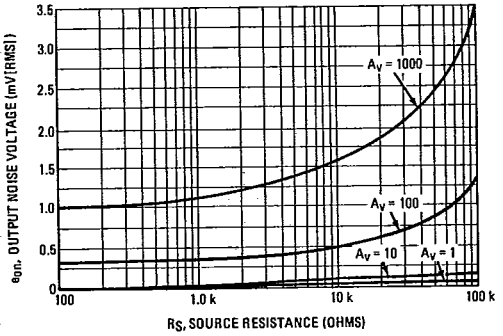


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

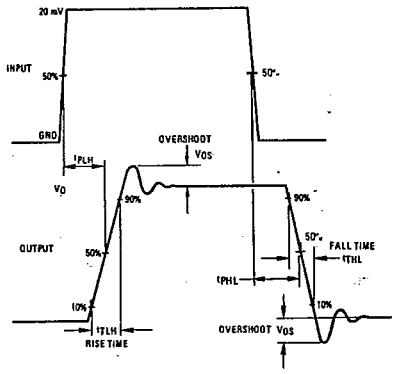
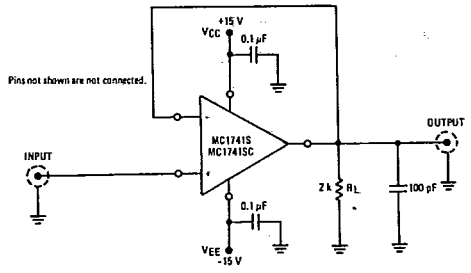


FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 -- POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

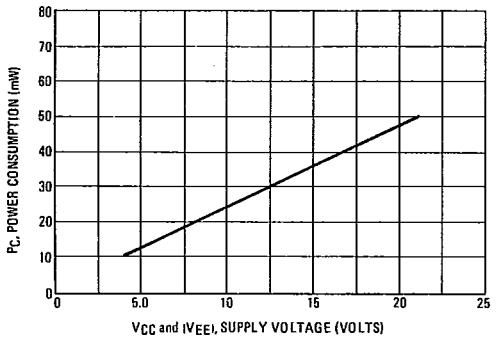


FIGURE 10 -- LARGE-SIGNAL TRANSIENT WAVEFORMS

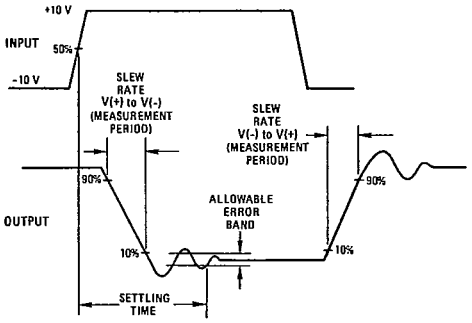
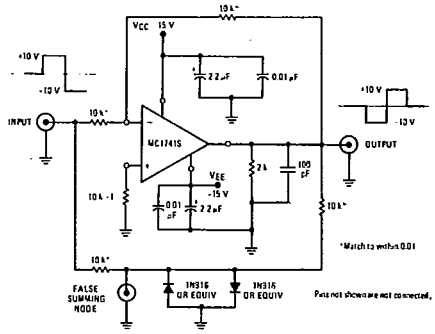


FIGURE 11 -- SETTLING TIME AND SLEW RATE TEST CIRCUIT



SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1741S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

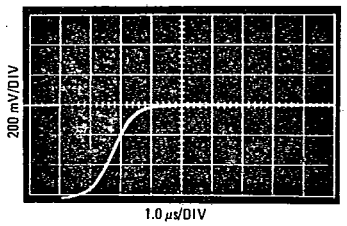
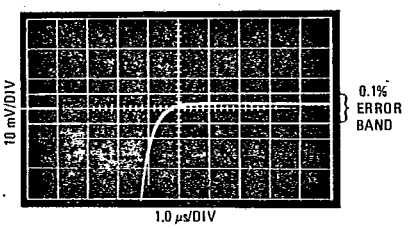
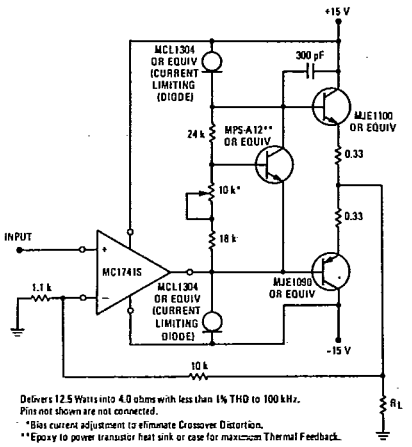


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE



TYPICAL APPLICATION

FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 Watts into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.
*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.