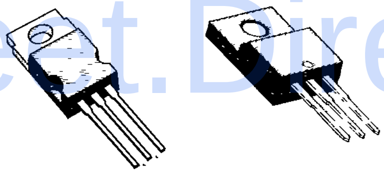
SGS-THOMSON MICROELECTRONICS

S G S-THOMSON

IRF 720/FI-721/FI IRF 722/FI-723/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF720	400 V	1.8 Ω	3.3 A
IRF720FI	400 V	1.8 Ω	2.5 A
IRF721	350 V	1.8 Ω	3.3 A
IRF721FI	350 V	1.8 Ω	2.5 A
IRF722	400 V	2.5 Ω	2.8 A
IRF722FI	400 V	2.5 Ω	2.0 A
IRF723	350 V	2.5 Ω	2.8 A
IRF723FI	350 V	2.5 Ω	2.0 A



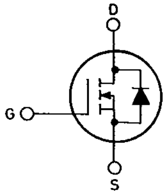
- HIGH VOLTAGE - FOR OFF LINE APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include off-line use, constant current source, ultrasonic equipment and switching powers supplies start-up circuits.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter (TO-220 / ISOWATT220)	IRF 720 / 720FI	721 / 721FI	722 / 722FI	723 / 723FI	Unit
V_{DS} *	Drain-source voltage ($V_{GS}=0$)	400	350	400	350	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)	400	350	400	350	V
V_{GS}	Gate-source voltage	±20				V
I_{DM} (•)	Drain current (pulsed)	13	13	11	11	A
I_{DLM}	Drain inductive current, clamped ($L=100\ \mu H$)	13	13	11	11	A
		720	**721**	**722**	**723**	
I_D	Drain current (cont.) at $T_c=25°C$	3.3	3.3	2.8	2.8	A
I_D	Drain current (cont.) at $T_c=100°C$	2.1	2.1	1.8	1.8	A
		720FI	**721FI**	**722FI**	**723FI**	
I_D ■	Drain current (cont.) at $T_c=25°C$	2.5	2.5	2	2	A
I_D ■	Drain current (cont.) at $T_c=100°C$	1.5	1.5	1.2	1.2	A
		TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at $T_c<25°C$	50		30		W
■	Derating factor	0.40		0.24		W/°C
T_{stg}	Storage temperature	−55 to 150				°C
T_j	Max. operating junction temperature	150				°C

* $T_j=25°C$ to $125°C$
(•) Repetitive Rating: Pulse width limited by max junction temperature.
■ See note on ISOWATT220 on this datasheet.

THERMAL DATA*

			TO-220	ISOWATT220	
$R_{thj-case}$	Thermal resistance junction-case	max	2.50	4.16	°C/W
R_{thc-s}	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

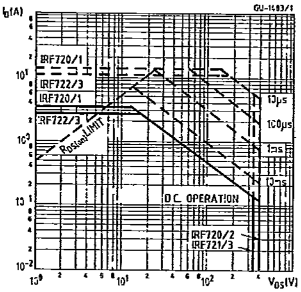
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
OFF					
$V_{(BR)DSS}$ Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF720/722/720FI/722FI** for **IRF721/723/721FI/723FI**	 400 350			 V V
I_{DSS} Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS} Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **					
$V_{GS(th)}$ Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$ On-state drain current	V_{DS} > $I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V for **IRF720/721/720FI/721FI** for **IRF722/723/722FI/723FI**	 3.3 2.8			 A A
$R_{DS(on)}$ Static drain-source on resistance	V_{GS} = 10 V I_D = 1.8 A for **IRF720/721/720FI/721FI** for **IRF722/723/722FI/723FI**			 1.8 2.5	 Ω Ω
DYNAMIC					
g_{fs} ** Forward transconductance	V_{DS} > $I_{D(on)} \times R_{DS(on)max}$ I_D = 1.8 A	1.0			mho
C_{iss} Input capacitance C_{oss} Output capacitance C_{rss} Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			600 200 40	pF pF pF
SWITCHING					
$t_{d(on)}$ Turn-on time t_r Rise time $t_{d(off)}$ Turn-off delay time t_f Fall time	V_{DD} = 175 V I_D = 1.5 A R_i = 50 Ω (see test circuit)			40 50 100 50	ns ns ns ns
Q_g Total Gate Charge	V_{GS} = 10 V I_D = 3.3 A V_{DS} = Max Rating × 0.8 (see test circuit)			15	nC

ELECTRICAL CHARACTERISTICS (Continued)

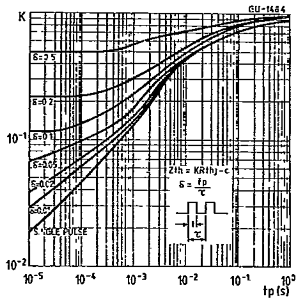
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					3.3 13	A A
V_{SD}	Forward on voltage	I_{SD} = 3.3 A	V_{GS} = 0			1.6	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 3.3 A	di/dt = 100 A/μs		450 3.1		ns μC

** Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

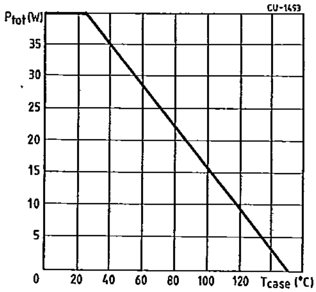
Safe operating areas (standard package)



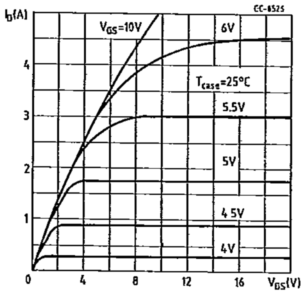
Thermal impedance (standard package)



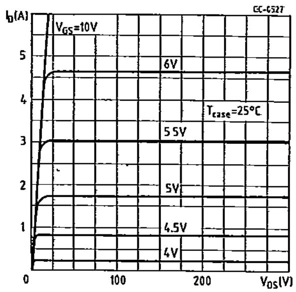
Derating curve (standard package)



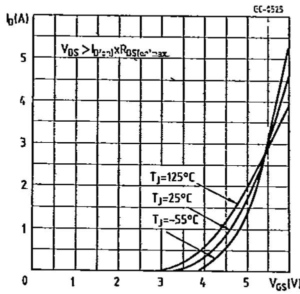
Output characteristics



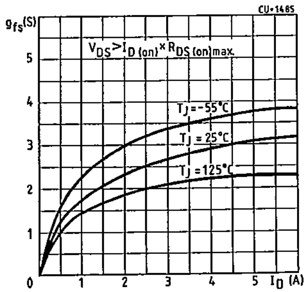
Output characteristics



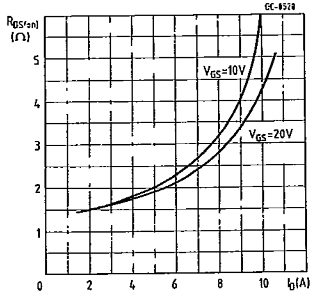
Transfer characteristics



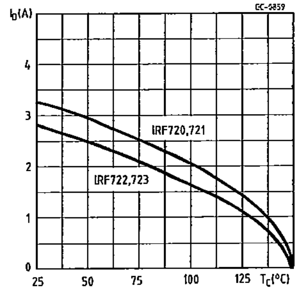
Transconductance



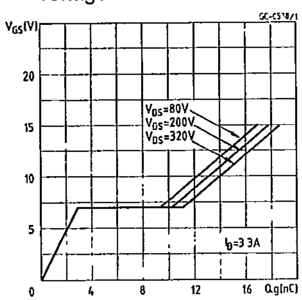
Static drain-source on resistance



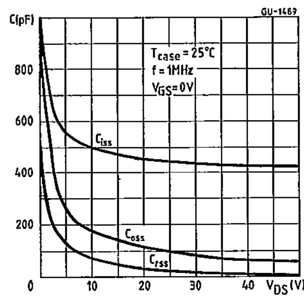
Maximum drain current vs temperature



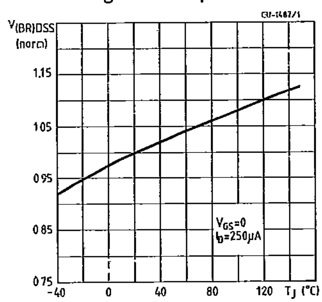
Gate charge vs gate-source voltage



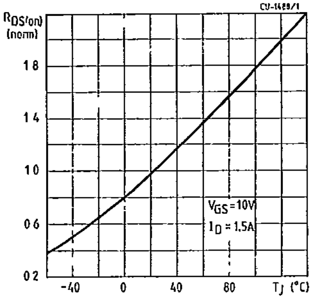
Capacitance variation



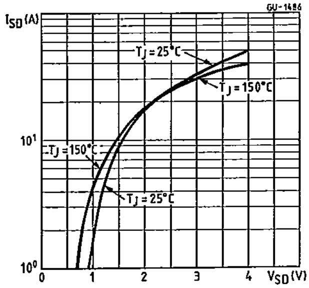
Normalized breakdown voltage vs temperature



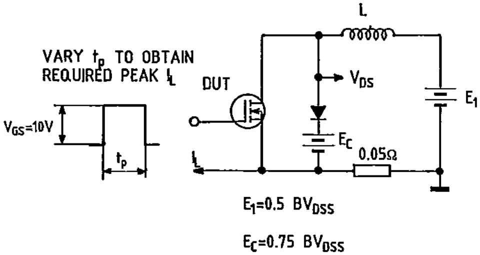
Normalized on resistance vs temperature



Source-drain diode forward characteristics

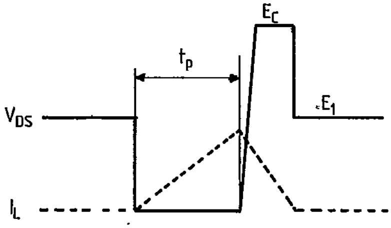


Clamped inductive test circuit



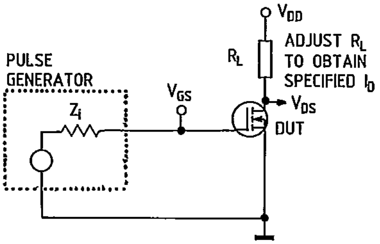
SC-0242

Clamped inductive waveforms



SC-0243

Switching times test circuit



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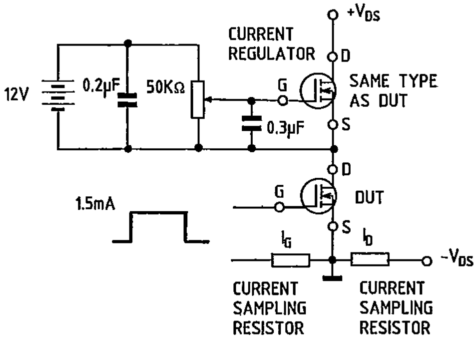
Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (\text{at } 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\,(tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

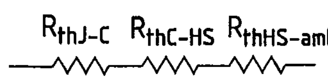
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

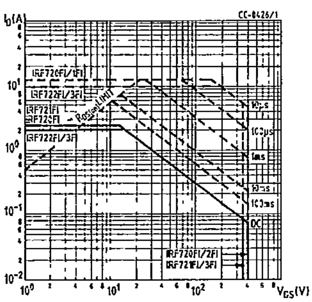
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

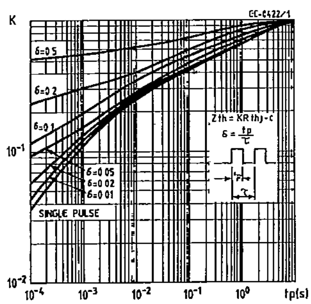


ISOWATT DATA

Safe operating areas



Thermal impedance



Derating curve