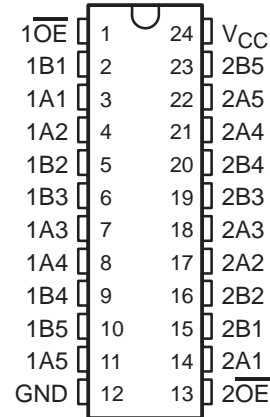


**SN74CBTS3384**  
**10-BIT FET BUS SWITCH**  
**WITH SCHOTTKY DIODE CLAMPING**  
SCDS0241 – MAY 1995 – REVISED MAY 2000

- Functionally Equivalent to QS3384 and QS3L384
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



**description**

The SN74CBTS3384 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit bus switches with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBTS3384 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**  
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
$\overline{1OE}$	$\overline{2OE}$	1B1–1B5	2B1–2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z



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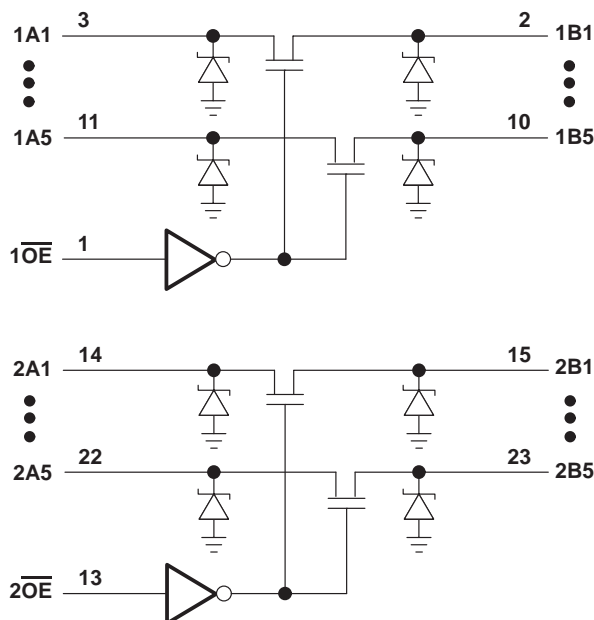
# SN74CBTS3384

## 10-BIT FET BUS SWITCH

### WITH SCHOTTKY DIODE CLAMPING

SCDS024I – MAY 1995 – REVISED MAY 2000

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Continuous channel current	.....	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ )	.....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):		
DB package	.....	63°C/W
DBQ package	.....	61°C/W
DGV package	.....	86°C/W
DW package	.....	46°C/W
PW package	.....	88°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-0.6	V	
$I_I$	$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = \text{GND}$			-1	$\mu\text{A}$	
	$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 5.5\text{ V}$			150		
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$I_O = 0$ , $V_I = V_{CC}$ or GND			3	$\mu\text{A}$	
$\Delta I_{CC}^\ddagger$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA	
$C_i$	Control inputs	$V_I = 3\text{ V}$ or 0				6	pF	
$C_{iO}(\text{OFF})$		$V_O = 3\text{ V}$ or 0,	$\overline{OE} = V_{CC}$			6.5	pF	
$r_{on}^\S$		$V_{CC} = 4\text{ V}$ , TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$ ,	$I_I = 15\text{ mA}$		14	20	$\Omega$
			$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$		5	
	$I_I = 30\text{ mA}$				5	7		
	$V_I = 2.4\text{ V}$ ,	$I_I = 15\text{ mA}$		10	15			

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

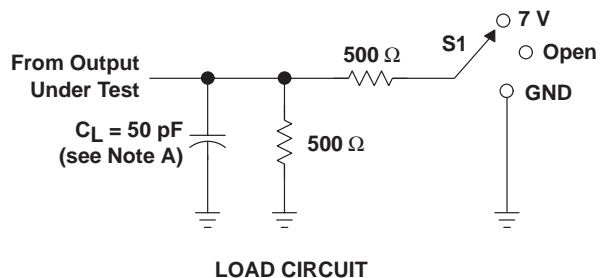
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\parallel$	A or B	B or A	0.35		0.25		ns
$t_{en}$	$\overline{OE}$	A or B		6.2	1.9	5.7	ns
$t_{dis}$	$\overline{OE}$	A or B		5.5	2.1	5.2	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

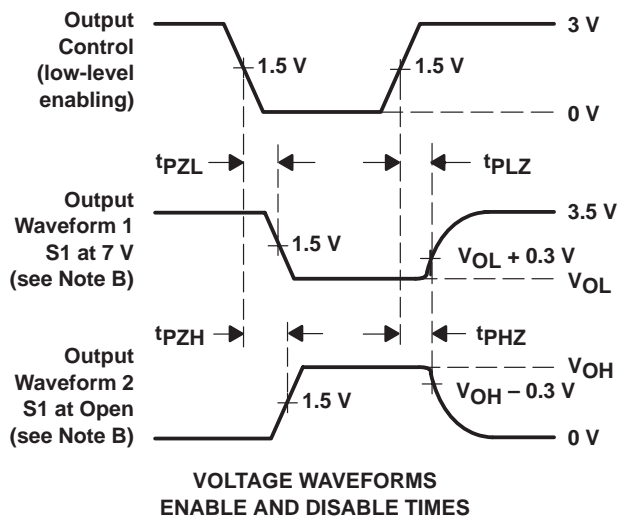
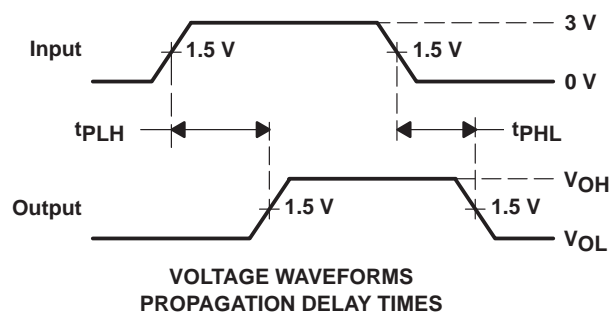
# SN74CBTS3384 10-BIT FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS024I – MAY 1995 – REVISED MAY 2000

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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## SN74CBTS3384, 10-Bit FET Bus Switch With Schottky Diode Clamping

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Related Documents](#)
- > [Training](#)

Parameter Name	SN74CBTS3384
Voltage Nodes (V)	4, 5
Vcc range (V)	4.0 to 5.5
No. of Bits	10
ron(max) (ohms)	7
tpd(max) (ns)	0.25


## Description

The SN74CBTS3384 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit bus switches with separate output-enable (OE\ ) inputs. When OE\ is low, the switch is on, and port A is connected to port B. When OE\ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBTS3384 is characterized for operation from -40°C to 85°C.

## Features

- Functionally Equivalent to QS3384 and QS3L384
- 5-  Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB, DBQ), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

To view the following documents, [Acrobat Reader 3.x](#) is required.

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## Datasheets

Full datasheet in Acrobat PDF: [scds024i.pdf](#) (71 KB)

Full datasheet in Zipped PostScript: [scds024i.psz](#) (69 KB)

## Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>Availability / Samples</u>
SN74CBTS3384DBLE	<a href="#">DB</a>	24	-40 TO 85	OBSOLETE			
SN74CBTS3384DBQR	<a href="#">DBQ</a>	24	-40 TO 85	ACTIVE	1.34	2500	<a href="#">Check stock or order</a>
SN74CBTS3384DBR	<a href="#">DB</a>	24	-40 TO 85	ACTIVE	1.17	2000	<a href="#">Check stock or order</a>
SN74CBTS3384DW	<a href="#">DW</a>	24	-40 TO 85	ACTIVE	1.40	25	<a href="#">Check stock or order</a>
SN74CBTS3384DWR	<a href="#">DW</a>	24	-40 TO 85	ACTIVE	1.20	2000	<a href="#">Check stock or order</a>
SN74CBTS3384PWLE	<a href="#">PW</a>	24	-40 TO 85	OBSOLETE			
SN74CBTS3384PWR	<a href="#">PW</a>	24	-40 TO 85	ACTIVE	1.17	2000	<a href="#">Check stock or order</a>

## Application Reports

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- [5-V To 3.3-V Translation With The SN74CBTD3384](#) (SCDA003B - Updated: 03/01/1997)
- [Flexible Voltage-Level Translation With CBT Family Devices](#) (SCDA006 - Updated: 07/20/1999)
- [Implications Of Slow Or Floating CMOS Inputs](#) (SCBA004C - Updated: 02/01/1998)
- [Low-Voltage Bus-Switch Technology And Applications](#) (SCDA005 - Updated: 12/01/1997)
- [Migration From 3.3-V To 2.5-V Power Supplies For Logic Devices](#) (SCEA005 - Updated: 12/01/1997)
- [SN74CBTS3384 Bus Switches Provide Fast Connection And Ensure Isolation](#) (SCDA002A - Updated: 08/01/1996)
- [TI Logic Solutions for Memory Interleaving With the Intel440BX Chipset](#) (SCCA001 - Updated: 04/08/1999)
- [Texas Instruments Crossbar Switches](#) (SCDA001A - Updated: 06/01/1995)
- [Texas Instruments Solution for Undershoot Protection for Bus Switches](#) (SCDA007 - Updated: 04/13/2000)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)

## Related Documents

- [Documentation Rules \(SAP\) And Ordering Information](#) (SZZU001B, 4 KB - Updated: 05/06/1999)
- [Logic Selection Guide Second Half 2000](#) (SDYU001N, 5035 KB - Updated: 04/17/2000)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 284 KB - Updated: 07/28/2000)
- [More Power In Less Space - Technical Article](#) (SCAU001A, 850 KB - Updated: 03/01/1996)

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