

Avalanche Energy Rated N-Channel Power MOSFETs

8A and 7A, 500V-400V
 $r_{DS(on)} = 0.85\Omega$ and 1.1Ω

Features:

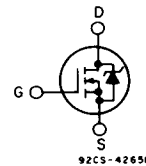
- Single pulse avalanche energy rated
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance

Datasheet.Directory

The IRF840R, IRF841R, IRF842R and IRF843R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

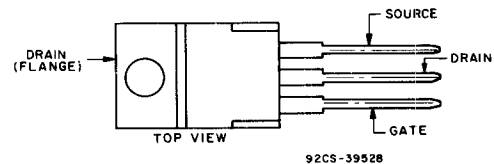
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-220AB

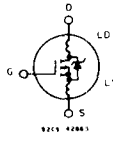
Absolute Maximum Ratings

Parameter	IRF840R	IRF841R	IRF842R	IRF843R	Units
V_{DS} Drain - Source Voltage ①	500	450	500	450	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ K}\Omega$) ①	500	450	500	450	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	8.0	8.0	7.0	7.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM} Pulsed Drain Current ③	32	32	28	28	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	125 (See Fig. 14)				W
Linear Derating Factor	1.0 (See Fig. 14)				W/ $^\circ\text{C}$
E_{as} Single Pulse Avalanche Energy Rating ④	510				mj
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

Rugged Power MOSFETs

IRF840R, IRF841R IRF842R, IRF843R

Electrical Characteristics @ $T_c = 25^\circ\text{C}$ (Unless Otherwise Specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	IRF840R IRF842R	500	—	—	V	V _{GS} = 0V I _D = 250μA	
	IRF841R IRF843R	450	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C	
I _{D(on)} On-State Drain Current ②	IRF840R IRF841R	8.0	—	—	A	V _{DS} > I _{D(on)} x R _{DSON(max)} , V _{GS} = 10V	
	IRF842R IRF843R	7.0	—	—	A		
R _{DSON} Static Drain-Source On-State Resistance ②	IRF840R IRF841R	—	0.8	0.85	Ω	V _{GS} = 10V, I _D = 4.0A	
	IRF842R IRF843R	—	1.0	1.1	Ω		
	ALL	—	—	—	—		
g _{fs} Forward Transconductance ②	ALL	4.0	6.5	—	S(Ω)	V _{DS} > I _{D(on)} x R _{DSON(max)} , I _D = 4.0A	
C _{iss} Input Capacitance	ALL	—	1225	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10	
C _{oss} Output Capacitance	ALL	—	200	—	pF		
C _{rss} Reverse Transfer Capacitance	ALL	—	85	—	pF		
t _{D(on)} Turn-On Delay Time	ALL	—	17	35	ns	V _{DD} = 200V, I _D = 4.0A, Z ₀ = 4.7Ω See Fig. 17	
t _r Rise Time	ALL	—	5	15	ns		
t _{D(off)} Turn-Off Delay Time	ALL	—	42	90	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t _f Fall Time	ALL	—	14	30	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	42	60	nC	V _{GS} = 10V, I _D = 10A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	20	—	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	22	—	nC		
L _D Internal Drain Inductance	—	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
	ALL	—	4.5	—	nH		
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

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Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	1.0	°C/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF840R IRF841R	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	IRF842R IRF843R	—	—	7.0	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRF840R IRF841R	—	—	32	A	
	IRF842R IRF843R	—	—	28	A	
V _{SD} Diode Forward Voltage ②	IRF840R IRF841R	—	—	2.0	V	T _C = 25°C, I _S = 8.0A, V _{GS} = 100A/μs
	IRF842R IRF843R	—	—	1.9	V	T _C = 25°C, I _S = 7.0A, V _{GS} = 100A/μs
t _{rr} Reverse Recovery Time	ALL	—	1100	—	ns	T _J = 150°C, I _R = 8.0A, dI _R /dt = 100A/μs
Q _{RR} Reverse Recovered Charge	ALL	—	6.4	—	μC	T _J = 150°C, I _R = 8.0A, dI _R /dt = 100A/μs
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50V, starting T_J = 25°C, L = 9.1 mH, R_{GS} = 50Ω, I_{peak} = 10A. See figures 15, 16.

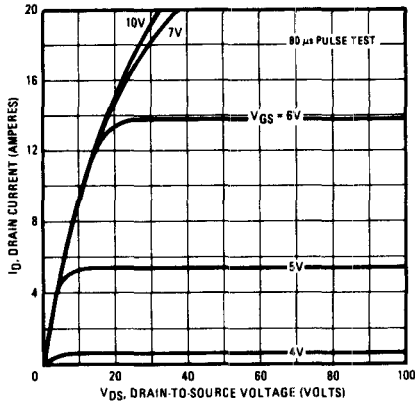


Fig. 1 - Typical Output Characteristics

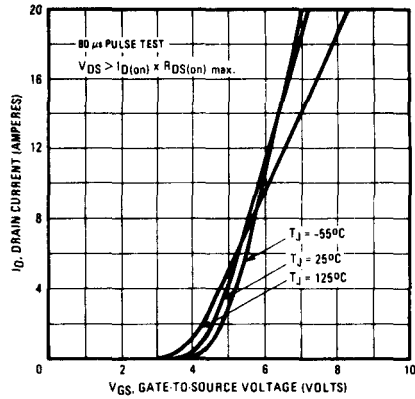


Fig. 2 - Typical Transfer Characteristics

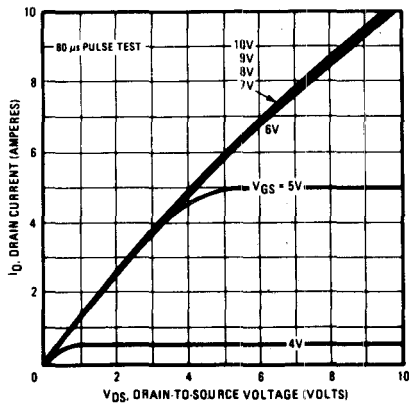


Fig. 3 - Typical Saturation Characteristics

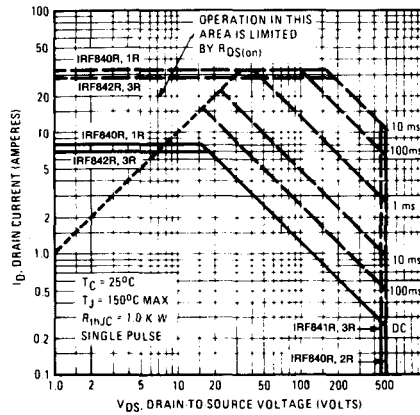


Fig. 4 - Maximum Safe Operating Area

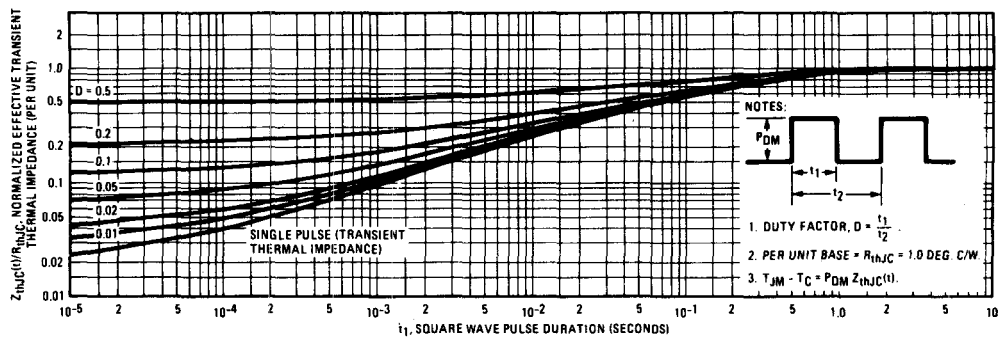


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF840R, IRF841R
IRF842R, IRF843R

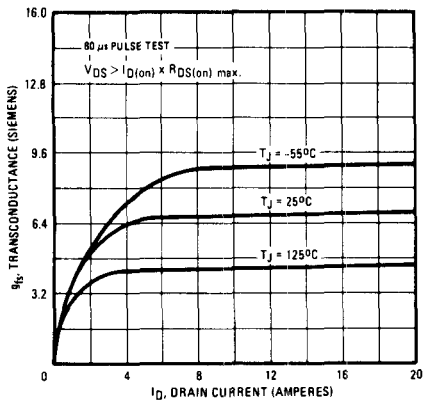


Fig. 6 - Typical Transconductance Vs. Drain Current

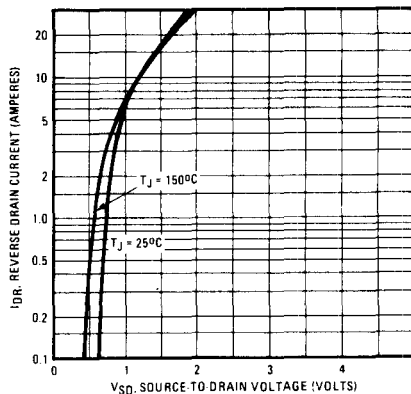


Fig. 7 - Typical Source-Drain Diode Forward Voltage

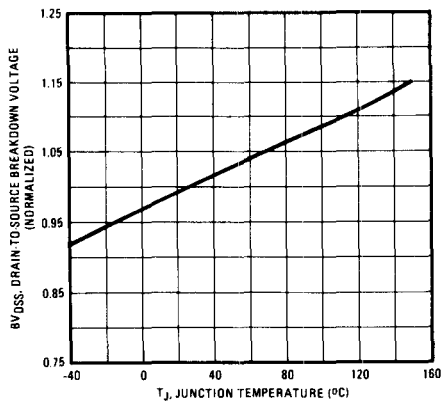


Fig. 8 - Breakdown Voltage Vs. Temperature

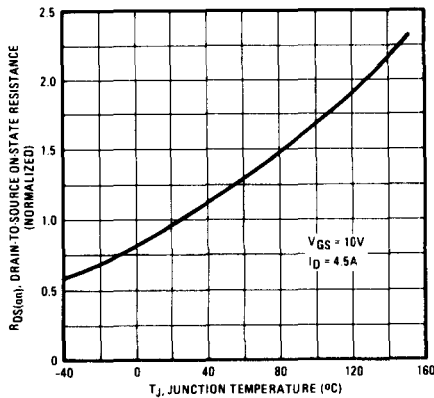


Fig. 9 - Normalized On-Resistance Vs. Temperature

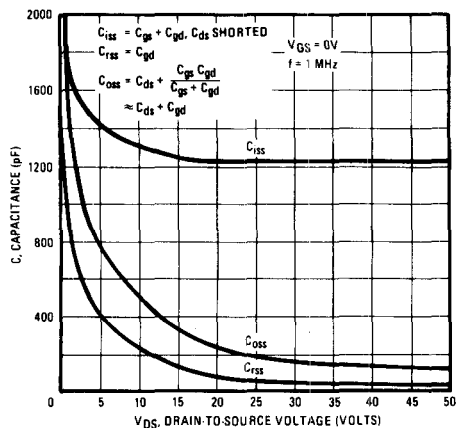


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

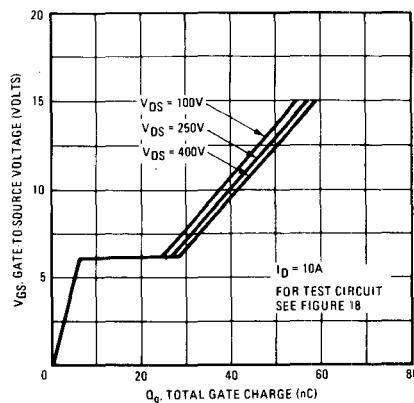


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

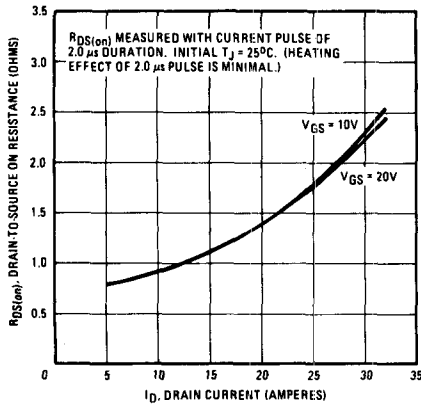


Fig. 12 – Typical On-Resistance Vs. Drain Current

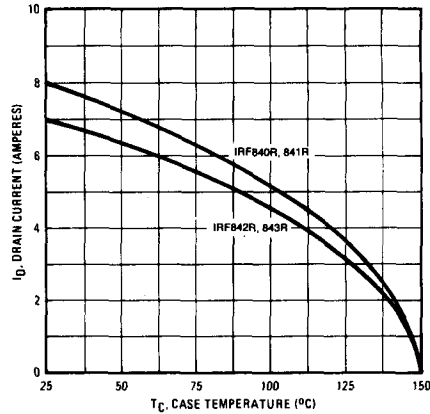


Fig. 13 – Maximum Drain Current Vs. Case Temperature

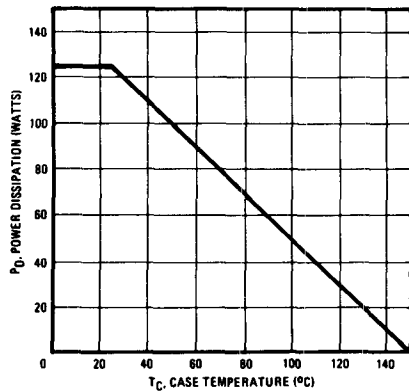


Fig. 14 – Power Vs. Temperature Derating Curve

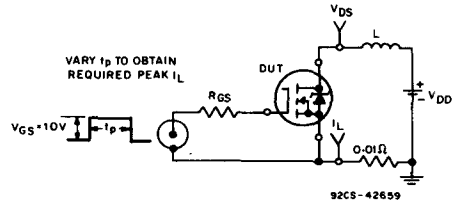


Fig. 15 – Unclamped Energy Test Circuit

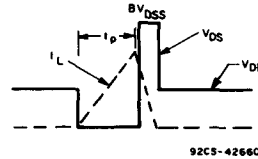


Fig. 16 – Unclamped Energy Waveforms

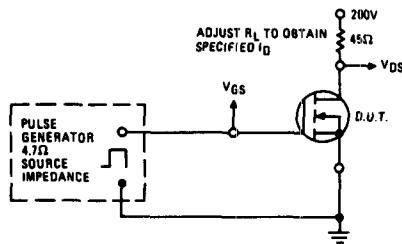


Fig. 17 – Switching Time Test Circuit

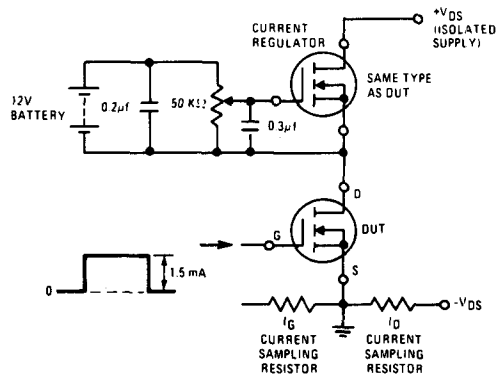


Fig. 18 – Gate Charge Test Circuit