HiRel SX-A Family FPGAs

Leading Edge Performance

- 215 MHz System Performance (Military Temperature)
- 5.3 ns Clock-to-Out (Pin-to-Pin) (Military Temperature)
- 284 MHz Internal Performance (Military Temperature)

Specifications

- 12,000 to 108,000 Available System Gates
- Up to 225 User-Programmable I/O Pins
- Up to 2,012 Dedicated Flip-Flops
- 0.25µ CMOS Process Technology

Features

- I/Os with Live or "Hot-Swapping" Capability
- Power Up/Down Friendly (No Sequencing Required for Supply Voltages)
- Offered as Commercial or Military Temperature Tested and Class B
- Cost Effective QML MIL-Temp Plastic Packaging Options
- Standard Hermetic Package Offerings
- QML Certified Devices
- 100% Military Temperature Tested (–55°C to +125°C)
- 66 MHz PCI Compliant
- CPLD and FPGA Integration
- Single-Chip Solution
- Configurable I/O Support for 3.3V/5.0V PCI, LVTTL, and TTL
- Configurable Weak Resistor Pull-up or Pull-down for Tristated Outputs at Power Up
- 100% Resource Utilization with 100% Pin Locking
- 2.5V, 3.3V, and 5.0V Mixed-Voltage Operation with 5.0V Input Tolerance and 5.0V Drive Strength
- Very Low Power Consumption
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Secure Programming Technology Prevents Reverse Engineering and Design Theft

Product Profile

Device	A54SX32A	A54SX72A
Capacity Typical Gates System Gates	 32,000 48,000	 72,000 108,00
Logic Modules	2,880	6,036
Combinatorial Cells	1,800	4,024
Register Cells (Dedicated Flip-Flops)	1,080	2,012
Maximum User I/Os	225	206
Global Clocks	3	3
Quadrant Clocks	0	4
Boundary Scan Testing	Yes	Yes
3.3V/5.0V PCI	Yes	Yes
Clock-to-Out	5.4 ns	6.7 ns
Input Setup (External)	0 ns	0 ns
Speed Grades	Std, –1	Std, –1
Package (by pin count) CQFP	 208, 256	 208, 256

General Description

Actel's SX-A family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX-A devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

Actel's SX-A architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX-A devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX-A devices gives fast and predictable performance, allows 100 percent pin locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX-A's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX-A devices have easy-to-use I/O cells that do not require HDL instantiation, facilitating design re-use and reducing design and verification time.

QML Certification

Actel has achieved full QML certification, demonstrating that quality management, procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military, and space applications.

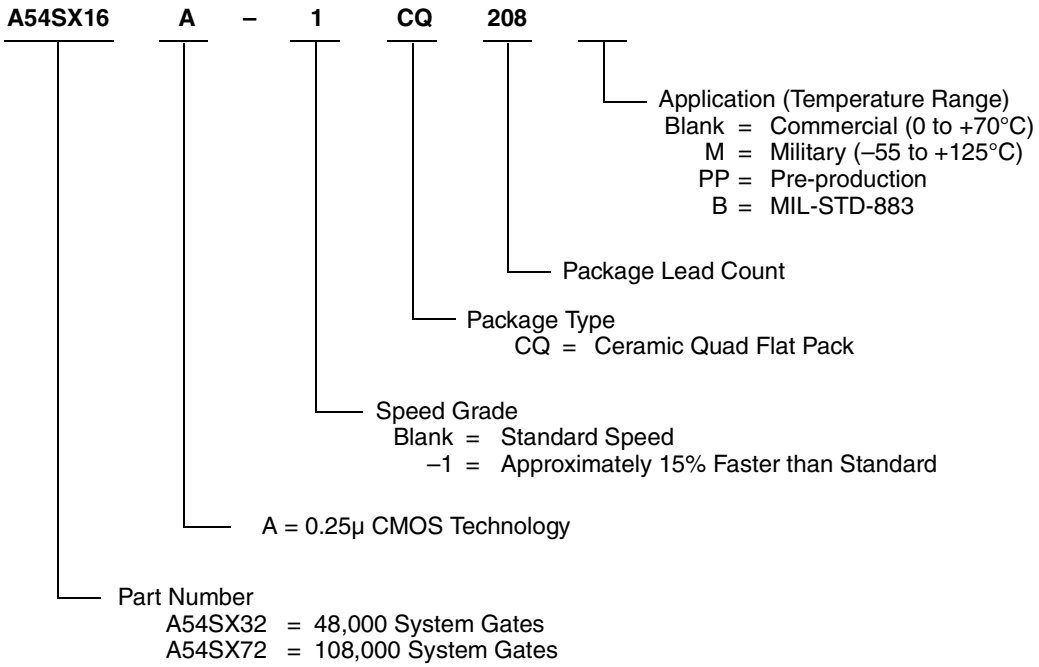
Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for a quality, reliable and cost-effective logistics support throughout QML products' life cycles.

Development Tool Support

The SX-A devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Advantage tools. The Actel DeskTOP series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place-and-route tools. Designer Advantage, Actel's suite of FPGA development point tools for PCs and Workstations, includes the ACTgen Macro Builder, Designer with DirectTime timing-driven place-and-route and analysis tools, and device programming software.

In addition, the SX-A devices contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100-percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to only a few seconds.

Ordering Information



Product Plan

	Speed Grade*		Application		
	Std	–1	C	M •	B
A54SX32A Device					
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P
A54SX72A Device					
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P	P

Contact your Actel sales representative for product availability.

Applications: C = Commercial M = Military B = MIL-STD-883

Availability: P = Planned

**Speed Grade: –1 = Approx. 15% faster than Standard*

• Only Std and –1 Speed Grades

Ceramic Device Resources

Device	User I/Os (including clock buffers)	
	CQFP 208-Pin	CQFP 256-Pin
A54SX32A	174	228
A54SX72A	171	213

Contact your Actel sales representative for product availability.

Package Definitions

CQFP = Ceramic Quad Flat Pack

Actel MIL-STD-883 Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.	Internal Visual	2010, Test Condition B	100%
2.	Temperature Cycling	1010, Test Condition C	100%
3.	Constant Acceleration	2001, Test Condition D or E, Y_1, Orientation Only	100%
4.	Seal a. Fine b. Gross	1014	 100% 100%
5.	Visual Inspection	2009	100%
6.	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
7.	Burn-in Test	1015, Condition D, 160 hours @ 125°C or 80 hours @ 150°C	100%
8.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
9.	Percent Defective Allowable	5%	All Lots
10.	Final Electrical Test	In accordance with applicable Actel device specification, which includes a, b, and c:	
	a. Static Tests (1) 25°C (Subgroup 1, Table I) (2) –55°C and +125°C (Subgroups 2, 3, Table I)	 5005 5005	100%
	b. Functional Tests (1) 25°C (Subgroup 7, Table I) (2) –55°C and +125°C (Subgroups 8A and 8B, Table I)	 5005 5005	100%
	c. Switching Tests at 25°C (Subgroup 9, Table I)	 5005	100%
11.	External Visual	2009	100%

Note: *When Destructive Physical Analysis (DPA) is performed on Class B devices, the step coverage requirement as specified in Method 2018 must be waived.*

SX-A Family Architecture

The SX-A family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

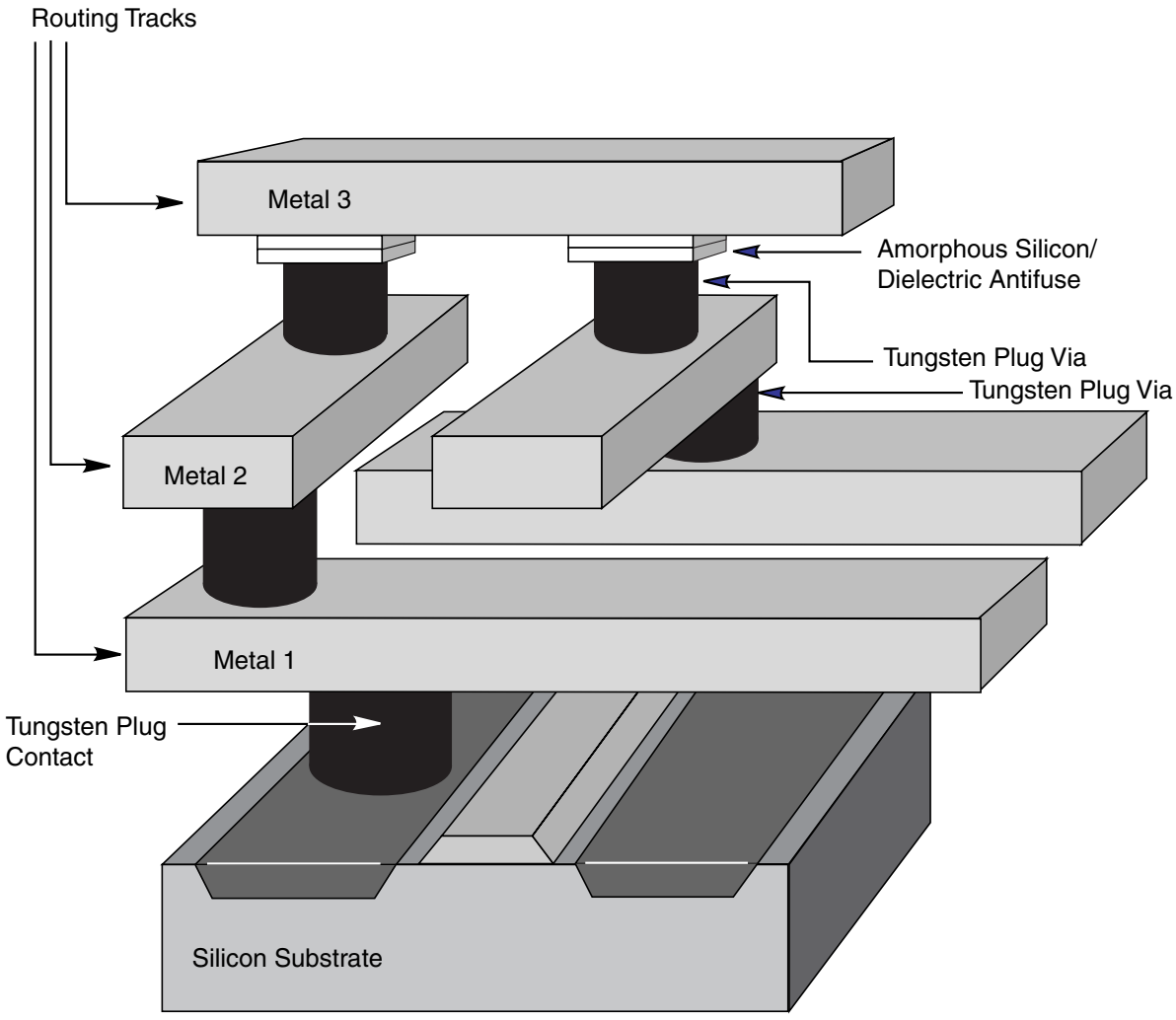
Programmable Interconnect Element

The SX-A family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX-A family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.



Note: *A54SX72A has 4 layers of metal with the antifuse between Metal 3 and Metal 4.*

Figure 1 • *SX-A Family Interconnect Elements*

Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Actel's SX-A family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 2). The R-cell registers feature programmable clock polarity selectable on a register by register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to 5 inputs (Figure 3 on page 7). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX-A architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Chip Architecture

The SX-A family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into SuperClusters (Figure 4 on page 7). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 5 and Figure 6 on page 8). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

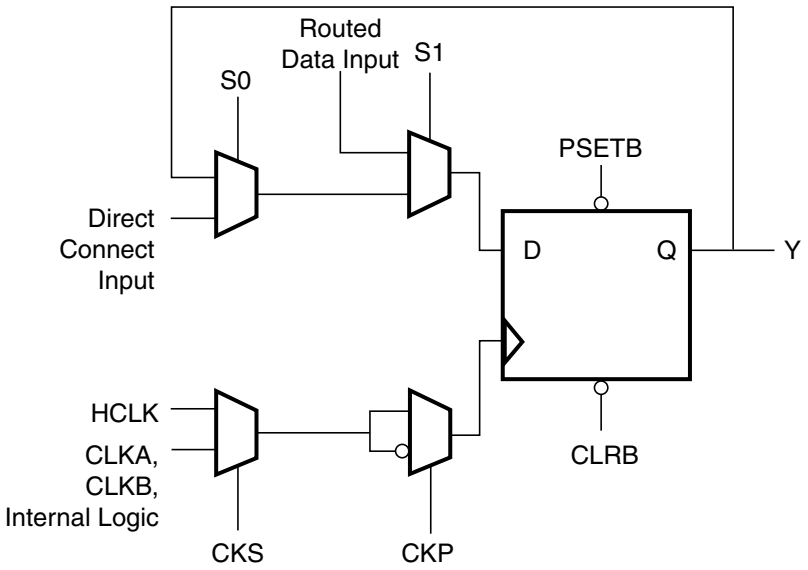


Figure 2 • R-Cell

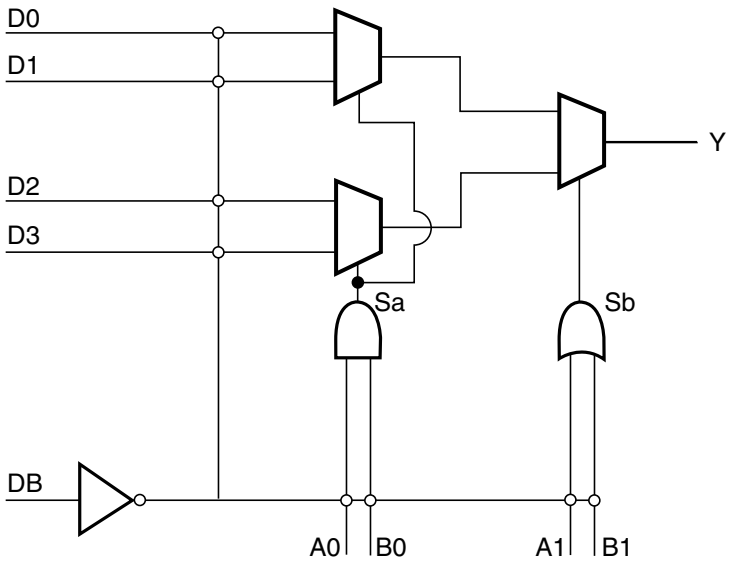


Figure 3 • *C-Cell*

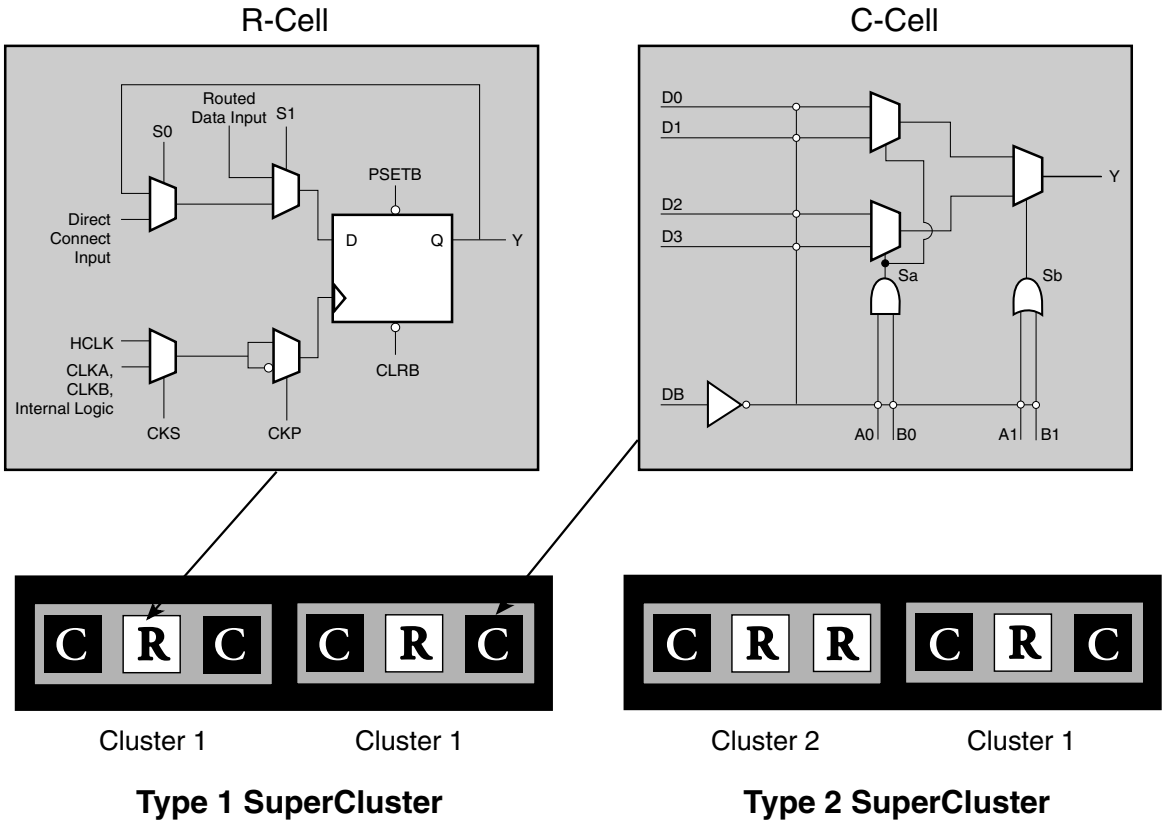
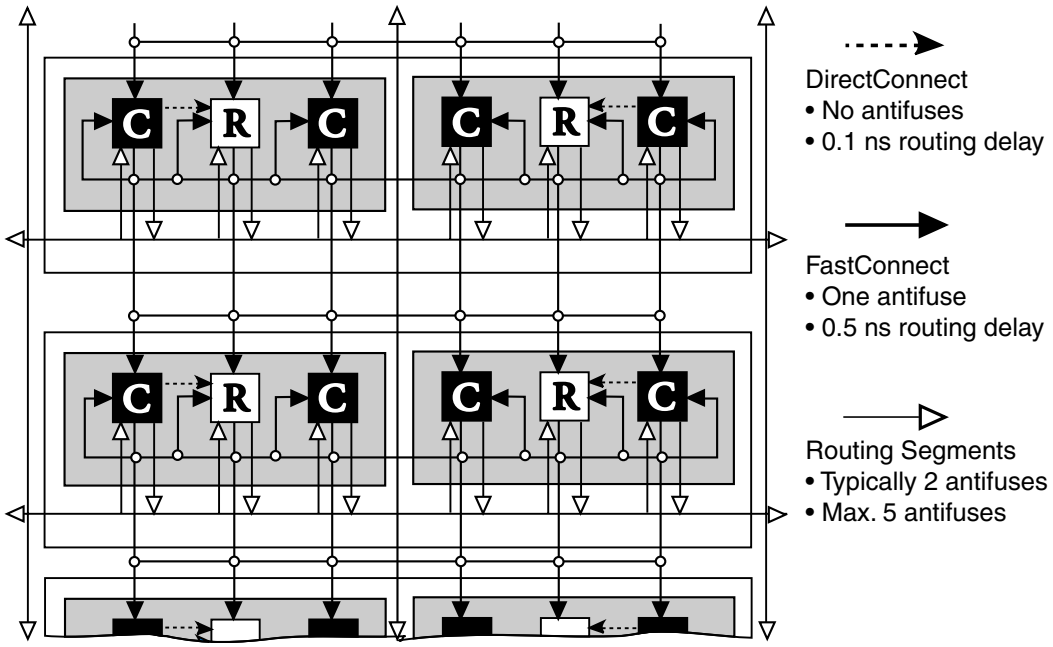
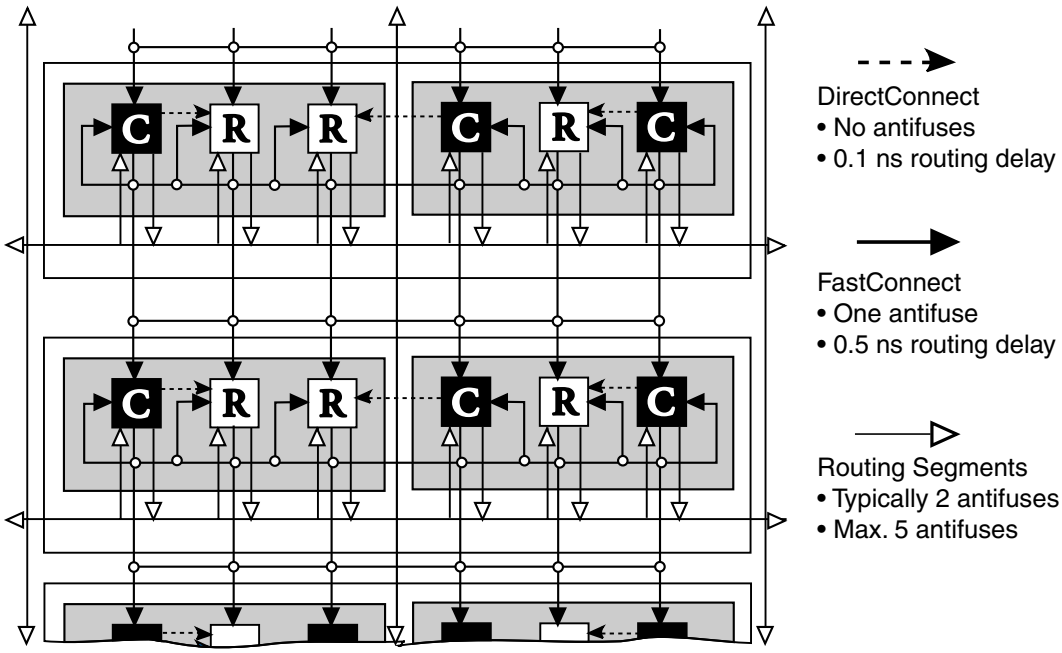


Figure 4 • *Cluster Organization*



Type 1 SuperClusters

Figure 5 • *DirectConnect and FastConnect for Type 1 SuperClusters*



Type 2 SuperClusters

Figure 6 • *DirectConnect and FastConnect for Type 2 SuperClusters*

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.2 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. This provides a fast propagation path for the clock signal, enabling the 5.3 ns clock-to-out (pin-to-pin) performance of the SX-A devices. The hardwired clock is tuned to provide clock skew as low as 0.29 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants.

Other Architectural Features

Technology

Actel's SX-A family is implemented on a high-voltage twin-well CMOS process using 0.25µ design rules (moving quickly to 0.22µ). The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 ohms with capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX-A devices to operate with internal clock frequencies exceeding 284 MHz, enabling very fast execution of even complex logic functions. Thus, the SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX-A device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX-A devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 5.3 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

Hot Swapping

SX-A I/Os are specifically designed to be programmed to be hot swappable. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power up/down and they do not require a specific power up or power down sequence in order to avoid damage to the SX-A devices. After the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The devices' output pins are driven to a high impedance state until normal chip operating conditions are reached.

Power Requirements

The SX-A family supports 2.5V/3.3V/5.0V mixed voltage operation and is designed to tolerate 5.0V inputs in each case (Table 1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power architecture FPGA available today.

Table 1 • *Supply Voltages*

	V_{CCA}	V_{CCI}	Maximum Input Tolerance	Maximum Output Drive
A54SX32A A54SX72A	2.5V	2.5V	5.0V	2.5V
	2.5V	3.3V	5.0V	3.3V
	2.5V	5.0V	5.0V	5.0V

Boundary Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant. SX-A devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 2.

Table 2 • *Boundary Scan Pin Functionality*

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10k¾ on TMS

In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10k¾. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

SX-A Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification. The TRST pin is equipped with an internal pull-up resistor. To remove the boundary scan state machine from the reset state during probing, it is recommended that TRST be left floating.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

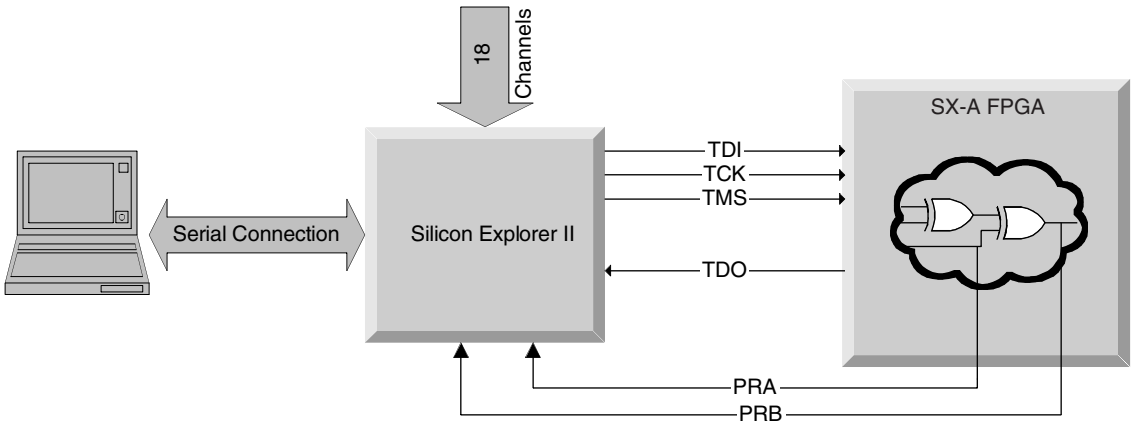


Figure 7 • *Probe Setup*

2.5V/3.3V/5.0V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage[2]	–0.5 to +V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*
2. *The I/O source sink numbers refer to tristated inputs and outputs.*

Recommended Operating Conditions

Parameter	Military	Units
Temperature Range[1]	–55 to +125	°C
3.3V Power Supply Tolerance	±10	%V_{CC}
5.0V Power Supply Tolerance	±10	%V_{CC}
2.5V Power Supply Tolerance	±8	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
V_{OH}	(I_{OH} = -20uA) (CMOS) (I_{OH} = -8mA) (TTL) (I_{OH} = -6mA) (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	(I_{OL}= 20uA) (CMOS) (I_{OL} = 12mA) (TTL) (I_{OL} = 8mA) (TTL)		0.10 0.50		 0.50	V
V_{IL}	Low Level Inputs		0.8		0.8	V
V_{IH}	High Level Inputs	2.0		2.0		V
I_{IL}	Input Leakage Current, V_{IN} = V_{CCI} or GND	–10	10	–10	10	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND	–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F		10		10	ns
C_{IO}	I/O Capacitance		10		10	pF
I_{CC}	Standby Current		10		20	mA

PCI Compliance for the SX-A Family

The SX-A family supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (5.0V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V_{IH}	Input High Voltage[1]		2.0	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage[1]		–0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter includes, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

AC Specifications (5.0V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$ [1]	–44		mA
		$1.4 \le V_{OUT} < 2.4$ [1, 2]	$(-44 + (V_{OUT} - 1.4)/0.024)$		mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]		Equation A on page 14	
	(Test Point)	$V_{OUT} = 3.1$ [3]		–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \ge 2.2$ [1]	95		mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$		mA
		$0.71 > V_{OUT} > 0$ [1, 3]		Equation B on page 14	
	(Test Point)	$V_{OUT} = 0.71$ [3]		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4V to 2.4V load [4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4V to 0.4V load [4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 8 on page 14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 8 on page 14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*

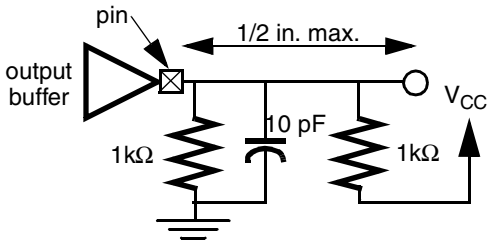


Figure 8 shows the 5.0V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

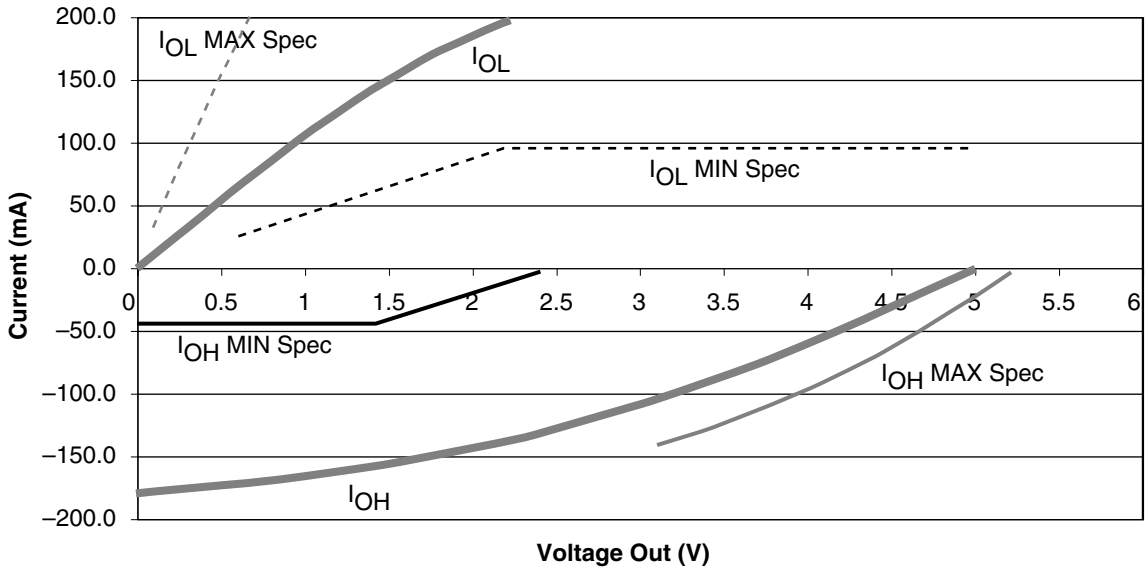


Figure 8 • *5.0V PCI Curve for SX-A Family*

Equation A

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$
$$\text{for } V_{CCI} > V_{OUT} > 3.1V$$

Equation B

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.71V$$

DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CCI}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$		±10	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{CCI}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

AC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$ [1]	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ [1]	$(-17.1 + (V_{CCI} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2]		Equation C on page 17	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ [1]	$16V_{CCI}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$ [1, 2]		Equation D on page 17	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load [3]	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load [3]	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 9 on page 17. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD, which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 9 on page 17. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

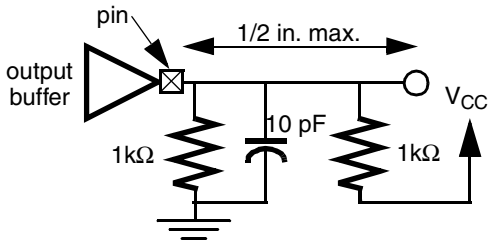


Figure 9 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

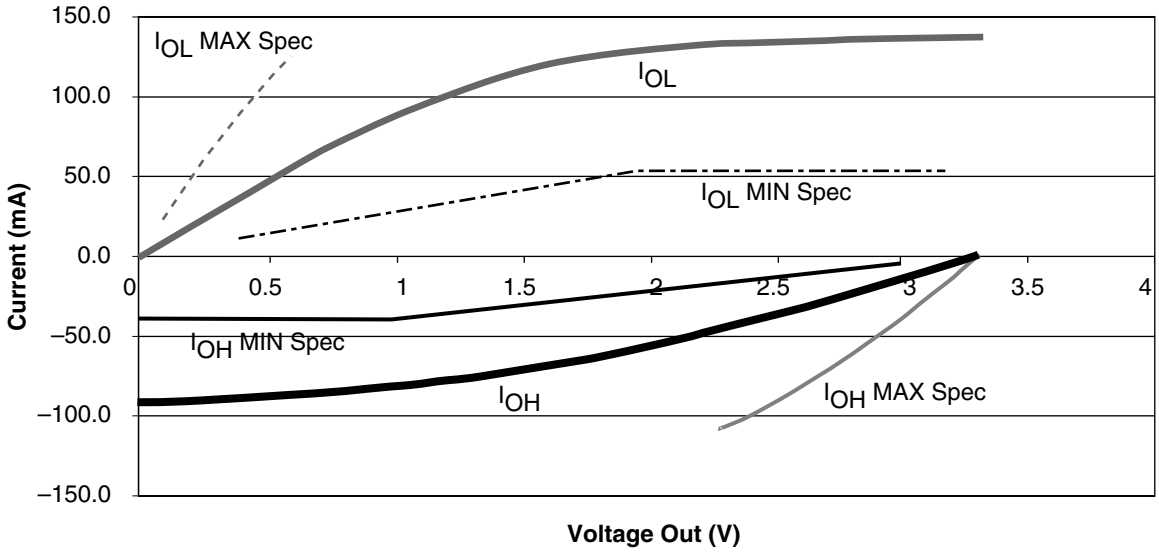


Figure 9 • *3.3V PCI Curve for SX-A Family*

Equation C

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$
$$\text{for } V_{CCI} > V_{OUT} > 0.7\ V_{CCI}$$

Equation D

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.18\ V_{CCI}$$

Junction Temperature (T_J)

The temperature variable in the Designer Series software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Equation 4, shown below, can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (4)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} * P$

P = Power calculated from Estimating Power Consumption section

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the Package Thermal Characteristics section below.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

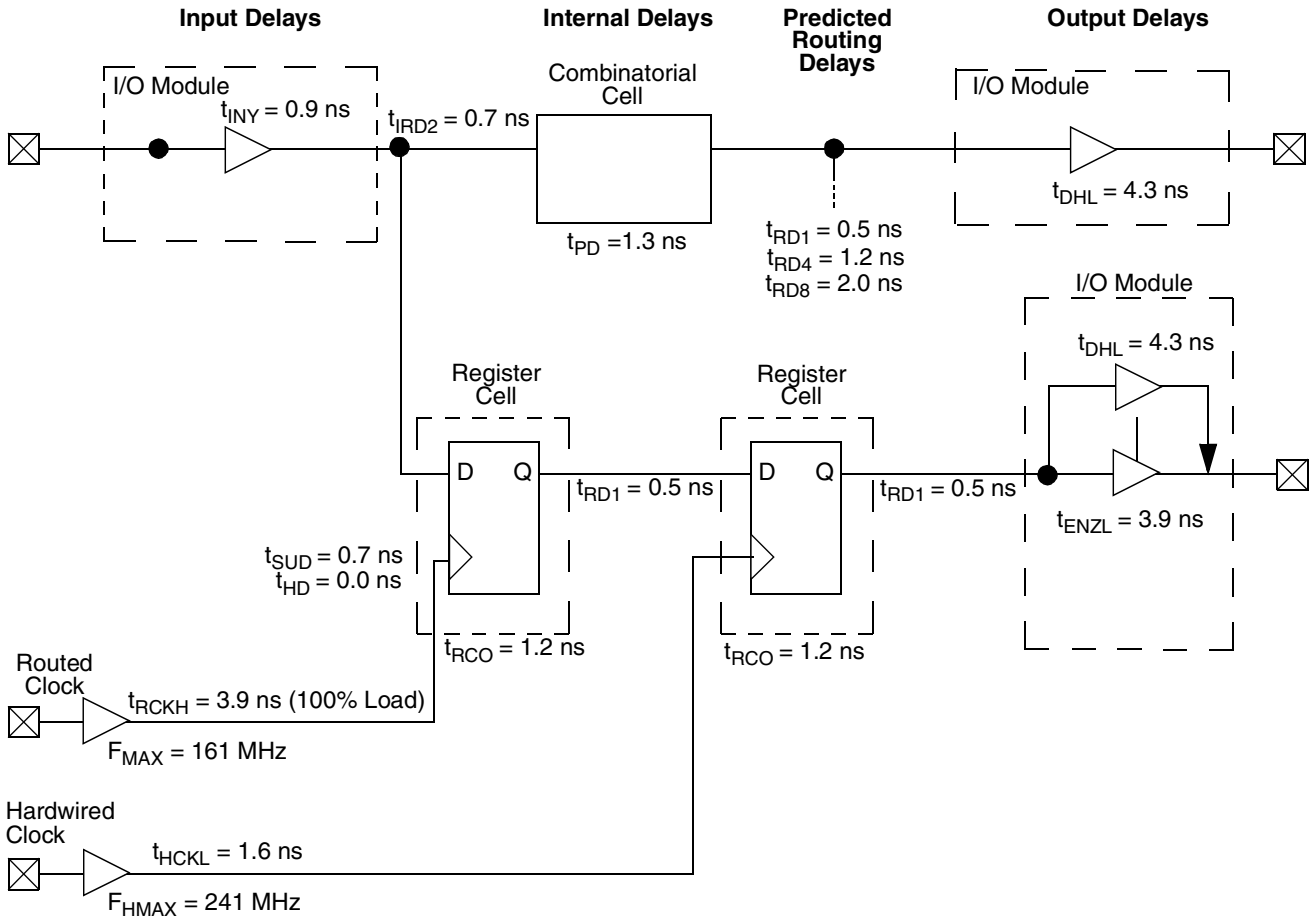
The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CQFP 256-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{20\text{°C/W}} = 4.0\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Ceramic Quad Flatpack (CQFP)	208	6.3	22	14	°C/W
Ceramic Quad Flatpack (CQFP)	256	6.2	20	10	°C/W

SX-A Timing Model*



**Values shown for A54SX32A–1, worst-case military conditions.*

Hardwired Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKL}$
= 0.9 + 0.5 + 0.7 – 1.6 = 0.5 ns

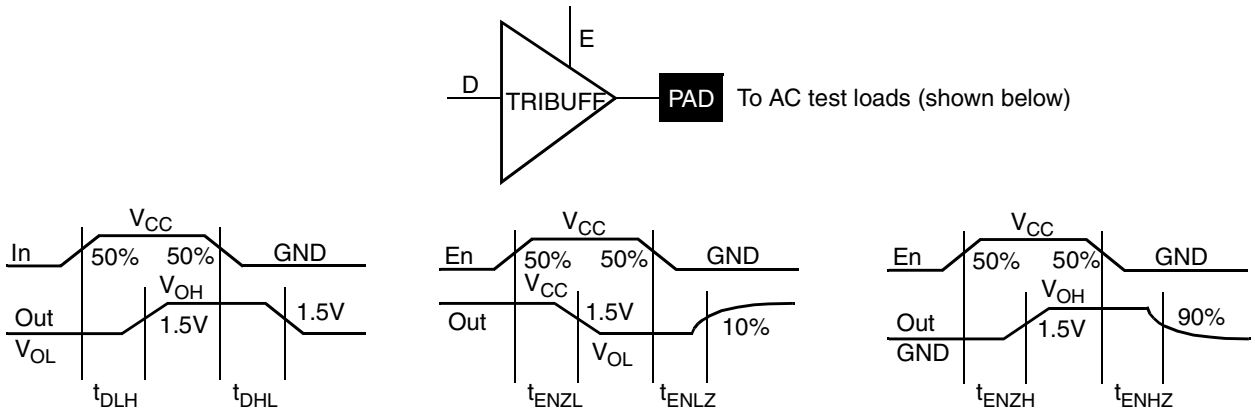
Clock-to-Out (Pin-to-Pin)
= $t_{HCKL} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.6 + 1.2 + 0.5 + 4.3 = 7.6 ns

Routed Clock

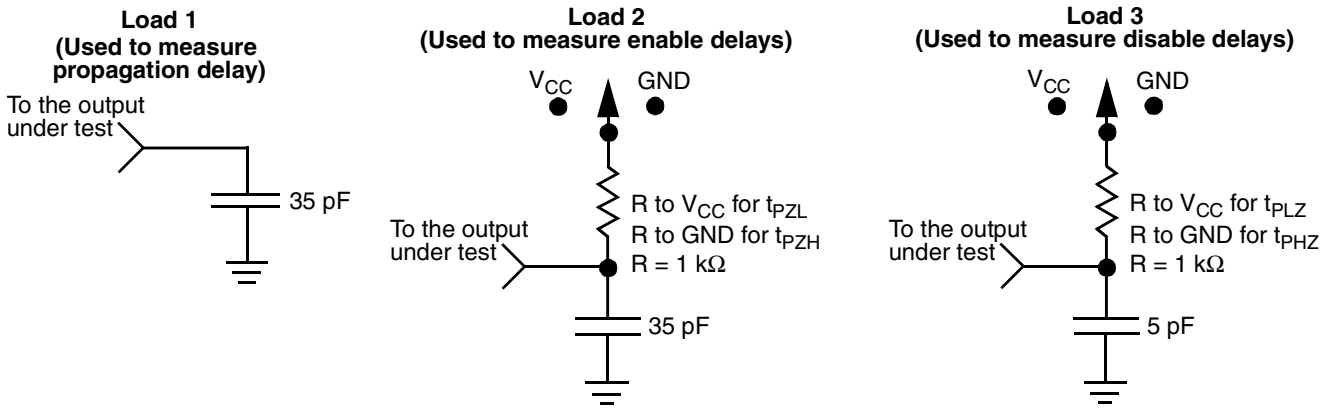
External Setup = $t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$
= 0.9 + 0.5 + 0.7 – 3.9 = -1.8 ns

Clock-to-Out (Pin-to-Pin)
= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 3.9 + 1.2 + 0.5 + 4.3 = 9.9 ns

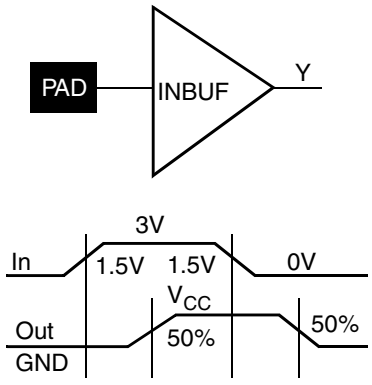
Output Buffer Delays



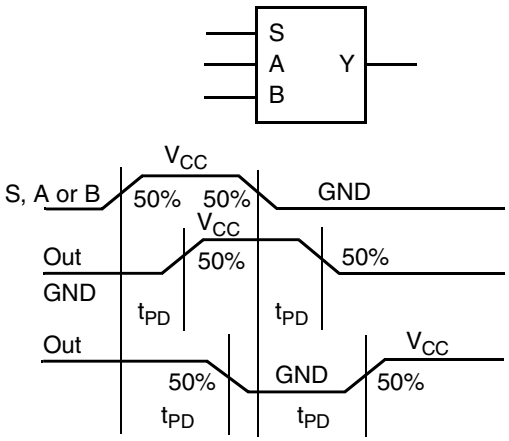
AC Test Loads



Input Buffer Delays

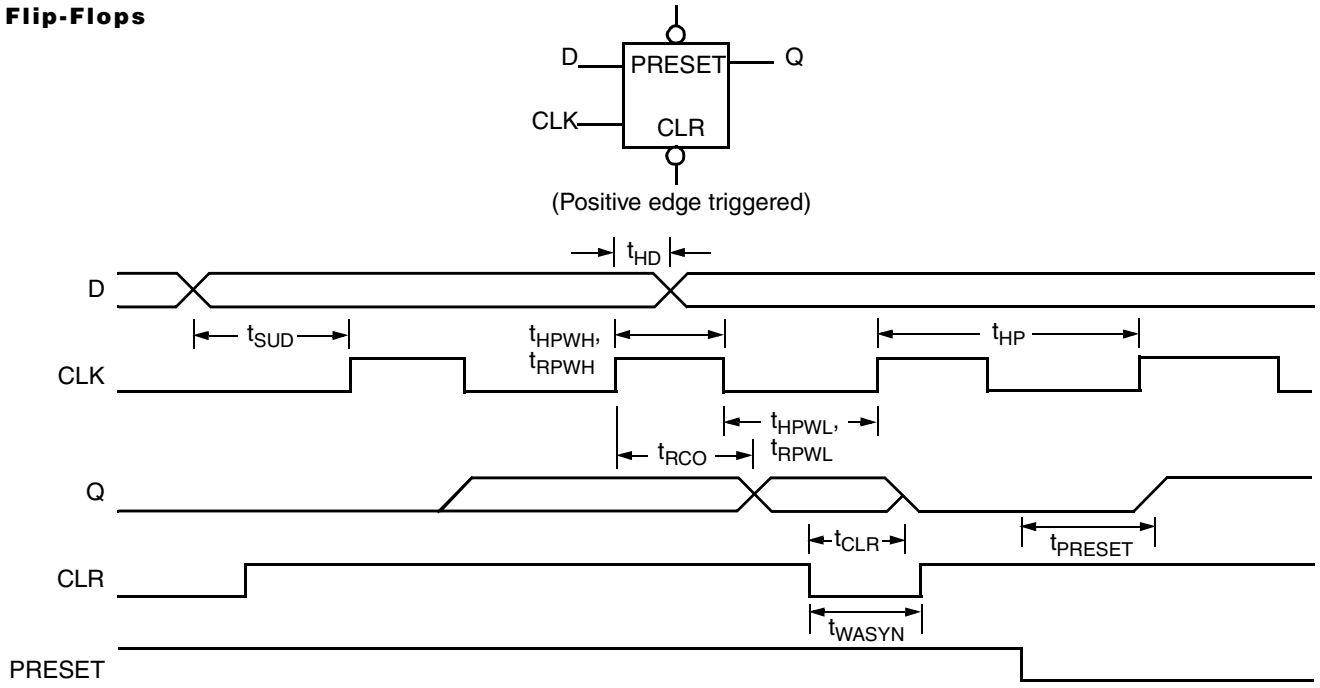


C-Cell Delays



Cell Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with postlayout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to six percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to six percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO=24) routing delays in the Timing Characteristics tables starting on page 22.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

(Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.3V)

V_{CCA}	Junction Temperature (T_J)						
	–55	–40	0	25	70	85	125
2.3	0.75	.079	0.88	0.89	1.00	1.04	1.16
2.5	0.70	0.74	0.82	0.83	0.93	0.97	1.08
2.7	0.66	0.69	0.79	0.79	0.88	0.92	1.02

A54SX32A Timing Characteristics

(Worst-Case Military Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.3		1.4	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.2		0.2	ns
t_{RD1}	FO=1 Routing Delay		0.5		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.7		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.9		1.0	ns
t_{RD4}	FO=4 Routing Delay		1.2		1.3	ns
t_{RD8}	FO=8 Routing Delay		2.0		2.4	ns
t_{RD12}	FO=12 Routing Delay		2.9		3.5	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9		1.0	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0		1.3	ns
t_{SUD}	Flip-Flop Data Input Setup	0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.6		1.9		ns
$t_{RECASYN}$	Asynchronous Recovery		0.4		0.5	ns
t_{HASYN}	Asynchronous Hold Time		0.4		0.5	ns
Input Module Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH		0.9		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.4		1.6	ns
Input Module Predicted Routing Delays[2]						
t_{IRD1}	FO=1 Routing Delay		0.5		0.6	ns
t_{IRD2}	FO=2 Routing Delay		0.7		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.9		1.0	ns
t_{IRD4}	FO=4 Routing Delay		1.2		1.3	ns
t_{IRD8}	FO=8 Routing Delay		2.0		2.4	ns
t_{IRD12}	FO=12 Routing Delay		2.9		3.5	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX32A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hardwired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.9		2.2	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.6		2.0	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.4		ns
t_{HCKSW}	Maximum Skew		0.2		0.2	ns
t_{HP}	Minimum Period	4.2		4.9		ns
f_{HMAX}	Maximum Frequency		241		206	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.8		3.3	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.0		3.5	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.1		3.6	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.2		3.8	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.9		4.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		3.9		4.6	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.3		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		2.2		2.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		2.0		2.3	ns

A54SX32A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.7		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.6		4.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.0		2.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.8		4.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.4		5.1	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF
3.3V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		4.9		5.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.3		5.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		4.9		5.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.2		4.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		5.0		5.8	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF

Note:

1. *Delays based on 10 pF loading.*
2. *Delays based on 35 pF loading.*

A54SX32A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5.0V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		4.7		5.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.2		6.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.0		2.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.1		4.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		5.1		6.0	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF
5.0V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.8		4.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.8		5.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.5		4.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		5.1		6.0	ns
t_{ENHZ}	Enable-to-Pad, H to Z		6.4		7.3	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF

Note:

1. *Delays based on 50 pF loading.*
2. *Delays based on 35 pF loading.*

A54SX72A Timing Characteristics

(Worst-Case Military Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.3		1.5	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.2		0.2	ns
t_{RD1}	FO=1 Routing Delay		0.5		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.7		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.9		1.0	ns
t_{RD4}	FO=4 Routing Delay		1.2		1.3	ns
t_{RD8}	FO=8 Routing Delay		2.0		2.4	ns
t_{RD12}	FO=12 Routing Delay		2.9		3.5	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.1		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9		1.0	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0		1.3	ns
t_{SUD}	Flip-Flop Data Input Setup	0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.6		1.9		ns
$t_{RECASYN}$	Asynchronous Recovery		0.4		0.5	ns
t_{HASYN}	Asynchronous Hold Time		0.4		0.5	ns
Input Module Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH		0.9		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.4		1.6	ns
Input Module Predicted Routing Delays[2]						
t_{IRD1}	FO=1 Routing Delay		0.5		0.6	ns
t_{IRD2}	FO=2 Routing Delay		0.7		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.9		1.0	ns
t_{IRD4}	FO=4 Routing Delay		1.2		1.3	ns
t_{IRD8}	FO=8 Routing Delay		2.0		2.4	ns
t_{IRD12}	FO=12 Routing Delay		2.9		3.5	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX72A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

Dedicated (Hardwired) Array Clock Network		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		2.4		2.9	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.1		2.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.4		ns
t_{HCKSW}	Maximum Skew		0.5		0.6	ns
t_{HP}	Minimum Period	4.2		4.9		ns
f_{HMAX}	Maximum Frequency		241		206	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		4.2		4.9	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		4.4		5.2	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		5.1		6.0	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		5.2		6.2	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		7.0		8.1	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		7.0		8.2	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.3		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		2.0		2.3	ns
Quadrant Clock Networks						
t_{QCKH}	Input LOW to HIGH (Light Load)		2.3		2.7	ns
t_{QCKL}	Input HIGH to LOW (Light Load)		2.6		3.1	ns
t_{QCKH}	Input LOW to HIGH (50% Load)		2.4		2.8	ns
t_{QCKL}	Input HIGH to LOW (50% Load)		2.7		3.2	ns
t_{QCKH}	Input LOW to HIGH (100% Load)		2.6		3.0	ns
t_{QCKL}	Input HIGH to LOW (100% Load)		2.9		3.4	ns
t_{QCKSW}	Maximum Skew (Light Load)		0.3		0.4	ns
t_{QCKSW}	Maximum Skew (50% Load)		0.4		0.5	ns
t_{QCKSW}	Maximum Skew (100% Load)		0.5		0.6	ns

A54SX72A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.7		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.6		4.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.0		2.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.4		2.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.8		4.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.4		5.1	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF
3.3V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		4.9		5.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.3		5.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		4.9		5.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.2		4.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		5.0		5.8	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF

Notes:

1. *Delays based on 10 pF loading.*
2. *Delays based on 35 pf loading.*

A54SX72A Timing Characteristics (Continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5.0 V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		4.3		5.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.2		6.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.0		2.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.2		2.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.1		4.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		5.1		5.9	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF
5.0V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.8		4.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.8		5.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.5		4.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		5.1		6.0	ns
t_{ENHZ}	Enable-to-Pad, H to Z		6.4		7.3	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.05	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *Delays based on 35 pf loading.*

Pin Description

CLKA/B Clock A and B

These pins are 3.3V/5.0V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

QCLKA/B/C/D Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs. They are 3.3V/5.0V PCI/TTL clock input for clock distribution networks. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (These quadrant clocks are only for A54SX72A).

GND Ground

LOW supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the 3.3V/5.0V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3V PCI, or 5.0V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

PRB, I/O Probe B

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 2 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 2 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 2 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 2 on page 10). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 Specifications.

TRST Boundary Scan (JTAG) Reset Pin

Once configured as the Boundary Scan Reset pin, the TRST pin functions as an active low input to asynchronously initialize or reset the boundary scan circuit. The TRST is equipped with an internal pull-up resistor. This pin functions as an I/O when "Reserve JTAG Reset Pin" is not selected in Designer.

V_{CCI} Supply Voltage

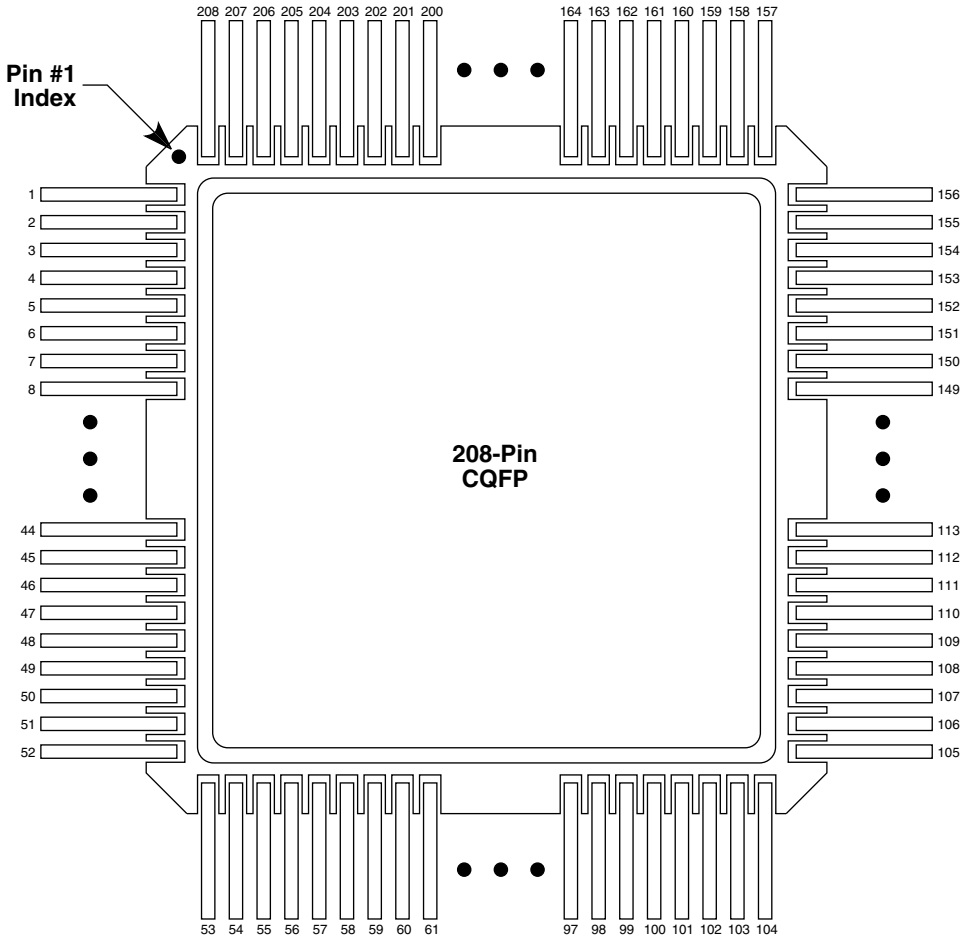
Supply voltage for I/Os. See Table 1 on page 9.

V_{CCA} Supply Voltage

Supply voltage for Array. See Table 1 on page 9.

Package Pin Assignments

208-Pin CQFP (Top View)



208-Pin CQFP

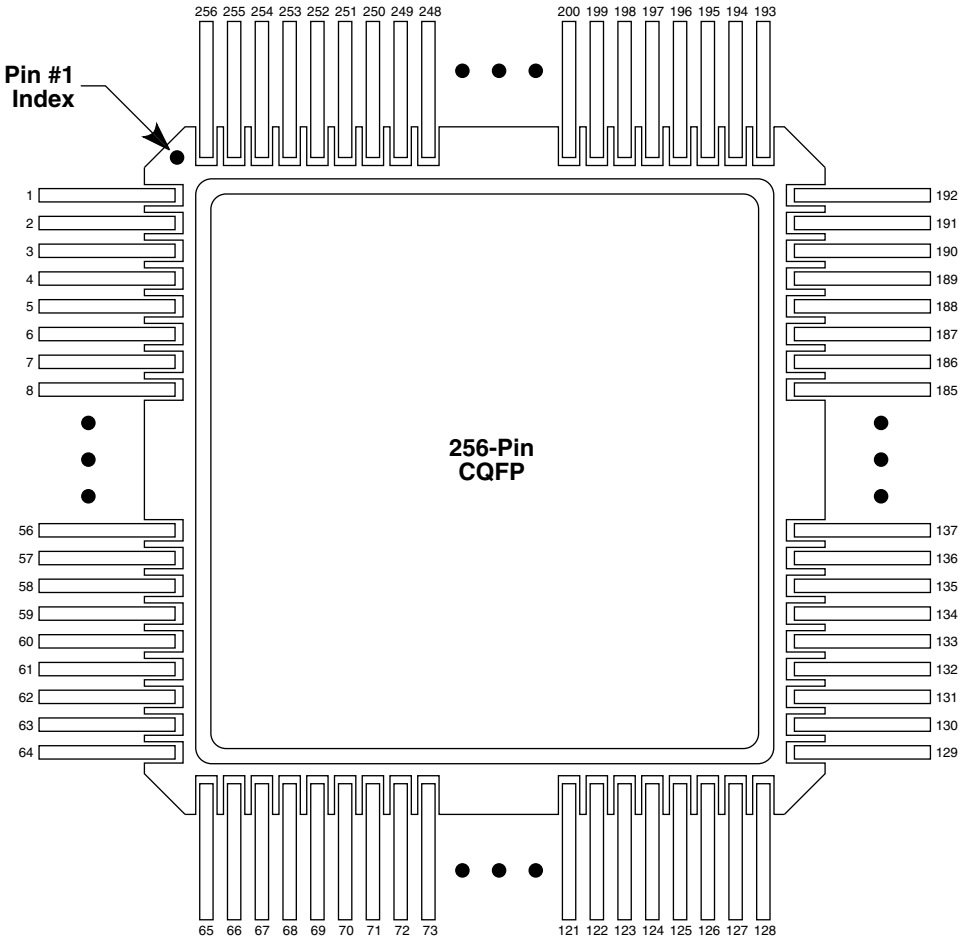
Pin Number	A54SX32A Function	A54SX72A Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	TMS	TMS
12	V_{CCI}	V_{CCI}
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	GND
19	I/O	V_{CCA}
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	NC	I/O
26	GND	GND
27	V_{CCA}	V_{CCA}
28	GND	GND
29	I/O	I/O
30	TRST, I/O	TRST, I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	GND	GND
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	V_{CCI}	V_{CCI}
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	NC	NC
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	QCLKA
75	I/O	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	V_{CCA}	V_{CCA}
79	GND	GND
80	V_{CCR}	NC
81	I/O	I/O
82	HCLK	HCLK
83	I/O	V_{CCI}
84	I/O	QCLKB
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O
89	I/O	I/O
90	I/O	I/O
91	I/O	I/O
92	I/O	I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	V_{CCI}	V_{CCI}
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	TDO, I/O	TDO, I/O
104	I/O	I/O

208-Pin CQFP (Continued)

Pin Number	A54SX32A Function	A54SX72A Function
105	GND	GND
106	I/O	I/O
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O
110	I/O	I/O
111	I/O	I/O
112	I/O	I/O
113	I/O	I/O
114	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}
116	I/O	GND
117	I/O	V_{CCA}
118	I/O	I/O
119	I/O	I/O
120	I/O	I/O
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	I/O	I/O
125	I/O	I/O
126	I/O	I/O
127	I/O	I/O
128	I/O	I/O
129	GND	GND
130	V_{CCA}	V_{CCA}
131	GND	GND
132	V_{CCR}	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	I/O	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	V_{CCA}	V_{CCA}
146	GND	GND
147	I/O	I/O
148	V_{CCI}	V_{CCI}
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	I/O
156	I/O	I/O
157	GND	GND
158	I/O	I/O
159	I/O	I/O
160	I/O	I/O
161	I/O	I/O
162	I/O	I/O
163	I/O	I/O
164	V_{CCI}	V_{CCI}
165	I/O	I/O
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	I/O	I/O
175	I/O	I/O
176	I/O	I/O
177	I/O	I/O
178	I/O	QCLKD
179	I/O	I/O
180	CLKA	CLKA
181	CLKB	CLKB
182	NC	NC
183	GND	GND
184	V_{CCA}	V_{CCA}
185	GND	GND
186	PRA, I/O	PRA, I/O
187	I/O	V_{CCI}
188	I/O	I/O
189	I/O	I/O
190	I/O	QCLKC
191	I/O	I/O
192	I/O	I/O
193	I/O	I/O
194	I/O	I/O
195	I/O	I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O
200	I/O	I/O
201	V_{CCI}	V_{CCI}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	I/O
207	I/O	I/O
208	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

256-Pin CQFP (Top View)



256-Pin CQFP

Pin Number	A54SX32A Function	A54SX72A Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	TMS	TMS
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	V_{CCI}
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	V_{CCI}	V_{CCI}
29	GND	GND
30	V_{CCA}	V_{CCA}
31	GND	GND
32	I/O	I/O
33	I/O	I/O
34	TRST, I/O	TRST, I/O
35	I/O	I/O
36	I/O	V_{CCA}
37	I/O	GND
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	V_{CCA}	V_{CCA}
47	I/O	V_{CCI}
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	I/O	I/O

Pin Number	A54SX32A Function	A54SX72A Function
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	GND
57	I/O	I/O
58	I/O	I/O
59	GND	GND
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	V_{CCI}
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O
89	I/O	QCLKA
90	PRB, I/O	PRB, I/O
91	GND	GND
92	V_{CCI}	V_{CCI}
93	GND	GND
94	V_{CCA}	V_{CCA}
95	I/O	I/O
96	HCLK	HCLK
97	I/O	I/O
98	I/O	QCLKB
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	I/O	I/O
104	I/O	I/O

256-Pin CQFP (Continued)

Pin Number	A54SX32A Function	A54SX72A Function
105	I/O	I/O
106	I/O	I/O
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O
110	GND	GND
111	I/O	I/O
112	I/O	I/O
113	I/O	I/O
114	I/O	I/O
115	I/O	I/O
116	I/O	I/O
117	I/O	I/O
118	I/O	I/O
119	I/O	I/O
120	I/O	V_{CCI}
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	I/O	I/O
125	I/O	I/O
126	TDO, I/O	TDO, I/O
127	I/O	I/O
128	I/O	I/O
129	GND	GND
130	I/O	I/O
131	I/O	I/O
132	I/O	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	V_{CCA}	V_{CCA}
142	I/O	V_{CCI}
143	I/O	GND
144	I/O	V_{CCA}
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	I/O
156	I/O	I/O

Pin Number	A54SX32A Function	A54SX72A Function
157	I/O	I/O
158	GND	GND
159	NC	NC
160	GND	GND
161	V_{CCI}	V_{CCI}
162	I/O	V_{CCA}
163	I/O	I/O
164	I/O	I/O
165	I/O	I/O
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CCA}	V_{CCA}
175	GND	GND
176	GND	GND
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	I/O
181	I/O	I/O
182	I/O	I/O
183	I/O	V_{CCI}
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	I/O	I/O
189	GND	GND
190	I/O	I/O
191	I/O	I/O
192	I/O	I/O
193	I/O	I/O
194	I/O	I/O
195	I/O	I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O
200	I/O	I/O
201	I/O	I/O
202	I/O	V_{CCI}
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	I/O
207	I/O	I/O
208	I/O	I/O

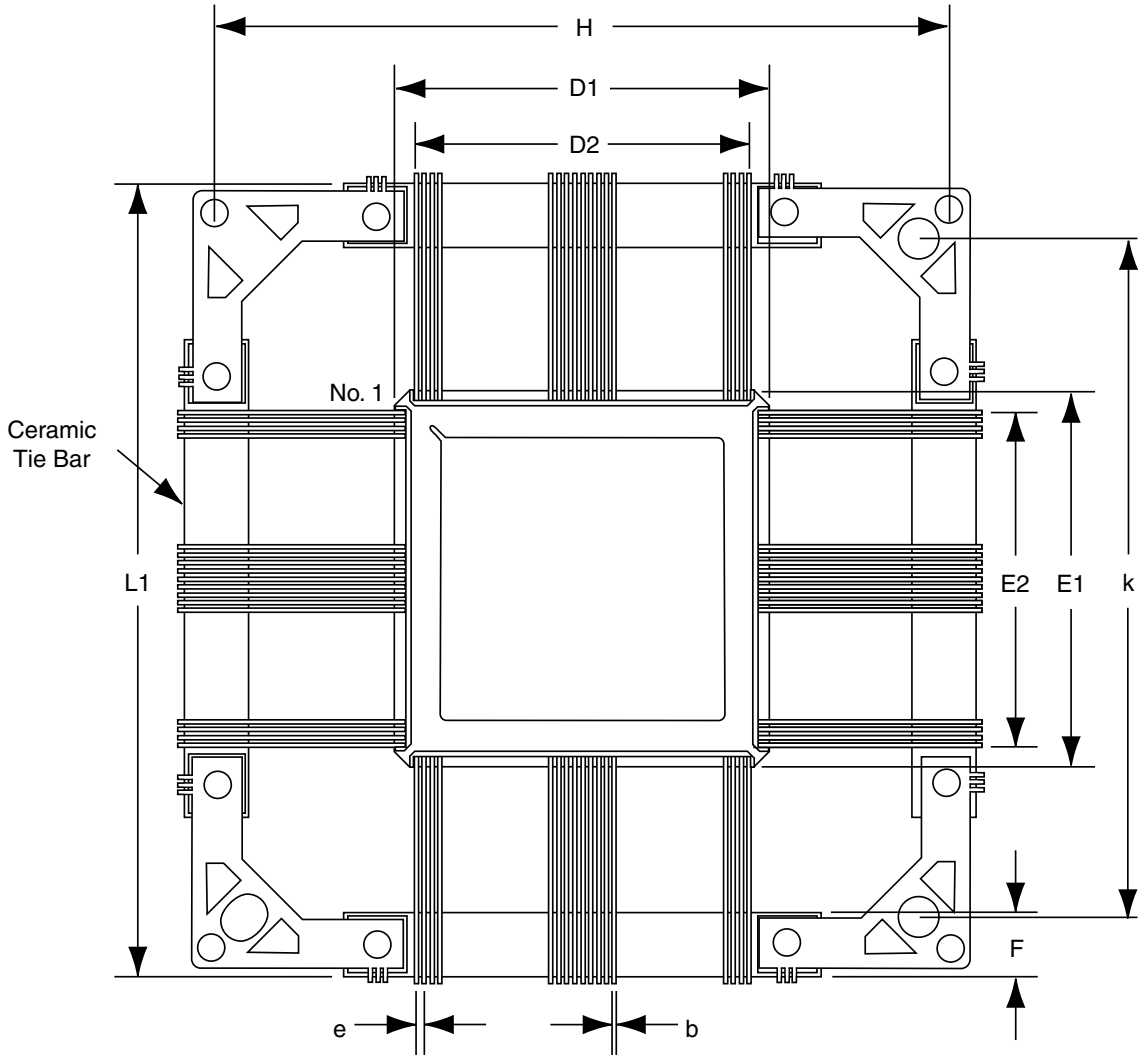
256-Pin CQFP (Continued)

Pin Number	A54SX32A Function	A54SX72A Function
209	I/O	I/O
210	I/O	I/O
211	I/O	I/O
212	I/O	I/O
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O
216	I/O	I/O
217	I/O	I/O
218	I/O	QCLKD
219	CLKA	CLKA
220	CLKB	CLKB
221	V_{CCI}	V_{CCI}
222	GND	GND
223	V_{CCR}	NC
224	GND	GND
225	PRA, I/O	PRA, I/O
226	I/O	I/O
227	I/O	I/O
228	I/O	V_{CCA}
229	I/O	I/O
230	I/O	I/O
231	I/O	QCLKC
232	I/O	I/O
233	I/O	I/O
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	GND
241	I/O	I/O
242	I/O	I/O
243	I/O	I/O
244	I/O	I/O
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	I/O
249	I/O	V_{CCI}
250	I/O	I/O
251	I/O	I/O
252	I/O	I/O
253	I/O	I/O
254	I/O	I/O
255	I/O	I/O
256	TCK, I/O	TCK, I/O

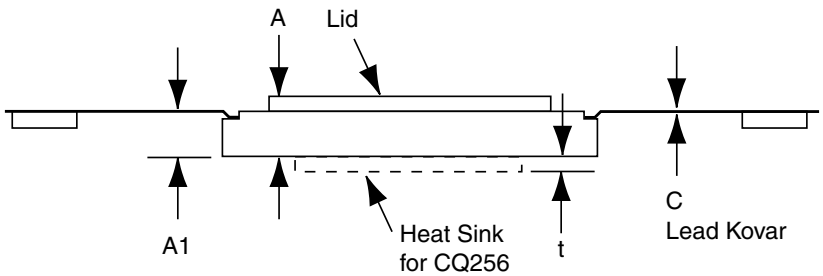
Package Mechanical Drawings

208-Pin and 256-Pin CQFP (Cavity Up)

Top View



Side View



Notes:

1. *Outside lead frame holes (from dimension H) are circular.*
2. *Seal ring and lid are connected to Ground.*
3. *Lead material is Kovar with minimum 50 microinches gold plate over nickel.*
4. *Packages are shipped unformed with the ceramic tie bar.*
5. *CQ256 has a Heat Sink on the back.*

Ceramic Quad Flat Pack

	CQFP 208			CQFP 256		
Dimension	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	2.20	2.44	2.67	2.19	2.44	2.69
A1	2.05	2.29	2.52	2.04	2.29	2.50
b	0.18	0.20	0.22	0.18	0.20	0.22
c	0.10	0.15	0.20	0.10	0.15	0.18
D1/E1	28.96	29.21	29.46	35.64	36.00	36.36
D2/E2	25.50 BSC			31.50 BSC		
e	0.50 BSC			0.50 BSC		
F	6.86	7.75	8.64	7.67	7.75	7.83
H	70.00 BSC			70.00 BSC		
K	65.90 BSC			65.90 BSC		
L1	74.60	75.00	75.40	74.62	75.00	75.38
t				0.38	0.51	0.64

Notes:

1. *All dimensions are in millimeters.*
2. *BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

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