



**PRODUCT INFORMATION
LETTER**

PIL APG-MID/14/8431
Dated 21 Apr 2014

BOLERO FAMILY : ERRATA SHEET Update

Sales Type/product family label	SPC560B/C/Dxx, SPC56ECxx, SPC564Bxx
Type of change	Product electrical spec. change
Reason for change	ERRATA SHEET UPDATE
Description	Please be informed that Errata Sheet for Bolero Family has been updated.
Forecasted date of implementation	30-Apr-2014
Forecasted date of samples for customer	14-Apr-2014
Forecasted date for STMicroelectronics change Qualification Plan results availability	30-Apr-2014
Involved ST facilities	NA

DOCUMENT APPROVAL

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BOLERO FAMILY : ERRATA SHEET Update

WHAT:

Please be informed that Errata Sheet for Bolero Family has been updated.

HOW:

See attached **ERR004146**.

WHO:

All The products belonging to BOLERO Family:

- SPC560B/C/Dxx
- SPC56ECxx
- SPC564Bxx

ERR004146: When an ADC conversion is injected, the aborted channel is not restored under certain conditions

Description:

When triggered conversions interrupt the ADC, it is possible that the aborted conversion does not get restored to the ADC and is not converted during the chain. Vulnerable configurations are:

- Injected chain over a normal chain
- CTU trigger over a normal chain
- CTU trigger over an injected chain

When any of these triggers arrive whilst the ADC is in the conversion stage of the sample and conversion, the sample is discarded and is not restored. This means that the channel data register will not show the channel as being valid and the CEOCFRx field will not indicate a pending conversion. The sample that was aborted is lost. When the trigger arrives during the final channel in a normal or injected chain, the same failure mode can cause two ECH/JECH interrupts to be raised.

If the trigger arrives during the sampling phase of the last channel in the chain, an ECH is triggered immediately, the trigger is processed and the channel is restored and after sampling/conversion, a second ECH interrupt occurs.

In scan mode, the second ECH does not occur if the trigger arrives during the conversion phase. In one-shot mode, the trigger arriving during the conversion phase of the last channel restarts the whole conversion chain and the next ECH occurs at completion of that chain.

Workaround:

It is suggested that the application check for valid data using the CDR status bits or the CEOCFRx registers to ensure all expected channels have converted. This can be tested by running a bitwise AND and an XOR with either the JCMRx or NCMRx registers and the CEOCFRx registers during the ECH or JECH handler. Any non-zero value for (xCMRx & (xCMRx CEOCFRx)) indicates that a channel has been missed and conversion should be requested again.

Spurious ECH/JECH interrupts can be detected by checking the NSTART/JSTART flags in the ADC Module Status Registers – if the flag remains set during an ECH/JECH interrupt then another interrupt will follow after the restored channel or chain has been sampled and converted.

The spurious ECH/JECH workaround above applies to single-shot conversions. In single-shot mode, NSTART changes from 1 to 0. Therefore, the user can rely on checking the NSTART bit to confirm if a spurious ECH has occurred. However, for scan mode, the NSTART bit will remain set during normal operation, so it cannot be relied upon to check for the spurious ECH/JECH issue. Consequently, if CTU is being used in trigger mode, the conversions must be single-shot and not scan mode.

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