FAIRCHILD SEMICONDUCTOR®

January 2010

Single-Channel: 6N135M, 6N136M, HCPL4503M
Dual-Channel: HCPL2530M, HCPL2531M (Preliminary)
High Speed Transistor Optocouplers

Features

- High speed –1 MBit/s
- Superior CMR – 10kV/µs
- Dual-Channel HCPL2530M, HCPL2531M (Preliminary)
- CTR guaranteed 0–70°C
- U.L. recognized (File # E90700, Vol. 2)
- VDE recognition (pending)
  - – Ordering option 'V', e.g., 6N135VM
- 5,000Vrms (1 minute) isolation rating
- Superior CMR of 15,000V/µs min. (HCPL4503M)
- No base connection for improved noise immunity (HCPL4503M)

Applications

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

Description

The HCPL4503M, 6N135M, 6N136M, HCPL2530M and HCPL2531M optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

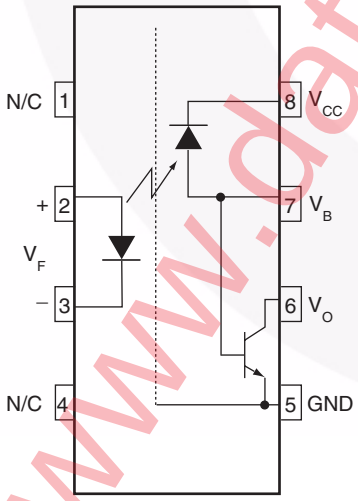
The HCPL4503M has no internal connection to the phototransistor base for improved noise immunity.

An internal noise shield provides superior common mode rejection of up to 50,000V/µs.

Related Resources

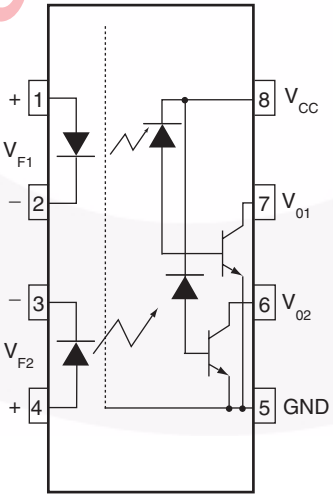
- www.fairchildsemi.com/products/opto/
- www.fairchildsemi.com/pf/HC/HCPL0500.html
- www.fairchildsemi.com/pf/FO/FODM452.html
- www.fairchildsemi.com/pf/FO/FOD050L.html

Schematics



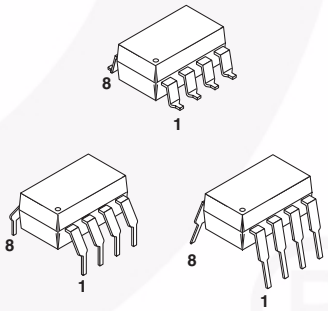
6N135M, 6N136M, HCPL4503M

Pin 7 is not connected in the HCPL4503M



HCPL2530M/HCPL2531M

Package Outlines



Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Value	Units
T_{STG}	Storage Temperature		-40 to +125	°C
T_{OPR}	Operating Temperature		-40 to +100	°C
T_{SOL}	Lead Solder Temperature (Wave)		260 for 10 sec	°C
EMITTER				
I_F (avg)	DC/Average Forward Input Current Each Channel[1]		25	mA
I_F (pk)	Peak Forward Input Current Each Channel[2]	50% duty cycle, 1ms P.W.	50	mA
I_F (trans)	Peak Transient Input Current Each Channel	≤1µs P.W., 300pps	1.0	A
V_R	Reverse Input Voltage Each Channel		5	V
P_D	Input Power Dissipation Each Channel[3]	6N135M, 6N136M, HCPL4503M	45	mW
		HCPL2530M, HCPL2531M		
DETECTOR				
I_O (avg)	Average Output Current Each Channel		8	mA
I_O (pk)	Peak Output Current Each Channel		16	mA
V_{EBR}	Emitter-Base Reverse Voltage	6N135M and 6N136M only	5	V
V_{CC}	Supply Voltage		-0.5 to 30	V
V_O	Output Voltage		-0.5 to 20	V
I_B	Base Current	6N135M and 6N136M only	5	mA
PD	Output Power Dissipation Each Channel[4]	6N135M, 6N136M, HCPL4503M	100	mW
		HCPL2530M, HCPL2531M	35	mW

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.

Electrical Characteristics

(T_A = 0 to 70°C unless otherwise specified. Typical value is measured at T_A = 25ºC and V_{CC} = 5.0V.)

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Device	Min.	Typ.	Max.	Unit
EMITTER							
V_F	Input Forward Voltage	I_F = 16mA, T_A =25°C	All		1.45	1.7	V
		I_F = 16mA	All			1.8	
B_{VR}	Input Reverse Breakdown Voltage	I_R = 10 µA	All	5.0	21		V
$\Delta V_F/\Delta T_A$	Temperature Coefficient of Forward Voltage	I_F = 16mA	All		-1.7		mV/°C
DETECTOR							
I_{OH}	Logic High Output Current	I_F = 0mA, V_O = V_{CC} = 5.5V, T_A =25°C	All		0.0007	0.5	µA
		I_F = 0mA, V_O = V_{CC} = 15V, T_A =25°C	6N135M 6N136M HCPL4503M		0.0019	1	
		I_F = 0mA, V_O = V_{CC} = 15V	All			50	
I_{CCL}	Logic Low Supply Current	I_F = 16mA, V_O = Open, V_{CC} = 15V	6N135M 6N136M HCPL4503M		163	200	µA
		I_{F1} = I_{F2} = 16mA, V_O = Open, V_{CC} = 15V	HCPL2530M HCPL2531M			400	
I_{CCH}	Logic High Supply Current	I_F = 0mA, V_O = Open, V_{CC} = 15V, T_A =25°C	6N135M 6N136M HCPL4503M		0.0002	1	µA
		I_F = 0mA, V_O = Open, V_{CC} = 15V	6N135M 6N136M HCPL4503M		0.0004	2	
		I_F = 0mA, V_O = Open, V_{CC} = 15V	HCPL2530M HCPL2531M			4	

Electrical Characteristics (Continued)

(T_A = 0 to 70°C unless otherwise specified. Typical value is measured at T_A = 25ºC and V_{CC} = 5.0V.)

Transfer Characteristics

Symbol	Parameter	Test Conditions		Device	Min.	Typ.	Max.	Unit
COUPLED								
CTR	Current Transfer Ratio[5]	I_F = 16mA, V_O = 0.4 V, V_{CC} = 4.5V, T_A =25°C		6N135M	7	38	50	%
				HCPL2530M				
				6N136M HCPL4503M	19	38	50	%
				HCPL2531M				
		I_F = 16mA, V_{CC} = 4.5V	V_{OL} = 0.4V	6N135M	5			%
			V_{OL} = 0.5V	HCPL2530M				
			V_{OL} = 0.4V	6N136M HCPL4503M	15			%
			V_{OL} = 0.5V	HCPL2531M				
V_{OL}	Logic LOW Output Voltage	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V, T_A =25°C		6N135M		0.12	0.4	V
				HCPL2530M			0.5	
		I_F = 16mA, I_O = 3mA, V_{CC} = 4.5V, T_A =25°C		6N136M HCPL4503M		0.20	0.4	
				HCPL2531M			0.5	
		I_F = 16mA, I_O = 0.8mA, V_{CC} = 4.5V		6N135M		0.11	0.5	
				HCPL2530M				
		I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V		HCPL4503M		0.18	0.5	
				HCPL2531M				

Note:

5. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.

Electrical Characteristics (Continued)

(T_A = 0 to 70°C unless otherwise specified. Typical values are measured at T_A = 25°C and V_{CC} = 5V.)

Switching Characteristics (V_{CC} = 5V)

Symbol	Parameter	Test Conditions	Device	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay Time to Logic LOW	T_A = 25°C, R_L = 4.1kΩ, I_F = 16mA[6] (Fig. 7)	6N135M		0.23	1.5	µs
			HCPL2530M				
		R_L = 1.9kΩ, I_F = 16mA, T_A = 25°C[7] (Fig. 7)	6N136M HCPL4503M		0.25	0.8	µs
			HCPL2531M				
		R_L = 4.1kΩ, I_F = 16mA[6] (Fig. 7)	6N135M HCPL2530M			2.0	µs
		R_L = 1.9kΩ, I_F = 16mA[7] (Fig. 7)	6N136M HCPL4503M HCPL2531M			1.0	µs
t_{PLH}	Propagation Delay Time to Logic HIGH	T_A = 25°C, (R_L = 4.1kΩ, I_F = 16mA[6] (Fig. 7)	6N135M		0.45	1.5	µs
			HCPL2530M				
		R_L = 1.9kΩ, I_F = 16mA[7] (Fig. 7) T_A = 25°C	6N136M HCPL4503M		0.26	0.8	µs
			HCPL2531M				
		R_L = 4.1kΩ, I_F = 16mA[6] (Fig. 7)	6N135M HCPL2530M			2.0	µs
		R_L = 1.9kΩ, I_F = 16mA[7] (Fig. 7)	6N136M HCPL4503M HCPL2531M			1.0	µs
$\|CM_H\|$	Common Mode Transient Immunity at Logic High	I_F = 0mA, V_{CM} = $10V_{P-P}$, R_L = 4.1kΩ, T_A = 25°C[8] (Fig. 8)	6N135M HCPL2530M		10,000		V/µs
		I_F = 0mA, V_{CM} = $10V_{P-P}$, R_L = 1.9kΩ, T_A = 25°C[8] (Fig. 8)	6N136M HCPL2531M		10,000		V/µs
		I_F = 0mA, V_{CM} = $1,500V_{P-P}$, R_L = 1.9kΩ, T_A = 25°C[8] (Fig. 8)	HCPL4503M	15,000	50,000		
$\|CM_L\|$	Common Mode Transient Immunity at Logic Low	I_F = 16mA, V_{CM} = $10V_{P-P}$, R_L = 4.1kΩ, T_A = 25°C[8] (Fig. 8)	6N135M HCPL2530M		10,000		V/µs
		I_F = 16mA, V_{CM} = $10V_{P-P}$, R_L = 1.9kΩ[8] (Fig. 8)	6N136M HCPL2531M		10,000		V/µs
		I_F = 0mA, V_{CM} = $1,500V_{P-P}$, R_L = 1.9kΩ, T_A = 25°C[8] (Fig. 8)	HCPL4503M	15,000	50,000		

Notes:

6. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
7. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and 5.6kΩ pull-up resistor.
8. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O > 2.0V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O < 0.8V).

Electrical Characteristics (Continued)

(T_A = 0 to 70°C unless otherwise specified. Typical values are measured at T_A = 25°C and V_{CC} = 5V.)

Isolation Characteristics (T_A = 0 to 70°C Unless otherwise specified)

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Withstand Insulation Test Voltage	RH ≤ 50%, T_A = 25°C, I_{I-O} ≤ 10μA, t = 1 min., f = 50Hz[9][11]	5,000			V_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500VDC[9]		10^{11}		Ω
C_{I-O}	Capacitance (Input to Output)	f = 1MHz, V_{I-O} = 0V[9]		1		pF
I_{I-I}	Input-Input Insulation Leakage Current	RH ≤ 45%, V_{I-I} = 500VDC[10] t = 5 s, (HCPL2530M/2531M only)				μA
R_{I-I}	Input-Input Resistance	V_{I-I} = 500 VDC[10] (HCPL2530M/2531M only)				Ω
C_{I-I}	Input-Input Capacitance	f = 1MHz[10] (HCPL2530M/2531M only)				pF

Notes:

9. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
10. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
11. 5,000Vrms for 1 minute duration is equivalent to 6,000Vrms for 1 second duration.

Typical Performance Curves

Fig. 1 Normalized CTR vs. Forward Current

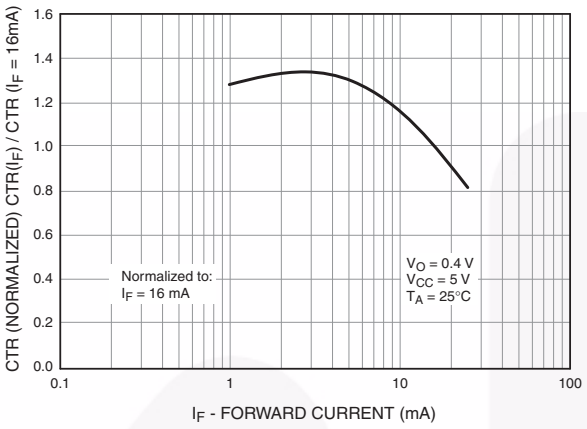


Fig. 2 Normalized CTR vs. Temperature

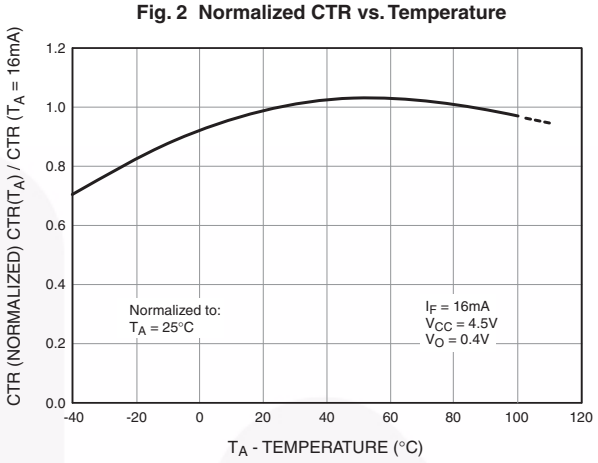


Fig. 3 Output Current vs. Output Voltage

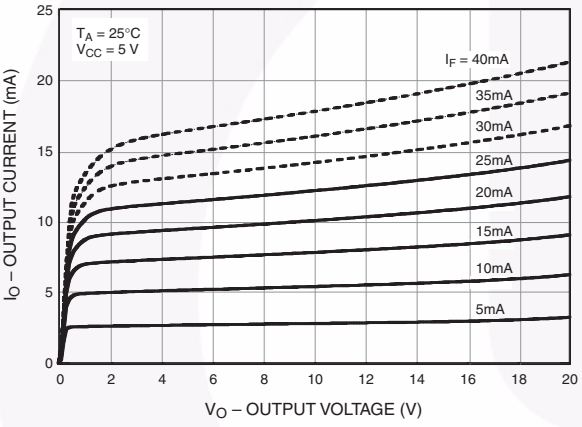


Fig. 4 Logic High Output Current vs. Temperature

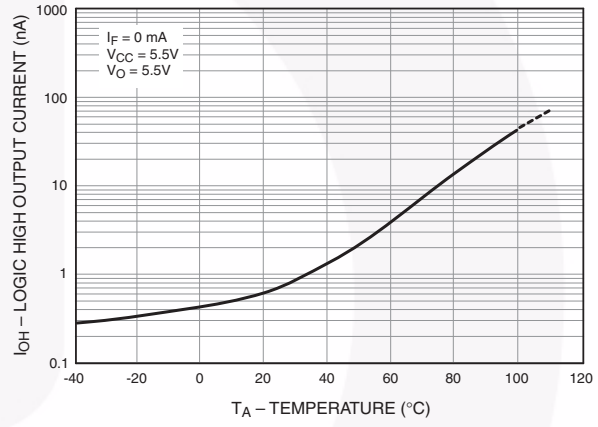


Fig. 5 Propagation Delay vs. Temperature

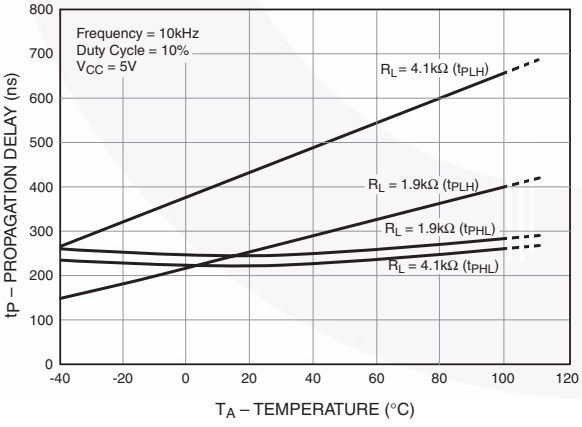
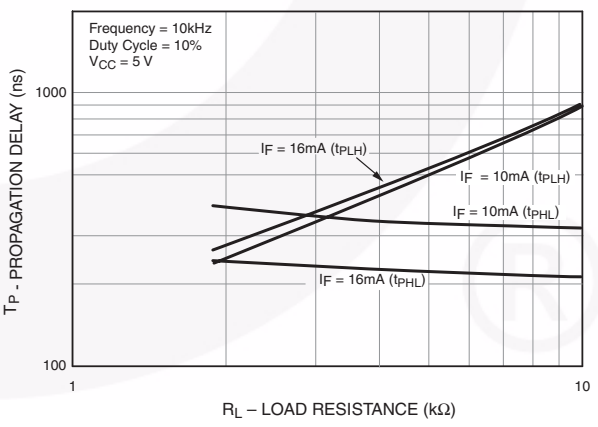
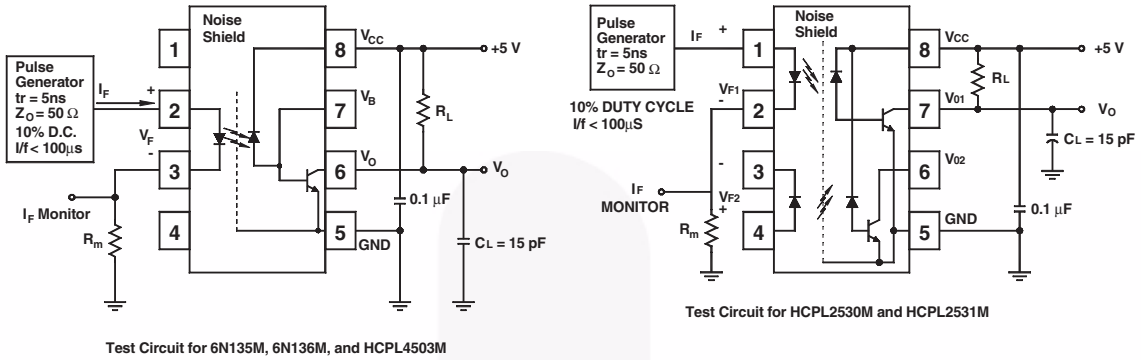


Fig. 6 Propagation Delay vs. Load Resistance



Test Circuits



Test Circuit for 6N135M, 6N136M, and HCPL4503M

Test Circuit for HCPL2530M and HCPL2531M

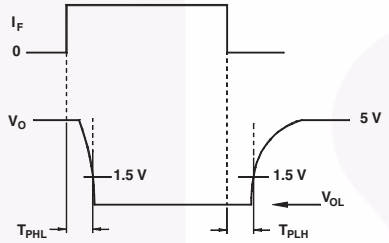
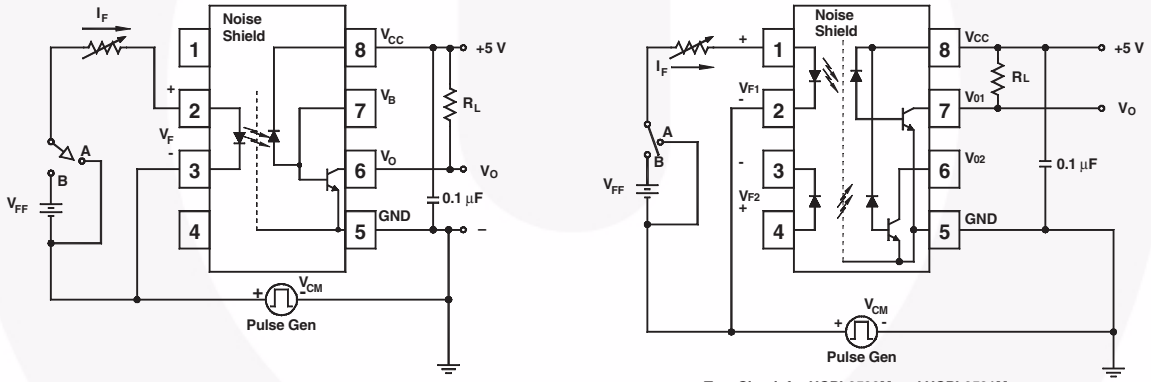


Fig. 7 Switching Time Test Circuit



Test Circuit for 6N135M, 6N136M, and HCPL4503M

Test Circuit for HCPL2530M and HCPL2531M

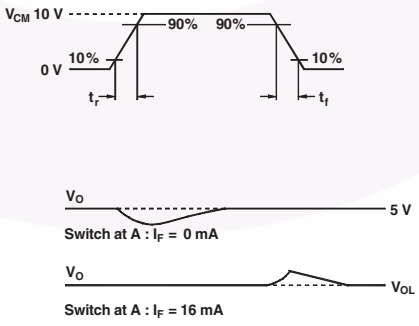
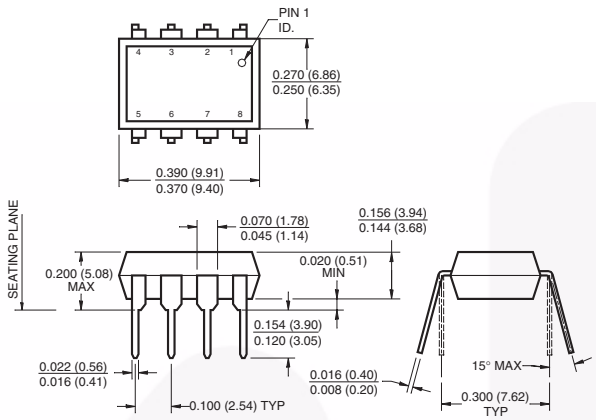


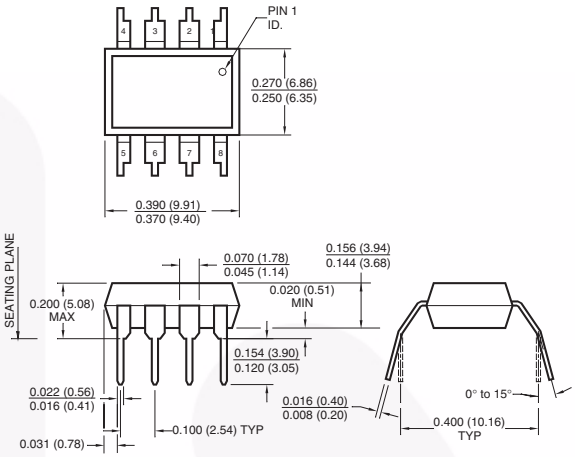
Fig. 8 Common Mode Immunity Test Circuit

Package Dimensions

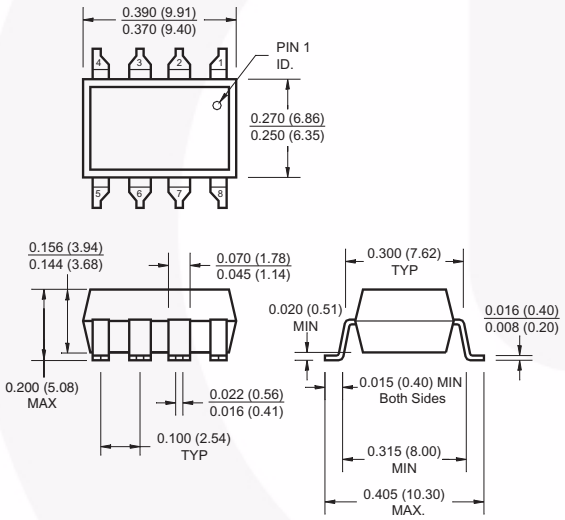
Through Hole



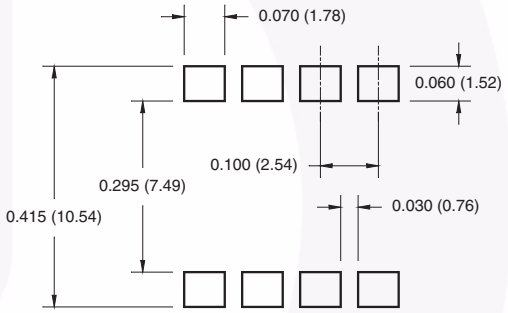
0.4" Lead Spacing (Option T)



Surface Mount – 0.3" Lead Spacing (Option S)



8-Pin Surface Mount DIP – Land Pattern (Option S)



Note:
All dimensions are in inches (millimeters)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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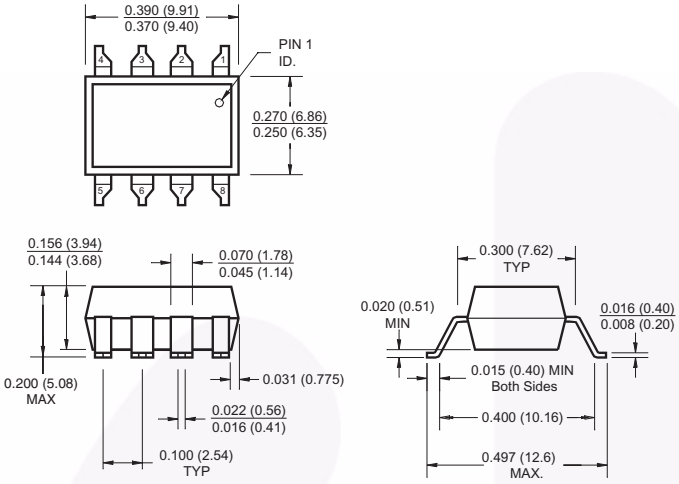
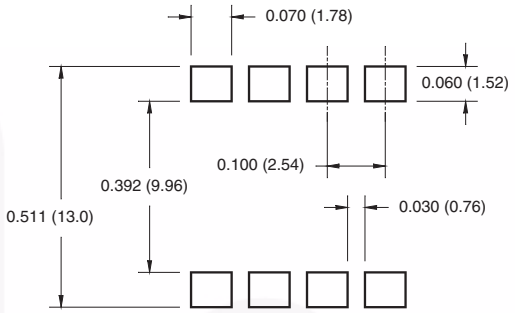
http://www.fairchildsemi.com/packaging/

Package Dimensions (Continued)

Surface Mount – 0.4" Lead Spacing (Option TS) (Pending)



8-Pin Surface Mount DIP – Land Pattern (Option TS)



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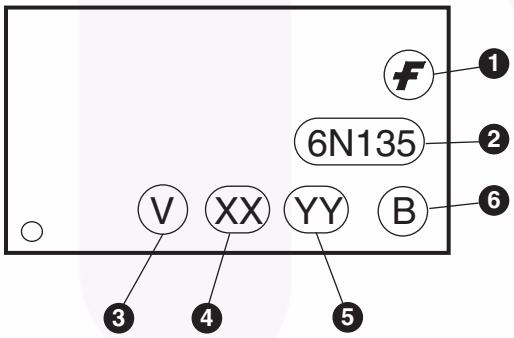
Ordering Information

Option	Example Part Number	Description
No option	6N135M	Standard through hole lead form (50 units per tube)
S	6N135SM	Surface mount lead bend
SD	6N135SDM	Surface mount; tape and reel
V	6N135VM	IEC60747-5-2 (approval pending)
TSV	6N135TSVM	IEC60747-5-2 (approval pending); surface mount
TSDV	6N135TSDVM	IEC60747-5-2 (approval pending); surface mount; tape and reel
TV	6N135TVM	IEC60747-5-2 (approval pending); 0.4" lead spacing
SV	6N135SVM	IEC60747-5-2 (approval pending); surface mount
SDV	6N135SDVM	IEC60747-5-2 (approval pending); surface mount; tape and reel

Marking Information

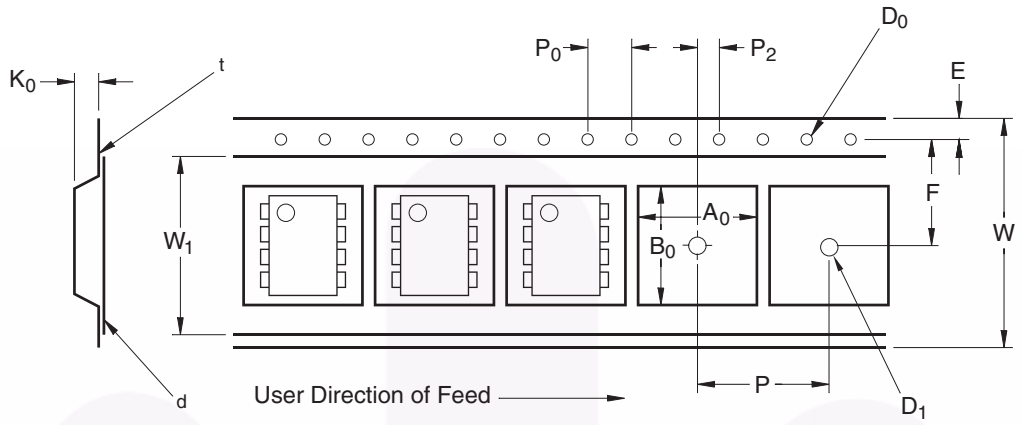


Definitions	
1	Fairchild logo
2(1)	Device number
3	IEC60747-5-2 mark (Note: Only appears on parts ordered with this option – See order entry table)
4	Two digit year code, e.g., ‘08’
5	Two digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

Note:

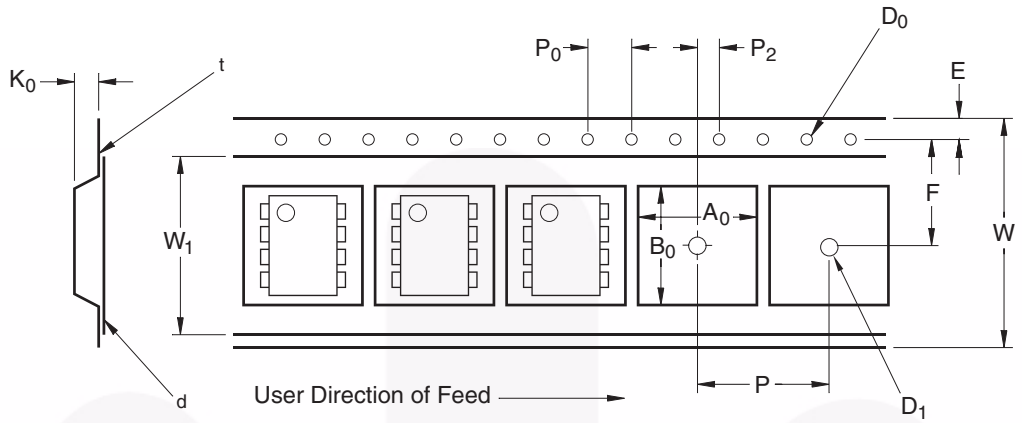
1. ‘HCPL’ devices are marked with only the numeric characters (for example, HCPL4503M is marked as ‘4503’).
2. The ‘M’ suffix is an ordering identifier only. It is used to indicated the white package version. The ‘M’ does no appear in the top mark.

Carrier Tape Specifications (Option SD)



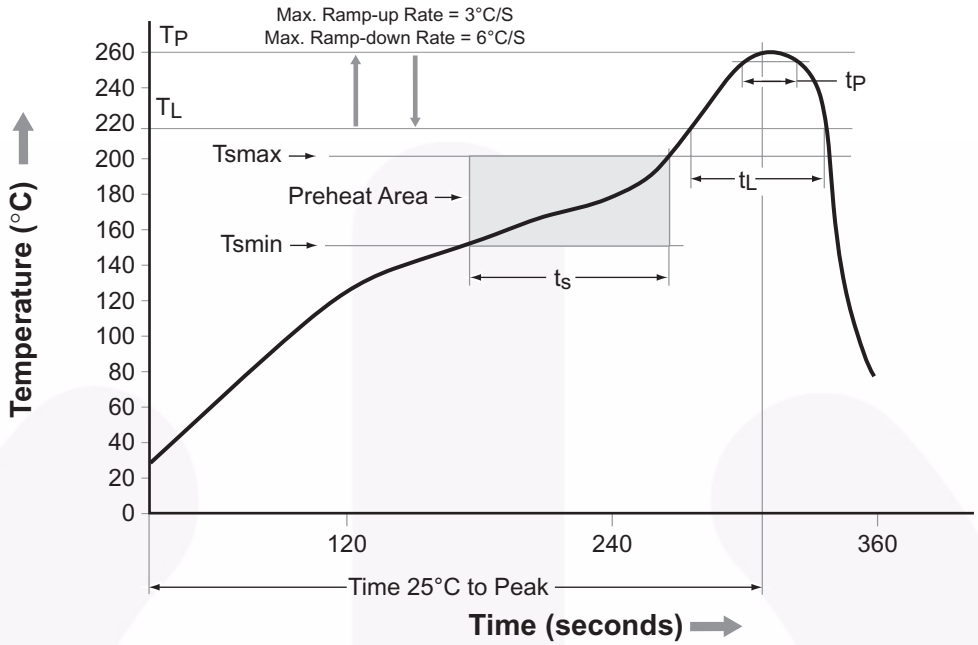
Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A_0	Pocket Dimensions	10.30 ±0.20
B_0		10.30 ±0.20
K_0		4.90 ±0.20
W_1	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

Carrier Tape Specifications (Option TSR2) (Pending)



Symbol	Description	Dimension in mm
W	Tape Width	24.0 ± 0.3
t	Tape Thickness	0.40 ± 0.1
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	11.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	16.0 ± 0.1
A_0	Pocket Dimensions	12.80 ± 0.1
B_0		10.35 ± 0.1
K_0		5.7 ±0.1
W_1	Cover Tape Width	21.0 ± 0.1
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

Reflow Profile



Profile Freature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60–120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

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