

## FEATURES

- 1-of-4 Bidirectional Translating Switches
- I<sup>2</sup>C Bus and SMBus Compatible
- Active-Low Reset Input
- Three Address Pins, Allowing up to Eight Devices on the I<sup>2</sup>C Bus
- Channel Selection Via I<sup>2</sup>C Bus
- Power Up With All Switch Channels Deselected
- Low R<sub>ON</sub> Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5.5-V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA Per JESD 78
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

The PCA9546A is a quad bidirectional translating switch controlled via the I<sup>2</sup>C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active-low reset ( $\overline{\text{RESET}}$ ) input allows the PCA9546A to recover from a situation in which one of the downstream I<sup>2</sup>C buses is stuck in a low state. Pulling  $\overline{\text{RESET}}$  low resets the I<sup>2</sup>C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the V<sub>CC</sub> pin can be used to limit the maximum high voltage, which will be passed by the PCA9546A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts without any additional protection. External pullup resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5-V tolerant.

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RGV              | Reel of 3000 | PCA9546ARVR           | PREVIEW          |
|                | QFN – RGY              | Reel of 1000 | PCA9546ARGYR          | PD546A           |
|                | SOIC – DW              | Tube of 40   | PCA9546ADW            | PCA9546A         |
|                |                        | Reel of 2000 | PCA9546ADWR           |                  |
|                |                        | Reel of 250  | PCA9546ADWT           | PREVIEW          |
|                | TSSOP – PW             | Tube of 90   | PCA9546APW            | PD546A           |
|                |                        | Reel of 2000 | PCA9546APWR           |                  |
|                |                        | Reel of 250  | PCA9546APWT           |                  |
|                | TVSOP – DGV            | Reel of 2000 | PCA9546ADGVR          | PD546A           |
|                |                        | Reel of 250  | PCA9546ADGVT          | PREVIEW          |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

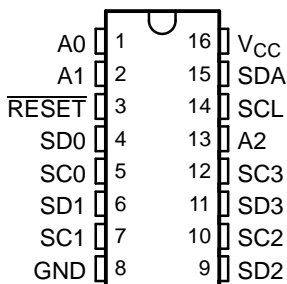


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

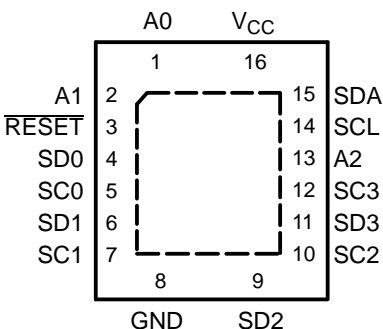
# PCA9546A 4-CHANNEL I<sup>2</sup>C AND SMBus SWITCH WITH RESET FUNCTION

SCPS148A—OCTOBER 2005—REVISED DECEMBER 2005

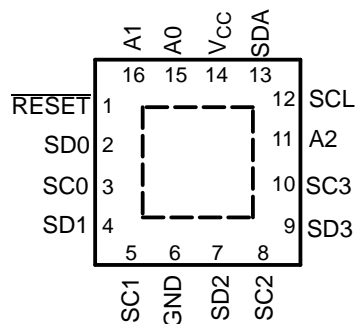
**DGV, DW, OR PW PACKAGE  
(TOP VIEW)**



**RGY PACKAGE  
(TOP VIEW)**



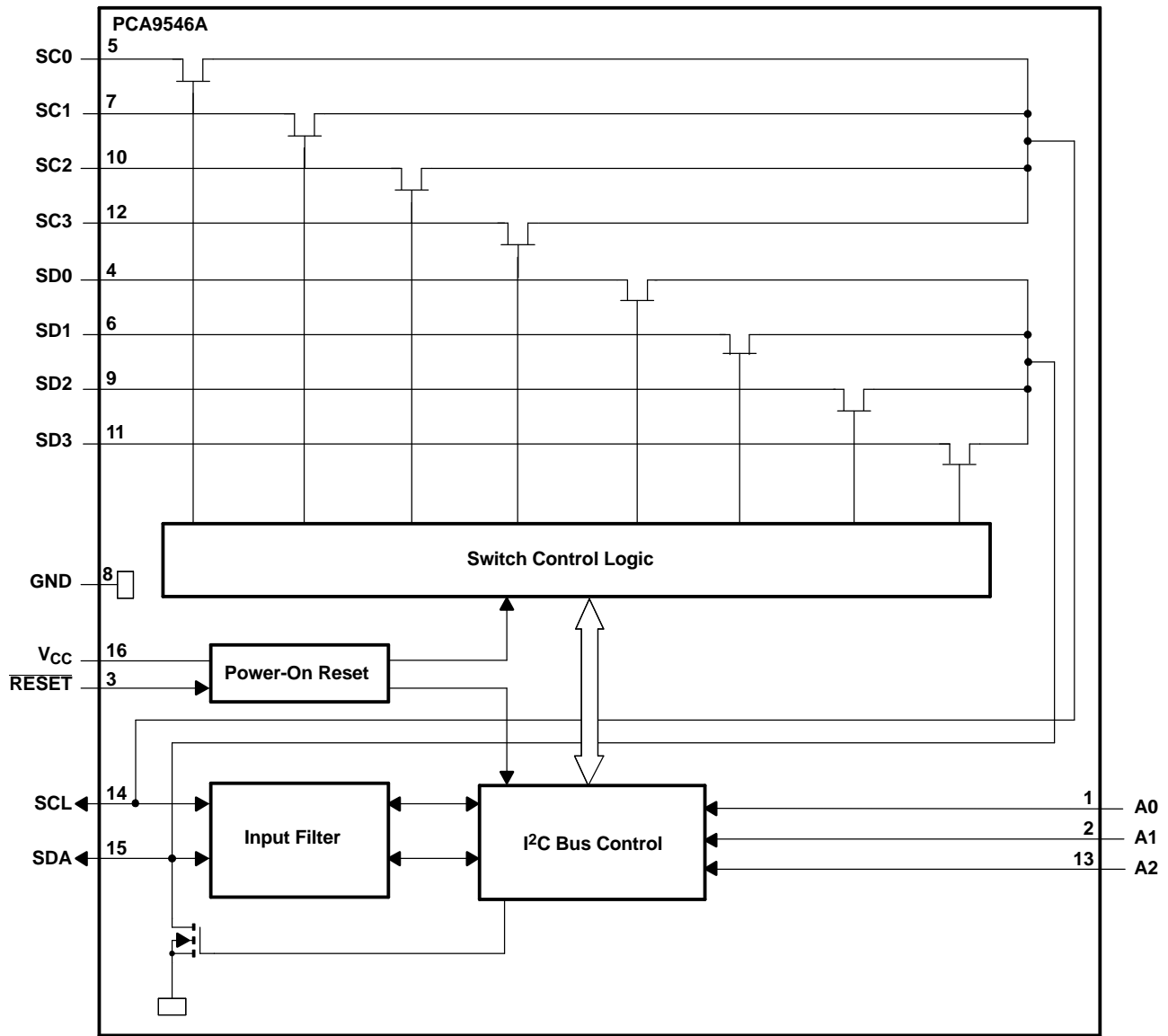
**RGV PACKAGE  
(TOP VIEW)**



## TERMINAL FUNCTIONS

| NO.                  |     | NAME  | DESCRIPTION            |
|----------------------|-----|-------|------------------------|
| DGV, DW, PW, AND RGY | RGV |       |                        |
| 1                    | 15  | A0    | Address input 0        |
| 2                    | 16  | A1    | Address input 1        |
| 3                    | 1   | RESET | Active low reset input |
| 4                    | 2   | SD0   | Serial data 0          |
| 5                    | 3   | SC0   | Serial clock 0         |
| 6                    | 4   | SD1   | Serial data 1          |
| 7                    | 5   | SC1   | Serial clock 1         |
| 8                    | 6   | GND   | Ground                 |
| 9                    | 7   | SD2   | Serial data 2          |
| 10                   | 8   | SC2   | Serial clock 2         |
| 11                   | 9   | SD3   | Serial data 3          |
| 12                   | 10  | SC3   | Serial clock 3         |
| 13                   | 11  | A2    | Address input 2        |
| 14                   | 12  | SCL   | Serial clock line      |
| 15                   | 13  | SDA   | Serial data line       |
| 16                   | 14  | VCC   | Supply power           |

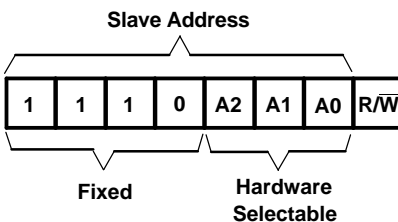
**BLOCK DIAGRAM**



Pin numbers shown are for the DGV, DW, PW, and RGY packages.

### Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9546A is shown in Figure 1. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low.

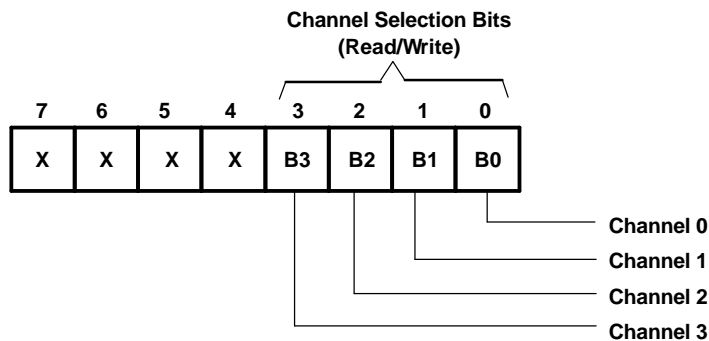


**Figure 1. PCA9546A Address**

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

### Control Register

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9546A, which is stored in the control register (see Figure 2). If multiple bytes are received by the PCA9546A, it will save the last byte received. This register can be written and read via the I<sup>2</sup>C bus.



**Figure 2. Control Register**

### Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). This register is written after the PCA9546A has been addressed. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I<sup>2</sup>C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)<sup>(1)</sup>

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | COMMAND  |
|----|----|----|----|----|----|----|----|--|
| X  | X  | X  | X  | X  | X  | X  | 0  | Channel 0 disabled                                   |
|    |    |    |    |    |    |    | 1  | Channel 0 enabled                                    |
| X  | X  | X  | X  | X  | X  | 0  | X  | Channel 1 disabled                                   |
|    |    |    |    |    |    |    |    | 1  |
| X  | X  | X  | X  | X  | 0  | X  | X  | Channel 2 disabled                                   |
|    |    |    |    |    | 1  |    |    | Channel 2 enabled                                    |
| X  | X  | X  | X  | 0  | X  | X  | X  | Channel 3 disabled                                   |
|    |    |    |    | 1  |    |    |    | Channel 3 enabled                                    |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | No channel selected,<br>power-up/reset default state |

(1) Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 and 2 are enabled. Care should be taken not to exceed the maximum bus capacity.

## RESET Input

The  $\overline{\text{RESET}}$  input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of  $t_{\text{WL}}$ , the PCA9446A resets its registers and I<sup>2</sup>C state machine and deselects all channels. The  $\overline{\text{RESET}}$  input must be connected to  $V_{\text{CC}}$  through a pullup resistor.

## Power-On Reset

When power is applied to  $V_{\text{CC}}$ , an internal power-on reset holds the PCA9546A in a reset condition until  $V_{\text{CC}}$  has reached  $V_{\text{POR}}$ . At this point, the reset condition is released, and the PCA9546A registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter,  $V_{\text{CC}}$  must be lowered below 0.2 V to reset the device.

## Voltage Translation

The pass-gate transistors of the PCA9546A are constructed such that the  $V_{\text{CC}}$  voltage can be used to limit the maximum voltage that will be passed from one I<sup>2</sup>C bus to another.

Figure 3 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using the data specified in the electrical characteristics section of this data sheet). In order for the PCA9546A to act as a voltage translator, the  $V_{\text{pass}}$  voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V, and the downstream buses are 3.3 V and 2.7 V, then  $V_{\text{pass}}$  must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 3,  $V_{\text{pass}}(\text{max})$  is at 2.7 V when the PCA9546A supply voltage is 3.5 V or lower, so the PCA9546A supply voltage could be set to 3.3 V. Pullup resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 12).

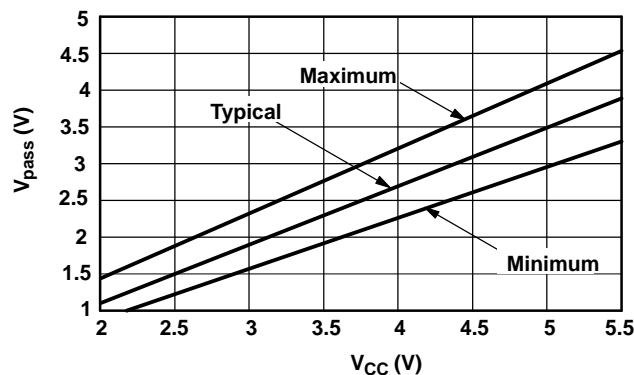
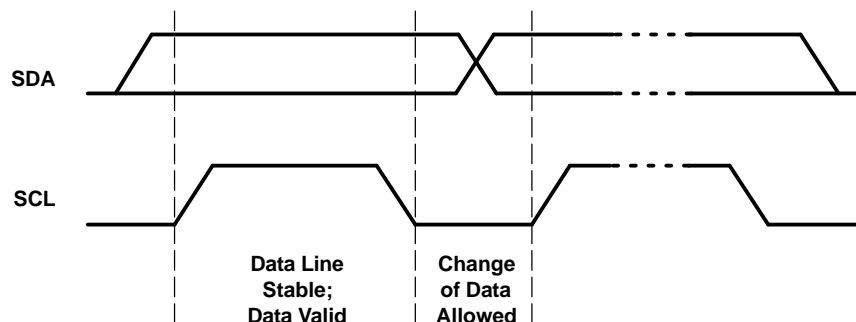


Figure 3.  $V_{\text{pass}}$  Voltage vs  $V_{\text{CC}}$

### I<sup>2</sup>C Interface

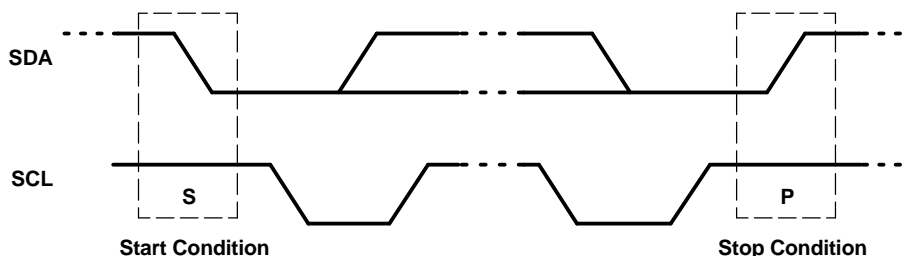
The I<sup>2</sup>C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 4).



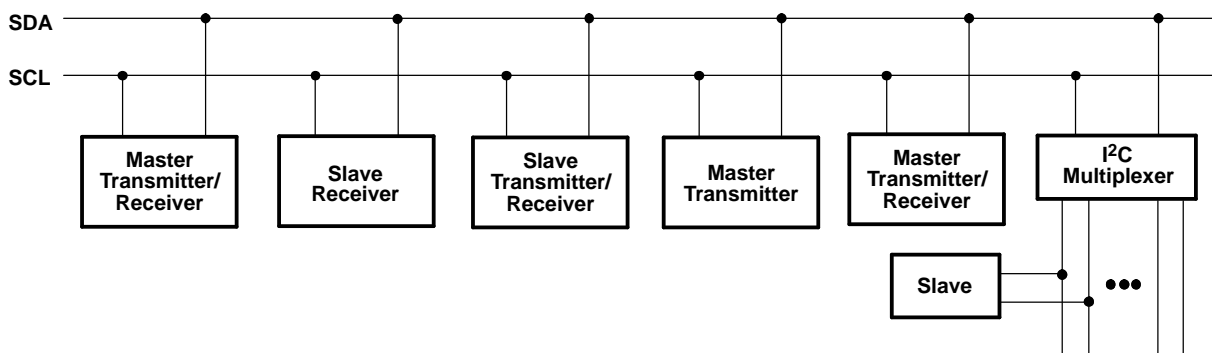
**Figure 4. Bit Transfer**

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 5).



**Figure 5. Definition of Start and Stop Conditions**

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 6).



**Figure 6. System Configuration**

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). Setup and hold times must be taken into account.

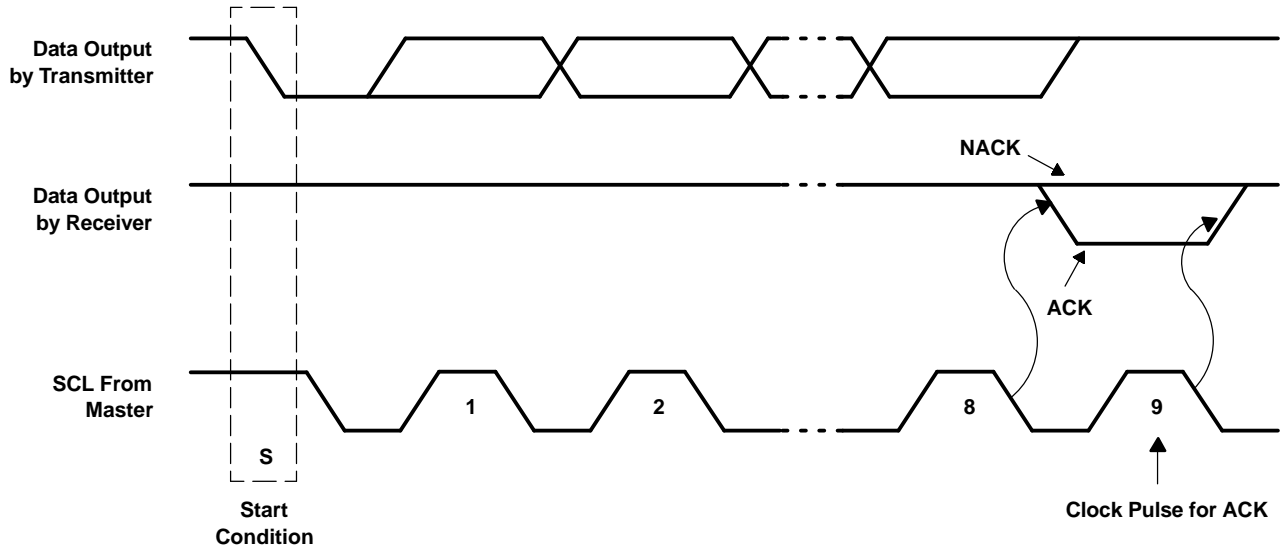


Figure 7. Acknowledgment on the I<sup>2</sup>C Bus

Data is transmitted to the PCA9546A control register using the write mode shown in Figure 8.

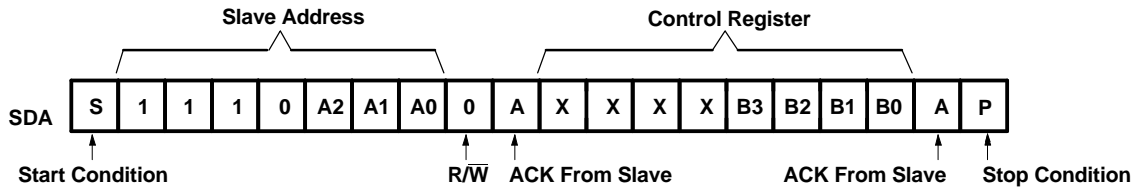


Figure 8. Write Control Register

Data is read from the PCA9546A control register using the read mode shown in Figure 9.

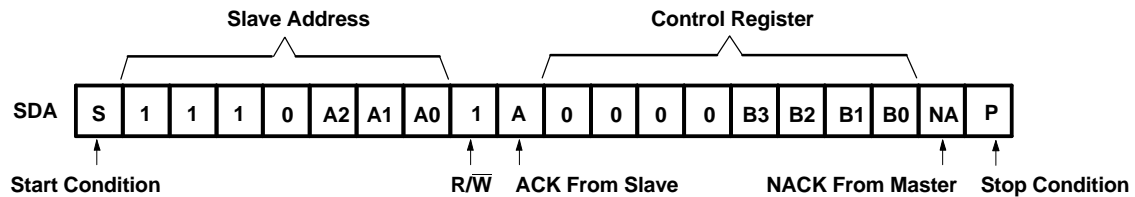


Figure 9. Read Control Register

# PCA9546A 4-CHANNEL I<sup>2</sup>C AND SMBus SWITCH WITH RESET FUNCTION

SCPS148A—OCTOBER 2005—REVISED DECEMBER 2005

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |  | MIN         | MAX  | UNIT |
|------------------|--|-------------|------|------|
| V <sub>CC</sub>  | Supply voltage range                       | -0.5        | 7    | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>         | -0.5        | 7    | V    |
| I <sub>I</sub>   | Input current                              |             | ±20  | mA   |
| I <sub>O</sub>   | Output current                             |             | ±25  | mA   |
|                  | Continuous current through V <sub>CC</sub> |             | ±100 | mA   |
|                  | Continuous current through GND             |             | ±100 | mA   |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(3)</sup>   | DGV package | 120  | °C/W |
|                  |  | DW package  | 57   |      |
|                  |  | PW package  | 108  |      |
|                  |  | RGV package | TBD  |      |
|                  |  | RGY package | 50   |      |
| P <sub>tot</sub> | Total power dissipation                    |             | 400  | mW   |
| T <sub>stg</sub> | Storage temperature range                  | -65         | 150  | °C   |
| T <sub>A</sub>   | Operating free-air temperature range       | -40         | 85   | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

|                 |                                | MIN                              | MAX                   | UNIT                  |
|-----------------|--------------------------------|----------------------------------|-----------------------|-----------------------|
| V <sub>CC</sub> | Supply voltage                 | 2.3                              | 5.5                   | V                     |
| V <sub>IH</sub> | High-level input voltage       | SCL, SDA                         | 0.7 × V <sub>CC</sub> | 6                     |
|                 |                                | A2-A0, $\overline{\text{RESET}}$ | 0.7 × V <sub>CC</sub> | V <sub>CC</sub> + 0.5 |
| V <sub>IL</sub> | Low-level input voltage        | SCL, SDA                         | -0.5                  | 0.3 × V <sub>CC</sub> |
|                 |                                | A2-A0, $\overline{\text{RESET}}$ | -0.5                  | 0.3 × V <sub>CC</sub> |
| T <sub>A</sub>  | Operating free-air temperature | -40                              | 85                    | °C                    |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                           |                                       | TEST CONDITIONS  |   | V <sub>CC</sub>  | MIN                     | TYP <sup>(1)</sup> | MAX | UNIT |
|-------------------------------------|---------------------------------------|--|---|------------------|-------------------------|--------------------|-----|------|
| V <sub>POR</sub>                    | Power-on reset voltage <sup>(2)</sup> | No load, V <sub>I</sub> = V <sub>CC</sub> or GND                   |   | V <sub>POR</sub> | 1.6                     | 2.1                |     | V    |
| V <sub>pass</sub>                   | Switch output voltage                 | V <sub>SWin</sub> = V <sub>CC</sub> , I <sub>SWout</sub> = -100 μA |   | 5 V              | 3.6                     |                    |     | V    |
|                                     |                                       |  |   | 4.5 V to 5.5 V   | 2.6                     | 4.5                |     |      |
|                                     |                                       |  |   | 3.3 V            | 1.9                     |                    |     |      |
|                                     |                                       |  |   | 3 V to 3.6 V     | 1.6                     | 2.8                |     |      |
|                                     |                                       |  |   | 2.5 V            | 1.5                     |                    |     |      |
|                                     |                                       |  |   | 2.3 V to 2.7 V   | 1.1                     | 2                  |     |      |
| I <sub>OL</sub>                     | SCL, SDA                              |  |   | 2.3 V to 5.5 V   | 3                       | 7                  |     | mA   |
|                                     |                                       |  |   |                  | V <sub>OL</sub> = 0.4 V | 6                  | 10  |      |
| I <sub>I</sub>                      | SCL, SDA                              | V <sub>I</sub> = V <sub>CC</sub> or GND                            |   | 2.3 V to 5.5 V   |                         |                    | ±1  | μA   |
|                                     | SC3–SC0, SD3–SD0                      |  |   |                  |                         |                    | ±1  |      |
|                                     | A2–A0                                 |  |   |                  |                         |                    | ±1  |      |
|                                     | RESET                                 |  |   |                  |                         |                    | ±1  |      |
| I <sub>CC</sub>                     | Operating mode                        | f <sub>SCL</sub> = 100 kHz   | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                         | 5.5 V            | 3                       | 12                 | μA  |      |
|                                     |                                       |  |   | 3.6 V            | 3                       | 11                 |     |      |
|                                     |                                       |  |   | 2.7 V            | 3                       | 10                 |     |      |
|                                     | Standby mode                          | Low inputs   | V <sub>I</sub> = GND, I <sub>O</sub> = 0  | 5.5 V            | 0.3                     | 1                  |     |      |
|                                     |                                       |  |   | 3.6 V            | 0.1                     | 1                  |     |      |
|                                     |                                       | High inputs  | V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0                               | 2.7 V            | 0.1                     | 1                  |     |      |
|                                     |                                       |  |   | 5.5 V            | 0.3                     | 1                  |     |      |
|                                     |                                       |  |   | 3.6 V            | 0.1                     | 1                  |     |      |
| 2.7 V                               | 0.1                                   | 1  |   |                  |                         |                    |     |      |
| ΔI <sub>CC</sub>                    | Supply-current change                 | SCL, SDA   | SCL or SDA input at 0.6 V, Other inputs at V <sub>CC</sub> or GND                   |                  | 8                       | 15                 | μA  |      |
|                                     |                                       |  | SCL or SDA input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.3 V to 5.5 V   | 8                       | 15                 |     |      |
| C <sub>I</sub>                      | A2–A0                                 | V <sub>I</sub> = V <sub>CC</sub> or GND                            |   | 2.3 V to 5.5 V   | 4.5                     | 6                  | pF  |      |
|                                     | RESET                                 |  |   |                  | 4.5                     | 5.5                |     |      |
| C <sub>IO(OFF)</sub> <sup>(3)</sup> | SCL, SDA                              | V <sub>I</sub> = V <sub>CC</sub> or GND, Switch OFF                |   | 2.3 V to 5.5 V   | 15                      | 19                 | pF  |      |
|                                     | SC3–SC0, SD3–SD0                      |  |   |                  | 6                       | 8                  |     |      |
| R <sub>ON</sub>                     | Switch on-state resistance            |  |   | 4.5 V to 5.5 V   | 4                       | 9                  | 16  | Ω    |
|                                     |                                       |  |   | 3 V to 3.6 V     | 5                       | 11                 | 20  |      |
|                                     |                                       |  |   | 2.3 V to 2.7 V   | 7                       | 16                 | 45  |      |

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V<sub>CC</sub>), T<sub>A</sub> = 25°C.

(2) The power-on reset circuit resets the I<sup>2</sup>C bus logic with V<sub>CC</sub> < V<sub>POR</sub>. V<sub>CC</sub> must be lowered to 0.2 V to reset the device.

(3) C<sub>IO(ON)</sub> depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON.

# PCA9546A 4-CHANNEL I<sup>2</sup>C AND SMBus SWITCH WITH RESET FUNCTION

SCPS148A–OCTOBER 2005–REVISED DECEMBER 2005

## I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 10)

|                        |  | STANDARD MODE<br>I <sup>2</sup> C BUS     |      | FAST MODE<br>I <sup>2</sup> C BUS     |     | UNIT |
|------------------------|--|---|------|---------------------------------------|-----|------|
|                        |  | MIN                                       | MAX  | MIN                                   | MAX |      |
| t <sub>scl</sub>       | I <sup>2</sup> C clock frequency                         | 0   | 100  | 0                                     | 400 | kHz  |
| t <sub>sch</sub>       | I <sup>2</sup> C clock high time                         | 4   |      | 0.6                                   |     | μs   |
| t <sub>scl</sub>       | I <sup>2</sup> C clock low time                          | 4.7                                       |      | 1.3                                   |     | μs   |
| t <sub>sp</sub>        | I <sup>2</sup> C spike time                              |   | 50   |                                       | 50  | ns   |
| t <sub>sds</sub>       | I <sup>2</sup> C serial-data setup time                  | 250                                       |      | 100                                   |     | ns   |
| t <sub>sdh</sub>       | I <sup>2</sup> C serial-data hold time                   | 0 <sup>(1)</sup>                          |      | 0 <sup>(1)</sup>                      |     | μs   |
| t <sub>icr</sub>       | I <sup>2</sup> C input rise time                         |   | 1000 | 20 + 0.1C <sub>b</sub> <sup>(2)</sup> | 300 | ns   |
| t <sub>icf</sub>       | I <sup>2</sup> C input fall time                         |   | 300  | 20 + 0.1C <sub>b</sub> <sup>(2)</sup> | 300 | ns   |
| t <sub>ocf</sub>       | I <sup>2</sup> C output fall time                        |   | 300  | 20 + 0.1C <sub>b</sub> <sup>(2)</sup> | 300 | ns   |
| t <sub>buf</sub>       | I <sup>2</sup> C bus free time between stop and start    | 4.7                                       |      | 1.3                                   |     | μs   |
| t <sub>sts</sub>       | I <sup>2</sup> C start or repeated start condition setup | 4.7                                       |      | 0.6                                   |     | μs   |
| t <sub>sth</sub>       | I <sup>2</sup> C start or repeated start condition hold  | 4   |      | 0.6                                   |     | μs   |
| t <sub>sps</sub>       | I <sup>2</sup> C stop condition setup                    | 4   |      | 0.6                                   |     | μs   |
| t <sub>vdL(Data)</sub> | Valid-data time (high to low) <sup>(3)</sup>             | SCL low to SDA output low valid           |      | 1                                     | 1   | μs   |
| t <sub>vdH(Data)</sub> | Valid-data time (low to high) <sup>(3)</sup>             | SCL low to SDA output high valid          |      | 0.6                                   | 0.6 | μs   |
| t <sub>vd(ack)</sub>   | Valid-data time of ACK condition                         | ACK signal from SCL low to SDA output low |      | 1                                     | 1   | μs   |
| C <sub>b</sub>         | I <sup>2</sup> C bus capacitive load                     |   | 400  |                                       | 400 | pF   |

- (1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH</sub> min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.  
(2) C<sub>b</sub> = total bus capacitance of one bus line in pF  
(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see Figure 10)

## Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see Figure 10)

| PARAMETER                      |                        | FROM<br>(INPUT)                                | TO<br>(OUTPUT) | MIN        | MAX | UNIT |
|--------------------------------|------------------------|--|----------------|------------|-----|------|
| t <sub>pd</sub> <sup>(1)</sup> | Propagation delay time | R <sub>ON</sub> = 20 Ω, C <sub>L</sub> = 15 pF | SDA or SCL     | SDn or SCn | 0.3 | ns   |
|                                |                        | R <sub>ON</sub> = 20 Ω, C <sub>L</sub> = 50 pF |                |            | 1   |      |

- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

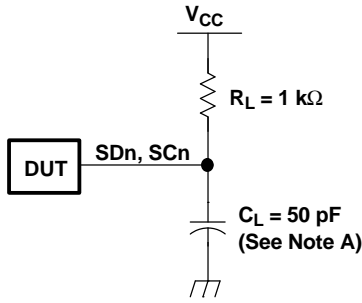
## Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

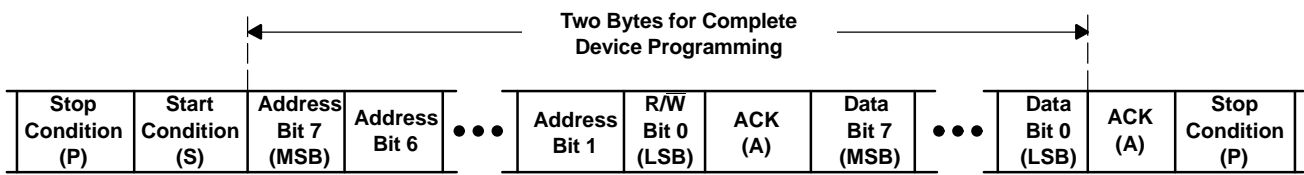
| PARAMETER                       |   | MIN | MAX | UNIT |
|---------------------------------|---|-----|-----|------|
| t <sub>wL</sub>                 | Pulse duration, $\overline{\text{RESET}}$ low         | 6   |     | ns   |
| t <sub>rst</sub> <sup>(1)</sup> | $\overline{\text{RESET}}$ time (SDA clear)            |     | 500 | ns   |
| t <sub>REC(STA)</sub>           | Recovery time from $\overline{\text{RESET}}$ to start | 0   |     | ns   |

- (1) t<sub>rst</sub> is the propagation delay measured from the time the  $\overline{\text{RESET}}$  pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t<sub>wL</sub>.

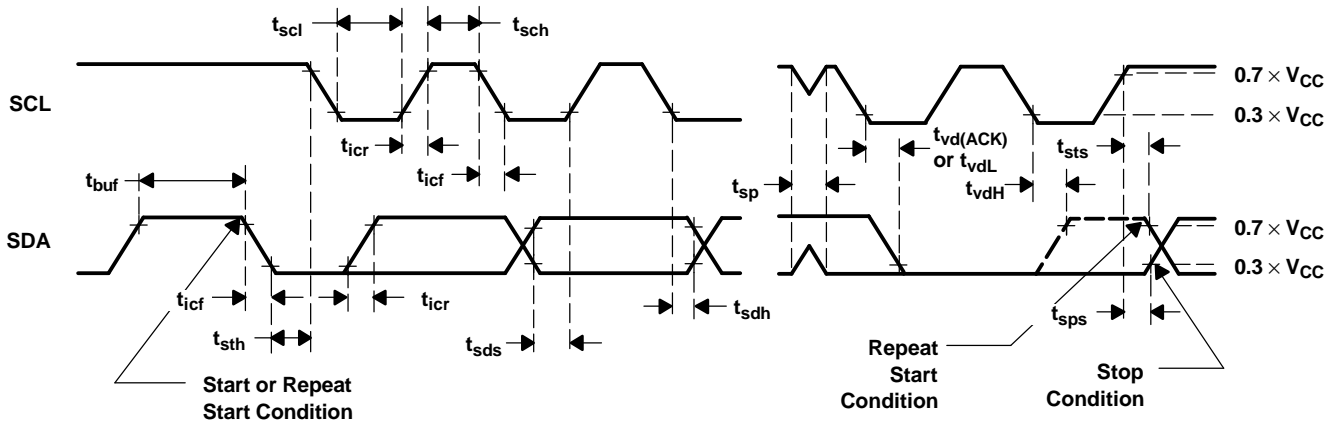
PARAMETER MEASUREMENT INFORMATION



I<sup>2</sup>C PORT LOAD CONFIGURATION



| BYTE | DESCRIPTION                    |
|------|--------------------------------|
| 1    | I <sup>2</sup> C address + R/W |
| 2    | Control register data          |



VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. The outputs are measured one at a time, with one transition per measurement.

Figure 10. I<sup>2</sup>C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

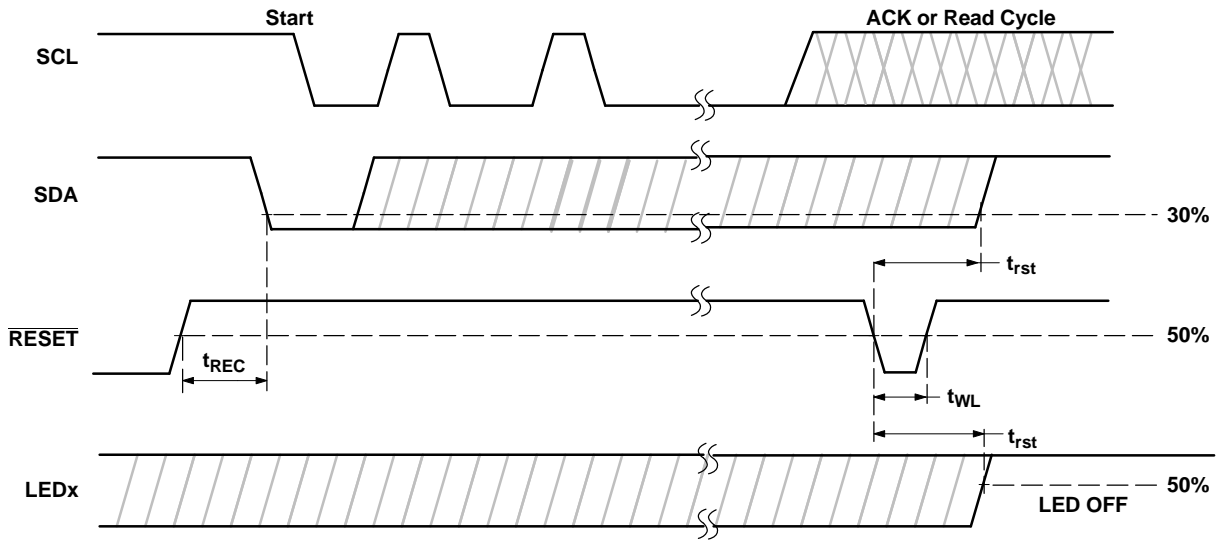
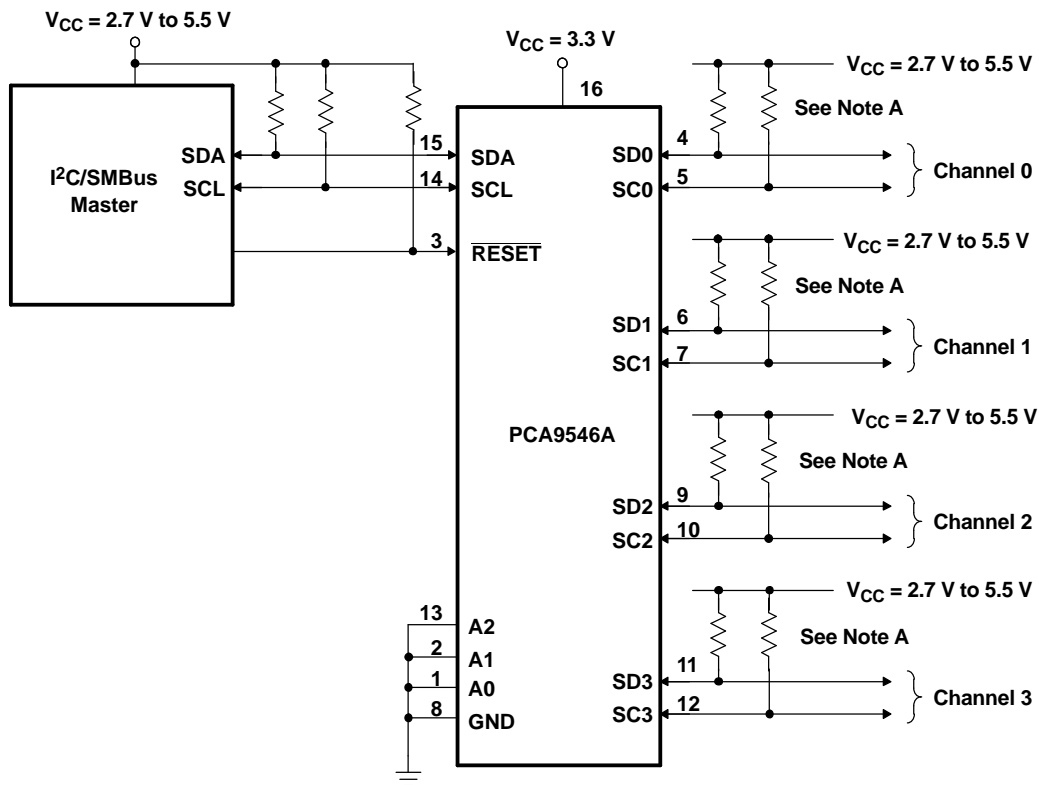


Figure 11. Reset Timing

**APPLICATION INFORMATION**

Figure 12 shows an application in which the PCA9546A can be used.



A. Pin numbers shown are for the DGV, DW, PW, and RGY packages.

**Figure 12. Typical Application**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type         | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|----------------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| PCA9546ADGVR     | ACTIVE                | TVSOP                | DGV             | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546ADGVT     | PREVIEW               | TVSOP                | DGV             | 20   | 250         | TBD                     | Call TI          | Call TI                      |
| PCA9546ADW       | ACTIVE                | SOIC                 | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546ADWR      | ACTIVE                | SOIC                 | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546ADWT      | PREVIEW               | SOIC                 | DW              | 16   | 250         | TBD                     | Call TI          | Call TI                      |
| PCA9546AGQNR     | PREVIEW               | BGA MICROSTAR JUNIOR | GQN             | 20   | 1000        | TBD                     | Call TI          | Call TI                      |
| PCA9546APW       | ACTIVE                | TSSOP                | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546APWE4     | ACTIVE                | TSSOP                | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546APWR      | ACTIVE                | TSSOP                | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546APWRE4    | ACTIVE                | TSSOP                | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546APWT      | ACTIVE                | TSSOP                | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546APWTE4    | ACTIVE                | TSSOP                | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCA9546ARGWR     | PREVIEW               | QFN                  | RGW             | 20   | 3000        | TBD                     | Call TI          | Call TI                      |
| PCA9546ARGYR     | ACTIVE                | QFN                  | RGY             | 16   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1YEAR           |
| PCA9546AZQNR     | PREVIEW               | BGA MICROSTAR JUNIOR | ZQN             | 20   | 1000        | TBD                     | Call TI          | Call TI                      |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

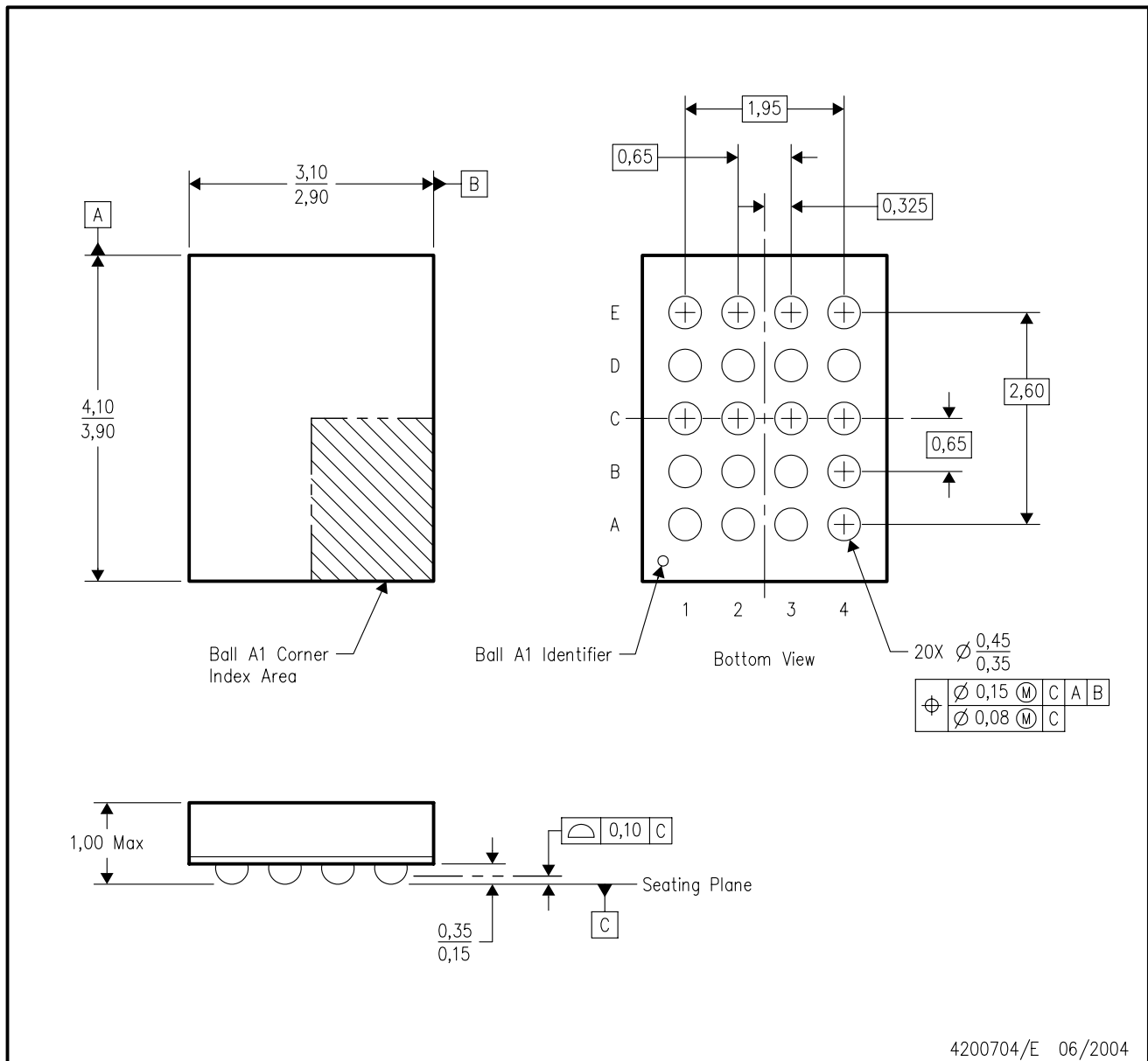
temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY

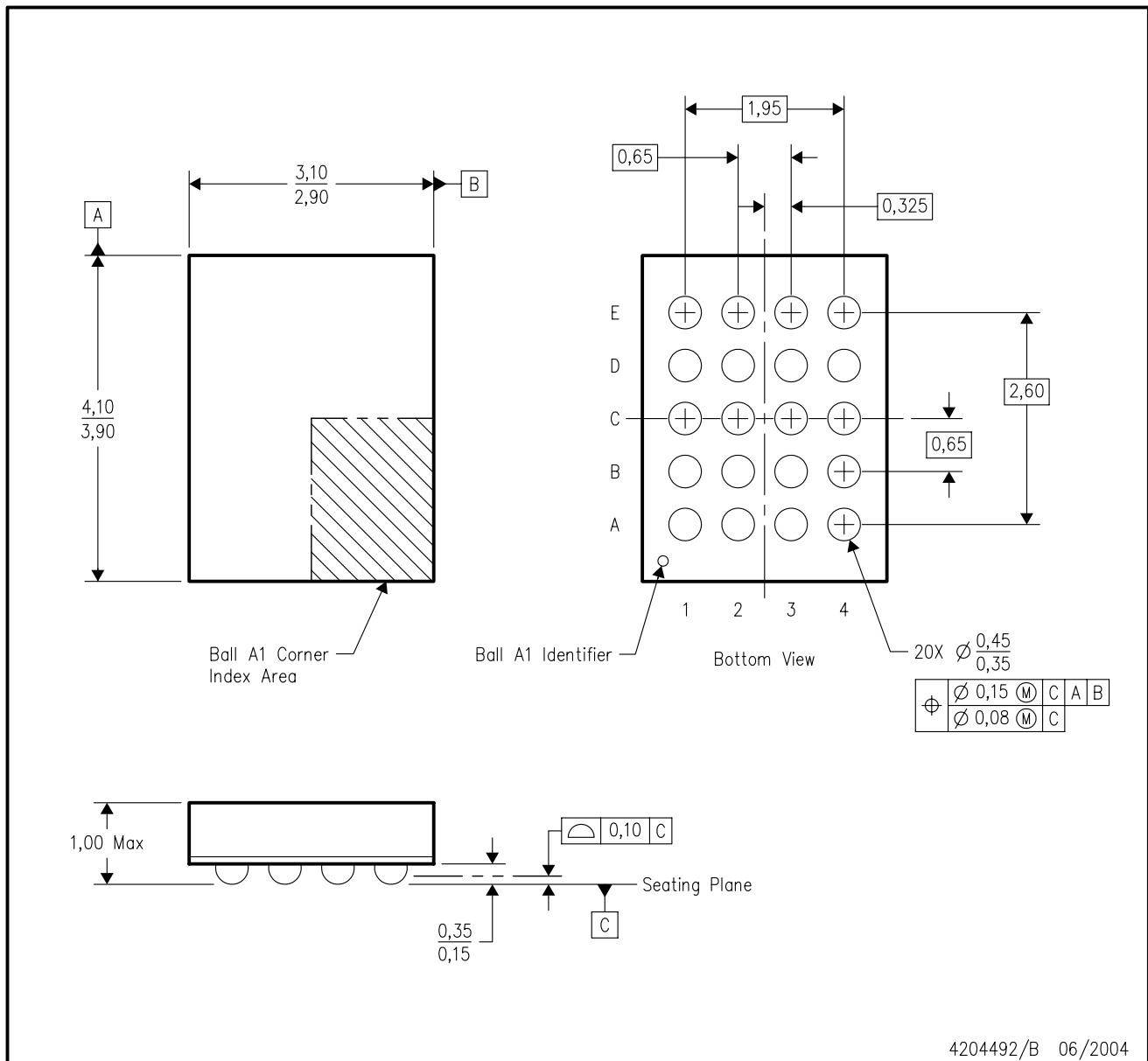


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BC.
  - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.



ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BC.
  - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

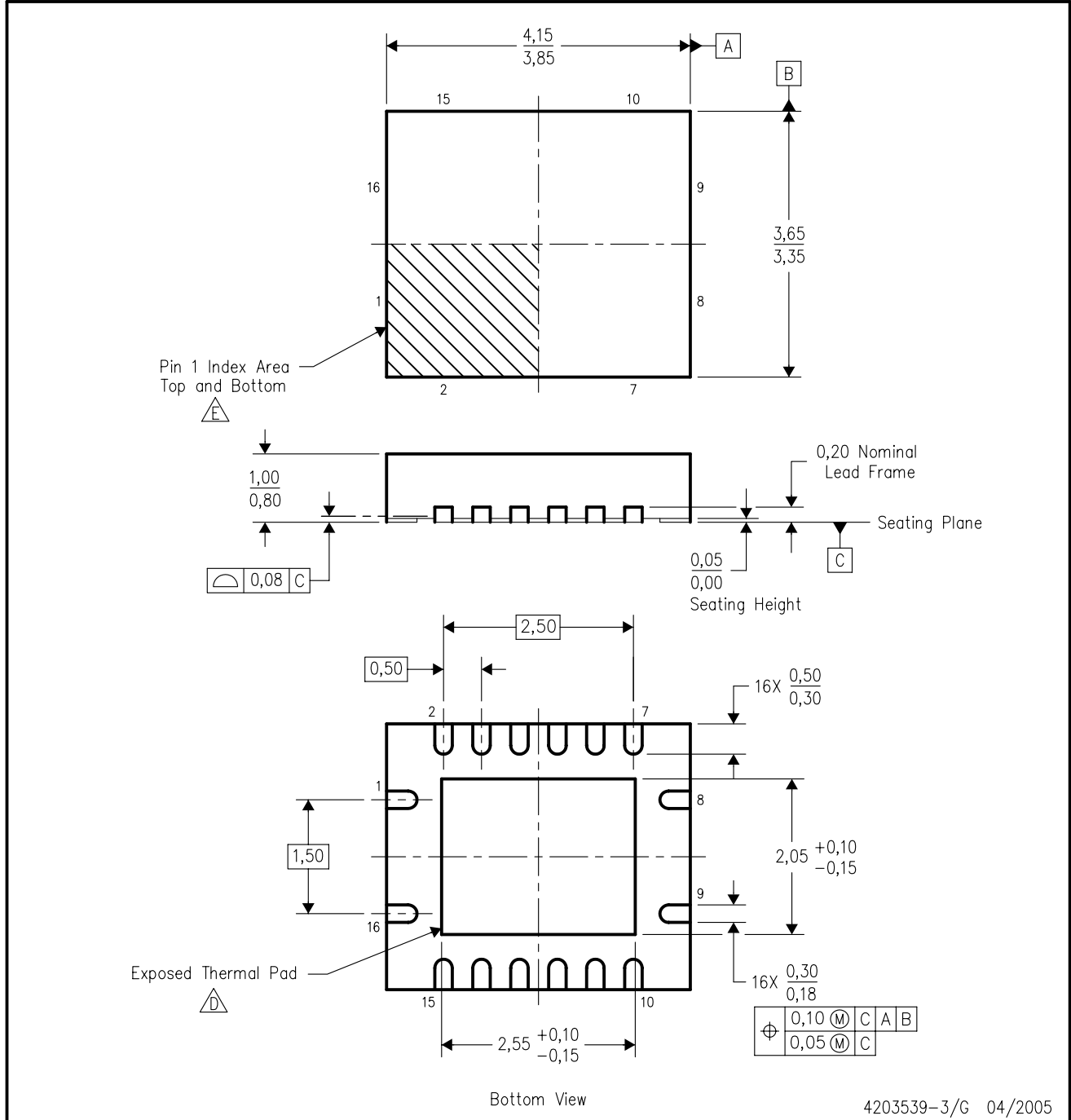


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK

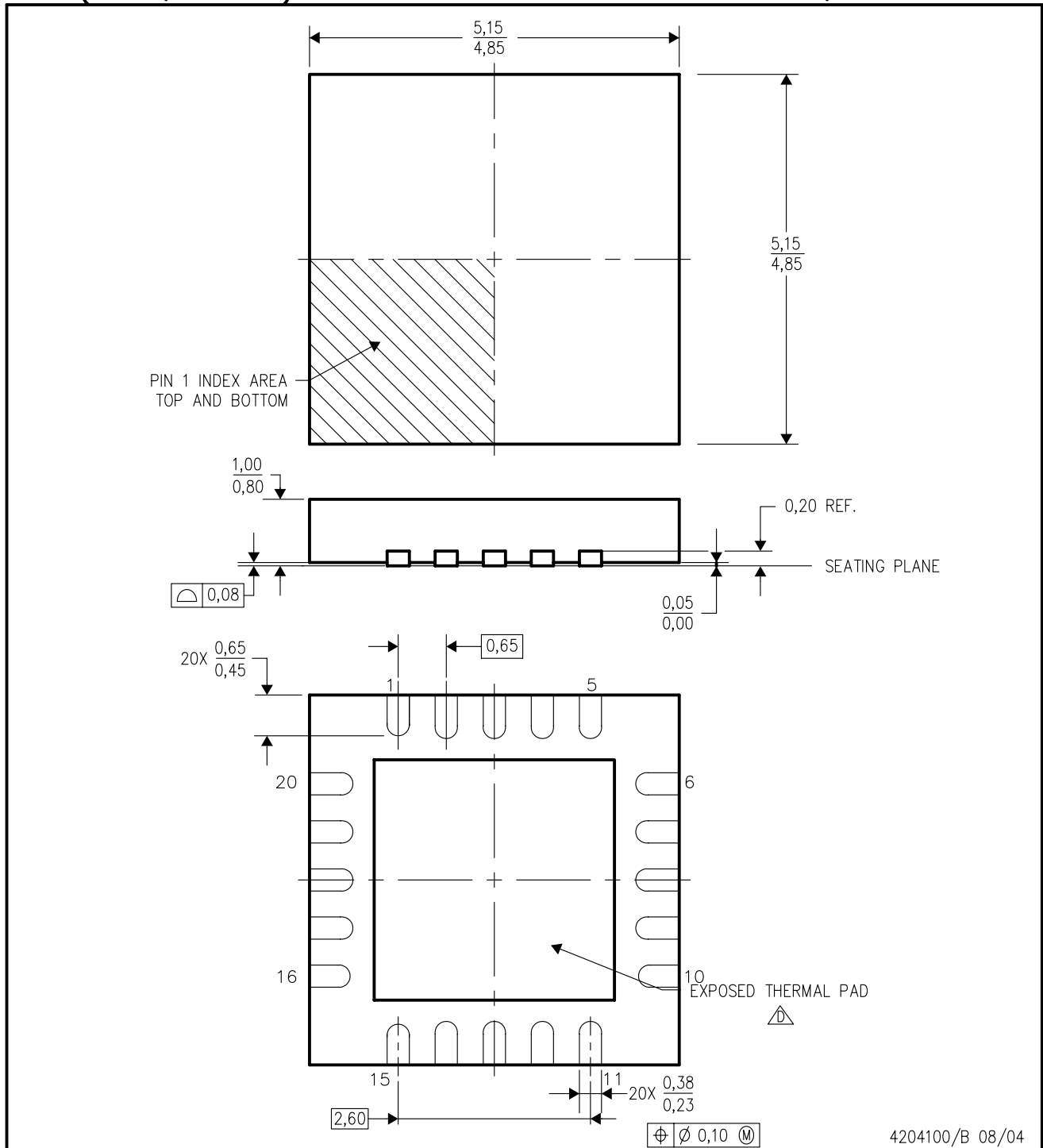


4203539-3/G 04/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BB.

RGW (S-PQFP-N20)

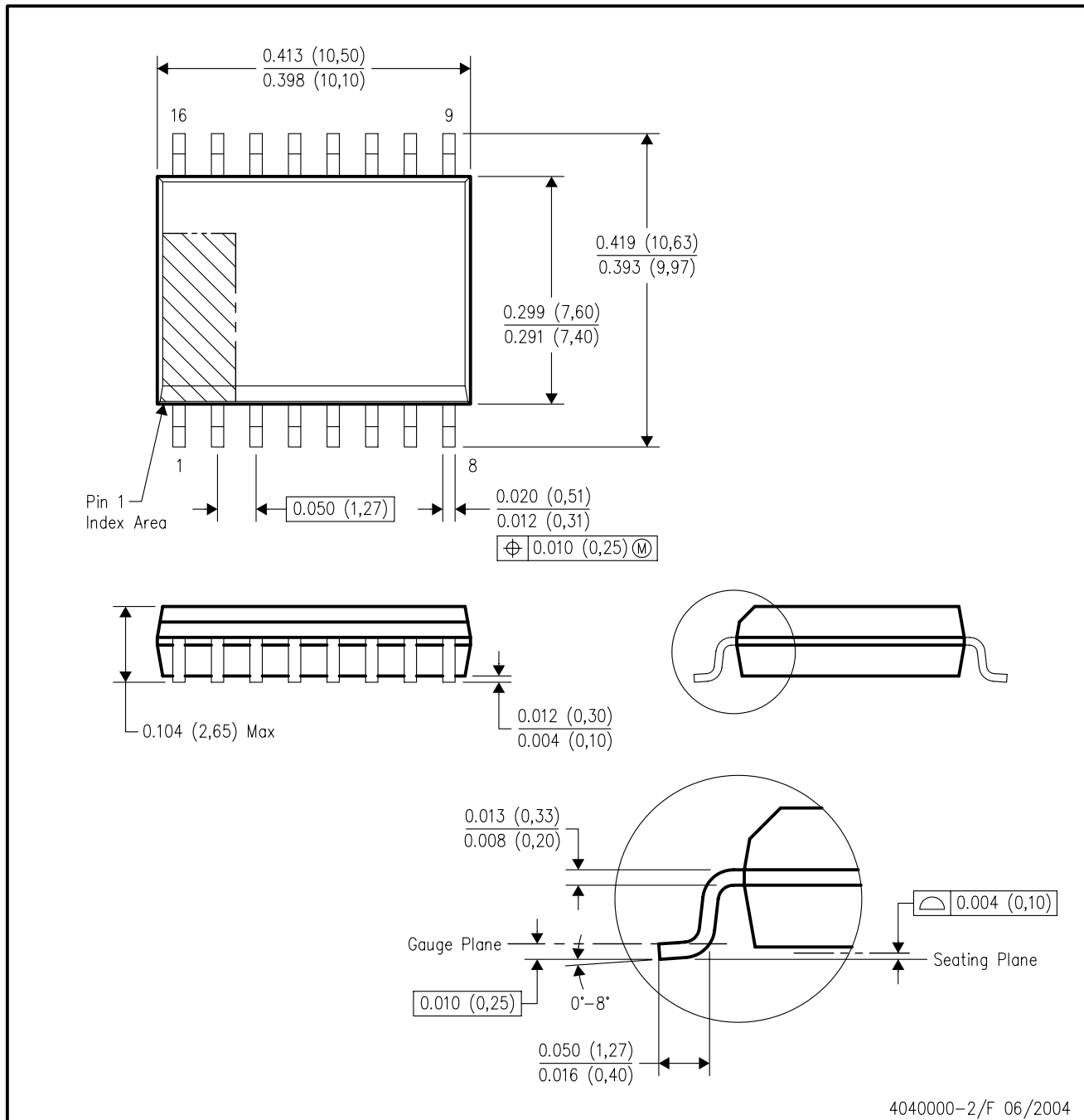
PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flat pack, No-leads (QFN) package configuration
  - △ The package thermal pad must be soldered to the board for thermal and mechanical performance.. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| <b>Products</b>  |  | <b>Applications</b> |  |
|------------------|--|---------------------|--|
| Amplifiers       | <a href="http://amplifier.ti.com">amplifier.ti.com</a>             | Audio               | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                   |
| Data Converters  | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     | Automotive          | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| DSP              | <a href="http://dsp.ti.com">dsp.ti.com</a>                         | Broadband           | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
| Interface        | <a href="http://interface.ti.com">interface.ti.com</a>             | Digital Control     | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Logic            | <a href="http://logic.ti.com">logic.ti.com</a>                     | Military            | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Power Mgmt       | <a href="http://power.ti.com">power.ti.com</a>                     | Optical Networking  | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Microcontrollers | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> | Security            | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
|                  |  | Telephony           | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
|                  |  | Video & Imaging     | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
|                  |  | Wireless            | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated