

# UT54ACTS08E

Radiation-Hardened  
Quadruple 2-Input AND Gates

December 2006

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## FEATURES

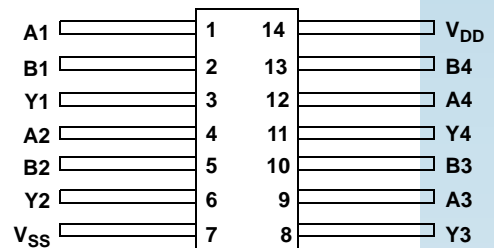
- 0.6µm CRH CMOS Process
  - Latchup immune
- High speed
- Low power consumption
- Wide operating power supply range of 3.0V to 5.5V
- Available QML Q or V processes
- 14-lead flatpack

## FUNCTION TABLE

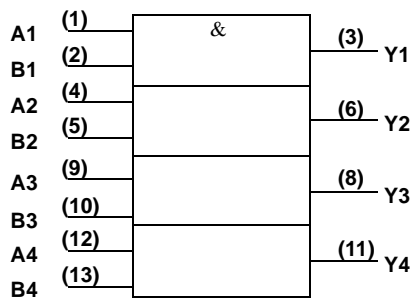
INPUT		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

## PINOUT

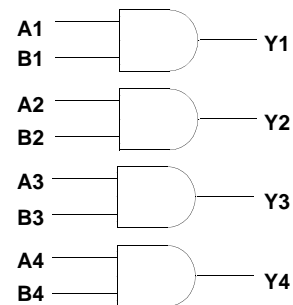
14-Pin Flatpack  
Top View



## LOGIC SYMBOL



## LOGIC DIAGRAM



### Note:

1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

## DESCRIPTION

The UT54ACTS08E is a quadruple two-input AND gate. The circuit performs the Boolean functions  $Y = A \cdot B$  or

$$Y = \overline{\overline{A} + \overline{B}} \text{ in positive logic.}$$

The devices are characterized over full military temperature range of -55°C to +125°C.

## RADIATION HARDNESS SPECIFICATIONS<sup>1</sup>

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold <sup>2</sup>	80	MeV-cm <sup>2</sup> /mg
SEL Threshold	120	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

**Notes:**

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0	V
V <sub>I/O</sub>	Voltage any pin	-.3 to V <sub>DD</sub> +.3	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
T <sub>LS</sub>	Lead temperature (soldering 5 seconds)	+300	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub>	Maximum power dissipation	1	W

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	3.0 to 5.5	V
V <sub>IN</sub>	Input voltage any pin	0 to V <sub>DD</sub>	V
T <sub>C</sub>	Temperature range	-55 to +125	°C

## DC ELECTRICAL CHARACTERISTICS FOR THE UT54ACTS08E<sup>7</sup>

( $V_{DD} = 3.0V$  to  $5.5V$ ;  $V_{SS} = 0V$ <sup>6</sup>;  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	Description	CONDITION	VDD	MIN	MAX	UNIT
$V_{IL}$	Low-level input voltage <sup>1</sup>		3.0V		0.8	V
			5.5V		0.8	
$V_{IH}$	High-level input voltage <sup>1</sup>		3.0V	2.0		V
			5.5V	2.75		
$I_{IN}$	Input leakage current	$V_{IN} = V_{DD}$ or $V_{SS}$	5.5V	-1	1	$\mu A$
$V_{OL}$	Low-level output voltage <sup>3</sup>	$I_{OL} = 6mA$	3.0V		0.4	V
		$I_{OL} = 8mA$	4.5V		0.4	V
$V_{OH}$	High-level output voltage <sup>3</sup>	$I_{OH} = -6mA$	3.0V	2.4		V
		$I_{OH} = -8mA$	4.5V	3.15		V
$I_{OS}$	Short-circuit output current <sup>2,4</sup>	$V_O = V_{DD}$ and $V_{SS}$	3.0V	-100	100	mA
			5.5V	-200	200	
$I_{OL}$	Low level output current <sup>10</sup>	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OL} = 0.4V$	3.0V	6		mA
			5.5V	8		
$I_{OH}$	High level output current <sup>10</sup>	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OH} = V^{DD}-0.4V$	3.0V		-6	mA
			5.5V		-8	
$P_{total}$	Power dissipation <sup>2, 8, ,9</sup>	$C_L = 50pF$	5.5V		1.8	mW/ MHz
			3.0V		0.72	
$I_{DDQ}$	Quiescent Supply Current	$V_{IN} = V_{DD}$ or $V_{SS}$	5.5V		10	$\mu A$
$\Delta I_{DDQ}$	Quiescent Supply Current Delta	For input under test $V_{IN} = V_{DD} - 2.1V$ For all other inputs $V_{IN} = V_{DD}$ or $V_{SS}$	5.5V		1.6	mA
$C_{IN}$	Input capacitance <sup>5</sup>	$f = 1MHz$	0V		15	pF
$C_{OUT}$	Output capacitance <sup>5</sup>	$f = 1MHz$	0V		15	pF

### Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH}(\min) + 20\%$ ,  $-0\%$ ;  $V_{IL} = V_{IL}(\max) + 0\%$ ,  $-50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH}(\min)$  and  $V_{IL}(\max)$ .
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-PRF-38535, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose  $\leq 1E6$  rads(Si) per MIL-STD-883 Method 1019 Condition A and section 3.11.2.
- Power does not include power contribution of any TTL output sink current
- Power dissipation specified per switching output.
- This value is guaranteed based on characterization data, but not tested.

**AC ELECTRICAL CHARACTERISTICS FOR THE UT54ACTS08E<sup>2</sup>**

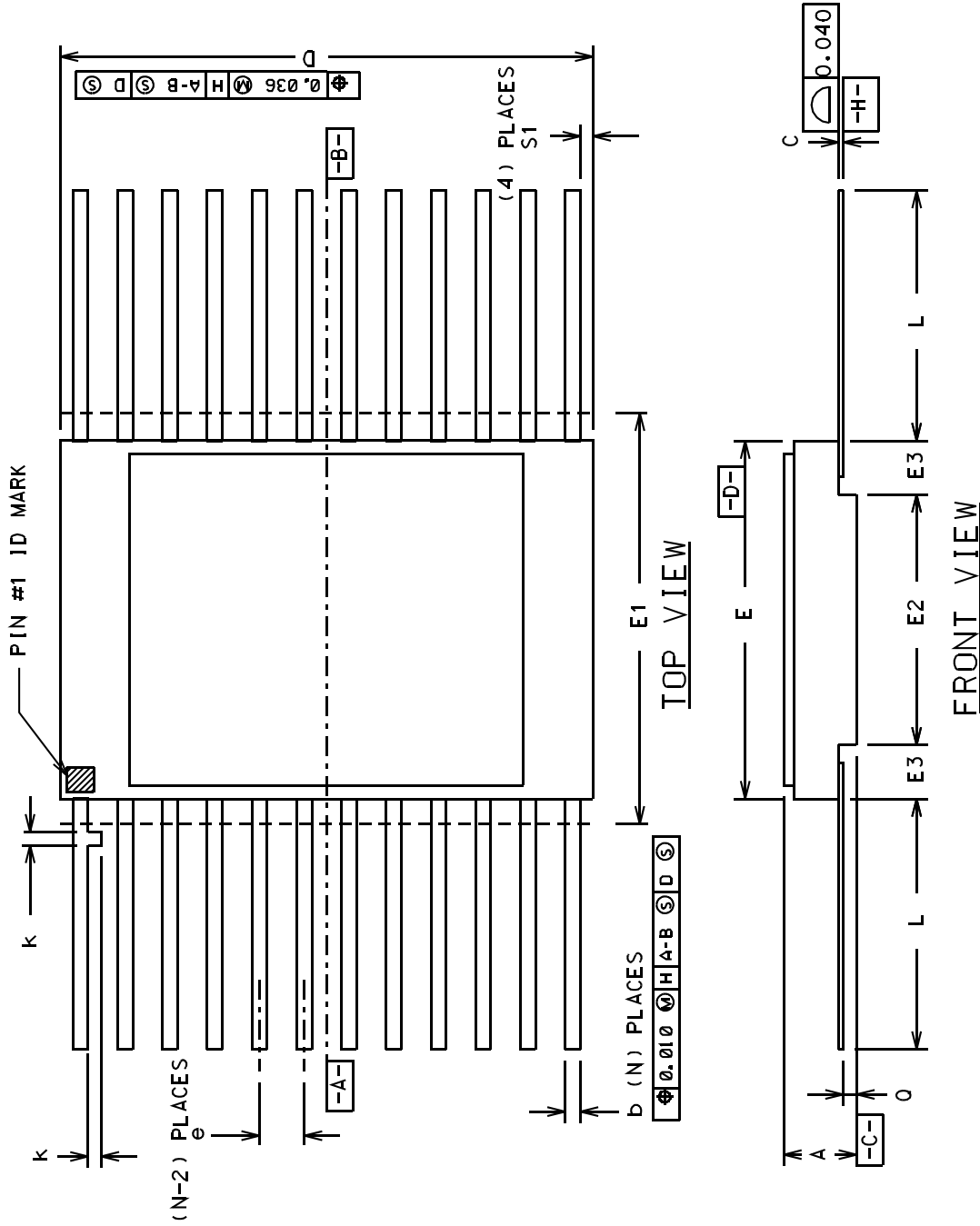
( $V_{DD} = 3.0V$  to  $5.5V$ ;  $V_{SS} = 0V$ <sup>1</sup>,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER		$V_{DD}$	MINIMUM	MAXIMUM	UNIT
$t_{PLH}$	Input to Yn	$C_L = 30pF$	3.0V & 3.6V	1	10	ns
			4.5V & 5.5V	1	6	
		$C_L = 50pF$	3.0V & 3.6V	1	14	ns
			4.5V & 5.5V	1	10	
$t_{PHL}$	Input to Yn	$C_L = 30pF$	3.0V & 3.6V	1	13	ns
			4.5V & 5.5V	1	9	
		$C_L = 50pF$	3.0V & 3.6V	1	17	ns
			4.5V & 5.5V	1	13	

**Notes:**

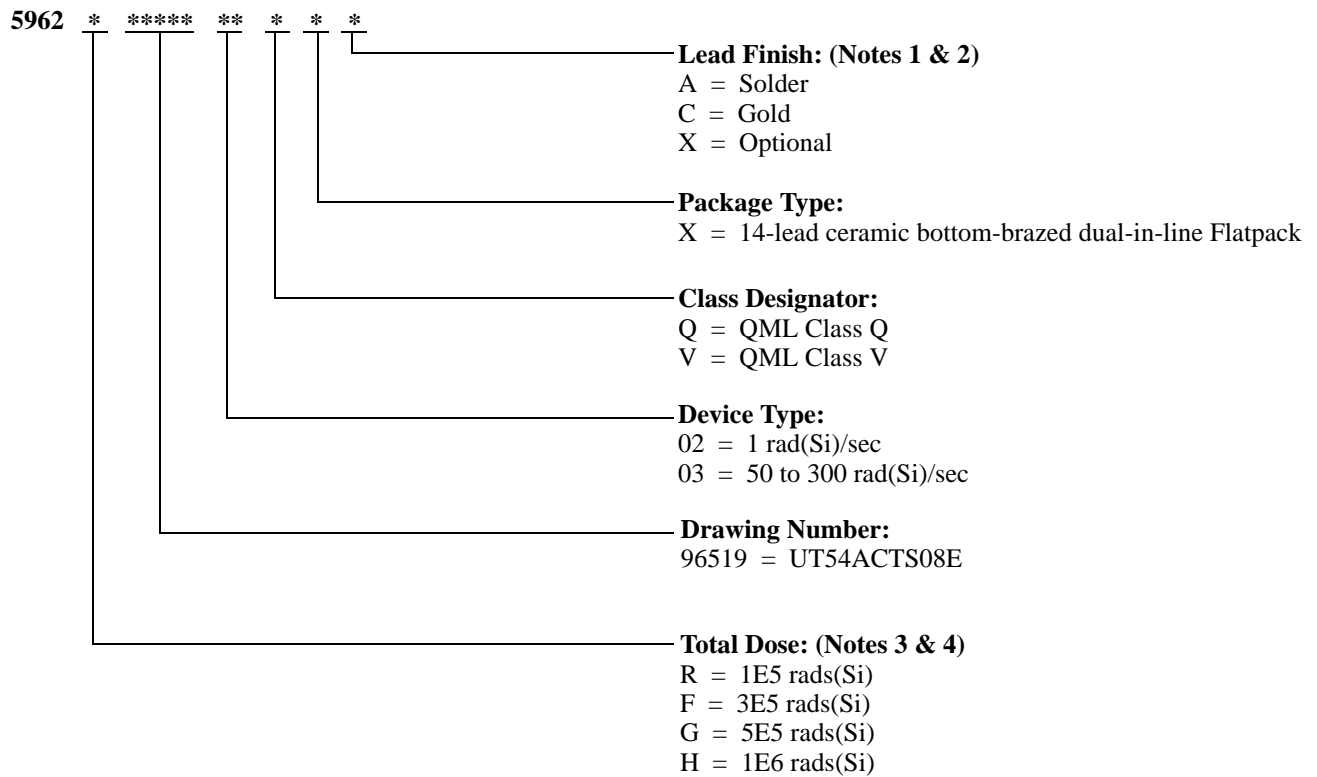
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose  $\leq 1E6$  rads(Si) per MIL-STD-883 Method 1019 Condition A and section 3.11.2.

Packaging



PKG CONFIG	LEAD COUNT	MLL-STD 1835 DMG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	0	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	0.130 -----	0.030 -----	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	0.130 -----	0.030 -----	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	0.130 -----	0.030 -----	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000

**Ordering Information: UT54ACTS08E: SMD**



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

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