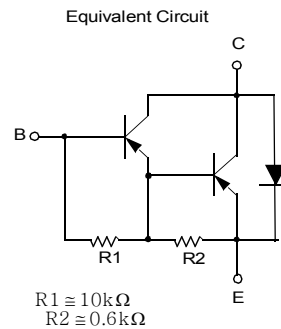
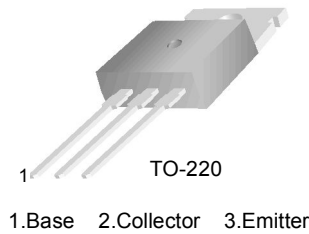


# TIP115/TIP116/TIP117

## PNP Epitaxial Silicon Darlington Transistor

- Monolithic Construction With Built In Base-Emitter Shunt Resistors
- High DC Current Gain :  $h_{FE}=1000$  @  $V_{CE}=-4V$ ,  $I_C=-1A$  (Min.)
- Low Collector-Emitter Saturation Voltage
- Industrial Use
- Complementary to TIP110/111/112



### Absolute Maximum Ratings\* $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{CBO}$	Collector-Base Voltage : TIP115	- 60	V
	: TIP116	- 80	V
	: TIP117	- 100	V
$V_{CEO}$	Collector-Emitter Voltage : TIP115	- 60	V
	: TIP116	- 80	V
	: TIP117	- 100	V
$V_{EBO}$	Emitter-Base Voltage	- 5	V
$I_C$	Collector Current (DC)	- 2	A
$I_{CP}$	Collector Current (Pulse)	- 4	A
$I_B$	Base Current (DC)	- 50	mA
$P_C$	Collector Dissipation ( $T_a=25^\circ\text{C}$ )	2	W
	Collector Dissipation ( $T_C=25^\circ\text{C}$ )	50	W
$T_J$	Junction Temperature	150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	- 65 ~ 150	$^\circ\text{C}$

\* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

**Electrical Characteristics\***  $T_a=25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage : TIP115 : TIP116 : TIP117	$I_C = -30\text{mA}, I_B = 0$	-60 -80 -100			V V V
$I_{CEO}$	Collector Cut-off Current : TIP115 : TIP116 : TIP117	$V_{CE} = -30\text{V}, I_B = 0$ $V_{CE} = -40\text{V}, I_B = 0$ $V_{CE} = -50\text{V}, I_B = 0$			-2 -2 -2	mA mA mA
$I_{CBO}$	Collector Cut-off Current : TIP115 : TIP116 : TIP117	$V_{CB} = -60\text{V}, I_E = 0$ $V_{CB} = -80\text{V}, I_E = 0$ $V_{CB} = -100\text{V}, I_E = 0$			-1 -1 -1	mA mA mA
$I_{EBO}$	Emitter Cut-off Current	$V_{BE} = -5\text{V}, I_C = 0$			-2	mA
$h_{FE}$	DC Current Gain	$V_{CE} = -4\text{V}, I_C = -1\text{A}$ $V_{CE} = -4\text{V}, I_C = -2\text{A}$	1000 500			
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = -2\text{A}, I_B = -8\text{mA}$			-2.5	V
$V_{BE(on)}$	Base-Emitter On Voltage	$V_{CE} = -4\text{V}, I_C = -2\text{A}$			-2.8	V
$C_{ob}$	Output Capacitance	$V_{CB} = -10\text{V}, I_E = 0, f = 0.1\text{MHz}$			200	pF

\* Pulse Test: Pulse Width $\leq 300\mu\text{s}$ , Duty Cycle $\leq 2\%$

# Typical Characteristics

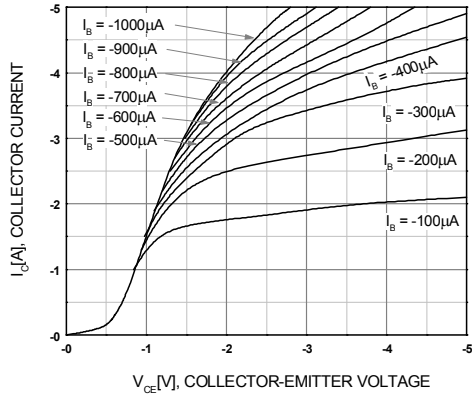


Figure 1. Static Characteristic

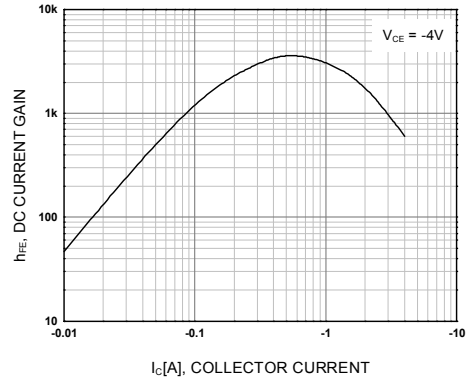


Figure 2. DC current Gain

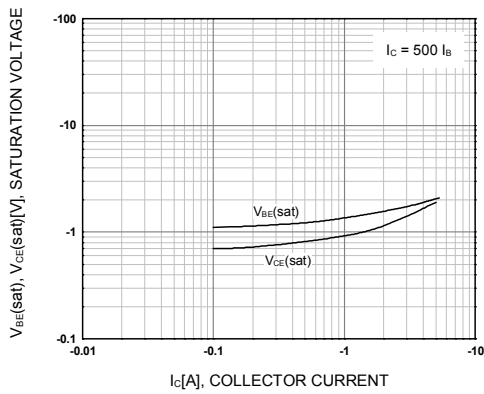


Figure 3. Collector-Emitter Saturation Voltage  
Base-Emitter Saturation Voltage

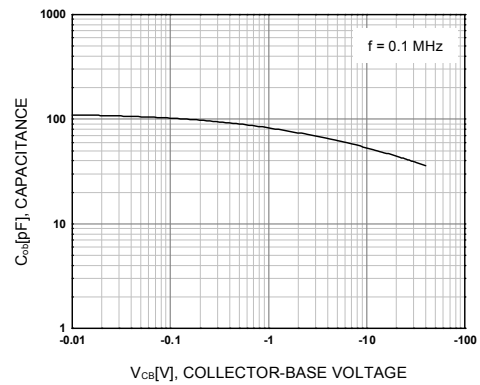


Figure 4. Collector Output Capacitance

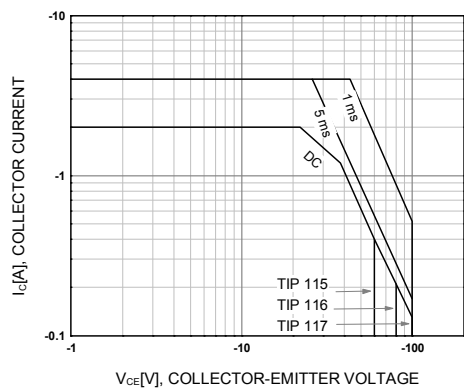


Figure 5. Safe Operating Area

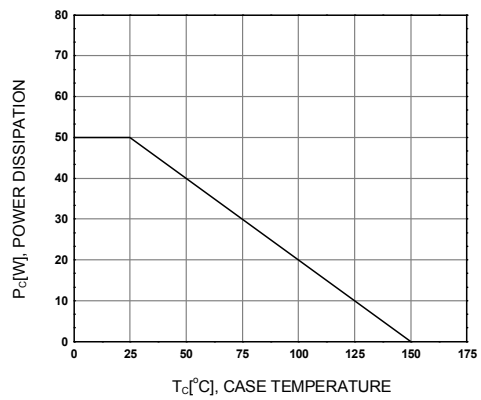
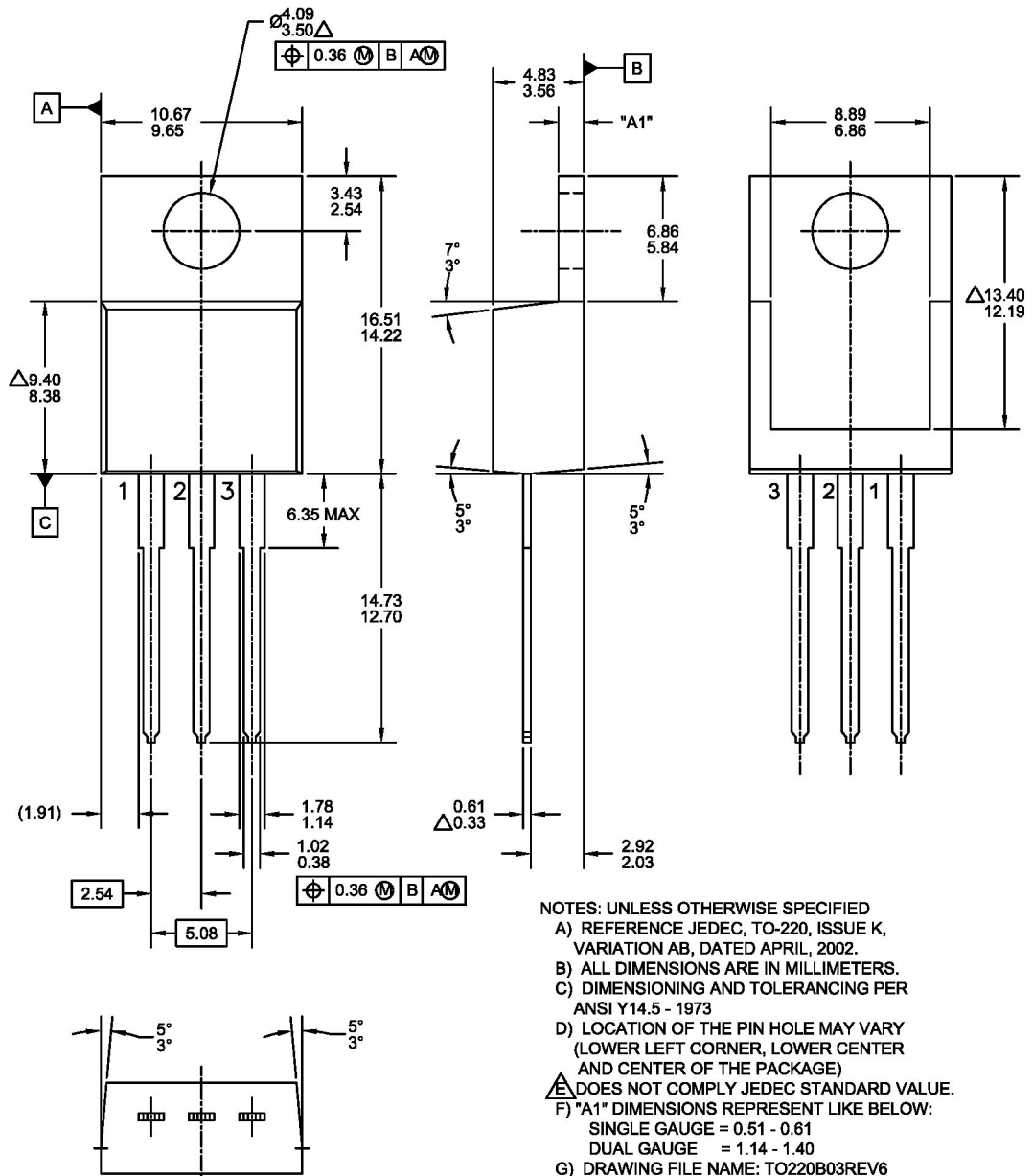


Figure 6. Power Derating

Mechanical Dimensions

TO220




- NOTES: UNLESS OTHERWISE SPECIFIED
- A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
  - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
  - $\triangle$  DOES NOT COMPLY JEDEC STANDARD VALUE.
  - F) "A1" DIMENSIONS REPRESENT LIKE BELOW:  
 SINGLE GAUGE = 0.51 - 0.61  
 DUAL GAUGE = 1.14 - 1.40
  - G) DRAWING FILE NAME: TO220B03REV6



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