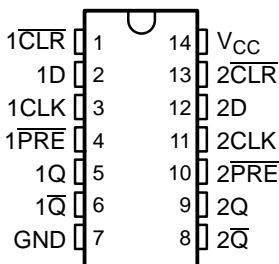


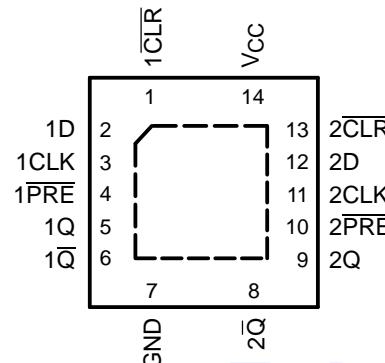
FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

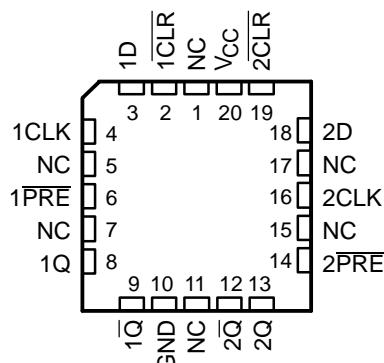
SN54LVC74A . . . J OR W PACKAGE
SN74LVC74A . . . D, DB, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC74A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC74A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC74A dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC74A dual positive-edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC74ARGYR
	SOIC – D	Tube of 50	SN74LVC74AD
		Reel of 2500	SN74LVC74ADR
		Reel of 250	SN74LVC74ADT
	SOP – NS	Reel of 2000	SN74LVC74ANSR
	SSOP – DB	Reel of 2000	SN74LVC74ADBR
	TSSOP – PW	Tube of 90	SN74LVC74APW
		Reel of 2000	SN74LVC74APWR
		Reel of 250	SN74LVC74APWT
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC74AJ
	CFP – W	Tube of 150	SNJ54LVC74AW
	LCCC – FK	Tube of 55	SNJ54LVC74AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVC74A, SN74LVC74A
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH CLEAR AND PRESET

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 **TEXAS
INSTRUMENTS**
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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

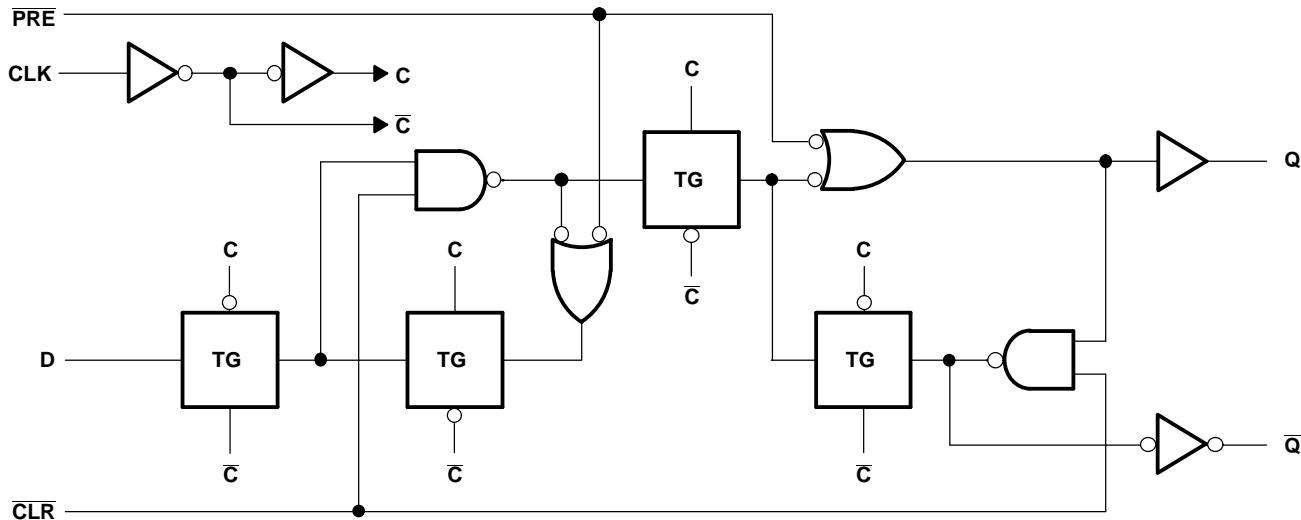
The data I/Os and control inputs are overvoltage tolerant. This feature allows the use of these devices for down-translation in a mixed-voltage environment.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	$H^{(1)}$	$H^{(1)}$
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\overline{Q}_0

- (1) This configuration is nonstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

**LOGIC DIAGRAM, EACH FLIP-FLOP
(POSITIVE LOGIC)**



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Output voltage range ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50 mA
I _{OK}	Output clamp current	V _O < 0		-50 mA
I _O	Continuous output current			±50 mA
	Continuous current through V _{CC} or GND			±100 mA
θ _{JA}	Package thermal impedance	D package ⁽⁴⁾		86 °C/W
		DB package ⁽⁴⁾		96
		NS package ⁽⁴⁾		76
		PW package ⁽⁴⁾		113
		RGY package ⁽⁵⁾		47
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

		SN54LVC74A		SN74LVC74A		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.65 × V _{CC}		V	
		V _{CC} = 2.3 V to 2.7 V		1.7			
		V _{CC} = 2.7 V to 3.6 V	2	2			
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		V	
		V _{CC} = 2.3 V to 2.7 V		0.7			
		V _{CC} = 2.7 V to 3.6 V	0.8	0.8			
V _I	Input voltage	0	5.5	0	5.5	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V			-4	mA	
		V _{CC} = 2.3 V			-8		
		V _{CC} = 2.7 V	-12	-12			
		V _{CC} = 3 V	-24	-24			
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4	mA	
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V	12	12			
		V _{CC} = 3 V	24	24			
Δt/Δv	Input transition rise or fall rate		10		10	ns/V	
T _A	Operating free-air temperature	-55	125	-40	85	°C	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS
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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC74A			SN74LVC74A			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = -100 µA	1.65 V to 3.6 V			V _{CC} – 0.2				V
		2.7 V to 3.6 V	V _{CC} – 0.2						
	I _{OH} = -4 mA	1.65 V			1.2				
	I _{OH} = -8 mA	2.3 V			1.7				
	I _{OH} = -12 mA	2.7 V	2.2		2.2				
		3 V	2.4		2.4				
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V			0.2				V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V			0.45				
	I _{OL} = 8 mA	2.3 V			0.7				
	I _{OL} = 12 mA	2.7 V	0.4		0.4				
	I _{OL} = 24 mA	3 V	0.55		0.55				
I _I	V _I = 5.5 V or GND	3.6 V	±5		±5				µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		10				µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		500				µA
C _i	V _I = V _{CC} or GND	3.3 V	5		5				pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

				SN54LVC74A		UNIT
				V _{CC} = 2.7 V	V _{CC} = 3.3 V ± 0.3 V	
				MIN	MAX	
f _{clock}	Clock frequency			83	100	MHz
t _w	Pulse duration	PRE or CLR low	3.3	3.3		ns
		CLK high or low	3.3	3.3		
t _{su}	Setup time before CLK↑	Data	3.4	3		ns
		PRE or CLR inactive	2.2	2		
t _h	Hold time, data after CLK↑		1	1		ns

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		SN74LVC74A								UNIT	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency		83		83		83		150	MHz	
t_w	Pulse duration	PRE or \overline{CLR} low	4.1		3.3		3.3		3.3	ns	
		CLK high or low	4.1		3.3		3.3		3.3		
t_{su}	Setup time before CLK^\uparrow	Data	3.6		2.3		3.4		3	ns	
		PRE or \overline{CLR} inactive	2.7		1.9		2.2		2		
t_h	Hold time, data after CLK^\uparrow		1		1		1		0	ns	

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC74A				UNIT	
			$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
			MIN	MAX	MIN	MAX		
f_{max}				83		100	MHz	
t_{pd}	CLK	Q or \overline{Q}			6	1	5.2	ns
	PRE or \overline{CLR}				6.4	1	5.4	

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC74A						UNIT		
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 2.7 \text{ V}$				
			MIN	MAX	MIN	MAX	MIN	MAX			
f_{max}			83		83		83		150	MHz	
t_{pd}	CLK	Q or \overline{Q}	1	7.1	1	4.4	1	6	1	5.2	ns
	PRE or \overline{CLR}		1	6.9	1	4.6	1	6.4	1	5.4	
$t_{sk(o)}$									1	ns	

Operating Characteristics

$T_A = 25^\circ\text{C}$

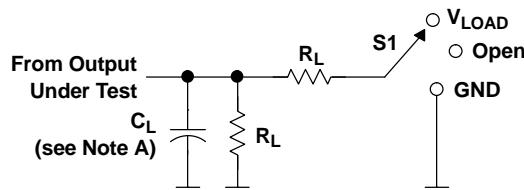
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per flip-flop	$f = 10 \text{ MHz}$	24	24	26 pF

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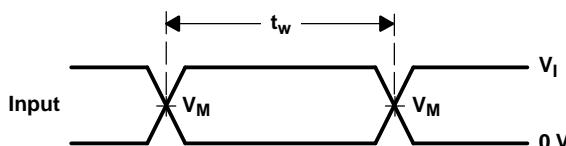
PARAMETER MEASUREMENT INFORMATION



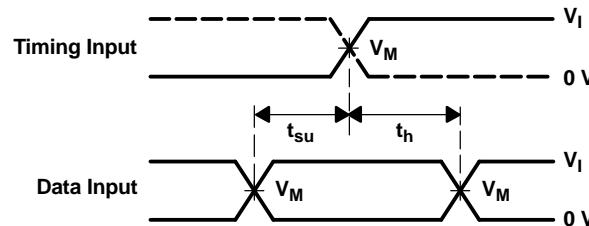
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

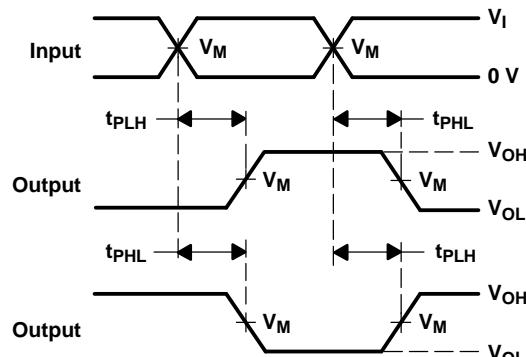
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



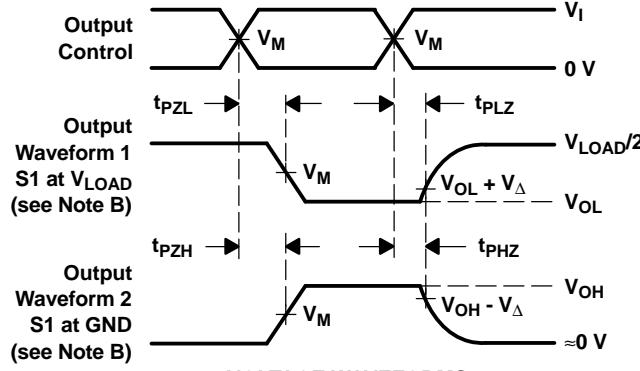
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PZH} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9761601Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9761601QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9761601QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9761601VCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9761601VDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN74LVC74AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LVC74ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ADTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LVC74APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC74ARGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
no Sb/Br)								
SN74LVC74ARGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SNJ54LVC74AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LVC74AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LVC74AW	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

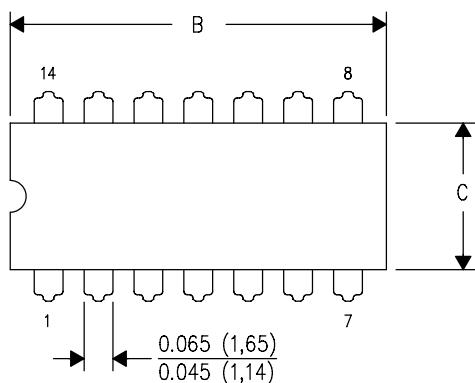
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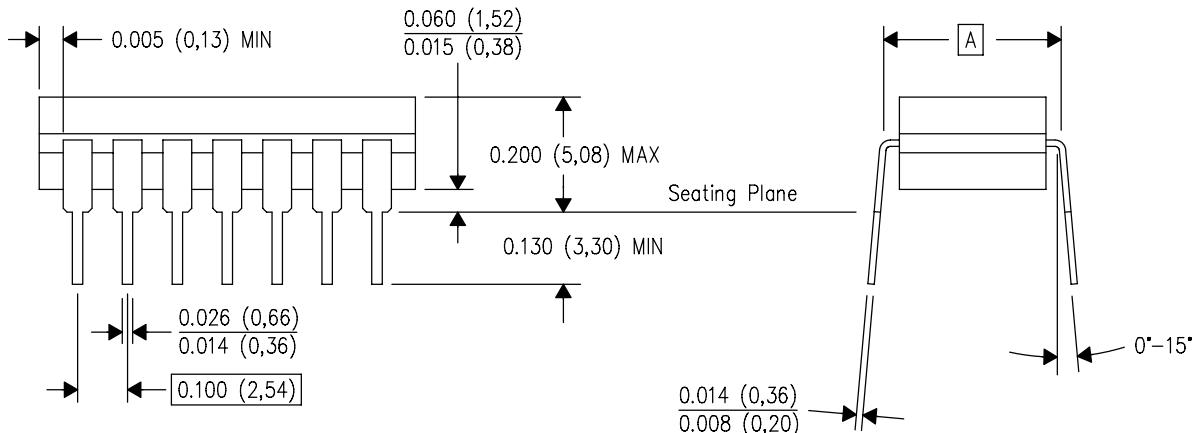
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

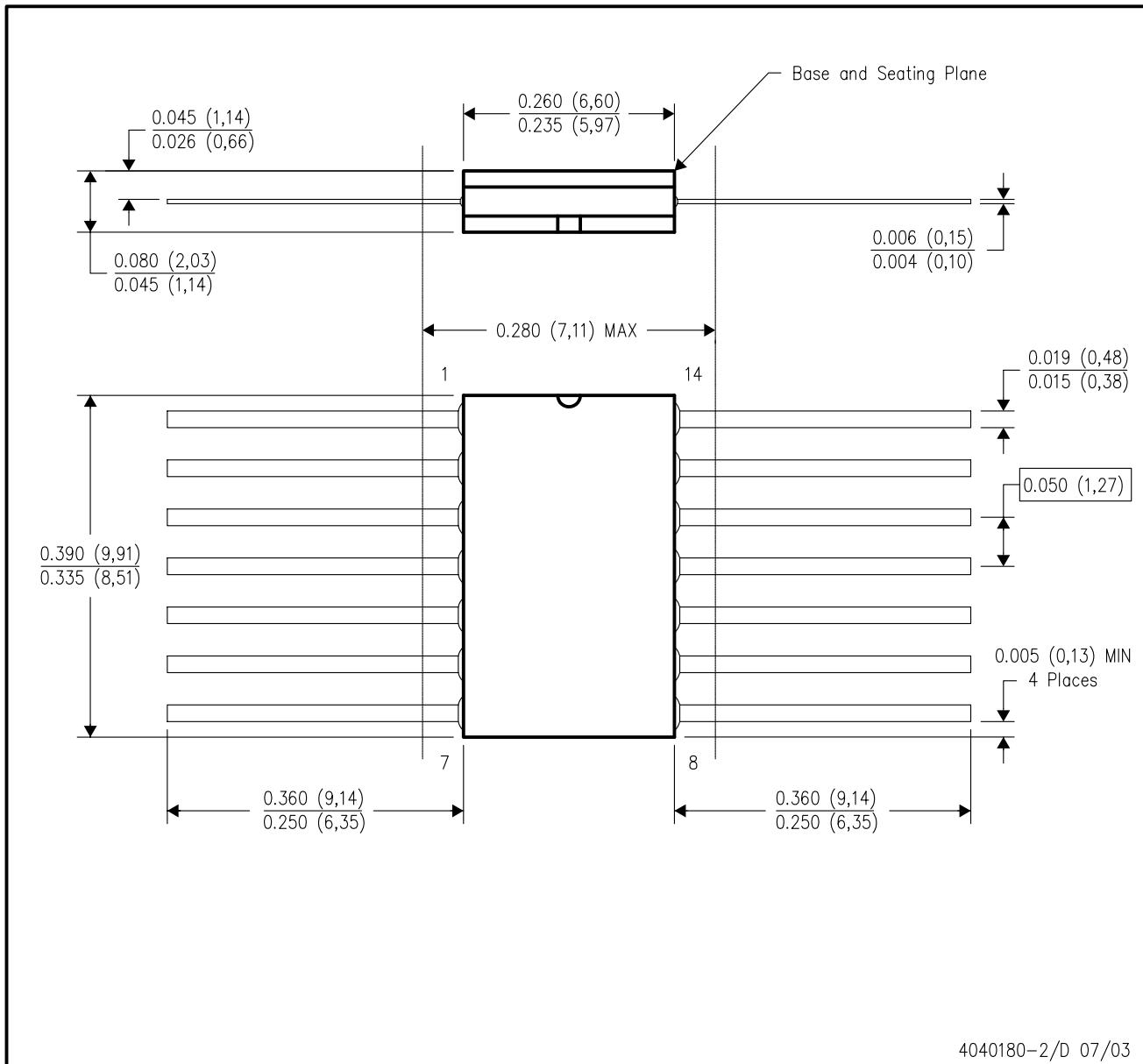


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

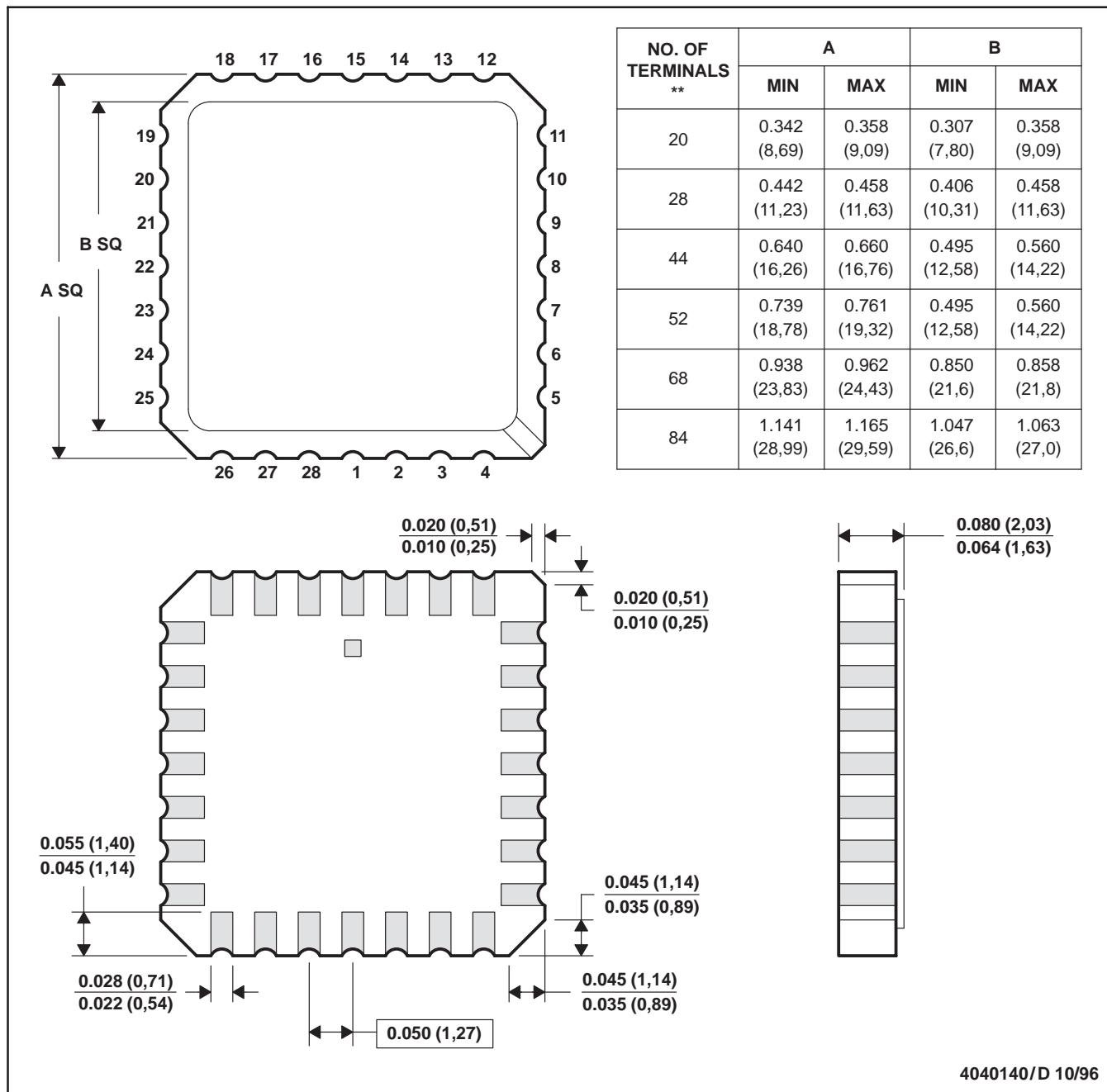


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL-STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

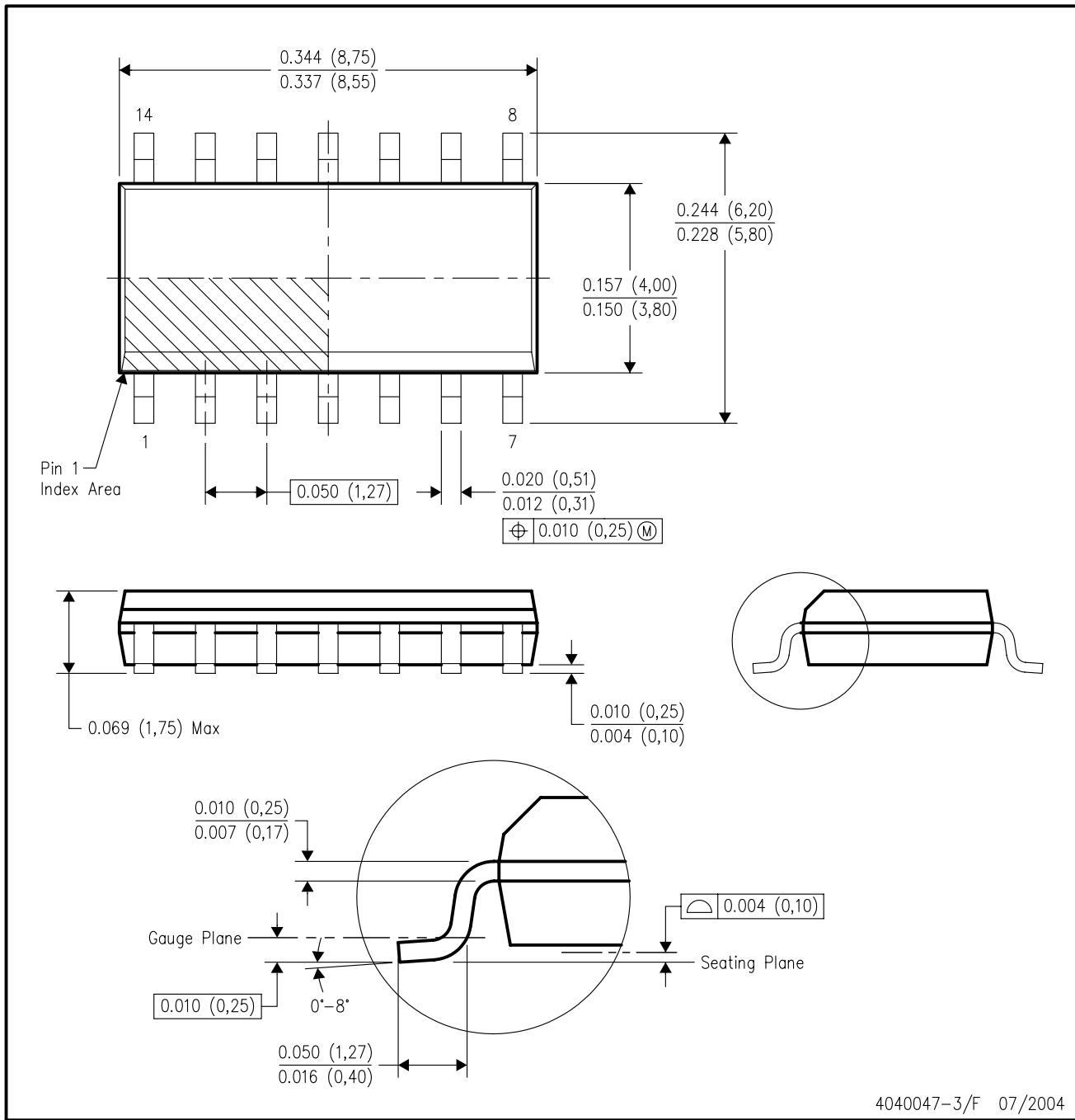
D. The terminals are gold plated.

E. Falls within JEDEC MS-004

4040140/D 10/96

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



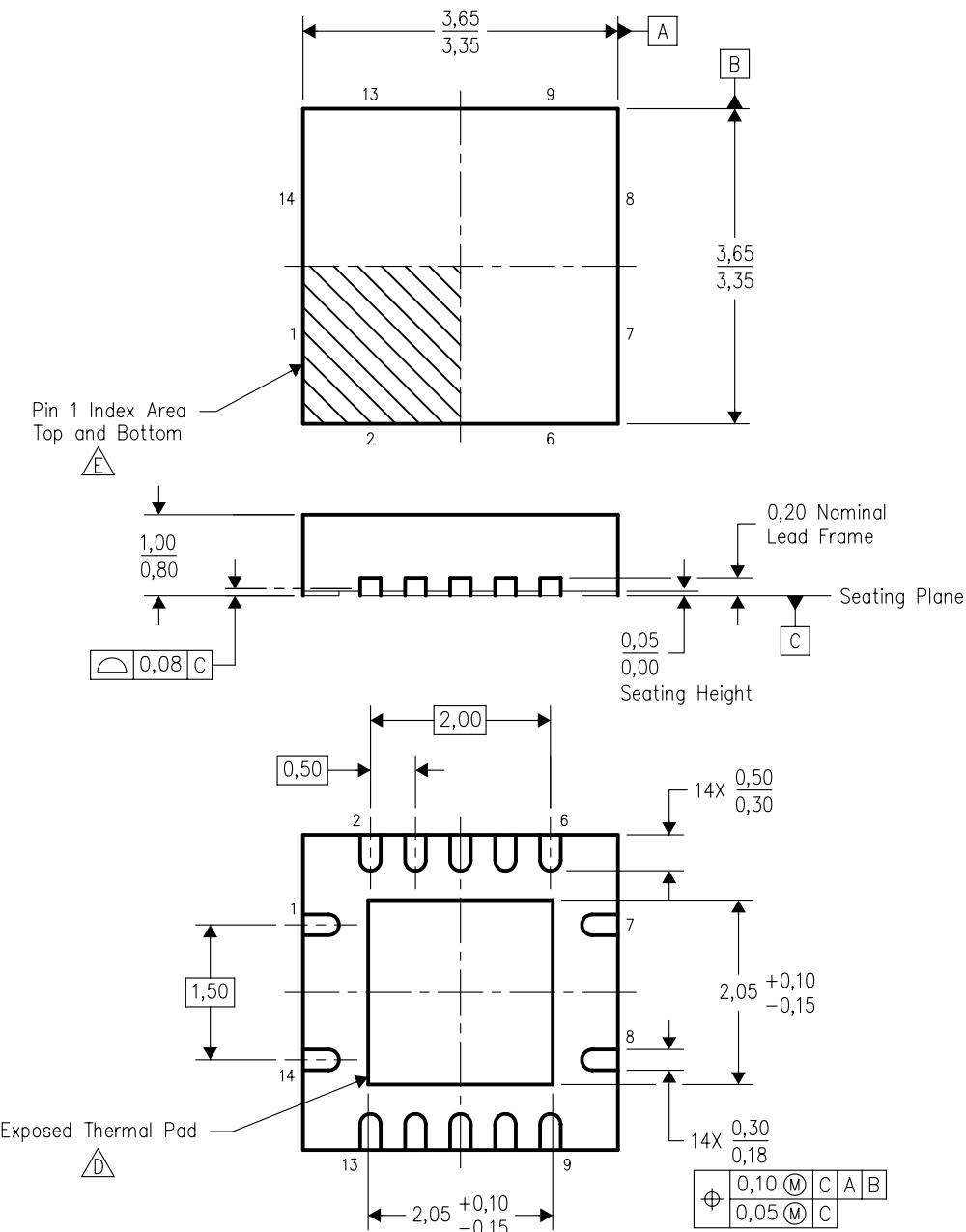
4040047-3/F 07/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



Bottom View

4203539-2/G 04/2005

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

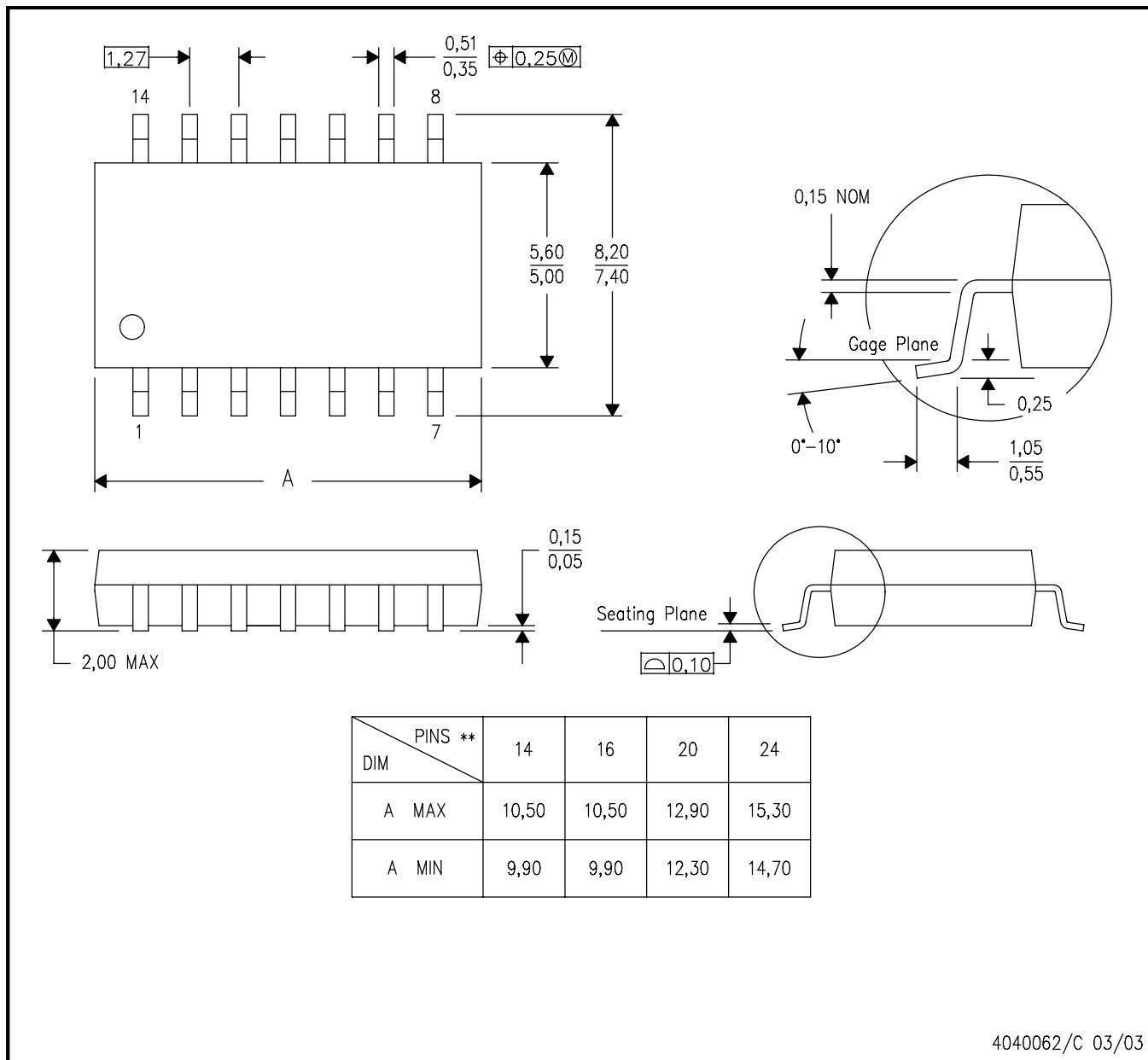
F. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

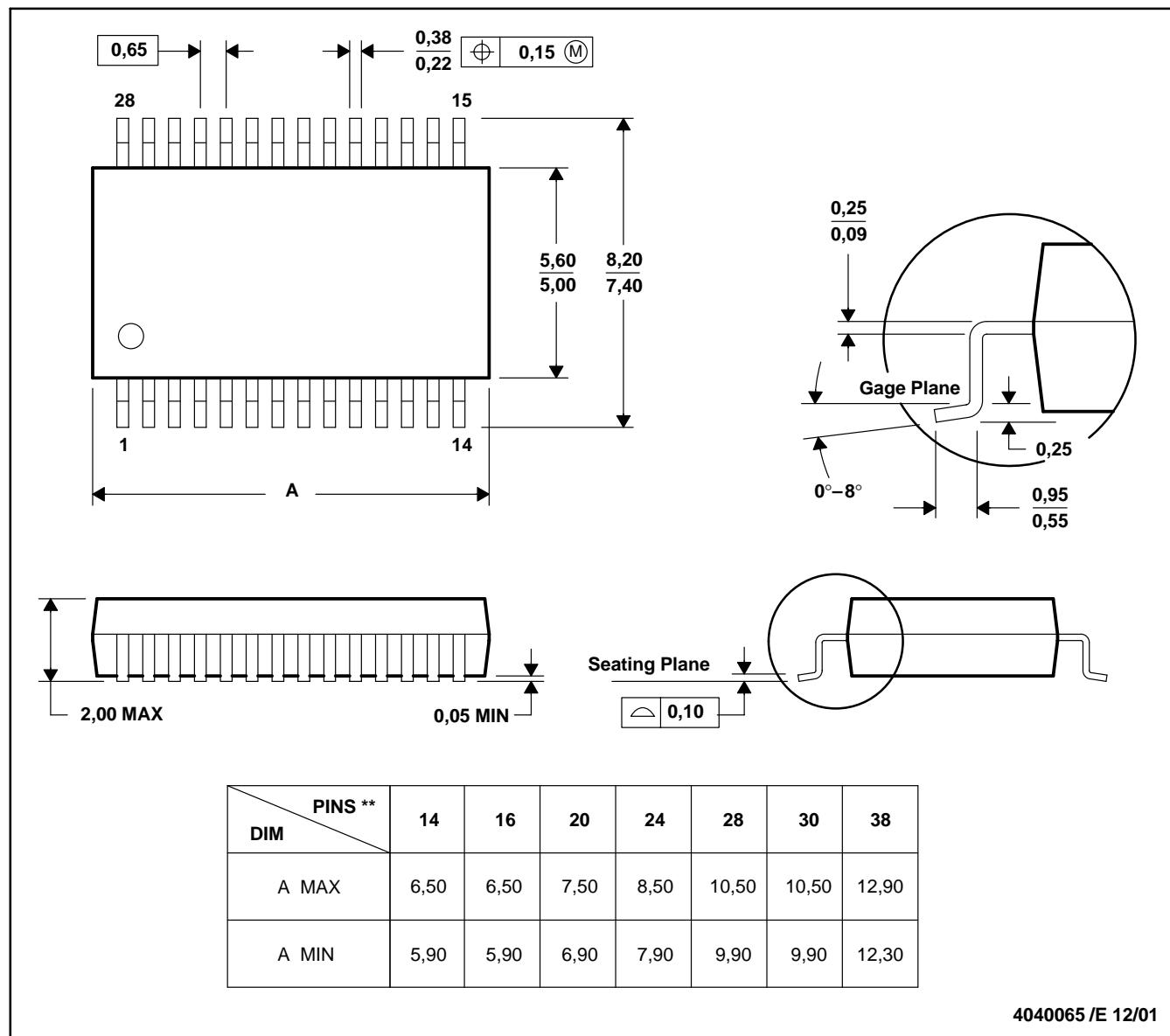


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

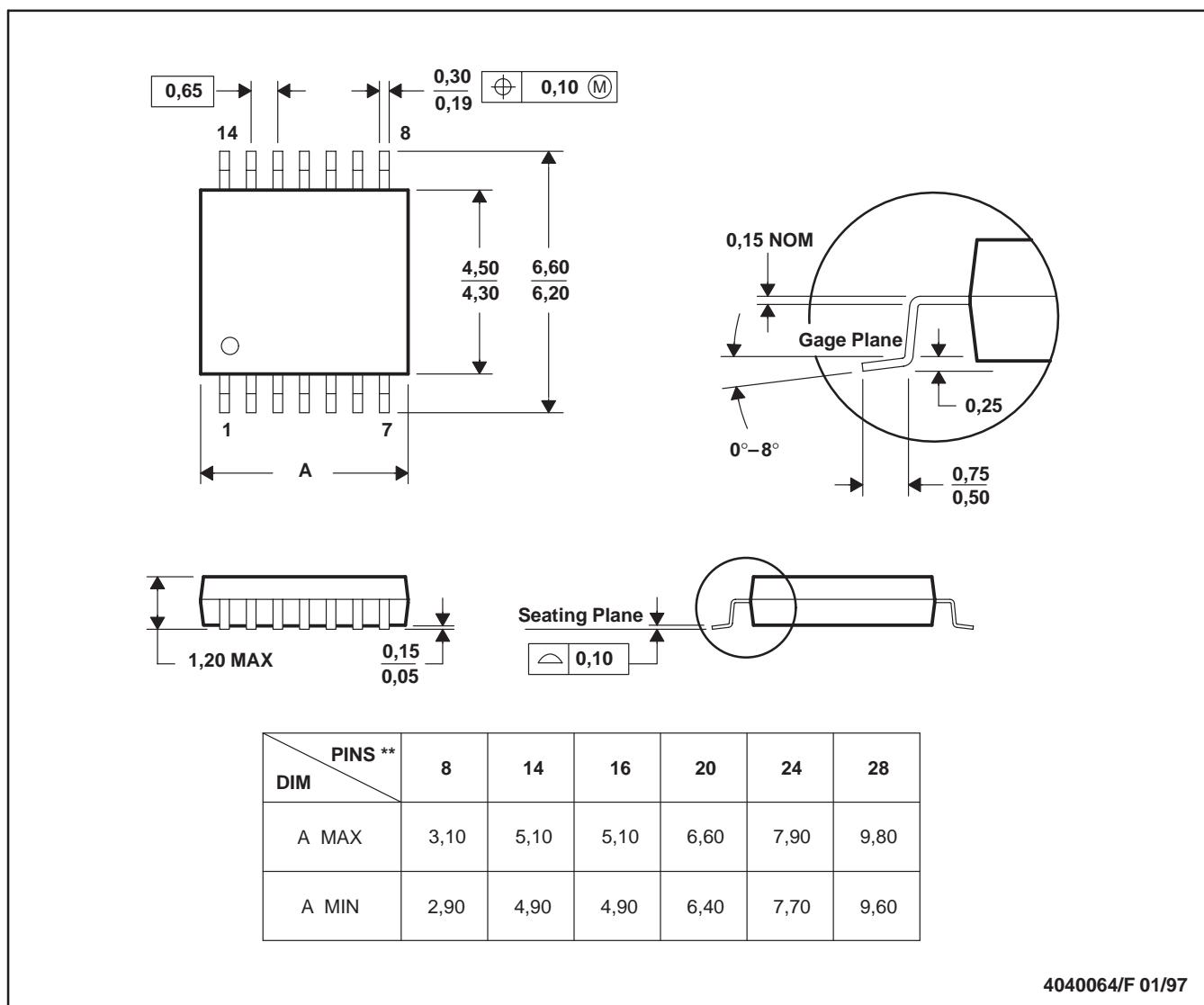


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

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View ROHS Compliant Devices clear gif**SN74LVC74A, Status: ACTIVE**

View RoHS Compliant Devices

Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear And Preset

 clear gif Features Quality & Pb-Free Data Related Products Tools & Software Samples Pricing/Packaging Inventory Symbols/Footprints Technical Documents Applications Notes Simulation Models Reference Designs**Refine Your Selection**

- Logic: D-Type Flip-Flop

Support

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomenclature

Datasheet Download Datasheet**SN54LVC74A, SN74LVC74A (Rev. S)** (sn74lvc74a.pdf, 526 KB)09 Aug 2004 [Download](#)

	SN54LVC74A	SN74LVC74A
Voltage Nodes(V)	3.3, 2.7, 2.5, 1.8	3.3, 2.7, 2.5, 1.8
Vcc range(V)	2.0 to 3.6	2.0 to 3.6
Input Level	TTL/CMOS	TTL/CMOS
Output Level	LVTTL	LVTTL
Output Drive(mA)	-24/24	-24/24
No. of Bits	2	2
No. of Outputs	4	
Static Current	0.01	0.01
th(ns)	1	0
tpd max(ns)	5.4	5.2
tsu(ns)	3	3
	Samples	Samples
	Inventory	Inventory

Product Information Features Save this to your personal library

Operate From 1.65 V to 3.6 V

Inputs Accept Voltages to 5.5 V

Max t_{pd} of 5.2 ns at 3.3 VTypical V_{OLP} (Output Ground Bounce)<0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$ Typical V_{OHV} (Output V_{OH} Undershoot)>2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$

Latch-Up Performance Exceeds 250 mA Per JESD 17

ESD Protection Exceeds JESD 22

- 2000-V Human-Body Model (A114-A)

- 200-V Machine Model (A115-A)

1000-V Charged-Device Model (C101)

 Description

The SN54LVC74A dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC74A dual positive-edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The data I/Os and control inputs are overvoltage tolerant. This feature allows the use of these devices for down-translation in a mixed-voltage environment.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74LVC74AD	ACTIVE	-40 to 85	0.17 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LVC74ADBLE	OBsolete	-40 to 85		SSOP (DB) 14	View		<input type="checkbox"/>	Not Available
SN74LVC74ADBR	ACTIVE	-40 to 85	0.17 1KU	SSOP (DB) 14	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC74ADB RG4	ACTIVE	-40 to 85	0.18 1KU	SSOP (DB) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC74ADE4	ACTIVE	-40 to 85	0.18 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LVC74ADG4	ACTIVE	-40 to 85	0.18 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LVC74ADR	ACTIVE	-40 to 85	0.17 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC74ADRE4	ACTIVE	-40 to 85	0.18 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Purchase Samples
SN74LVC74ADRG4	ACTIVE	-40 to 85	0.18 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Purchase Samples
SN74LVC74ADT	ACTIVE	-40 to 85	0.29 1KU	SOIC (D) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC74ADTE4	ACTIVE	-40 to 85	0.29 1KU	SOIC (D) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC74ANSR	ACTIVE	-40 to 85	0.18 1KU	SO (NS) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC74ANSRG4	ACTIVE	-40 to 85	0.18 1KU	SO (NS) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC74APW	ACTIVE	-40 to 85	0.17 1KU	TSSOP (PW) 14	View	90	<input type="checkbox"/>	Purchase Samples
SN74LVC74APWE4	ACTIVE	-40 to 85	0.17 1KU	TSSOP (PW) 14	View	90	<input type="checkbox"/>	Purchase Samples
SN74LVC74APWLE	OBsolete	-40 to 85		TSSOP (PW) 14	View		<input type="checkbox"/>	Not Available
SN74LVC74APWR	ACTIVE	-40 to 85	0.17 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC74APWRE4	ACTIVE	-40 to 85	0.18 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC74APWRG4	ACTIVE	-40 to 85	0.18 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC74APWT	ACTIVE	-40 to 85	0.29 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC74APWTE4	ACTIVE	-40 to 85	0.55 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC74APWTG4	ACTIVE	-40 to 85	0.51 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC74ARGYR	ACTIVE	-40 to 85	0.33 1KU	QFN (RGY) 14	View	1000		Request Free Samples
SN74LVC74ARGYRG4	ACTIVE	-40 to 85	0.33 1KU	QFN (RGY) 14	View	1000		Request Free Samples

Inventory

	TI Inventory Status			Reported Distributor Inventory				
SN74LVC74AD	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005				View all Distributors
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	Choose a Region
								

	>10k*	9000 12 Dec	10 Weeks	Americas	Arrow	>1k	
		1000 23 Jan			DigiKey	>1k	
		7000 6 Feb		Europe	Abacus Polar	845	
					Arrow Northern Europe	>1k	
					Avnet-SILICA	>1k	
					EBV Elektronik	>1k	
					Spoerle	>1k	

SN74LVC74ADBR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2000 6 Jan	8 Weeks	Americas	DigiKey	889	
		2000 1 Feb		Europe	Arrow Northern Europe	>1k	
		>10k 16 Feb					

SN74LVC74ADB RG4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1471 30 Nov	8 Weeks	None Reported View Distributors			
		693 10 Jan					
		840 7 Feb					
		>10k 14 Feb					

SN74LVC74ADE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Mar	14 Weeks	None Reported View Distributors			

SN74LVC74ADG4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 12 Dec	10 Weeks	None Reported View Distributors			

SN74LVC74ADR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2500 3 Jan	14 Weeks	Americas	DigiKey	>1k	
		>10k 6 Mar			Arrow Southern Europe	>1k	
					Avnet-SILICA	>1k	
					EBV Elektronik	>1k	
					Rutronik	>1k	

SN74LVC74ADRE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Mar	14 Weeks	None Reported View Distributors			

SN74LVC74ADRG4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Mar	14 Weeks	None Reported View Distributors			

SN74LVC74ADT	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	750*	>10k 6 Mar	10 Weeks	None Reported View Distributors			
SN74LVC74ADTE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	750*	>10k 6 Mar	10 Weeks	None Reported View Distributors			
SN74LVC74ANSR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	396 9 Jan	10 Weeks	None Reported View Distributors			
		267 16 Jan					
		633 23 Jan					
		980 30 Jan					
		1981 20 Feb					
SN74LVC74ANSRG4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	393 9 Jan	10 Weeks	None Reported View Distributors			
		265 16 Jan					
		629 23 Jan					
		974 30 Jan					
		1968 20 Feb					
SN74LVC74APW	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	6750 6 Mar	14 Weeks	Europe	Arrow Southern Europe	>1k	
					Avnet-SILICA	900	
SN74LVC74APWE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	6750 6 Mar	14 Weeks	None Reported View Distributors			
SN74LVC74APWR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2000 14 Feb	13 Weeks	Europe	EBV Elektronik	88	
		7951 16 Feb					
		>10k 28 Feb					
SN74LVC74APWRE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC74APWRG4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC74APWT	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported View Distributors			
SN74LVC74APWTE4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	4750 12 Dec	12 Weeks	None Reported View Distributors			
SN74LVC74APWTG4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC74ARGYR	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 12 Dec	8 Weeks	Americas	DigiKey	540	
				Europe	EBV Elektronik	500	
SN74LVC74ARGYRG4	As of 9:06 AM GMT, 29 Nov 2005			As of 9:06 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 12 Dec	8 Weeks	None Reported View Distributors			

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Quality & Lead (Pb)-Free Data

	Product Content					MTBF/FIT Rate
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details	
SN74LVC74AD <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADBR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADBRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ADTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ANSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ANSRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74APW <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74APWE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74APWR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74APWRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74APWRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74APWT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74APWTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74APWTG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
SN74LVC74ARGYR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View	
SN74LVC74ARGYRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View	

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

Technical Documents

Datasheets

[Keep track of what's new](#)

SN54LVC74A, SN74LVC74A (Rev. S) (sn74lvc74a.pdf, 526 KB)

09 Aug 2004 [Download](#)

Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)

08 Jul 2004 [Abstract](#)

Selecting the Right Level Translation Solution (Rev. A) (scea035a.htm, 9 KB)

22 Jun 2004 [Abstract](#)

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)

24 May 2004 [Abstract](#)

Use of the CMOS Unbuffered Inverter in Oscillator Circuits (szza043.htm, 9 KB)

06 Nov 2003 [Abstract](#)

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)

28 May 2003 [Abstract](#)

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