

LM158QML

Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15V$ power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

- Two internally compensated op amps
- Eliminates need for dual supplies
- Allows direct sensing near Gnd and V_O also goes to Gnd
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Available with radiation guarantee
 - High Dose Rate 100 krad(Si)
 - ELDRS Free 100 krad(Si)
- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply range:
 - Single supply: 3V to 32V
 - or dual supplies: $\pm 1.5V$ to $\pm 16V$
- Very low supply current drain (500 μA) – essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing: 0V to $V^+ - 1.5V$

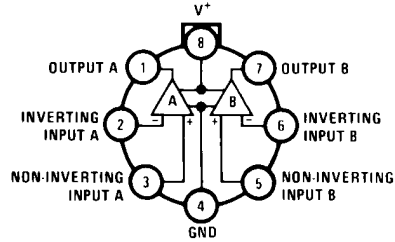
Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM158H/883		H08C	8LD T0–99 Metal Can
LM158J/883	5962–8771001PA	J08A	8LD Ceramic DIP
LM158H-SMD	5962–8771001GA	H08C	8LD T0–99 Metal Can
LM158AH/883	5962–8771002GA	H08C	8LD T0–99 Metal Can
LM158AJ/883	5962–8771002PA	J08A	8LD Ceramic DIP
LM158AWG/883	5962–8771002QXA	WG10A	10LD Ceramic SOIC
LM158AH-QMLV	5962–8771002VGA	H08C	8LD T0–99 Metal Can
LM158AHRQMLV HIGH DOSE RATE (Note 10)	5962R8771002VGA 100 krd(Si)	H08C	8LD T0–99 Metal Can
LM158AJ-QMLV	5962–8771002VPA	J08A	8LD Ceramic DIP
LM158AJRQMLV HIGH DOSE RATE (Note 10)	5962R8771002VPA 100 krd(Si)	J08A	8LD Ceramic DIP
LM158AWG-QMLV	5962–8771002VXA	WG10A	10LD Ceramic SOIC
LM158AWGRQMLV HIGH DOSE RATE (Note 10)	5962R8771002VXA 100 krd(Si)	WG10A	10LD Ceramic SOIC
LM158AHLRQMLV ELDRS FREE ONLY (Note 11)	5962R8771003VGA 100 krd(Si)	H08C	8LD T0–99 Metal Can

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM158AJRLQMLV ELDRS FREE ONLY (Note 11)	5962R8771003VPA 100 krd(Si)	J08A	8LD Ceramic DIP
LM158AWGRLQMLV ELDRS FREE ONLY (Note 11)	5962R8771003VXA 100 krd(Si)	WG10A	10LD Ceramic SOIC

Connection Diagrams

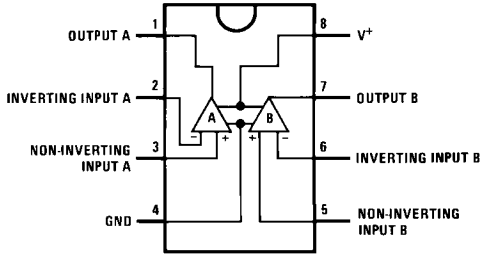
Metal Can Package



20150201

Top View
See NS Package Number H08C

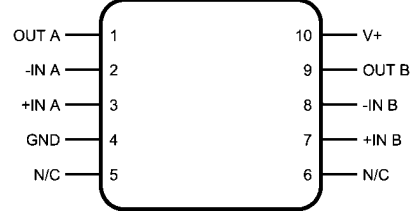
DIP Package



20150204

Top View
See NS Package Number J08A

10LD Ceramic SOIC

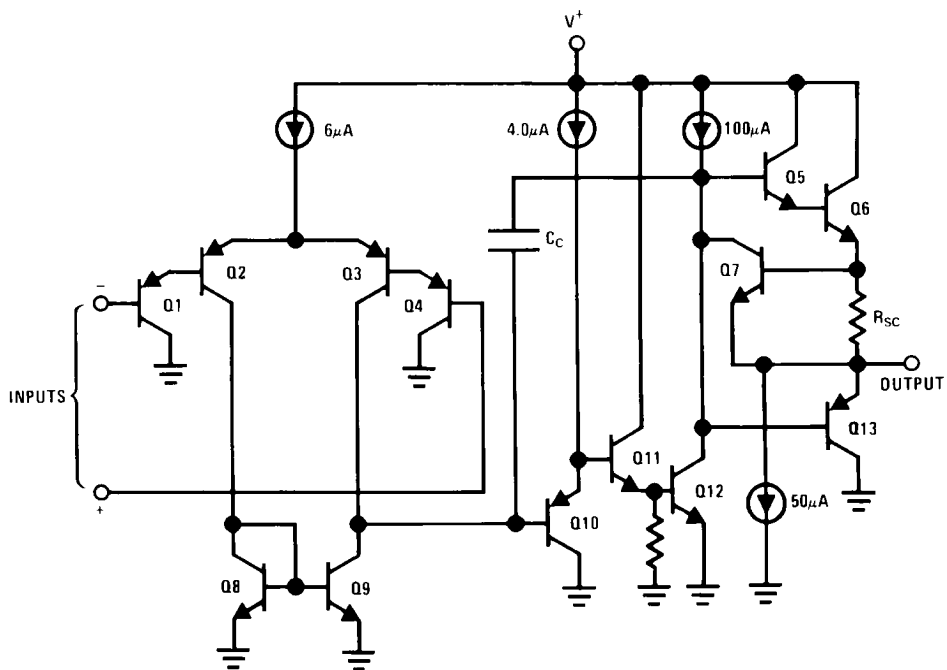


20150202

Top View
See NS Package Number WG10A

Schematic Diagram

(Each Amplifier)



20150203

Absolute Maximum Ratings (Note 1)

Supply Voltage, V^+	$32V_{DC}$
Differential Input Voltage	$32V_{DC}$
Input Voltage	$-0.3V_{DC}$ to $+32V_{DC}$
Power Dissipation (Note 2)	830 mW
Output Short-Circuit to GND(Note 3) (One Amplifier)	Continuous
$V^+ \leq 15V_{DC}$ and $T_A = 25^\circ C$	
Maximum Junction Temperature (T_{Jmax})	$150^\circ C$
Input Current ($V_I < -0.3V$)(Note 4)	50 mA
Operating Temperature Range	$-55^\circ C \leq T_A \leq +125^\circ C$
Storage Temperature Range	$-65^\circ C \leq T_A \leq +150^\circ C$
Lead Temperature (Soldering, 10 seconds)	
Metal Can	$300^\circ C$
Ceramic DIP	$260^\circ C$
Ceramic SOIC	$260^\circ C$
Thermal Resistance	
θ_{JA}	
Metal Can (Still Air)	$155^\circ C/W$
Metal Can (500LF/Min Air Flow)	$80^\circ C/W$
Ceramic DIP (Still Air)	$132^\circ C/W$
Ceramic DIP (500LF/Min Air Flow)	$81^\circ C/W$
Ceramic SOIC (Still Air)	$195^\circ C/W$
Ceramic SOIC (500LF/Min Air Flow)	$131^\circ C/W$
θ_{JC}	
Metal Can	$42^\circ C/W$
Ceramic DIP	$23^\circ C/W$
Ceramic SOIC	$33^\circ C/W$
Package Weight	
Metal Can	1,000mg
Ceramic DIP	1,100mg
Ceramic SOIC	220mg
ESD Tolerance (Note 7)	250V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LM158 Electrical Characteristics SMD 5962–8771001

DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Power Supply Current	$+V_{CC} = 5V, R_L = 100K,$ $V_O = 1.4V$			1.2	mA	1, 2, 3
		$+V_{CC} = 30V, R_L = 100K,$ $V_O = 1.4V$			3.0	mA	1
					4.0	mA	2, 3
V_{OH}	Output Voltage High	$+V_{CC} = 30V, R_L = 2K\Omega$		26		V	1, 2, 3
		$+V_{CC} = 30V, R_L = 10K\Omega$		27		V	1, 2, 3
V_{OL}	Output Voltage Low	$+V_{CC} = 30V, R_L = 10K\Omega$			20	mV	1, 2, 3
		$+V_{CC} = 30V, I_{Sink} = 1\mu A$			20	mV	1, 2, 3
		$+V_{CC} = 5V, R_L = 10K\Omega$			20	mV	1, 2, 3
I_{Sink}	Output Sink Current	$+V_{CC} = 15V, V_O = 200mV,$ $+V_I = 0V, -V_I = +65mV$		12		μA	1
		$+V_{CC} = 15V, V_O = 2V,$ $+V_I = 0V, -V_I = +65mV$		10		mA	1
				5.0		mA	2, 3
I_{Source}	Output Source Current	$+V_{CC} = 15V, V_O = 2V,$ $+V_I = 0V, -V_I = -65mV$			-20	mA	1
					-10	mA	2, 3
I_{OS}	Short Circuit Current	$+V_{CC} = 5V, V_O = 0V$		-60		mA	1
V_{IO}	Input Offset Voltage	$+V_{CC} = 30V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC} = 30V, V_{CM} = 28.5V,$ $R_S = 50\Omega, V_O = 1.4V$		-5.0	5.0	mV	1
		$+V_{CC} = 30V, V_{CM} = 28V,$ $R_S = 50\Omega, V_O = 1.4V$		-7.0	7.0	mV	2, 3
		$+V_{CC} = 5V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
CMRR	Common Mode Rejection Ratio	$+V_{CC} = 30V, R_S = 50\Omega$ $V_I = 0V$ to 28.5V,		70		dB	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 5V, V_{CM} = 0V$	(Note 5)	-150	-1.0	nA	1
			(Note 5)	-300	-1.0	nA	2, 3
I_{IO}	Input Offset Current	$+V_{CC} = 5V, V_{CM} = 0V$		-30	30	nA	1
				-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	$+V_{CC} = 5V$ to 30V, $V_{CM} = 0V$		65		dB	1
V_{CM}	Common Mode Voltage Range	$+V_{CC} = 30V$	(Note 6), (Note 8)		28.5	V	1
			(Note 6), (Note 8)		28.0	V	2, 3
V_{Diff}	Differential Input Voltage		(Note 9)		32	V	1, 2, 3
A_{VS}	Large Signal Gain	$+V_{CC} = 15V, R_L = 2K\Omega,$ $V_O = 1V$ to 11V		50		V/mV	4
				25		V/mV	5, 6

LM158A Electrical Characteristics SMD 5962–8771002, High Dose Rate

DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I _{CC}	Power Supply Current	+V _{CC} = 5V, R _L = 100K, V _O = 1.4V			1.2	mA	1, 2, 3
		+V _{CC} = 30V, R _L = 100K, V _O = 1.4V			3.0	mA	1
					4.0	mA	2, 3
V _{OH}	Output Voltage High	+V _{CC} = 30V, R _L = 2KΩ		26		V	1, 2, 3
		+V _{CC} = 30V, R _L = 10KΩ		27		V	1, 2, 3
V _{OL}	Output Voltage Low	+V _{CC} = 30V, R _L = 10KΩ			40	mV	1
					100	mV	2, 3
		+V _{CC} = 30V, I _{Sink} = 1μA			40	mV	1
					100	mV	2, 3
		+V _{CC} = 5V, R _L = 10KΩ			40	mV	1
					100	mV	2, 3
I _{Sink}	Output Sink Current	+V _{CC} = 15V, V _O = 200mV, +V _I = 0V, -V _I = +65mV		12		μA	1
		+V _{CC} = 15V, V _O = 2V, +V _I = 0V, -V _I = +65mV		10		mA	1
				5.0		mA	2, 3
I _{Source}	Output Source Current	+V _{CC} = 15V, V _O = 2V, +V _I = 0V, -V _I = -65mV			-20	mA	1
					-10	mA	2, 3
I _{OS}	Short Circuit Current	+V _{CC} = 5V, V _O = 0V		-60		mA	1
V _{IO}	Input Offset Voltage	+V _{CC} = 30V, V _{CM} = 0V, R _S = 50Ω, V _O = 1.4V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V _{CC} = 30V, V _{CM} = 28.5V, R _S = 50Ω, V _O = 1.4V		-2.0	2.0	mV	1
		+V _{CC} = 30V, V _{CM} = 28V, R _S = 50Ω, V _O = 1.4V		-4.0	4.0	mV	2, 3
		+V _{CC} = 5V, V _{CM} = 0V, R _S = 50Ω, V _O = 1.4V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
CMRR	Common Mode Rejection Ratio	+V _{CC} = 30V, R _S = 50Ω, V _I = 0V to 28.5V,		70		dB	1
±I _{IB}	Input Bias Current	+V _{CC} = 5V, V _{CM} = 0V	(Note 5)	-50	-1.0	nA	1
			(Note 5)	-100	-1.0	nA	2, 3
I _{IO}	Input Offset Current	+V _{CC} = 5V, V _{CM} = 0V		-10	10	nA	1
				-30	30	nA	2, 3
PSRR	Power Supply Rejection Ratio	+V _{CC} = 5V to 30V, V _{CM} = 0V		65		dB	1
V _{CM}	Common Mode Voltage Range	+V _{CC} = 30V	(Notes 6, 8)		28.5	V	1
			(Notes 6, 8)		28.0	V	2, 3
V _{Diff}	Differential Input Voltage		(Note 9)		32	V	1, 2, 3
A _{VS}	Large Signal Gain	+V _{CC} = 15V, R _L = 2KΩ, V _O = 1V to 11V		50		V/mV	4
				25		V/mV	5, 6

SMD 5962–8771002, High Dose Rate DC Drift Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.
Delta calculations are performed on QMLV devices at Group B, Subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 30V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$		-0.5	0.5	mV	1
		$+V_{CC} = 30V, V_{CM} = 28.5V,$ $R_S = 50\Omega, V_O = 1.4V$		-0.5	0.5	mV	1
		$+V_{CC} = 5V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 5V, V_{CM} = 0V$	(Note 5)	-10	10	nA	1

SMD 5962–8771002, High Dose Rate 100K Post Radiation Limits @ +25°C (Note 10) DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 30V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$	(Note 10)	-4.0	4.0	mV	1
		$+V_{CC} = 30V, V_{CM} = 28.5V,$ $R_S = 50\Omega, V_O = 1.4V$	(Note 10)	-4.0	4.0	mV	1
		$+V_{CC} = 5V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$	(Note 10)	-4.0	4.0	mV	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 5V, V_{CM} = 0V$	(Notes 5, 10)	-60	-1.0	nA	1
I_{CC}	Power Supply Current	$+V_{CC} = 5V, R_L = 100K,$ $V_O = 1.4V$	(Note 10)		1.5	mA	1

LM158A Electrical Characteristics SMD 5962–8771003 ELDRS Free Only

DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I _{CC}	Power Supply Current	+V _{CC} = 5V, R _L = 100K, V _O = 1.4V			0.75	mA	1, 2, 3
		+V _{CC} = 30V, R _L = 100K, V _O = 1.4V			1.2	mA	1, 2, 3
V _{OH}	Output Voltage High	+V _{CC} = 30V, R _L = 2KΩ		26		V	1, 2, 3
		+V _{CC} = 30V, R _L = 10KΩ		27		V	1, 2, 3
V _{OL}	Output Voltage Low	+V _{CC} = 30V, R _L = 10KΩ			40	mV	1
					100	mV	2, 3
		+V _{CC} = 30V, I _{Sink} = 1μA			40	mV	1
					100	mV	2, 3
					40	mV	1
		100	mV	2, 3			
I _{Sink}	Output Sink Current	+V _{CC} = 15V, V _O = 200mV, +V _I = 0V, -V _I = +65mV		12		μA	1
				10		mA	1
		+V _{CC} = 15V, V _O = 2V, +V _I = 0V, -V _I = +65mV		5.0		mA	2, 3
I _{Source}	Output Source Current	+V _{CC} = 15V, V _O = 2V, +V _I = 0V, -V _I = -65mV			-20	mA	1
					-10	mA	2, 3
I _{OS}	Short Circuit Current	+V _{CC} = 5V, V _O = 0V		-60		mA	1
V _{IO}	Input Offset Voltage	+V _{CC} = 30V, V _{CM} = 0V, R _S = 50Ω, V _O = 1.4V		-1.0	1.0	mV	1
				-2.0	2.0	mV	2, 3
		+V _{CC} = 30V, V _{CM} = 28.5V, R _S = 50Ω, V _O = 1.4V		-1.0	1.0	mV	1
				-2.0	2.0	mV	2, 3
+V _{CC} = 5V, V _{CM} = 0V, R _S = 50Ω, V _O = 1.4V		-1.0	1.0	mV	1		
		-2.0	2.0	mV	2, 3		
CMRR	Common Mode Rejection Ratio	+V _{CC} = 30V, R _S = 50Ω V _I = 0V to 28.5V,		90		dB	1
±I _{IB}	Input Bias Current	+V _{CC} = 5V, V _{CM} = 0V	(Note 5)	-30	-1.0	nA	1
			(Note 5)	-50	-1.0	nA	2, 3
I _{IO}	Input Offset Current	+V _{CC} = 5V, V _{CM} = 0V		-3.0	3.0	nA	1
				-5.0	5.0	nA	2, 3
PSRR	Power Supply Rejection Ratio	+V _{CC} = 5V to 30V, V _{CM} = 0V		100		dB	1
V _{CM}	Common Mode Voltage Range	+V _{CC} = 30V	(Note 6), (Note 8)		28.5	V	1
			(Note 6), (Note 8)		28.0	V	2, 3
V _{Diff}	Differential Input Voltage		(Note 9)		32	V	1, 2, 3
A _{VS}	Large Signal Gain	+V _{CC} = 15V, R _L = 2KΩ, V _O = 1V to 11V		200		V/mV	4
				75		V/mV	5, 6

SMD 5962–8771003, ELDRS Free Only DC Drift Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.
Delta calculations are performed on QMLV devices at Group B, Subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 30V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$		-0.5	0.5	mV	1
		$+V_{CC} = 30V, V_{CM} = 28.5V,$ $R_S = 50\Omega, V_O = 1.4V$		-0.5	0.5	mV	1
		$+V_{CC} = 5V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 5V, V_{CM} = 0V$	(Note 5)	-10	10	nA	1

SMD 5962–8771003, ELDRS Free Only 100K Post Radiation Limits @ +25°C (Note 11) DC Parameters

The following conditions apply, unless otherwise specified. All voltages referenced to device ground.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 30V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$	(Note 11)	-2.0	2.0	mV	1
		$+V_{CC} = 30V, V_{CM} = 28.5V,$ $R_S = 50\Omega, V_O = 1.4V$	(Note 11)	-2.0	2.0	mV	1
		$+V_{CC} = 5V, V_{CM} = 0V,$ $R_S = 50\Omega, V_O = 1.4V$	(Note 11)	-2.0	2.0	mV	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 5V, V_{CM} = 0V$	(Notes 5, 11)	-60	-1.0	nA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+ . At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$ (at 25°C).

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 6: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage, independent of the magnitude of V^+ .

Note 7: Human body model, 1.5 k Ω in series with 100 pF.

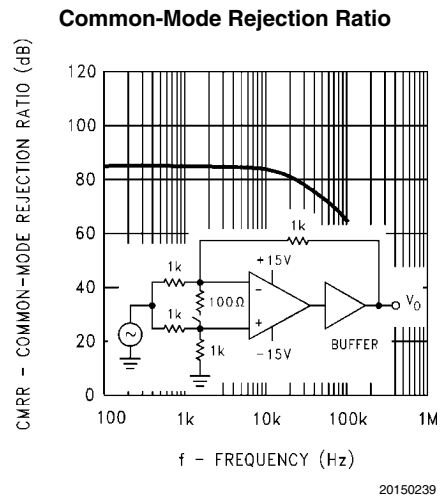
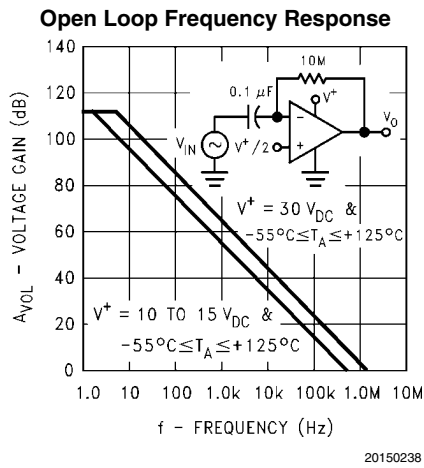
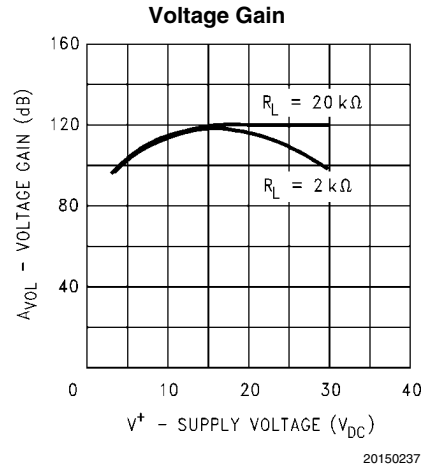
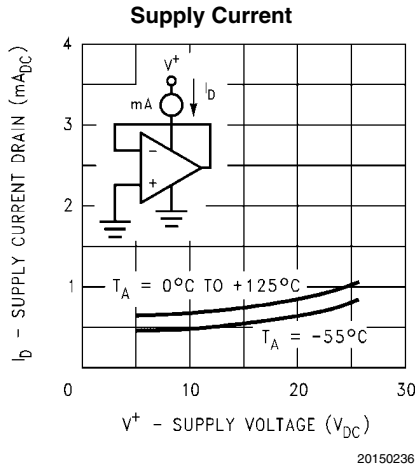
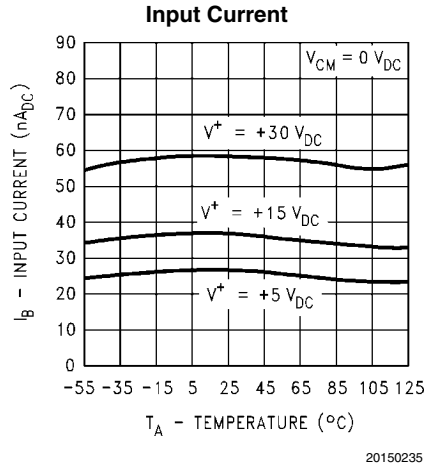
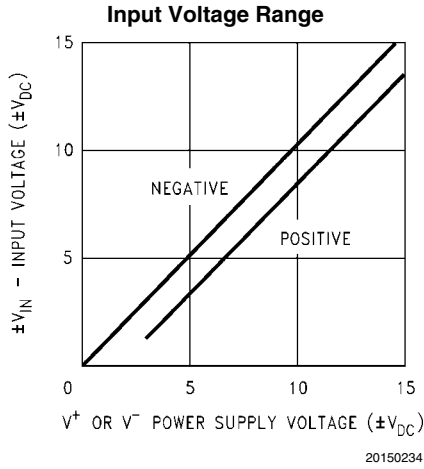
Note 8: Guaranteed by input offset voltage.

Note 9: Guaranteed parameter not tested.

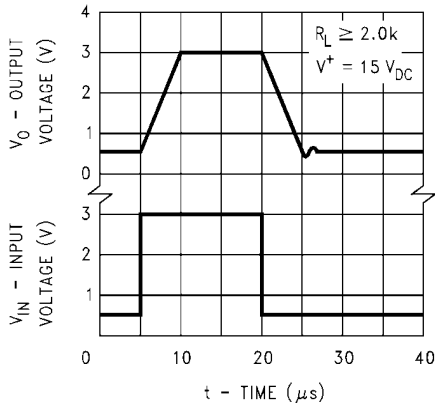
Note 10: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019

Note 11: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect

Typical Performance Characteristics

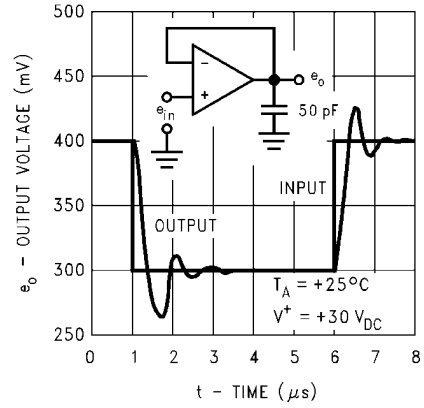


Voltage Follower Pulse Response



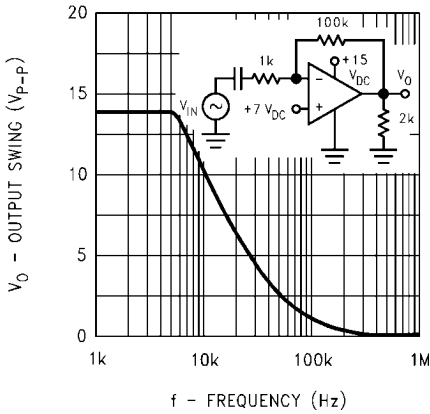
20150240

Voltage Follower Pulse Response (Small Signal)



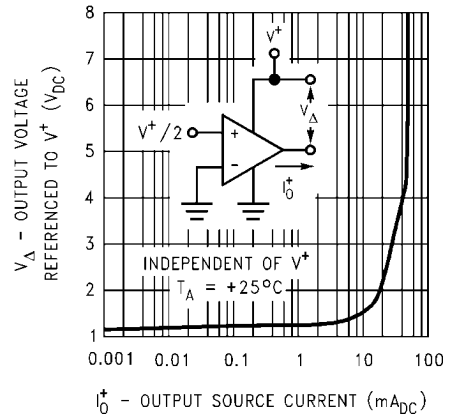
20150241

Large Signal Frequency Response



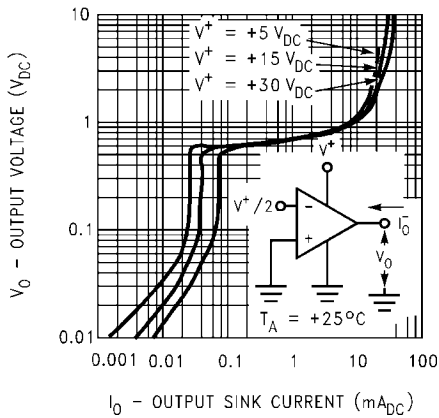
20150242

Output Characteristics Current Sourcing



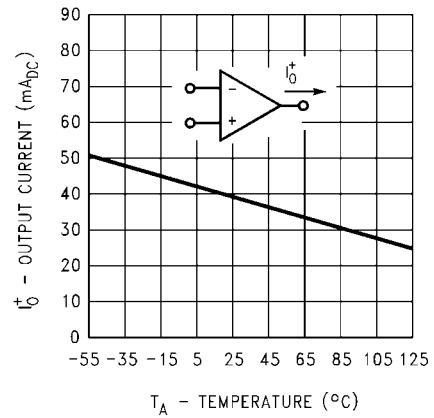
20150243

Output Characteristics Current Sinking



20150244

Current Limiting



20150245

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of $0 V_{DC}$. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of $2.3 V_{DC}$.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3 V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of $3 V_{DC}$ to $30 V_{DC}$.

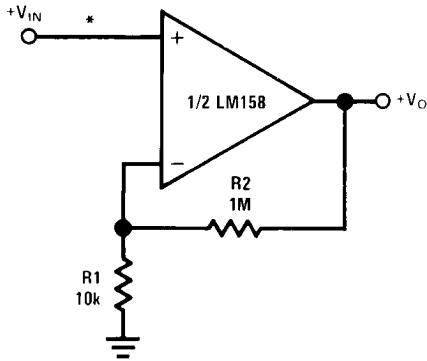
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications

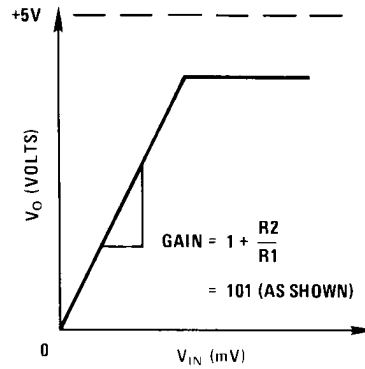
($V^+ = 5.0 V_{DC}$)

Non-Inverting DC Gain (0V Output)



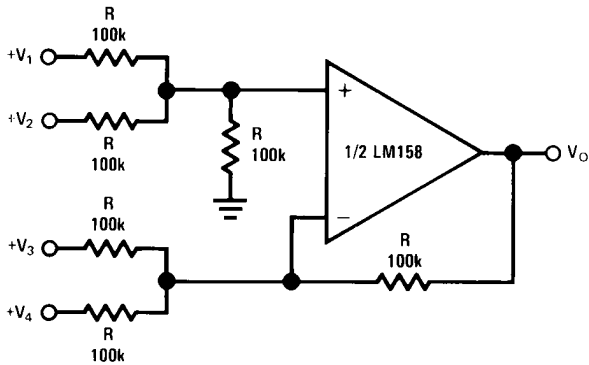
20150206

*R not needed due to temperature independent I_{IN}



20150207

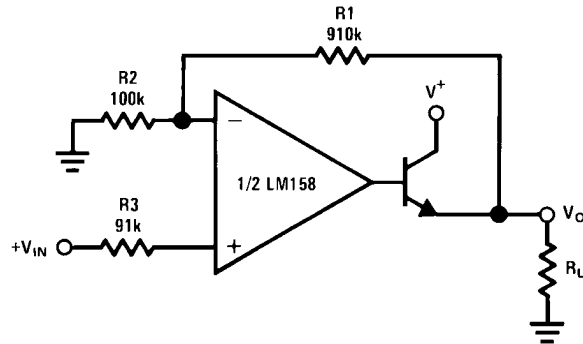
DC Summing Amplifier ($V_{IN'S} \geq 0 V_{DC}$ and $V_O \geq 0 V_{DC}$)



20150208

Where: $V_O = V_1 + V_2 - V_3 - V_4$
 $(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0 V_{DC}$

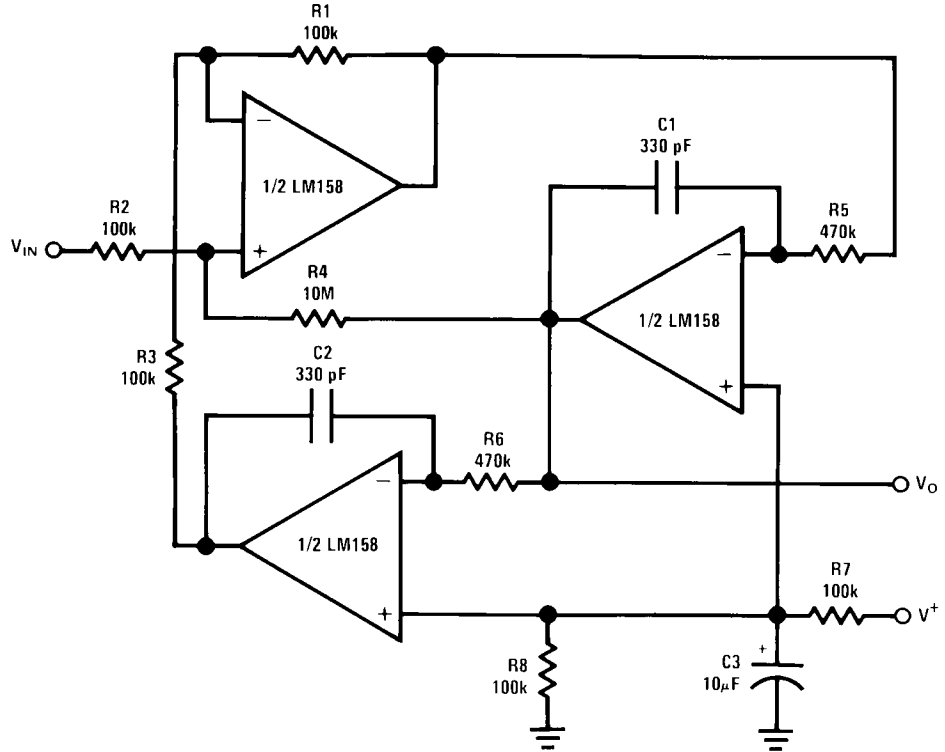
Power Amplifier



20150209

$V_O = 0 V_{DC}$ for $V_{IN} = 0 V_{DC}$
 $A_V = 10$

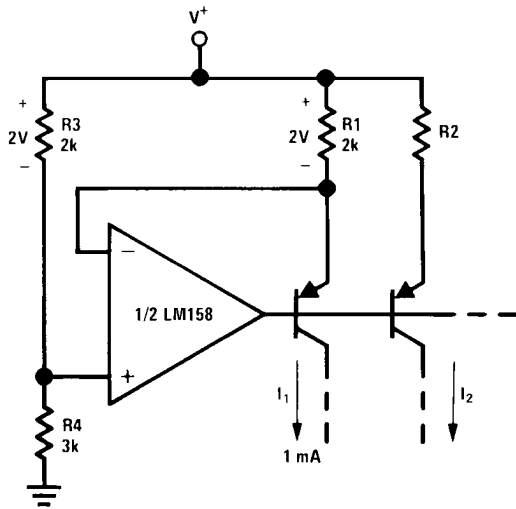
"BI-QUAD" RC Active Bandpass Filter



20150210

$f_o = 1 \text{ kHz}$
 $Q = 50$
 $A_v = 100 \text{ (40 dB)}$

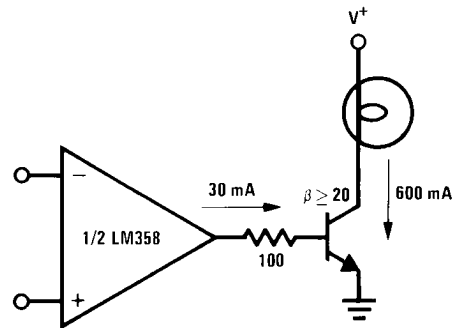
Fixed Current Sources



20150211

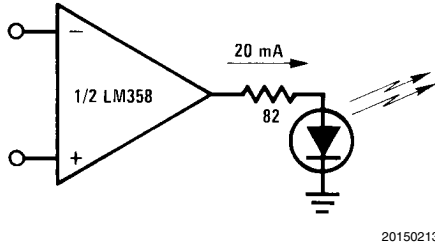
$$I_2 = \left(\frac{R_1}{R_2} \right) I_1$$

Lamp Driver



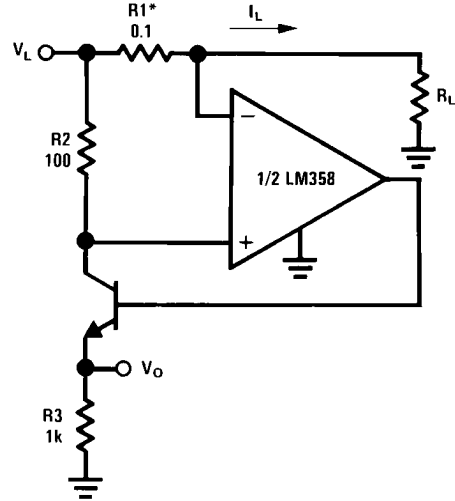
20150212

LED Driver



20150213

Current Monitor

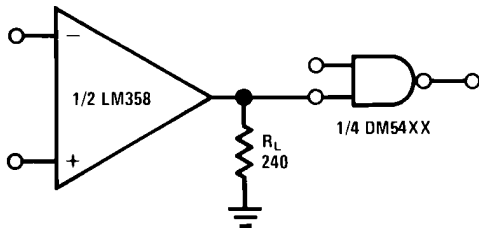


20150214

$$V_O = \frac{1V(I_L)}{1A}$$

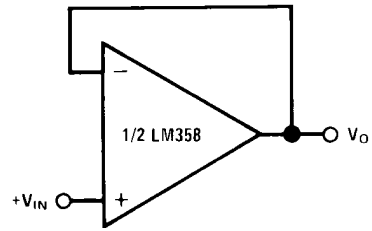
*(Increase R1 for I_L small)
 $V_L \leq V^+ - 2V$

Driving TTL



20150215

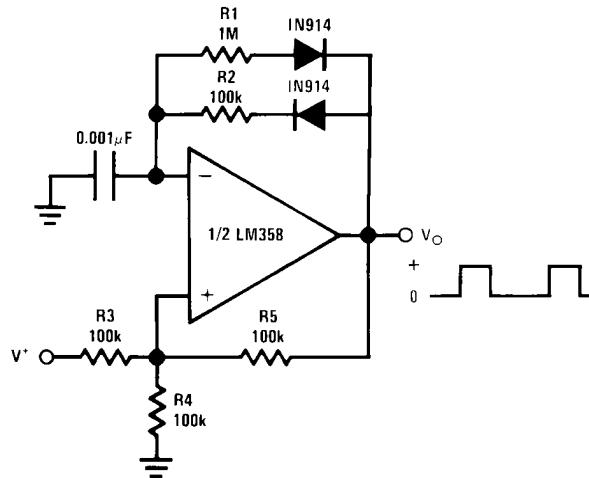
Voltage Follower



20150217

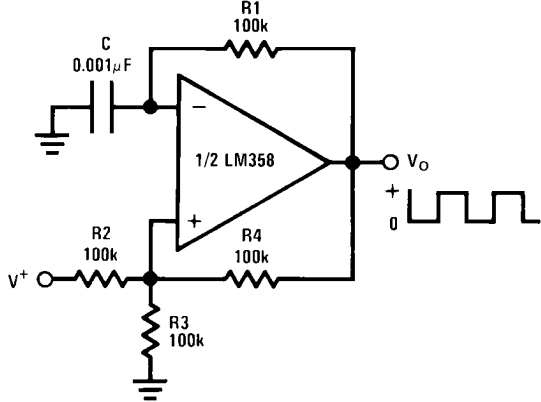
$$V_O = V_{IN}$$

Pulse Generator



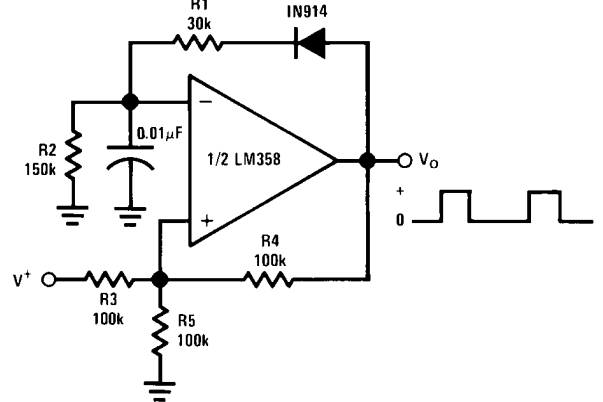
20150216

Squarewave Oscillator



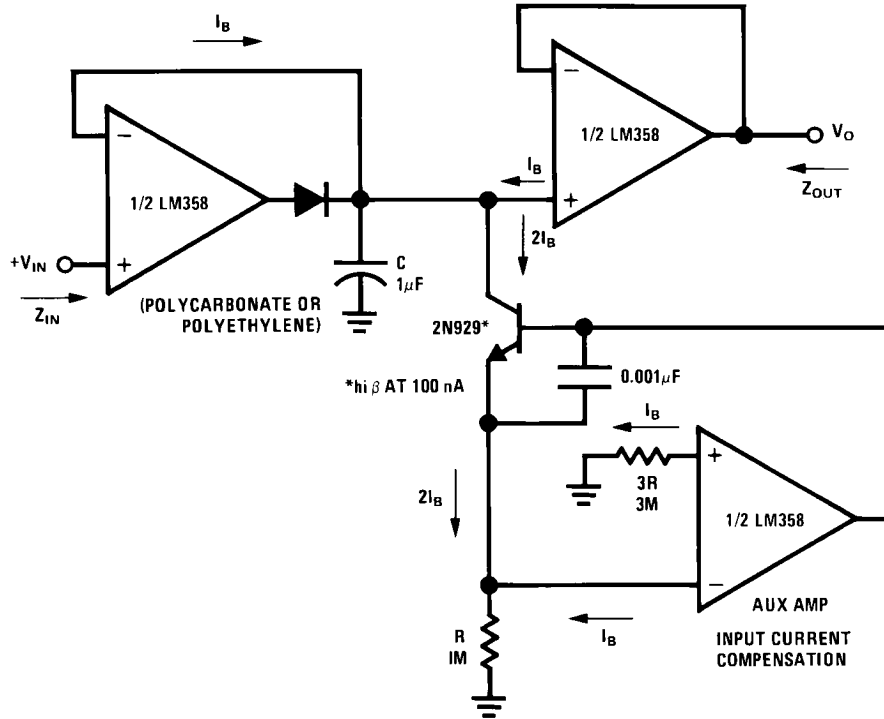
20150218

Pulse Generator



20150219

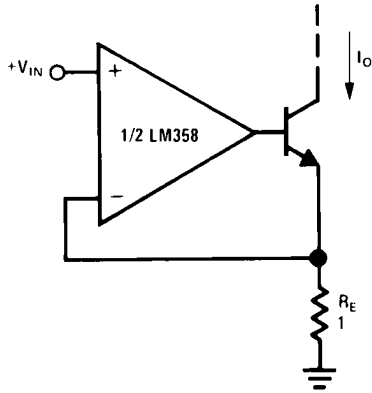
Low Drift Peak Detector



20150220

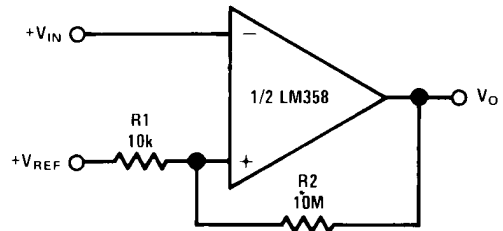
HIGH Z_{IN}
LOW Z_{OUT}

High Compliance Current Sink



20150221

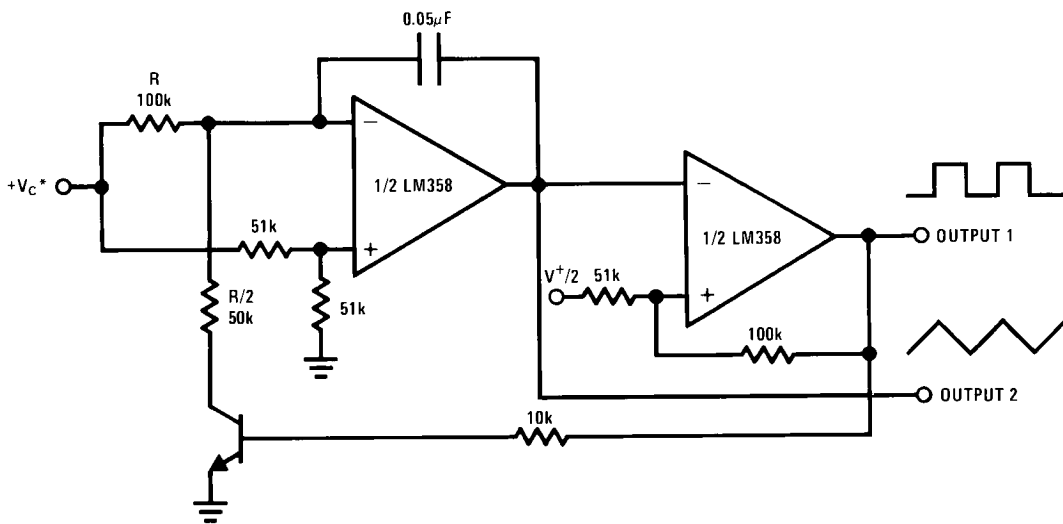
Comparator with Hysteresis



20150222

$I_O = 1 \text{ amp/volt } V_{IN}$
 (Increase R_E for I_O small)

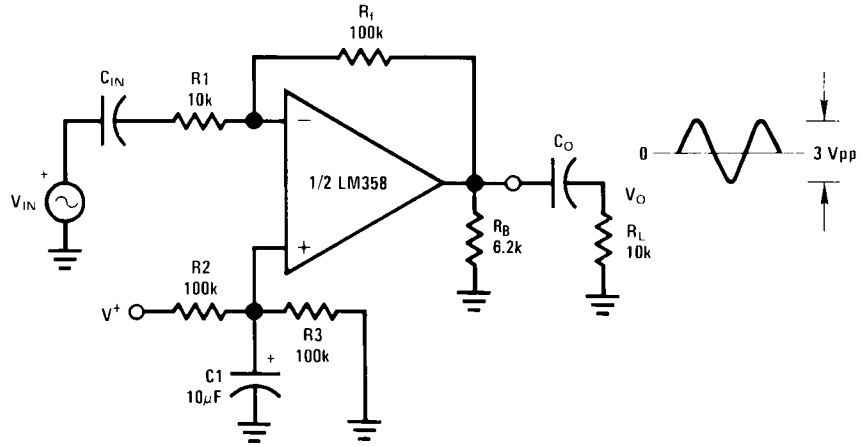
Voltage Controlled Oscillator (VCO)



20150223

*WIDE CONTROL VOLTAGE RANGE: $0 V_{DC} \leq V_C \leq 2 (V^+ - 1.5V_{DC})$

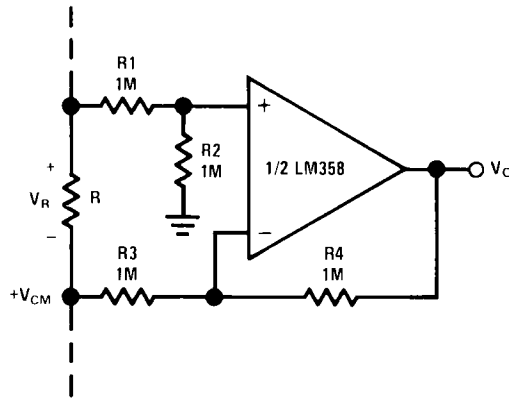
AC Coupled Inverting Amplifier



20150224

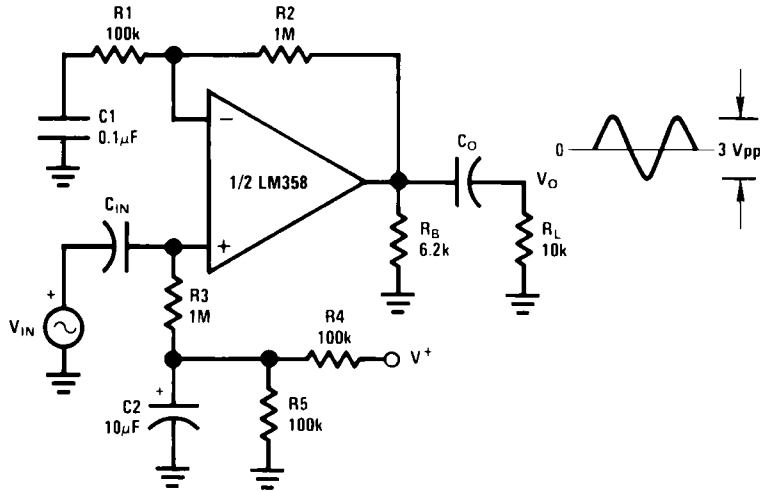
$$A_V = \frac{R_f}{R_1} \text{ (As shown, } A_V = 10 \text{)}$$

Ground Referencing a Differential Input Signal



20150225

AC Coupled Non-Inverting Amplifier

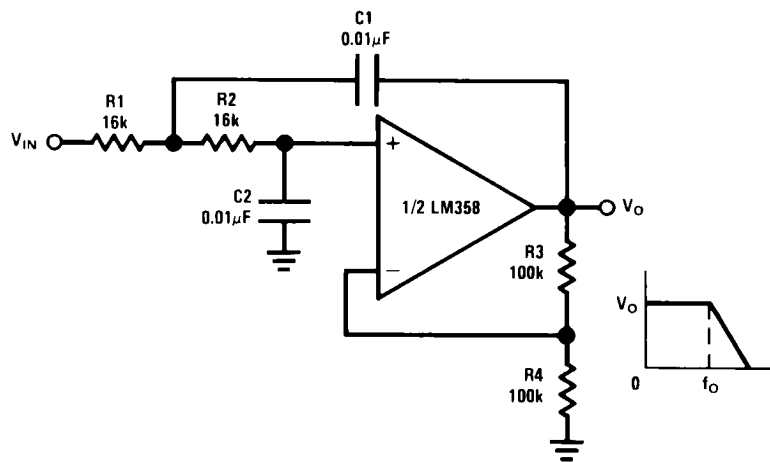


20150226

$$A_V = 1 + \frac{R_2}{R_1}$$

$A_V = 11$ (As Shown)

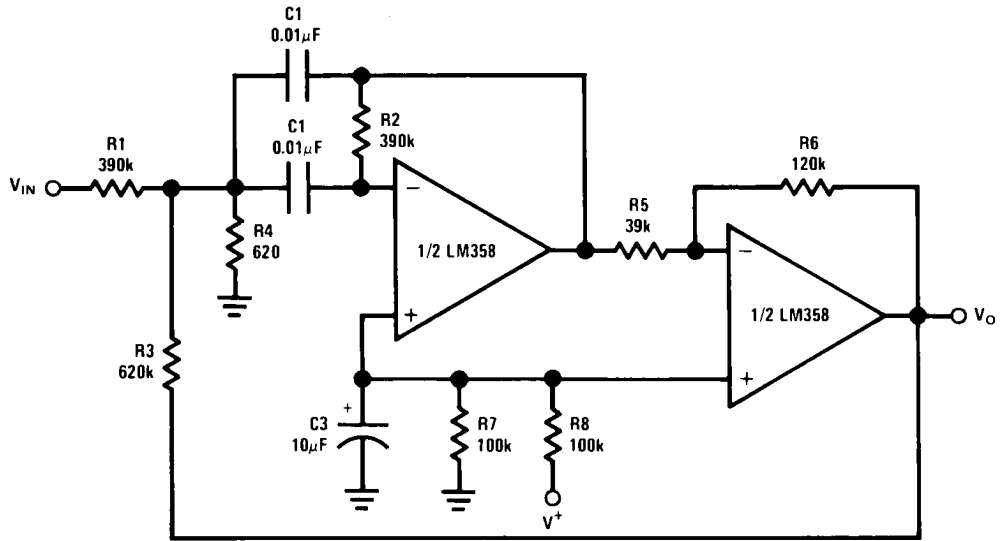
DC Coupled Low-Pass RC Active Filter



20150227

$f_o = 1$ kHz
 $Q = 1$
 $A_V = 2$

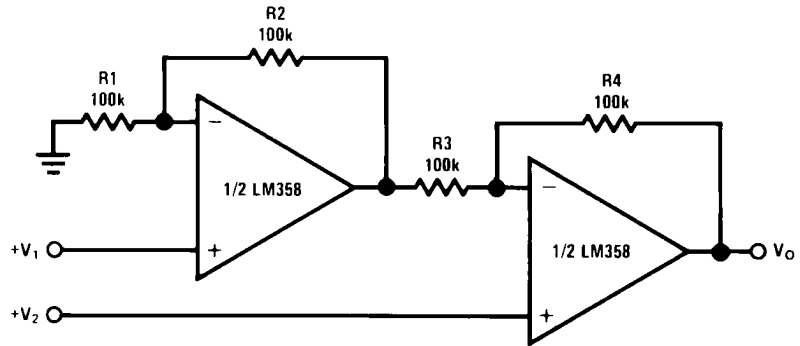
Bandpass Active Filter



20150228

$f_o = 1 \text{ kHz}$
 $Q = 25$

High Input Z, DC Differential Amplifier



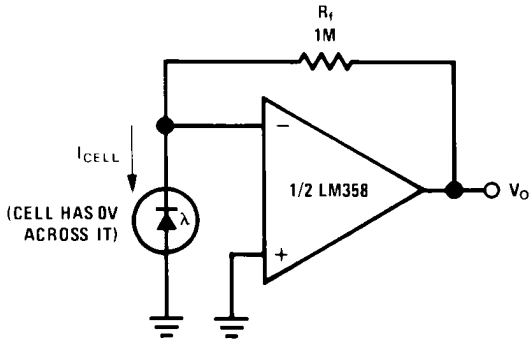
20150229

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3} (V_2 - V_1)$$

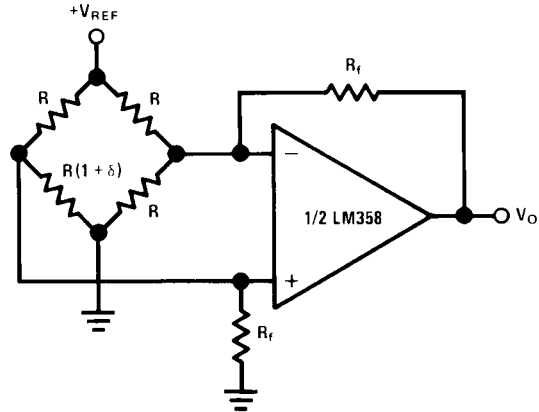
As Shown: $V_O = 2 (V_2 - V_1)$

Photo Voltaic-Cell Amplifier



20150230

Bridge Current Amplifier

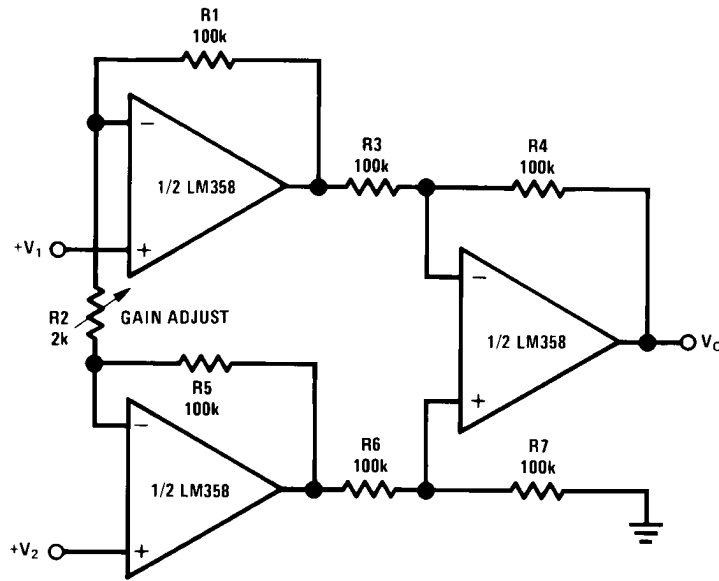


20150233

For $\delta \ll 1$ and $R_f \gg R$

$$V_O \approx V_{REF} \left(\frac{\delta}{2} \right) \frac{R_f}{R}$$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



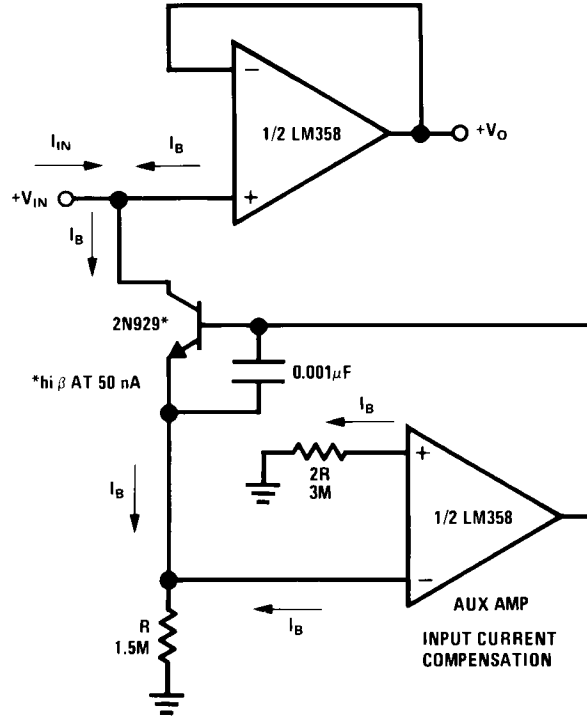
20150231

If $R_1 = R_5$ & $R_3 = R_4 = R_6 = R_7$ (CMRR depends on match)

$$V_O = 1 + \frac{2R_1}{R_2} (V_2 - V_1)$$

As shown $V_O = 101 (V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)

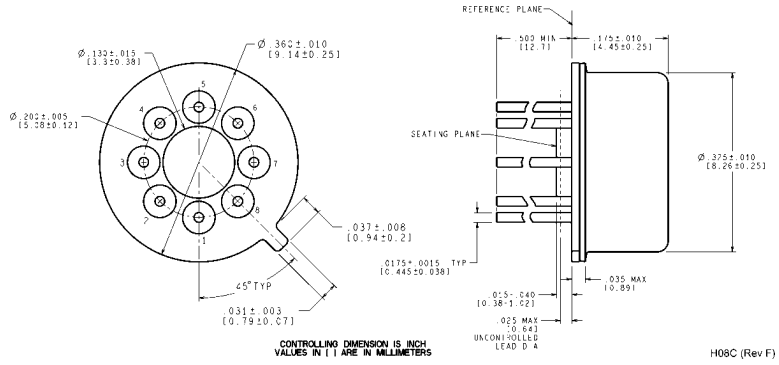


20150232

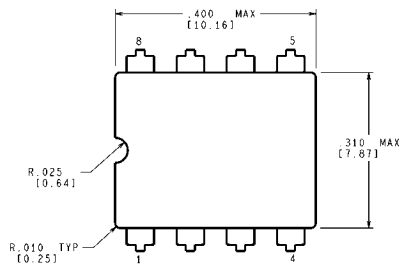
Revision History

Date Released	Revision	Section	Originator	Changes
07/12/05	A	New release to corporate format.	L. Lytle	2 MDS datasheets converted into one Corporate datasheet format. MNLM158-X-RH Rev 1C1 & MNLM158-X Rev 1A1 will be archived.
01/09/06	B	Typical Single-Supply Applications	R. Malone	Correct an equation From: $V1 + V2 + V3 + V4$ To: $V1 + V2 - V3 - V4$ (right after art -08, pg 12). Reason: To reflect same correction made in commercial data sheet. Revision A will be archived.
01/27/06	C	Features, Ordering Information Table and Post Radiation Electrical's	Larry McGee	Added reference to radiation, NSID's to Ordering Table and Post Rad limits for 100k
10/05/06	D	Connection Diagram, page 2	R. Malone	Corrected typo title for Ceramic SOIC. Revision C will be Archived
08/21/08	E	Features, Ordering Information, Electrical Sections and Notes.	Larry McGee	Added reference to ELDRS, NSID's to Ordering Table, and ELDRS Electricals. Deleted 50k Rad NSID's and Post Rad table. Revision D will be Archived.

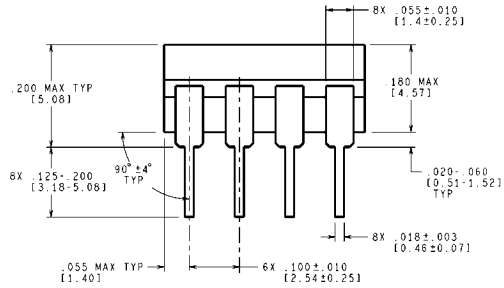
Physical Dimensions inches (millimeters) unless otherwise noted



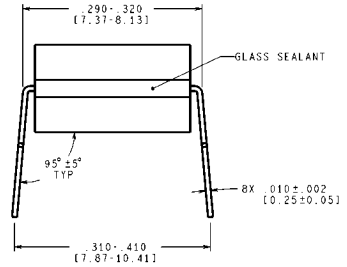
Metal Can Package (H)
NS Package Number H08C



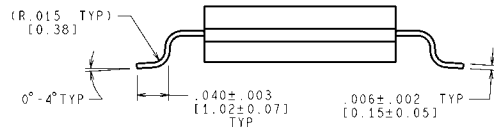
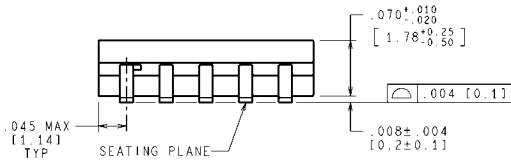
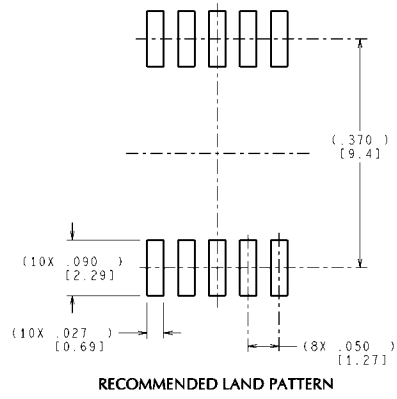
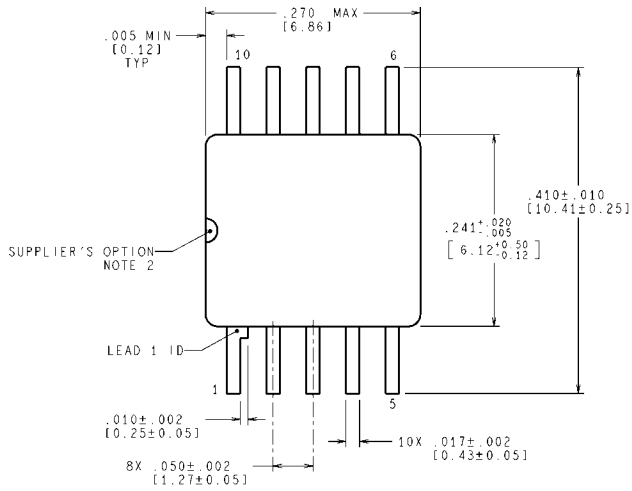
CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS



CERDIP Package (J)
NS Package Number J08A



J08A (Rev M)



MIL-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

WG10A (Rev E)

**10LD Ceramic SOIC Package
NS Package Number WG10A**

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2008 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com