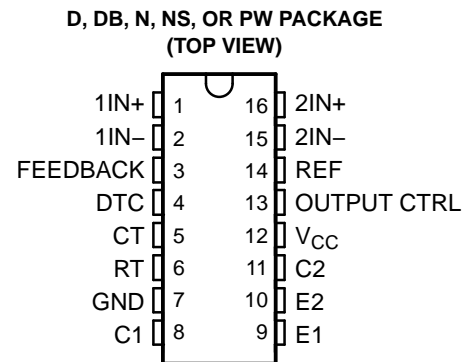


## FEATURES

- Complete PWM Power-Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source Current
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance
- Circuit Architecture Allows Easy Synchronization



## DESCRIPTION

The TL494 incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application.

The TL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from  $-0.3\text{ V}$  to  $V_{CC} - 2\text{ V}$ . The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 provides for push-pull or single-ended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494C is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . The TL494I is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES <sup>(1)</sup>				
	SMALL OUTLINE (D)	PLASTIC DIP (N)	SMALL OUTLINE (NS)	SHRINK SMALL OUTLINE (DB)	THIN SHRINK SMALL OUTLINE (PW)
$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	TL494CD	TL494CN	TL494CNS	TL494CDB	TL494CPW
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	TL494ID	TL494IN	—	—	—

(1) The D, DB, NS, and PW packages are available taped and reeled. Add the suffix R to device type (e.g., TL494CDR).

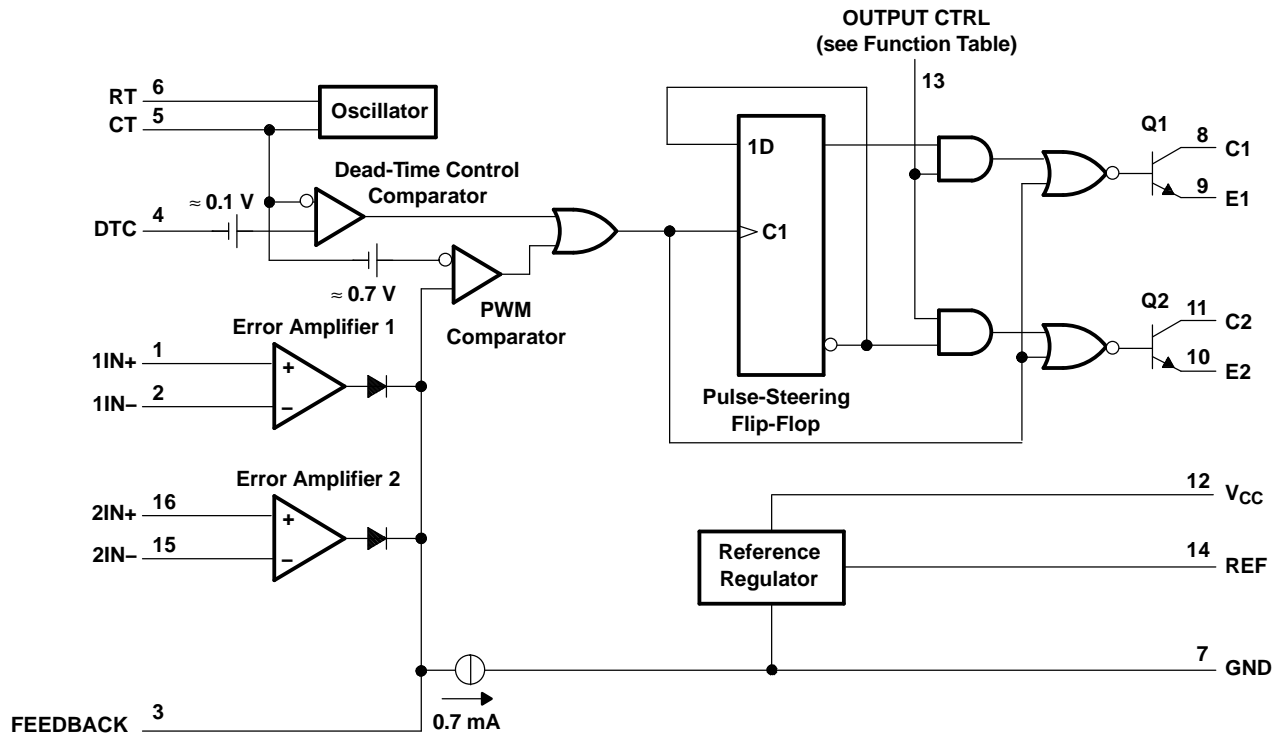


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE**

INPUT TO OUTPUT CTRL	OUTPUT FUNCTION
$V_I = \text{GND}$	Single-ended or parallel output
$V_I = V_{\text{ref}}$	Normal push-pull operation

**FUNCTIONAL BLOCK DIAGRAM**



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage <sup>(2)</sup>		41	V
$V_I$	Amplifier input voltage		$V_{CC} + 0.3$	V
$V_O$	Collector output voltage		41	V
$I_O$	Collector output current		250	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)(4)</sup>	D package	73	°C/W
		DB package	82	
		N package	67	
		NS package	64	
		PW package	108	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the network ground terminal.
- (3) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JEDEC 51-7.

### Recommended Operating Conditions

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	7	40	V	
$V_I$	Amplifier input voltage	–0.3	$V_{CC} - 2$	V	
$V_O$	Collector output voltage		40	V	
	Collector output current (each transistor)		200	mA	
	Current into feedback terminal		0.3	mA	
$f_{OSC}$	Oscillator frequency	1	300	kHz	
$C_T$	Timing capacitor	0.47	10000	nF	
$R_T$	Timing resistor	1.8	500	k $\Omega$	
$T_A$	Operating free-air temperature	TL494C	0	70	°C
		TL494I	–40	85	

## Electrical Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 15\text{ V}$ ,  $f = 10\text{ kHz}$  (unless otherwise noted)

## Reference Section

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TL494C, TL494I			UNIT
		MIN	TYP <sup>(2)</sup>	MAX	
Output voltage (REF)	$I_O = 1\text{ mA}$	4.75	5	5.25	V
Input regulation	$V_{CC} = 7\text{ V to }40\text{ V}$		2	25	mV
Output regulation	$I_O = 1\text{ mA to }10\text{ mA}$		1	15	mV
Output voltage change with temperature	$\Delta T_A = \text{MIN to MAX}$		2	10	mV/V
Short-circuit output current <sup>(3)</sup>	REF = 0 V		25		mA

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
(2) All typical values, except for parameter changes with temperature, are at  $T_A = 25^\circ\text{C}$ .  
(3) Duration of short circuit should not exceed one second.

## Oscillator Section

$C_T = 0.01\text{ }\mu\text{F}$ ,  $R_T = 12\text{ k}\Omega$  (see Figure 1)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TL494C, TL494I			UNIT
		MIN	TYP <sup>(2)</sup>	MAX	
Frequency			10		kHz
Standard deviation of frequency <sup>(3)</sup>	All values of $V_{CC}$ , $C_T$ , $R_T$ , and $T_A$ constant		100		Hz/kHz
Frequency change with voltage	$V_{CC} = 7\text{ V to }40\text{ V}$ , $T_A = 25^\circ\text{C}$		1		Hz/kHz
Frequency change with temperature <sup>(4)</sup>	$\Delta T_A = \text{MIN to MAX}$			10	Hz/kHz

- (1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
(2) All typical values, except for parameter changes with temperature, are at  $T_A = 25^\circ\text{C}$ .  
(3) Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^N (x_n - \bar{X})^2}{N - 1}}$$

- (4) Temperature coefficient of timing capacitor and timing resistor are not taken into account.

## Error-Amplifier Section

See Figure 2

PARAMETER	TEST CONDITIONS	TL494C, TL494I			UNIT
		MIN	TYP <sup>(1)</sup>	MAX	
Input offset voltage	$V_O (\text{FEEDBACK}) = 2.5\text{ V}$		2	10	mV
Input offset current	$V_O (\text{FEEDBACK}) = 2.5\text{ V}$		25	250	nA
Input bias current	$V_O (\text{FEEDBACK}) = 2.5\text{ V}$		0.2	1	$\mu\text{A}$
Common-mode input voltage range	$V_{CC} = 7\text{ V to }40\text{ V}$		-0.3 to $V_{CC} - 2$		V
Open-loop voltage amplification	$\Delta V_O = 3\text{ V}$ , $V_O = 0.5\text{ V to }3.5\text{ V}$ , $R_L = 2\text{ k}\Omega$		70	95	dB
Unity-gain bandwidth	$V_O = 0.5\text{ V to }3.5\text{ V}$ , $R_L = 2\text{ k}\Omega$		800		kHz
Common-mode rejection ratio	$\Delta V_O = 40\text{ V}$ , $T_A = 25^\circ\text{C}$		65	80	dB
Output sink current (FEEDBACK)	$V_{ID} = -15\text{ mV to }-5\text{ V}$ , $V (\text{FEEDBACK}) = 0.7\text{ V}$		0.3	0.7	mA
Output source current (FEEDBACK)	$V_{ID} = 15\text{ mV to }5\text{ V}$ , $V (\text{FEEDBACK}) = 3.5\text{ V}$		-2		mA

- (1) All typical values, except for parameter changes with temperature, are at  $T_A = 25^\circ\text{C}$ .

## Electrical Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 15\text{ V}$ ,  $f = 10\text{ kHz}$  (unless otherwise noted)

### Output Section

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Collector off-state current		$V_{CE} = 40\text{ V}$ , $V_{CC} = 40\text{ V}$		2	100	$\mu\text{A}$
Emitter off-state current		$V_{CC} = V_C = 40\text{ V}$ , $V_E = 0$			-100	$\mu\text{A}$
Collector-emitter saturation voltage	Common emitter	$V_E = 0$ , $I_C = 200\text{ mA}$		1.1	1.3	V
	Emitter follower	$V_{O(C1\text{ or }C2)} = 15\text{ V}$ , $I_E = -200\text{ mA}$		1.5	2.5	
Output control input current		$V_I = V_{ref}$			3.5	mA

(1) All typical values, except for temperature coefficient, are at  $T_A = 25^\circ\text{C}$ .

### Dead-Time Control Section

See Figure 1

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Input bias current (DEAD-TIME CTRL)		$V_I = 0$ to $5.25\text{ V}$		-2	-10	$\mu\text{A}$
Maximum duty cycle, each output		$V_I$ (DEAD-TIME CTRL) = 0, $C_T = 0.01\ \mu\text{F}$ , $R_T = 12\text{ k}\Omega$		45		%
Input threshold voltage (DEAD-TIME CTRL)	Zero duty cycle			3	3.3	V
	Maximum duty cycle		0			

(1) All typical values, except for temperature coefficient, are at  $T_A = 25^\circ\text{C}$ .

### PWM Comparator Section

See Figure 1

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Input threshold voltage (FEEDBACK)		Zero duty cycle		4	4.5	V
Input sink current (FEEDBACK)		$V$ (FEEDBACK) = $0.7\text{ V}$	0.3	0.7		mA

(1) All typical values, except for temperature coefficient, are at  $T_A = 25^\circ\text{C}$ .

### Total Device

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Standby supply current	$R_T = V_{ref}$ , All other inputs and outputs open	$V_{CC} = 15\text{ V}$		6	10	mA
		$V_{CC} = 40\text{ V}$		9	15	
Average supply current		$V_I$ (DEAD-TIME CTRL) = $2\text{ V}$ , See Figure 1		7.5		mA

(1) All typical values, except for temperature coefficient, are at  $T_A = 25^\circ\text{C}$ .

### Switching Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Rise time	Common-emitter configuration, See Figure 3			100	200	ns
Fall time				25	100	ns
Rise time	Emitter-follower configuration, See Figure 4			100	200	ns
Fall time				40	100	ns

(1) All typical values, except for temperature coefficient, are at  $T_A = 25^\circ\text{C}$ .

PARAMETER MEASUREMENT INFORMATION



Figure 1. Operational Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



Figure 2. Amplifier Characteristics



NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 3. Common-Emitter Configuration



NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS



† Frequency variation ( $\Delta f$ ) is the change in oscillator frequency that occurs over the full temperature range.

Figure 5.



Figure 6.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL494CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	<a href="#">Samples</a>
TL494CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	<a href="#">Samples</a>
TL494CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	<a href="#">Samples</a>
TL494CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	TL494C	<a href="#">Samples</a>
TL494CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	<a href="#">Samples</a>
TL494CDRG3	PREVIEW	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	TL494C	
TL494CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494C	<a href="#">Samples</a>
TL494CJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI			
TL494CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL494CN	<a href="#">Samples</a>
TL494CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL494CN	<a href="#">Samples</a>
TL494CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494	<a href="#">Samples</a>
TL494CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL494	<a href="#">Samples</a>
TL494CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T494	<a href="#">Samples</a>
TL494CPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T494	<a href="#">Samples</a>
TL494CPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T494	<a href="#">Samples</a>
TL494CPWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI			
TL494CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T494	<a href="#">Samples</a>
TL494CPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T494	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL494CPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T494	<a href="#">Samples</a>
TL494ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	<a href="#">Samples</a>
TL494IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	<a href="#">Samples</a>
TL494IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	<a href="#">Samples</a>
TL494IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	TL494I	<a href="#">Samples</a>
TL494IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	<a href="#">Samples</a>
TL494IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL494I	<a href="#">Samples</a>
TL494IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL494IN	<a href="#">Samples</a>
TL494INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL494IN	<a href="#">Samples</a>
TL494MJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
TL494MJB	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL494CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL494CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL494CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL494CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL494IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL494IDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL494CDR	SOIC	D	16	2500	333.2	345.9	28.6
TL494CDR	SOIC	D	16	2500	367.0	367.0	38.0
TL494CDRG4	SOIC	D	16	2500	333.2	345.9	28.6
TL494CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TL494IDR	SOIC	D	16	2500	333.2	345.9	28.6
TL494IDRG4	SOIC	D	16	2500	333.2	345.9	28.6

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

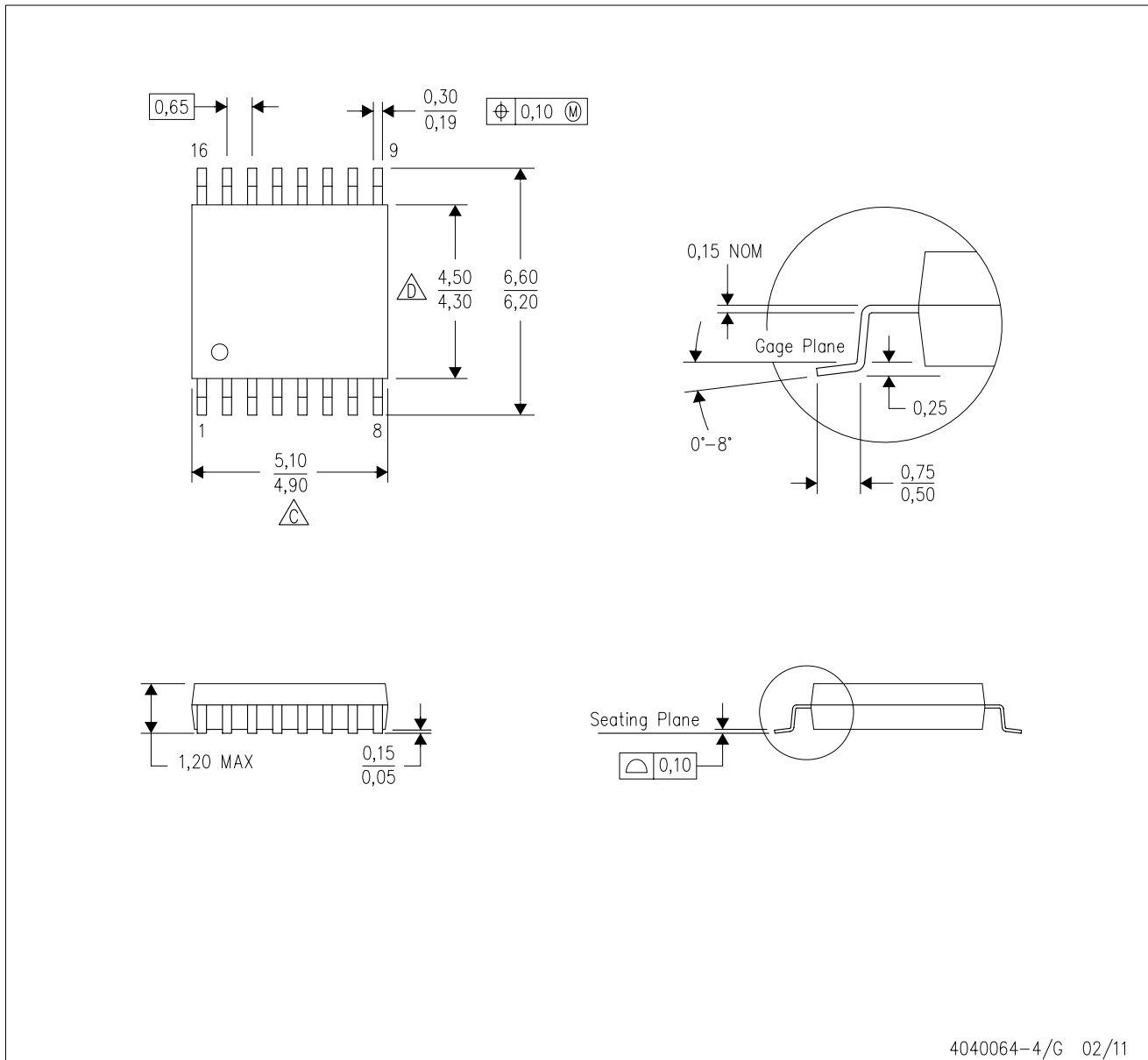


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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