VSMF SERIES: Multi-Frequency Voltage Control Crystal Oscillator with Low Jitter Output
10MHz – 1200MHz

PRODUCT DESCRIPTION

The VSMF clock series is a cutting edge family of High Frequency, Low Jitter Output, Multi-Frequency VCXO based on an advanced digital PLL platform. The VSMF oscillators are available in a 7x5mm ceramic package with output frequency from 10MHz to 1.2 GHz. The VSMF units are pre-programmed with up to 2 different output frequencies, any of which are user selected. Such flexibility significantly reduces design cycle time and overall cost. The VSMF oscillator design incorporates a low frequency crystal along with low Jitter frequency synthesizer to provide a wide range of frequencies. The VSMF Clocks are available in LVCMOS, LVPECL and LVDS outputs, making them suitable for a wide range of applications.

APPLICATION

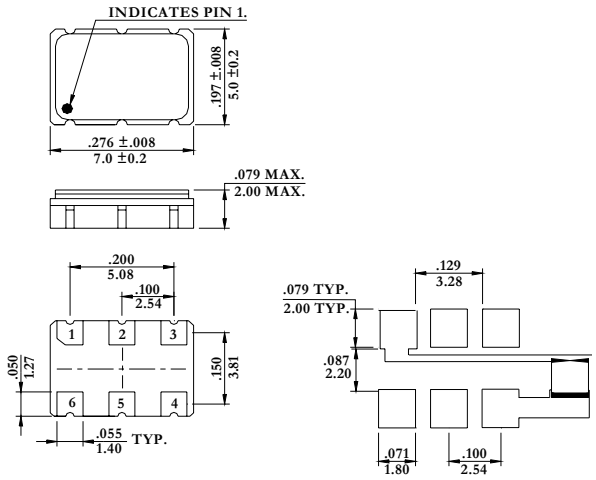
- SONET/SDH
- FIBRE CHANNEL
- 10G,100G, GIGABIT ETHERNET
- CLOCK / DATA RECOVERY
- TEST AND MEASUREMENT

ELECTRICAL SPECIFICATION

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Frequency, nominal	f_O	Up to 2 available output frequencies	10 -1200	MHz
Supply voltage, nom.	V_{CC}		2.5 or 3.3	V
Supply current	Is	Typical (depending on output)	35 ~ 45	mA
LVPECL output levels	VOH	Output termination 50Ω ~ Vcc - 2.0V	Vcc -1.4 ~ Vcc - 0.9	V
	VOL		Vcc - 2.0 ~ Vcc - 1.7	V
LVPECL output voltage swing	Vp-p	Output termination 50Ω ~ Vcc - 2.0V	0.6 ~ 1.0	V
LVDS differential output voltage	ΔV_{OD}	100Ω termination between outputs	350	mV
LVDS offset voltage, typical	V_{OS}		1.25	V
LVCMOS / LVTTL output levels	VOH / VOL	min/max	0.7Vcc / 0.3Vcc	V
Duty cycle	DC	Load = 10kΩ // 20pF	40/60 or 45/55	%
Rise/ fall time, max.	tr / tf	20% - 80% (VOL, VOH)	0.6	ns
Absolute Pull Range	APR	Min guaranteed freq. pull over Δf/fc	±32,50,80,100	ppm
Control Voltage	VC	Centered = ½ (Vcc)	1.25, 1.65	V
Control Voltage Range		Positive Slope; 10% Linearity, max	0.3 ~ 0.9 (Vcc)	V
Modulation Bandwidth, min	BW	-3dB	10	KHz
RMS phase jitter	J	Typical	0.8	ps
Overall freq. stability, max.[1]	Δf/fc	Various available, specified when ordered	±20 ~ ±100.	ppm
Enable / Disable	En / Dis	Min (logic 1) / Max (logic 0)	0.7 (Vcc) / 0.3 (Vcc)	V
Operating temperature	Ta		-40 ~ +85	°C
Storage temperature	T(stg)	Absolute max	-45 ~ +100	°C
Absolute voltage range	Vcc(abs)		Vcc ± 0.5	V

Notes
[1] See part numbering table
[2] Contact factory

MECHANICAL SPECIFICATION



SOLDER PATTERN

OUTLINE TOLERANCE
IF NOT SPECIFIED
±0.015" / 0.4mm

PIN FUNCTIONS:
[1] CONTROL VOLTAGE (**VC**) [2]
[2] FREQ. SELECT (**SEL**) [3]
[3] GROUND
[4] OUTPUT
[5] COMP. OUTPUT
[6] SUPPLY VOLTAGE

MARKING:
VSMF293 – (family)
ASH X-Y– (frequency codes)
R D/C – (factory date code)

***0.01uF external bypass capacitor is recommended as seen in solder pattern**

Notes
[2] V_C available on pin 1 or 2. See options on part numbering table.
[3] Frequency Select pin (SEL)
Logic 1 (NC) = Output Frequency 1 (First frequency listed in part # is automatically available. Customer specified at time of order)
Logic 0 = Output Frequency 2 (Second frequency listed in part # is available. Customer sets SEL pin to Low)

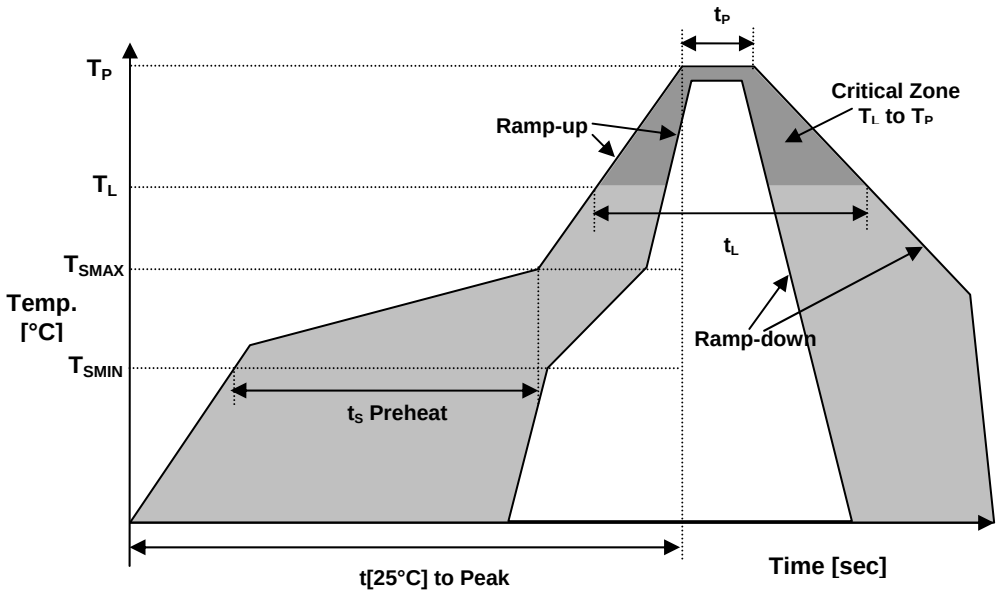
PART NUMBERING SYSTEM:

SERIES	NUMBER OF OUTPUTS	OUTPUT	SUPPLY VOLTAGE (V)	SYMMETRY (%)	TEMP RANGE (°C)	APR (ppm)	V_C and SEL Option		OUTPUT FREQUENCY (MHz)
Surface mount Multi-frequency Clock Oscillator	**1**: Single Output **2**: Dual Output	**9**: LVPECL **8**: LVDS **4**: LVCMOS	**1**: Vcc =2.5 **3**: Vcc =3.3	**A**: 40/60 **T**: 45/55	**R**: 0~50 **S**: 0~70 **U**: -20~70 **V**: -40~85	**F**: ±32 **H**:±50 **G**:±80 **J**:±100 [4]	**1**[5]: Pin 1= V_C **2**: Pin 1 = SEL		**XXX.XXX-YYY.YYY** Freq1- Freq 2
VSMF	**2**	**9**	**3**	**A**	**S**	**H**	**2**	**-**	**XXX-YYY**

Notes
[4] ± 100ppm APR may not be available with all frequencies and operating temperature ranges
[5] Pin 1= V_C is default configuration.

EXAMPLE: VSMF293ASH2-622-311
Clock Oscillator, 7x5mm package, Dual output, LVPECL, +3.3V Supply, 40/60 Symmetry, 0~+70°C Operating Temperature Range, ±50ppm APR, Select on pin 1, 622.080 MHz and 311.040MHz output frequency.

REFLOW PROFILE:



Reflow profile IPC/JEDEC J-STD-020 REV. C		
Temperature Min Preheat	T_{SMIN}	150°C
Temperature Max Preheat	T_{SMAX}	200°C
Time (T_{SMIN} to T_{SMAX})	t_S	60-180 sec.
Temperature	T_L	217°C
Peak Temperature	T_P	260°C
Ramp-up rate	R_{UP}	3°C/sec max.
Ramp-down rate	R_{DOWN}	6°C/sec max.
Time within 5°C of Peak Temperature	t_P	20-40 sec.
Time t[25°C] to Peak Temperature	t[25°C] to Peak	480 sec.
Time	t_L	60-150 sec.