ACT™ 3 3.3 Volt Field Programmable Gate Arrays

Features

- 3.3V Functionality fully compliant with JEDEC specifications
- Highly Predictable Performance with 100% Automatic Placement and Routing
- 13 ns Clock-to-Output Times
- Up to 100 MHz On-Chip Performance
- Up to 200 User-Programmable I/O Pins
- Four Fast, Low-Skew Clock Networks
- More Than 500 Macro Functions
- Up to 10,000 Gate Array Equivalent Gates (up to 25,000 equivalent PLD Gates)
- Replaces up to 250 TTL Packages
- Replaces up to 100 20-pin PAL® Packages
- Up to 1153 Dedicated Flip-Flops
- I/O Drive to 12 mA
- VQFP, TQFP, BGA, and PLCC Packages
- Nonvolatile, User Programmable
- Low-power 0.8 micron CMOS Technology
- Fully Tested Prior to Shipment

Product Family Profile

Device	A14V15A	A14V25A	A14V40A	A14V60A	A14V100A
Capacity					
Gate Array Equivalent Gates	1,500	2,500	4,000	6,000	10,000
PLD Equivalent Gates	3,750	6,250	10,000	15,000	25,000
TTL Equivalent Packages (40 gates)	40	60	100	150	250
20-Pin PAL Equivalent Packages (100 gates)	15	25	40	60	100
Logic Modules	200	310	564	848	1,377
S-Module	104	160	288	432	697
C-Module	96	150	276	416	680
Dedicated Flip-Flops[1]	264	360	568	768	1,153
User I/Os (maximum)	80	100	140	168	228
Packages[2] (by pin count)					
PLCC	84	84	84	—	—
PQFP	—	—	—	208	—
RQFP	—	—	—	—	208
VQFP	100	100	100	—	—
TQFP	—	—	176	176	—
BGA	—	—	—	—	313
Performance (maximum, worst-case commercial)					
Chip-to-Chip[3]	63 MHz	63 MHz	60 MHz	59 MHz	57 MHz
Accumulators (16-bit)	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz
Loadable Counter (16-bit)	56 MHz	56 MHz	56 MHz	52 MHz	52 MHz
Prescaled Loadable Counters (16-bit)	100 MHz	100 MHz	100 MHz	75 MHz	75 MHz
Datapath, Shift Registers	100 MHz	100 MHz	100 MHz	75 MHz	75 MHz
Clock-to-Output (pad-to-pad)	13.0 ns	13.0 ns	14.4 ns	15.0 ns	15.7 ns

Note:

1. *One flip-flop per S-Module, two flip-flops per I/O-Module.*
2. *See product plan on page 1-3 for package availability.*
3. *Clock-to-Output + Setup*

Description

The ACT 3 family, based on Actel's proprietary PLICE® antifuse technology and 0.8-micron double-metal, double-poly CMOS process, offers a high-performance programmable solution capable of 200 MHz on-chip performance and 6.5 nanosecond clock-to-output speeds. The ACT 3 family spans capacities from 1,500 to 10,000 gate array equivalent gates (up to 25,000 PLD gates), and offers very high pin-to-gate ratios, with up to 228 user I/Os for 10,000 gate designs.

Predictable Performance* (Worst-Case Commercial)

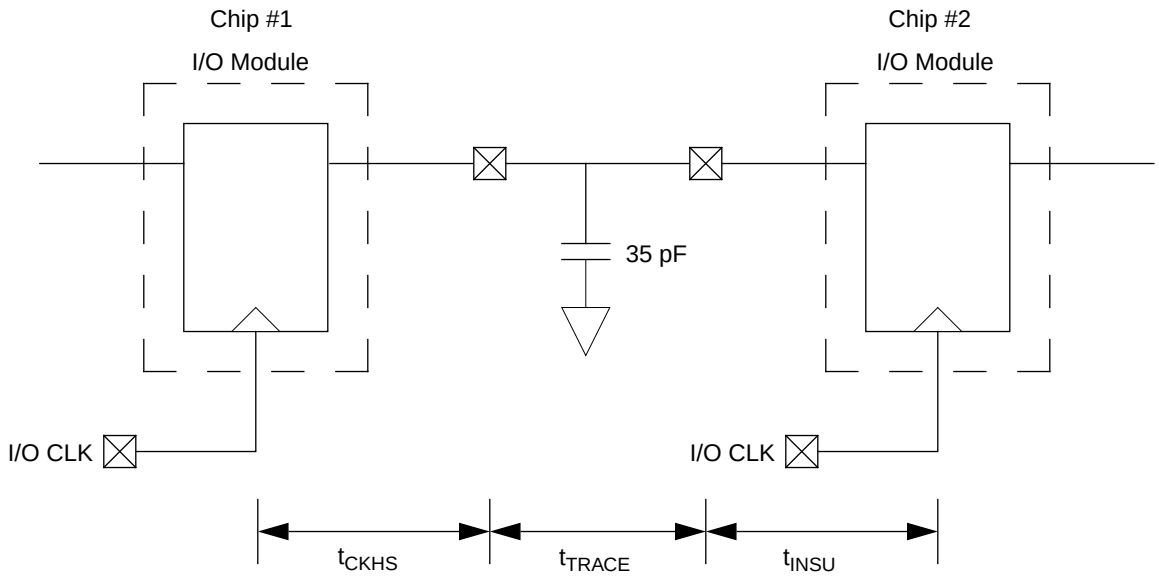
Accumulators (16-bit)	30–33 MHz
Loadable Counters (16-bit)	50–56 MHz
Prescaled Loadable Counters (16-bit)	90–100 MHz
Shift Registers	100–100 MHz

*See page 5 for further details.

The ACT 3 family represents the third generation of Actel Field Programmable Gate Arrays (FPGAs). The family improves on the proven ACT 2 family two-module architecture, consisting of combinatorial and sequential-combinatorial logic modules. The ACT 3 family offers registered I/O modules delivering 9 ns clock-to-out times. The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals like resets or output enables, reducing buffering requirements.

The ACT 3 family is supported by the Designer and Designer Advantage systems, allowing logic design implementation with minimum effort. The systems offer Microsoft® Windows™ and X Window™ graphical user interfaces and integrate with the resident CAE system to provide a complete gate array design environment: schematic capture, simulation, fully automatic placement and routing, timing verification and device programming. The systems also include the ACTmap™ optimization and synthesis tool, and the ACTgen™ Macro Builder, a powerful macro function generator for counters, adders, and other structured blocks. The systems are available for 386/486/Pentium PCs and for HP™, and Sun™ workstations running Viewlogic®, Mentor Graphics®, and OrCAD™ tools.

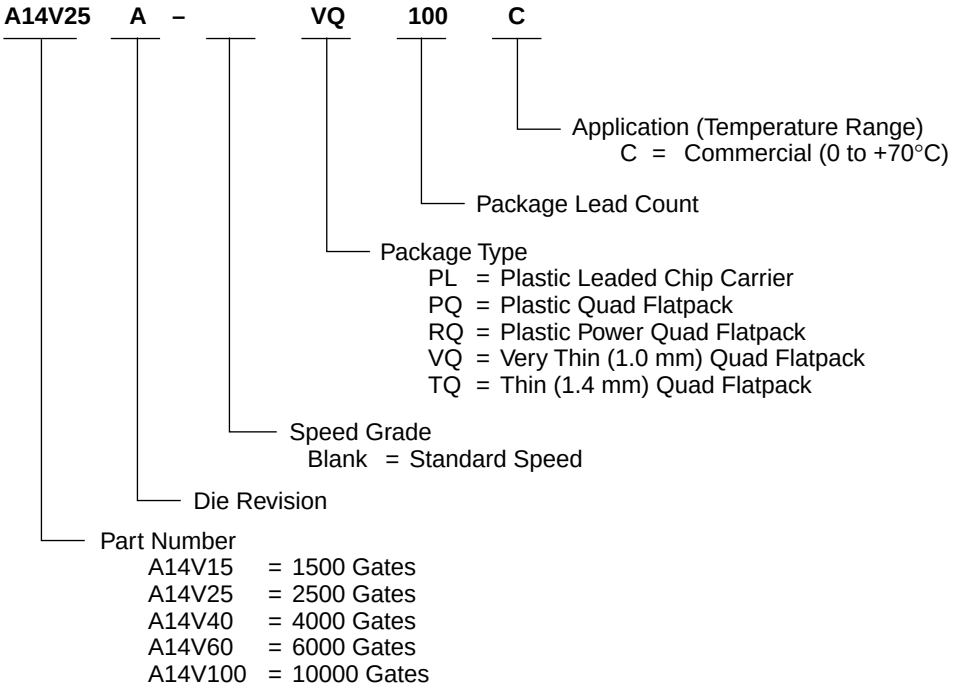
Chip-to-Chip Performance



Chip-to-Chip Performance (Worst-Case Commercial)

	t_{CKHS}	t_{TRACE}	t_{INSU}	Total	MHz
A14V25A	13.0	1.0	2.6	16.6	60
A14V60A	15.0	1.0	2.0	18.0	56

Ordering Information



Product Plan

	Speed Grade	Application
	Std	C
A14V15A Device		
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔
A14V25A Device		
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔
A14V40A Device		
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔
176-pin Thin Quad Flatpack (TQFP)	✔	✔
A14V60A Device		
176-pin Thin Quad Flatpack (TQFP)	✔	✔
208-pin Plastic Quad Flatpack (PQFP)	✔	✔
A14V100A Device		
208-pin Power Quad Flatpack (RQFP)	✔	✔
313-pin Plastic Ball Grid Array (BGA)	✔	✔

Applications: *C = Commercial*

Availability: ✔ = *Available*, *P* = *Planned*, — = *Not Planned.*

Plastic Device Resources

Device Series	Logic Modules	Gates	User I/Os				
			PLCC	PQFP, RQFP	VQFP	TQFP	BGA
			84-pin	208-pin	100-pin	176-pin	313-pin
A14V15A	200	1500	70	—	80	—	—
A14V25A	310	2500	70	—	83	—	—
A14V40A	564	4000	70	—	83	140	—
A14V60A	848	6000	—	167	—	151	—
A14V100A	1377	10000	—	175	—	—	228

Pin Description

CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

TTL Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

IOCLK Dedicated (Hard-wired) I/O Clock (Input)

TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-wired) I/O Preset/Clear (Input)

TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 3.3 V Supply Voltage

HIGH supply voltage.

V_{KS} Programming Voltage

Supply voltage used for device programming. This pin must be connected to GND during normal operation.

V_{PP} Programming Voltage

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

V_{SV} Programming Voltage

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

Architecture

This section of the data sheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 1.

Logic Modules

ACT 3 logic modules are enhanced versions of the ACT 2 family logic modules. As in the ACT 2 family, there are two types of modules: C-modules and S-modules. The C-module is functionally equivalent to the ACT 2 C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module. S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make

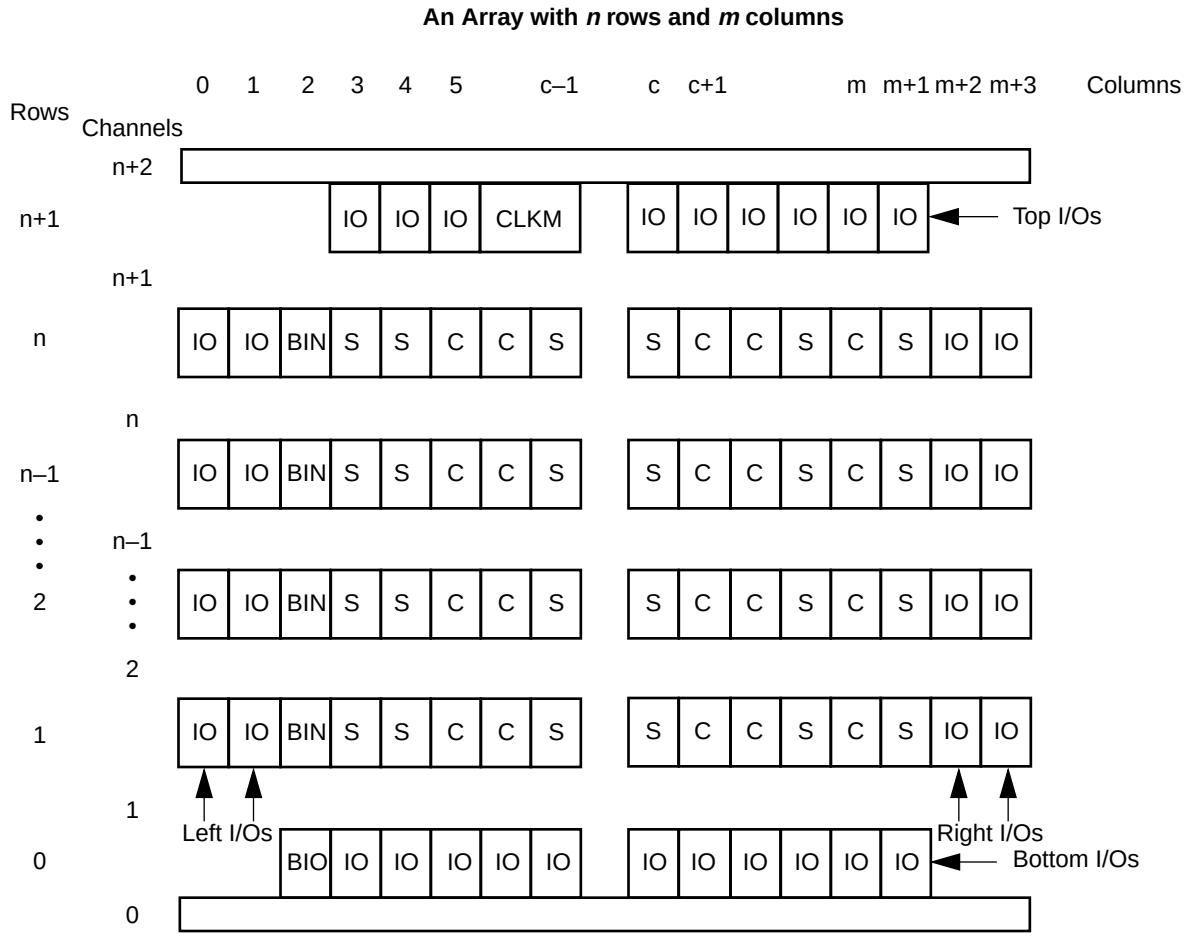


Figure 1 • *Generalized Floor Plan of ACT 3 Device*

up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11

where: S0 = A0 * B0 and S1 = A1 + B1

The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Action Logic System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLK0, CLK1, or HCLK. The C-module and S-module functional descriptions are shown in Figures 2 and 3. The clock selection multiplexor selects the clock input to the S-module.

I/Os

I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. There are two types of I/O modules: side and top/bottom. The I/O module schematic is shown in Figure 4. UO1 and UO2 are inputs from the routing channel, one for the routing channel above and one for the routing channel below the module. The top/bottom I/O modules interact with only one channel and therefore have only one UO input. The signals DataIn and DataOut connect to the I/O pad driver. Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

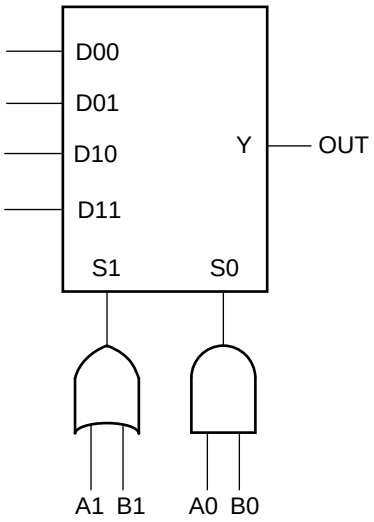


Figure 2 • *C-Module Diagram*

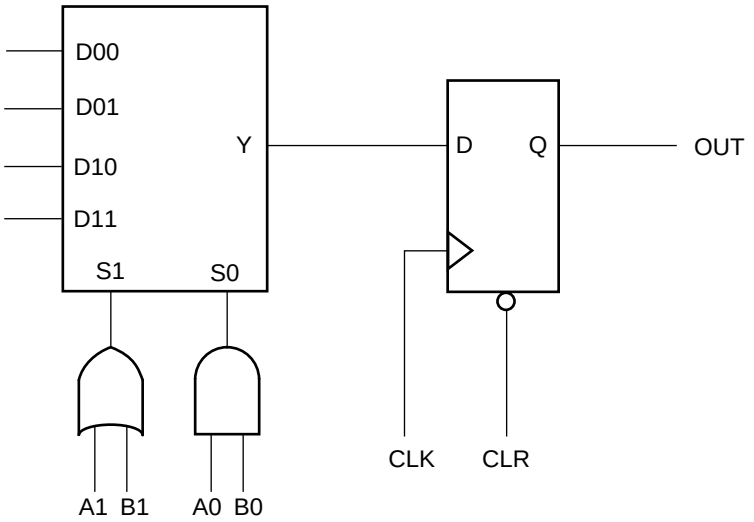


Figure 3 • *S-Module Diagram*

The I/O module output Y is used to bring Pad signals into the array *or* to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 5.

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 100 MHz, while the general purpose routed networks function up to 75 MHz.

Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver

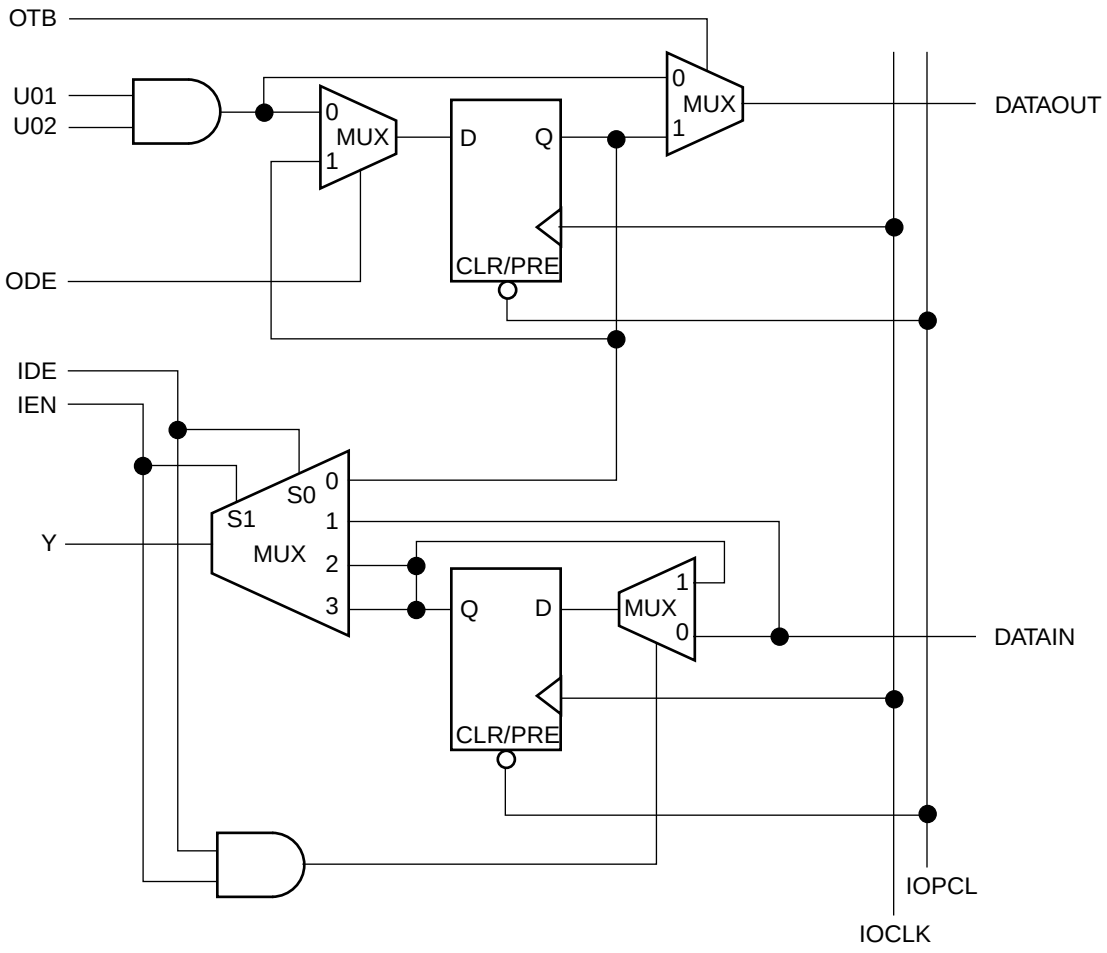


Figure 4 • *Functional Diagram for I/O Module*

to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

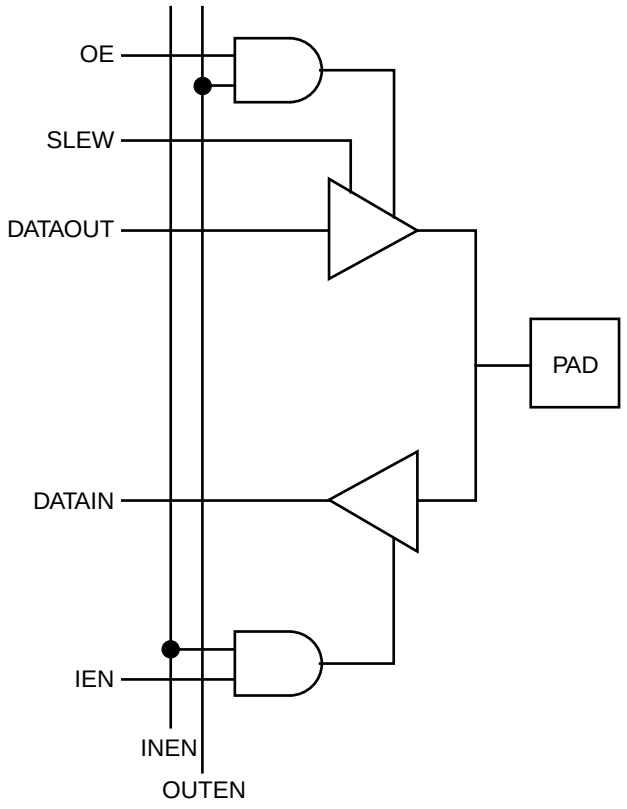


Figure 5 • *Function Diagram for I/O Pad Driver*

Routed Clocks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (see Figure 6):

- externally from the CLKA pad
- externally from the CLKB pad
- internally from the CLKINA input
- internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

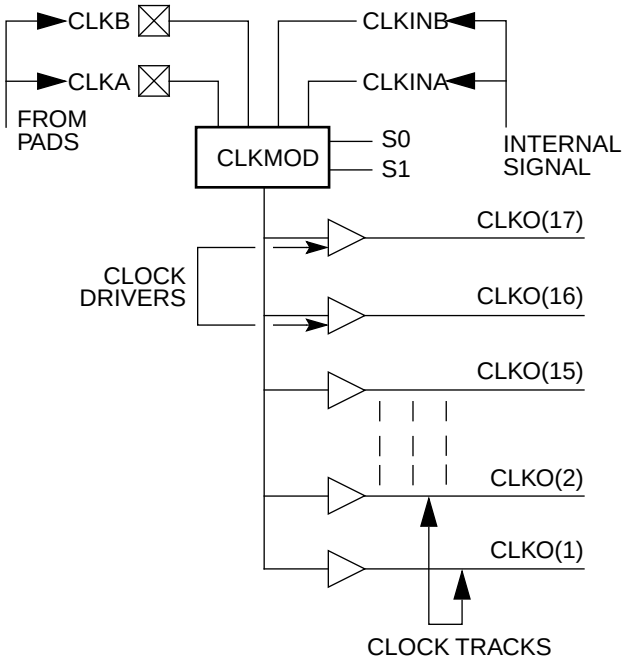


Figure 6 • *Clock Networks*

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where

edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 8.

Antifuse Connections

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.) Table 1 shows four types of antifuses.

Table 1 • *Antifuse Types*

XF	Horizontal-to-Vertical Connection
HF	Horizontal-to-Horizontal Connection
VF	Vertical-to-Vertical Connection
FF	"Fast" Vertical Connection

Examples of all four types of connections are shown in Figures 7 and 8.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below as shown in Figure 9.

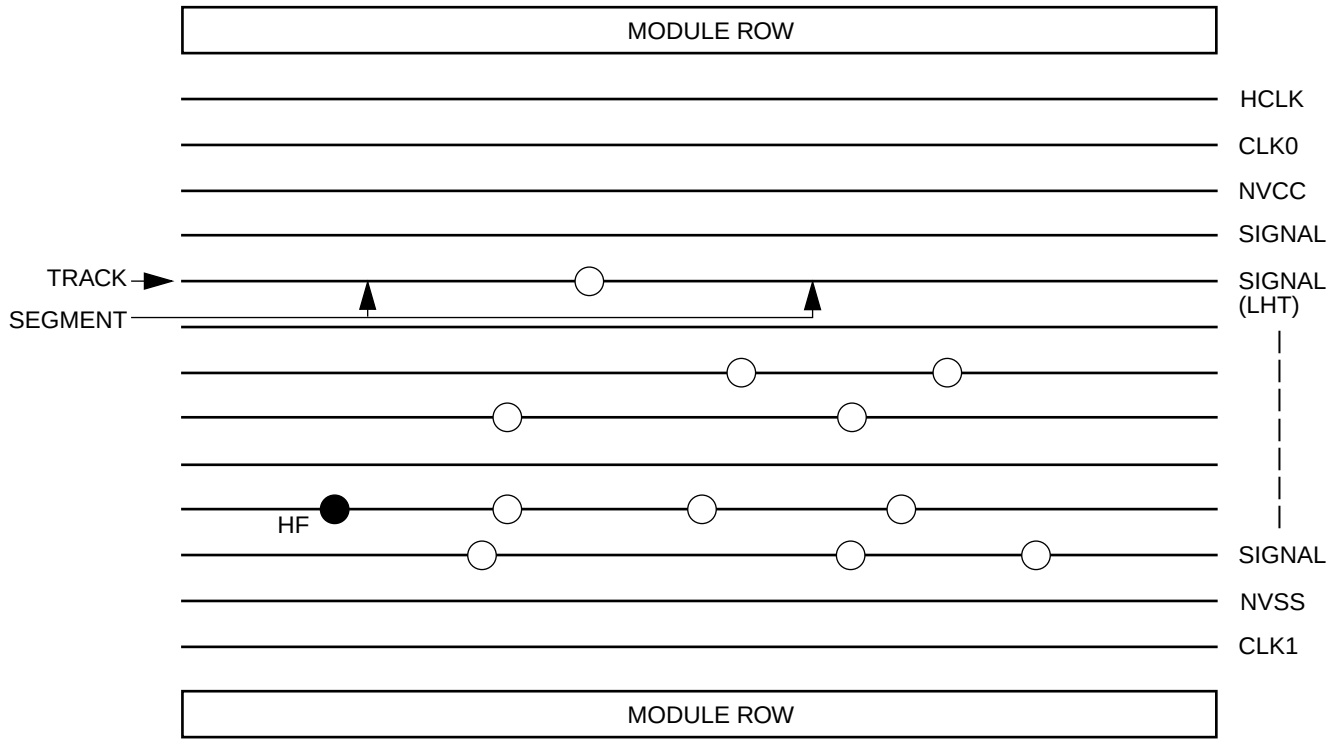


Figure 7 • *Horizontal Routing Tracks and Segments*

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 9, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe® circuits allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.

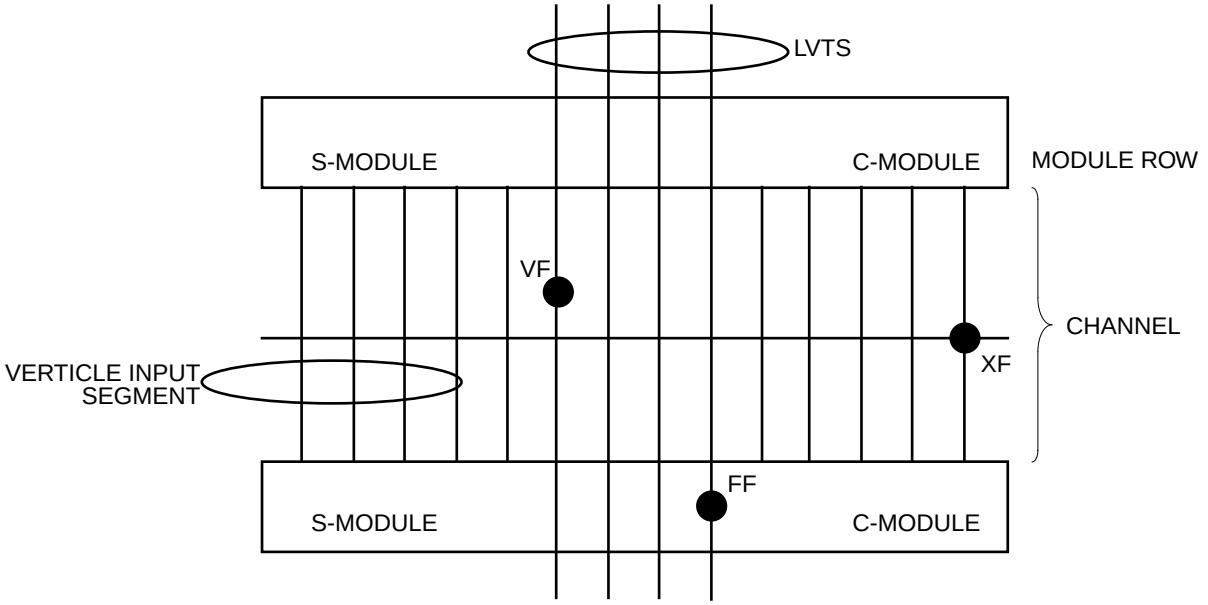


Figure 8 • *Vertical Routing Tracks and Segments*

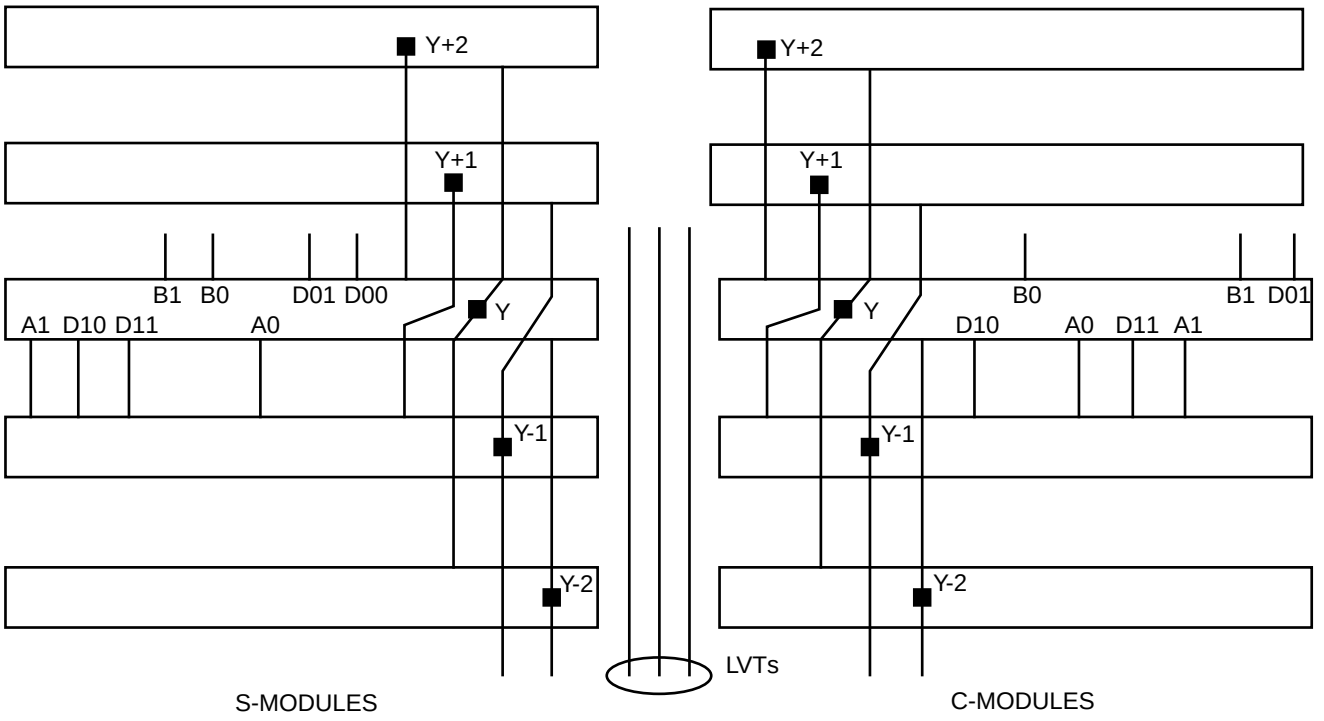


Figure 9 • *Logic Module Routing Interface*

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[3]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *V_{PP} , V_{SV} = V_{CC} , except during device programming.*
3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Units
Temperature Range[1]	0 to +70	°C
Power Supply Tolerance	3.0 to 3.6	V

Note:

1. *Ambient temperature (T_A) is used for commercial.*

Electrical Specifications

Parameter		Commercial		Units
		Min.	Max.	
V_{OH}[1]	(I_{OH} = –4 mA)	2.15		V
	(I_{OH} = –3.2 mA)	2.4		V
V_{OL}[1]	(I_{OL} = 6 mA)		0.4	V
V_{IL}		–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500	ns
C_{IO} I/O Capacitance[2, 3]			10	pF
Standby Current, I_{CC}[4] (typical = 0.3 mA)			0.75	mA
Leakage Current[5]		–10	10	µA

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
4. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = V_{CC} or GND.*
5. *V_O, V_{IN} = V_{CC} or GND.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a RQFP 208-pin package at commercial temperature and still air is as follows:

$$\text{Absolute Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{17°C/W} = 4.7\ W$$

Package Type	Pin Count	θja Still Air	θja 300 ft/min	Units
Plastic Quad Flatpack[1]	208	33	26	°C/W
Very Thin Quad Flatpack	100	43	35	°C/W
Thin Quad Flatpack	176	32	25	°C/W
Power Quad Flatpack	208	17	13	°C/W
Plastic Leaded Chip Carrier[2]	84	37	28	°C/W
Plastic Ball Grid Array	313	23	17	°C/W

Notes:

1. *Maximum Power Dissipation for 176-pin TQFP package is 2.5 Watts, 208-pin PQFP package is 2.4 Watts, and 100-pin VQFP package is 1.9 Watts.*
2. *Maximum Power Dissipation for PLCC package is 2.2 Watts, 208-pin RQFP package is 4.7 Watts, and 313-pin BGA packages is 3.5 Watts.*

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

Where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst case conditions.

I_{CC} V_{CC} Power

0.75 mA 3.6 V 2.70 mW (max)

0.30 mA 3.3 V 0.99 mW (typ)

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the

external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus

external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed in Equation 1.

$$\text{Power (uW)} = C_{EQ} * V_{CC}^2 * F \quad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC} active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

Modules (C_{EQM})5.7

Input Buffers (C_{EQI})5.4

Output Buffers (C_{EQO})7.8

Routed Array Clock Buffer Loads (C_{EQCR})1.4

Dedicated Clock Buffer Loads (C_{EQCD})0.6

I/O Clock Buffer Loads (C_{EQCI})0.7

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 show a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk} + (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}] \quad (2)$$

Where:

m=Number of logic modules switching at f_m

n=Number of input buffers switching at f_n

p=Number of output buffers switching at f_p

q_1=Number of clock loads on the first routed array clock

q_2=Number of clock loads on the second routed array clock

r_1=Fixed capacitance due to first routed array clock

r_2=Fixed capacitance due to second routed array clock

s_1=Fixed number of clock loads on the dedicated array clock

s_2=Fixed number of clock loads on the dedicated I/O clock

C_{EQM}=Equivalent capacitance of logic modules in pF

C_{EQI}=Equivalent capacitance of input buffers in pF

C_{EQO}=Equivalent capacitance of output buffers in pF

C_{EQCR}=Equivalent capacitance of routed array clock in pF

C_{EQCD}=Equivalent capacitance of dedicated array clock in pF

C_{EQCI}=Equivalent capacitance of dedicated I/O clock in pF

C_L=Output lead capacitance in pF

f_m=Average logic module switching rate in MHz

f_n=Average input buffer switching rate in MHz

f_p=Average output buffer switching rate in MHz

f_{q1}=Average first routed array clock rate in MHz

f_{q2}=Average second routed array clock rate in MHz

f_{s1}=Average dedicated array clock rate in MHz

f_{s2}=Average dedicated I/O clock rate in MHz

Fixed Capacitance Values for Actel FPGAs (pF)

r_1 r_2
Device Typerouted clock 1routed clock 2

A14V15A5757

A14V25A7272

A14V40A100100

A14V60A157157

A14V100A185185

Fixed Clock Loads

S_1 S_2
Device Typededicated array clockdedicated I/O clock

A14V15A10480

A14V25A160100

A14V40A288140

A14V60A432168

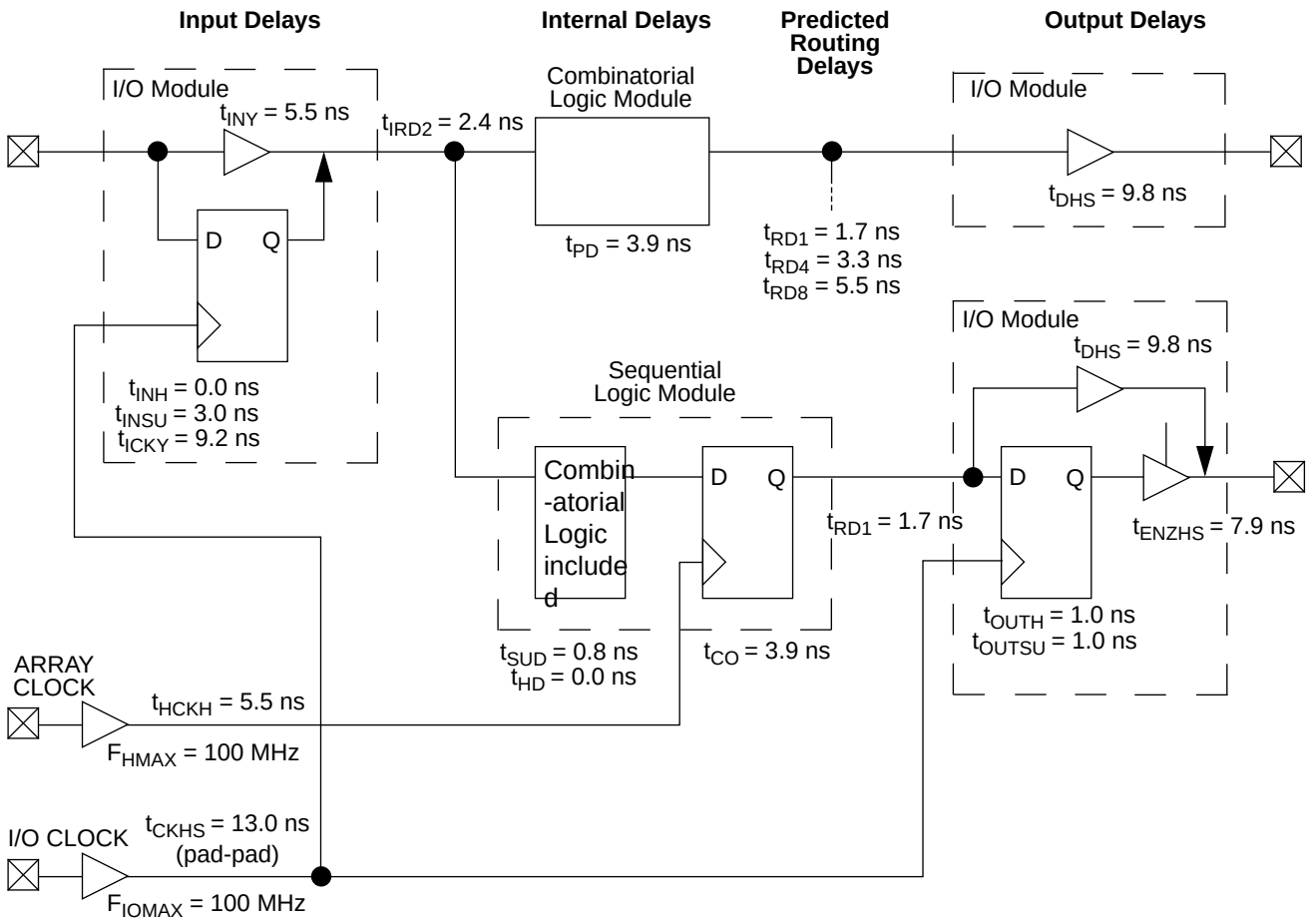
A14V100A697228V

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

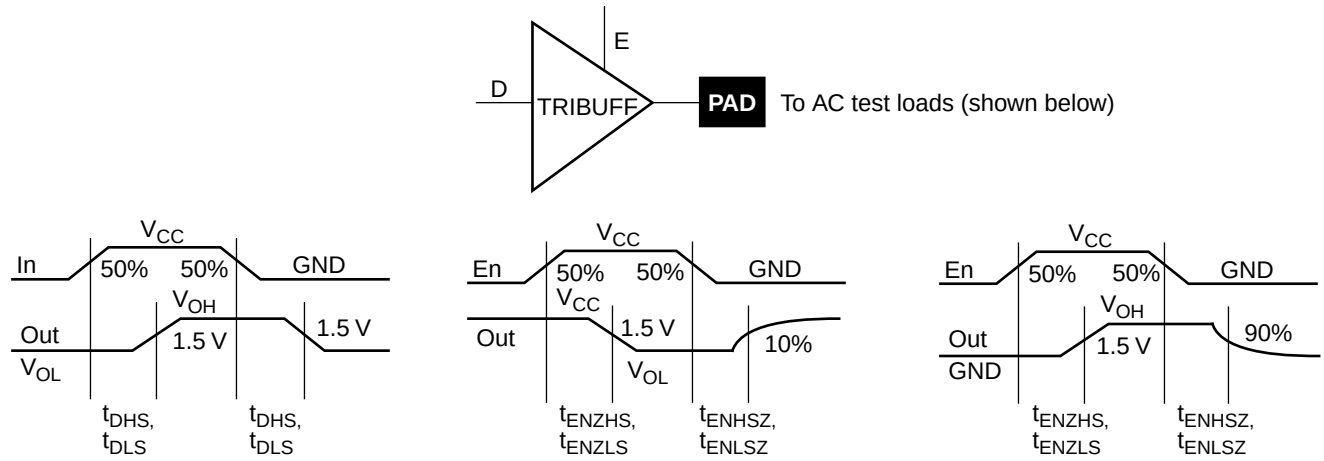
Logic Modules (m)	80% of modules
Inputs switching (n)	# inputs/4
Outputs switching (p)	# output/4
First routed array clock loads (q_1)	40% of sequential modules
Second routed array clock loads (q_2)	40% of sequential modules
Load capacitance (C_L)	35 pF
Average logic module switching rate (f_m)	F/10
Average input switching rate (f_n)	F/5
Average output switching rate (f_p)	F/10
Average first routed array clock rate (f_{q1})	F/2
Average second routed array clock rate (f_{q2})	F/2
Average dedicated array clock rate (f_{s1})	F
Average dedicated I/O clock rate (f_{s2})	F

ACT 3 Timing Model*



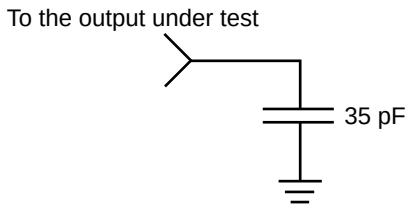
**Values shown for A14V25A.*

Output Buffer Delays

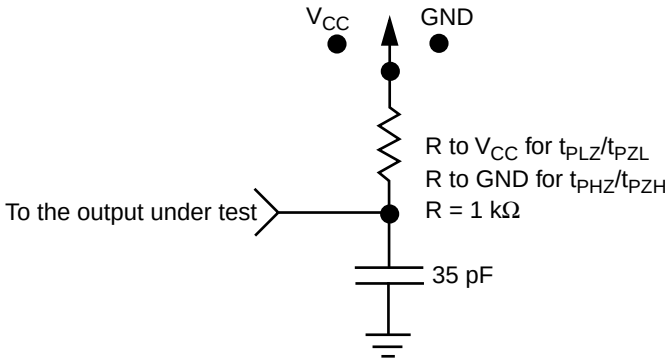


AC Test Loads

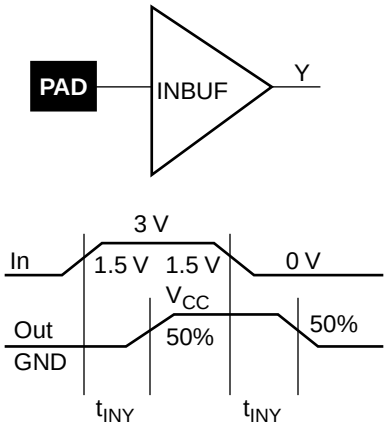
Load 1
(Used to measure propagation delay)



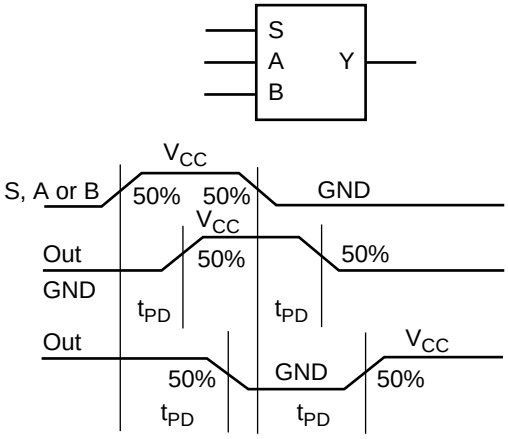
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

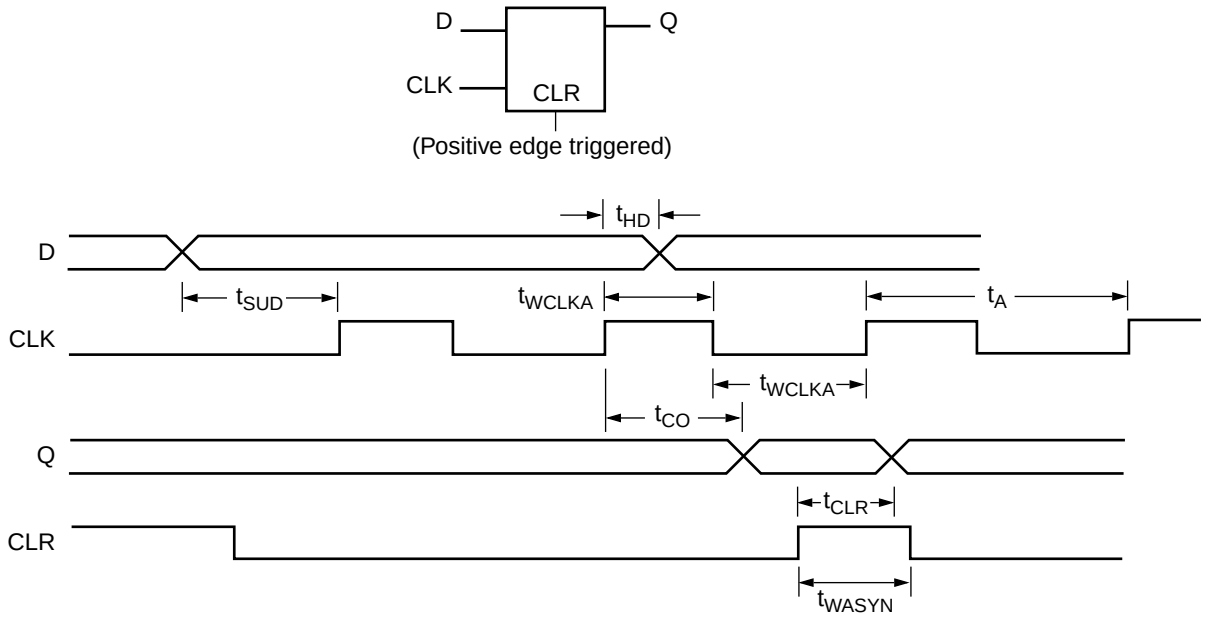


Module Delays

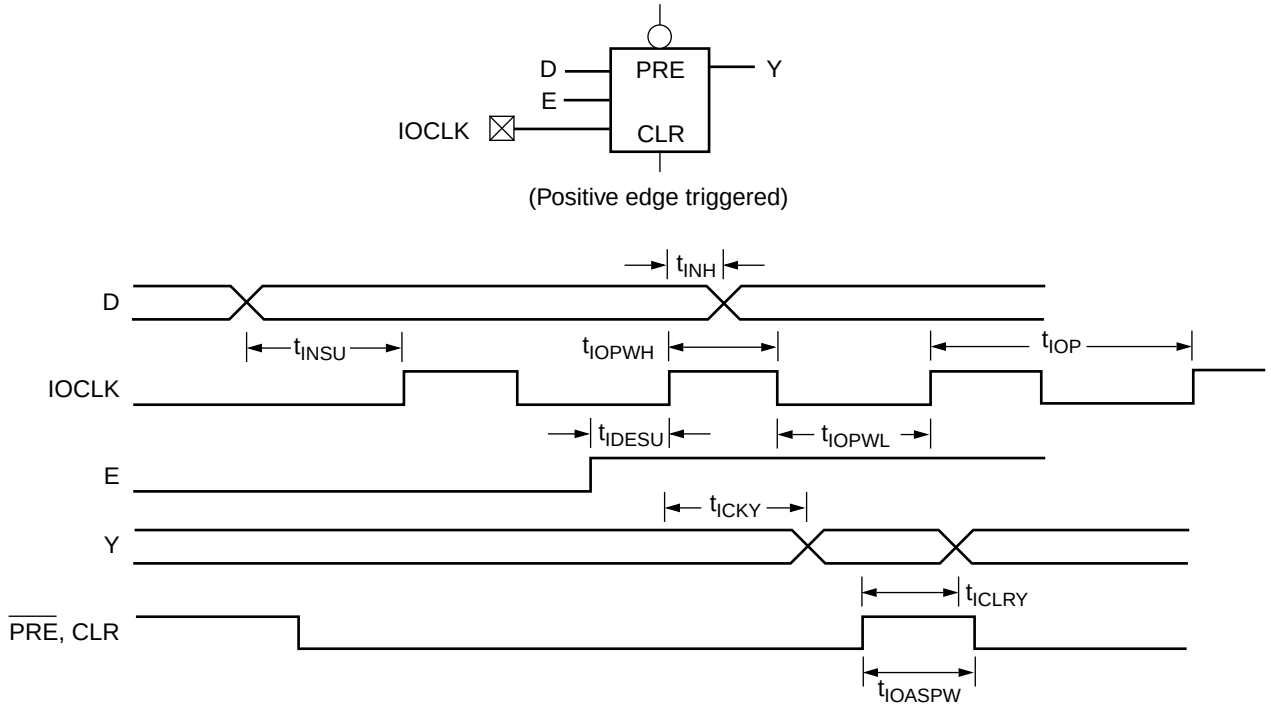


Sequential Module Timing Characteristics

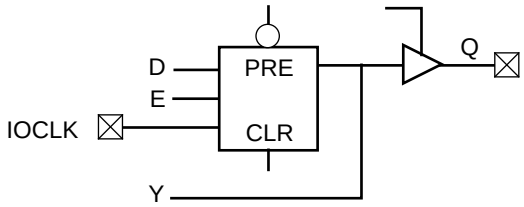
Flip-Flops



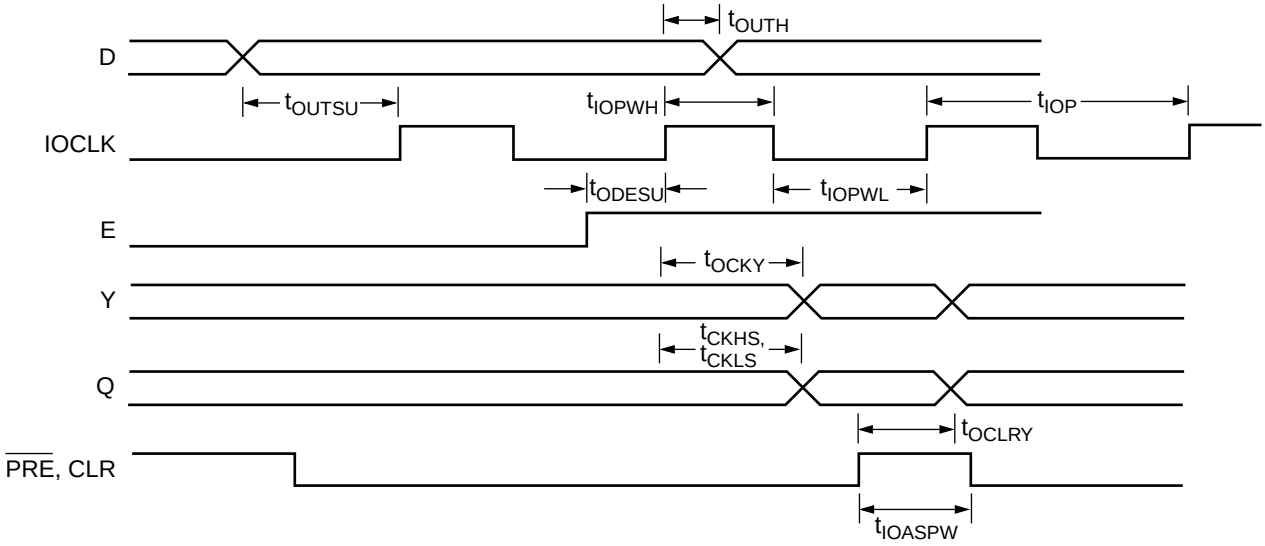
I/O Module: Sequential Input Timing Characteristics



I/O Module: Sequential Output Timing Characteristics



(Positive edge triggered)



Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximatley 4 ns to 14 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

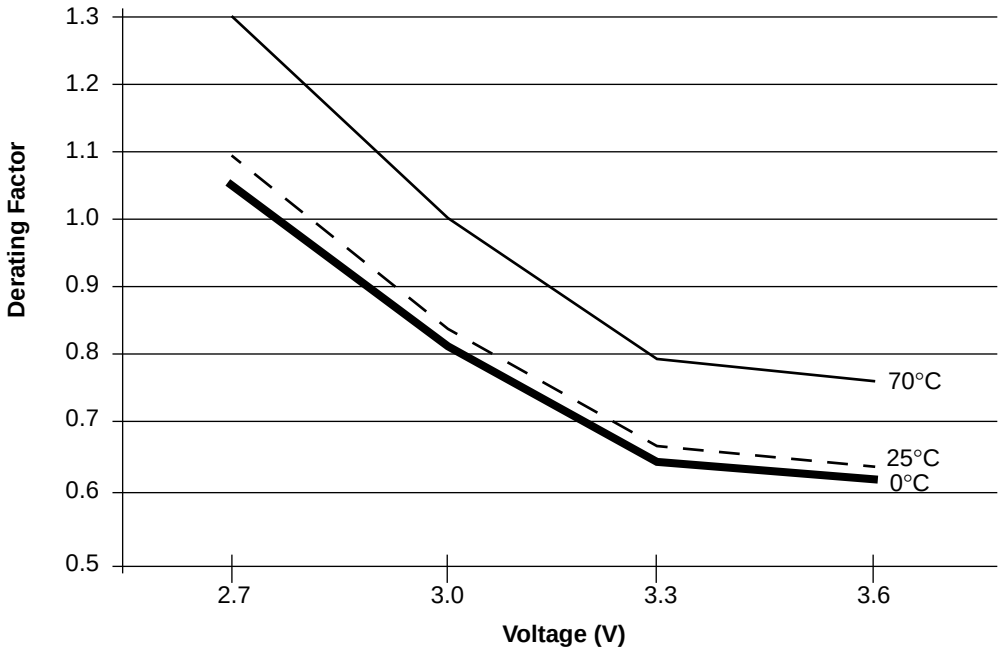
ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

ACT 3 Timing Model*

Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, T_J = 3.0 V, 70°C)

	0	25	70
2.7	1.05	1.09	1.30
3.0	0.81	0.84	1.00
3.3	0.64	0.67	0.79
3.6	0.62	0.64	0.76

Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, T_J = 3.0 V, 70°C)



Note: *This derating factor applies to all routing and propagation delays.*