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FIRENZE

CPU : Dothan533
Chip Set : ALVISO & ICH6-M
Remarks : EXTERNAL GFX

Model Name : FIRENZE
PBA Name : MAIN
PCB Code : BA41-00509A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2005.06.07

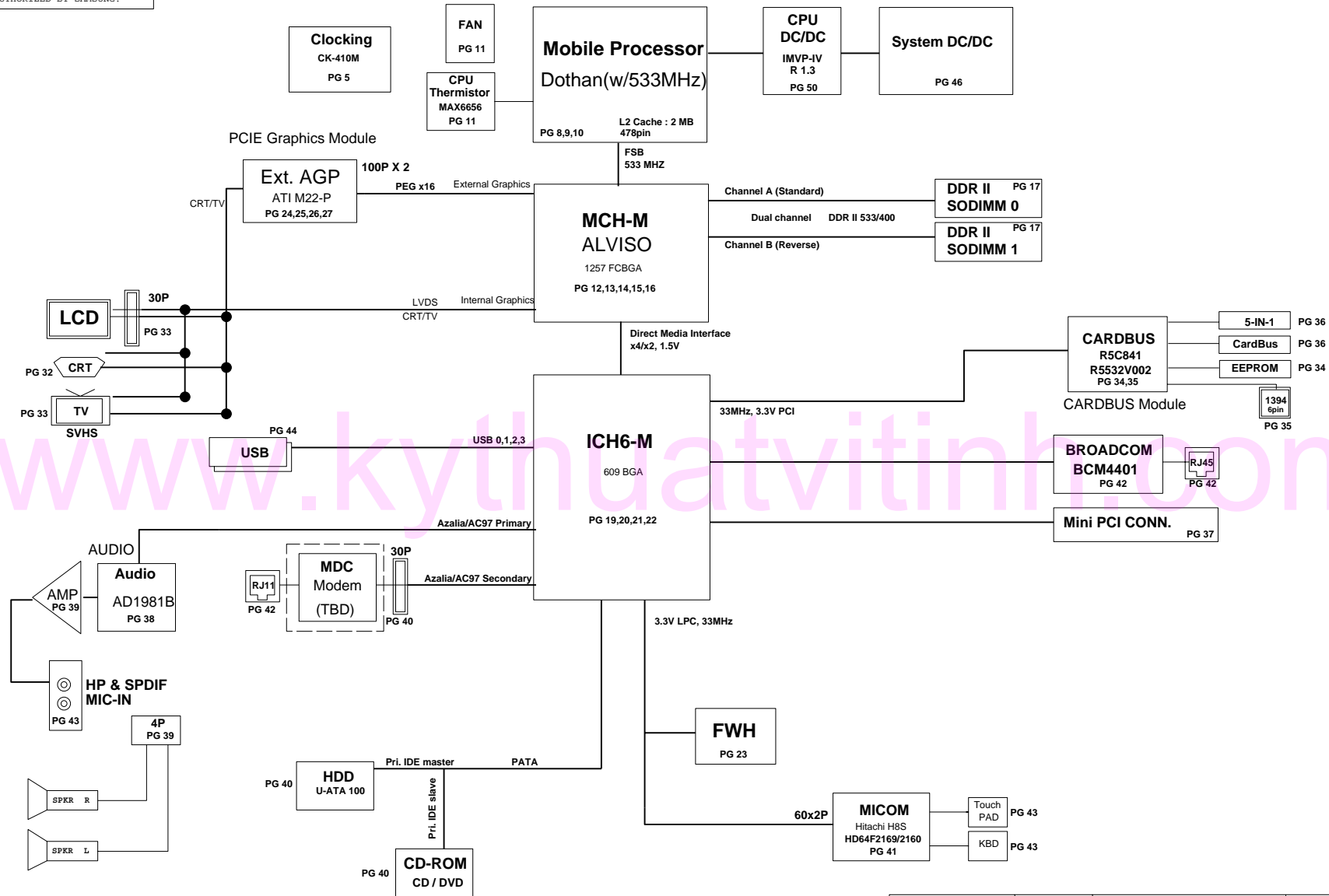
DRAW	CHECK	APPROVAL
SON, C. W	YUN, C. Y	LIM, J. G

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DRAW	SON, C. W	DATE	6/15/2005	TITLE	FIRENZE MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	MP			
APPROVAL	LIM, J. G	REV	1.0			
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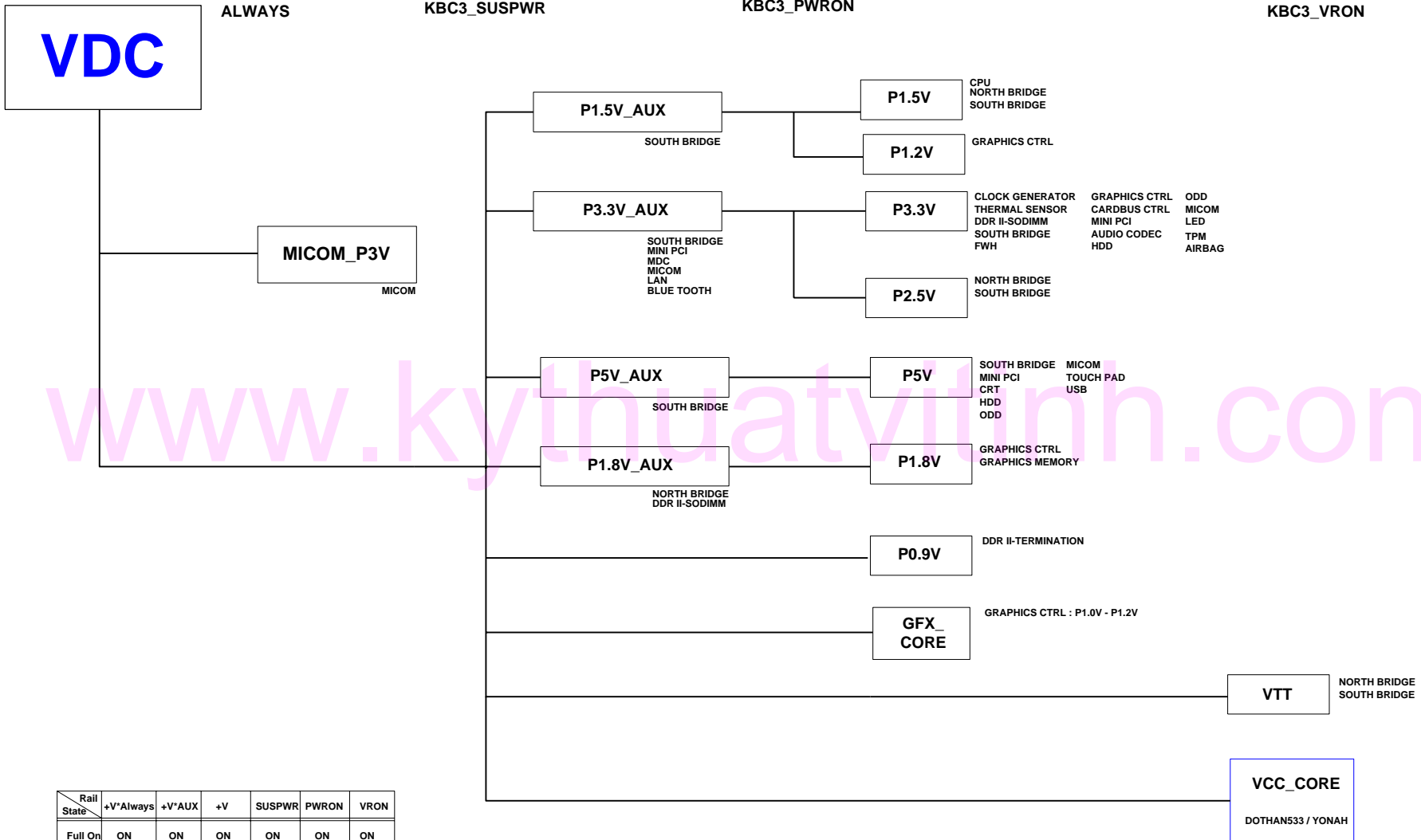
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Power Diagram



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF	OFF
S4	ON	OFF	OFF	OFF	OFF	OFF
S5	ON	OFF	OFF	OFF	OFF	OFF

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

DEVICES	IDSEL#	REQ/GNT#	INTERRUPTS
CARDBUS CONTROLLER	AD25	0	A, B, C
MINIPCI	AD23	1	E, F
LAN CONTROLLER	AD21	2	G

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core voltage for DOTHAN (0.7-1.708V)
VTT	DOZHAN/ALVISO Processor System Bus(PSB) Termination (1.05V)
GFX_CORE	MCH-M Core Voltage (off in S3-S5) ATI M24-P Core Voltage (1.0-1.2V) (off in S3-S5)
P0.9V	0.9V power rail (off in S3-S5)
P1.2V	1.2V power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	1	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	1	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	1	0	0	0	1	1.164 V
0	0	0	0	1	1	1.660 V	1	1	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	1	0	0	1	0	1.132 V
0	0	0	1	0	1	1.628 V	1	1	0	0	1	0	1.116 V
0	0	0	1	1	0	1.612 V	1	1	0	0	1	1	1.100 V
0	0	0	1	1	1	1.596 V	1	1	0	0	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	1	0	1	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	1	0	1	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	1	0	1	0	1	1.036 V
0	0	1	0	1	1	1.532 V	1	1	0	1	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	1	0	1	1	0	1.004 V
0	0	1	1	0	1	1.500 V	1	1	0	1	1	0	0.988 V
0	0	1	1	1	0	1.484 V	1	1	0	1	1	1	0.972 V
0	0	1	1	1	1	1.468 V	1	1	0	1	1	1	0.956 V
0	0	1	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V
Highest Freq.	0	1	0	1	1	1.356 V	1	1	0	1	1	0	0.844 V
	0	1	0	1	1	1.340 V	1	1	0	1	1	1	0.828 V
	0	1	1	0	0	1.324 V	1	1	1	0	0	0	0.812 V
	0	1	1	0	0	1.308 V	1	1	1	0	0	1	0.796 V
	0	1	1	0	1	1.292 V	1	1	1	0	1	0	0.780 V
	0	1	1	0	1	1.276 V	1	1	1	0	1	1	0.764 V
	0	1	1	1	0	1.260 V	1	1	1	1	0	0	0.748 V
	0	1	1	1	0	1.244 V	1	1	1	1	0	1	0.732 V
	0	1	1	1	1	1.228 V	1	1	1	1	1	0	0.716 V
	0	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V
													Lowest Freq.
													Deeper Sleep

IC / SMB Address

Devices	Address	Hex	Bus
SOUTH BRIDGE	Master	-	SMBUS Master
ADM1032(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
1,3	SYSTEM PORT A
0,2	SYSTEM PORT B

System Power States

- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

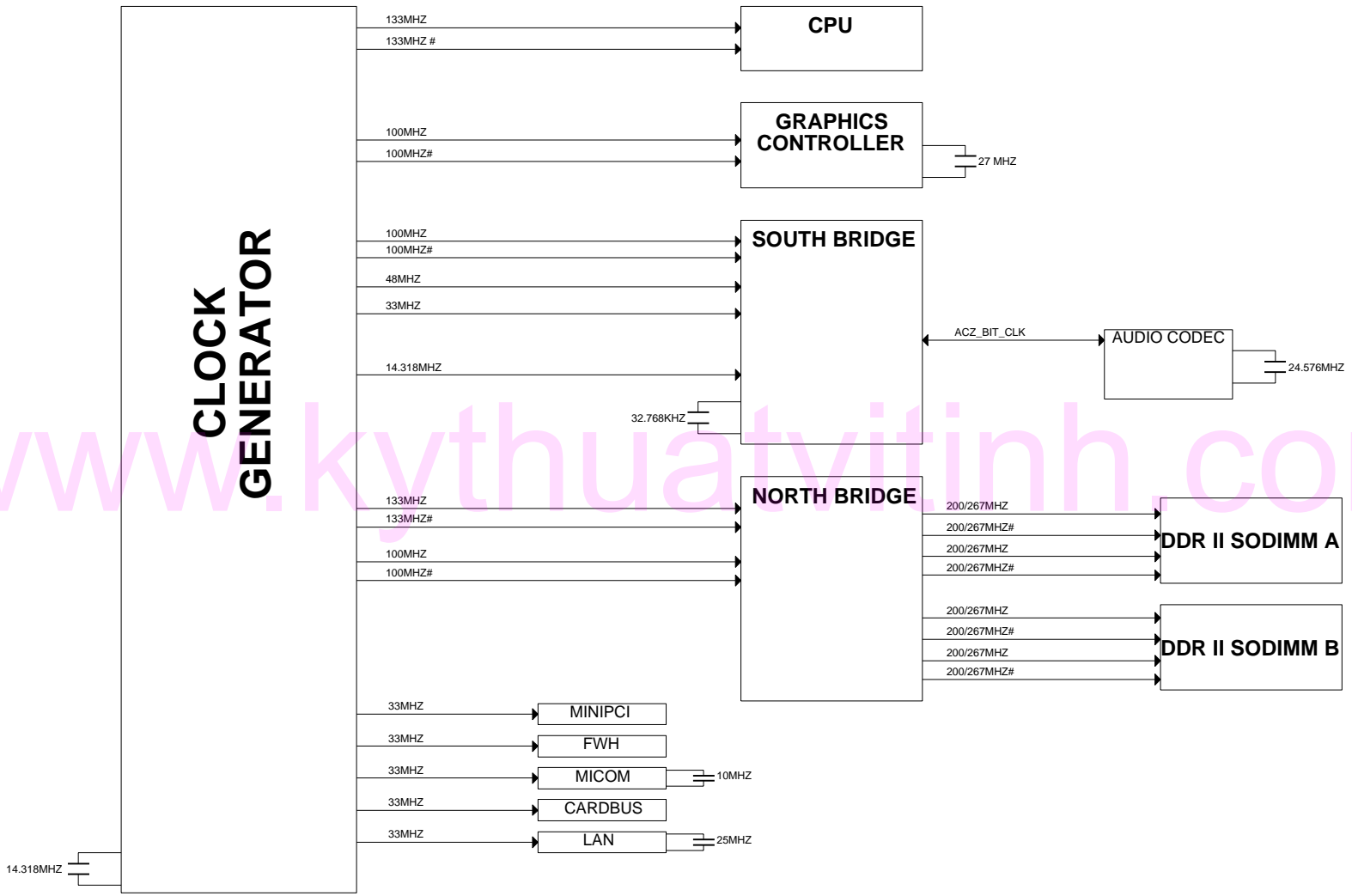
REVISION HISTORY

See rev notes in the changes file for more information.

MiniPCI SLOT1

DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	MP		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0		BOARD INFORMATION	PART NO. BA41-00509A
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	4	OF 55

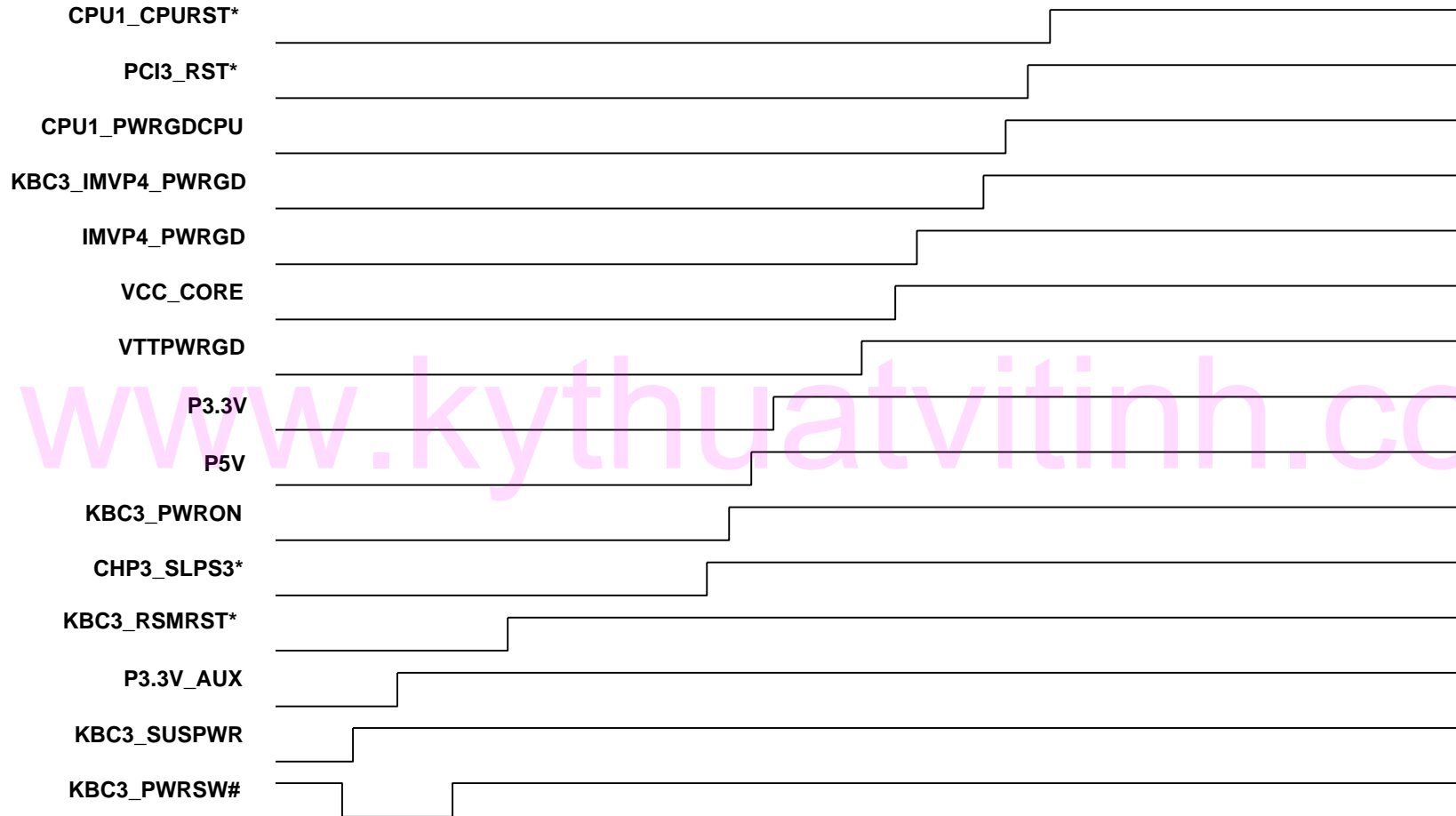
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RESET DIAGRAM



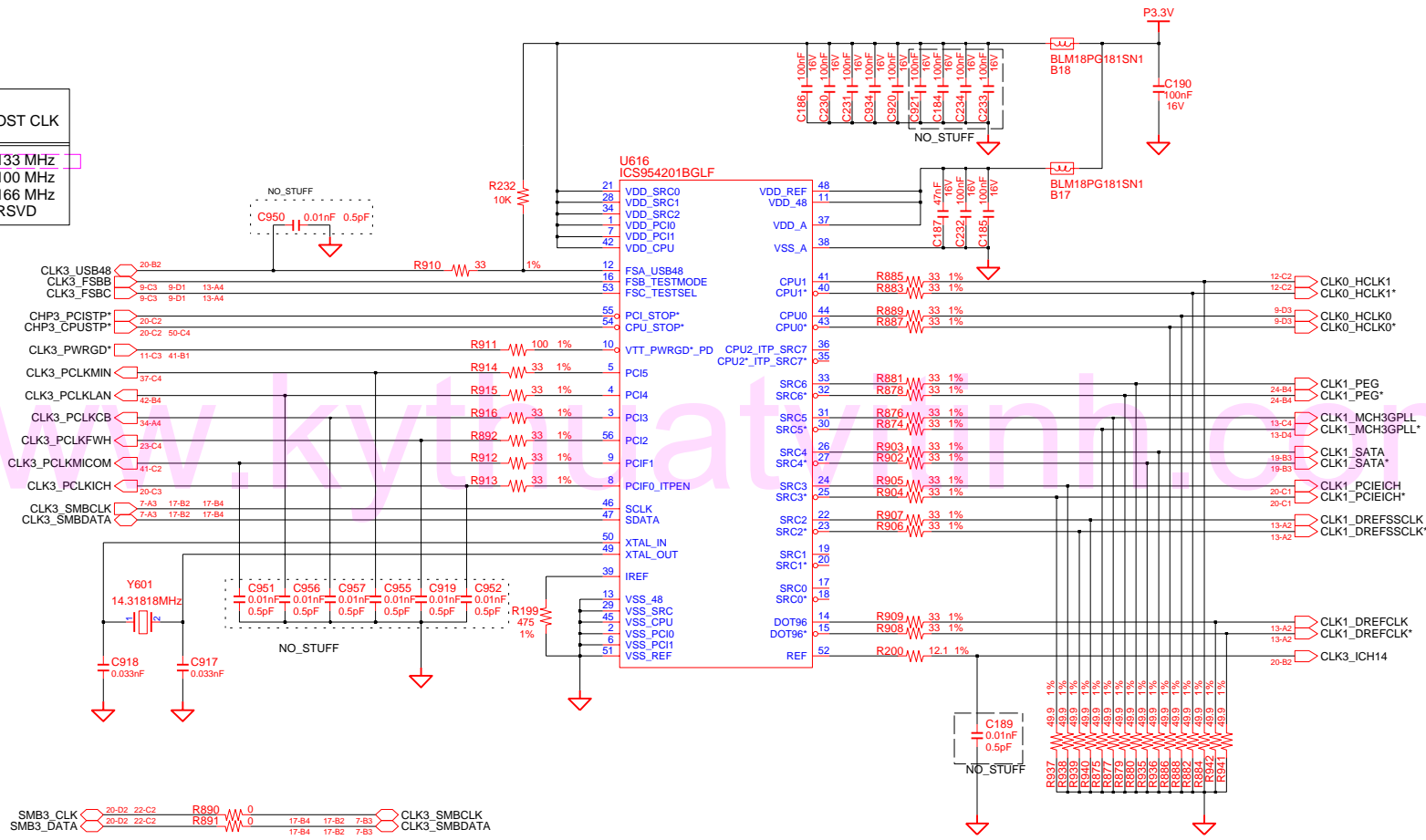
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN RESET DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00509A
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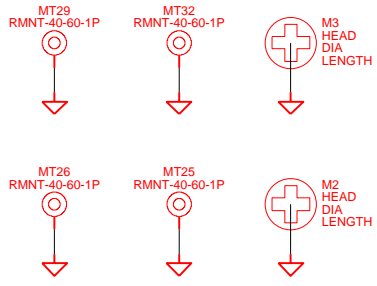
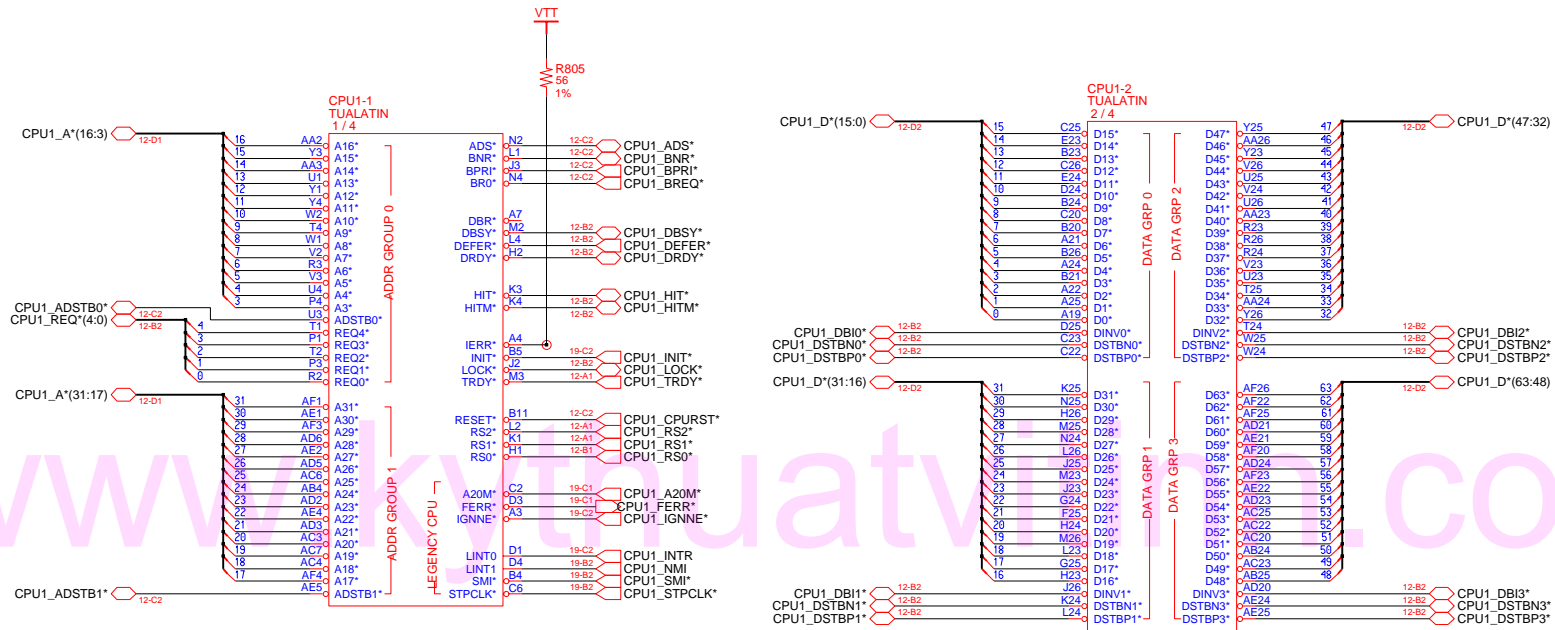
FSA	FSB	FSC	HOST CLK
BSEL2	BSEL1	BSEL0	
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



SMB3_CLK	20-D2	22-C2	R890	0	17-B4	17-B2	7-B3	CLK3_SMBCLK
SMB3_DATA	20-D2	22-C2	R891	0	17-B4	17-B2	7-B3	CLK3_SMBDATA

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CHECK	YUN, C.Y	DEV. STEP	MP	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	7 OF 55	PART NO. BA41-00509A

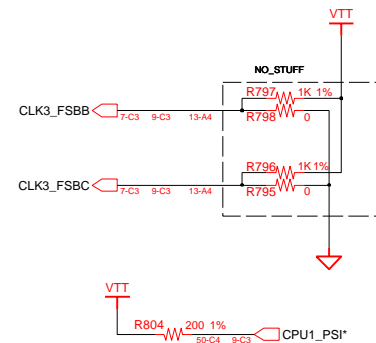
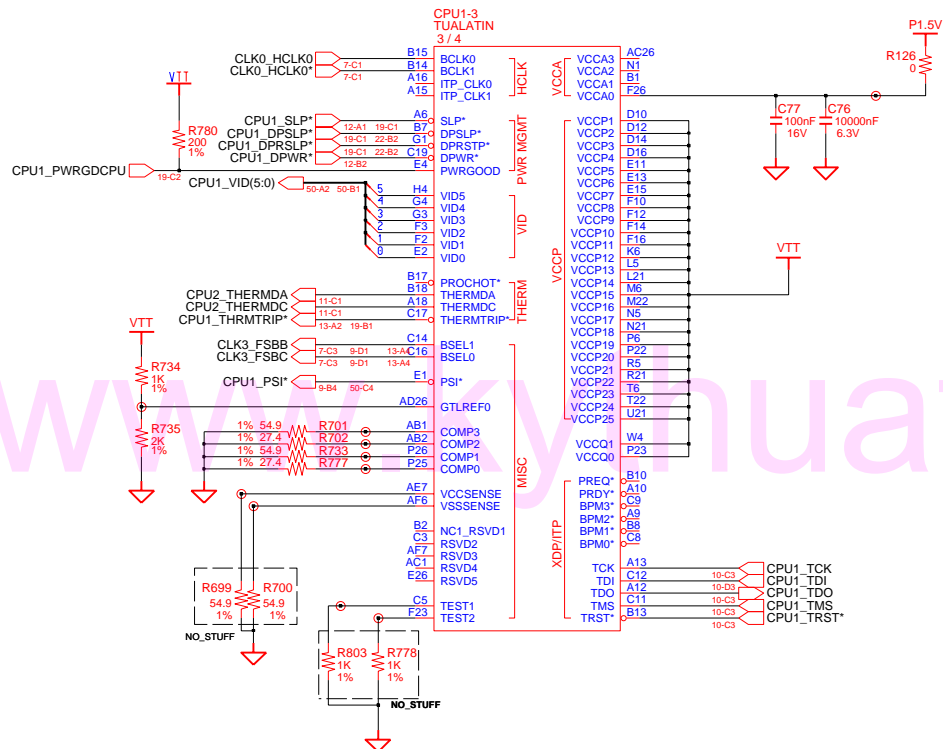
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CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0	1.708 V	1 0 0 0 0	1.196 V
0 0 0 0 1	1.692 V	1 0 0 0 1	1.180 V
0 0 0 1 0	1.676 V	1 0 0 1 0	1.164 V
0 0 0 1 1	1.660 V	1 0 0 1 1	1.148 V
0 0 1 0 0	1.644 V	1 0 1 0 0	1.132 V
0 0 1 0 1	1.628 V	1 0 1 0 1	1.116 V
0 0 1 1 0	1.612 V	1 0 1 1 0	1.100 V
0 0 1 1 1	1.596 V	1 0 1 1 1	1.084 V
0 1 0 0 0	1.580 V	1 0 1 0 0	1.068 V
0 1 0 0 1	1.564 V	1 0 1 0 1	1.052 V
0 1 0 1 0	1.548 V	1 0 1 1 0	1.036 V
0 1 0 1 1	1.532 V	1 0 1 1 1	1.020 V
0 1 1 0 0	1.516 V	1 0 1 1 0	1.004 V
0 1 1 0 1	1.500 V	1 0 1 1 1	0.988 V
0 1 1 1 0	1.484 V	1 0 1 1 1	0.972 V
0 1 1 1 1	1.468 V	1 0 1 1 1	0.956 V
0 1 0 0 0	1.452 V	1 1 0 0 0	0.940 V
0 1 0 0 1	1.436 V	1 1 0 0 1	0.924 V
0 1 0 1 0	1.420 V	1 1 0 1 0	0.908 V
0 1 0 1 1	1.404 V	1 1 0 1 1	0.892 V
0 1 1 0 0	1.388 V	1 1 0 1 0	0.876 V
0 1 1 0 1	1.372 V	1 1 1 0 0	0.860 V
0 1 1 1 0	1.356 V	1 1 1 0 1	0.844 V
0 1 1 1 1	1.340 V	1 1 1 1 1	0.828 V
0 1 1 0 0	1.324 V	1 1 1 0 0	0.812 V
0 1 1 0 1	1.308 V	1 1 1 0 1	0.796 V
0 1 1 1 0	1.292 V	1 1 1 1 0	0.780 V
0 1 1 1 1	1.276 V	1 1 1 1 1	0.764 V
0 1 1 1 0	1.260 V	1 1 1 1 1	0.748 V
0 1 1 1 1	1.244 V	1 1 1 1 0	0.732 V
0 1 1 1 0	1.228 V	1 1 1 1 1	0.716 V
0 1 1 1 1	1.212 V	1 1 1 1 1	0.700 V

Highest Freq. of Dothan400(1.8GHz)
* Highest Freq. of Dothan533(?? GHz : TBD)

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4

3

2

1

D

C

B

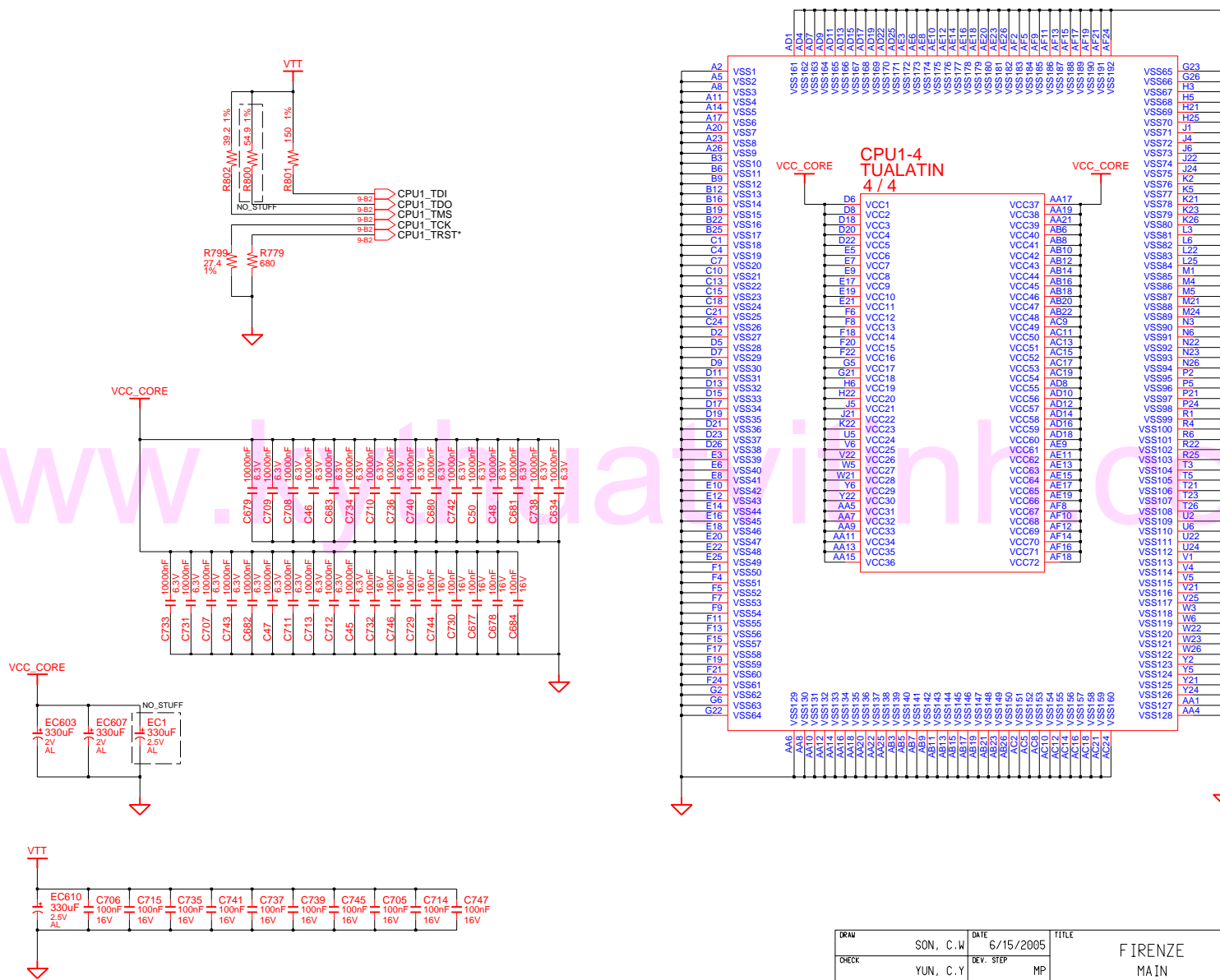
A

D

C

B

A

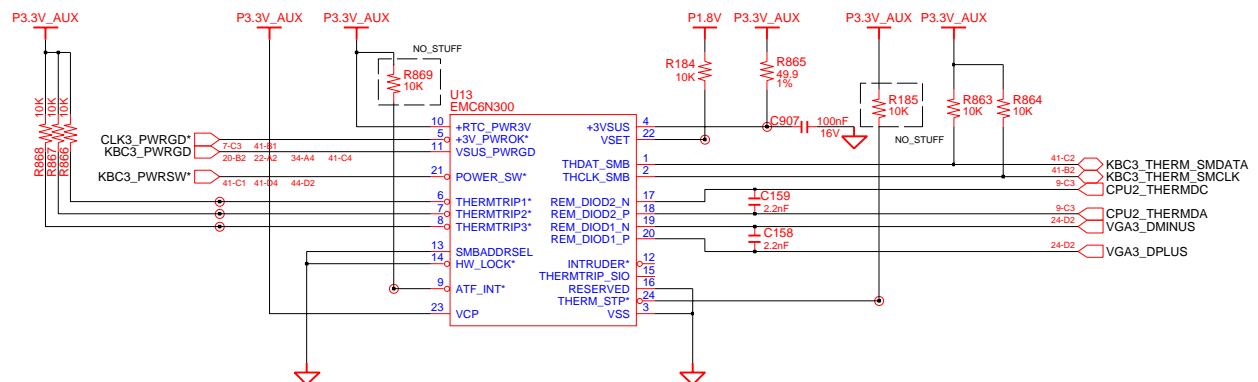


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MODULE CODE	undef ined	LAST EDIT				
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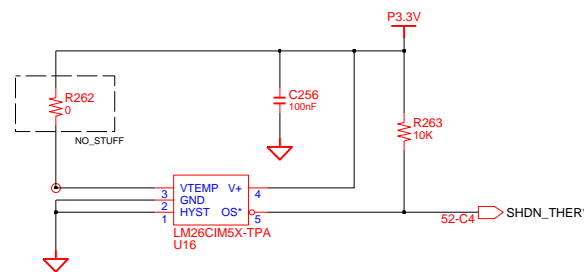
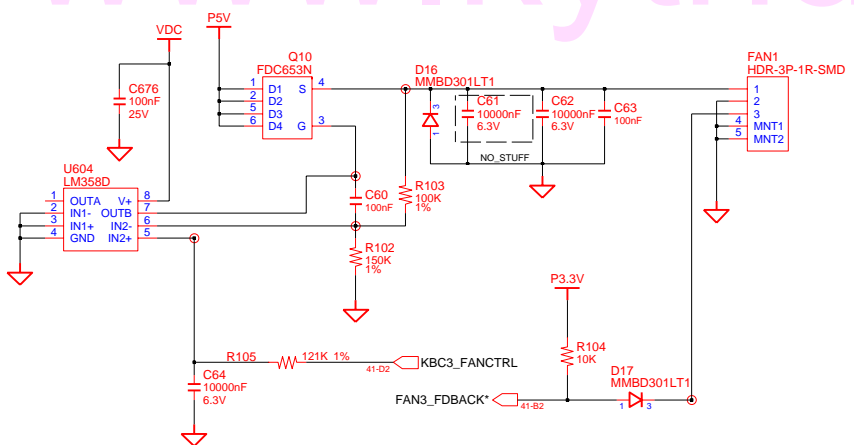
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CPU/GFX Thermal Sensor



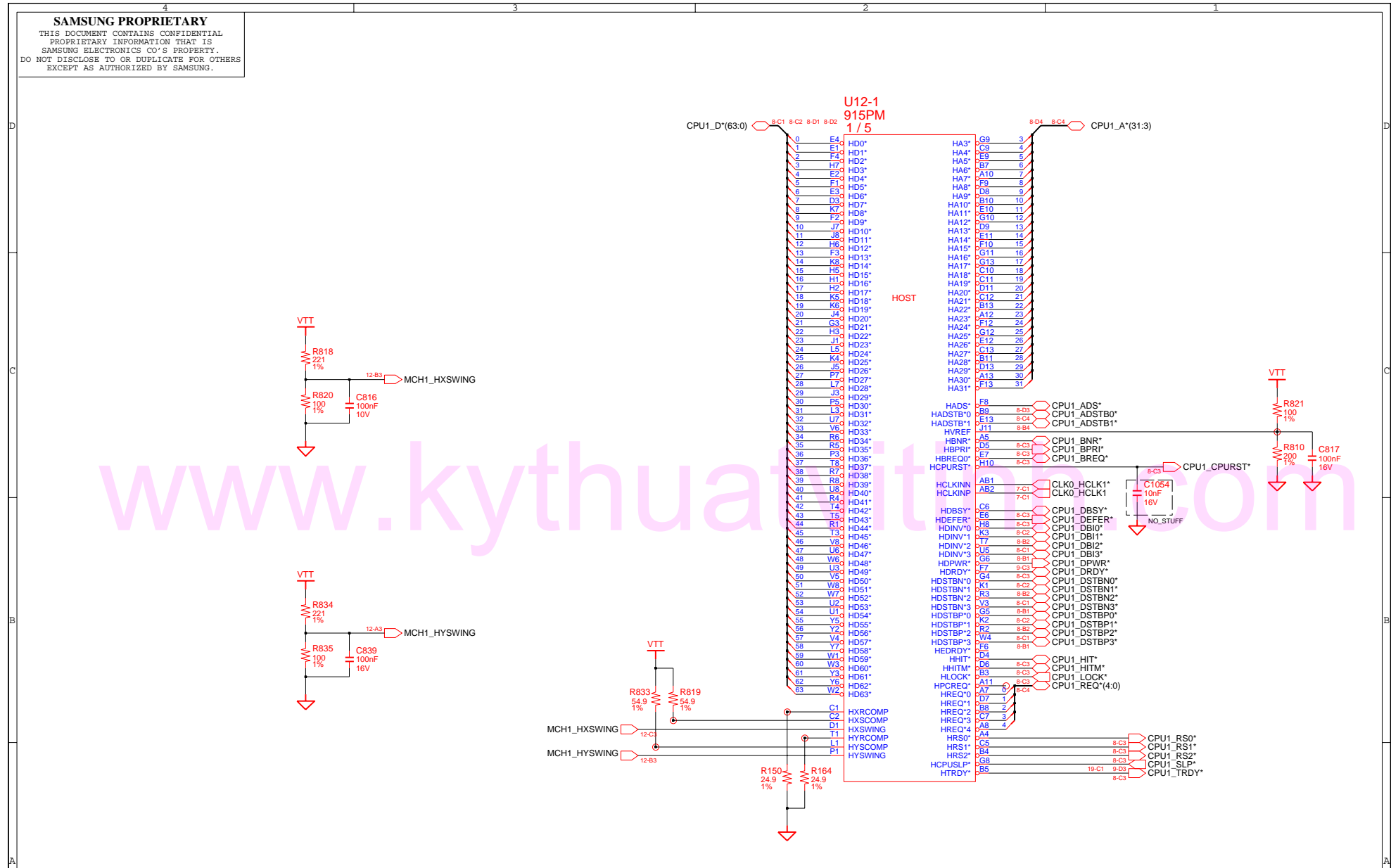
FAN CONTROL

OPT CIRCUIT



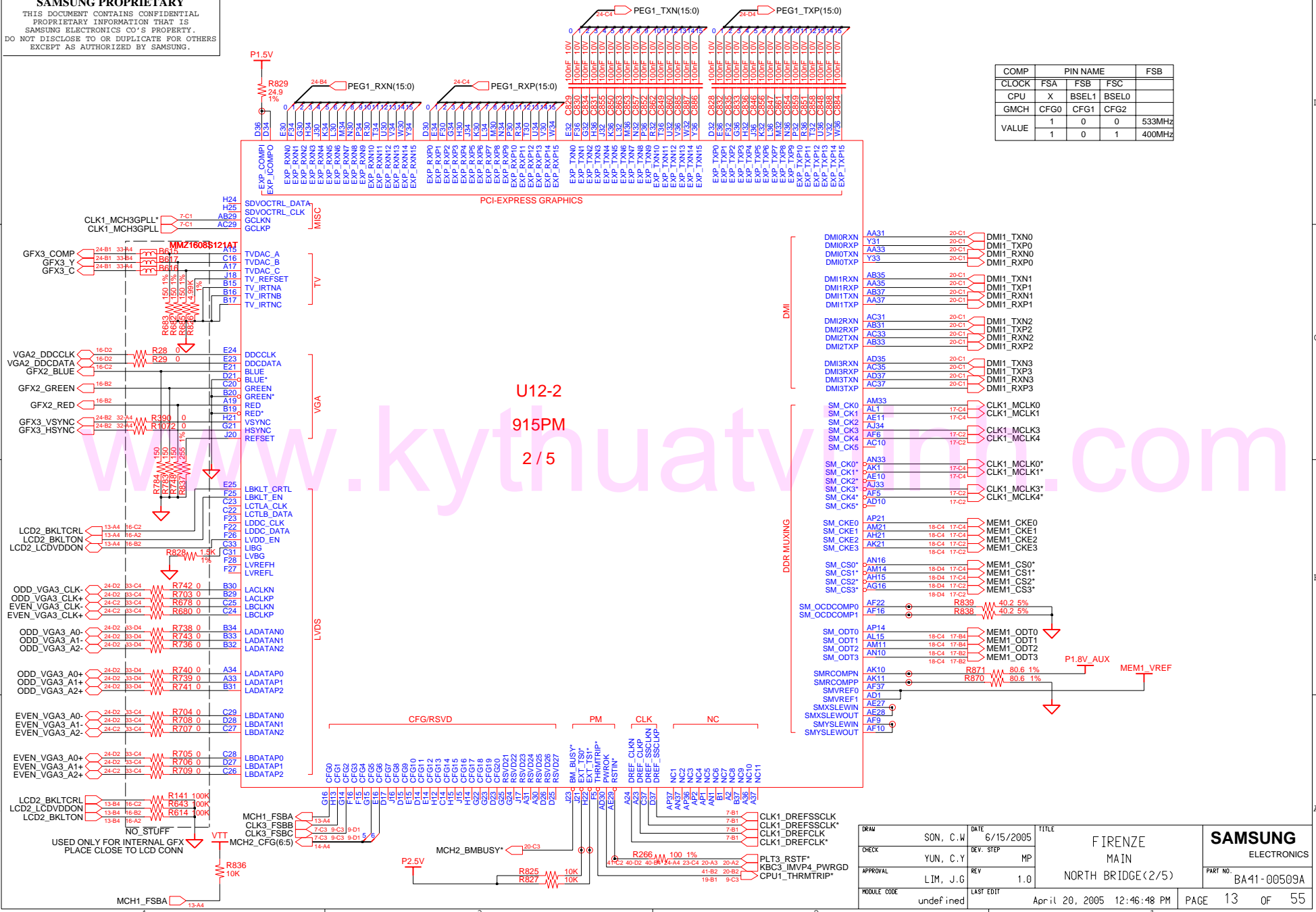
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CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0	THERMAL SENSOR/FAN CTRL	PART NO.	BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	11	OF 55

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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	NORTHE BRIDGE(1/5)		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00509A
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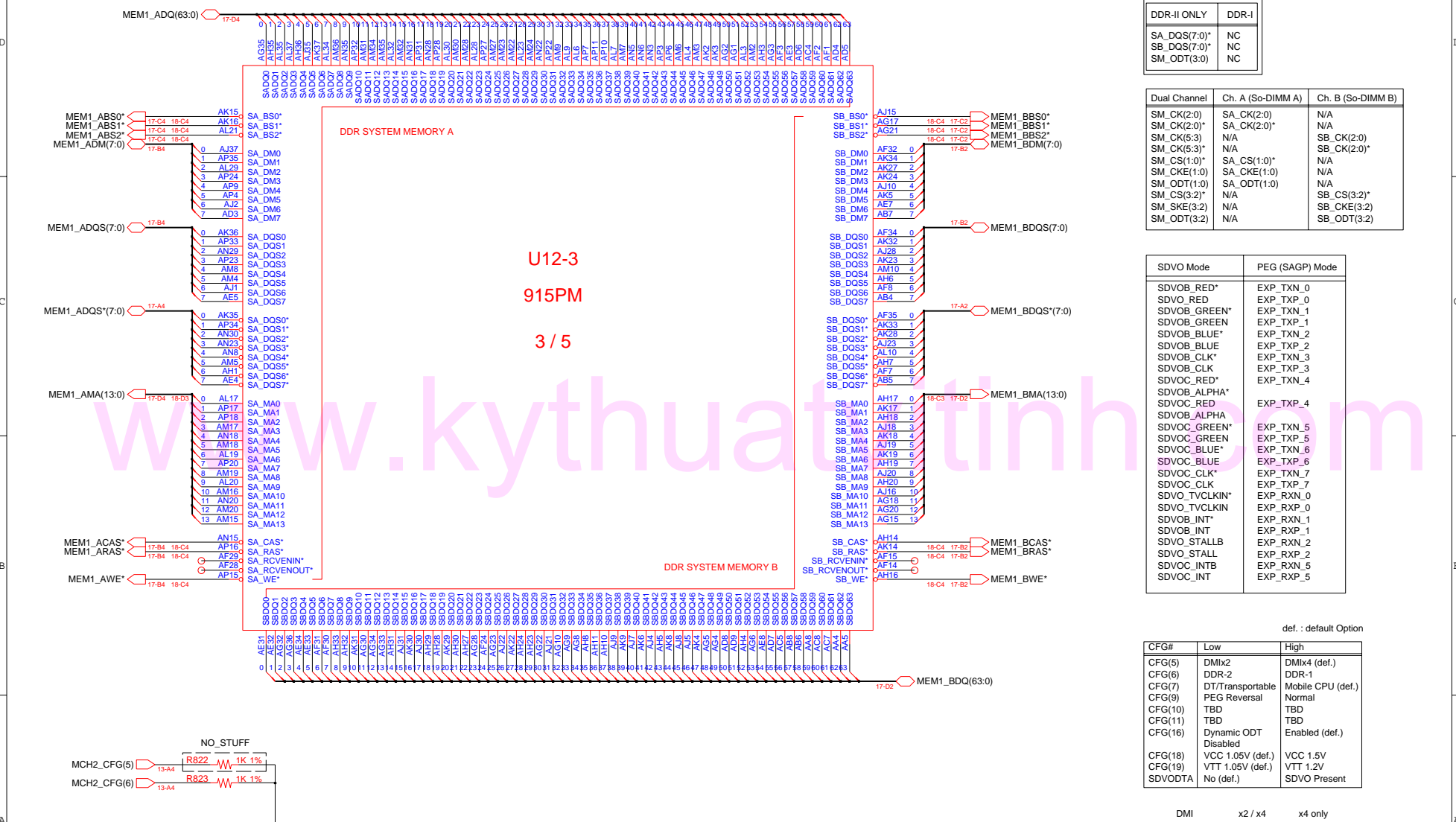
COMP	FSA	FSB	FSC	FSB
CLOCK	X	BSEL1	BSEL0	
CPU		0	0	533MHz
GMCH	CFG0	CFG1	CFG2	
VALUE	1	0	1	400MHz

U12-2
 915PM
 2 / 5

DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	MP		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0		NORTH BRIDGE(2/5)	PART NO. BA41-00509A
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DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	N/A
SM_CK(5:3)*	N/A	N/A
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXP_4
SDVOC_RED	EXP_TXN_5
SDVOB_ALPHA	EXP_TXP_5
SDVOC_GREEN*	EXP_TXN_6
SDVOC_GREEN	EXP_TXP_6
SDVOC_BLUE*	EXP_TXN_7
SDVOC_BLUE	EXP_TXP_7
SDVOC_CLK*	EXP_TXN_8
SDVOC_CLK	EXP_TXP_8
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

def. : default Option

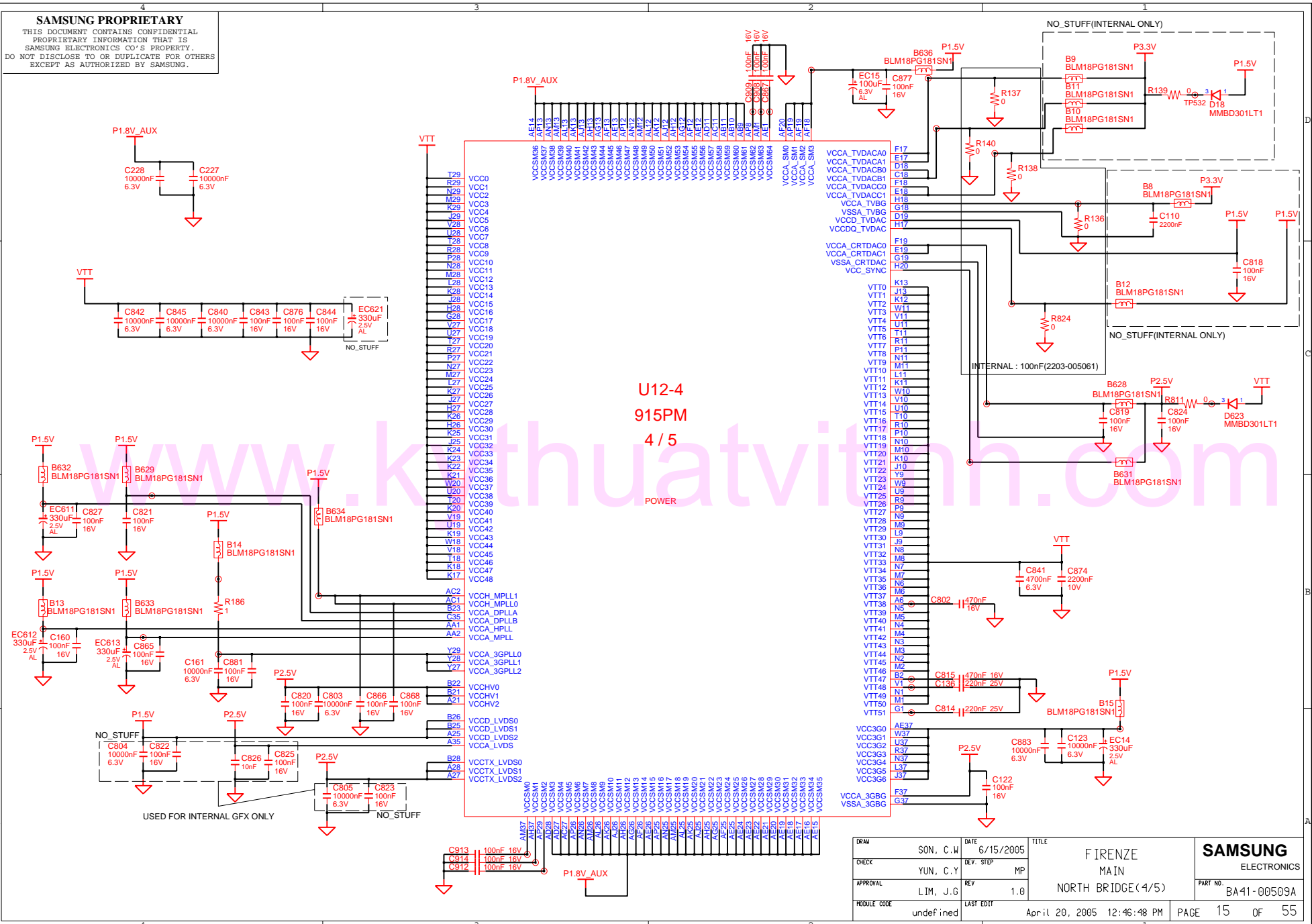
CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

DMI x2 / x4 x4 only

DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN NORTH BRIDGE(3/5)	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	14 OF 55	

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U12-4
915PM
4 / 5
POWER

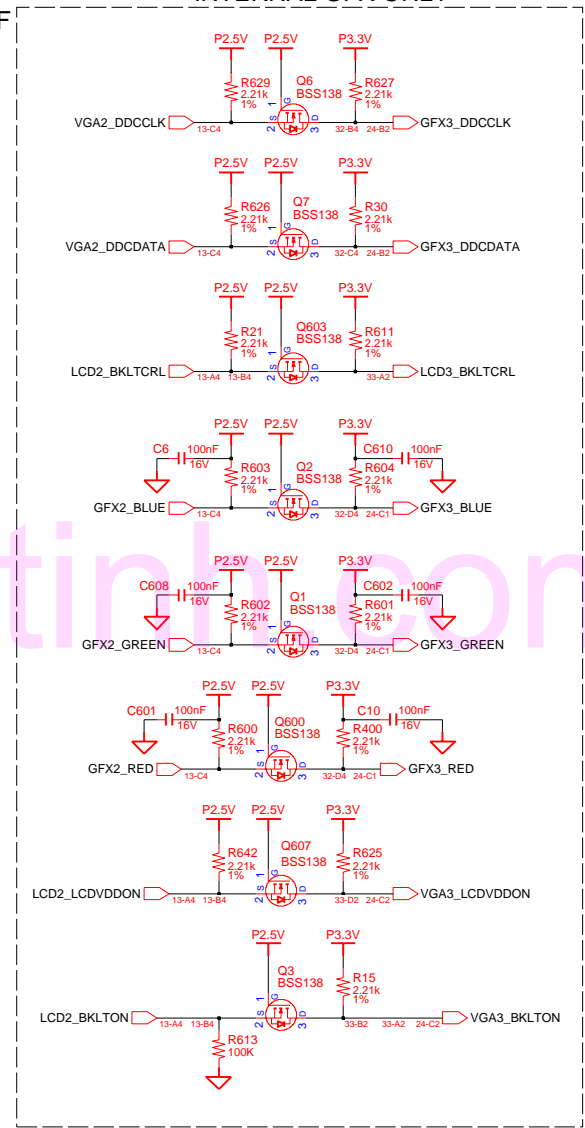
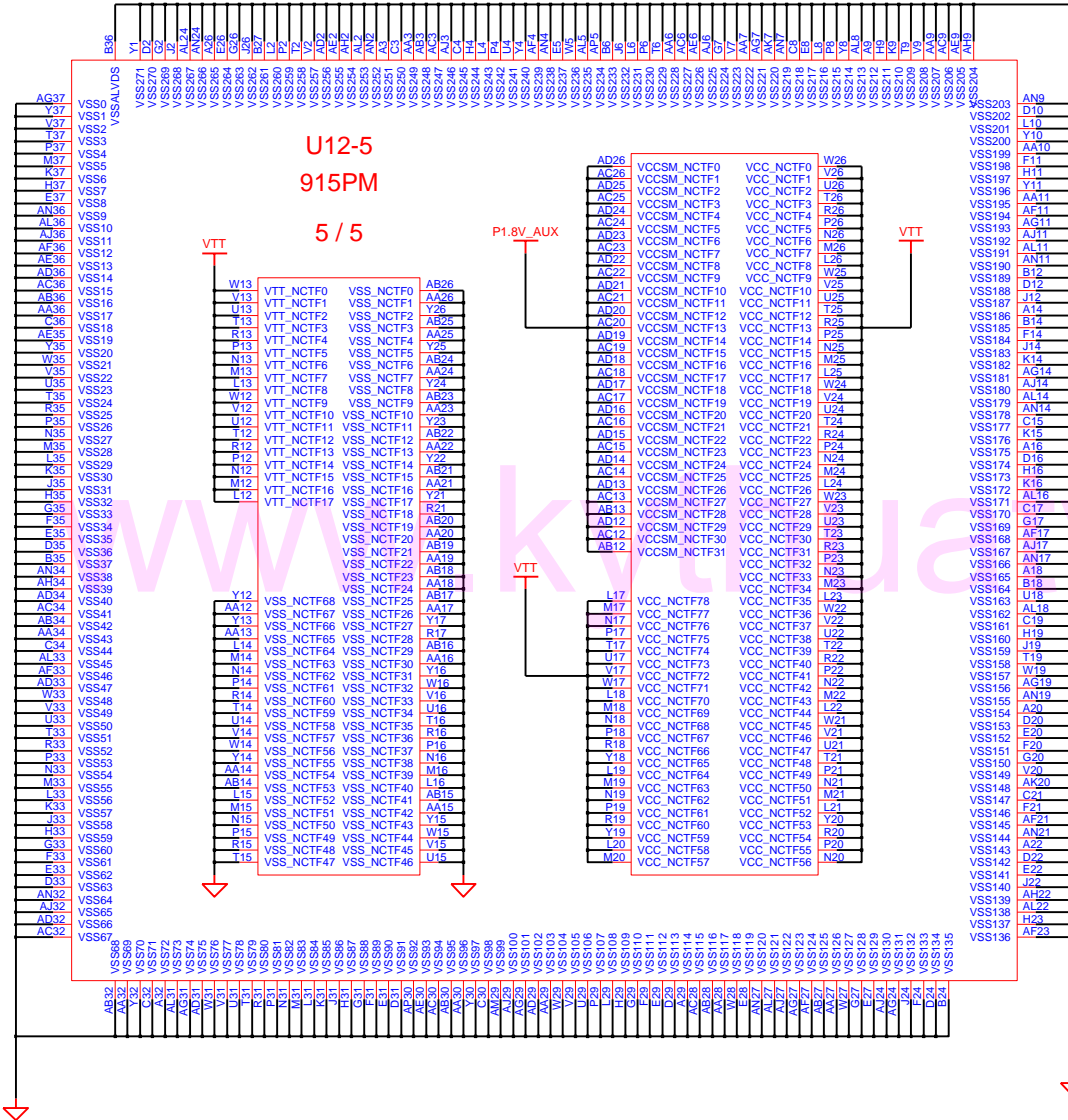
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CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			
				PAGE	15 OF 55	

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**LVDS Voltage Translation Logic
 (2.5V -> 3.3V)
 INTERNAL GFX ONLY**

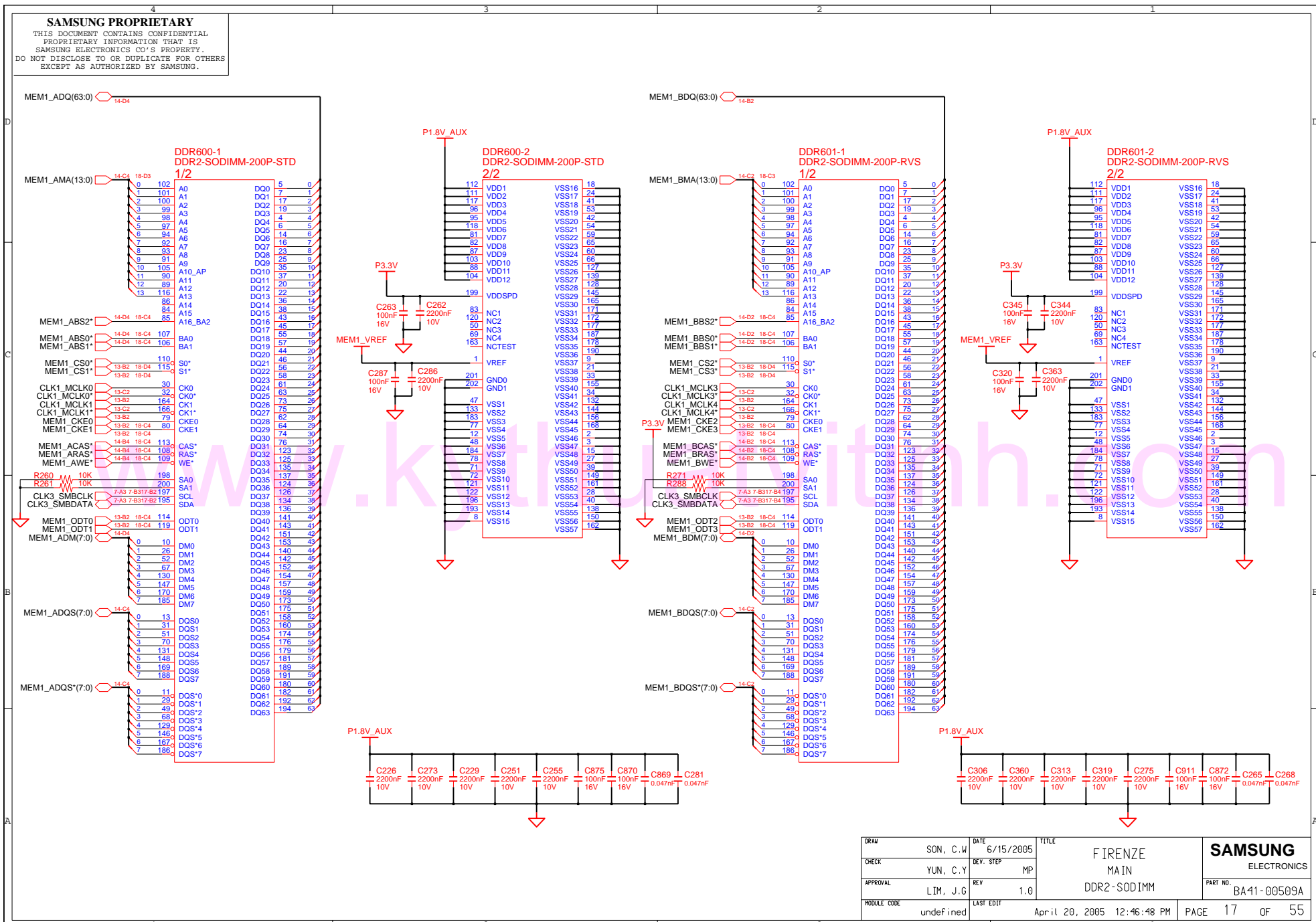
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN	BA41-00509A	
APPROVAL	LIM, J.G	REV	1.0	NORTH BRIDGE(5/5)		
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	16	OF 55

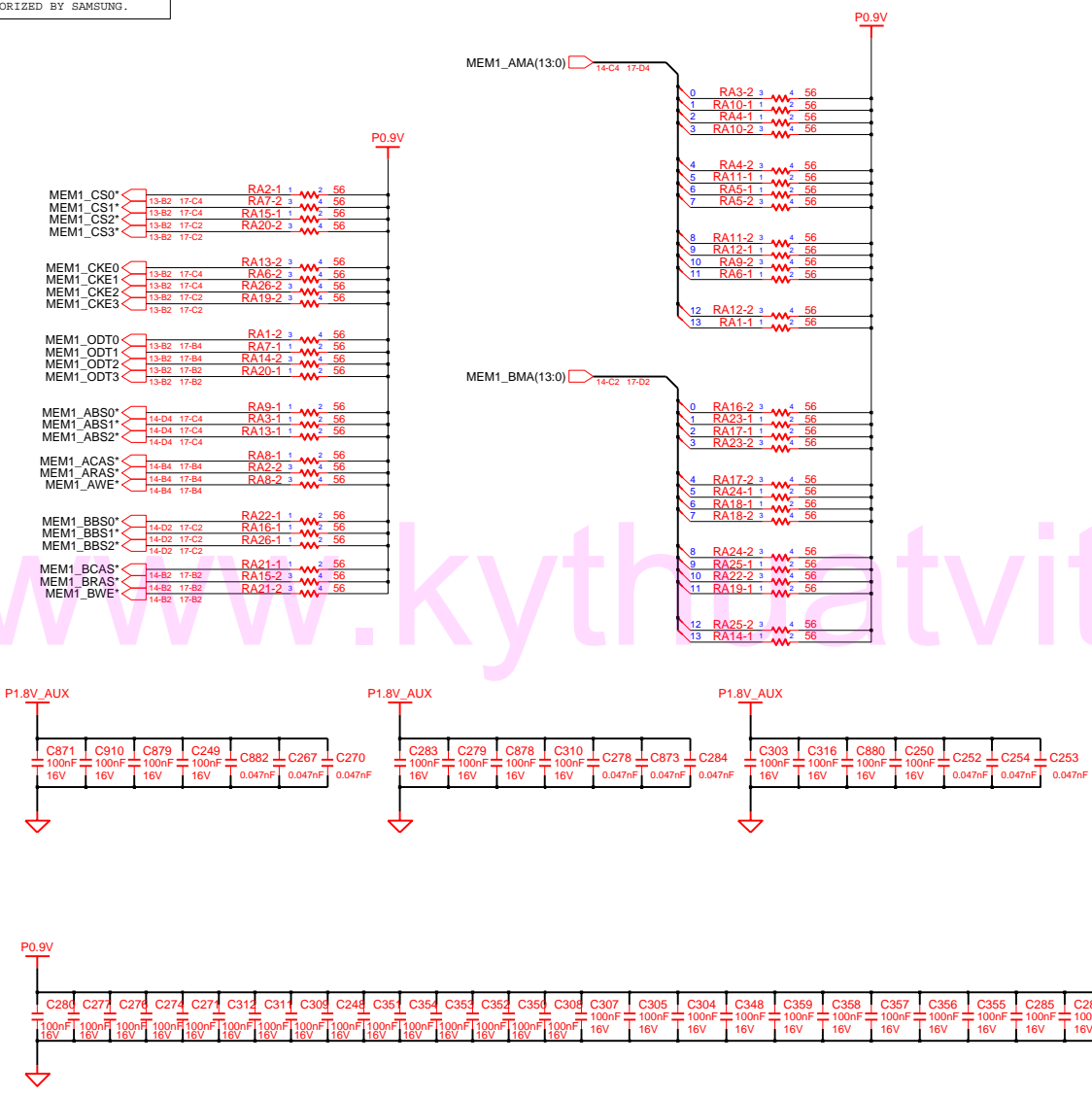
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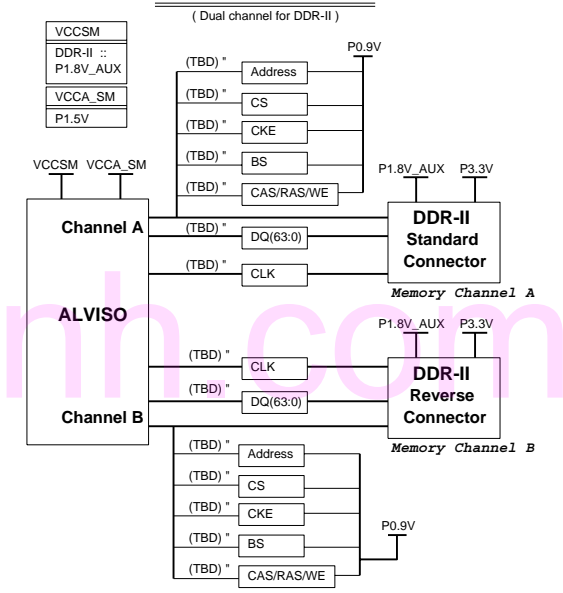


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP		DDR2-SODIMM	
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	17	OF 55

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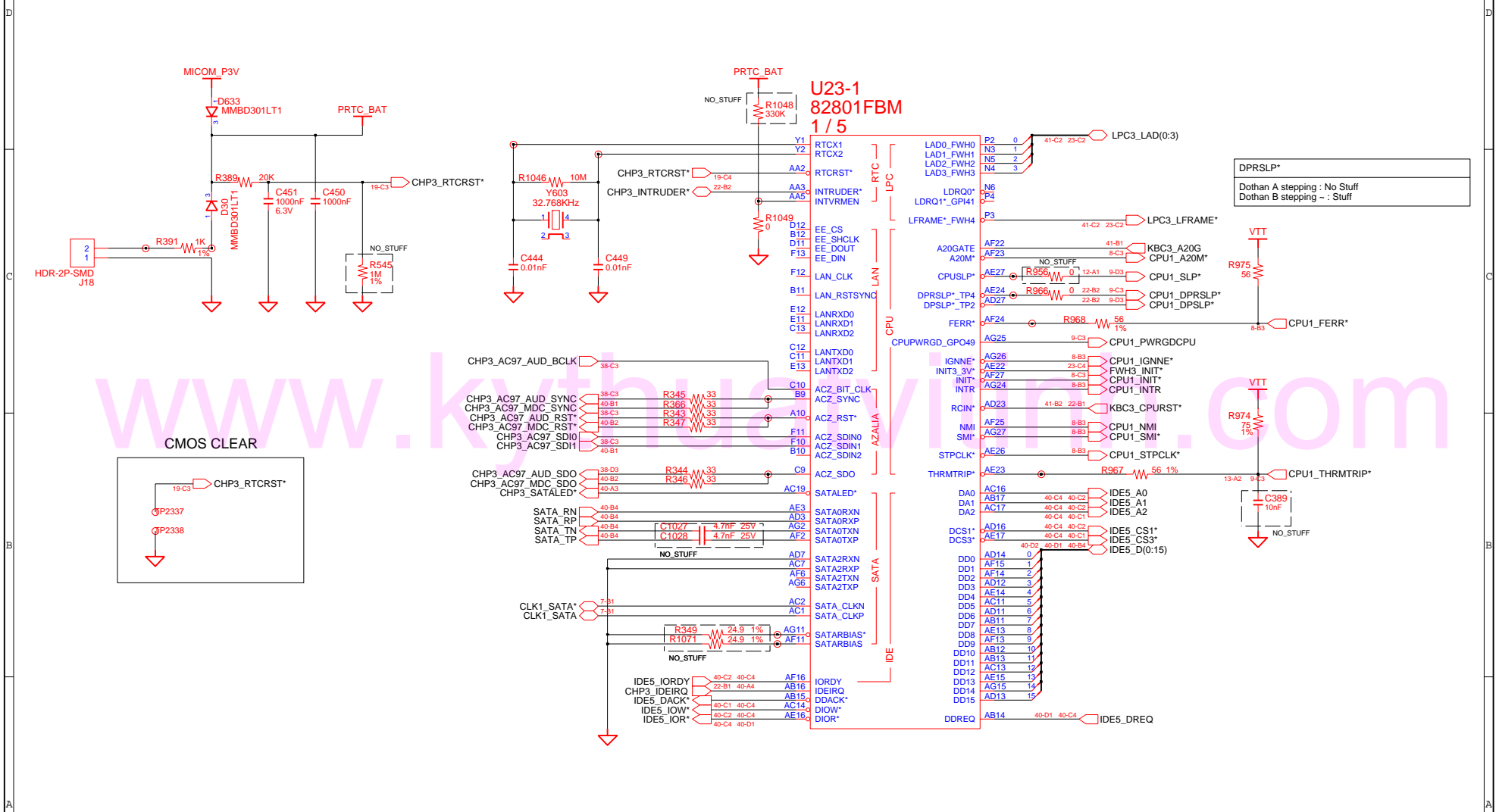


Memory Topology

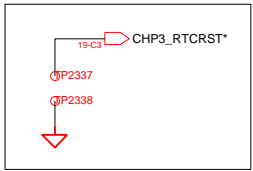


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	18 OF 55	PART NO. BA41-00509A

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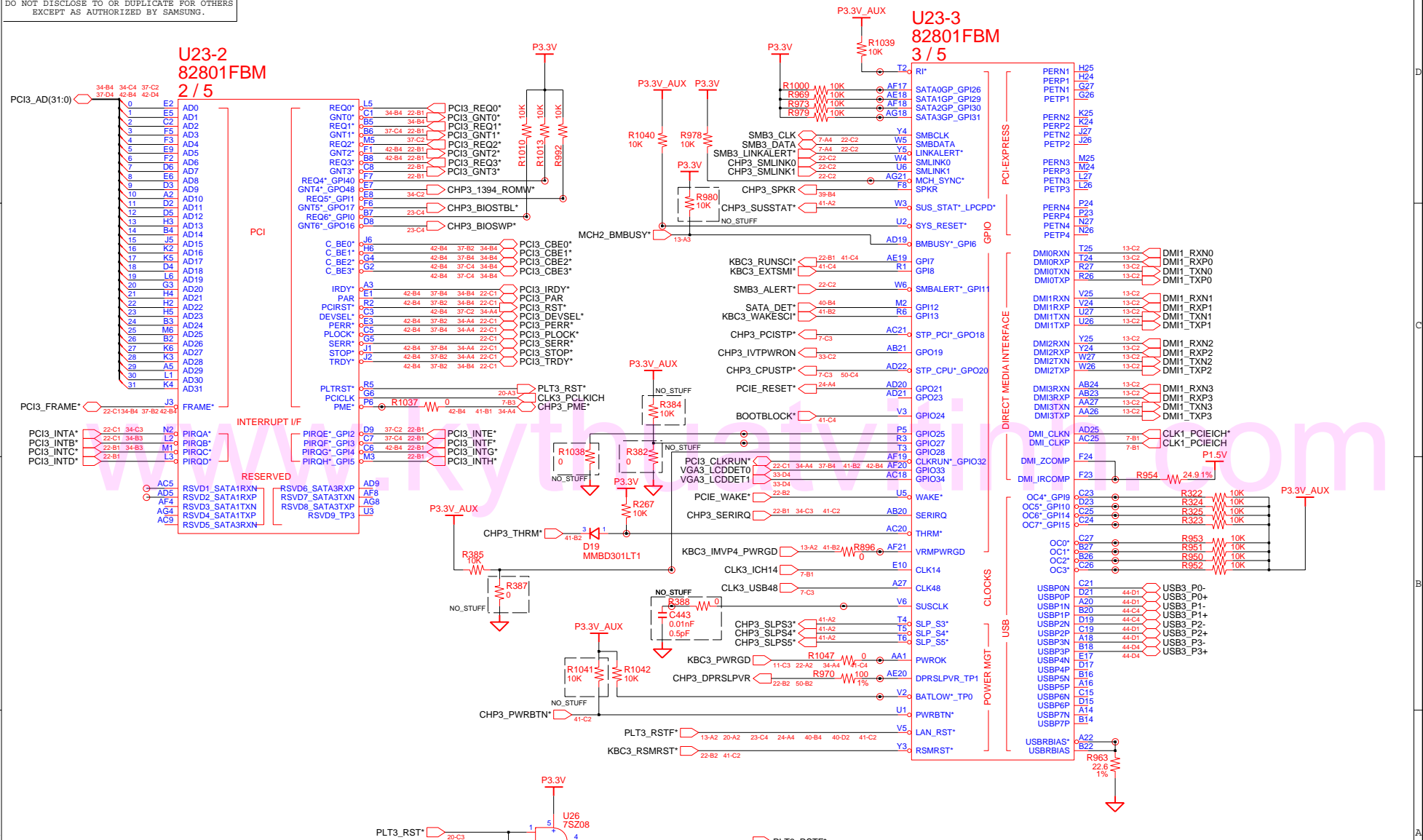
DPRSPL*
 Dothan A stepping : No Stuff
 Dothan B stepping - : Stuff



GRAM	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN SOUTH BRIDGE(1/4)	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	19 OF 55	

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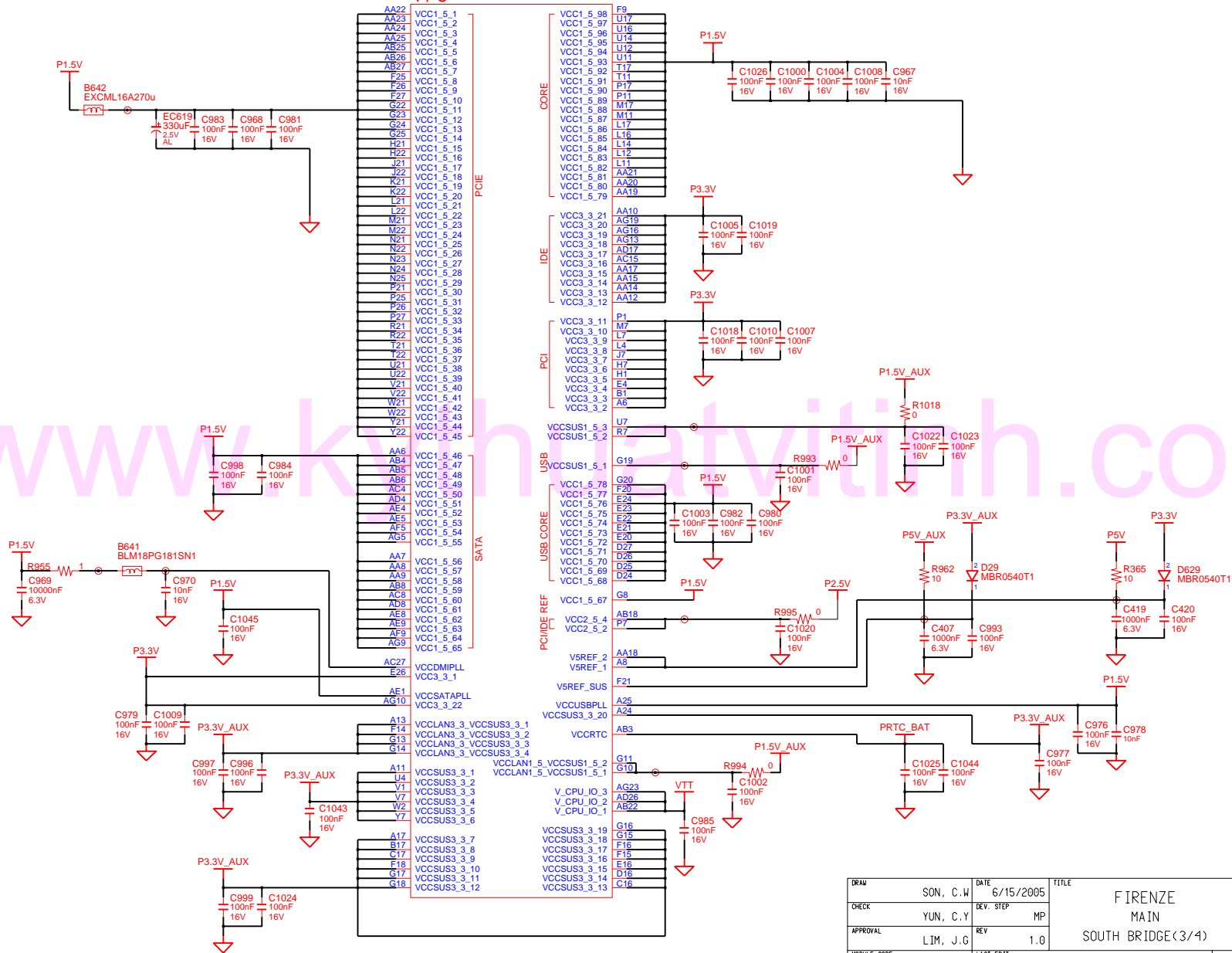


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G	REV	1.0	SOUTH BRIDGE(2/4)	PART NO.	BA41-00509A
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	20	OF 55

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**U23-4
82801FBM
4 / 5**



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN SOUTH BRIDGE(3/4)	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			

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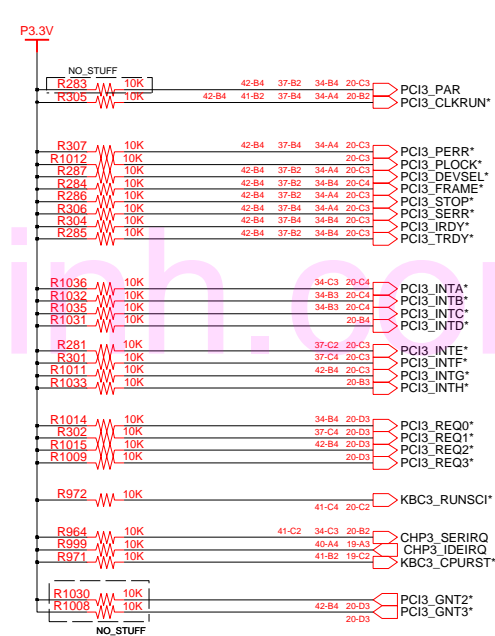
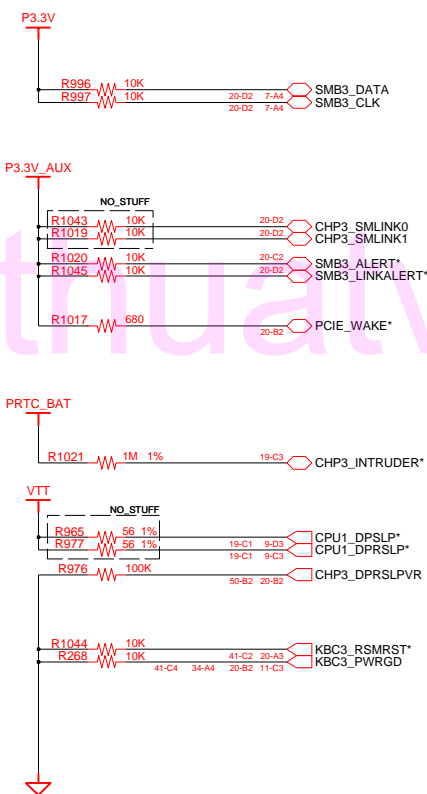
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ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI_GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
ECP_DOUT		TBD

**U23-5
82801FBM
5 / 5**

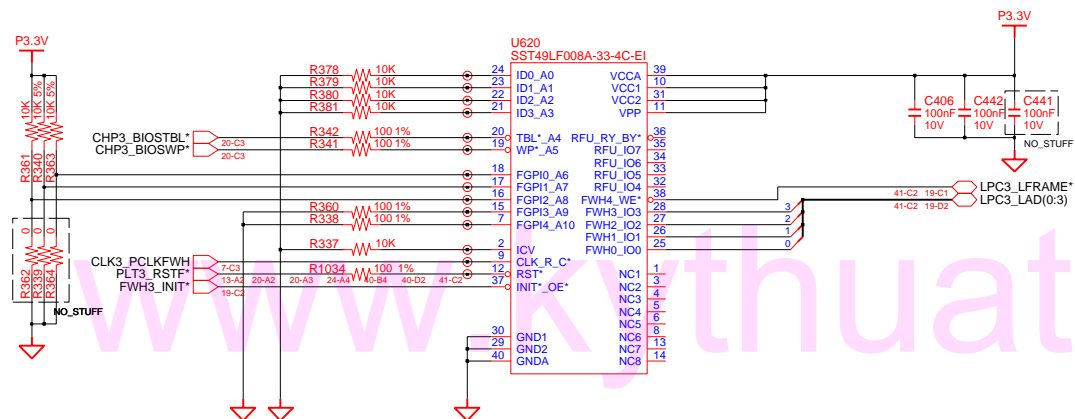
AG22	VSS_172	VSS_86	P22
AG20	VSS_171	VSS_85	P16
AG17	VSS_170	VSS_84	P15
AG14	VSS_169	VSS_83	P14
AG12	VSS_168	VSS_82	P13
AG3	VSS_167	VSS_81	P12
AG1	VSS_166	VSS_80	N17
AF26	VSS_165	VSS_79	N16
AF12	VSS_164	VSS_78	N15
AF10	VSS_163	VSS_77	N14
AF7	VSS_162	VSS_76	N13
AF3	VSS_161	VSS_75	N12
AF1	VSS_160	VSS_74	N11
AE26	VSS_159	VSS_73	N7
AE21	VSS_158	VSS_72	N1
AE12	VSS_157	VSS_71	M27
AE11	VSS_156	VSS_70	M26
AE10	VSS_155	VSS_69	M23
AE7	VSS_154	VSS_68	M18
AE6	VSS_153	VSS_67	M16
AE2	VSS_152	VSS_66	M15
AD24	VSS_151	VSS_65	M14
AD18	VSS_150	VSS_64	M13
AD15	VSS_149	VSS_63	M12
AD10	VSS_148	VSS_62	M11
AD2	VSS_147	VSS_61	M10
AD6	VSS_146	VSS_60	M9
AD1	VSS_145	VSS_59	M8
AC26	VSS_144	VSS_58	M7
AC24	VSS_143	VSS_57	M6
AC23	VSS_142	VSS_56	M5
AC22	VSS_141	VSS_55	M4
AC12	VSS_140	VSS_54	M3
AC10	VSS_139	VSS_53	M2
AC6	VSS_138	VSS_52	M1
AC2	VSS_137	VSS_51	K27
AB19	VSS_136	VSS_50	K26
AB10	VSS_135	VSS_49	K23
AB9	VSS_134	VSS_48	K22
AB7	VSS_133	VSS_47	K21
AB2	VSS_132	VSS_46	K20
AB1	VSS_131	VSS_45	K19
AA16	VSS_130	VSS_44	K18
AA13	VSS_129	VSS_43	K17
AA11	VSS_128	VSS_42	K16
AA4	VSS_127	VSS_41	K15
Y27	VSS_126	VSS_40	K14
Y26	VSS_125	VSS_39	K13
Y23	VSS_124	VSS_38	K12
Y6	VSS_123	VSS_37	K11
W25	VSS_122	VSS_36	K10
W24	VSS_121	VSS_35	K9
W23	VSS_120	VSS_34	K8
W7	VSS_119	VSS_33	K7
W1	VSS_118	VSS_32	K6
V27	VSS_117	VSS_31	K5
V26	VSS_116	VSS_30	K4
V23	VSS_115	VSS_29	K3
V4	VSS_114	VSS_28	K2
U25	VSS_113	VSS_27	K1
U24	VSS_112	VSS_26	J27
U23	VSS_111	VSS_25	J26
U15	VSS_110	VSS_24	J23
U13	VSS_109	VSS_23	J22
T27	VSS_108	VSS_22	J21
T26	VSS_107	VSS_21	J20
T23	VSS_106	VSS_20	J19
T16	VSS_105	VSS_19	J18
T15	VSS_104	VSS_18	J17
T14	VSS_103	VSS_17	J16
T13	VSS_102	VSS_16	J15
T12	VSS_101	VSS_15	J14
T11	VSS_99	VSS_13	J13
R25	VSS_98	VSS_12	J12
R24	VSS_97	VSS_11	J11
R23	VSS_96	VSS_10	J10
R17	VSS_95	VSS_9	J9
R16	VSS_94	VSS_8	J8
R15	VSS_93	VSS_7	J7
R14	VSS_92	VSS_6	J6
R13	VSS_91	VSS_5	J5
R12	VSS_90	VSS_4	J4
R11	VSS_89	VSS_3	J3
R4	VSS_88	VSS_2	J2
	VSS_87	VSS_1	J1



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP		MAIN	
APPROVAL	LIM, J.G	REV	1.0		SOUTH BRIDGE(4/4)	PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	22	OF 55

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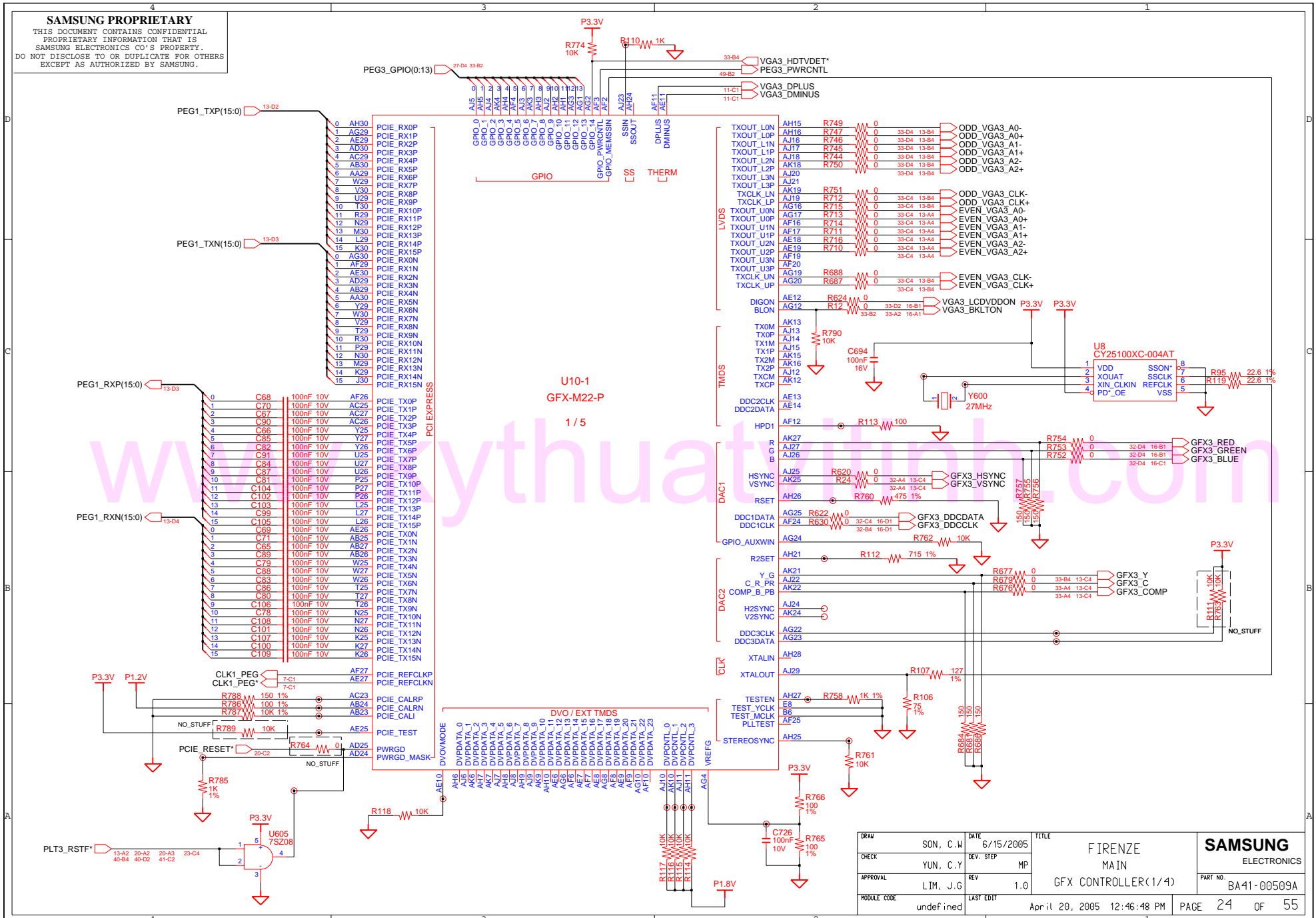


- | | | | |
|----|--|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE | 7E | TEST COPROCESSER IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT |
| 14 | INIT. KEYBOARD CONTROLLER | 88 | INIT. BIOS DATA ROM |
| 16 | CHECK CHECKSUM | 8A | INIT.EXTENDED BIOS DATA AREA |
| 18 | 8254 TIMER INIT. | 8C | INIT. FDD CONTROLLER |
| 1A | 8237 DMA CONTROLLER INIT. | 9A | SHADOW OPTION ROMS |
| 1C | RESET INTERRUPT CONTROLLER | 9C | SETUP POWER MANAGEMENT |
| 20 | TEST DRAM REFRESH | 9E | ENABLE H/W INTERRUPT |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A0 | SET TIME OF DAY |
| 24 | SET ES SEGMENT REG. TO 4GB | A4 | INIT. TYPEMATIC RATE |
| 26 | ENABLE A20 | A8 | ERASE F2 PROMPT |
| 28 | AUTO SIZING DRAM | AA | SCAN FOR F2 KEY STROKE |
| 32 | COMPUTE THE CPU SPEED | AC | ENTER SETUP |
| 34 | TESET CMOS RAM | AE | CLEAR IN POST FLAG |
| 38 | SHADOW SYSTEM BIOS ROM | B0 | CHECK FOR ERRORS |
| 3A | AUTO SIZING CACHE | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B4 | ONE BEEP |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B6 | CHECK PASSWORD (OPTION) |
| 42 | INIT. INTERRUPT VECTOR | B7 | ACPI INIT |
| 44 | INIT. BIOS INTERRUPT | BA | DMI INIT |
| 46 | CHECK ROM COPYRIGHT NOTICE | BE | CLEAR SCREEN |
| 47 | INIT. I20 SUPPORT IF INSTALLED | C0 | TRY BOOT WITH INT19 |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D0 | INTERRUPT HANDLER ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D2 | UNKNOWN INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D4 | PENDING INTERRUPT ERROR |
| 4C | SHADOW VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 50 | DISPLAY CPU TYPE AND SPEED | D8 | SHUTDOWN ERROR |
| 52 | TEST KEYBOARD | DA | EXTENDED BLOCK MOVE |
| 54 | SET KEYCLICK IF ENABLED | DC | SHUTDOWN 10 |
| 56 | ENABLE KEYBOARD | 89 | ENABLE NMI |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 90 | INIT. HDD CONTROLLER |
| 5A | DISPLAY " PRESS SETUP" | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5C | TEST RAM BETWEEN 512K AND 640K | 92 | JUMP TO USER PATCH 2 |
| 60 | TEST EXTENDED MEMORY | 94 | DISABLE A20 ADDRESS LINE |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 96 | CLEAR HUGE ES SEGMENT REG. |
| 64 | JUMP TO USER PATCH 1 | 98 | SEARCH FOR OPTION ROMS |

DRAW	SON, C. W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	MP		MAIN	
APPROVAL	LIM, J. G	REV	1.0		FWH	PART NO. BA41-00509A
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	23	OF 55

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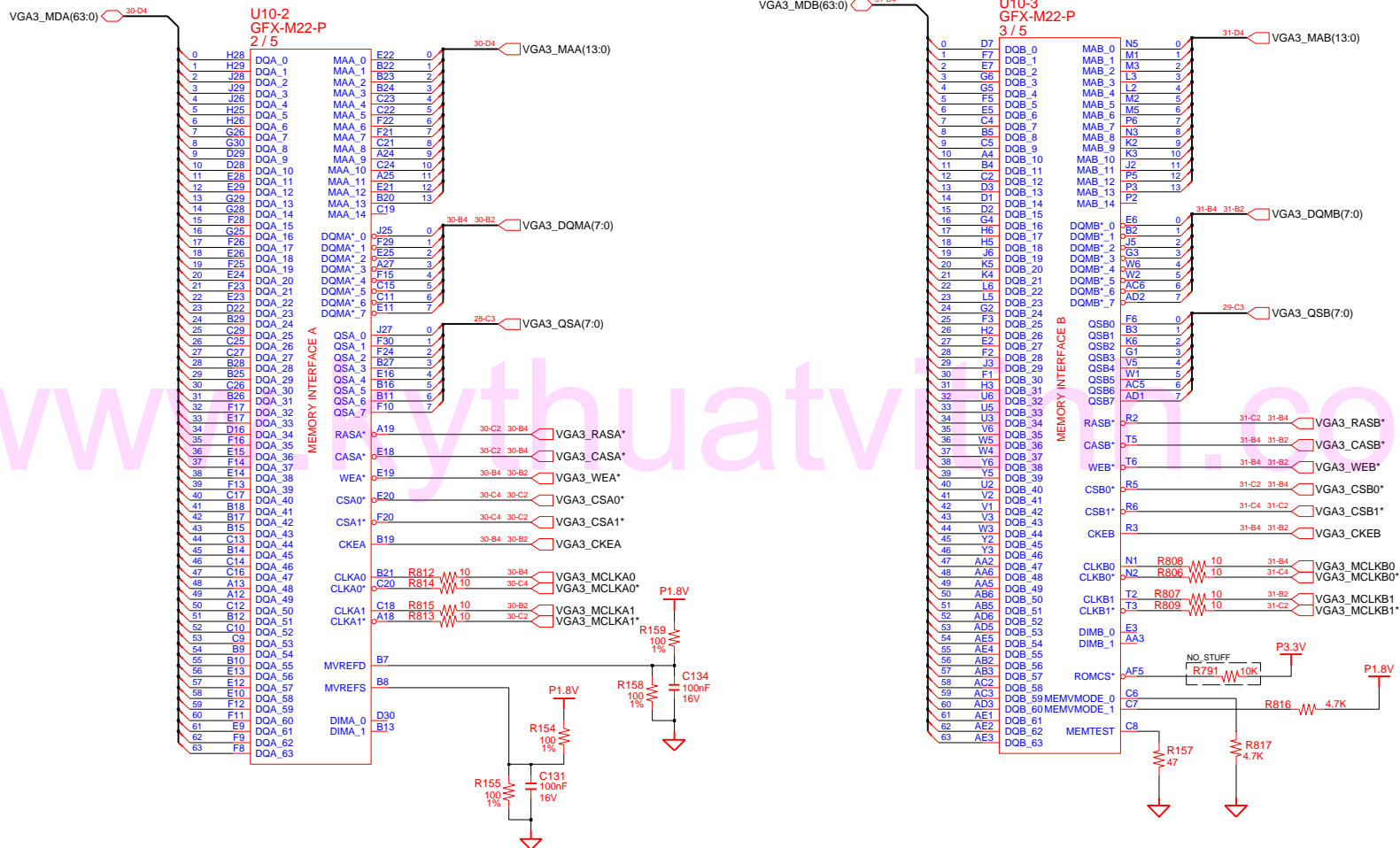
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	GFX CONTROLLER(1/4)		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00509A
MODULE CODE	undef ined	LAST EDIT	Apr il 20, 2005 12:46:48 PM	PAGE	24	OF 55

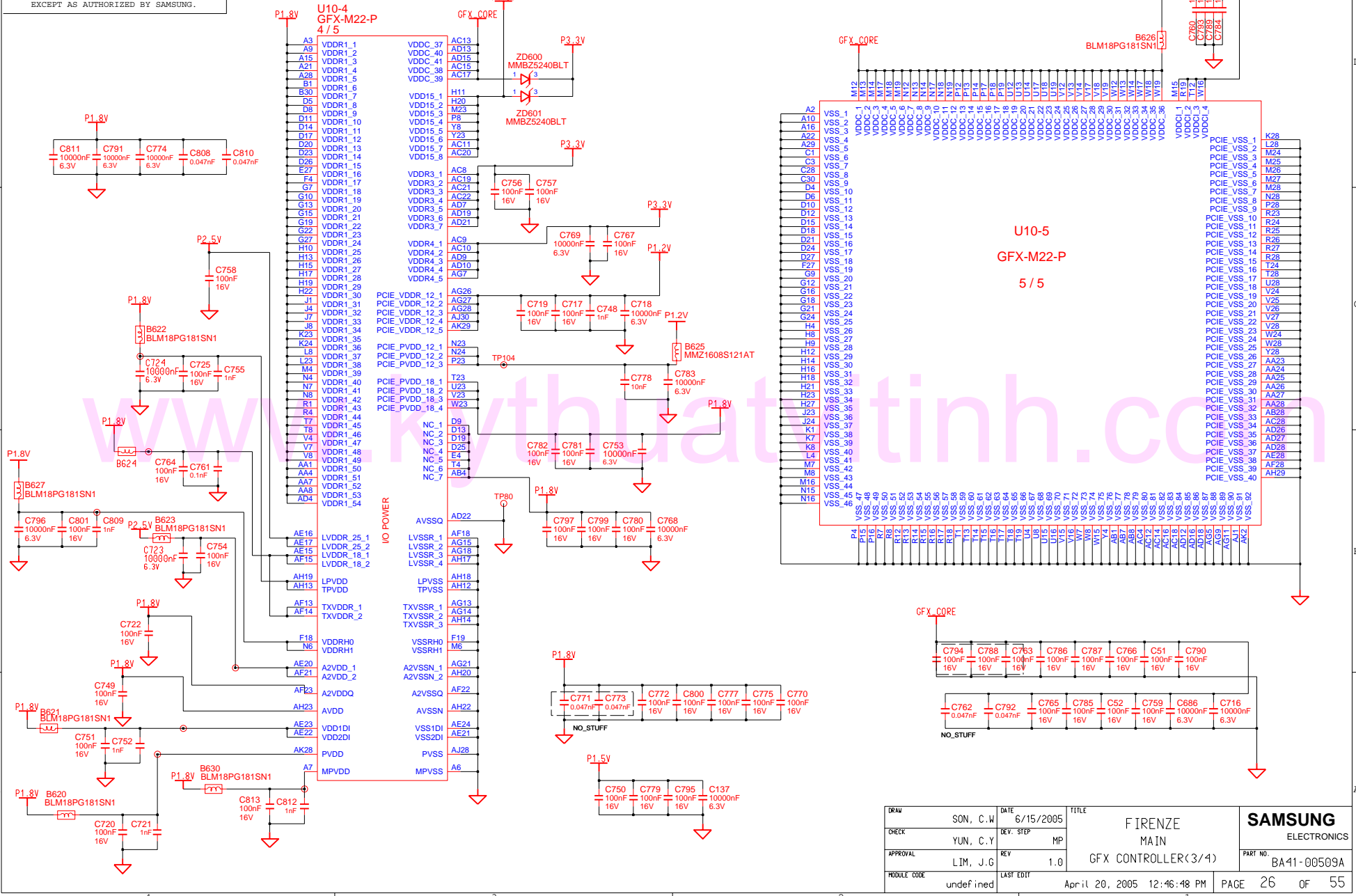
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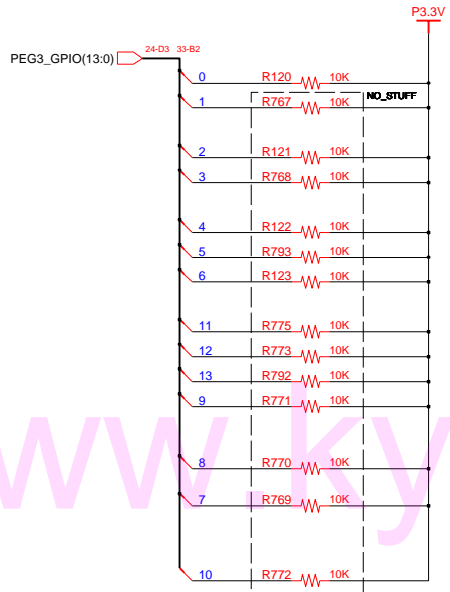
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	GFX CONTROLLER(2/4)		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	25	OF 55

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CHECK	YUN, C.Y	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G	REV	1.0	GFX CONTROLLER(3/4)	PART NO.	BA41-00509A
MODULE CODE	undef ined	LAST EDIT	Apr il 20, 2005 12:46:48 PM	PAGE	26	OF 55

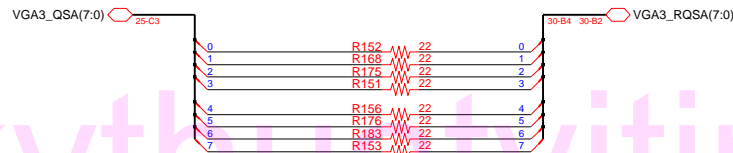
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Straps	Pin Number	Descriptions
CAL_BG_BACKUP	GPIO0	PCI-Express Current Calibration Bandgap Backup 0 : use reference voltage from bandgap (Default) 1 : use reference voltage from resistor divider
PLL_CAL_FORCE_EN	GPIO1	PCI-Express PLL Calibration Force Enable 0 : Disable PLL force calibration (Default) 1 : Enable PLL force calibration
PCIe Mode(1:0)	GPIO(3:2)	PCI-Express Mode 00 : PCI Express 1.0A mode (Default) 01 : Reserved 10 : PCI Express 1.0 mode 11 : Reserved
CAL_OFF	GPIO4	Turn-Off PCI-Express Impedance / Strength Calibration 0 : Enable (Default) 1 : Disable Also, used to demux VCOREF / CALREF
BYPASS_PLL	GPIO5	Bypass PCI-Express PLL 0 : - (Default) 1 : -
ICOMP	GPIO6	PCI-Express Transmitter Current Compensation 0 : Normal (Default) 1 : Inject extra current for output buffer switching
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. 0000 : No ROM, CHG_ID = 0 0001 : No ROM, CHG_ID = 1 0100 : Reserved 0110 : Reserved Others : ROM (Third party vendors)
DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.

DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN GFX CONTROLLER(4/4)	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			
				PAGE	27	OF 55

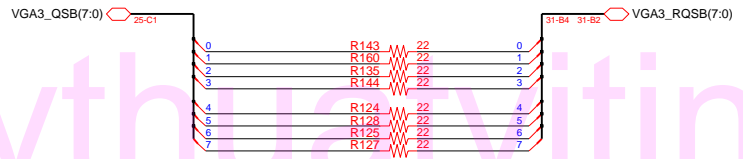
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0	GFX MEMORY TERM(1/2)		PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	28	OF 55

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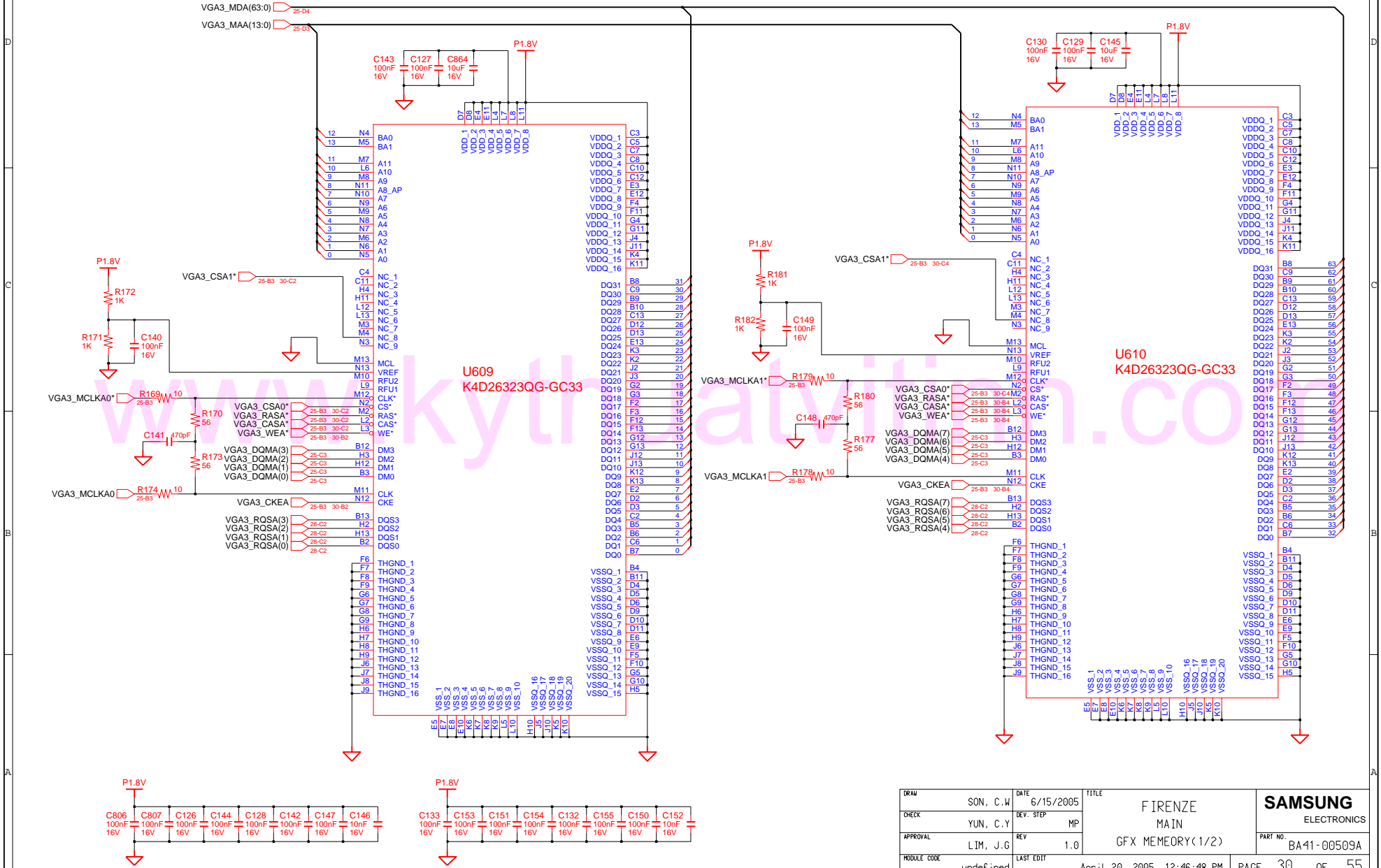


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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0	GFX MEMORY TERM(2/2)		PART NO. BA41-00509A
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	29	OF 55

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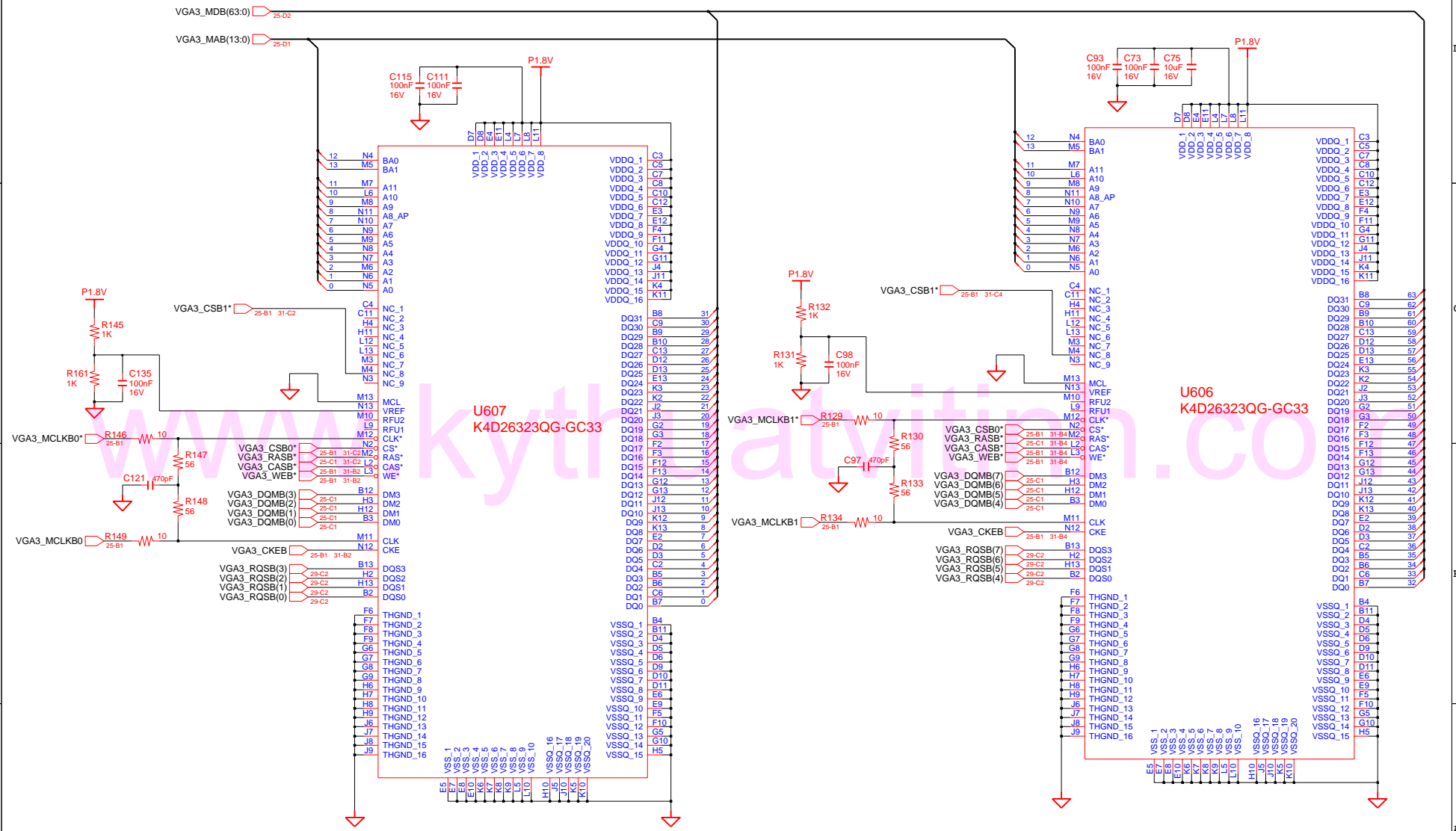
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DRAW	SON, C.W.	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y.	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G.	REV	1.0	GFX MEMORY(1/2)		PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	30	OF 55

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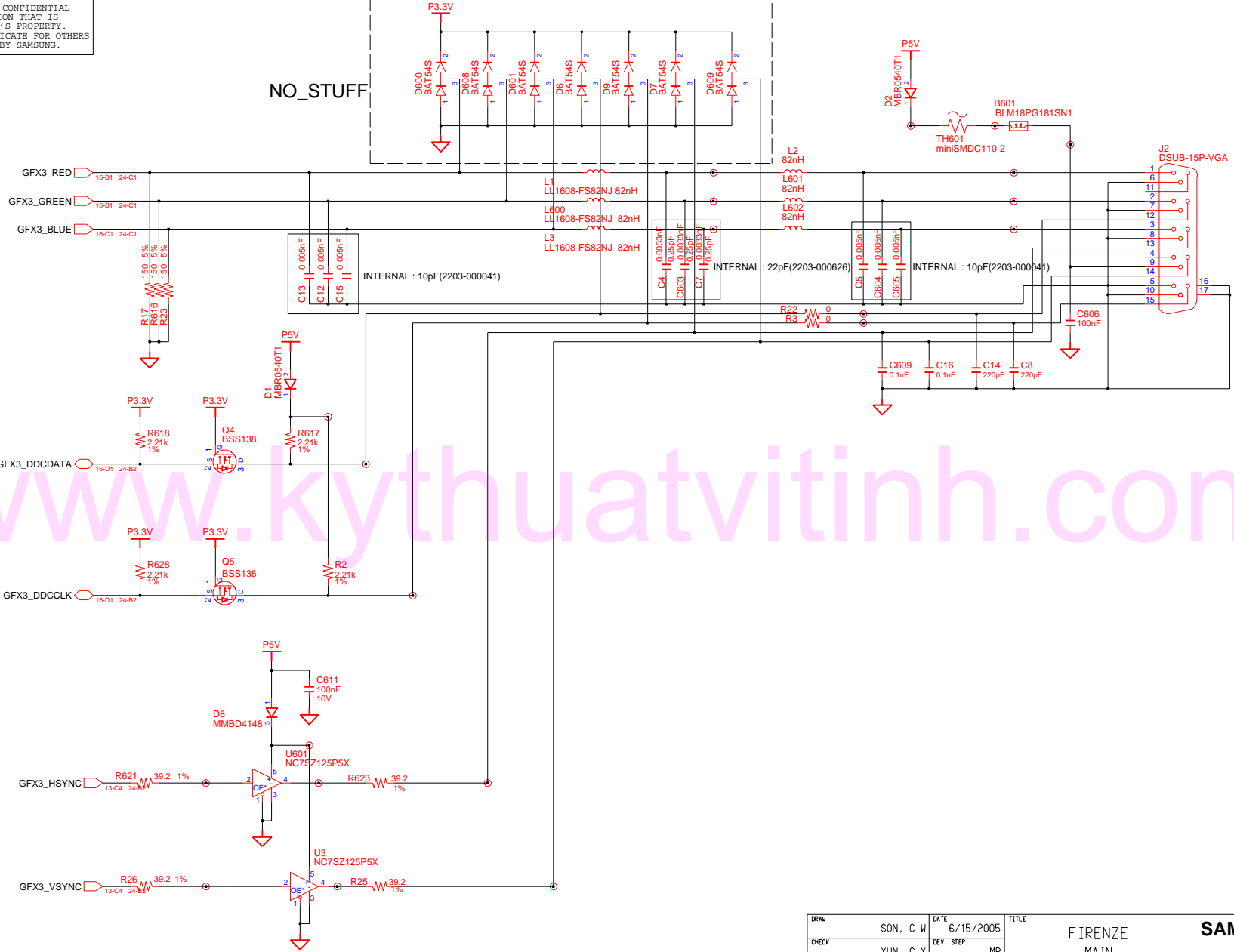


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN GFX MEMORY(2/2)	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	Apr 10, 2005 12:46:48 PM	PAGE	31 OF 55	

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NO_STUFF



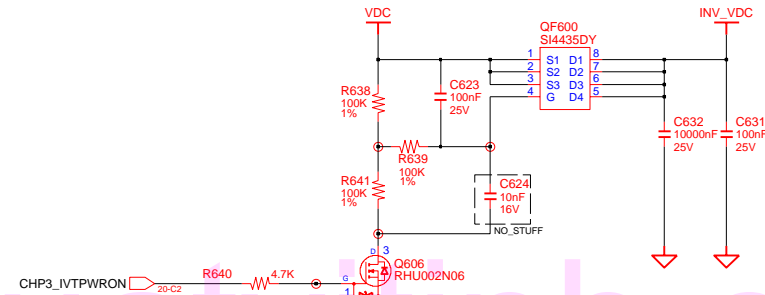
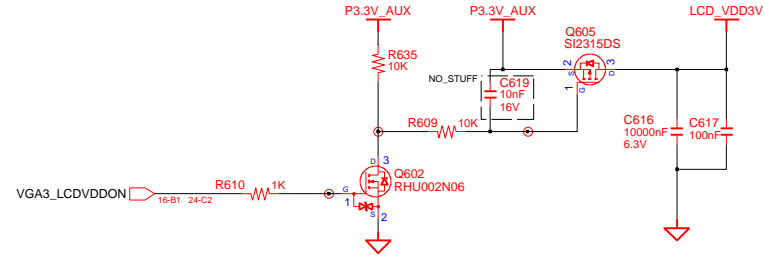
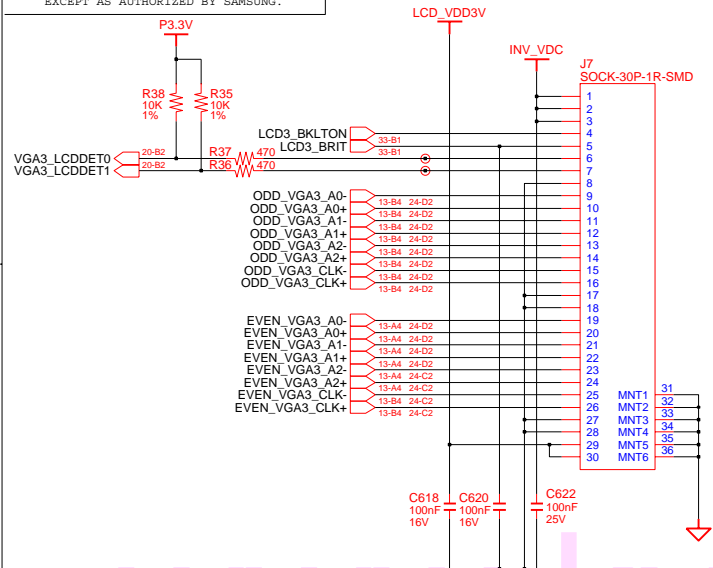
www.kythuatvinh.com

DRAW	SON, C. W	DATE	6/15/2005	TITLE	FIRENZE MAIN CRT PORT	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	MP			
APPROVAL	LIM, J. G	REV	1.0			PART NO. BA41-00509A
MODULE CODE	undefind	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	32	OF 55

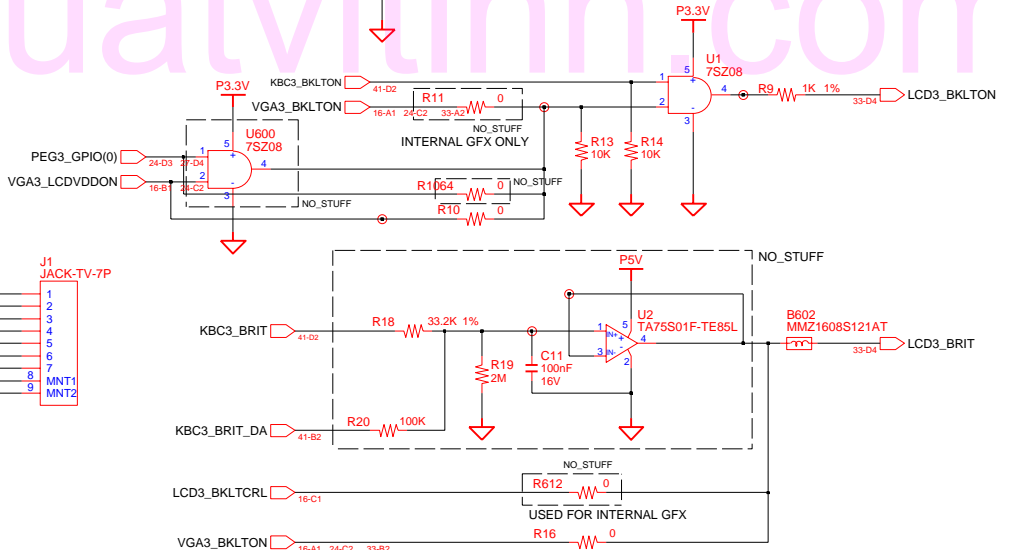
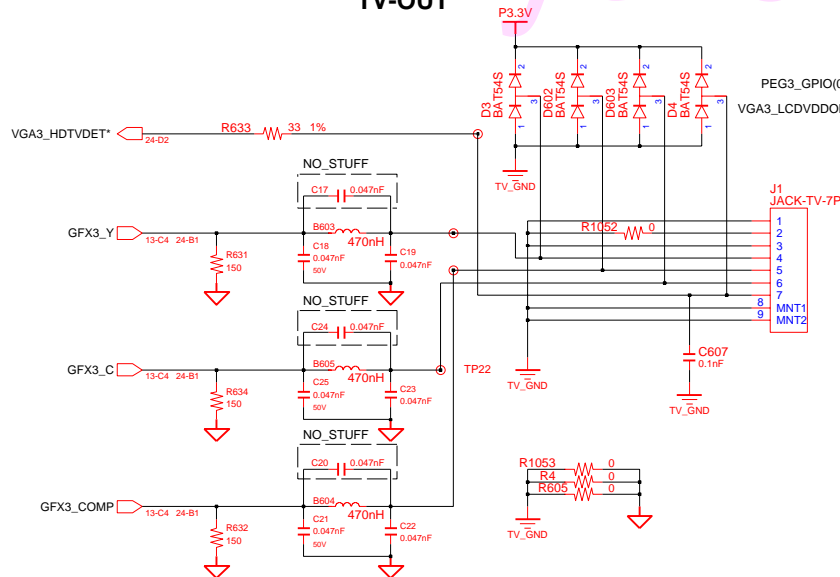
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LCD CONNECTOR



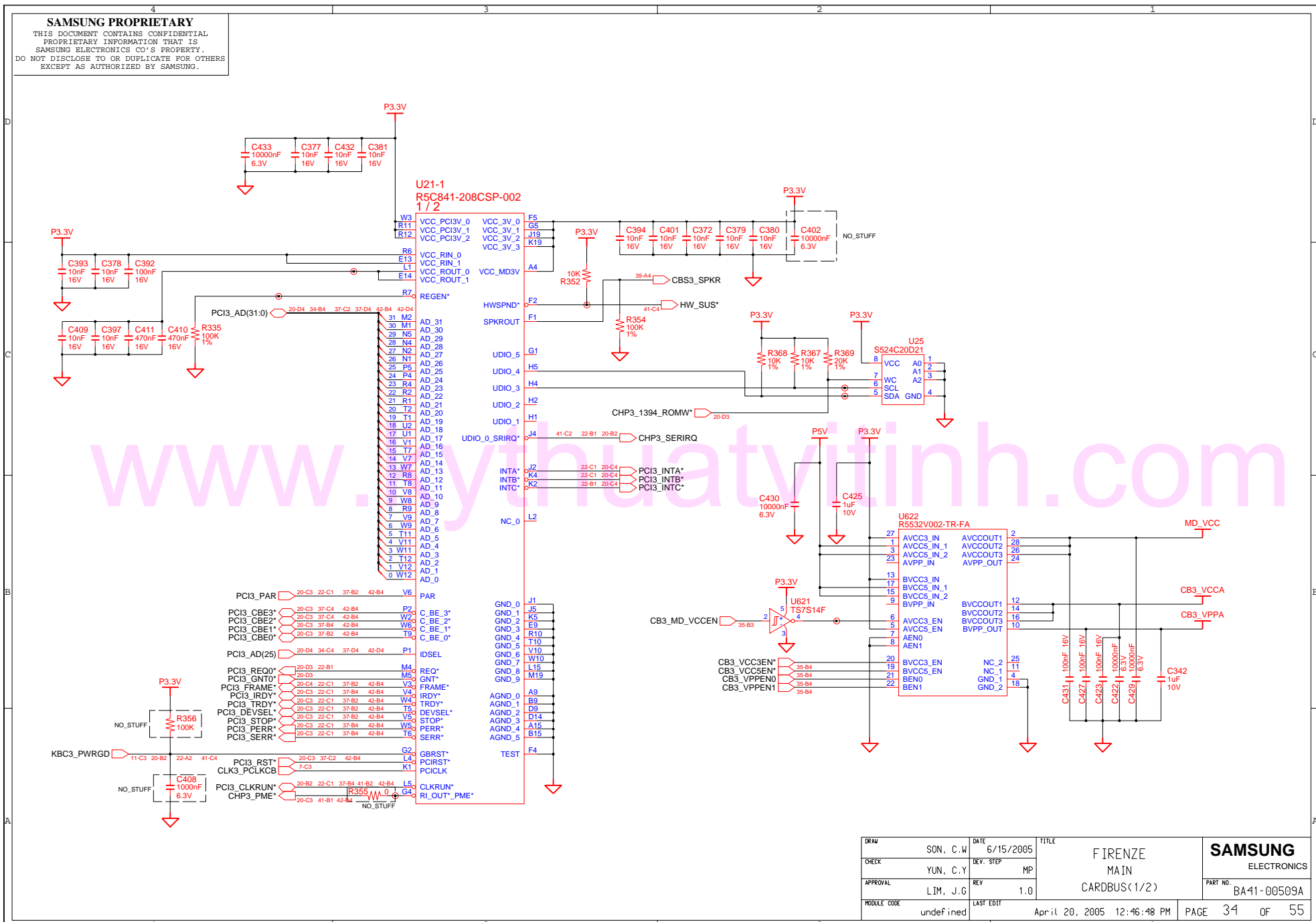
TV-OUT



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN	BA41-00509A	
APPROVAL	LIM, J.G	REV	1.0	LCD/TV-OUT		
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	33	OF 55

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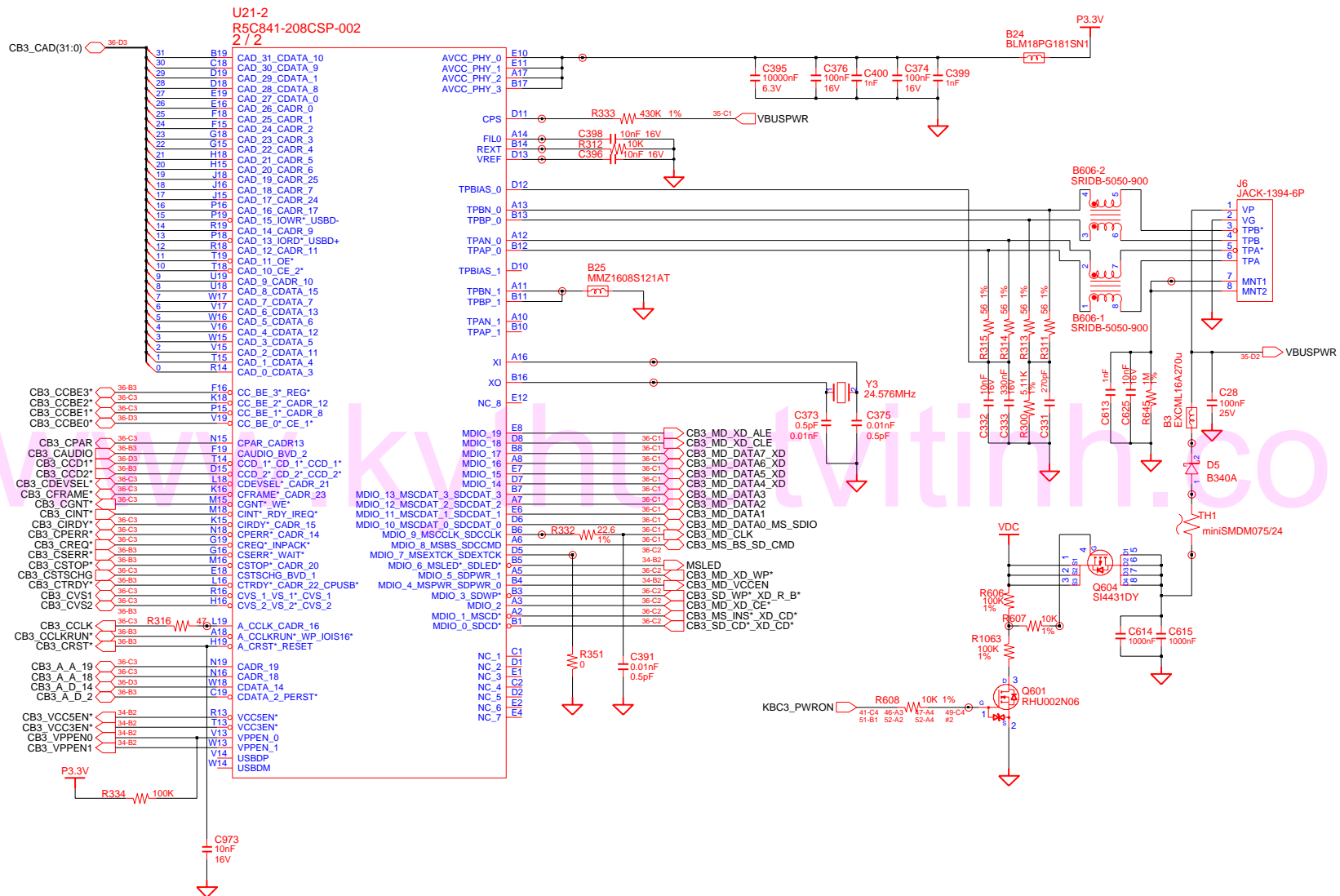


PCI3_PAR	20-C3	22-C1	37-B2	42-B4	V6	PAR
PCI3_CBE3*	20-C3	37-C4	42-B4		P2	C_BE_3*
PCI3_CBE2*	20-C3	37-C4	42-B4		19	C_BE_2*
PCI3_CBE1*	20-C3	37-B4	42-B4		W6	C_BE_1*
PCI3_CBE0*	20-C3	37-B2	42-B4		T9	C_BE_0*
PCI3_AD(25)	20-D4	34-C4	37-D4	42-D4	P1	IDSEL
PCI3_REQ0*	20-D3	22-B1			M4	REQ0*
PCI3_GNT0*	20-D3				M5	GNT0*
PCI3_FRAME*	20-C4	22-C1	37-B2	42-B4	V3	FRAME*
PCI3_IRDY*	20-C3	22-C1	37-B4	42-B4	V4	IRDY*
PCI3_TRDY*	20-C3	22-C1	37-B2	42-B4	W4	TRDY*
PCI3_DEVSEL*	20-C3	22-C1	37-B2	42-B4	T5	DEVSEL*
PCI3_STOP*	20-C3	22-C1	37-B2	42-B4	V5	STOP*
PCI3_PERR*	20-C3	22-C1	37-B4	42-B4	W5	PERR*
PCI3_SERR*	20-C3	22-C1	37-B4	42-B4	T6	SERR*
PCI3_RST*	20-C3	37-C2	42-B4		G2	GBRST*
CLK3_PCLKCB	7-C3				K1	PCIRST*
PCI3_CLKRUN*	20-B2	22-C1	37-B4	41-B2	L5	CLKRUN*
CHP3_PME	20-C3	41-B1	42-B4		G4	RI_OUT*_PME*

DRAW	SON, C. W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	MP		CARBUS(1/2)	
APPROVAL	LIM, J. G	REV	1.0			PART NO. BA41-00509A
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	34	OF 55

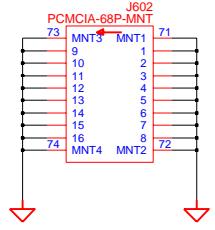
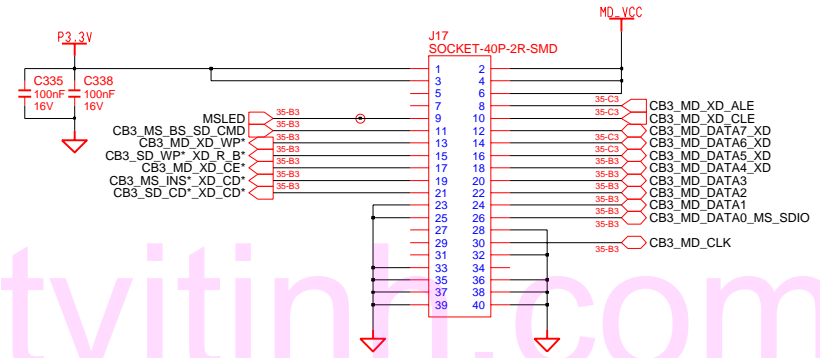
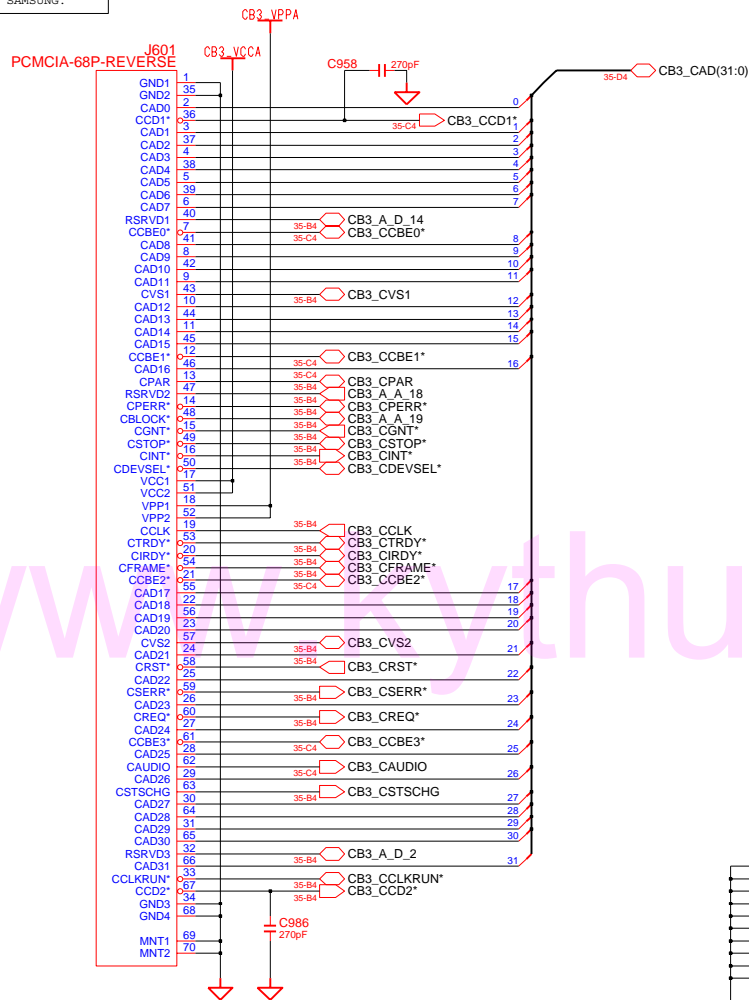
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CARDBUS(2/2)	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	35 OF 55	

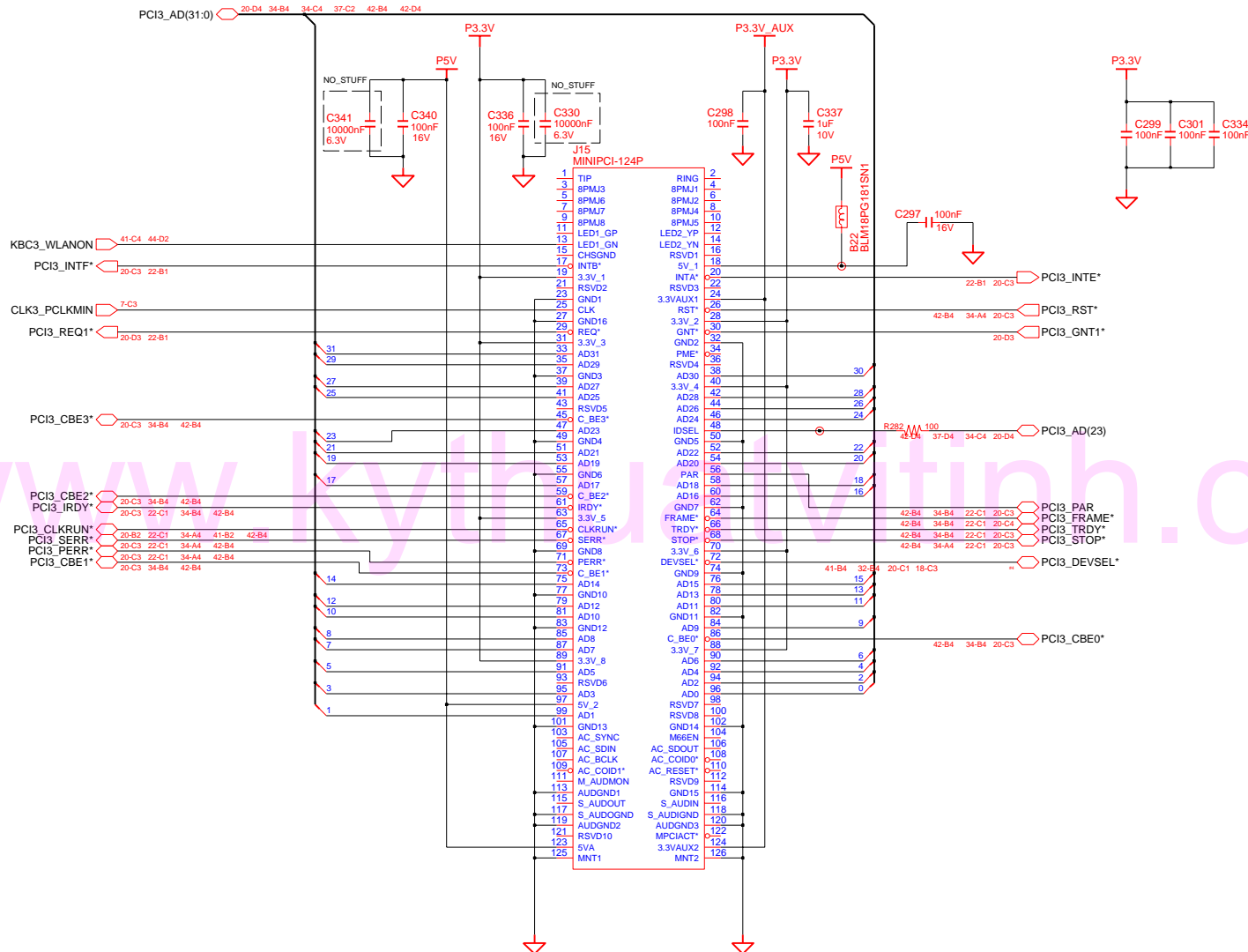
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DRAW	SON, C. W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	MP	REV	1.0	
APPROVAL	LIM, J. G	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	36 OF 55	PART NO. BA41-00509A
MODULE CODE	undef:ined					

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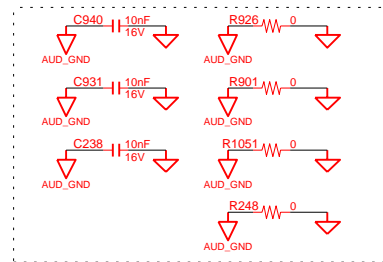
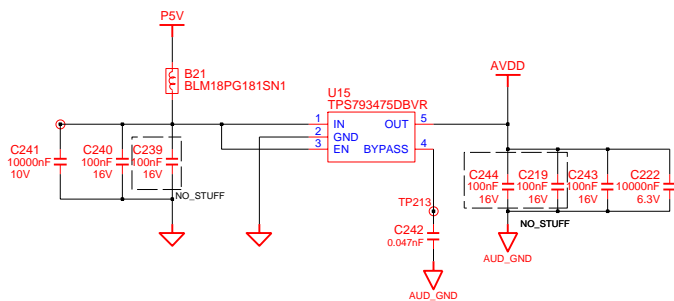
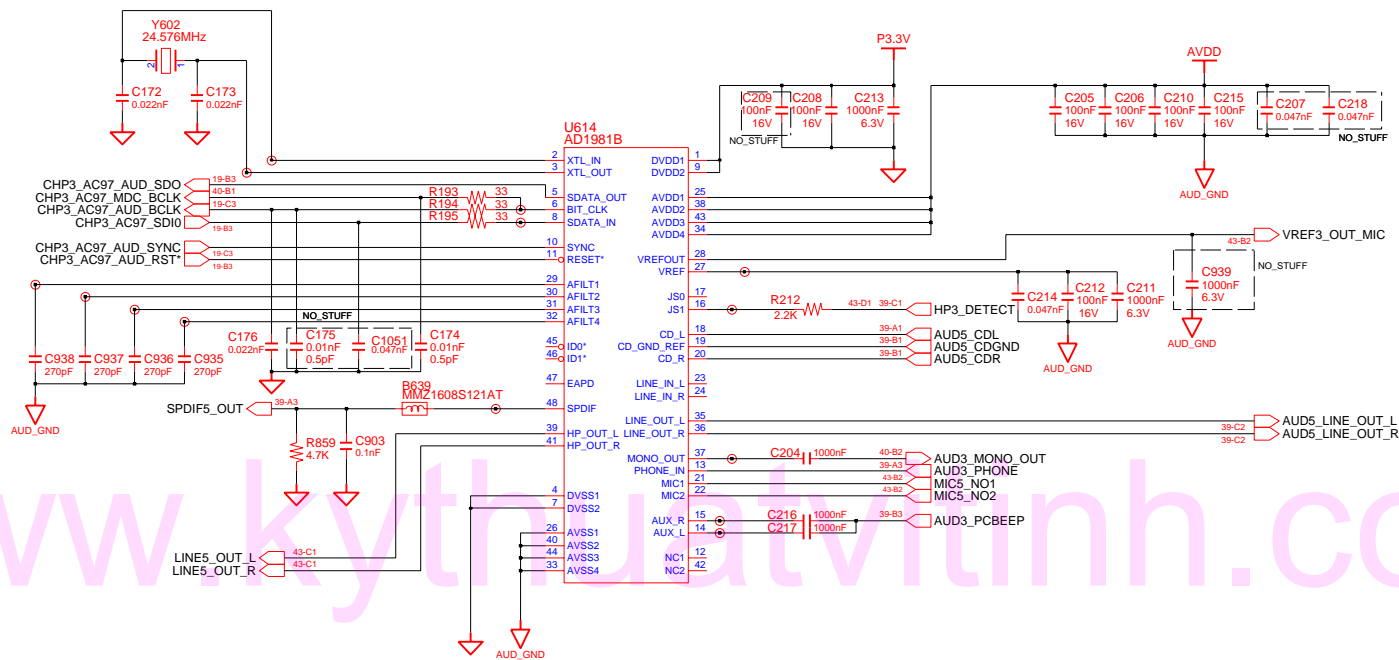
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE 37 OF 55		

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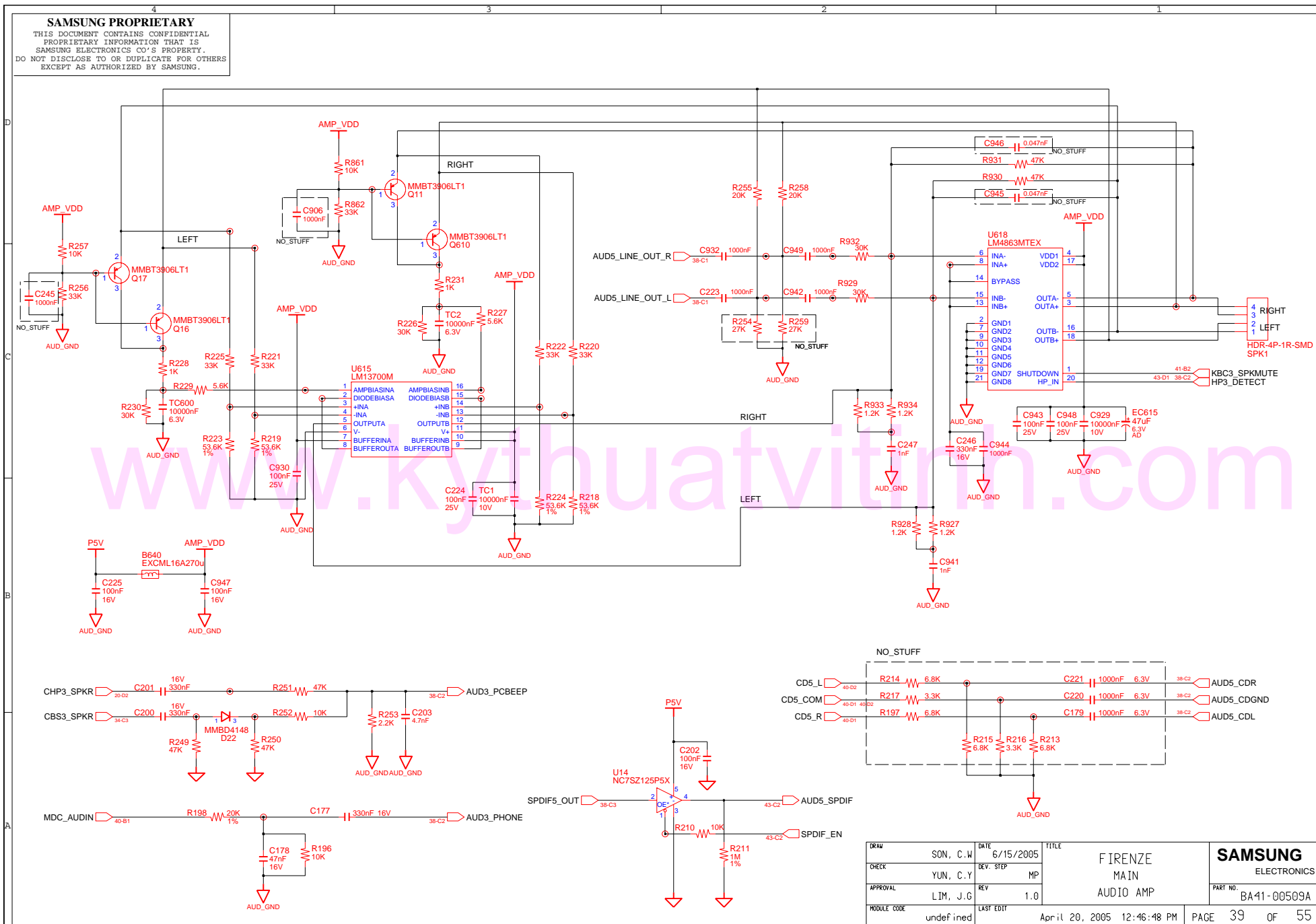
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00509A
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	38	OF 55

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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN AUDIO AMP	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	39 OF 55	

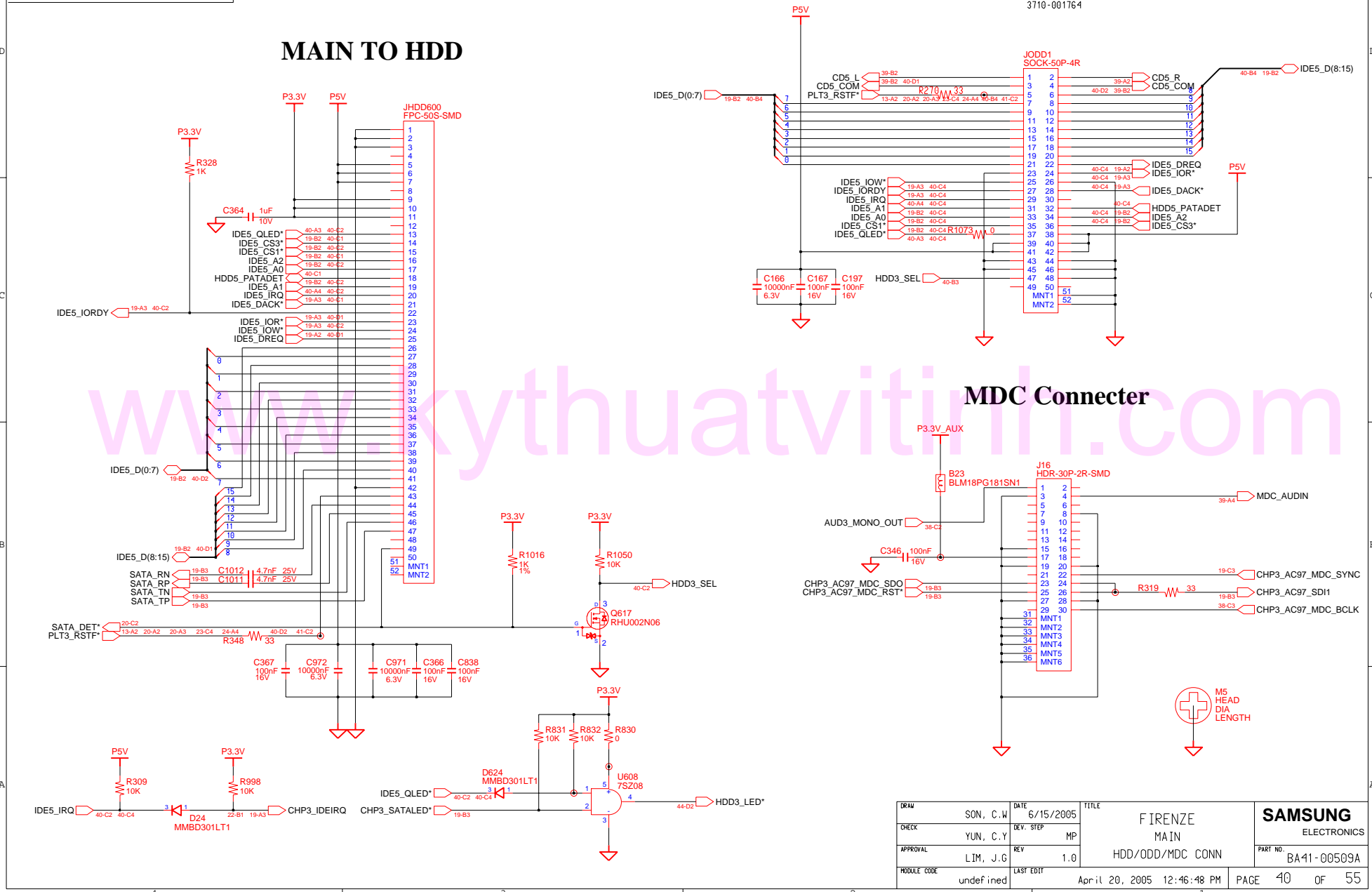
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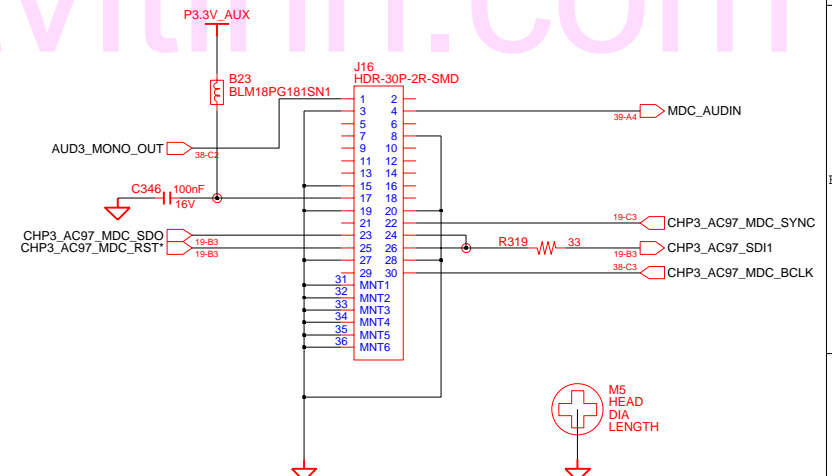
MAIN TO ODD

3710-001764

MAIN TO HDD



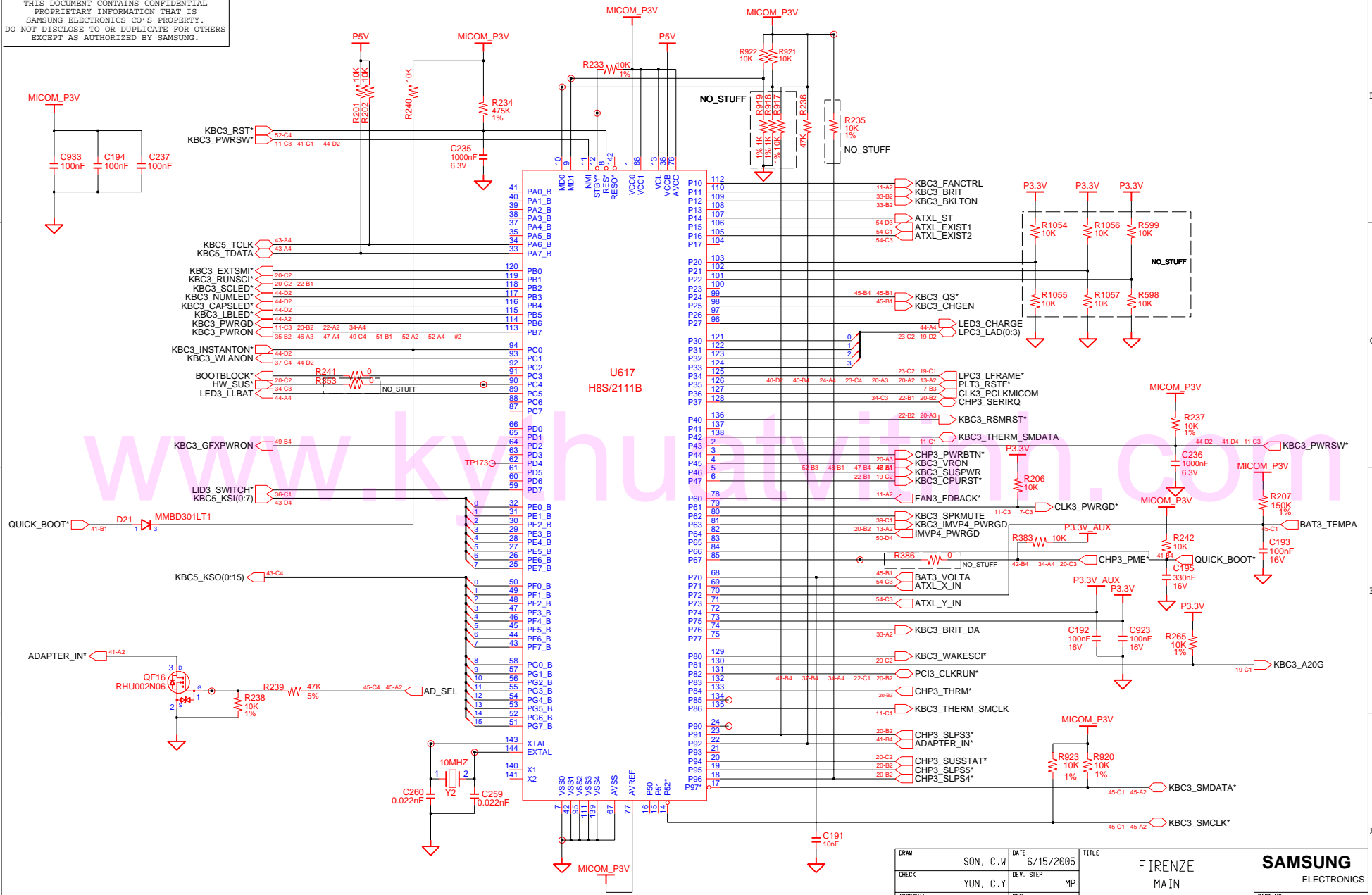
MDC Connector



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN HDD/ODD/MDC CONN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	REV		
APPROVAL	LIM, J.G	REV	1.0	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE 40 OF 55
MODULE CODE	undefined					PART NO. BA41-00509A

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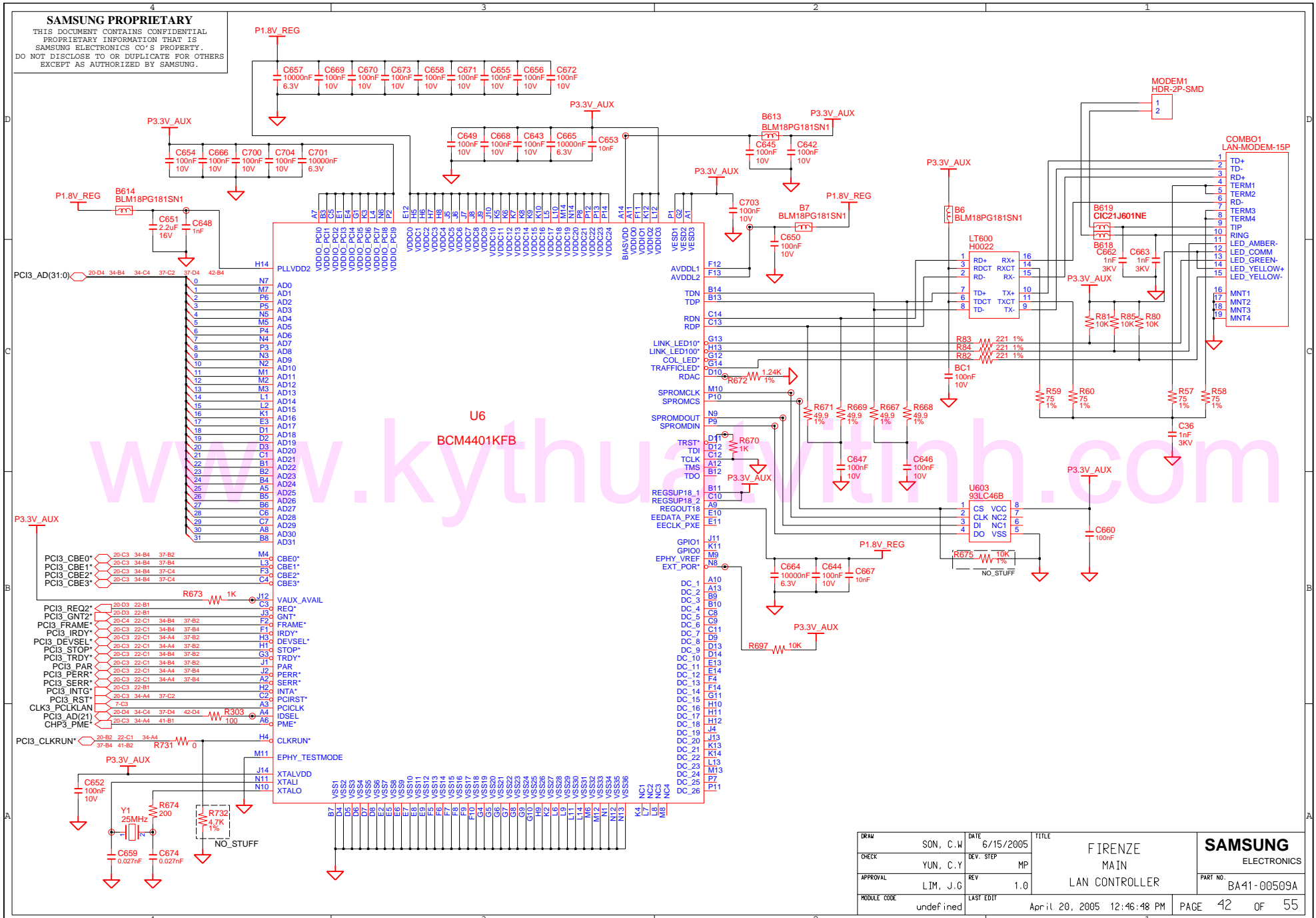
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	MP		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0		MICOM	PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			PAGE 41 OF 55

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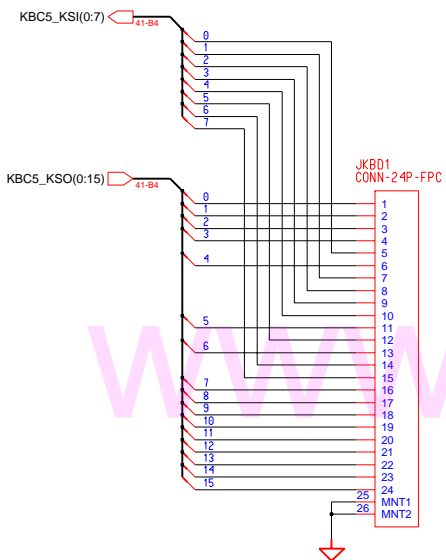
DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	42 OF 55	

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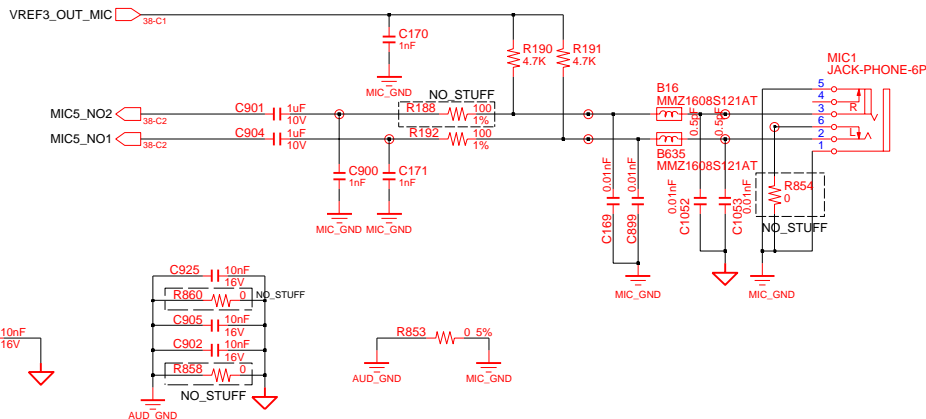
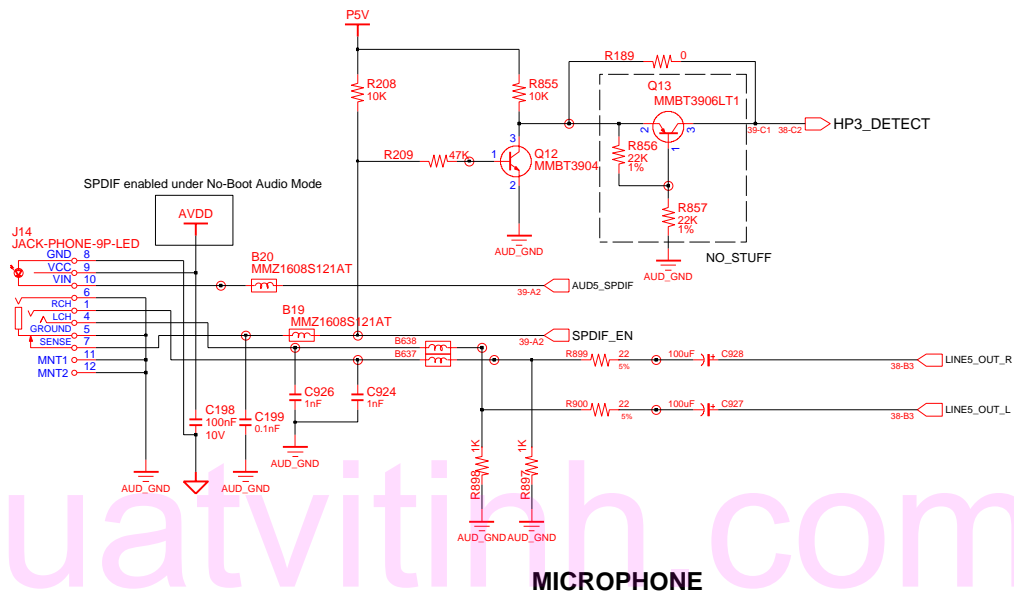
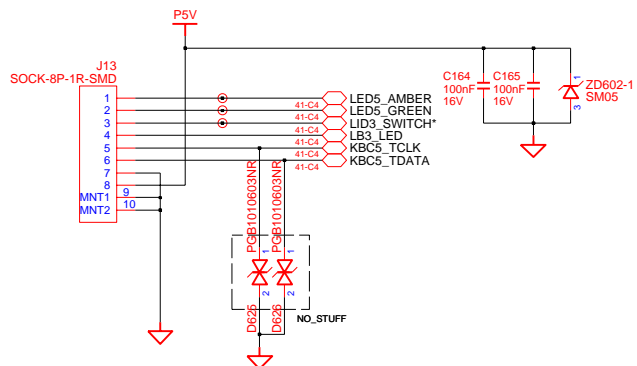
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OPTICAL SPDIF OUTPUT & HEADPHONE

KEYBOARD



TOUCH PAD

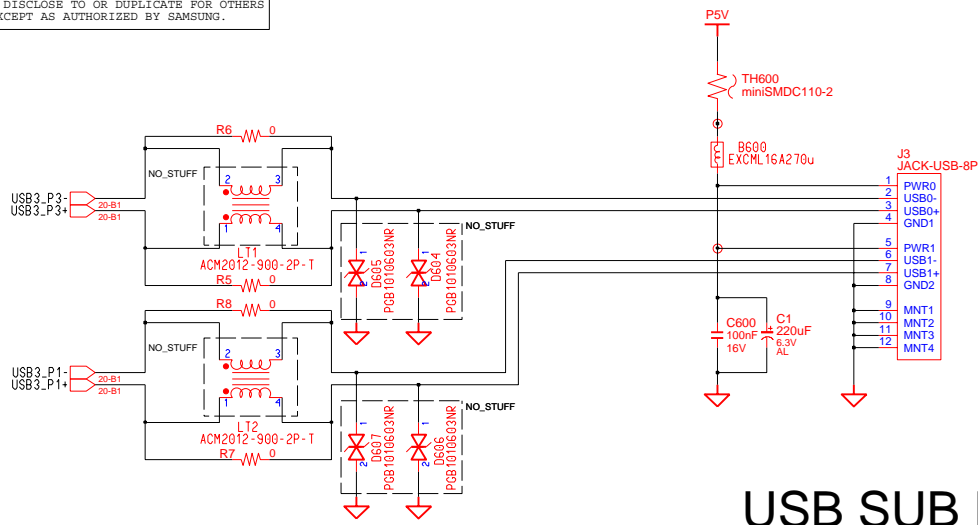


DRAW	SON, C. W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	MP	KBD/TPAD/HP/MIC		
APPROVAL	LIM, J. G	REV	1.0	PAGE 43 OF 55		PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			

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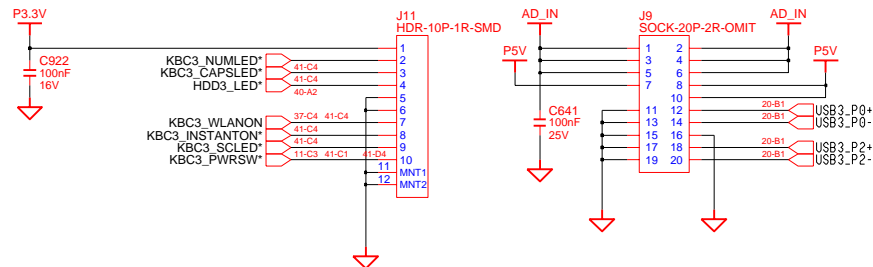
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USB PORT

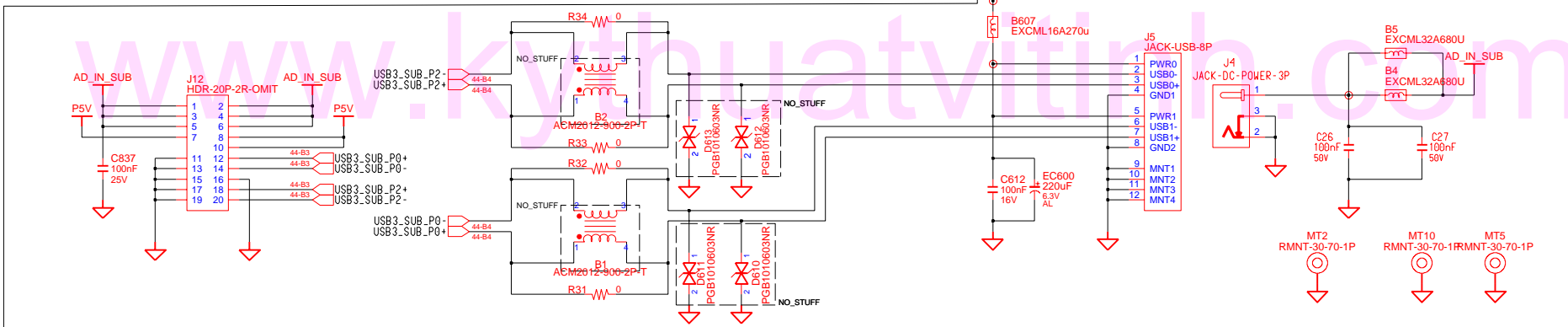


MAIN TO ON-TOP

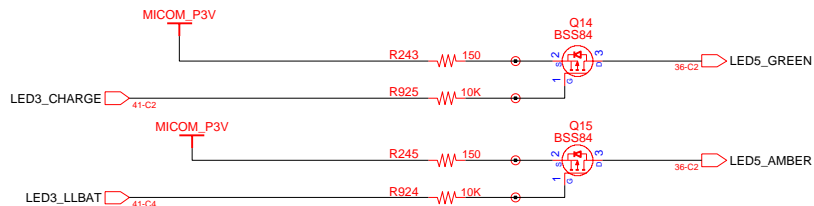
MAIN TO USB



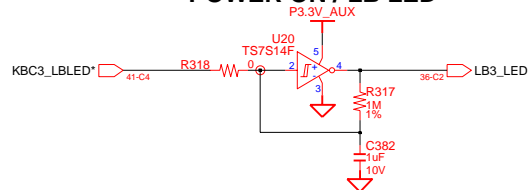
USB SUB B'D



ADAPTER IN / CHARGER LED



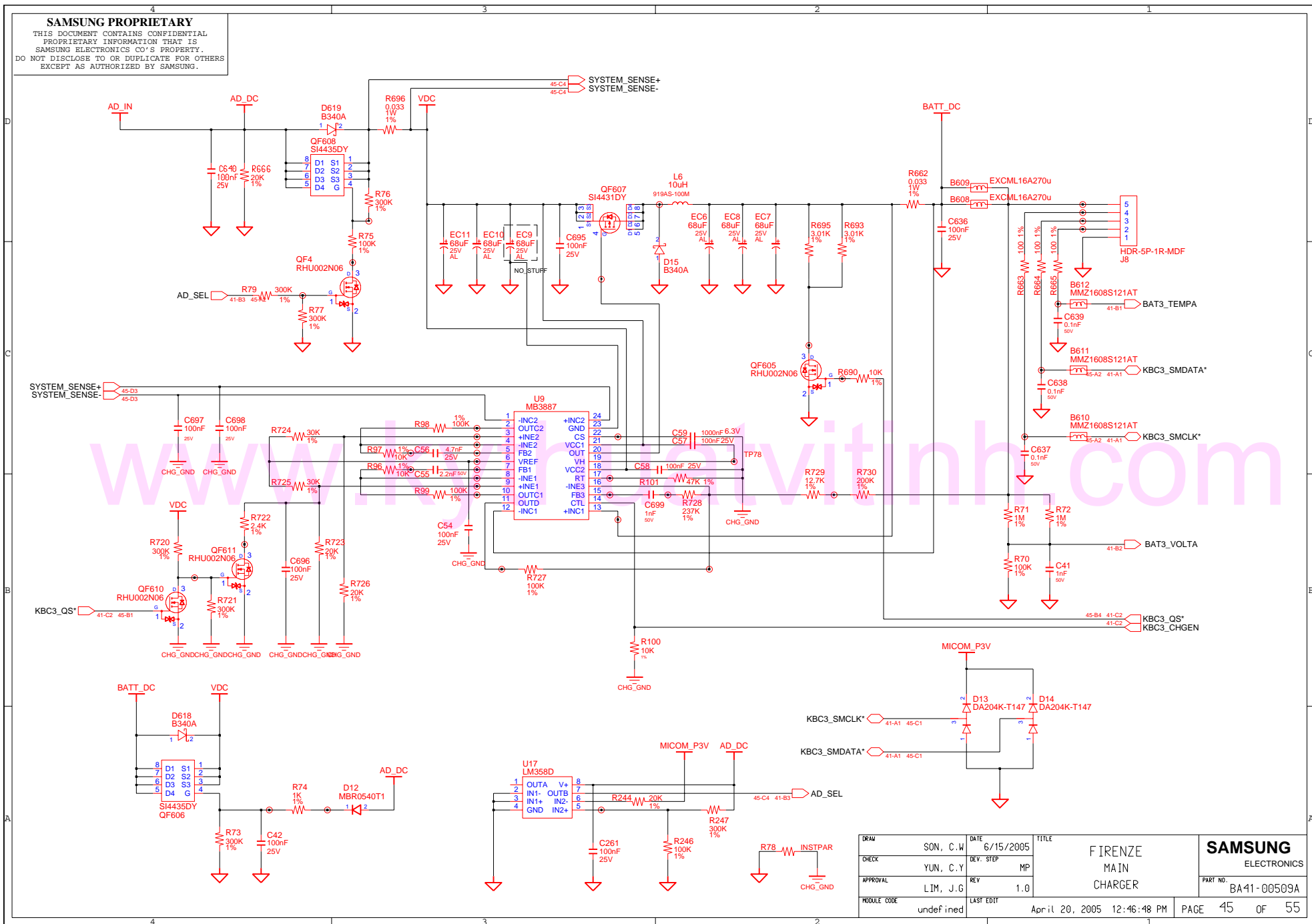
POWER ON / LB LED



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G	REV	1.0	USB PORT/LED/ON-TOP	PART NO.	BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	44	OF 55

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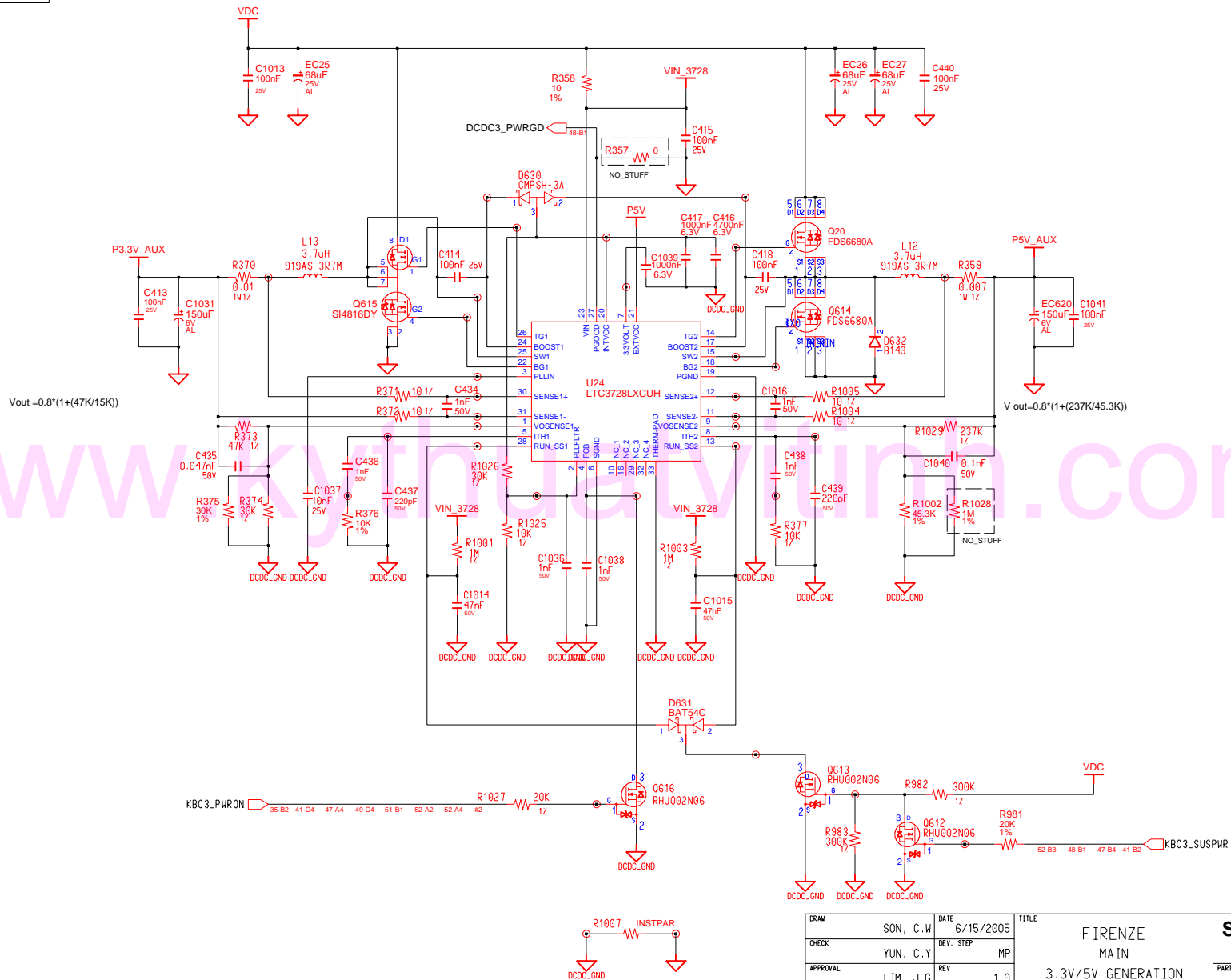
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE 45 OF 55		

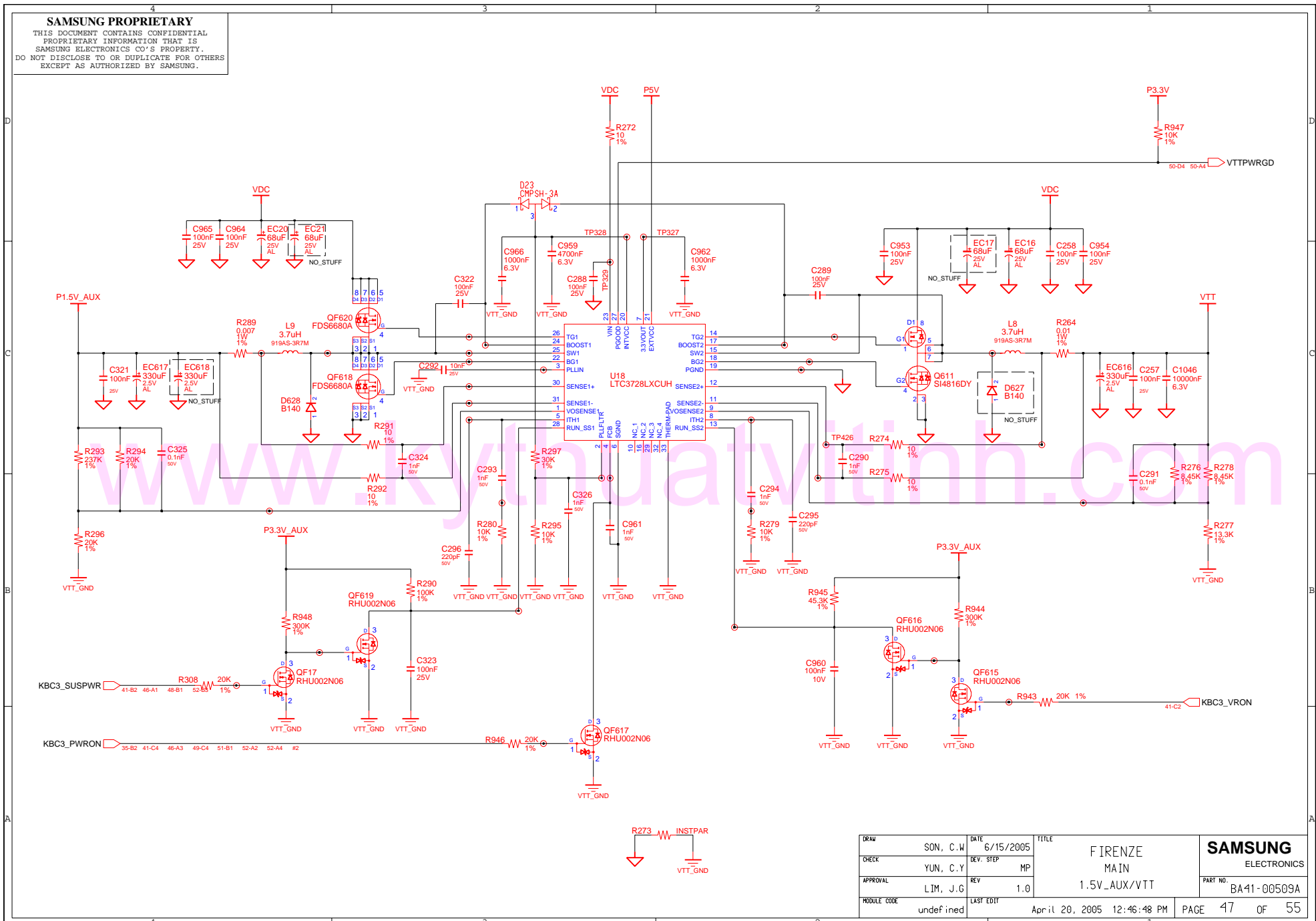
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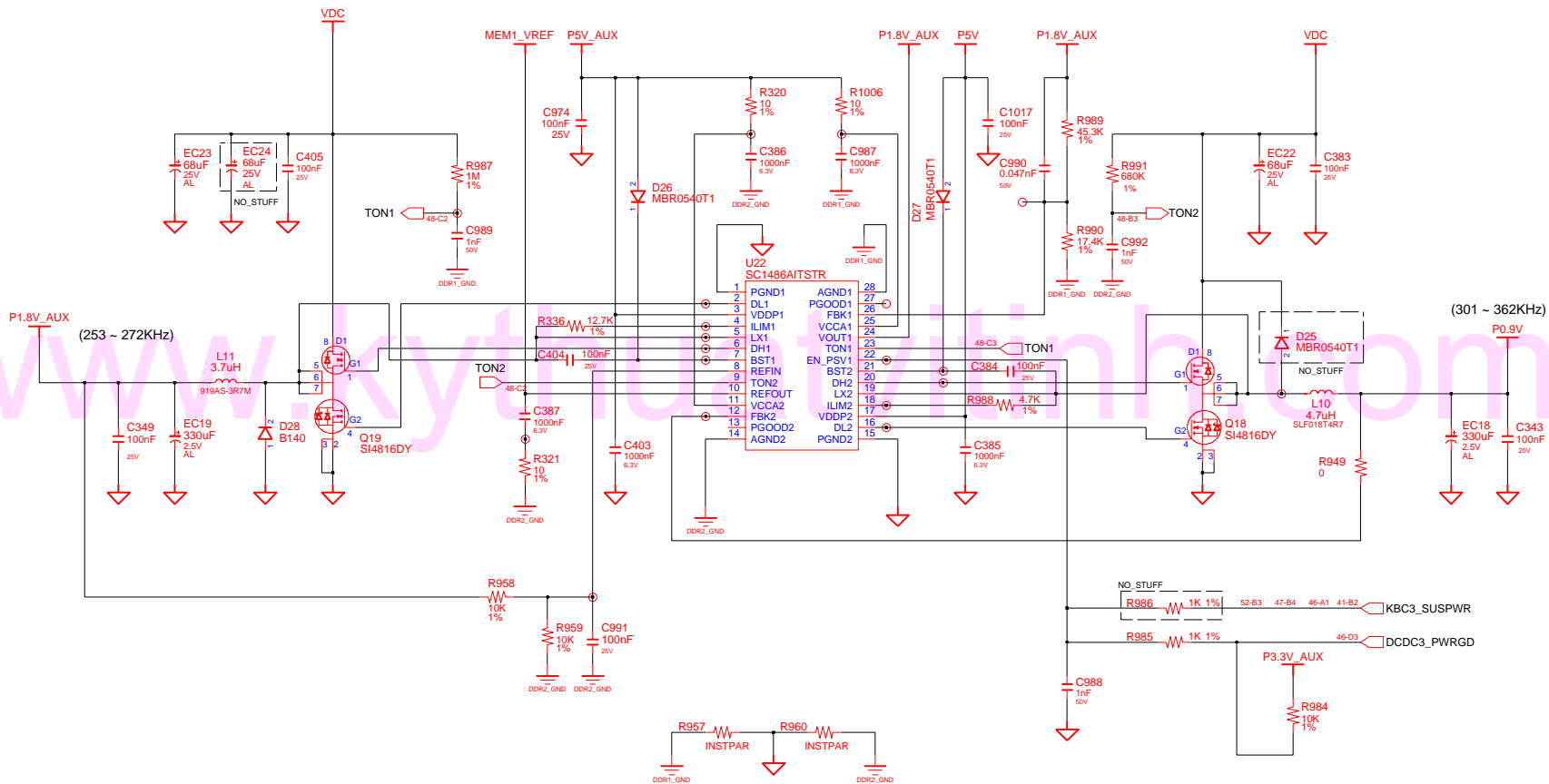


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN 1.5V_AUX/VTT	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP	REV		
APPROVAL	LIM, J.G	REV	1.0	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE 47 OF 55
MODULE CODE	undefind					

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DDR2 POWER

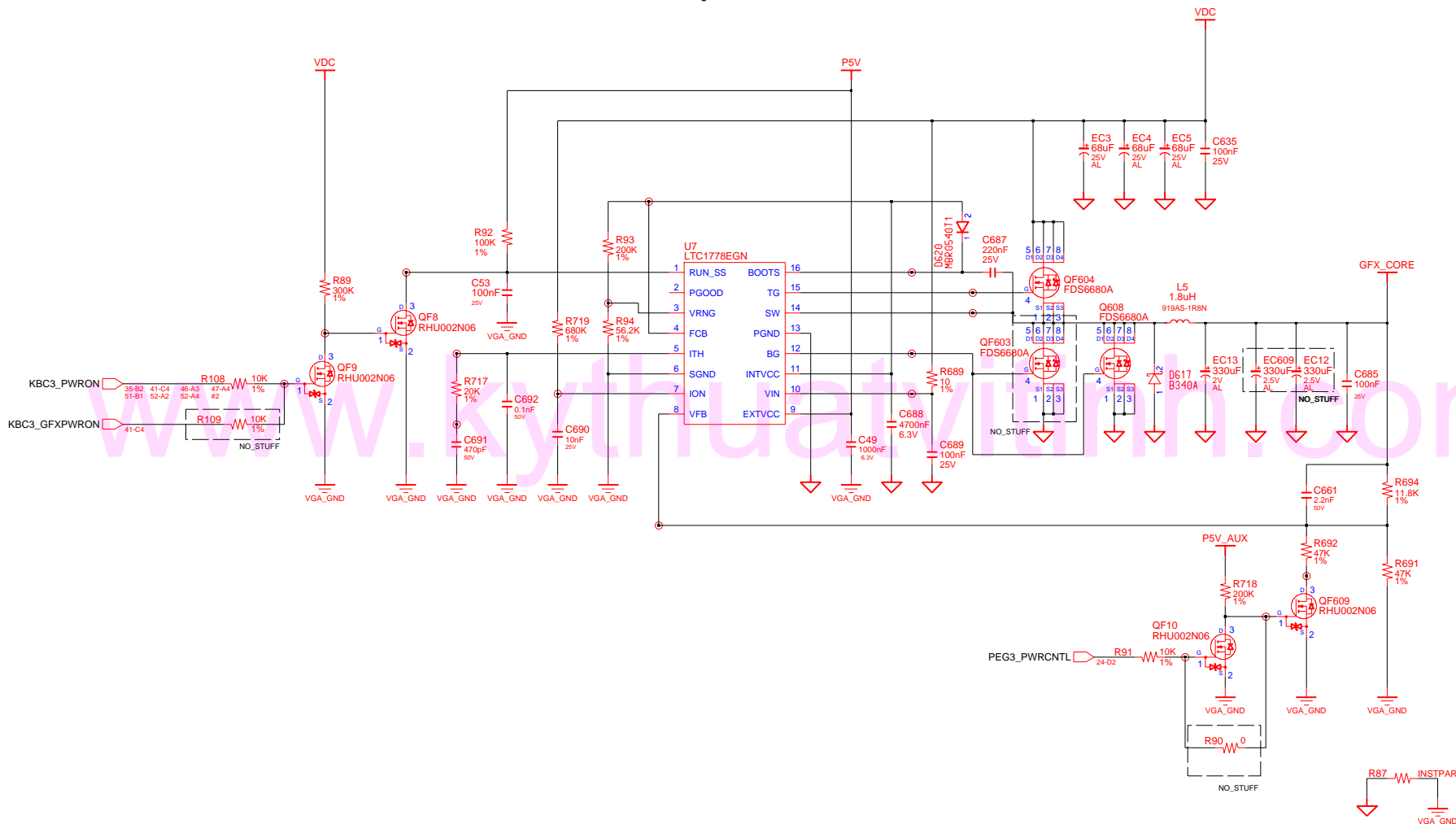


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP		DDR2 POWER	
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef:ned	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	48	OF 55

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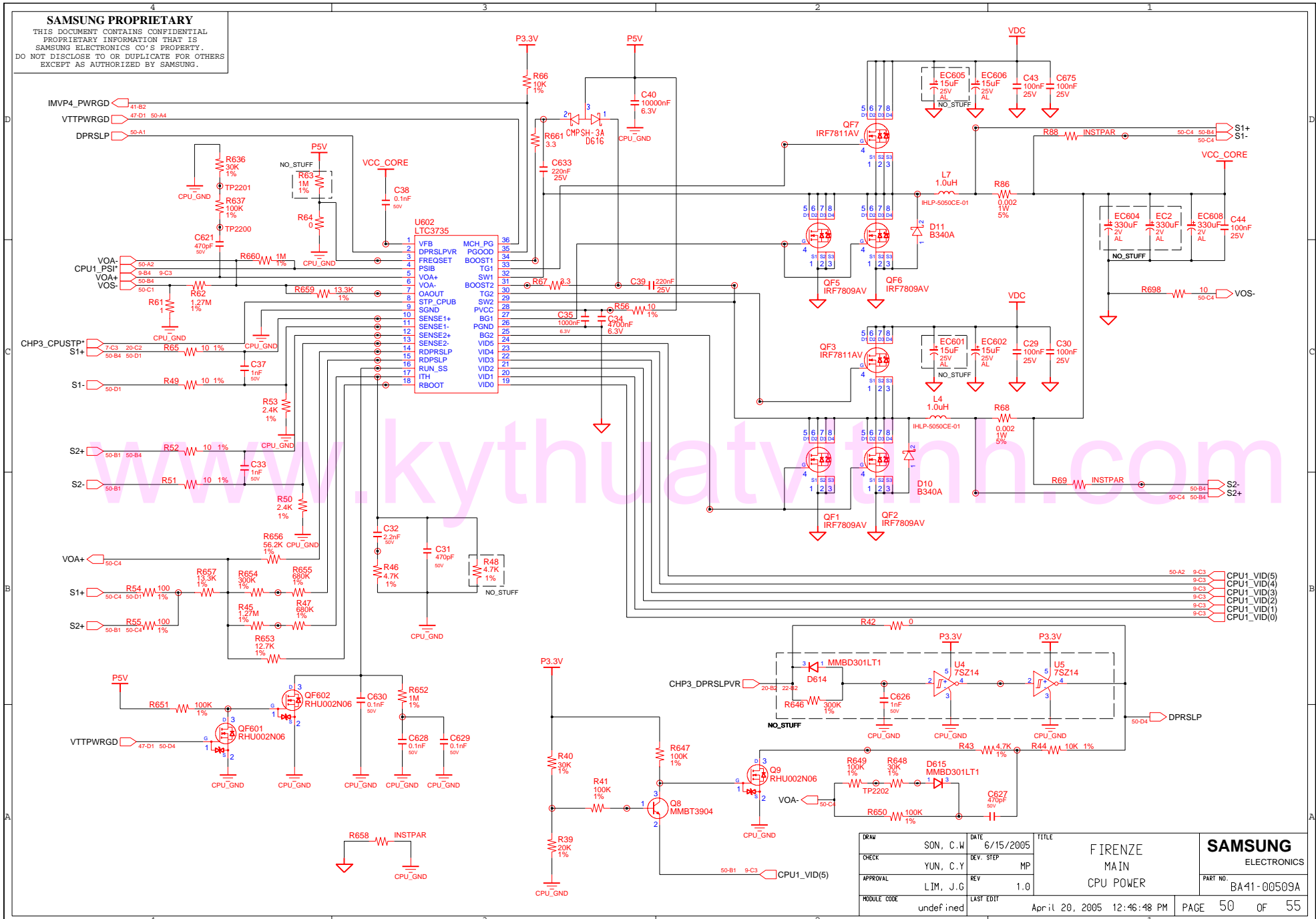
Graphic Core Power



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN GRAPHIC CORE POWER	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE 49 OF 55		

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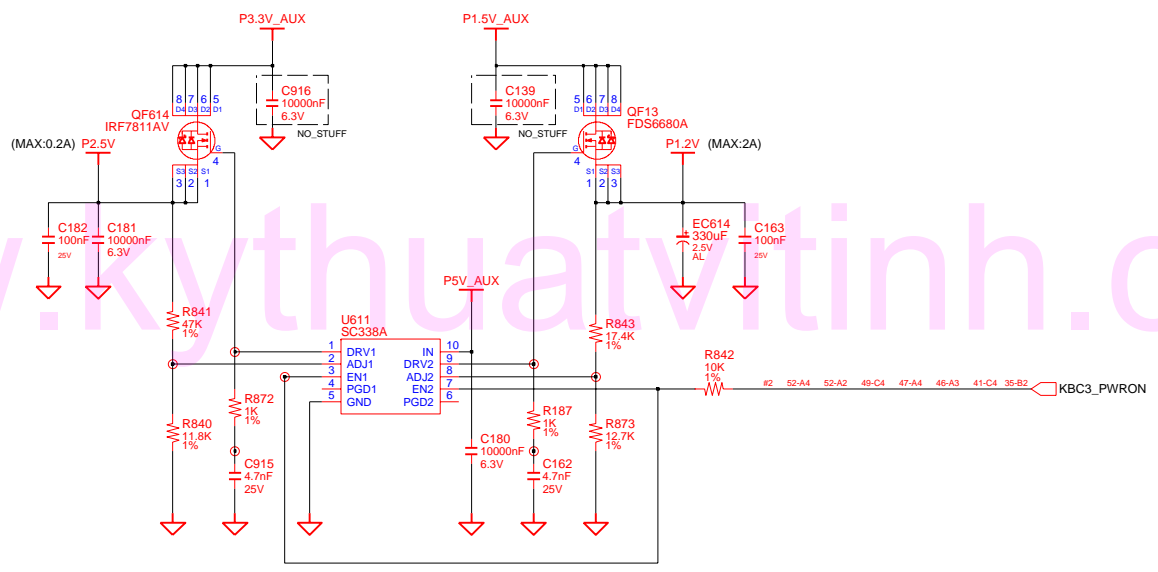
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	50 OF 55	

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P1.2V / P2.5V POWER

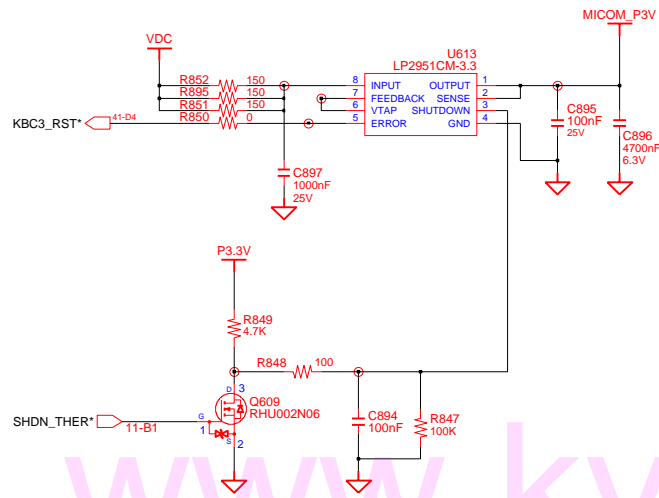


DRAW	SON, C. W	DATE	6/15/2005	TITLE	FIRENZE MAIN 1.2V/2.5V POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	MP			
APPROVAL	LIM, J. G	REV	1.0		PART NO.	BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	51	OF 55

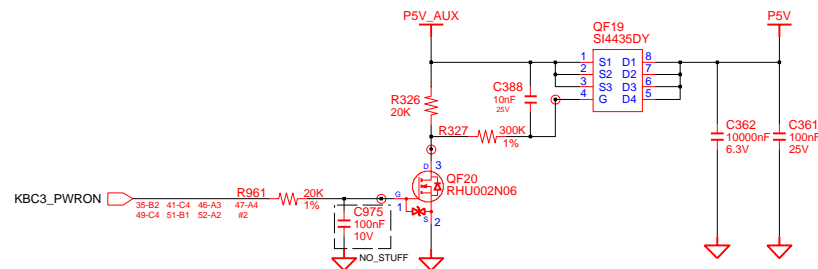
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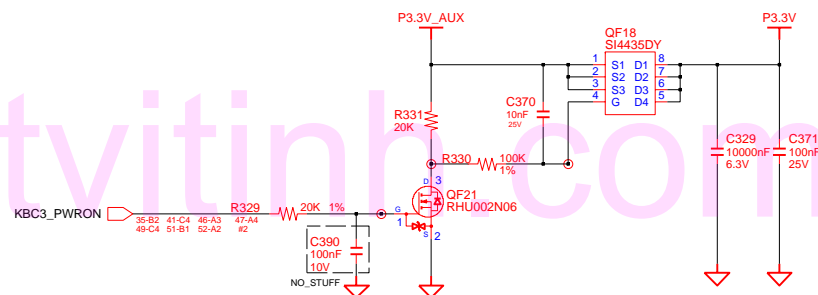
MICOM_P3V Power



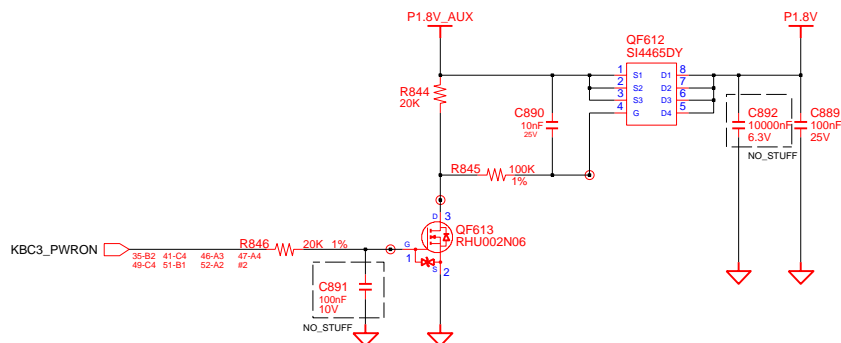
Switched Power On (P5V)



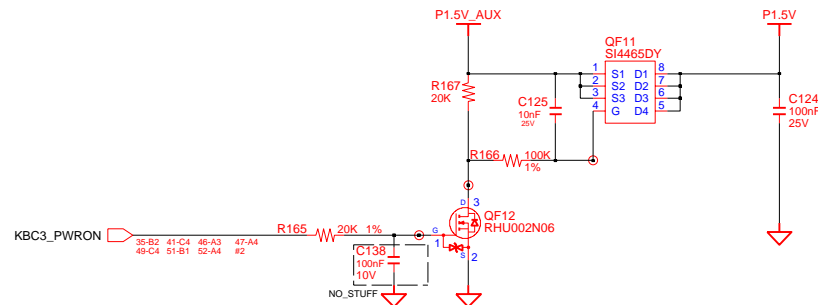
Switched Power On (P3.3V)



Switched Power On (P1.8V)



Switched Power On (P1.5V)

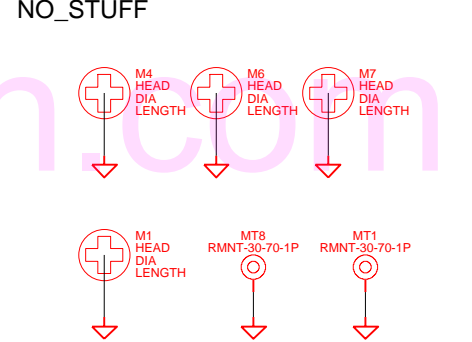
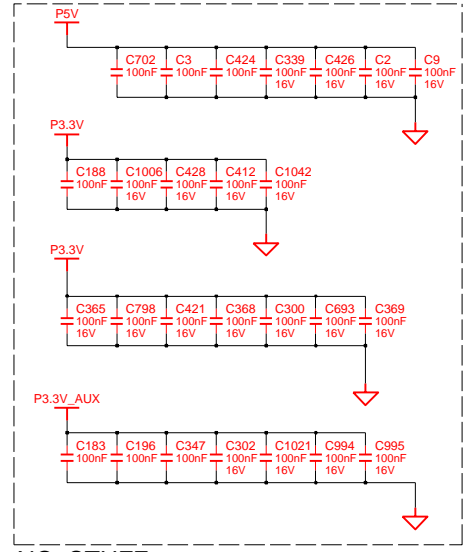
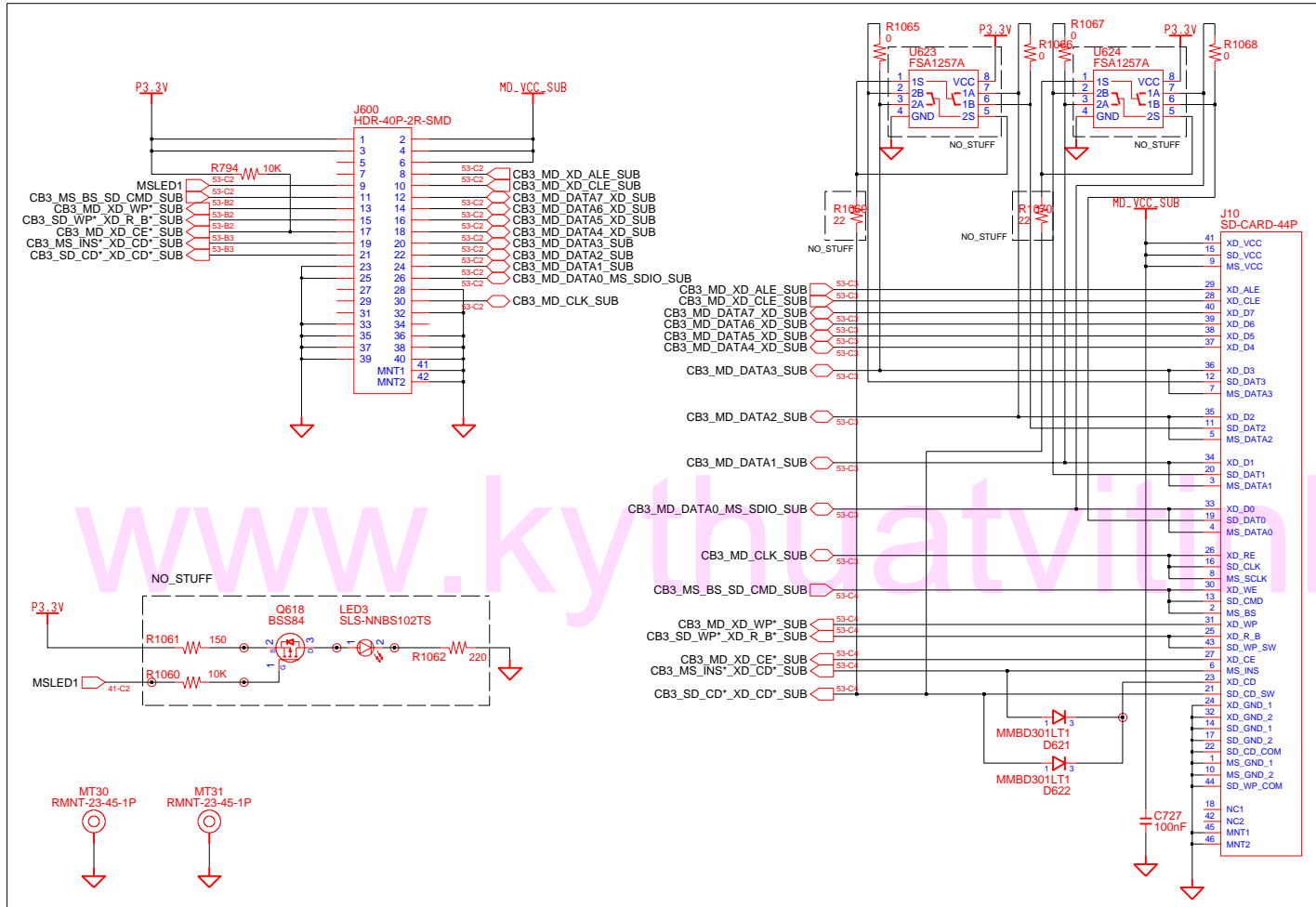


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	MICOM&SWITCHED POWER		
APPROVAL	LIM, J.G	REV	1.0	PART NO. BA41-00509A		PAGE 52 OF 55
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			

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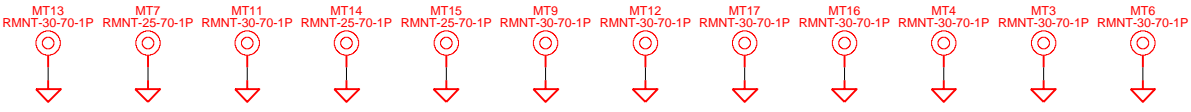
5-IN-1 SUB B'D



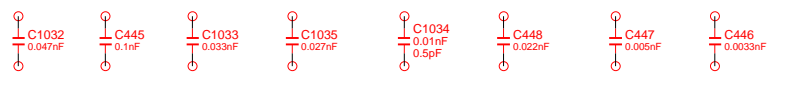
PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV600
1
2 3

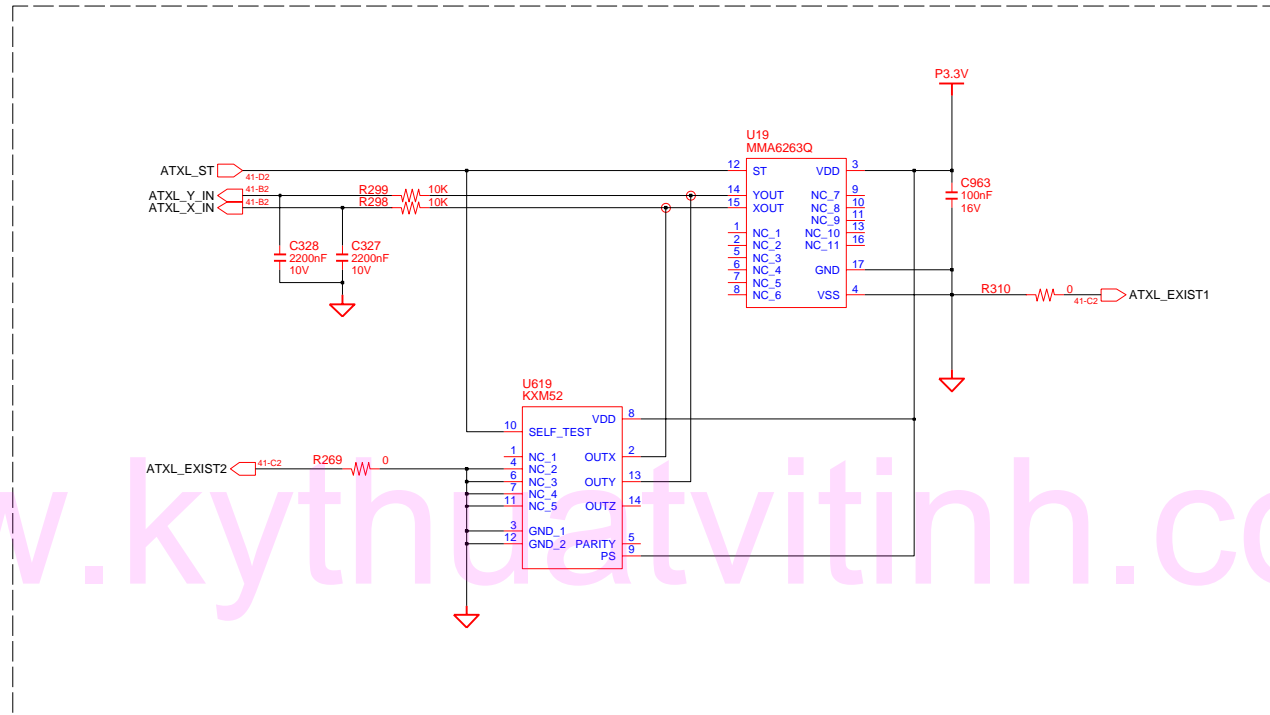


CAPS FOR ICT TEST

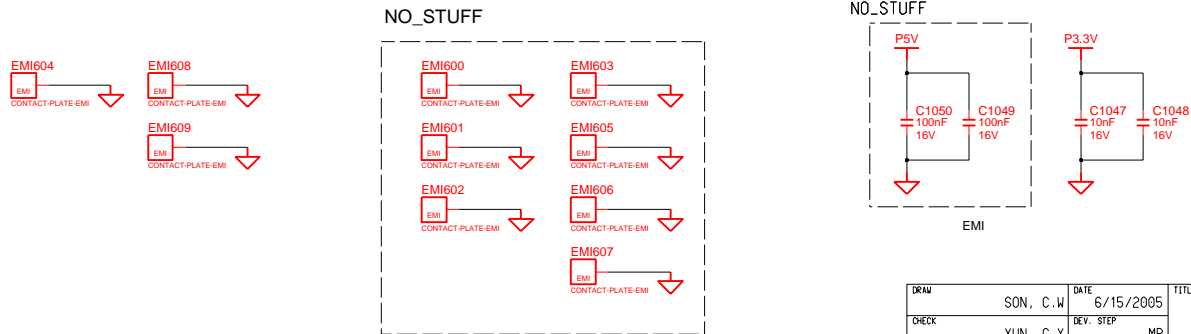


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	REV	1.0	PART NO. BA-01-00509A
APPROVAL	LIM, J.G	LAST EDIT	Apr 10, 2005 12:46:48 PM	PAGE	53	OF 55
MODULE CODE	undefined					

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NO_STUFF



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN AIR BAG	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP	PART NO.		
APPROVAL	LIM, J.G	REV	1.0	BA41-00509A		
MODULE CODE	undef ined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE 54 OF 55		

