

IRF530, IRF531, IRF532, IRF533

Power MOS Field-Effect Transistors

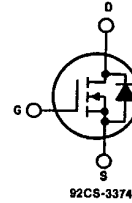
N-Channel Enhancement-Mode Power Field-Effect Transistors

12A and 14A, 60V-100V
 $r_{DS(on)} = 0.18 \Omega$ and 0.25Ω

Features:

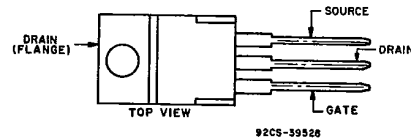
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF530, IRF531, IRF532 and IRF533 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Datasheet.Directory

Absolute Maximum Ratings

Parameter	IRF530	IRF531	IRF532	IRF533	Units
V_{DS} Drain - Source Voltage (1)	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) (1)	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	14	14	12	12	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM} Pulsed Drain Current (2)	56	56	48	48	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	75 (See Fig. 14)				W
Linear Derating Factor	0.8 (See Fig. 14)				W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100 \mu\text{H}$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
T_{atg} Lead Temperature	300 (0.063 in (1.6mm) from case for 10s)				$^\circ\text{C}$

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Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain-Source Breakdown Voltage	IRF530 IRF532	100	—	—	V	V _{GS} = 0V I _D = 250μA
	IRF531 IRF533	60	—	—	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
		—	—	1000	μA	
I _{D(on)} On-State Drain Current ②	IRF530 IRF531	14	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V
	IRF532 IRF533	12	—	—	A	
R _{DS(on)} Static Drain-Source On State Resistance ②	IRF530 IRF531	—	0.14	0.18	Ω	V _{GS} = 10V, I _D = 8.0A
	IRF532 IRF533	—	0.20	0.25	Ω	
g _{fs} Forward Transconductance ②	ALL	4.0	5.5	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 8.0A
C _{iss} Input Capacitance	ALL	—	600	800	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	—	300	500	pF	
C _{rss} Reverse Transfer Capacitance	ALL	—	100	150	pF	
t _{d(on)} Turn-On Delay Time	ALL	—	—	30	ns	V _{DD} = 36V, I _D = 8.0A, Z ₀ = 15Ω See Fig. 17
t _r Rise Time	ALL	—	—	75	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	—	40	ns	IMOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	—	—	45	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V _{GS} = 10V, I _D = 18A, V _{DS} = 0.8 Max. Rating See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	—	9.0	—	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
		—	4.5	—	nH	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

R _{thJC} Junction to Case	ALL	—	—	1.67	°C/W	Mounting surface flat, smooth, and greased. Free Air Operation
R _{thCS} Case to Sink	ALL	—	1.0	—	°C/W	
R _{thJA} Junction to Ambient	ALL	—	—	80	°C/W	

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF530 IRF531	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF532 IRF533	—	—	12	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRF530 IRF531	—	—	56	A	
	IRF532 IRF533	—	—	48	A	
V _{SD} Diode Forward Voltage ②	IRF530 IRF531	—	—	2.5	V	T _C = 25°C, I _S = 14A, V _{GS} = 0V
	IRF532 IRF533	—	—	2.3	V	
t _{rr} Reverse Recovery Time	ALL	—	360	—	ns	T _J = 150°C, I _F = 14A, dI _F /dt = 100A/μs
Q _{RR} Reverse Recovered Charge	ALL	—	2.1	—	μC	T _J = 150°C, I _F = 14A, dI _F /dt = 100A/μs
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C ② Pulse Test: Pulse width < 300μs, Duty Cycle < 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

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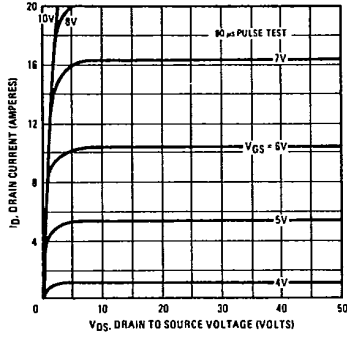


Fig. 1 - Typical Output Characteristics

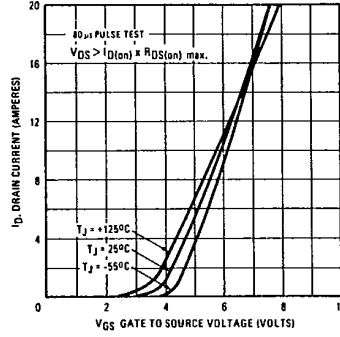


Fig. 2 - Typical Transfer Characteristics

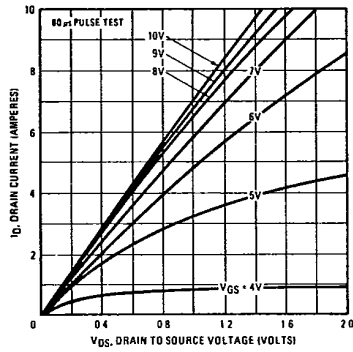


Fig. 3 - Typical Saturation Characteristics

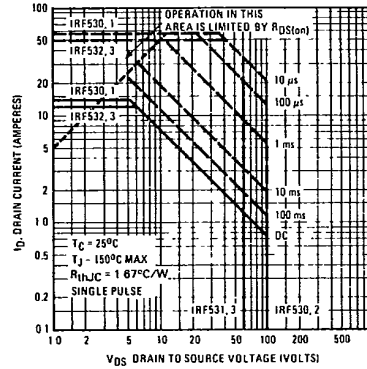


Fig. 4 - Maximum Safe Operating Area

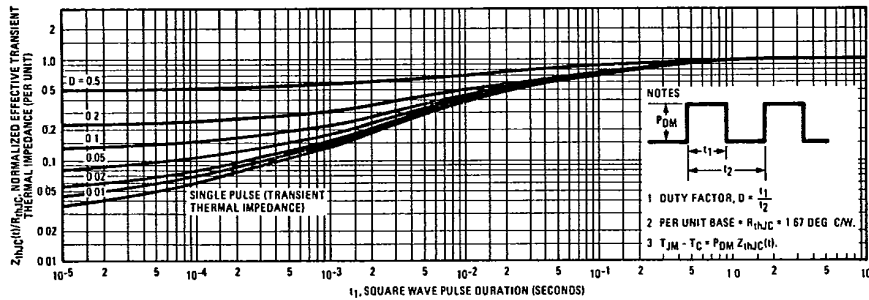


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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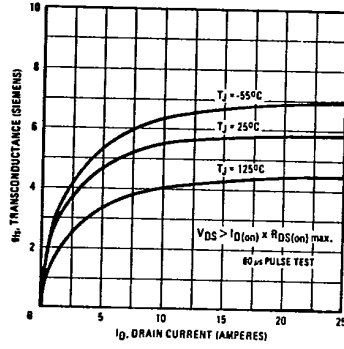


Fig. 6 - Typical Transconductance Vs. Drain Current

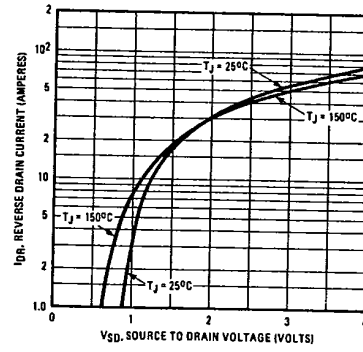


Fig. 7 - Typical Source-Drain Diode Forward Voltage

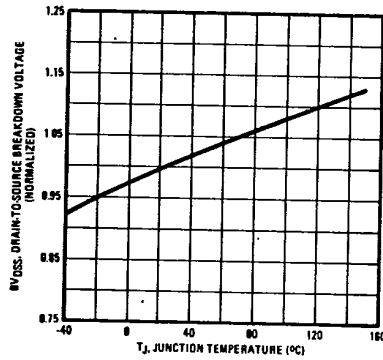


Fig. 8 - Breakdown Voltage Vs. Temperature

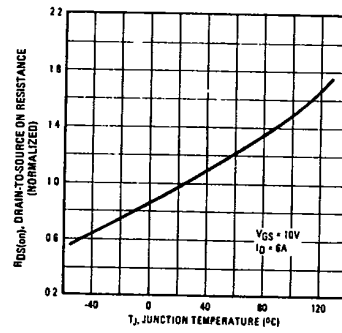


Fig. 9 - Normalized On-Resistance Vs. Temperature

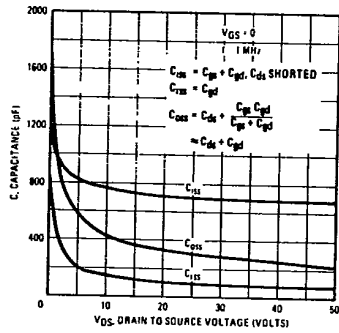


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

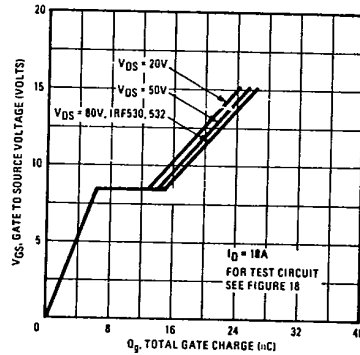


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

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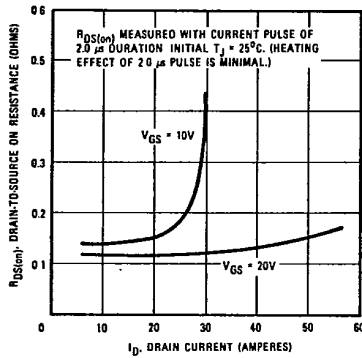


Fig. 12 - Typical On-Resistance Vs. Drain Current

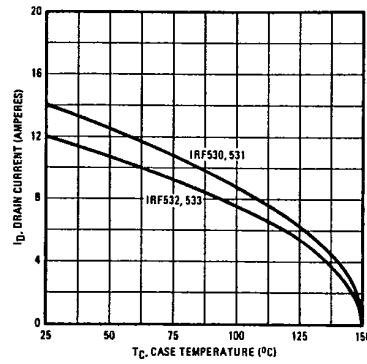


Fig. 13 - Maximum Drain Current Vs. Case Temperature

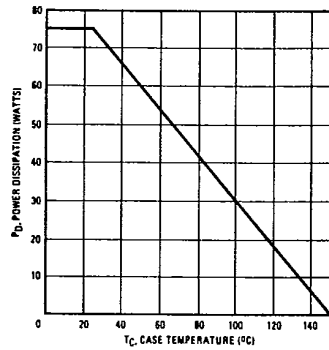


Fig. 14 - Power Vs. Temperature Derating Curve

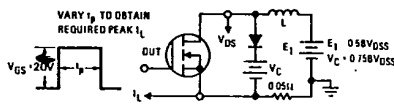


Fig. 15 - Clamped Inductive Test Circuit

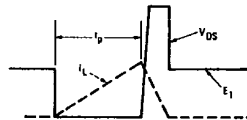


Fig. 16 - Clamped Inductive Waveforms

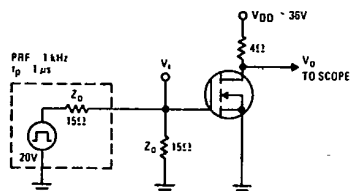


Fig. 17 - Switching Time Test Circuit

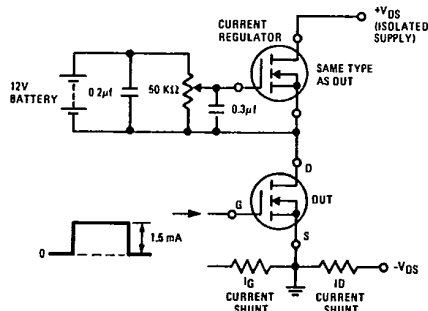


Fig. 18 - Gate Charge Test Circuit