# AN10907

## TEA1613T resonant power supply control IC

Rev. 1 — 28 December 2010 Application note

### Document information

| Info | Content |
|---|---|
| **Keywords** | TEA1613T, burst mode, adapter, LCD TV, plasma TV, resonant, converter. |
| **Abstract** | This application note discusses the TEA1613T application functions.<br>The TEA1613T provides the drive function for the two discrete power MOSFETs in a resonant half-bridge configuration.<br>The TEA1613T integrates a controller for a half-bridge resonant converter (HBC).<br>The controller for a zero-voltage switching LLC resonant converter includes a high-voltage level-shift circuit and several protection features like over-current protection, open-loop protection, capacitive mode protection and a general purpose latched protection input.<br>In addition to the normal frequency controlled operation mode, it also supports burst mode operation.<br>The proprietary high voltage BCD Powerlogic process makes an efficient, direct start-up possible from the rectified universal mains voltage. A second low voltage SOI IC is used for accurate, high speed protection functions and control.<br>The integrated functionality makes the TEA1613T very suitable for power supplies in LCD-TV, plasma televisions, PC power supplies, high-power office equipment and adapters.<br>A similar product is the TEA1713, which also contains an integrated PFC controller. |

## Revision history

| Rev | Date | Description |
|---|---|---|
| v.1 | 20101228 | first issue |

# 1. Introduction

## 1.1 Scope and setup of this document

This application note discusses the TEA1613T functions for applications in general. The extensive functionality of the TEA1613T leads to a high number of subjects to discuss.

To facilitate the reading of this application note, the setup of this document is made in such a way, that a chapter or paragraph on a selected subject can be read as a stand-alone explanation with a minimum number of cross-references to other document parts or the data sheet. This leads to some repetition of information within the application note and to descriptions or figures that are similar to the ones published in the TEA1613T data sheet. In most cases typical values are given to enhance the readability.



**Please note that all values provided throughout this document are typical values unless otherwise stated.**

## 1.2 Related documents

Additional information and tools can be found in other TEA1613T documents such as:

- Data sheet
- Calculation sheet
- User manual of demo board

# 2. TEA1613T highlights and features

## 2.1 Resonant conversion

Today's market demands high quality, reliable, small, lightweight and efficient power supplies.

In principle, the higher the operating frequency, the smaller and lighter the transformers, filter inductors and capacitors can be. On the other hand, the core, switching and winding losses of the transformer increases at higher frequencies and become dominant. This effect reduces efficiency at high frequencies, which limits the minimum size of the transformer.

The corner frequency of the output filter usually determines the bandwidth of the control loop. A well-chosen corner frequency allows high operating frequencies for achieving a fast dynamic response.

Pulse-Width Modulated (PWM) power converters, such as flyback, up- and down converters, are widely used in low and medium power applications. A disadvantage of these converters is that the PWM rectangular voltage and current waveforms cause turn-on and turn-off losses that limit the operating frequency. The rectangular waveforms also generate broadband electromagnetic energy that can produce ElectroMagnetic Interference (EMI).

A resonant DC-DC converter produces sinusoidal waveforms and reduces the switching losses, which allows it to operate at higher frequencies.

Recent environmental considerations have resulted in a need for high efficiency performance at low loads. Burst-mode operation of the resonant converter can provide this if the converter is to remain active as for adapter applications.

Resonant conversion provides the following benefits:

- High power
- High efficiency
- EMI friendly
- Compact

## 2.2 General features

- Universal mains supply operation
- High level of integration, resulting in a low external component count and a cost effective design
- Enable input
- On-chip high-voltage start-up source
- Stand-alone operation or IC supply from external DC supply

## 2.3 Resonant half-bridge controller features

- Integrated high-voltage level shifter
- Adjustable minimum and maximum frequency
- Maximum 500 kHz half-bridge switching frequency
- Adaptive non-overlap timing
- Burst mode switching

## 2.4 Protection features

- Safe restart mode for system fault conditions
- General latched protection input for output over-voltage protection or external temperature protection
- Protection timer for time-out and restart
- Overtemperature protection
- Soft (re)start
- Under-voltage protection for boost (brownout), IC supply and output voltage
- Over-current regulation and protection
- Input voltage brownout
- Capacitive mode protection for resonant converter

## 2.5 Protection

The TEA1613T provides several protection functions that combine detection with a response to solve the problem. By regulating the frequency as a reaction to, for example, over-power or bad half-bridge switching, the problem can be solved or operation kept safe until it is decided to stop and restart (timer-function).

## 2.6 Typical areas of application

- LCD television
- Plasma television
- High-power adapters
- Slim notebook adapters
- PC power supplies
- Office equipment

# 3. Pin overview with functional description

**Table 1. Pinning overview**

| Pin | Name | Functional description |
|---|---|---|
| 1 | SNSOUT/PFCON | Input for sensing (indirectly) the output voltage of resonant converter. Normally connected to an auxiliary winding of HBC.<br>Also output signal for PFC to hold switching in order to provide synchronous burst mode operation.<br>This pin has 2 functions related to internal comparators:<br>• Overvoltage protection: SNSOUT >3.5 V, latched<br>• Undervoltage protection: SNSOUT <2.3 V, protection timer<br>The pin also contains an internal current source of 100 mA that, initially, generates a voltage up to 1.5 V across an external impedance (>20 kΩ recommended). This voltage level should enable PFC operation (PFCON). After start-up this level is higher, representing the state of the output voltage.<br>During burst mode, an internal switch makes this voltage level low during the time that the HBC is not switching. |
| 2 | SNSFB | Sense input for HBC output regulation feedback by voltage.<br>Sinking a current from SNSFB provides the feedback-voltage on SNSFB. This current through an internal resistor (1.5 kΩ), internally connected to 8.4 V results in the regulation voltage.<br>The regulation voltage range is from 4.1 V to 6.4 V, and corresponds with the maximum and minimum frequency that can be controlled by SNSFB. The SNSFB range is limited to 65 % of the maximum frequency preset by RFMAX.<br>Open loop detection is provided, activating the protection timer when SNSFB is (remains) above 7.7 V. |
| 3 | SNSBURST | Sense input for regulation voltage to enter burst mode.<br>Externally connected to SNSFB by using a resistive divider.<br>When the voltage on SNSBURST drops below $V_{burst(SNSBURST)}$ = 3.5 V, the HBC pauses its operation. When the voltage on SNSBURST increases to above $V_{burst(SNSBURST)}$ + internal hysteresis = 3.6 V it resumes operation without a soft-start sequence. The transition level can be chosen by the values of the resistors used.<br>An internal current source compensates the transition level for variations on boost voltage (supply voltage of the converter) by using the SNSBOOST information. The total impedance of the resistive divider determines the amount of compensation. |
| 4 | SNSBOOST | Sense input for boost voltage.<br>Externally connected to resistor divided boost voltage.<br>As soon as the voltage on this pin drops below $V_{UVP(SNSBOOST)}$ = 1.6 V, switching of the HBC is stopped at the moment the low-side MOSFET is on.<br>An internal hysteresis current source of 3 mA in combination with the resistance of the external divider determines the start level. The boost voltage for starting is higher than the boost voltage for stopping. |

**Table 1. Pinning overview** *…continued*

| Pin | Name | Functional description |
|---|---|---|
| 5 | SUPIC | IC voltage supply input and output of the internal HV start-up source.<br>All internal circuits are directly or indirectly (via SUPREG) supplied from this pin, with the exception of the high-voltage circuit.<br>The buffer capacitor on SUPIC can be charged in several ways:<br>• Internal high-voltage (HV) start-up source<br>• Auxiliary winding from HBC transformer or capacitive supply from switching half-bridge node<br>• External DC supply, for example a standby supply<br>The IC enables operation when the SUPIC voltage has reached the start level of 22 V (for HV start) or 17 V (for external supply). It stops operation below 15 V and a shutdown reset is activated at 7 V. |
| 6 | PGND | Power ground. Reference (ground) for HBC low-side driver. |
| 7 | SUPREG | Output of the internal regulator: 10.9 V.<br>The supply made by this function is used by internal IC functions such as the MOSFET drivers. It can also be used to supply an external circuit. SUPREG can provide a minimum output current of 40 mA.<br>SUPREG becomes operational after SUPIC has reached its start level.<br>The IC starts full operation when SUPREG has reached 10.7 V.<br>UVP: If SUPREG drops below 10.3 V after start, the IC stops operating and the current from SUPIC is limited to 5.4 mA, to allow recovery. |
| 8 | GATELS | Gate driver output for low-side MOSFET of HBC. |
| 9 | n.c. | Not connected, high-voltage spacer. |
| 10 | SUPHV | High-voltage supply input for internal HV start-up source.<br>In a stand-alone power supply application, this pin is connected to the boost voltage. SUPIC and SUPREG are charged with a constant current by the internal start-up source. SUPHV operates at a voltage above 25 V.<br>Initially the charging current is low (1.1 mA). When the SUPIC exceeds the short-circuit protection level of 0.65 V, the generated current increases to 5.1 mA. The source is switched off when SUPIC reaches 22 V which initiates a start operation. During start operation the voltage drops until an auxiliary supply takes over the supply of SUPIC. If the takeover does not take place before SUPIC drops below 15 V, the SUPHV source is reactivated and a restart is made. |
| 11 | GATEHS | Gate driver output for high-side MOSFET of HBC. |
| 12 | SUPHS | High-side driver supply connected to an external bootstrap capacitor between HB and SUPHS. The supply is obtained using an external diode between SUPREG and SUPHS. |
| 13 | HB | Reference for the high-side driver GATEHS.<br>Input for the internal half-bridge slope detection circuit for adaptive non-overlap regulation and capacitive mode protection, externally connected to a half-bridge node between the MOSFETs of HBC. |
| 14 | n.c. | Not connected, high-voltage spacer. |
| 15 | SNSCURHBC | Sense input for the momentary current of the HBC. In case of too high voltage level (that represents the primary current), internal comparators determine to regulate to a higher frequency (SNSCURHBC = ±0.5 V) or protect (SNSCURHBC = ±1 V) by switching immediately to maximum frequency.<br>Variations on protection level, caused by HBC input voltage variations, can be compensated by additional current from SNSCURHBC. This current leads to a voltage offset across the external series resistance which adapts the protection levels. This series resistance is normally provided by the current measurement resistor and an extra series resistance which has a typical value of 1 kΩ. |

**Table 1. Pinning overview** *…continued*

| Pin | Name | Functional description |
|---|---|---|
| 16 | SGND | Signal ground, reference for IC. |
| 17 | CFMIN | Oscillator pin.<br>The value of the external capacitor determines the minimum switching frequency of the HBC. In combination with the resistor value on RFMAX, it sets the operating frequency range.<br>To facilitate switching timing, a triangular waveform is generated on the CFMIN capacitor $V_{low(CFMIN)}$ = 1 V and $V_{high(CFMIN)}$ = 3 V). The minimum frequency is determined by a fixed minimum (dis)charging current of 150 μA. During special conditions, the (dis)charging current is reduced to 30 μA to temporarily slow down the charging.<br>An internal function limits the operating frequency to 670 kHz. |
| 18 | RFMAX | Oscillator frequency pin.<br>The value of the resistor connected between this pin and ground, determines the frequency range. Both the minimum and maximum frequencies of the HBC are preset. The minimum frequency is set by CFMIN and the absolute maximum frequency is internally limited to 670 kHz.<br>The voltage on RFMAX and the value of the resistor connected to it, determine the variable part (in addition to the fixed 150 μA) of the (dis)charging current of the CFMIN-capacitor. The voltage on RFMAX can vary between 0 V (minimum frequency) and 2.5 V (maximum frequency).<br>The RFMAX voltage (running frequency) is driven by SNSFB- and SSHBC/EN- function.<br>The protection timer is started when the voltage level is above 1.83 V. An error is assumed when the HBC is operating at high frequency for a longer time. |
| 19 | SSHBC/EN | Combined soft-start/protection frequency control of HBC and IC enable input (PFC or PFC + HBC). Externally connected to a soft-start capacitor and an enable pull-down function.<br>This pin has 3 functions:<br>• Enable IC (>2.2 V)<br>• Frequency sweep during soft-start from 3.2 V to 8 V<br>• Frequency control during protections between 8 V to 3.2 V<br>Seven internal current sources operate the frequency control, depending on which of the following actions is required:<br>• Soft-start + overcurrent protection: high/low charge (160 μA/40 μA) + high/low discharge (160 μA/40 μA)<br>• Capacitive mode regulation: high/low discharge (1800 μA/440 μA)<br>• General: bias discharge (5 μA) |
| 20 | RCPROT | Timer presetting for time-out and restart.The timing is determined by the values of an externally connected resistor and capacitor.<br>Protection timer.<br>During the protections listed below, the timer is activated by a 100 μA charge current:<br>• OverCurrent Regulation OCR (SNSCURHBC)<br>• High Frequency Protection HFP (RFMAX)<br>• Open Loop Protection OLP (SNSFB)<br>• Undervoltage Protection UVP (SNSOUT)<br>When the level of 4 V is reached the protection is activated. The resistor discharges the capacitor and at a level of 0.5 V, a restart is made.<br>Restart timer. |

## 4. Application diagram

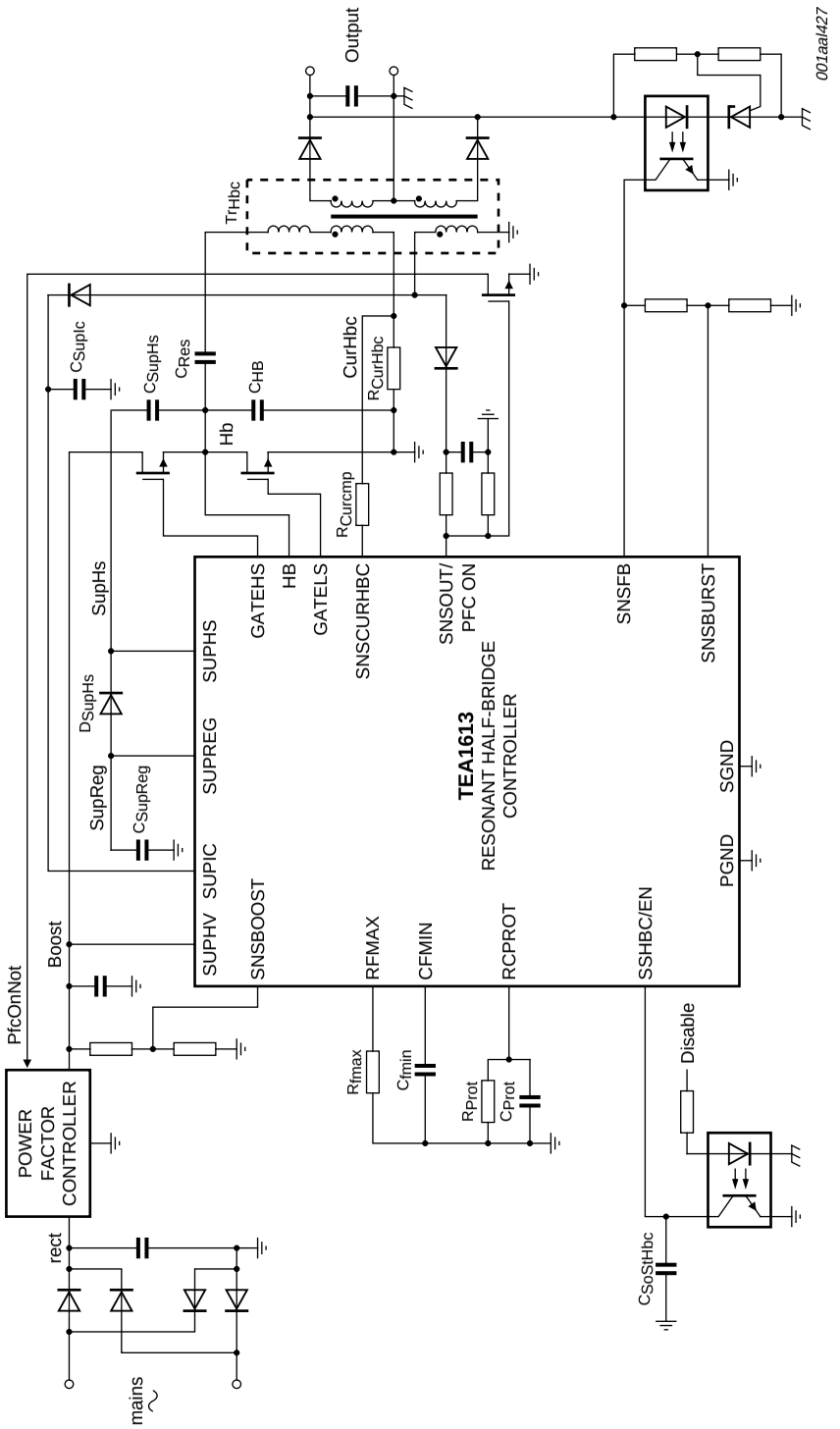


Fig 1. Basic application diagram TEA1613T

## 5. Block diagram

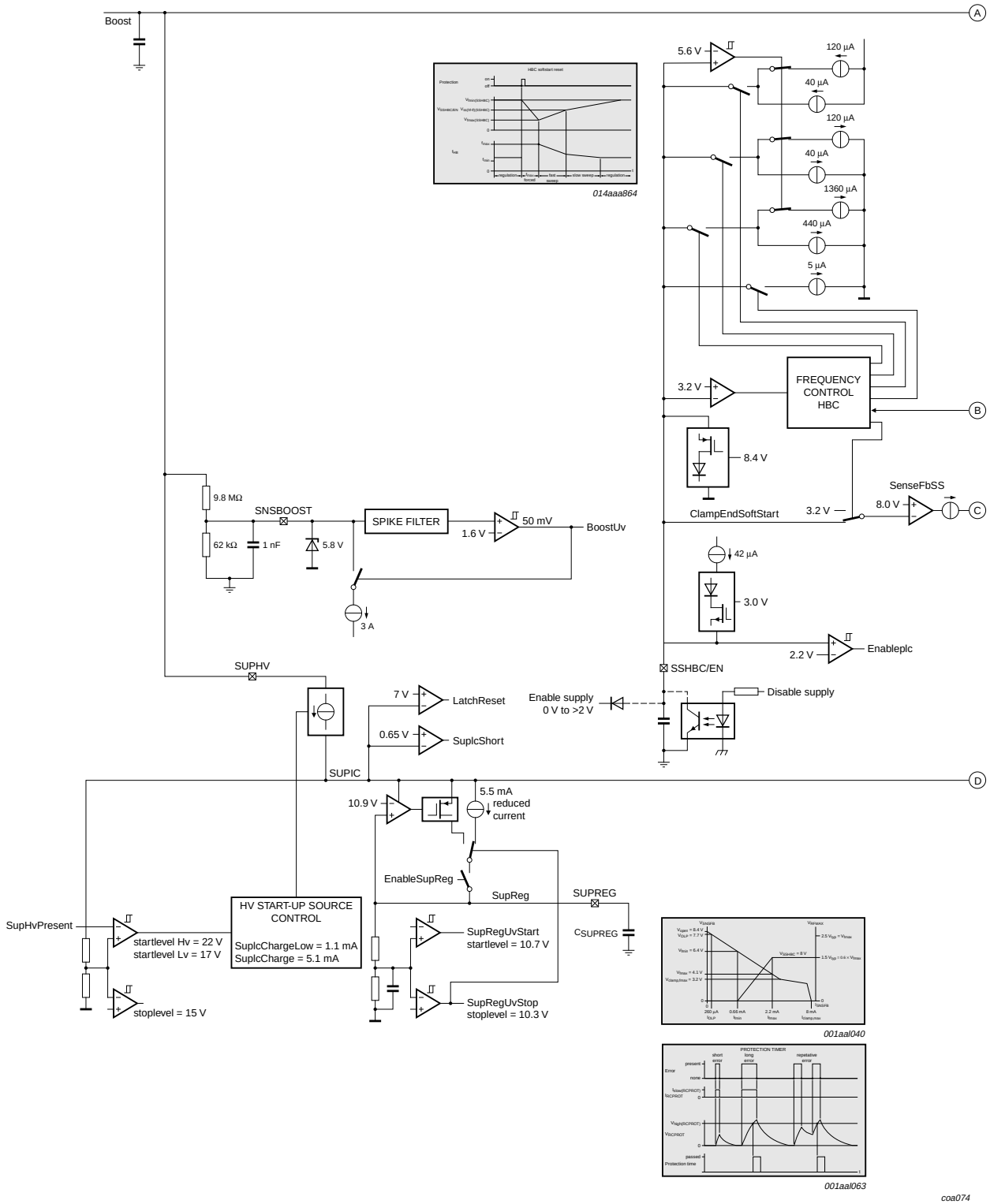


**Fig 2. TEA1613T with application block diagram (part 1)**

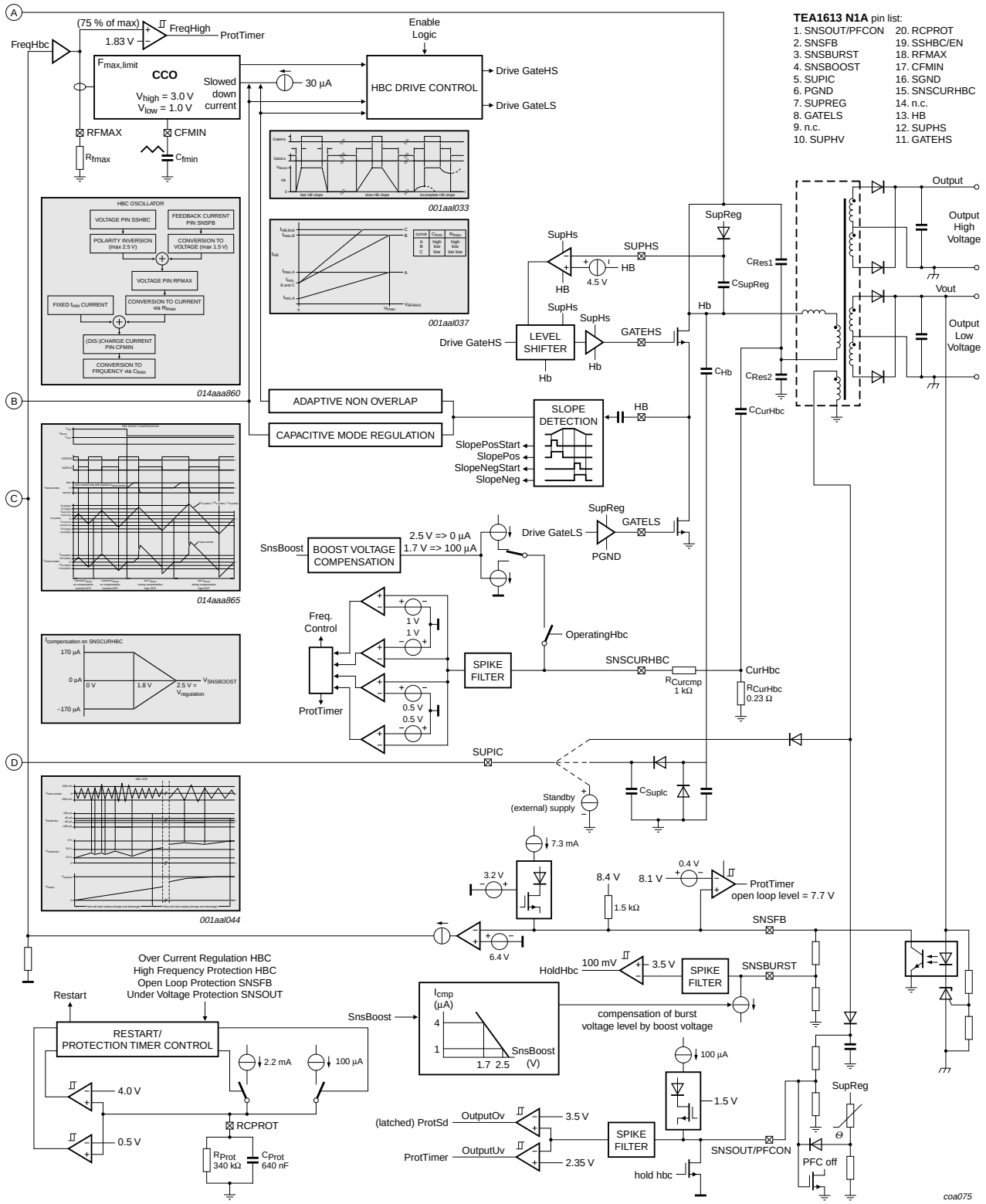


**Fig 3. TEA1613T with application block diagram (part 2)**

# 6. Supply functions

## 6.1 Basic supply system overview

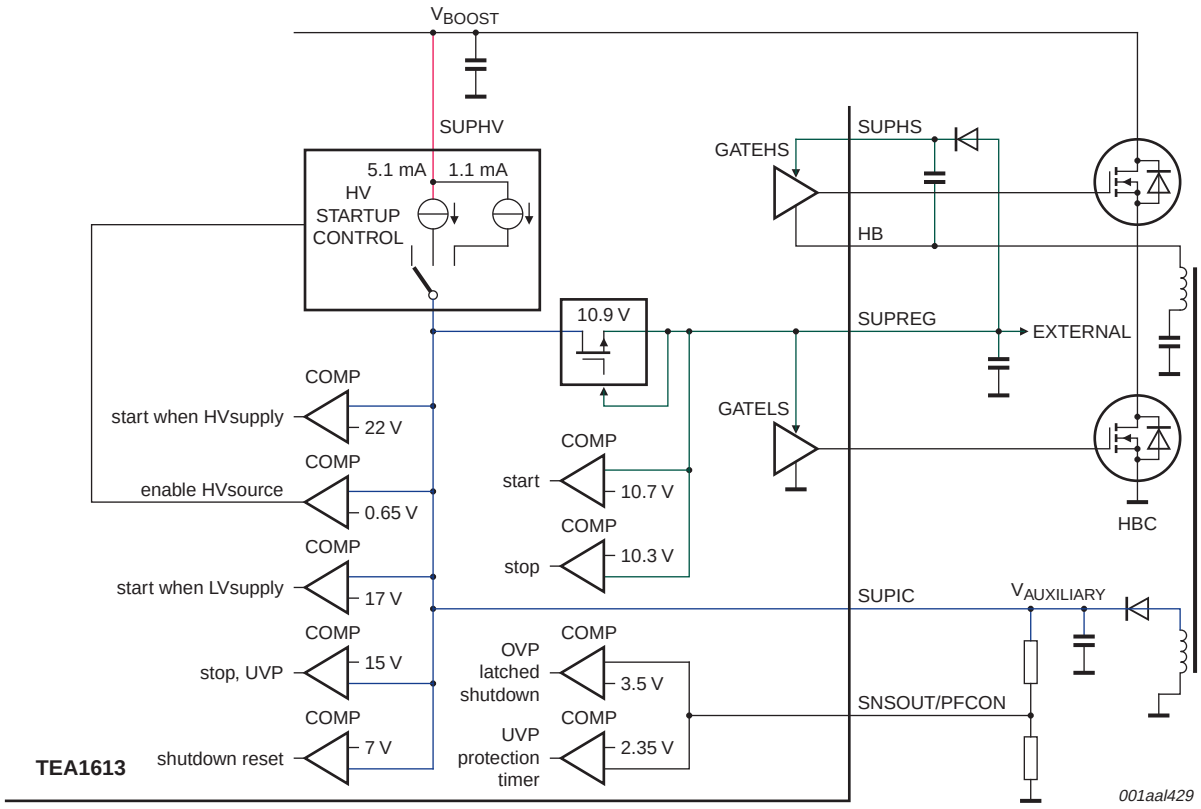


**Fig 4. Basic overview internal IC supplies**

### 6.1.1 TEA1613T supplies

The main supply for the TEA1613T is SUPIC.

SUPHV can be used to charge SUPIC for starting the supply. During operation a supply voltage is applied to SUPIC and the SUPHV source is switched off. The SUPHV source is only switched on again at a new start-up.

The internal regulator SUPREG generates a fixed voltage of 10.9 V to supply the internal MOSFET drivers GATELS and GATEHS. To supply GATEHS a bootstrap function with an external diode is used to make supply SUPHS.

SUPIC and SUPREG also supply other internal TEA1613T circuits.

### 6.1.2 Supply monitoring and protection

The supply voltages are internally monitored for deciding when to initiate certain actions i.e. starting, stopping or protection.

In several applications the SUPIC voltage can also be used to monitor the HBC output voltage by protection input SNSOUT/PFCON.

## 6.2 SUPIC - the low voltage IC supply

SUPIC is the main IC supply. With the exception of the SUPHV circuit, all internal circuits are either directly or indirectly supplied from this pin.

### 6.2.1 SUPIC start-up

SUPIC needs to be connected to an external buffer capacitor. This buffer capacitor can be charged in several ways:

- Internal high-voltage (HV) start-up source
- Auxiliary supply (e.g. from a winding on the HBC transformer)
- External DC supply (e.g. from a standby supply)

The IC starts operating when the SUPIC and SUPREG voltages have reached the start level. The start level value of SUPIC depends on the condition of the SUPHV pin.

SUPHV $\geq 25\ V_{max}$

This is the case in a stand-alone application where SUPIC is initially charged by the HV start-up source. The SUPIC start level is 22 V. The large difference between start level and stop level (15 V) is used to allow discharge of the SUPIC capacitor until the auxiliary supply can take over the IC supply.

SUPHV not connected/used

This is the case when the TEA1613T is supplied from an external DC supply. The SUPIC start level is now 17 V. During start-up and operation the IC is continuously supplied by the external DC supply. For this kind of application the SUPHV pin should be left open.

### 6.2.2 SUPIC stop, UVP and short-circuit protection

The IC stops operating when the SUPIC voltage drops below 15 V which is the Under-Voltage Protection (UVP) of SUPIC. While in the process of stopping, the HBC continues until the low-side MOSFET is active before stopping the HBC operation. SUPIC has a low level detection at 0.65 V to detect a short circuit to ground. This level also controls the current source from the SUPHV pin.

### 6.2.3 SUPIC current consumption

The SUPIC current consumption depends on the state of the TEA1613T.

- **Disabled IC state:** when the IC is disabled via the SSHBC/EN pin, the current consumption is low at 250 μA.
- **SUPIC charge, SUPREG charge, thermal hold, restart and shutdown state:** During the charging of SUPIC and SUPREG before start-up, during a restart sequence or during shutdown after activation of protection, only a small part of the IC is active. The HBC operation is disabled. The current consumption from SUPIC in these states is small: 400 μA.
- **Operating supply state:** When the HBC is operational and switching, the current consumption is larger. The MOSFET drivers are dominant in the current consumption, especially during a soft-start of the HBC, when the switching frequency is high, but also during normal operation (see Section 6.5.5). Initially the SUPIC current is delivered by the stored energy in the SUPIC capacitor. During normal operation, this is eventually taken over by the supply source on SUPIC.

## 6.3 SUPIC supply using HBC transformer auxiliary winding

### 6.3.1 Start-up by SUPHV

In a stand-alone power supply application, the IC can be started by a high voltage source such as the rectified mains voltage. For this purpose the high voltage input SUPHV can be connected to the boost voltage (for example a PFC output voltage).

The SUPIC and SUPREG are charged by the internal HV start-up source which delivers a constant current from SUPHV to SUPIC. SUPHV is operational at a voltage > 25 V.

As long as the voltage at SUPIC is below the short circuit protection level (0.65 V), the current from SUPHV is low (1.1 mA). This is to limit the dissipation in the HV start-up source when SUPIC is shorted to ground.

During normal conditions, SUPIC quickly exceeds the protection level and the HV start-up source switches to normal current (5.1 mA). The HV start-up source switches off when SUPIC has reached the start level (22 V). The current consumption from SUPHV is low (7 μA) when switched off.

When SUPIC has reached the start level (22 V), SUPREG is charged. When SUPREG reaches the level of 10.7 V, it enables operation of HBC.

The auxiliary winding supply of the HBC transformer must take over the supply of SUPIC before it is discharged to the SUPIC undervoltage stop level (15 V).

### 6.3.2 Block diagram for SUPIC start-up

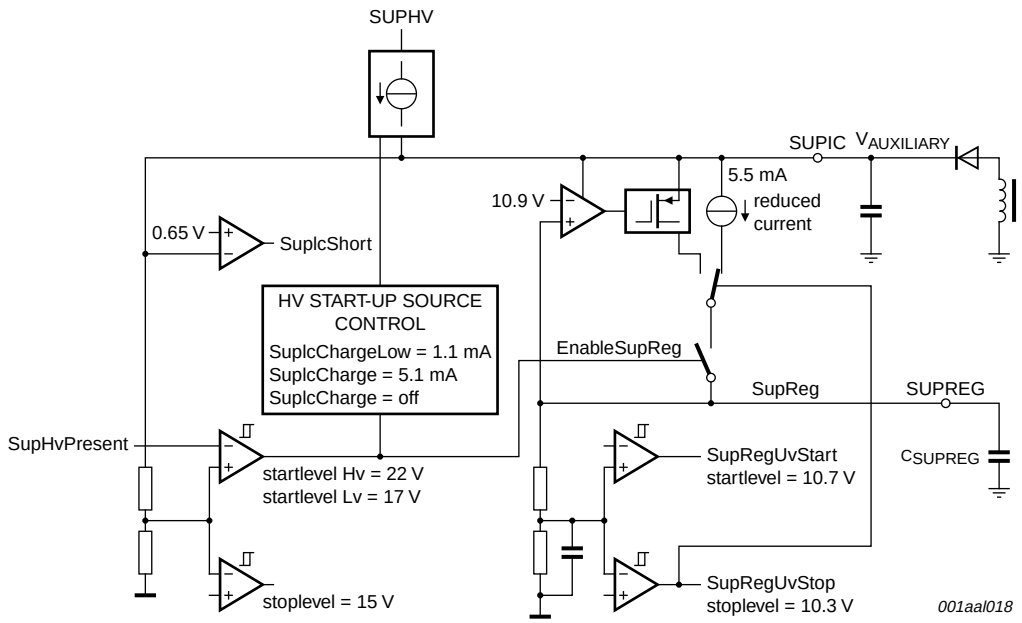


**Fig 5. Block diagram: SUPIC and SUPREG start-up with SUPHV and auxiliary supply**

### 6.3.3 Auxiliary winding on the HBC transformer

To obtain a supply voltage for SUPIC during operation, an auxiliary winding on the HBC transformer can be used. As SUPIC has a wide operational voltage range (15 V to 38 V), this is not a critical parameter.

Also note:

- For low power consumption, the voltage on SUPIC should be low.
- To use the voltage from the auxiliary winding for both the IC supply and the HBC output voltage measurement (by SNSOUT/PFCON). The auxiliary supply must be made accurately to represent the output voltage. To ensure good coupling, this winding needs to be placed on the secondary (output) side.
- When mains insulation is included in the HBC transformer, it can impact the construction of the auxiliary winding. Triple insulated wire is needed when the auxiliary winding is placed on the mains-insulated area of the transformer construction.

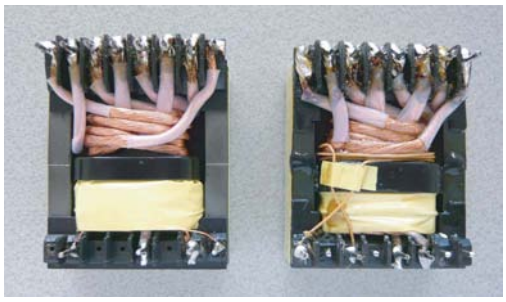

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**Fig 6. Auxiliary winding on primary side (left) and secondary side (right)**

#### 6.3.3.1 SUPIC and SNSOUT/PFCON by auxiliary winding

The SNSOUT/PFCON input provides a combination of 3 functions:

- Overvoltage protection: SNSOUT/PFCON > 3.5 V, latched
- Undervoltage protection: SNSOUT/PFCON < 2.35 V, protection timer
- During burst mode an internal switch makes this voltage level low during the time that the HBC is not switching. This signal can be used to make a PFC burst synchronously.

**Remark:** A more detailed discussion of the SNSOUT/PFCON functions can be found in Section 9.1 “Burst mode implementation”, Section 10.3.1 “OverVoltage Protection (OVP) output” and Section 10.3.2 “UnderVoltage Protection (UVP) output”.

Often, a circuit is used which combines SUPIC and the output voltage monitoring by SNSOUT/PFCON, with one auxiliary winding on the HBC transformer. But an independent construction for SUPIC and SNSOUT is also possible; for example when SUPIC is supplied by a separate standby supply and an auxiliary winding is only used for output voltage sensing. It is also possible not to use SNSOUT for output sensing. SNSOUT can be used as a general purpose protection input. For more details on the possibilities, refer to Section 10.3.3 “OVP and UVP combinations”.

In case of a combined function of SUPIC and SNSOUT/PFCON by an auxiliary winding on the HBC transformer, some issues need to be addressed to obtain a good representation of the output voltage for SNSOUT/PFCON measurement.

The advantage of a good coupling/representation of the auxiliary winding with the output windings is that a stable auxiliary voltage is also obtained for SUPIC. A low SUPIC voltage value can be designed more easily for lowest power consumption.

#### 6.3.3.2 Auxiliary supply voltage variations by output current

At high (peak) current loads, the voltage drop across the series components of the HBC output stage (resistance and diodes) is compensated by regulation. This results in a higher voltage on the windings at higher output currents due to the higher currents causing a larger voltage drop across the series components. An auxiliary winding supply shows this variation caused by the HBC output.

#### 6.3.3.3 Voltage variations by auxiliary winding position: primary side component

Due to a less optimal position of the auxiliary winding, the voltage for SNSOUT/PFCON and/or SUPIC can contain a certain amount of undesired primary voltage component. This can seriously endanger the feasibility of the SNSOUT/PFCON sensing function.

To avoid a primary voltage component on the auxiliary voltage, the coupling of the auxiliary winding with the primary winding should be as small as possible. To obtain this, the auxiliary winding should be placed on the secondary winding(s) and as physically remote as possible from the primary winding. See the differences in the results provided by the comparison on a secondary side position in Figure 7.

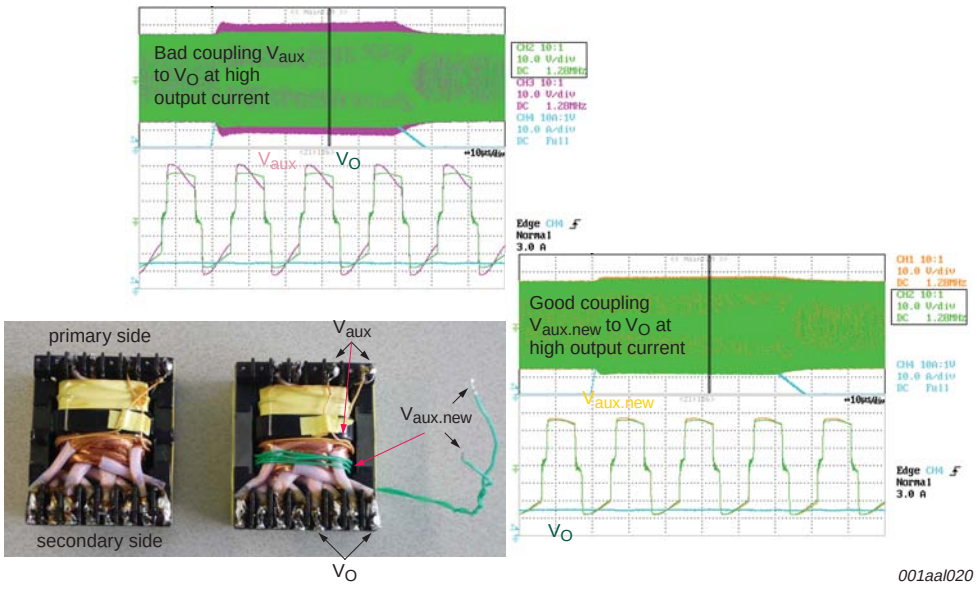



**Fig 7. Position the auxiliary winding for good output coupling**

### 6.3.4 Difference between UVP on SNSOUT/PFCON and SNSCURHBC OCP/OCR

In a system that uses output voltage sensing by means of the SNSOUT/PFCON function, there can be an overlap in functionality in an over-power or short circuit situation. In such a situation, often both the SNSOUT/PFCON UnderVoltage Protection (UVP) and the OverCurrent Protection/Regulation on SNSCURHBC, activates the protection timer.

There are basic differences between both functions:

- OCP/OCR monitors the power in the system by sensing the primary current in detail
- SNSOUT/PFCON monitors (indirectly) the HBC output voltage or another external protection circuit (e.g. NTC temperature measurement)

SNSOUT/PFCON is a more general protection input while SNSCURHBC is specifically designed for HBC operation.

In addition, SNSOUT/PFCON also offers two other functions: OVP (latched) and an output signal for PFC bursting.

## 6.4 SUPIC supply by external voltage

### 6.4.1 Start-up

When the TEA1613T is supplied by an external DC supply, the SUPHV pin can be left unconnected. The SUPIC start level is now 17 V.

When the SUPIC exceeds 17 V, the internal regulator is activated and charges SUPREG.

At SUPREG ³ 10.7 V, GATELS is switched on for the bootstrap function to charge SUPHS. The TEA1613T starts the converter as soon as $V_{BOOST}$ reaches a preset level (SNSBOOST ³ 1.6 V).

### 6.4.2 Stop

Operation of the TEA1613T can be stopped by switching off the external source for SUPIC. As soon as the voltage level on SUPIC drops below 15 V, operation is stopped.

In case of shutdown (because of protection), this state is reset by internal logic as soon as the SUPIC voltage drops below 7 V.

## 6.5 SUPREG

SUPIC has a large voltage range for easy application. But because of this, SUPIC can not directly be used to supply the internal MOSFET drivers as they would exceed the allowed gate voltage of many external MOSFETs.

To avoid this issue (and create a few other benefits), the TEA1613T contains an integrated series stabilizer. The series stabilizer generates an accurate regulated voltage on SUPREG on the external buffer capacitor.

This stabilized SUPREG voltage is used for:

- Supply of internal low-side HBC driver
- Supply of internal high-side driver via external components
- Reference voltage or supply of external circuits

The series stabilizer for SUPREG is enabled after SUPIC has been charged. In this way optional external circuitry at SUPREG does not draw from the start-up current during the charging of SUPIC. The capacitor on SUPIC acts as a buffer at charge of SUPREG and start-up of the IC.

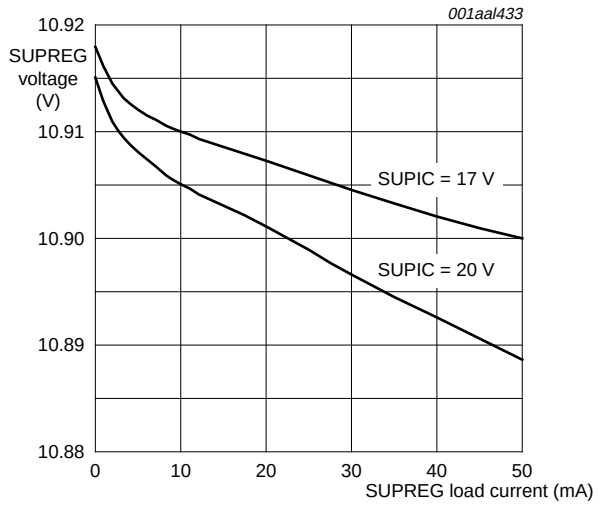
To ensure that the external MOSFETs receive sufficient gate drive, the SUPREG voltage must first reach the $V_{start(SUPREG)}$ level before the IC starts operating, provided that the SUPIC voltage has also reached the start level.

The SUPREG has an Under-Voltage Protection. When the SUPREG voltage drops below the 10.3 V two actions occur:

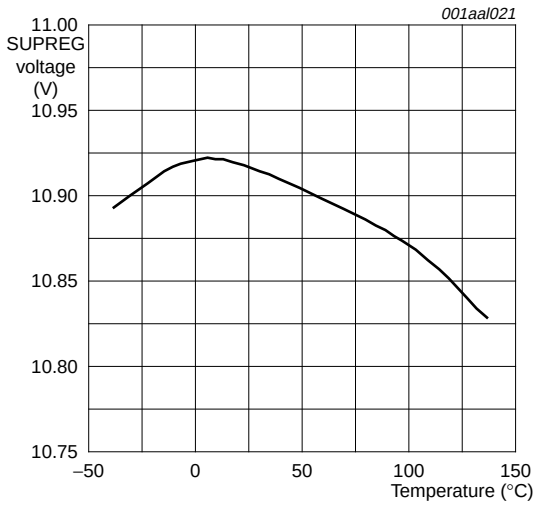
- The IC stops operating to prevent unreliable switching due to a too low gate driver voltage. The HBC continues until the low-side stroke is active.
- The maximum current from the internal SUPREG series stabilizer is reduced to 5.4 mA. In case of an overload at SUPREG in combination with an external DC supply for SUPIC, this action reduces the dissipation in the series stabilizer.

It is important to realize that in principle, SUPREG can only source current.

The GATELS driver (and indirectly the GATEHS driver) is supplied by this voltage and takes current from it during operation depending on the operating conditions. Some change in value can be expected due to current load and temperature.




Voltage characteristics for load




Voltage characteristics for temperature

**Fig 8. Typical SUPREG voltage characteristics for load and temperature**

### 6.5.1 Block diagram of SUPREG regulator

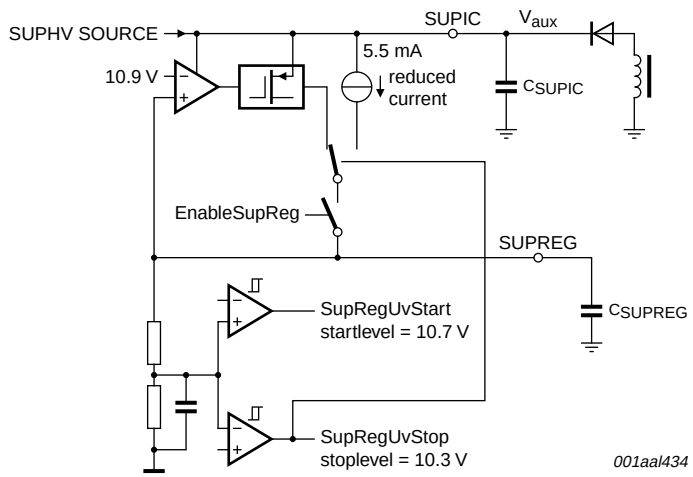



**Fig 9. Block diagram of internal SUPREG regulator**

### 6.5.2 SUPREG during start-up

SUPREG is supplied by SUPIC. SUPIC is the unregulated external power source that is the input voltage for the internal voltage regulator that provides SUPREG.

At start-up SUPIC needs to reach a specific voltage level before SUPREG is activated:

- When start-up is by the internal HV supply, SUPREG is activated when SUPIC ≥ 22 V.
- When start-up is by an external (low voltage) supply, SUPREG is activated when SUPIC ≥ 17 V.

### 6.5.3 Supply voltage for the output drivers: SUPREG

The TEA1613T has a powerful output stage for GATELS and GATEHS to drive large MOSFETs. These internal drivers are supplied by SUPREG which provides a fixed voltage.

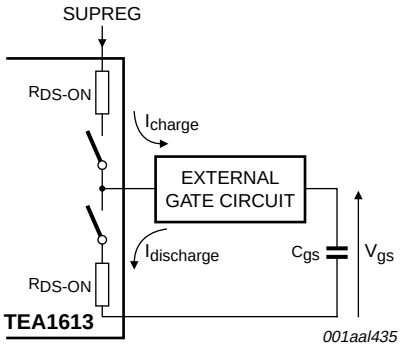



**Fig 10. Simplified model of MOSFET drive**

It can be seen from the simplified model that current is taken from SUPREG when the external MOSFET is switched on by charging the gate to a high voltage.

The shape of the current from SUPREG at switch on is related to:

- the supply voltage for the internal driver (10.9 V)
- the characteristic of the internal driver
- the gate capacitance to be charged
- the gate threshold voltage for the MOSFET to switch on
- the external circuit to the gate

The charging of SUPHS for GATEHS is synchronized in time with GATELS but has a different shape because of the bootstrap function.

### 6.5.4 Supply voltage for the output drivers: SUPHS

The high-side driver is supplied by an external bootstrap buffer capacitor. The bootstrap capacitor is connected between the high-side reference pin HB and the high-side driver supply input pin SUPHS. This capacitor is charged by an external diode from SUPREG during the time that HB is low. With the use of a suitable external diode, the voltage drop between SUPREG and SUPHS can be minimized. This is especially important when using a MOSFET that needs a large amount of gate charge and/or when switching at high frequencies.

Instead of using SUPREG as the power source for charging SUPHS, another supply source can be used. In such a construction it is important to check for correct start/stop sequences and to prevent the voltage exceeding the maximum value of HB +14 V.

Note that for each cycle, the current taken from SUPREG to charge SUPHS differs (in time and shape) from the current taken by GATELS.

#### 6.5.4.1 Initial charging of SUPHS

At start-up, SUPHS is charged by the bootstrap function by setting GATELS HIGH to switch on the low-side MOSFET, keeping the HB node at low voltage. The PFC operation is started while SUPHS is being charged. The time between start charging and start HBC operation is normally sufficient to charge SUPHS completely.

#### 6.5.4.2 Current load on SUPHS

The current taken from SUPHS consists of two parts:

- Internal MOSFET driver GATEHS
- Internal circuit to control GATEHS (37 μA)

It can be seen from Figure 11 that the current taken by the driver GATEHS occurs at switch on. The shape of the current from SUPHS at switch on is related to:

- the value of the supply voltage for the internal driver
- the characteristic of the internal driver
- the gate capacitance to be charged
- the gate threshold voltage for the MOSFET to switch on
- the external circuit to the gate

The voltage value of SUPHS can vary.

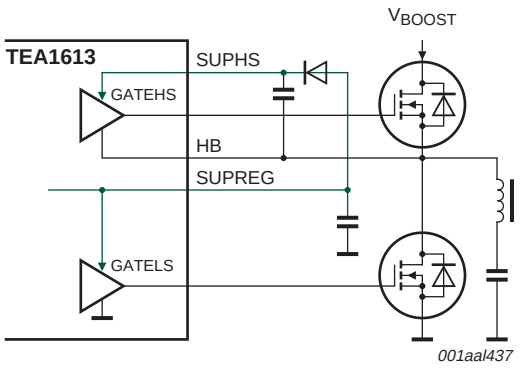



**Fig 11. Typical application of SUPHS**

#### 6.5.4.3 Lower voltage on SUPHS

During normal operation, each time the half-bridge node (HB) is switched to ground level, the SUPHS capacitor is charged by the bootstrap function. Because of the voltage drop across the bootstrap diode, the value of SUPHS is normally lower than SUPREG (or other bootstrap supply input).

The voltage drop across the bootstrap diode is directly related to the amount of current that is needed to charge SUPHS. The resultant SUPHS voltage is also influenced by the time available for charging.

A large voltage drop occurs when an external MOSFET with a large gate capacitance has to be switched at high frequency (high current + short time).

Also, during burst mode operation, a low voltage on SUPHS can occur. In burst mode there are (long) periods of not switching, and therefore no charging of SUPHS. During this time the circuit supplied by SUPHS slowly discharges the supply voltage capacitor. At the moment a new burst starts, the SUPHS voltage is lower than during normal operation. During the first switching cycles the SUPHS is recharged to its normal level. During burst mode, at low output power, the switching frequency is normally rather high which limits a fast recovery of the SUPHS voltage.

Although in most applications the voltage drop is limited, it is an important issue to be evaluated. It can influence the selection of the best diode type for the bootstrap function and the value of the buffer capacitor on SUPHS.

### 6.5.5 SUPREG power consumed by MOSFET drivers

During operation the drivers GATELS and GATEHS charging the gate capacitances of the external MOSFETs consume a major part of the power from SUPREG. The amount of energy needed for this in time, is linear to the switching frequency. Often, for the MOSFETs used, the total charge is specified for certain conditions. With this value an estimation can be made for the amount of current needed from SUPREG.

GATELS and GATEHS (driving two MOSFETs in total):

$\Delta I_{SUPIC} = 2 \times Q_{gate} \times f_{bridge}$

For example, a MOSFET with $Q_{gate}$ = 40 nC at a bridge frequency 100 kHz:

$\Delta I_{SUPIC} = 2 \times 40\ nC \times 100\ kHz = 8\ mA$

**Remark:** Note that the calculated value is generally higher than the value found in practice, because the switching operation deviates from the MOSFET specification for $Q_{gate}$.

### 6.5.6 SUPREG supply voltage for other circuits

The regulated voltage of SUPREG can also be used as a regulated supply for external circuits. The load of the external circuits has an effect on the start-up (time) and the total load (IC + external circuit) of SUPREG during operation.

**Current available for supplying an external circuit from SUPREG.**

The total current available from SUPREG is 40 mA. To determine how much current is available for an external circuit, it must be known how much is being used by the IC.

$I_{SUPREG\_for\_external} = 40\ mA - I_{SUPREG\_for\_IC}$

With respect to the IC, by far the most amount of current from SUPREG is consumed by the MOSFET drivers (GATELS and GATEHS). Other circuit parts in the IC, consume a maximum of 4 mA.

$I_{SUPREG\_for\_IC} = I_{SUPREG\_for\_MOSFET\text{-}drivers} + I_{SUPREG\_for\_other\_IC\text{-}circuits}$

$I_{SUPREG\_for\_IC} = I_{SUPREG\_for\_MOSFET\text{-}drivers} + 4\ mA_{max}$

$I_{SUPREG\_for\_MOSFET\text{-}drivers}$ can be estimated by the method provided in Section 6.5.5.

**An estimation by measurement**

The current used by SUPIC, while supplying the circuit from an external power supply, can be assumed as a first approximation of how much current the IC circuits take from SUPREG. Using this value, an estimation can be made of the power available for external circuits.

Be aware that the highest power consumption value is reached when the MOSFET drivers are switching at the highest frequency.

**Example:**

$I_{SUPIC(maximum\ measured)} = 14\ mA$

$I_{SUPREG(for\ IC\ circuits)} \approx I_{SUPIC(maximum\ measured)} = 14\ mA$

$I_{SUPREG(for\ externals)} = 40\ mA - I_{SUPREG(for\ IC\ circuits)} = 40\ mA - 14\ mA = 26\ mA$

**Remark:** Note that to maintain full functionality, SUPREG must remain above the undervoltage protection level (10.3 V). High external current loads can lead to problems during start-up.

## 6.6 Value of the capacitors on SUPIC, SUPREG and SUPHS

Some practical examples are provided in Section 12.

### 6.6.1 Value of the capacitor on SUPIC

#### 6.6.1.1 General

It is generally advisable to use two types of capacitor on SUPIC. An SMD ceramic type, with a smaller value located close to the IC, and an electrolytic type providing the major part of the capacitance.

#### 6.6.1.2 Start-up

When the supply is initially provided by an HV source before being handled by an auxiliary winding, a larger capacitor is needed on SUPIC. The capacitor value should be large enough to handle the start-up before the auxiliary winding takes over the supply of SUPIC.

**Example:**

This example provides an estimation and not an exact calculation.

$I_{SUPIC(start\text{-}up)}$ = 10 mA

$\Delta V_{SUPIC(start\text{-}up)}$ = 22 V − 15 V = 7 V

$\Delta t_{Vaux>15V}$ = 70 ms

$$C_{SUPIC} > I_{SUPIC(start\text{-}up)} \times \frac{\Delta t_{Vaux} > 15\ V}{\Delta V_{SUPIC(start\text{-}up)}} = 10\ mA \times \frac{70\ ms}{7\ V} = 100\ \mu F \quad (1)$$

#### 6.6.1.3 Normal operation

For normal operation, the main purpose of the capacitors on SUPIC is to keep the current load variations (e.g. gate drive currents) local.

#### 6.6.1.4 Burst mode operation

When burst mode operation is applied, the supply construction often uses an auxiliary winding and start-up from the HV source. While in the burst mode there are long periods during which the auxiliary winding is not able to charge the SUPIC because there is no HBC switching (time between two bursts). Therefore, the capacitor value on SUPIC should be large enough to keep the voltage above 15 V to prevent activating the SUPIC under-voltage stop level.

**Example:**

This example provides an estimation and not an exact calculation.

$I_{SUPIC(between\ 2\ bursts)}$ = 4 mA

$\Delta V_{SUPIC(burst)} = V_{aux\ burst} - 15\ V = 19\ V - 15\ V = 4\ V$

$\Delta t$ between 2 bursts = 25 ms

$$C_{SUPIC} > I_{SUPIC(between\ 2\ bursts)} \times \frac{\Delta t_{between\ 2\ bursts}}{\Delta V_{SUPIC(burst)}} = 4\ mA \times \frac{25\ ms}{4\ V} = 25\ \mu F \quad (2)$$

### 6.6.2 Value of the capacitor on SUPREG

To support charging of SUPREG during an HV source start, the capacitor on SUPREG should not be larger than the capacitor on SUPIC. This is to prevent a severe voltage drop on SUPIC due to the charge of SUPREG. If SUPIC is supplied by an external (standby) source, this is not important.

SUPREG is the supply for the current of the gate drivers. Keeping current peaks local can be achieved using an SMD ceramic capacitor which is supported by an electrolytic capacitor. This is necessary to provide sufficient capacitance to prevent voltage drop during high current loads. The value of the capacitor on SUPREG should be much larger than the total capacitance of the MOSFETs that need to be driven (including the load and capacitor on SUPHS that is in parallel with the bootstrap construction), to prevent significant voltage drop.

When considering the internal voltage regulator, the value of the capacitance on SUPREG should be $\geq 1\ \mu F$ to ensure basic regulation properties. Often a much larger value is used for the reasons mentioned previously.

### 6.6.3 Value of the capacitor for SUPHS

To support charging the gate of the high side MOSFET, the SUPHS capacitor should be much larger than the gate capacitance. This prevents a significant voltage drop on SUPHS by the gate charge. When burst mode is applied, SUPHS is discharged by 37 μA during the time between two bursts by the quiescent current of the internal circuit.

### 6.6.4 Relationship between the capacitors on SUPIC, SUPREG and SUPHS

It can be generally stated that:

- $C_{SUPIC} > C_{SUPREG} > C_{SUPHS}$
- In a system that uses burst mode operation, the capacitor values need to be larger than in a system without burst mode operation

# 7. MOSFET drivers GATELS and GATEHS

The TEA1613T provides 2 outputs for driving external high voltage power MOSFETs:

- GATELS for driving the low side of the HBC MOSFET
- GATEHS for driving the high side of the HBC MOSFET

## 7.1 GATELS and GATEHS

Both drivers have identical driving capabilities for the gate of an external high-voltage power MOSFET. The low-side driver is referenced to pin PGND and is supplied from SUPREG. The high-side driver is floating, referenced to HB, the connection to the midpoint of the external half-bridge. The high-side driver is supplied by a capacitor on SUPHS that is supplied by an external bootstrap function by SUPREG. The capacitor on SUPHS is charged by the bootstrap diode when the low-side MOSFET is on.

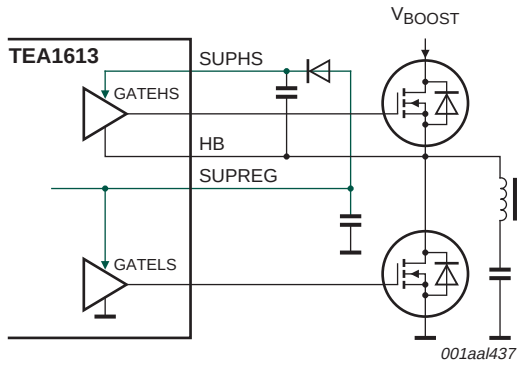



**Fig 12. GATELS and GATEHS drivers**

Both MOSFET drivers have a strong current source capability and an extra strong current sink capability. In general, operation of the HBC it is not critical to be able to quickly switch on the external MOSFET, as the HB node automatically swings to the correct state after switch off. Fast switch off however, is important to limit switching losses and prevent delays especially at high frequency.

## 7.2 Supply voltage and power consumption

For a description of the supply voltages and power consumption by the MOSFET drivers see Section 6.5.3 and Section 6.5.5.

## 7.3 General details regarding MOSFET drivers

### Switch on

The time to switch on is dependent upon:

- the supply voltage for the internal driver
- the characteristics of the internal driver
- the gate capacitance to be charged
- the gate threshold voltage for the MOSFET to switch on
- the external circuit to the gate

### Switch off

The time to switch off is dependent upon:

- the characteristic of the internal driver
- the gate capacitance to be discharged
- the voltage on the gate just before discharge
- the gate threshold voltage for the MOSFET to switch off
- the external circuit to the gate

Because the timing for switching off the MOSFET is more critical than switching it on, the internal driver can sink more current than it can source. At higher frequencies and/or short on-time, timing becomes more critical for correct switching. Sometimes a compromise must be made between fast switching and EMI effects. A gate circuit between the driver output and the gate can be used to optimize the switching behavior.

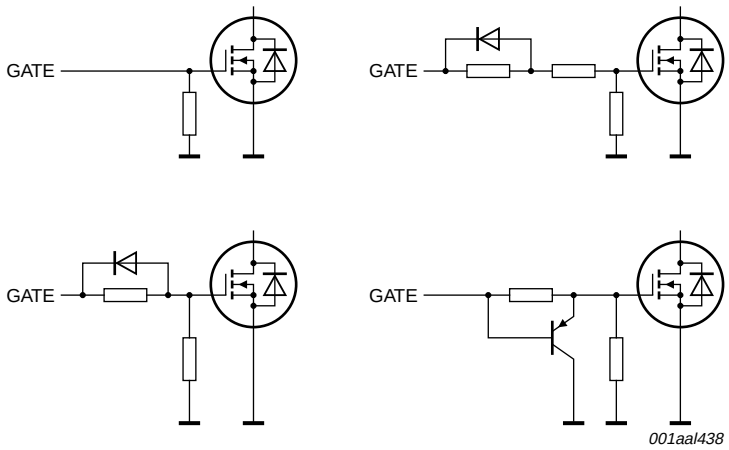



**Fig 13. Examples of gate circuits**

Switching the MOSFETs on and off by the drivers can be approximated by alternating charge and discharge of a (gate-source) capacitance of the MOSFET through a resistor (RDS-ON of the internal driver MOSFET).

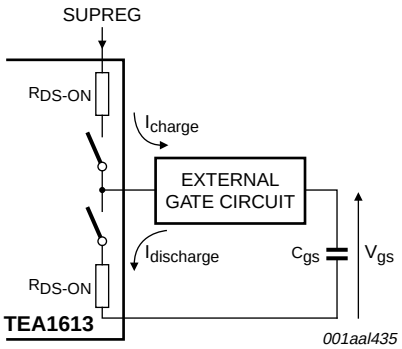



**Fig 14. Simplified model of a MOSFET drive**

## 7.4 Specifications

The main function of the internal MOSFET drivers is to source current and sink current to switch the external MOSFET switch on and off.

The amount of sink and source current required is specified to show the capability of the internal driver.

The simplified model in Figure 14 demonstrates that the values of the charge current and discharge current are strongly dependant upon the conditions of the supply voltage and gate voltage. The value of the source current is highest when the supply voltage is highest and the gate voltage 0 V. The value of the sink current is highest when the gate voltage is highest.

**Table 2. TEA1613T driver specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HBC high-side and low-side driver (pins GATEHS and GATELS)** | | | | | | |
| $I_{source(drv)}$ | driver source current | high-side; $V_{GATEHS} - V_{HB} = 4$ V | - | –310 | - | mA |
| | | low-side; $V_{GATELS} - V_{PGND} = 4$ V | - | –310 | - | mA |
| $I_{sink(drv)}$ | driver sink current | high-side; $V_{GATEHS} - V_{HB} = 4$ V | - | 560 | - | mA |
| | | high-side; $V_{GATEHS} - V_{HB} = 11$ V | - | 1.9 | - | A |
| | | low-side; $V_{GATELS} - V_{PGND} = 2$ V | - | 560 | - | mA |
| | | low-side; $V_{GATELS} - V_{PGND} = 11$ V | - | 1.9 | - | A |

The supply voltage provided by SUPREG for GATELS is constant at 10.9 V. The supply voltage for GATEHS is lower and depends on the operating conditions (see Section 6.5.4).

# 8. HBC functions

## 8.1 SNSBOOST undervoltage or brownout protection level

To prevent the HBC from operating at very low boost input voltages, the voltage on the SNSBOOST pin is sensed continuously.

After the voltage on this pin drops below VUVP(SNSBOOST) = 1.6 V, the switching of the HBC is stopped as soon as the low-side MOSFET is on. The start level is determined by an internal hysteresis current source of 3 μA in combination with the resistance values of the external divider. The boost voltage for starting is higher than the boost voltage for stopping. For starting, an additional internally fixed hysteresis of 50 mV is added to the comparator level: 1.6 V + 0.05 V = 1.65 V.

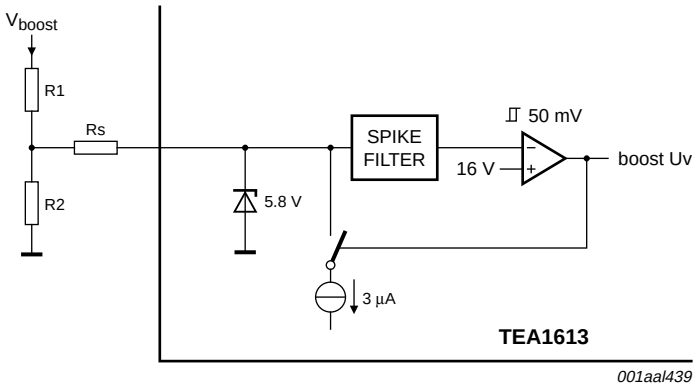



**Fig 15. SNSBOOST function**

### 8.1.1 Start and stop voltage without series resistance

The boost voltage at which the converter starts:

$$V_{Boost(start)} = R_1 \times \left(\frac{1.65\ \text{V}}{R_2} + 3\ \mu A\right) + 1.65\ \text{V} \quad (3)$$

The boost voltage at which the converter stops:

$$V_{Boost(stop)} = R_1 \times \left(\frac{1.60\ \text{V}}{R_2}\right) + 1.60\ \text{V} \quad (4)$$

**Example:**

$R_1$ = 9800 kΩ

$R_2$ = 47 kΩ

$R_s$ = 0 kΩ

$$V_{Boost(start)} = 9800\ \text{k}\Omega \times \left(\frac{1.65\ \text{V}}{47\ \text{k}\Omega} + 3\ \mu A\right) + 1.65\ \text{V} = 375\ \text{V} \quad (5)$$

$$V_{Boost(stop)} = 9800\ \text{k}\Omega \times \left(\frac{1.60\ \text{V}}{47\ \text{k}\Omega}\right) + 1.60\ \text{V} = 335\ \text{V} \quad (6)$$

### 8.1.2 Start and stop voltage with series resistance

When introducing a series resistance (Rs) in the connection of SNSBOOST, the start voltage can be increased independently.

$$V_{Boost(start,\ new)} = R_1 \times \left(\frac{1.65\ \text{V} + (R_s \times 3\ \mu A)}{R_2} + 3\ \mu A\right) + 1.65\ \text{V} + (R_s \times 3\ \mu A) \quad (7)$$

**Example:**

$R_1$ = 9800 kΩ

$R_2$ = 47 kΩ

$R_s$ = 22 kΩ

$$V_{Boost(start,\ new)} = 9800 \times \left(\frac{1.65 + (22 \times 3)}{47} + 3\right) + 1.65 + (22 \times 3) = 389\ V \quad (8)$$

### 8.1.3 SNSBOOST and compensation SNSBURST

The choices made for designing the brownout function affect the design of the burst-mode presetting on SNSBURST. If the burst mode is implemented, mainly the choice for the $V_{Boost(stop)}$ level has an effect on the (amount of) compensation current in SNSBURST. For information relating to combining both functions, see Section 9.5.2 “Advanced design of SNSBURST circuit”.

## 8.2 HBC switch control

The internal control for the MOSFET drivers, determines when the MOSFETs are switched on and off. It uses several inputs from the following functions:

- An internal divider is used to provide the alternating switching of high-side and low-side MOSFET for every oscillator cycle.
- The adaptive non-overlap (see Section 8.3) sensing on HB determines the switch-on moment.
- The oscillator (see Section 8.4) determines the switch-off moment.
- Several protection and enable functions determine if the resonant converter is allowed to switch.

## 8.3 HBC adaptive non-overlap

### 8.3.1 Inductive mode (normal operation)

The high efficiency of a resonant converter is the result of Zero-Voltage Switching (ZVS) of the power MOSFETs, also called soft-switching. To allow soft-switching, a small non-overlap time (also called dead time) is required between the on-time of the high-side MOSFET and low-side MOSFET. During this non-overlap time, the primary resonant current (dis)charges the capacitance of the half-bridge between ground and boost voltage. After the (dis)charge, the body diode of the MOSFET starts conducting and because the voltage across the MOSFET is zero, there are no switching losses.

This mode of operation is called inductive mode because the switching frequency is above the resonance frequency and the resonant tank has an inductive impedance.

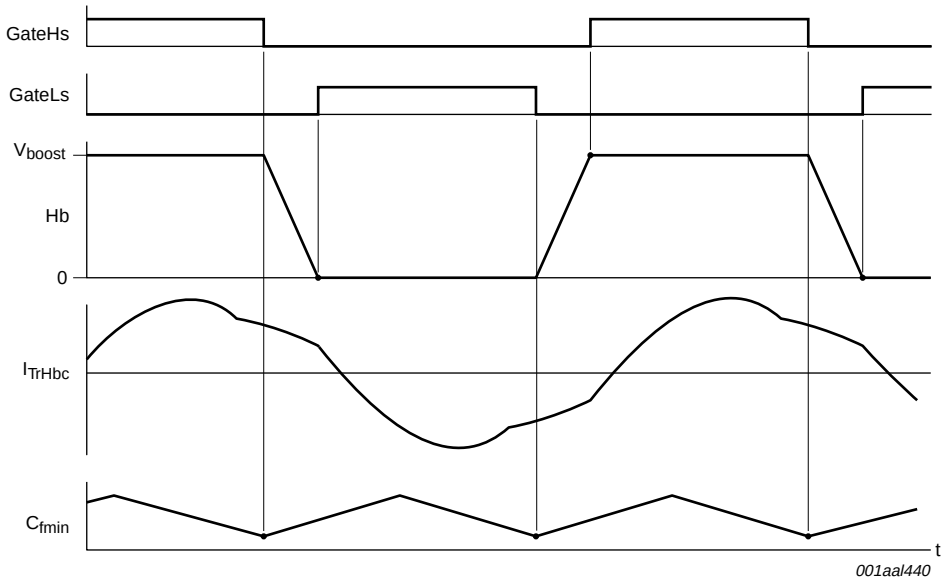



**Fig 16. Inductive mode HBC switching**

The time required for the transition of the HB depends on the amplitude of the resonant current at the moment of switching. There is a (complex) relationship between the amplitude, the frequency, the boost voltage and the output voltage. Ideally the IC should switch on the MOSFET as soon as the transition of the HB has reached its end value. To prevent a swing back of the HB voltage, it should not wait longer, especially at high output load.

The adaptive non-overlap function of the TEA1613T provides an automatic measurement and control function that decides when to switch on. As it uses actual measurement inputs, the control adapts for operation changes in time.

Because of this adaptive non-overlap function, it is not necessary to preset a fixed non-overlap time, which always is a compromise between different operating conditions.

The adaptive non-overlap function senses the slope at HB after one MOSFET has been switched-off. Normally the slope at the HB starts directly. Once the transition of the HB node is complete, the slope ends. This is detected by the adaptive non-overlap sensing

and the other MOSFET is switched-on. In this way the non-overlap time is automatically adjusted to the best value providing the lowest switching loss, even if the HB transition cannot be fully completed.

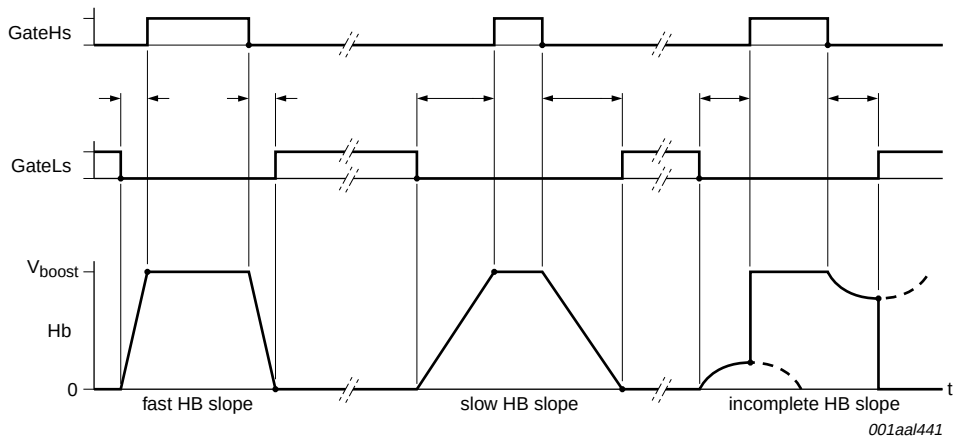



**Fig 17. Adaptive non-overlap switching during normal operating conditions**

The non-overlap time depends on the HB slope, but has an upper and lower time limit. An integrated minimum non-overlap time (160 ns) prevents accidental cross conduction in all conditions. The maximum non-overlap time is limited to the charging time of the oscillator. If the HB slope takes more time than the charging of the oscillator (25 % of HB switching period) the MOSFET is forced to switch on. In this case the MOSFET is not soft-switching. This limitation of the maximum non-overlap time ensures that at very high switching frequency the on-time of the MOSFET is at least 25 % of the HB switching period.

### 8.3.2 Capacitive mode

During error conditions (e.g. output short-circuit, load pulse too high) or special start-up conditions, the switching frequency can become lower than the resonance frequency. The resonant tank then has a capacitive impedance. In capacitive mode the HB slope doesn't start after the MOSFET has switched off. It is not preferred to just switch on the other MOSFET. The lack of soft-switching increases dissipation in the MOSFETs. The conducting body diode in the MOSFET at the switching moment can damage the device very quickly.

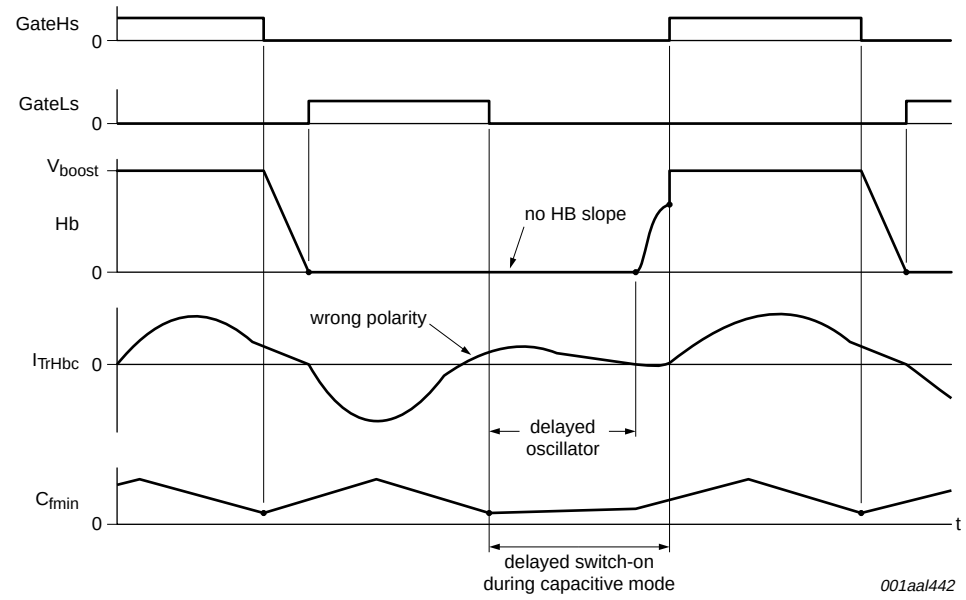



**Fig 18. Capacitive mode HBC switching**

The adaptive non-overlap system of the TEA1613T always waits until the slope at the half-bridge node starts. It guarantees safe/best switching of the MOSFETs in all circumstances. In capacitive mode, it can take half the resonance period before the resonant current changes back to the correct polarity and starts charging the half-bridge node. To allow this relatively long waiting time, the oscillator remains in its slow charging current mode until the half-bridge slope starts (see also Section 8.4.2 and Figure 22).

The MOSFET is forced to switch-on when the half-bridge slope doesn't start at all and the slowed-down oscillator reaches the high level.

To bring the converter from capacitive mode to inductive operation again, the oscillation frequency is increased by the capacitive mode regulation function.

### 8.3.3 Capacitive Mode Regulation (CMR)

The harmful switching in capacitive mode is prevented by the adaptive non-overlap function. However, to end the capacitive mode operation and go back to inductive mode operation, an extra action is executed which results in the Capacitive Mode Regulation.

Capacitive mode is detected when the HB slope doesn't start shortly (690 ns) after the MOSFET is switched-off. When the capacitive mode is detected, the switching frequency is quickly increased. This is realized by discharging SSHBC/EN with a high current (1800 μA) from the moment $t_{no\text{-}slope}$ = 690 ns has passed before the half-bridge slope starts. The resultant frequency increase regulates the HBC back to the threshold between capacitive and inductive mode.

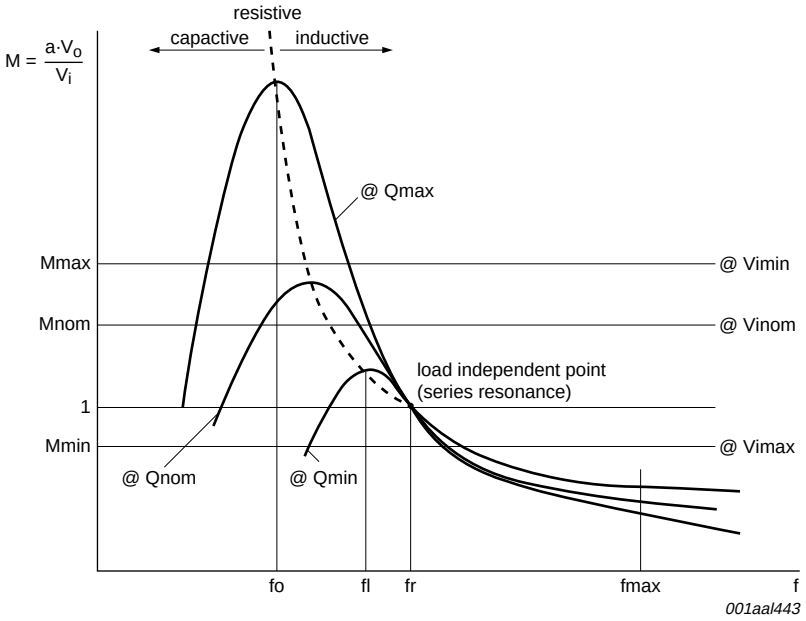
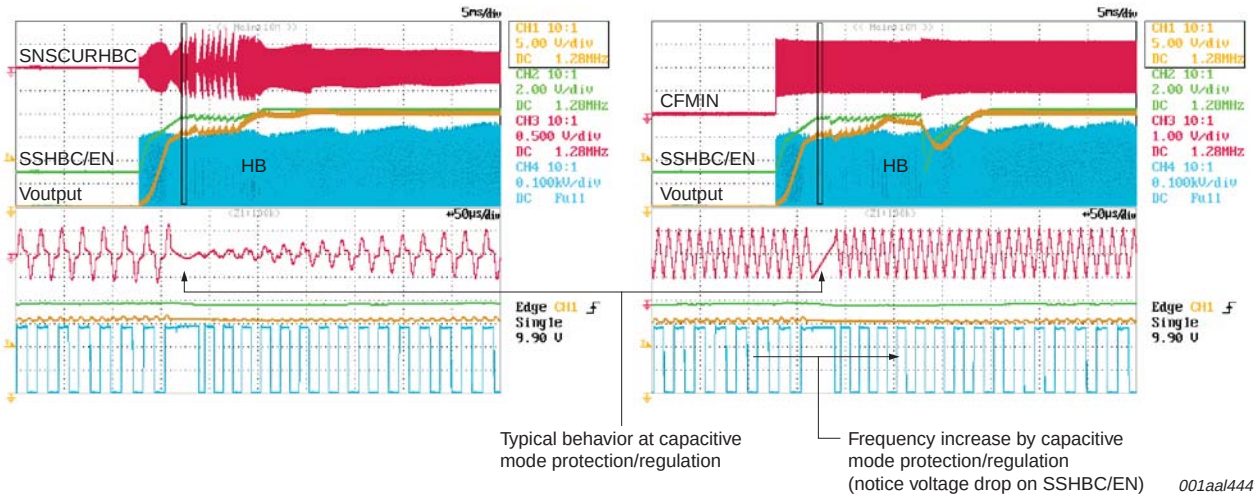



**Fig 19. Capacitive/inductive HBC operating frequencies**

CMR of the TEA1613T can be recognized by the typical slowing of the oscillator in combination with the discharging of SSHBC/EN.




Note: Oscilloscope traces contain normal time-base (top) and zoomed view (bottom)

**Fig 20. Typical protection and regulation behavior in capacitive mode (during bad start-up)**

## 8.4 HBC oscillator

The slope controlled oscillator determines the switching frequency of the half-bridge. The oscillator generates a triangular waveform at the external capacitor $C_{fmin}$.

### 8.4.1 Presets

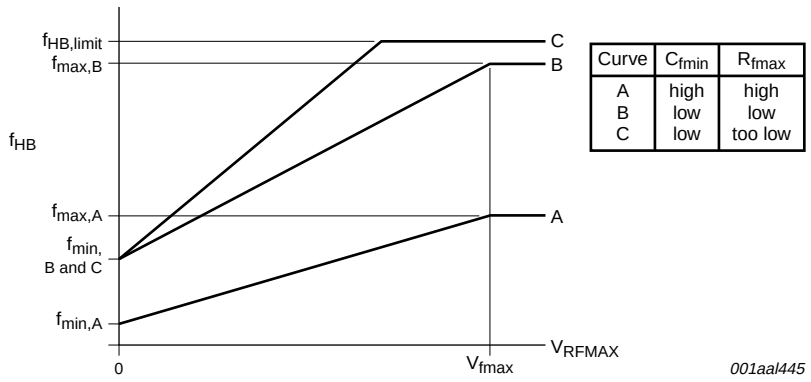
Two external components determine the frequency range:

- Capacitor at CFMIN: This sets the minimum frequency in combination with an internally trimmed current source.
- Resistor at RFMAX: This sets the frequency range and, in combination with $C_{fmin}$, the maximum frequency.

The oscillator frequency depends on the charge and discharge current of the capacitor on CFMIN. This (dis)charge current consists of a fixed part which determines the minimum frequency, and a variable part which depends on the value of the resistor on RFMAX and the voltage at pin RFMAX.

- The voltage on RFMAX is 0 V when the oscillator frequency is minimum.
- The voltage on RFMAX is 2.5 V when the oscillator frequency is maximum.
- The value of the resistor on RFMAX determines the relationship between $V_{RFMAX}$ and the frequency. It also determines the maximum frequency when $V_{RFMAX}$ = 2.5 V.

The maximum frequency of the oscillator is independent of the settings on CFMIN and RFMAX and is limited internally to a minimum of 500 kHz. Figure 21 visualizes the relationship between $V_{RFMAX}$, $R_{FMAX}$, $C_{fmin}$ and $f_{HB}$.




| Curve | $C_{fmin}$ | $R_{fmax}$ |
|---|---|---|
| A | high | high |
| B | low | low |
| C | low | too low |

**Fig 21. Frequency relationships**

### 8.4.2 Operational control

During operation, the oscillator is controlled by the state of the half-bridge node HB. To achieve this, an internal slope detection circuit monitors the voltage on HB.

The charge current of the oscillator is initially set to a low value of 30 μA. After the start of the half-bridge slope has been detected, the charge current is increased to the normal value that corresponds to the working frequency at that moment. The working frequency is controlled by feedback on SNSFB. Normally, the half-bridge slope starts directly after the switch-off of the MOSFET, the time with the low oscillator current (30 μA) being negligible.

The similarity when switching GATELS and GATEHS is that the oscillator signal determines the moment of switching off. The moment of switching on is determined by the HB sensing circuit.

As the moment of switching on is determined by the HB sensing (and therefore not fixed), the time between switching one MOSFET off and the other one on, is adaptive non-overlap time (or dead time). This non-overlap time has no influence on the oscillator signal.

The frequency control by oscillator frequency consists of determining the time between two moments of switching off (including a small period during which the oscillator current is only 30 μA).

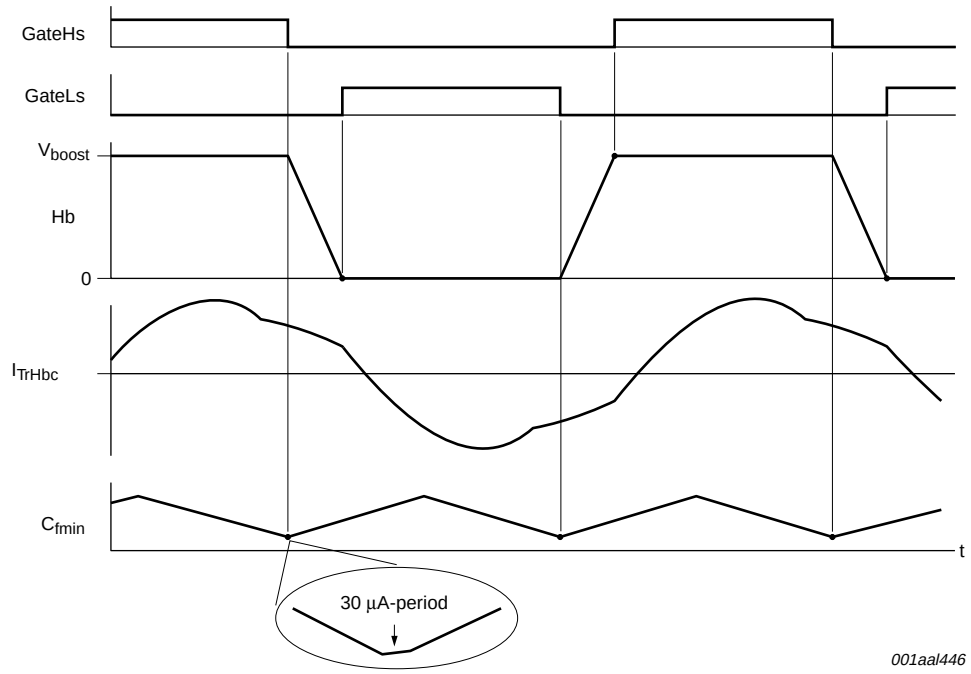



**Fig 22. Timing overview of the oscillator and HBC drive**

### 8.4.3 CFMIN and RFMAX

This section explains the method of calculating the values for the capacitor on CFMIN and the resistor on RFMAX.

#### 8.4.3.1 Minimum frequency setting for CFMIN

$$f_{oscillator} = 2 \times f_{HB} \tag{9}$$

$$t_{charge} \approx t_{discharge} \approx \frac{t_{oscillator}}{2} \tag{10}$$

$$\Delta V_{oscillator} = V_{high(CFMIN)} - V_{low(CFMIN)} = 3\ V - 1\ V = 2\ V \tag{11}$$

$$I_{oscillator(min)} = 150\ \mu A \tag{12}$$

$$CFMIN = \frac{I_{oscillator(min)}}{2 \times 2 \times f_{HB(min)} \times \Delta V_{oscillator}} = \frac{150\ \mu A}{8 \times f_{HB(min)}} \quad (13)$$

**Example:**

Given $f_{HB(min)}$ = 57 kHz

$$CFMIN = \frac{150\ \mu A}{2 \times 2 \times 57\ \text{kHz} \times 2} = \frac{0.00015}{456000} = 329\ \text{pF} \quad (14)$$

#### 8.4.3.2 Maximum frequency setting for RFMAX

$$I_{oscillator(max)} = 4.7^{(note)} \times I_{RFMAX(max)} + I_{oscillator(min)} \quad (15)$$

$$I_{RFMAX(max)} = \frac{V_{f(max)}}{RFMAX} \quad (16)$$

$$RFMAX = \frac{V_{f(max)}}{I_{RFMAX(max)}} = \frac{2.5\ \text{V}}{I_{RFMAX(max)}} \quad (17)$$

Analog to the situation with $I_{oscillator(min)}$:

$$f_{HB(max)} = \frac{I_{oscillator(max)}}{4 \times CFMIN \times \Delta V_{oscillator}} = \frac{4.7 \times I_{RFMAX(max)} + I_{oscillator(min)}}{4 \times CFMIN \times 2} \quad (18)$$

$$I_{RFMAX(max)} = \frac{8 \times CFMIN \times f_{HB(max)} - I_{oscillator(min)}}{4.7} \quad (19)$$

$$I_{RFMAX(max)} = \frac{8 \times CFMIN \times f_{HB(max)} - 150\ \mu A}{4.7} \quad (20)$$

$$RFMAX = \frac{2.5\ \text{V}}{I_{RFMAX(max)}} = \frac{11.75\ \text{V}}{8 \times CFMIN \times f_{HB(max)} - 150\ \mu A} \quad (21)$$

**Example:**

Requirement - $f_{HB(max)}$ = 180 kHz and CFMIN = 330 pF

$$I_{RFMAX(max)} = \frac{8 \times 330\ \text{pF} \times 180\ \text{kHz} - 150\ \mu A}{4.7} = \frac{(475\ \mu A - 150\ \mu A)}{4.7} = 69.15\ \mu A \quad (22)$$

$$RFMAX = \frac{2.5\ \text{V}}{69.15\ \mu A} = 36\ \text{k}\Omega \quad (23)$$

**Remark:** Note that the average multiplication factor is 4.7. There is a small deviation in value depending on other parameters and presetting conditions. Practical verification of the result is advised.

### 8.4.4 RFMAX and High Frequency Protection (HFP)

Normally the converter does not operate continuously at the preset maximum frequency. This maximum frequency is only used for a short time during soft-start or temporary fault/overload conditions.

When the operating frequency remains at, or close to, maximum frequency for a longer period, a fault condition is assumed and a protection activated.

For this, the HFP senses the voltage at pin RFMAX. This voltage indicates the actual operating frequency. When the frequency is higher than approximately 75 % of the frequency range (RFMAX = 1.83 V), the protection timer is started.

Be aware that during normal regulation the maximum frequency is limited to only 60 % of the present range and $V_{RFMAX}$ is a maximum of 1.5 V.

## 8.5 HBC feedback (SNSFB)

A typical power supply application contains mains insulation in the HBC. On the secondary (mains insulated) side, the output voltage is compared to a reference and amplified. The TEA1613T is normally placed on the primary side. The output of the error amplifier is transferred to the primary side via an optocoupler. The output of the optocoupler on the primary side can be connected directly to SNSFB.

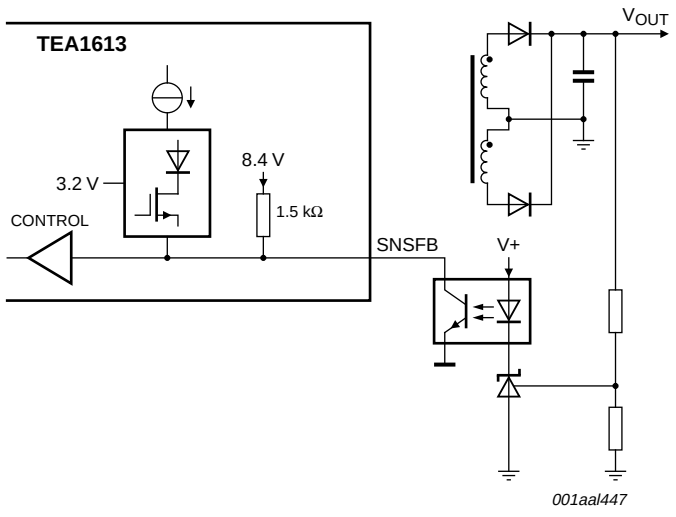



**Fig 23. Typical basic SNSFB application**

The SNSFB pin supplies the optocoupler from an internal voltage source of 8.4 V via an internal series resistor of 1.5 kΩ. The internal series resistance also allows spike filtering by an external capacitor at the pin.

To ensure sufficient bias current for proper working of the optocoupler, the feedback input has a threshold current of 0.66 mA at which the frequency is minimum. The maximum frequency controlled by SNSFB is reached at 2.2 mA. Notice that this is only approximately 60 % of the total preset frequency range. The remaining upper part of the present frequency range can only be reached by control of SSHBC/EN in case of soft-start or protection.

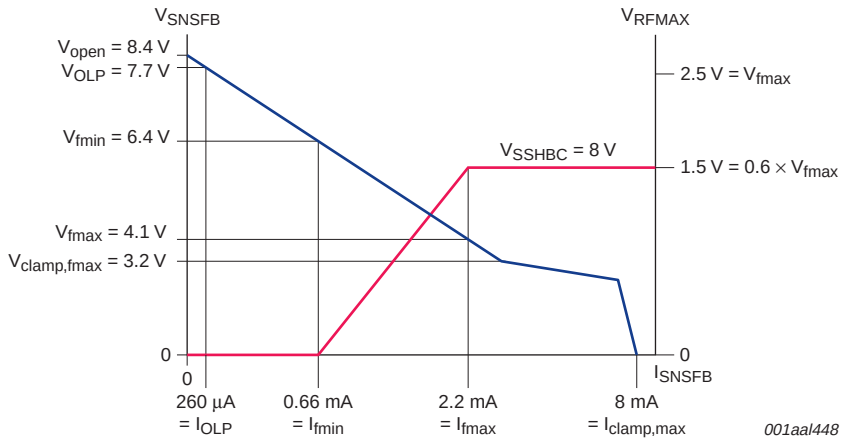
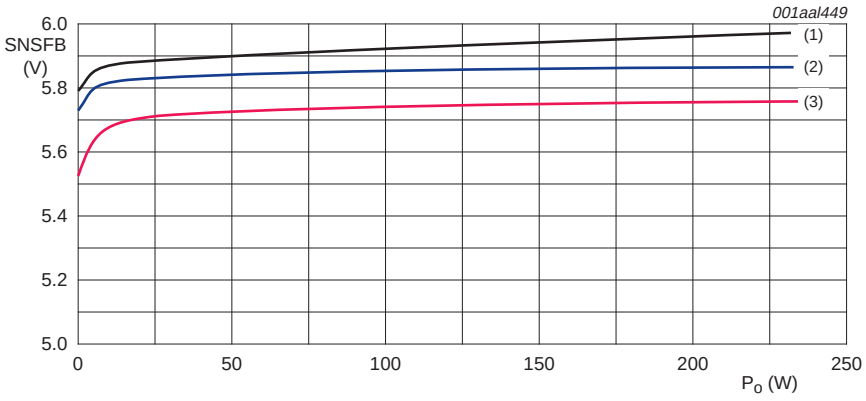



**Fig 24. SNSFB V-I characteristics**




(1) $V_{BOOST}$ = 310 V DC

(2) $V_{BOOST}$ = 350 V DC

(3) $V_{BOOST}$ = 390 V DC

**Fig 25. SNSFB voltage to output power characteristics examples**

### 8.5.1 HBC Open Loop Protection (OLP)

The resonant controller of the TEA1613T contains an Open-Loop Protection (OLP). This protection monitors the voltage on SNSFB. When it exceeds 7.7 V, the protection timer is started.

In normal operating conditions, the optocoupler current is between 0.66 mA and 2.2 mA which pulls down the voltage at pin SNSFB. If an error occurs in the feedback loop, the current can become less than 260 µA which leads to an open loop protection.

**Burst mode and open loop protection**

To implement a burst mode, a resistor divider is connected between SNSFB and ground. The impedance of this resistor divider should be significantly higher than 30 kΩ to keep the Open Loop Protection function. If the lower resistance value is lower, the voltage is lower than the threshold voltage of 7.7 V. This disables open loop error detection.

## 8.6 SSHBC/EN soft-start and enable

The SSHBC/EN pin provides the following three functions:

- Enables the IC (> 2.2 V)
- It performs an HBC frequency sweep during soft-start from 3.2 V to 8 V
- It provides frequency control during protection

Seven internal current sources operate the frequency control depending on the required action i.e.

- Soft-start + Over-Current Protection: high/low charge (160 μA/40 μA) + high/low discharge (160 μA/40 μA)
- Capacitive Mode Regulation: high/low discharge (1800 μA/440 μA)
- General: bias discharge (5 μA)

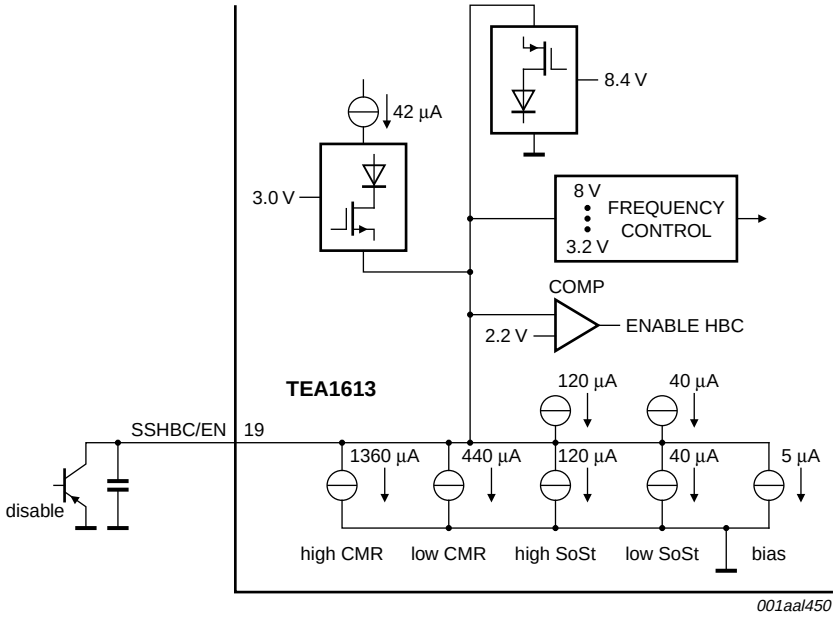



**Fig 26. SSHBC/EN: overview of sources, clamps and levels**

### 8.6.1 Switching on and off using an external control function

The SSHBC/EN can be used to switch the converters on and off using an external control function.

This function is often driven by a microcontroller from the secondary side of the optocoupler. By doing this, the main power supply [HBC and PFC (when supplied by an auxiliary of HBC)] can be switched off for Standby mode and on for normal operation. In such a concept a separate standby supply is needed to supply the microcontroller functions during the standby.

The TEA1613T also offers the possibility to switch on/off using the SNSBURST function. This function is intended for burst-mode operation where the duration of the on- and off-states are short.

#### 8.6.1.1 Switching on and off using SSHBC/EN

When a voltage is present at pin SUPHV or at pin SUPIC, a current of 42 μA from the SSHBC/EN pin charges the external capacitor. If the pin is not pulled-down, this current initially lifts the voltage to 3.0 V. Since this is above the enable level (2.2 V), the IC is enabled.

The IC can be disabled by pulling down the SSHBC/EN pin below 2.2 V. The HBC continues until the low-side stroke is active. The pull-down current must be larger than the current capability from the internal soft-start clamp: i.e. 42 μA.

#### 8.6.1.2 Hold and continue

The SNSBURST function can be used to start and stop the HBC. This method is intended for burst-mode operation to switch off the converters for only a short time. It is possible to either operate only the HBC in burst-mode or both HBC + PFC simultaneously (by use of the SNSOUT/PFCON signal). The possibilities are similar to SSHBC/EN with the main difference being that HBC continues without soft-start. For more details on burst mode operation, see Section 9.1.

### 8.6.2 Soft-start HBC

The soft-start function for the resonant converter is provided by SSHBC/EN.

The relationship between switching frequency and output current/power is not constant. It depends strongly on output voltage and boost voltage and the relationship can be complex. To ensure that the resonant converter starts or re-starts with safe currents, the TEA1613T has a soft-start function.

The soft-start function forces a start at high frequency so that currents are acceptable in all conditions. It slowly decreases the frequency until the output voltage regulation has taken over the frequency control. The limitation of the output current during start-up also limits the output voltage rise and prevents an overshoot.

During soft-start, and in parallel with the soft-start frequency sweep, the SNSCURHBC function monitors the primary current and can activate regulation in case of a (temporary) overpower situation.

The soft-start uses the voltage at pin SSHBC/EN. The timing (duration) of the soft-start event is set by an external capacitor on SSHBC/EN.

As the SSHBC/EN is also used as an input enable, the soft-start functionality is above the enable related voltage levels (see Figure 27).

#### 8.6.2.1 Soft-start voltage levels

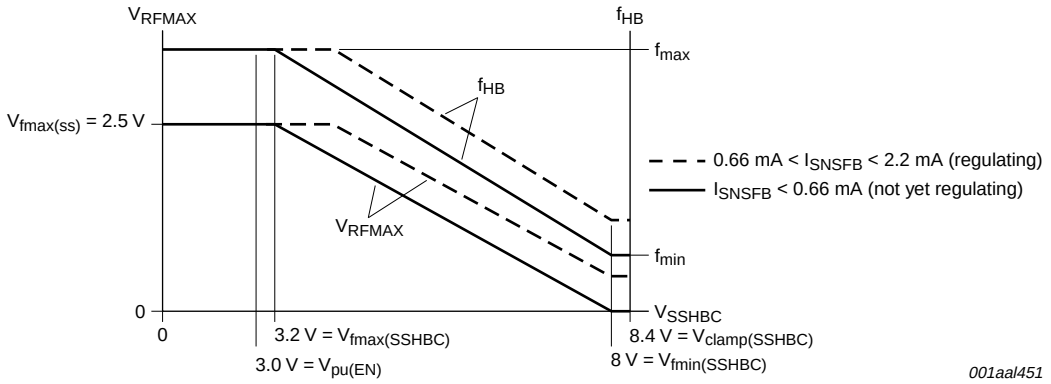



**Fig 27. Operating frequencies related to SSHBC/EN voltage**

At start-up, the SSHBC/EN voltage is low which corresponds to the maximum frequency. During the soft-start procedure, the external capacitor is charged, the SSHBC/EN voltage rises and the frequency decreases. The contribution of the soft-start function ends when SSHBC/EN is above 8 V.

The SSHBC/EN voltage is clamped at 8.4 V and remains at that level during normal operation.

When the voltage on SSHBC/EN is reduced during protection or regulation, the voltage is clamped at 3.0 V. This is to provide a quick response so that the operating frequency can be reduced again. Below 3.2 V the discharge current is reduced to 5 μA.

#### 8.6.2.2 SSHBC/EN charge and discharge

During initial start-up, the soft-start external capacitor on SSHBC/EN is only charged to obtain a decreasing frequency sweep from maximum to operating frequency.

Besides the function to soft-start, SSHBC/EN is also used for regulation purposes such as over-current regulation. Therefore the voltage on the capacitor on SSHBC/EN can vary by charging and discharging it by internal current sources.

For example: in case of over-current regulation, a continuous alternation between charging and discharging of the SSHBC/EN capacitor occurs. In this way the SSHBC/EN voltage can be regulated, thereby overruling the signal on the feedback input SNSFB.

The (dis)charge current can have a high value ±160 μA or a low value ±40 μA. The two-speed soft-start sweep of the TEA1613T allows a combination of a short start-up time of the resonant converter and stable regulation loops such as overcurrent regulation.

In some cases there can be a situation when overcurrent regulation is activated during the soft-start sequence. This results in a feedback controlled or corrected soft-start.

The fast (dis)charge speed is used for the upper frequency range where $V_{SSHBC/EN}$ is below 5.6 V. In the upper frequency range the current and power in the converter do not react strongly to fast frequency variations.

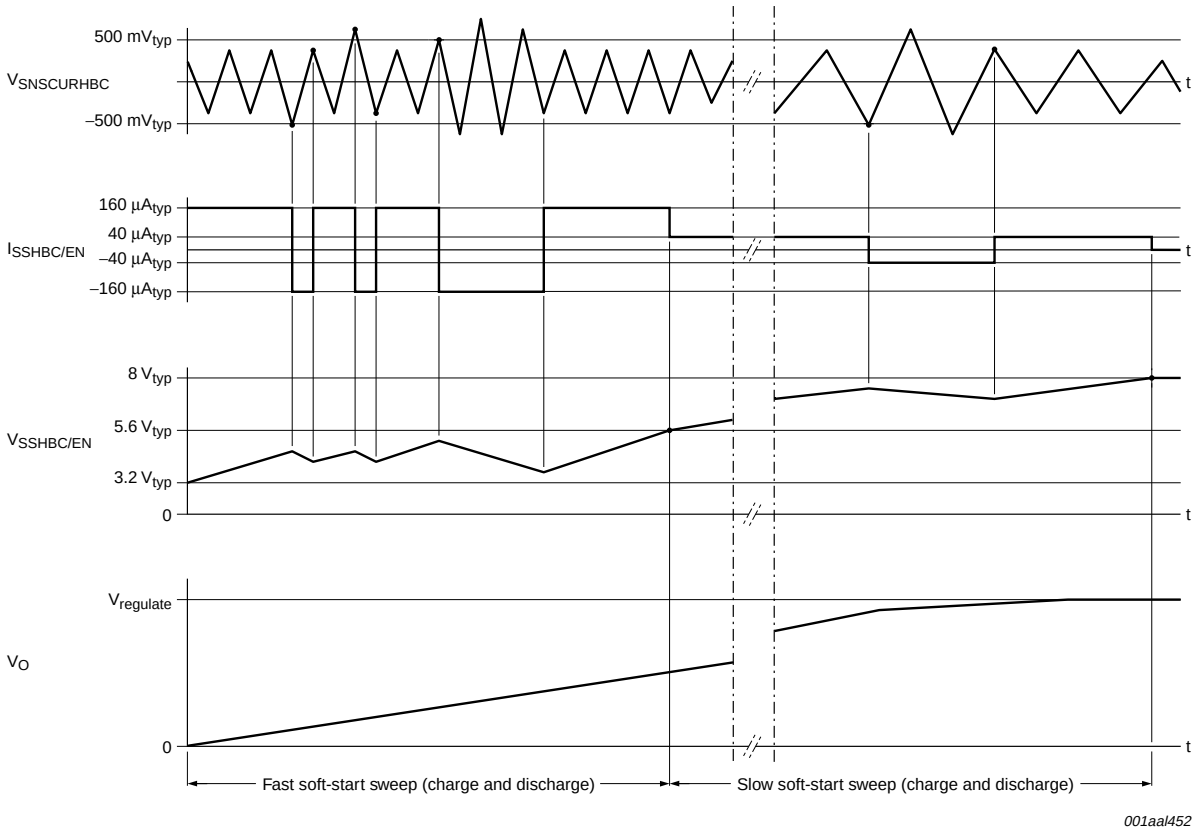



**Fig 28. OverCurrent Regulation (OCR) during start-up**

The slow (dis)charge speed is used for the lower frequency range where $V_{SSHBC/EN}$ is above 5.6 V. In the lower frequency range the current in the converter reacts strongly to frequency variations.

**Burst mode**

The soft-start capacitor is neither charged nor discharged during the no-operation time in burst mode operation. The soft-start voltage does not change during this time.

### 8.6.2.3 SNSFB, SSHBC/EN and soft-start reset - operating frequency control

The operating frequency can be controlled by the SNSFB and SSHBC/EN simultaneously. SSHBC/EN is dominant to provide protection and soft-start capability. In addition, there is an internal soft-start reset mechanism that overrules both SNSFB and SSHBC/EN control inputs and immediately sets the frequency to maximum.

### 8.6.2.4 Soft-start reset

Some protection functions require a fast correction of the operating frequency to the maximum value, but it is not needed to stop switching. The overcurrent protection is an example (see Table 3).

When this protection is activated, the control input of the oscillator is disconnected internally from the soft-start capacitor at pin SSHBC/EN and the switching frequency is immediately set to maximum. In most cases, the change to the maximum switching

frequency restores safe switching operation. Once the voltage at pin SSHBC/EN has reached 3.2 V, the control input of the oscillator is connected to the pin again and the normal soft-start sweep follows. Figure 29 shows the soft-start reset and the two-speed frequency downward sweep.

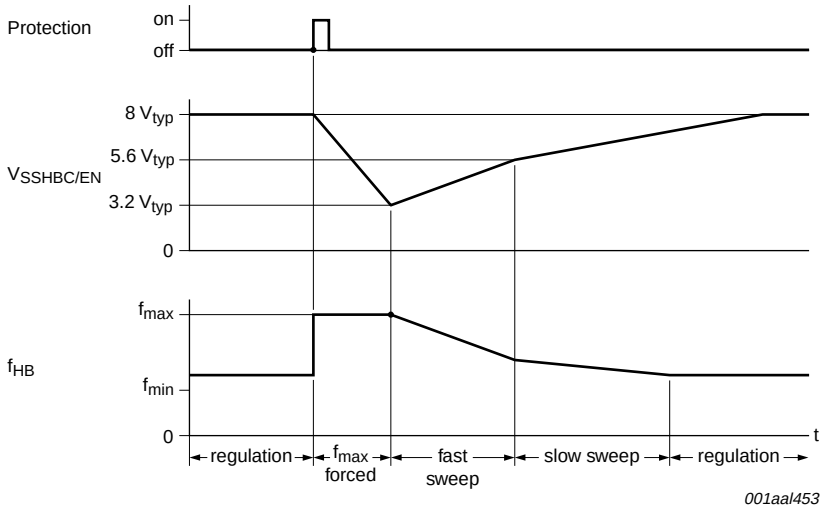



**Fig 29. Soft-start reset and two-speed soft-start**

The soft-start reset is also used to ensure a safe start-up at maximum frequency when the HBC is enabled by SSHBC/EN or after a restart. The soft-start reset is not used when the operation is stopped for burst mode.

## 8.7 Overcurrent protection and regulation HBC

Measurement of the primary resonant current indicates the level of output power that is being generated by the converter. In case of a fault or output overload condition, this current often increases considerably. By monitoring this current and then taking the appropriate action, the converter can remain operational.

The resonant controller of the TEA1613T has two functions when in an over-current condition:

- OverCurrent Regulation (OCR) slowly increases the frequency and the protection timer is started
- OverCurrent Protection (OCP) steps immediately to maximum frequency

A boost voltage compensation function is included to reduce the variation in the preset protection level of the resonant current.

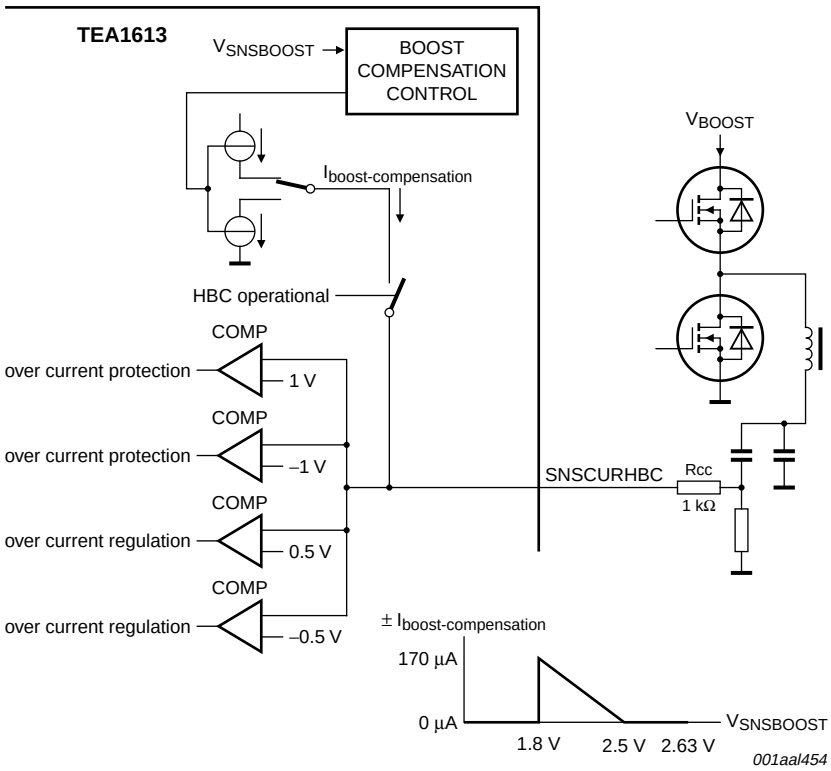



**Fig 30. OCP and regulation HBC**

### 8.7.1 HBC overcurrent regulation

The lowest comparator levels of ±0.5 V at the SNSCURHBC pin belong to the Over-Current Regulation (OCR) level. There is a comparator for both the positive and negative polarity. If either level is exceeded, the frequency is increased slowly. This is accomplished by discharging the soft-start capacitor on the SSHBC/EN pin. Every time the OCR level is exceeded, the state is latched until the next stroke and the soft-start discharge current is enabled. When both the positive and negative OCR levels are exceeded, the soft-start discharge current flows continuously. In this way the operating frequency is slowly increased until the resonant current value just reaches the value permitted by the preset.

The behavior during OCR can be observed on the SSHBC/EN pin as a resultant regulation voltage.

When an OCR situation is present for a long time, a serious fault condition is assumed. During OCR the protection timer is activated. The charging of the protection timer is active approximately a half period cycle after the ±0.5 V level is exceeded. If the detection levels are continuously exceeded, the timer is charged continuously. However, if the detection levels are only sometimes exceeded, the timer is charged accordingly. The restart state is activated when RCPROT reaches the protection level of 4 V.

**Start-up**

The OverCurrent Regulation is very effective for limiting the output current during start-up. A smaller soft-start capacitor can be chosen which allows faster start-up. The small soft-start capacitor may sometimes result in an excessive output current but the OCR function can slow down the frequency sweep to keep the output current within the limits.

### 8.7.2 HBC overcurrent protection

In most cases the OverCurrent Regulation is able to keep the current below the set maximum values. During certain error conditions however, the OCR might not be fast enough to limit the current. The OverCurrent Protection (OCP) is implemented to protect against these error conditions.

The internal OCP level is set to ±1 V for SNSCURHBC. This is significantly higher than the OCR level of ±0.5 V. When the OCP level is reached the frequency immediately jumps to the maximum via a soft-start reset procedure, followed by a normal sweep down.

The maximum frequency value for soft-start must be chosen to be able to limit the output power in these conditions sufficiently.

The behavior during OCP can be observed on the SSHBC/EN pin as a new soft-start. Depending on the (over)load or fault condition during this new soft-start, OCR or OCP can be activated again.

### 8.7.3 SNSCURHBC boost voltage compensation

The primary current, also called resonant current, is sensed via pin SNSCURHBC. It senses the momentary voltage across an external current sense resistor. The use of the momentary current signal allows a fast OCP and simplifies the stability of the OCR. The OCR and OCP comparators compare the SNSCURHBC voltage to the maximum positive and negative values.

For the same output power, the primary current is higher when the boost voltage is low. To reduce the dependency of the protected output current level for the boost voltage, a boost compensation is included. The boost compensation sources and sinks a current from the SNSCURHBC pin. This current creates a voltage drop across the series resistor Rcc. A typical value for this resistor is 1 kΩ.

The amplitude of the current depends linearly on the boost voltage. At nominal boost voltage the current is zero and the voltage across the current sense resistor is also present at the SNSCURHBC pin. At the boost start level SNSBOOST = 1.8 V and the current is a maximum of 170 μA. The direction of the current, sink or source, depends on the active gate signal. The voltage drop created across Rcc reduces the voltage amplitude at the pin, resulting in a higher effective current protection level. The amount of compensation is set by the value of Rcc.

### 8.7.4 Current measurement circuits

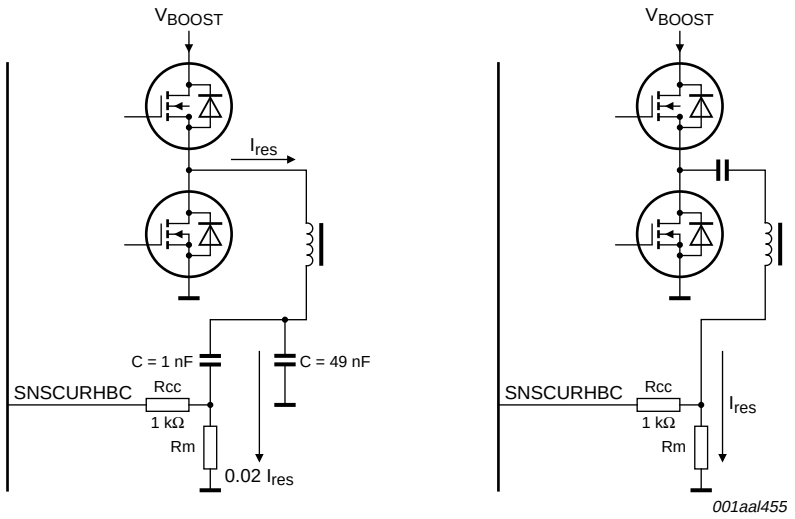



**Fig 31. SNSCURHBC: resonant current measurement configurations**

### 8.7.5 SNSCURHBC layout

Because the SNSCURHBC must be able to accurately sense the measurement signal cycle-by-cycle at higher frequencies, it is susceptible to disturbances. To prevent disturbances on this input, the series resistor Rcc should be placed close to the IC to reduce the length of the track that can pick up disturbing signals. As the impedance of the measurement resistor is normally low, the length of signal track between Rcc and the measurement resistor is not critical regarding disturbance.

# 9. Burst mode operation

Burst mode operation can be used to improve the efficiency at low output loads.

By temporarily interrupting the switching, losses during the idle time are minimized. Because the average power needed for the output is very low, it is easy for the converter to deliver it during a short time of conversion which is a burst.

The burst mode operation of the TEA1613T is based on interrupting the switching while maintaining regulation. Using an internal comparator, the regulation voltage can be monitored to determine when to stop switching and when to continue. When restarting after an interruption, no soft-start is applied as the system is still in regulation (close to the regular working point). The timing of switching on and off is determined by the regulation-loop of the system (normally by the output voltage). This deliberately creates a small ripple on the output voltage during burst mode.

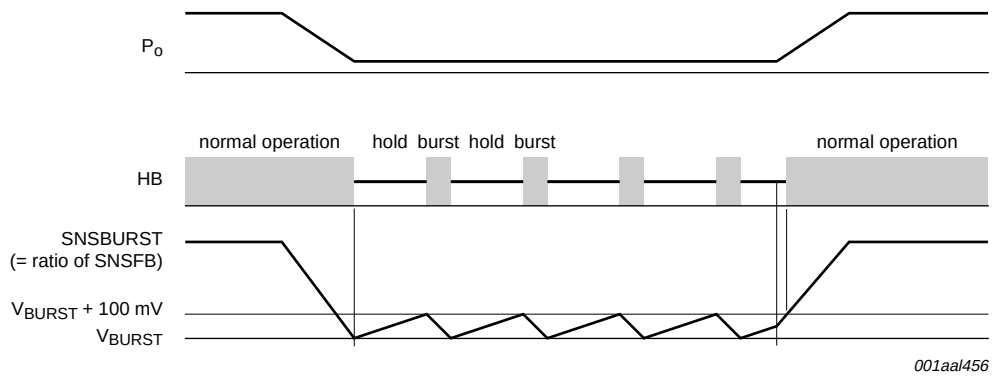



**Fig 32. Principle of burst mode operation with SNSFB and comparator levels**

## 9.1 Burst mode implementation

Burst mode can be Implemented by a resistance divider from SNSFB to ground.

The comparator input monitors the regulation voltage SNSFB to a preset burst voltage value by $R_{BURST1}$ and $R_{BURST2}$. When the HBC output power is low, the regulation voltage decreases. When the regulation voltage reaches $V_{BURST}$ = 3.5 V, the switching stops, no energy is converted and the output voltage drops. Following this, the regulation voltage increases again. As soon as the regulation voltage reaches $V_{BURST}$ + 100 mV, the switching resumes.

When the delivered power, during a burst, is larger than needed for the output, the regulation voltage SNSFB quickly decreases again, stopping the switching at $V_{BURST}$. The time needed for the regulation voltage to reach $V_{BURST}$, mainly depends on the output voltage and its load.

When the HBC output load increases to high levels, normal operation is resumed again as the regulation voltage does not reach the $V_{BURST}$ level.

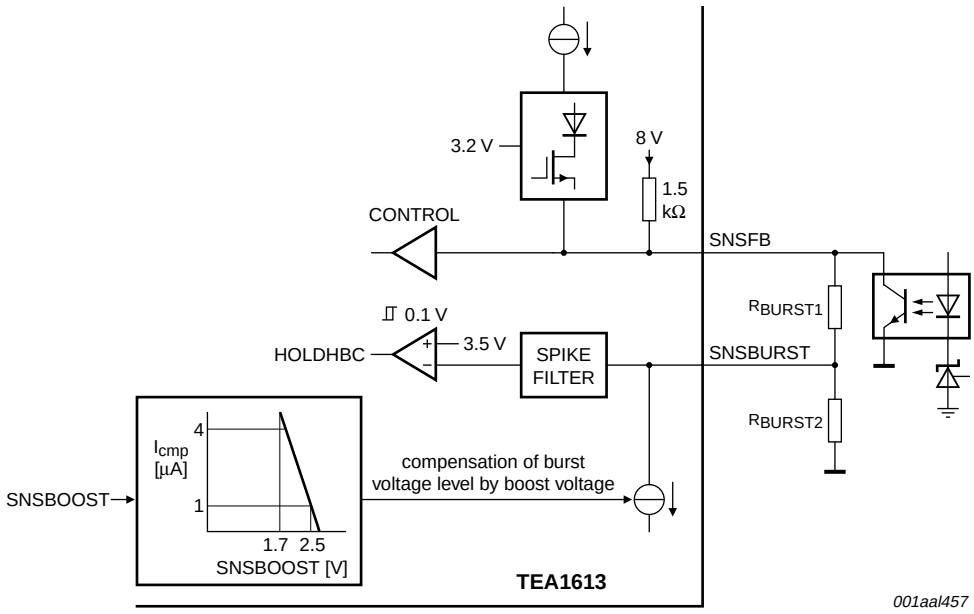



**Fig 33. Burst mode application**

## 9.2 PFC burst mode operation control by SNSOUT/PFCON

The PFC can be made to burst simultaneously with the HBC in burst mode. By doing this, the converters operate for a limited time, followed by a time of no-operation. Burst mode operation increases the efficiency in low-load conditions.

The SNSOUT/PFCON provides an on/off switching signal that can be used to stop and start the PFC. This signal switches between the voltage level for output voltage monitoring (2.35 V < $V_{SNSOUT/PFCON}$ < 3.5 V) and ground. An internal switch makes this voltage low when the HBC is put on hold by the SNSBURST function.

The behavior and interfacing circuit of this system for synchronous burst mode depends on the properties of the PFC-control circuit.

## 9.3 Advantages of burst mode in HBC

The main reason for applying burst mode in a resonant converter is to improve the efficiency at low output power by reducing the power losses.

The graphs in Figure 34 and Figure 35 show the principle improvements in a 250 W resonant converter including (non-bursting) PFC.

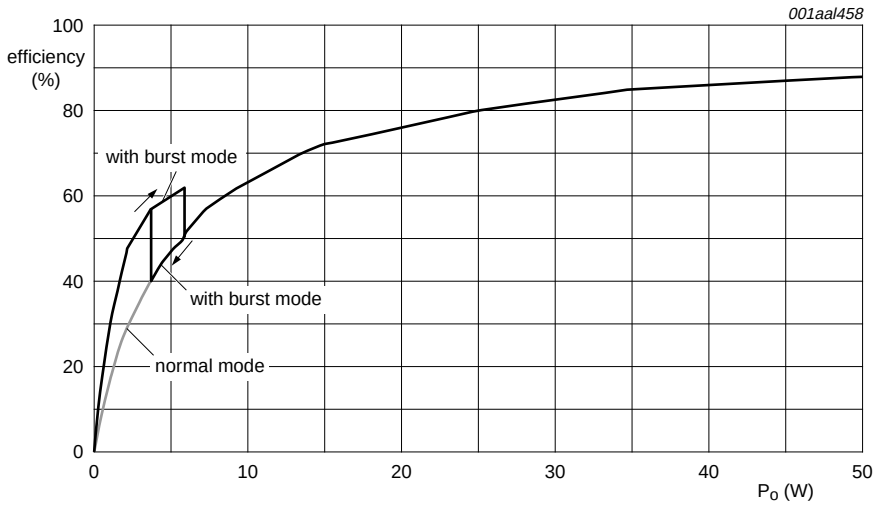



**Fig 34. Improved efficiency by HBC burst mode in a 250 W converter**

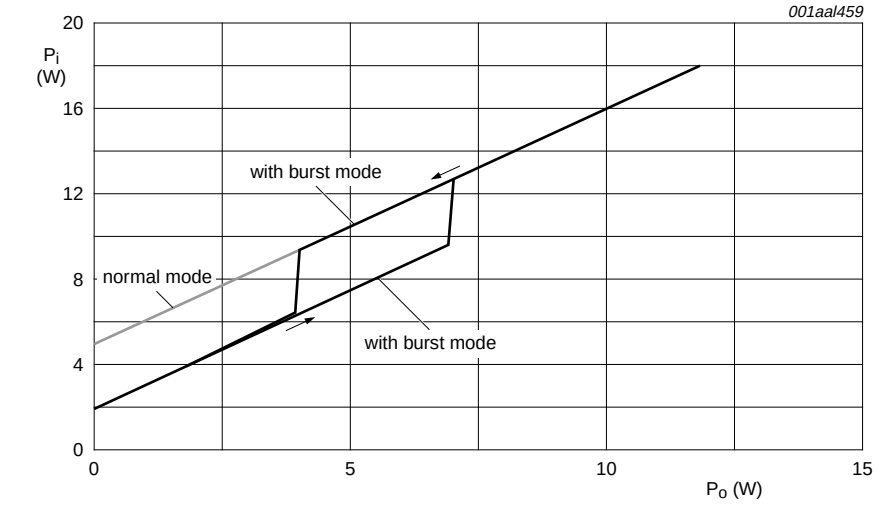



**Fig 35. Reduced losses by HBC burst mode in a 250 W converter**

## 9.4 Advantages of burst mode for HBC and PFC simultaneously

The TEA1613T provides a burst mode system that simultaneously switches the HBC and PFC. In this way, during the burst period, the power is transferred directly from the input to the output. The HBC determines the repetition time of the burst and the PFC follows. In the burst period, the PFC operates in normal regulation.

Power consumption is further reduced by PFC bursting. Examples of results obtained are shown in Figure 36, Figure 37 and Figure 38.

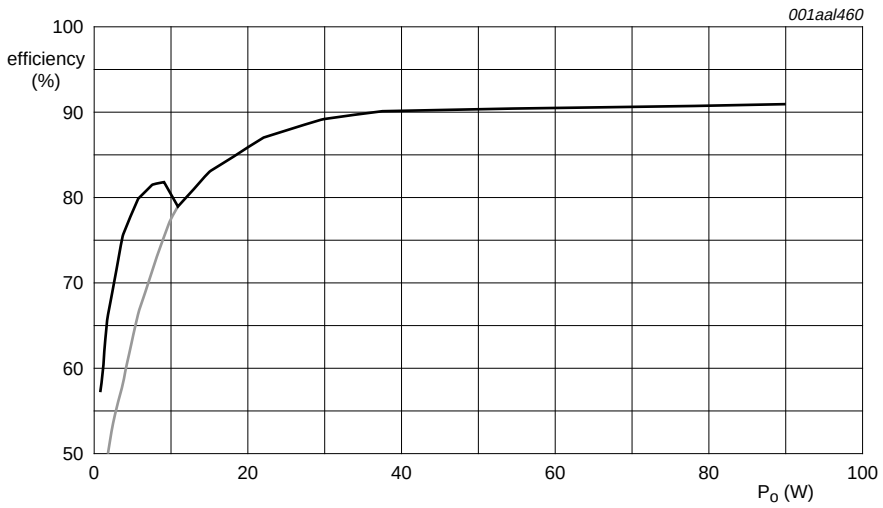



**Fig 36. Increased efficiency at low output power in burst HBC and PFC (90 W adapter)**

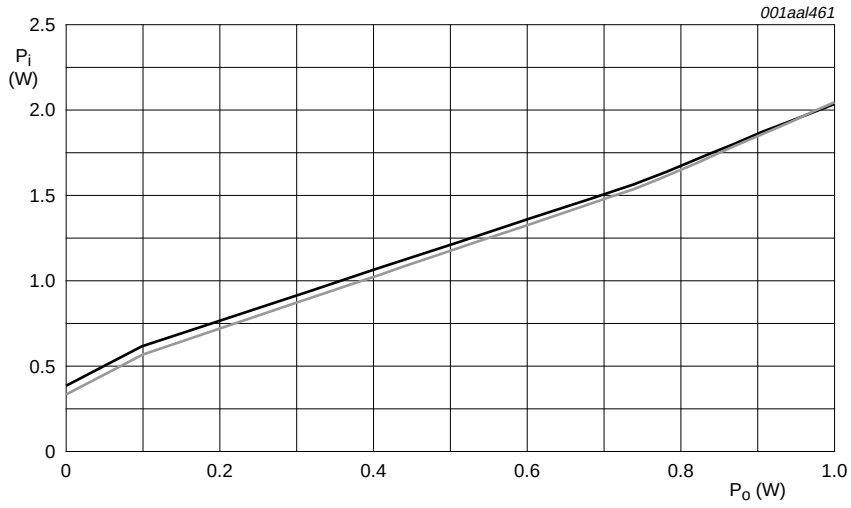



**Fig 37. Remaining 90 W adapter losses in burst mode**

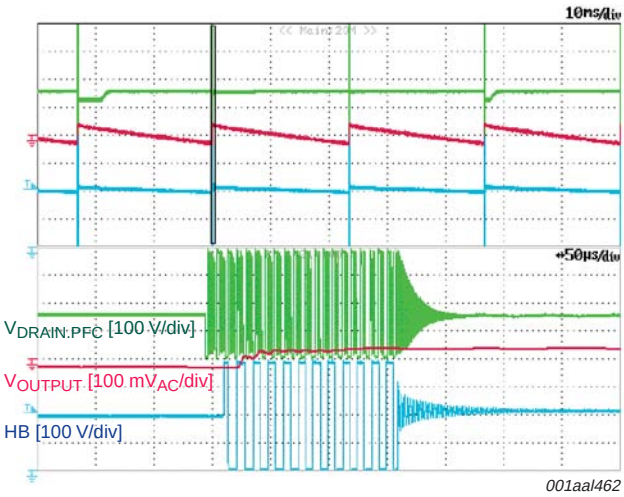



**Fig 38. Simultaneous HBC and PFC burst mode operation (and output voltage ripple)**

## 9.5 Choice of burst level and divider impedance

The power level at which burst mode is activated is set by a resistor divider on SNSFB. The burst mode ($V_{BURST}$ = 3.5 V) is activated by the internal comparator on SNSBURST at the SNSFB voltage level which can be chosen experimentally.

### 9.5.1 Basic design of an SNSBURST circuit

The SNSFB voltage level at which the converter enters burst mode can be chosen by a resistor divider. This voltage value can be adapted to correspond with the internal preset level of 3.5 V on the SNSBURST comparator.

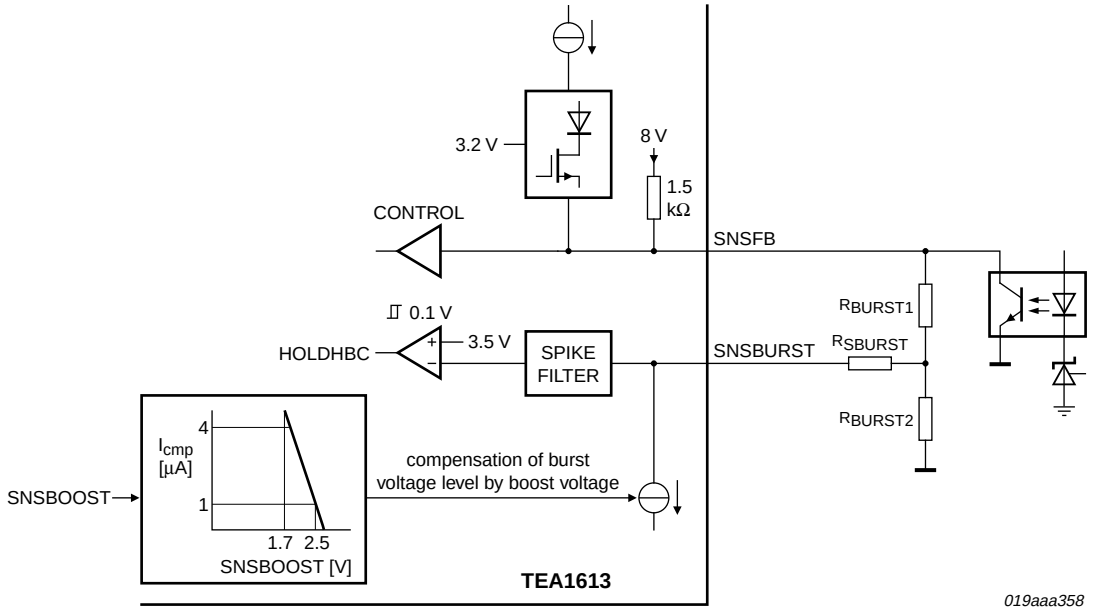



**Fig 39. Designing the burst mode level using two resistor values**

The optimum level for burst mode can be determined experimentally as demonstrated in the following example.

**Example:**

The required burst level frequency $f_{HB(burst)}$ = 90 kHz which corresponds to SNSFB = 5.4 V.

For the basic presetting of the burst level, the internal compensation function can be neglected.

$$3.5\ V = 5.4\ V \times \left(\frac{R_{BURST2}}{R_{BURST1} + R_{BURST2}}\right) \quad (24)$$

This can be provided by the following values:

$R_{BURST1}$ = 36 kΩ,

$R_{BURST2}$ = 68 kΩ.

### 9.5.2 Advanced design of SNSBURST circuit

Tolerance on the value of the converters input voltage (boost voltage) can have a considerable effect on the performance in burst mode. The SNSBURST function provides a possibility to compensate the preset burst level for variations in the boost voltage.

The impedance of the resistor divider determines the amount of compensation. The higher the impedance, the stronger the compensation is.

**Remarks:**

- Note that a very high impedance is more susceptible to disturbance
- The impedance should be higher than 20 kΩ to maintain normal regulation properties on SNSFB and higher than 90 kΩ to prevent disabling the OLP function on SNSFB
- The general advice is to use a total impedance ($R_{BURST1}$ + $R_{BURST2}$) of 100 kΩ or higher

The compensation is obtained by an internal current source whose current value depends on the SNSBOOST voltage. This current flows into the SNSBURST pin and gives a voltage offset, depending on the resistance value of the (external) divider.

Because the SNSBOOST voltage determines the value of the compensation current, the design of this function provides the nominal calculation value according to the relationship shown in Figure 40.

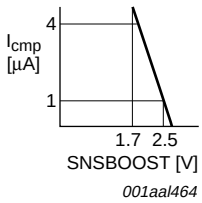



**Fig 40. Compensation current on SNSBURST**

The amount of compensation needed to obtain a more constant performance, can be determined during a few practical trials. This should give an indication of the target for the total impedance of the divider.

**Example:**

Nominal SNSBOOST voltage is 2.5 V with $I_{cmp}$ = 1 µA.

The required burst frequency $f_{HB(burst)}$ = 90 kHz which corresponds to SNSFB = 5.4 V.

Best compensation performance found with $R_{BURST1}$ is approximately 91 kΩ.

$$V_{SNSFB} = 3.5\ \text{V} + R_{BURST1} \times I_{cmp} + R_{BURST1} \times \frac{3.5\ \text{V}}{R_{BURST2}} = 5.4\ \text{V} \quad (25)$$

$$R_{BURST1} \times \left(1\ \mu A + \frac{3.5\ \text{V}}{R_{BURST2}}\right) = 1.9\ \text{V} \quad (26)$$

$R_{BURST2}$ = 176 kΩ

To obtain a better overview of the relationship between SNSBOOST and SNSBURST, regarding the compensation design, the calculation sheet can used. The sheet provides more details and the possibility to visualize the result of value variation.

In the calculation sheet, an indicator is calculated on the amount of boost compensation that is obtained for a certain situation. The indicator gives the change in burst frequency preset (above which frequency level, the regulation enters burst mode) due to the change in boost voltage.

For the given example this indicator amounts to: 72 Hz/V

### 9.5.3 Advanced design of SNSBURST circuit using a series resistor

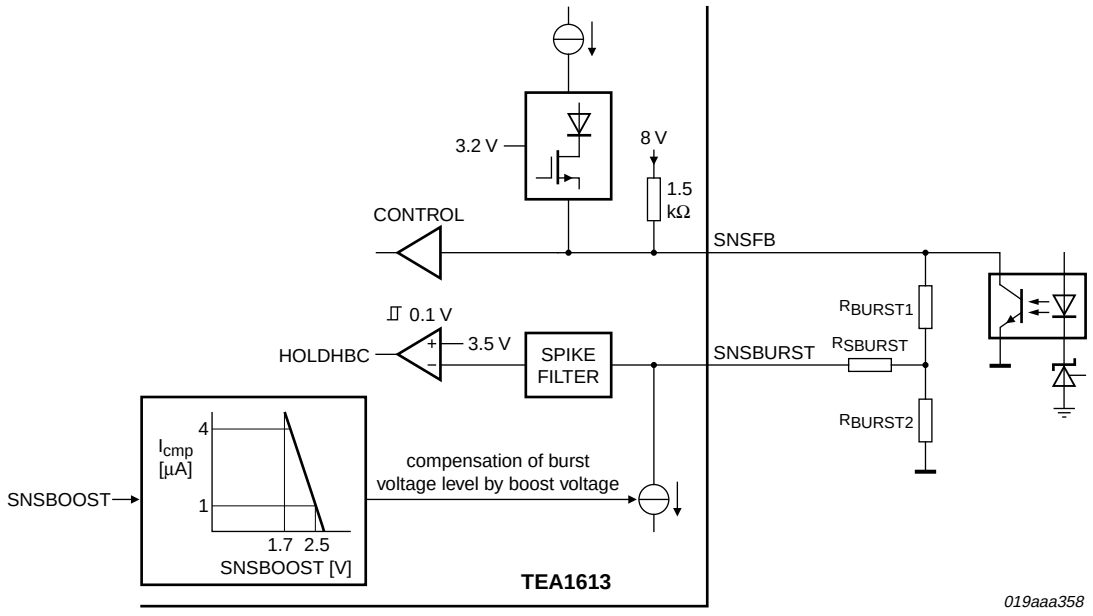



**Fig 41. Designing the burst mode level using a series resistor**

An alternative to the basic circuit construction given in Section 9.5.2 is a construction with an additional series resistance in the connection of SNSBURST ($R_{SBURST}$).

This construction allows lower impedance values to be used for the resistor divider while obtaining the same behavior for boost voltage compensation. The lower impedance has a positive effect on disturbance pickup, benefiting PCB-layout design. The series resistor can be placed directly near the SNSBURST pin, thereby minimizing the high-impedance track.

**Example:**

Nominal SNSBOOST voltage is 2.5 V with $I_{cmp}$ = 1 μA.

The required burst frequency $f_{HB(burst)}$ = 90 kHz which corresponds to SNSFB = 5.4 V.

Impedance target for $R_{BURST1}$ = 22 kΩ and the result should be the same as the example in Section 9.5.2.

**$V_{SNSFB}$ =**

$$3.5\ \text{V} + R_{SBURST} \times I_{cmp} + R_{BURST1} \times I_{cmp} + R_{BURST1} \times \frac{3.5\ \text{V} + R_{SBURST} \times I_{cmp}}{R_{BURST2}} = 5.4\ \text{V} \quad (27)$$

$$3.5\ \text{V} + R_{SBURST} \times 1\ \mu A + 22\ \text{k}\Omega \times 1\ \mu A + \frac{22\ \text{k}\Omega}{R_{BURST2}} \times (3.5\ \text{V} + R_{SBURST} \times 1\ \mu A) = 5.4\ \text{V} \quad (28)$$

Choose the value of $R_{SBURST}$ to obtain the same compensation as in example Section 9.5.2 (indicator gave 72 Hz/V). Because the relationships are complex, the calculation tool can be used to vary the $R_{SBURST}$ value to reach this indicator value.

$R_{SBURST}$ = 46 kΩ

$R_{BURST2}$ = 43 kΩ

Note that for the same compensation (as in the example in Section 9.5.2) the impedance of the network is much lower.

To obtain a better overview of the relationship between SNSBOOST and SNSBURST and the effect on impedance of the resistors, regarding the compensation design, the calculation sheet can used.

### 9.5.4 Other aspects regarding SNSBURST

Aspects that influence choices regarding the design of the SNSBURST circuit with respect to burst mode are:

- Voltage on SNSBOOST at nominal input voltage $V_{BOOST}$
- SNSFB voltage regulation levels in combination with the preset frequency range by RFMAX and CFMIN
- Dynamic behavior of the regulation during burst mode and during normal operation (large load variations)

## 9.6 Output power - operating frequency characteristics

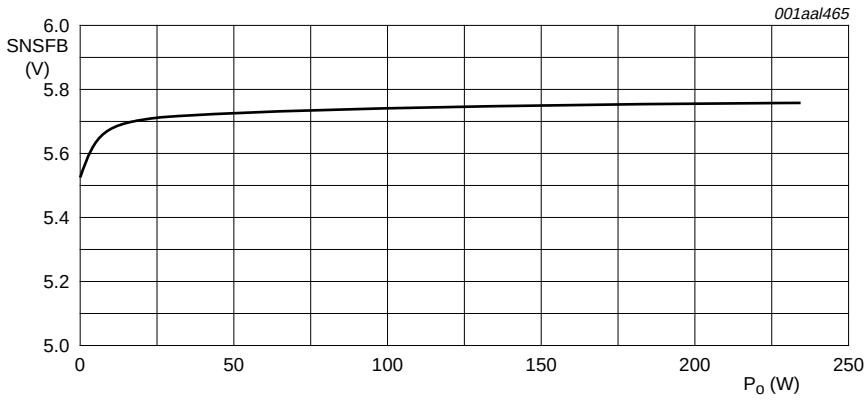



**Fig 42. Typical SNSFB voltage-to-output power characteristic of a converter without burst mode functionality**

As can be concluded from Figure 42, the design choice, for a certain SNSFB voltage at which bursting starts, is critical. With this kind of characteristic there is a risk that, due to spread, the system can either remain in burst mode or never reach burst-mode operation at all. The dimensioning of the LLC can be made more suitable for burst mode. The standard approach is to design the system in such a way that it cannot regulate to no-load, even at the highest frequency. During the lowest loads, the required frequency for regulation must become infinite. Because the characteristic is much steeper for low output power, a voltage level can then be chosen easily to make sure that burst mode is activated at the lowest load and that the remaining load conditions operates in normal mode. The burst mode now enables the system to operate at no-load.

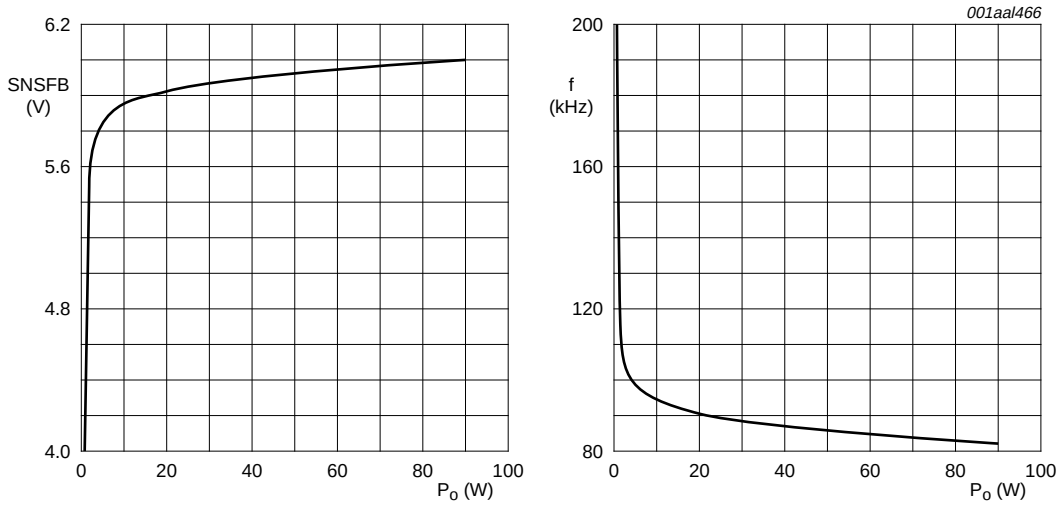



**Fig 43. Example of SNSFB and frequency as functions of output power characteristics (normal mode) adapted for easy implementation of burst mode comparator level detection**

## 9.7 Lower SUPHS in burst

During idle time SUPHS is not charged.

During normal operation, each time the half-bridge node HB is switched to ground level, the SUPHS capacitor is charged by the bootstrap function of the external diode between SUPHS and SUPREG. In burst mode there are periods of non-switching, and therefore no charging of SUPHS. During this time, the circuit supplied by SUPHS slowly discharges the supply voltage capacitor. At the moment a new burst starts, the SUPHS voltage is lower than during normal operation. During the first switching cycles, the SUPHS is re-charged to its normal level. It is important that, during these first re-charge cycles, SUPREG does not drop below the protection level of 10.3 V.

## 9.8 Audible noise

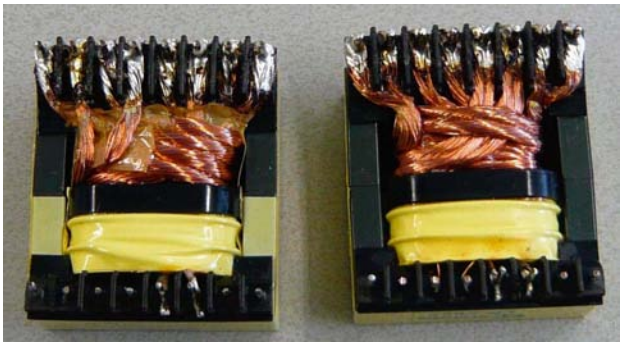
Because the burst mode is normally used when the output power is low, the converted energy does not contribute much to generate audible noise. The magnetization current however is still present during low loads and is the dominant energy during burst mode. Switching on and off the converter sequences continuously at a certain speed and duration can lead to audible noise. The main mechanism for producing noise is the interruption of magnetization current sequences leading to a mechanical force. This is especially the case on the core of the resonant transformer which starts acting as a loudspeaker.

When burst mode is applied at higher output power conditions, the converted energy also contributes and leads to an increased chance of audible noise.

### 9.8.1 Measurements in the resonant transformer construction

To prevent problems with audible noise under specific conditions, it is necessary to adapt the mechanical transformer construction to allow for this.

One possibility is to adhere the core parts to each other using a material with damping (vibration absorbing) properties. A combination can be made with the air gap construction. Other vibration damping measures can also help when audible noise is a critical issue for a product.



001aal467

(1) Left-hand transformer with glue to reduce audible noise

(2) Right-hand transformer has standard construction

**Fig 44. Transformer construction**

### 9.8.2 Burst power dependent noise level

The amount of audible noise is strongly related to the amount of energy in each burst. At low output power, the amount of energy is mainly determined by the magnetization current of the resonant converter. The amount of transferred energy is low. To avoid problems with audible noise, the burst mode should only be used at low power (a few watts output power). When the transition level between normal mode and burst mode is chosen at a higher output power, the level of audible noise is larger.

**Overshoot on feedback voltage**

When the output load is increased, the system reverts to normal operation. The transition from burst mode to normal mode is based on the feedback voltage. In certain burst conditions the feedback voltage can overshoot, keeping the system in burst mode at higher output power levels than intended. As the power level in this situation is larger, the amount of noise is also larger.

## 9.9 PFC converter and resonant converter simultaneous bursting

When in burst mode, it is beneficial to stop the PFC operation during the time that the resonant converter is not switching. In most cases this saves extra energy consumption by reducing switching losses from the PFC converter.

To control the external PFC, the signal from pin SNSOUT/PFCON can be used.

The behavior of the total system (PFC and resonant) in burst mode may differ from the situation when only the resonant converter operates in burst mode. Although this may result in good performance, there are a number of interactions.

### 9.9.1 PFC start delay

Depending on the PFC control system there is a certain delay in starting conversion in burst mode. This delay is the time between SNSOUT/PFCON becoming high and the PFC starting to switch. This results in a shorter power conversion time for the PFC-converter compared to the resonant converter.

### 9.9.2 PFC output voltage variations

When bursting the PFC converter, the resonant control system determines the timing. This may result in a situation that the PFC cannot maintain a constant output voltage. The time during which the PFC can convert power is limited by the HBC operation and can be too short. The result is a lower output voltage or a varying output voltage. This also has consequences for the resonant converter as its input voltage is not the same. The working conditions change towards a new balance.

The resonant converter must be able to remain operational during these conditions.

It is important to check that the resonant controller has not been stopped because the input voltage provided by SNSBOOST is too low. This may cause an unacceptable voltage decrease in the output of the resonant converter.

### 9.9.3 Switching between burst and normal operation

Interaction between the PFC converter and resonant converter in the burst mode can lead to a situation whereby the system alternates between burst mode and normal mode for certain output power conditions.

### 9.9.4 Audible noise during mode transition

Because of the above mentioned interactions, a stable situation can occur during the following operating modes, alternating in time:

- Resonant burst with short burst time without PFC burst (time too short to start)
- Resonant burst with long burst time and PFC burst
- Normal operation for resonant and PFC bursts

Transitions between modes and variations within a certain mode have a corresponding effect on audible noise.

## 9.10 Design guidelines for burst mode operation

Design for a stable PFC (nominal) output voltage during burst mode. When the PFC is operating in simultaneous burst mode, the issues mentioned in Section 9.9 are important.

Best efficiency is achieved when the number of cycles for each burst is kept to a minimum (only a few cycles).

Best efficiency is achieved by resistively tuning the comparator circuit to preset the SNSFB burst level and hysteresis.

System and component tolerances play a significant role in performance variations during production.

The regulation feedback loop can be optimized for normal mode and any additional filtering can be done in the comparator circuit see Section 9.5.3. However, this should be used moderately so that control of the situation can be maintained during burst mode operation.

## 9.11 Enable/disable burst mode

In microcontroller operated applications such as TV, a clear separation is made between normal operation and standby operation. To avoid the resonant converter going into burst during short periods of low load during normal operation, an enable/disable function can be added. This can be implemented by an extra enable/disable switch function in the comparator circuit.

## 9.12 Hold HBC and PFC

By switching the SNSBURST input below 3.5 V, the switching of HBC and PFC (by SNSOUT/PFCON) can be stopped immediately. Releasing the pin voltage resumes the operation (without soft-start) on the regulation point of that moment. For certain external protection procedures, this hold-function can be useful.

## 9.13 Unused burst mode

By connecting SNSBURST to a fixed voltage higher than 3.5 V (but below the limiting value of +12 V), the burst mode function is not activated. For example, SNSBURST can be connected to SUPREG.

# 10. Protection functions

Most protection functions are discussed in the sections of the systems of which they are a part. In the overview Table 3, links to the corresponding places in this document are given. In the following paragraphs the remaining, more independent, protection functions are discussed.

## 10.1 Protection overview

**Table 3. Overview of protection functions with links**

| Part | Symbol | Protection | Action | Link |
|---|---|---|---|---|
| IC | UVP-SUPIC | undervoltage protection | SUPIC IC disable | 6.2.2 |
| IC | UVP-SUPREG | undervoltage protection SUPREG | IC disable | 6.5 |
| IC | UVP supplies | undervoltage protection supplies | IC disable and reset | 6.2.2 |
| IC | SPC-SUPIC | short-circuit protection SUPIC | low HV start-up current | 6.2.2 |
| IC | OVP output | overvoltage protection output | IC shutdown | 10.3.1 |
| IC | UVP output | undervoltage protection output | IC restart after protection time | 10.3.2 |
| IC | OTP | overtemperature protection | IC disable | 10.2.1 |
| HBC | UVP-boost | undervoltage protection boost | HBC disable | 8.1 |
| HBC | OLP-HBC | open-loop protection HBC | IC restart after protection time | 8.5.1 |
| HBC | HFP-HBC | high frequency protection HBC | IC restart after protection time | 8.4.4 |
| HBC | OCR-HBC | overcurrent regulation HBC | HBC increase frequency<br>IC restart after protection time | 8.7.1 |
| HBC | OCP-HBC | overcurrent protection HBC | HBC step to maximum frequency | 8.7.2 |
| HBC | CMR | capacitive mode regulation | HBC increase frequency | 8.3.2 |
| HBC | ANO | adaptive non-overlap | HBC prevent hazardous switching | 8.3.1 |

## 10.2 IC protection

### 10.2.1 OverTemperature Protection (OTP)

The TEA1613T contains an accurate internal OverTemperature Protection (OTP). When the junction temperature exceeds the overtemperature level of 140 °C, the IC goes to the thermal hold state. The thermal hold state is left as soon as the temperature has dropped by 10 °C.

The circuit resumes operation with a complete restart including a soft-start.

### 10.2.2 Latched protection

Only an OVP detection on SNSOUT/PFCON, leads to a latched shutdown protection state. To initiate this, the voltage on SNSOUT/PFCON must exceed 3.5 V.

**Resetting a latched protection shutdown state**

When a latched protection shutdown state has occurred this state is reset by one of the following actions:

- SUPIC drops below 7 V and SUPHV is lower than 7 V
- SSHBC/EN is pulled below 2.2 V (enable level)

A possible reset by external control (for example microcontroller) is available using the SSHBC/EN function.

## 10.3 SNSOUT/PFCON protection

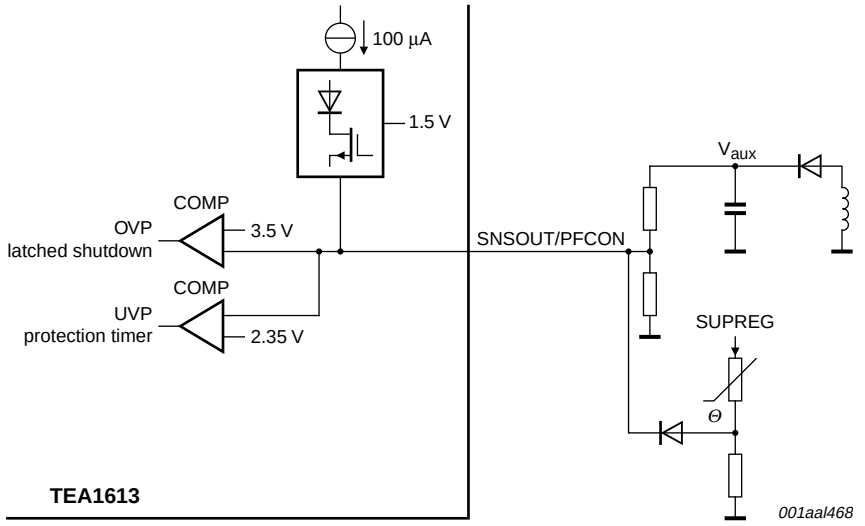



**Fig 45. SNSOUT protection**

### 10.3.1 OverVoltage Protection (OVP) output

The TEA1613T has overvoltage protection intended for monitoring the HBC output voltage. It is one of the functions that is combined on the SNSOUT/PFCON pin.

#### 10.3.1.1 Auxiliary winding

When dealing with a mains insulated converter, the HBC output voltage can be measured via the auxiliary winding of the resonant transformer. To accurately measure the secondary voltage of the primary circuit auxiliary winding, a special transformer construction is needed.

To facilitate correct working, it is important that this winding has a good coupling with the secondary winding(s) and a minimum coupling with the primary winding. In this way a good representation is obtained of the output voltage situation. For more details refer to Section 6.3.3.1 and Figure 6.

To meet the mains insulation requirements, triple insulated wire can be used.

#### 10.3.1.2 Principle of operation

The voltage is sensed at the SNSOUT/PFCON pin via an external rectifier and resistive divider. Overvoltage is detected when the SNSOUT/PFCON voltage exceeds 3.5 V. After detecting OVP the TEA1613T goes to the latched protection shutdown state.

#### 10.3.1.3 Connecting external measurement circuits

When latched protection is needed for other detection circuits, it can be added on SNSOUT/PFCON by means of a series diode. For example: external overtemperature protection.

### 10.3.2 UnderVoltage Protection (UVP) output

The TEA1613T has undervoltage protection intended for monitoring the HBC output voltage. It is one of the functions that is combined on the SNSOUT/PFCON pin.

#### 10.3.2.1 Auxiliary winding

When dealing with a mains insulated converter, the HBC output voltage can be measured via the auxiliary winding of the resonant transformer. To accurately measure the secondary voltage of the primary circuit auxiliary winding, a special transformer construction is needed.

To facilitate correct working, it is important that this winding has a good coupling with the secondary winding(s) and a minimum coupling with the primary winding. This is to obtain a good representation of the output voltage situation. For more details refer to Section 6.3.3.1 and Figure 6.

To meet the mains insulation requirements, triple insulated wire can be used.

#### 10.3.2.2 Principle of operation

The voltage is sensed at the SNSOUT/PFCON pin via an external rectifier and resistor divider. Undervoltage is detected when the SNSOUT/PFCON voltage drops below 2.35 V. When detecting UVP the TEA1613T starts the protection timer by charging it with 100 μA.

When the undervoltage state remains until the timer reaches the protection level, the controller stops and is then re-started by the restart timer.

At start-up, the SNSOUT/PFCON voltage normally starts at a level lower than 2.35 V. To prevent undesired protection during start-up, the timer setting must allow sufficient time for start-up to charge the SNSOUT/PFCON voltage to a value above 2.35 V.

In applications where the TEA1613T is supplied from an auxiliary winding (to SUPIC), the SUPIC monitoring can also activate a protection when an error condition results in a drop of the output voltage (see Section 6.2.2).

#### 10.3.2.3 Connecting external measurement circuits

When re-start protection is required for another detection circuit, it can be added to SNSOUT/PFCON by means of a series diode. An example of external temperature protection is given in Figure 45.

### 10.3.3 OVP and UVP combinations

#### 10.3.3.1 Circuit configurations

The following list contains examples of configurations for which certain functionality on the SNSOUT/PFCON pin is disabled.

- OVP functional and UVP disabled (refer to Section 10.3.3.2)
- UVP functional and OVP disabled (refer to Section 10.3.3.3)
- Both OVP and UVP disabled (refer to Section 10.3.3.4)

Note that in the examples given in the referenced sections, the PFCON signal can still be generated for burst mode operation.

#### 10.3.3.2 OVP functionality and UVP disabled

In some applications it may be required to prevent the activation of the UVP on SNSOUT/PFCON. To achieve this, it is necessary to disable UVP. This can be realized by adding a circuit that prevents the voltage on SNSOUT from dropping below 2.35 V.

**Practical example**

The voltage on SNSOUT/PFCON can be prevented from dropping below a preset voltage by externally adding a low impedance resistor divider, with a fixed voltage, and connecting it to SNSOUT/PFCON via a diode. This simple circuit is not very accurate but it does provide the basic capability to disable the UVP function of SNSOUT/PFCON. Note that higher voltages on SNSOUT/PFCON are blocked by the diode so that the OVP is still functional.

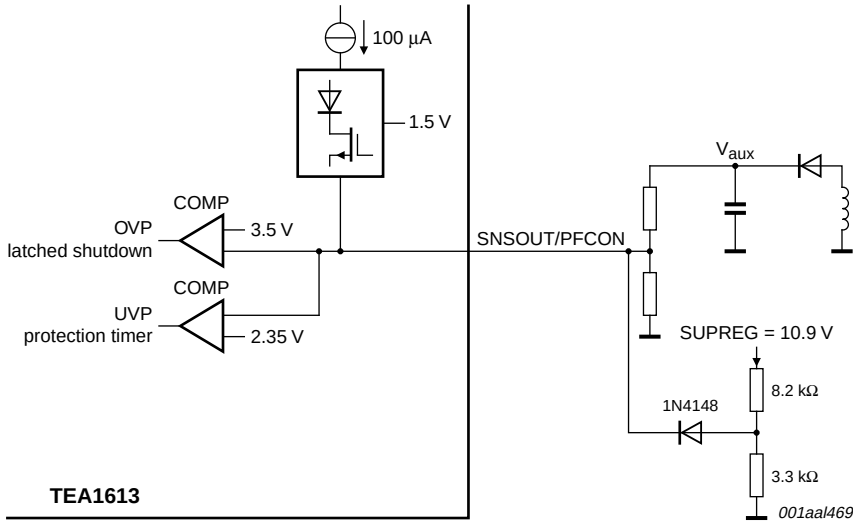



**Fig 46. Example of disabling the UVP function of SNSOUT/PFCON**

#### 10.3.3.3 UVP functionality and OVP disabled

In some applications it may be required to prevent the activation of the OVP on SNSOUT/PFCON. To achieve this, it is necessary to disable OVP. This can be realized by adding a circuit that prevents the voltage on SNSOUT/PFCON from exceeding 3.5 V.

**Practical example**

The voltage on SNSOUT/PFCON can be prevented from exceeding the preset voltage by externally adding a low impedance resistor divider, with a fixed voltage, and connecting it to SNSOUT/PFCON via a diode denoted by (1) in Figure 47. This simple circuit is not very accurate but it does provide the basic capability to disable the OVP function of SNSOUT/PFCON. Note that lower voltages on SNSOUT/PFCON are blocked by the diode so that the UVP is still functional.

Another possibility is to add a Zener diode function on SNSOUT/PFCON to limit the voltage on this pin denoted by (2) in Figure 47.

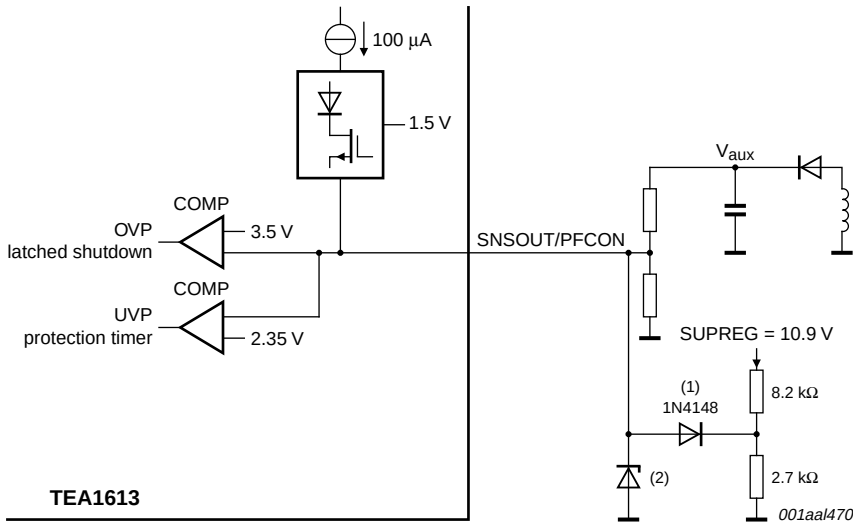



**Fig 47. Example of disabling the OVP function of SNSOUT/PFCON**

### 10.3.3.4 Both OVP and UVP disabled

When neither OVP or UVP functionality is required, a fixed voltage between 2.35 V and 3.5 V can be applied to SNSOUT. This can be obtained from a resistor divider that is referenced to the SUPREG.

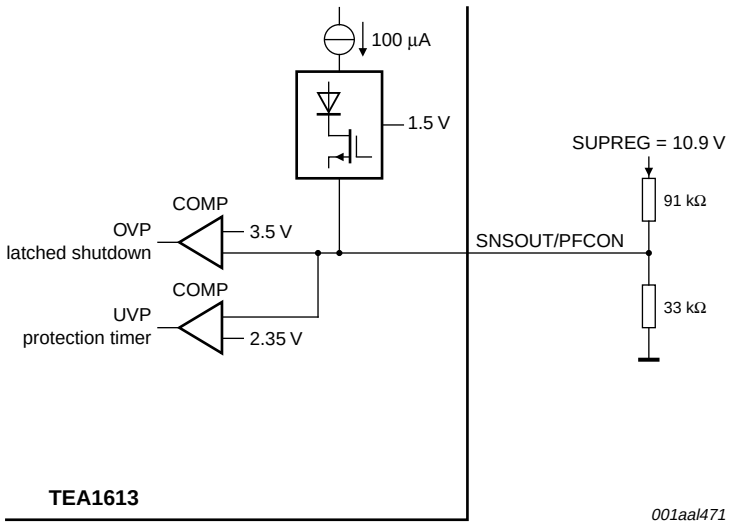



**Fig 48. Example of disabling both the UVP and the OVP functions of SNSOUT/PFCON**

### 10.3.3.5 UVP during burst mode operation

When the system is in burst mode operation, the undervoltage protection is not active while switching is off. This is to prevent incorrect protection during this interval. As soon as switching is resumed, the UVP protection becomes active again.

## 10.4 Protection timer

The TEA1613T has a programmable timer that is used for the timing of several forms of protection. The timer is basically used in two ways:

- As a protection timer - the time that an error exists before the system stops operation
- As a restart timer - the time between stopping and restarting operation

The values for both types of timer can be independently preset by an external resistor and capacitor connected to RCPROT.

### 10.4.1 Block diagram of the RCPROT function

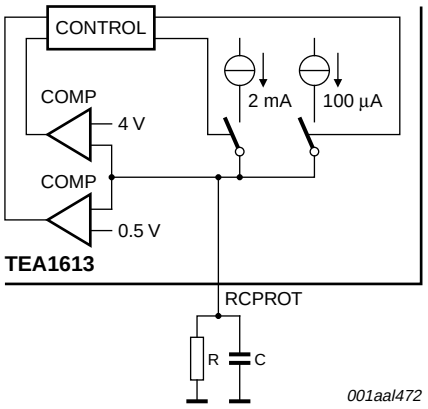



**Fig 49. Block diagram of the RCPROT function**

#### 10.4.1.1 RCPROT working as protection timer

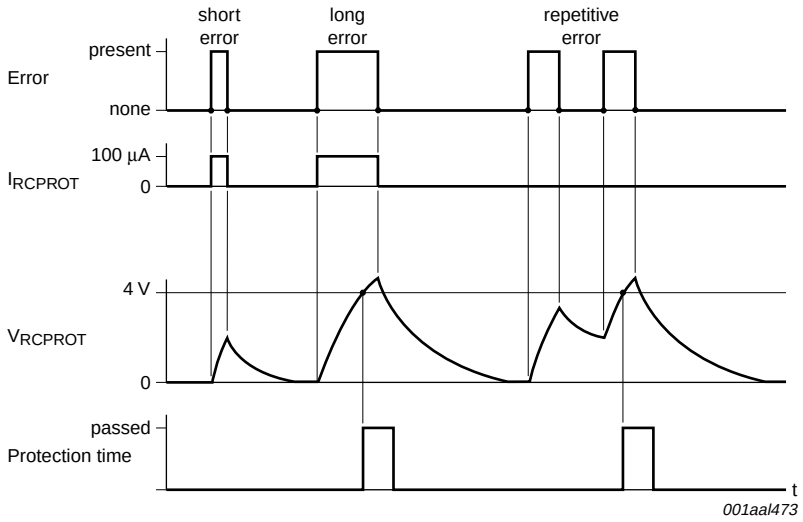



**Fig 50. RCPROT protection timer operation**

Figure 50 demonstrates the operation of the protection timer. When an error condition occurs, a fixed current of 100 µA flows from the RCPROT pin and charges the external capacitor. Due to the external resistor, the voltage rises exponentially. The protection time

is passed when the upper switching level of 4 V has been reached. At that moment, the appropriate protective action is executed, the current source is stopped and RCPROT is discharged by the external resistor.

In the case that the error condition ends before 4 V has been reached, the current source is stopped and the pin discharges through the external resistor and no further action is taken.

If the error condition is permanent, the system fluctuates between stopping (RCPROT = 4 V) and restarting (RCPROT = 0.5 V). This is sometimes referred to as a hiccup mode.

The protection timer is activated by one of the following:

- overcurrent regulation SNSCURHBC
- high frequency protection RFMAX
- open loop protection SNSFB
- undervoltage protection SNSOUT/PFCON

Protection can be forcibly activated (including restart) by increasing the RCPROT voltage to above 4 V (but not higher than +12 V) using an external circuit.

### 10.4.2 RCPROT working as a restart timer

During certain error conditions, it may be desirable to temporarily disable the IC. This is especially useful when an error can over-heat components. A temporary disable allows power supply components to cool down, after which the IC must automatically restart. The time to restart is determined by the restart timer.

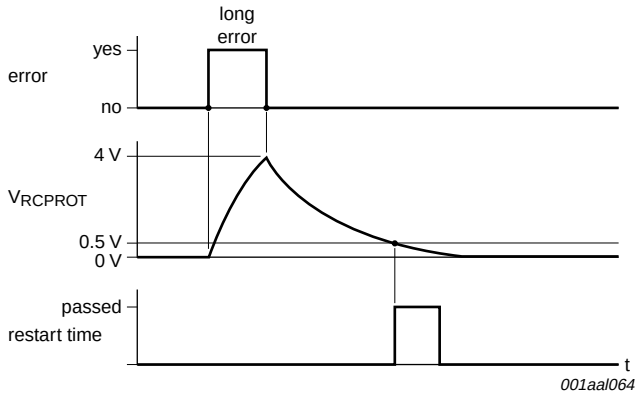



**Fig 51. RCPROT operating as a restart timer**

Normally, the capacitor is discharged to 0 V. When an error occurs, $C_{prot}$ is charged and it operates as a protection timer until it reaches the upper switching level of 4 V. After this, the RCPROT pin becomes high ohmic and the external resistor discharges the external capacitor. The restart time is exceeded when the lower switching level of 0.5 V is reached. At that moment, the IC is restarted and the RCPROT pin is further discharged.

### 10.4.3 Dimensioning the timer function

The required restart time $t_{restart}$ determines the time constant $t_{RCPROT}$ made by the values of R and C.

$$t_{RCPROT} = \frac{-t_{restart}}{1n\left\langle \frac{V_{low(RCPROT)}}{V_{high(RCPROT)}} \right\rangle} = \frac{-t_{restart}}{1n\left\langle \frac{0.5}{4} \right\rangle} = 0.48 \times t_{restart} \quad (29)$$

With this time constant and the required protection time $t_{protection}$, the value of R and C can be calculated as follows:

$$R = \frac{V_{high(RCPROT)}}{I_{slow(RCPROT)} \times \left\langle 1 - e^{-\frac{t_{protection}}{t_{RCPROT}}} \right\rangle} = \frac{4\ \text{V}}{100\ \mu A \times \left\langle 1 - e^{-\frac{t_{protection}}{t_{RCPROT}}} \right\rangle} \quad (30)$$

$$C = \frac{t_{RCPROT}}{R} \quad (31)$$

**Example**:

$t_{restart}$ = 500 ms;

$t_{protection}$ = 30 ms;

$t_{RCPROT}$ = 240 ms;

R = 341 kΩ;

C = 705 nF.

# 11. Miscellaneous advice and tips

## 11.1 PCB layout

### 11.1.1 Grounding

SGND + PGND **must** be connected directly under the IC (in ground plane if possible) to avoid false signal detection by driver current disturbance (see Figure 54).

A star grounding construction provides the lowest risk of mutual converter disturbance or signal detection disturbance. In this system, the central star point can be chosen at the $V_{BOOST}$ capacitor ground.

Large currents should be avoided on grounding tracks that are intended for signal measurement.

### 11.1.2 Large current loops

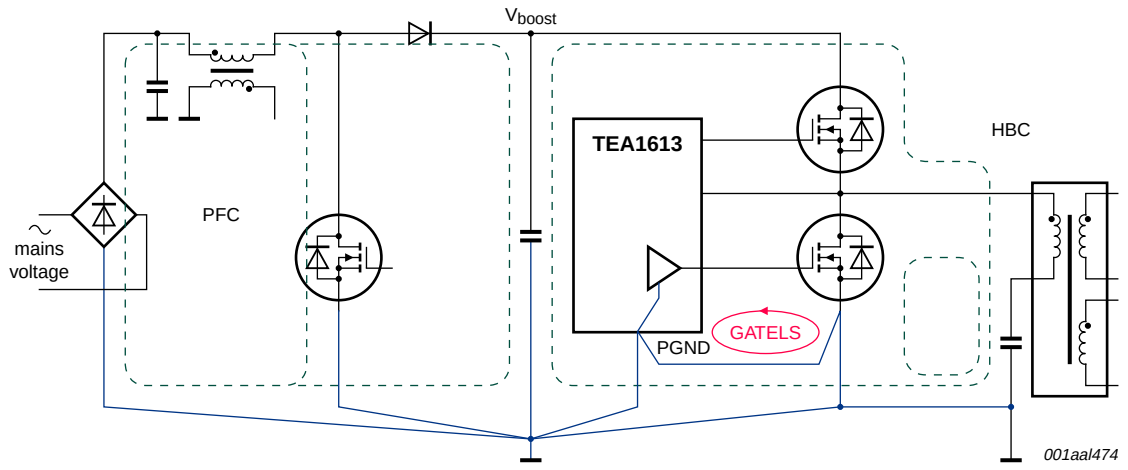



**Fig 52. Ground structure and current loops in an application with PFC**

### 11.1.3 Ground layout example

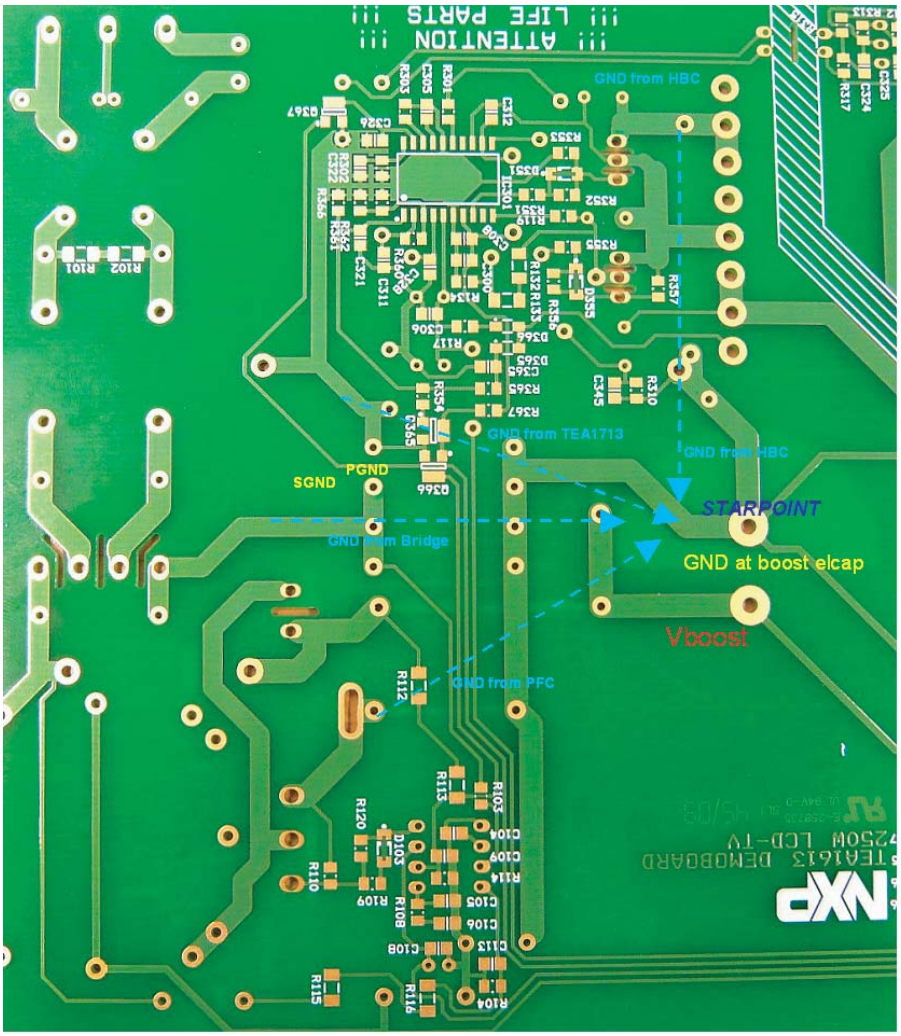



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**Fig 53. Ground layout example with star point at the boost capacitor**

### 11.1.4 Miscellaneous

**Connecting SNSCURHBC pin 15**

Place a series resistor in the SNSCURHBC connection as close as possible to pin 15. This is important for avoiding disturbance pickup. Also avoid capacitive coupling between the connection to pin 15 and the HB track (to pin 13) that contains high dV/dt signals.

**CFMIN pin 17 (and RFMAX pin 18)**

Connect the oscillator capacitor on CFMIN from pin 17 to SGND pin 16 with short tracks to prevent pickup of disturbances by an external field. Although less critical, a similar construction can be used for RFMAX.

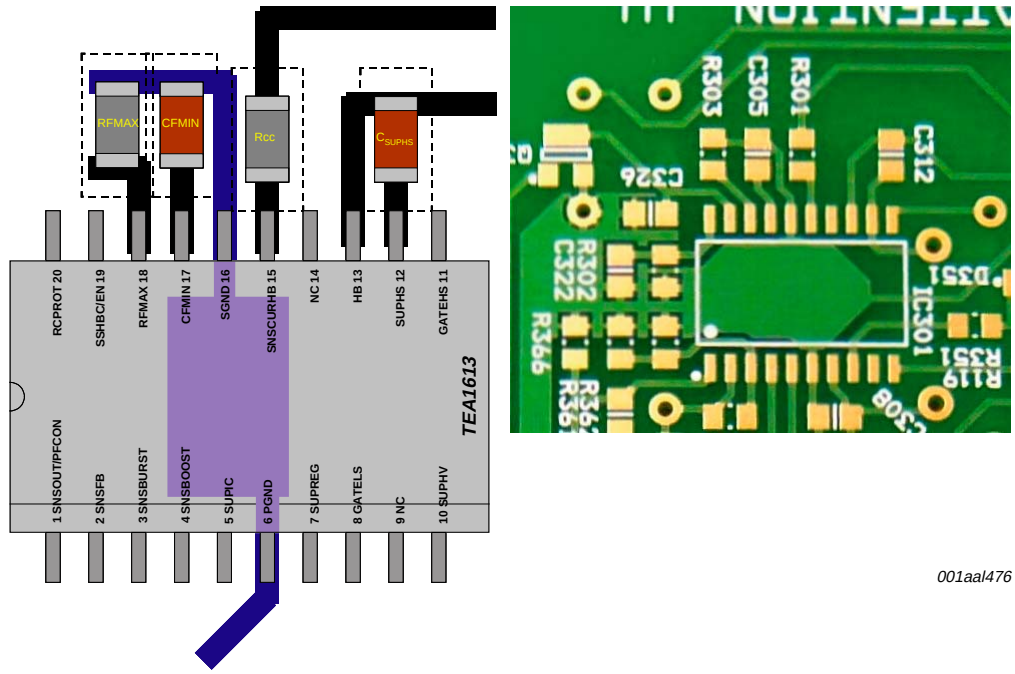


**Fig 54. PCB layout connecting SGND, PGND, CFMIN, RFMAX and SNSCURHBC**

**SNSBURST (pin 3)**

If a high-impedance value is chosen for the resistor divider on SNSBURST, the connecting tracks of the resistors should be kept short to avoid disturbance (refer to Section 9.5.2 and Section 9.5.3).

## 11.2 Starting/debugging partial circuits

When starting a newly built application for the first time or when an error is observed during operation, it is possible to activate parts of the circuit step by step. This enables errors to be located more easily and an evaluation to be performed under conditions that restrict influences from other circuit parts.

The following list provides a step-by-step sequence for debugging:

1. IC only, with protection disabled
2. HBC with protection disabled and variable DC input voltage
3. HBC with protection enabled

The best approach is to check the HBC converter first with external supplies for SUPIC and $V_{BOOST}$.

### 11.2.1 HBC only

A proposal for the setup (temporary additions to the existing application to force operation) and the sequence for disabling/enabling the different functions is given in Figure 55. A moderate (current) load can be applied to the converters output to ascertain the correct functioning.

**Start:**

1. 25 V external supply on SUPIC by series diode
2. 3 V on SNSBOOST to enable
3. RCPROT to ground to disable protection timer
4. SNSCURHBC to ground to disable OCP
   - step A: increase the HBC input voltage ($V_{BOOST}$)
   - step B: enable SNSCURHBC
   - step C: enable RCPROT

Be aware that a latching, overvoltage detection on SNSOUT (>3.5 V), can still prevent operation.

CFMIN, GATELS, GATEHS and HB can be monitored to continuously assess the functioning of the converter/controller.

**Practical tip:** When an external PFC function is disabled, $V_{BOOST}$ can often be applied by simply applying a DC or AC voltage to the mains input connections.

Check the regulation by increasing the input voltage $V_{BOOST}$ for the following situations:

1. Initially at $V_{BOOST}$ = 0 V, the running frequency is low with a short on-time and a long off-time. This is due to the HB detection not working properly at low voltage and the internal slope detection (HB) not detecting a proper (fast) slope.
2. Increasing the value of $V_{BOOST}$, at a certain input voltage the HB detection works correctly and the frequency to drive maximum power, is minimal. If the HB slope remains slow, the output current is probably low. Increasing the output current probably results in proper HB switching.
3. When the $V_{BOOST}$ input voltage has reached a level closer to the nominal working voltage, the correct output voltage is reached (depending on the output load), and regulation starts working. This results in increasing the frequency with increasing the input voltage until the nominal working voltage of $V_{BOOST}$ is set.
4. When the basic functioning of the HBC is working well including SNSFB regulation, protections can be added one by one. Proper functioning or a need for change can be evaluated.
5. When a self-supplying application is used, the external supply voltage can be removed as soon as the system works well at nominal $V_{BOOST}$ voltage. The system should now be able to start with the internal high voltage start-up supply and an auxiliary winding can take over the SUPIC supply.

**Remark:** If, during debugging or starting, a protection has been activated, it may be necessary to switch the SUPIC supply off and on to reset a latched protection state.

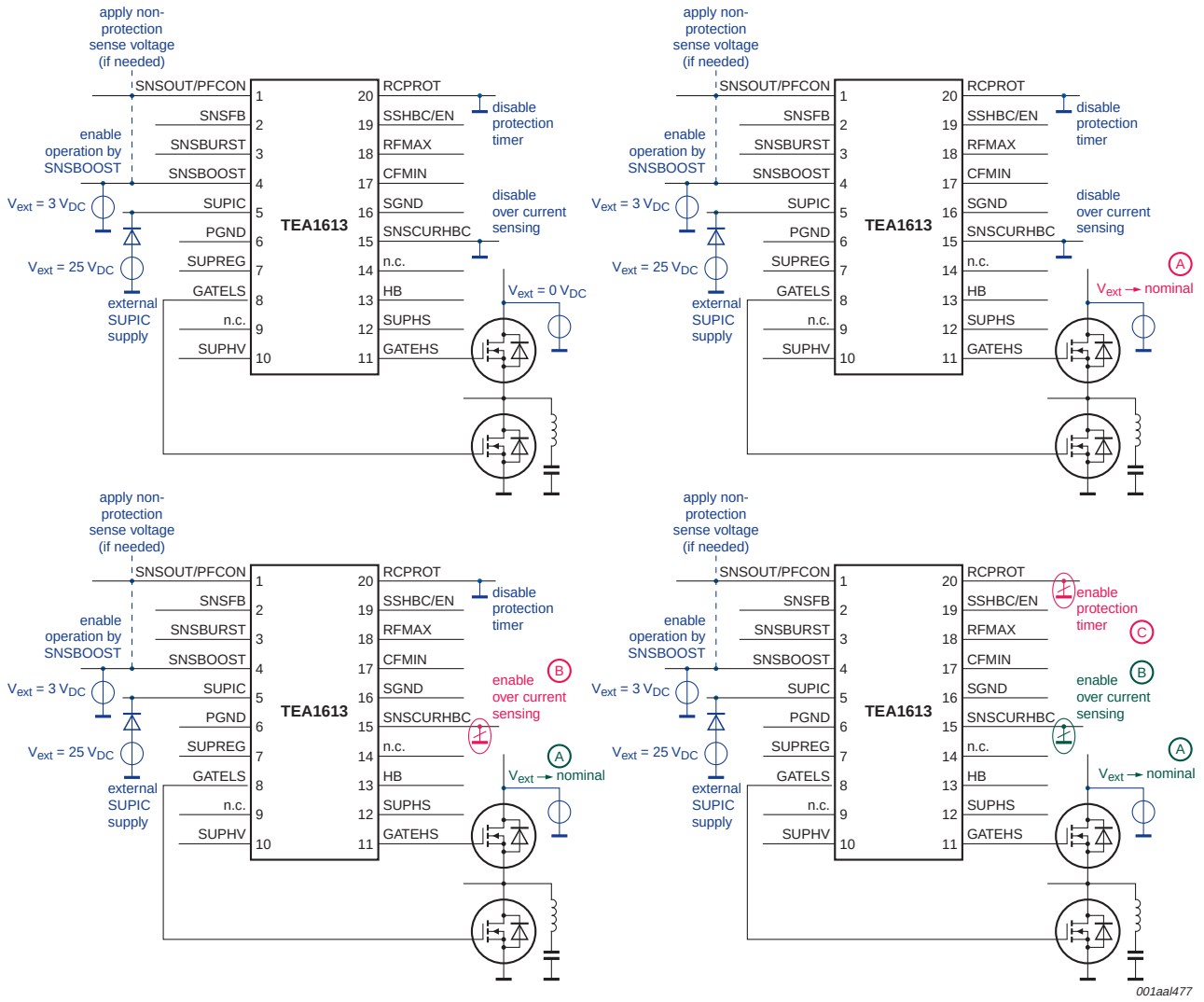


**Fig 55. Start-up and debugging step-by-step**

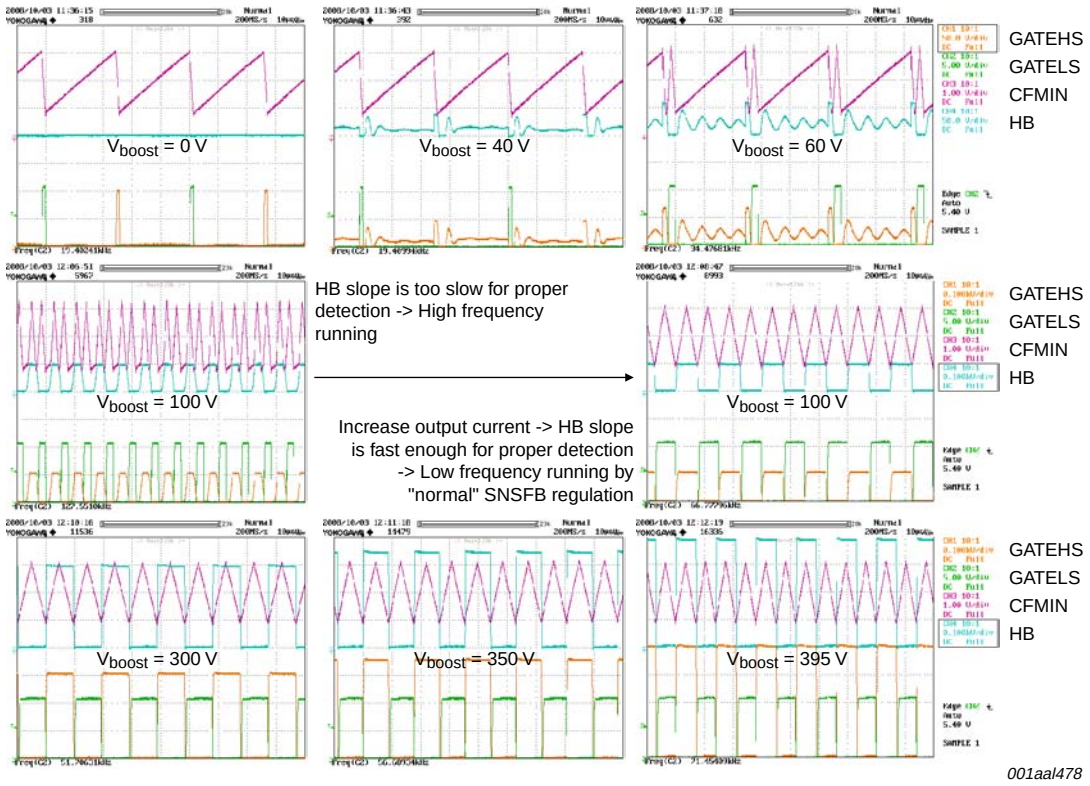


**Fig 56. Typical signals during a separate HBC start-up for an increase in $V_{boost}$**

The following list provides an association between pins and the protection states for which they are being monitored:

- **SSHBC/EN:** When the TEA1613T lowers the voltage to this pin, it indicates a protection with correction to high frequency. This is often caused by OCR/OCP.
- **RFMAX:** The voltage level on RFMAX indicates the oscillator frequency, which may cause a high frequency protection when the voltage level is higher than 1.8 V.
- **CFMIN:** No proper detection of HB-slope or a possible capacitive mode detection can be observed by a (partially) slow oscillator signal.
- **PGND and SGND:** If the TEA1613T detects HB operation while there is zero input voltage, it indicates that the connection between these pins, directly at the IC, is not present. Gate currents lead to false HB slope detection.
- **SNSCURHBC:** Any disturbances on this pin (voltage spikes) can lead to an increase of frequency while the original measurement voltage/signal is ok.
- **SNSOUT/PFCON:** The voltage on this pin should be between 2.35 V and 3.5 V for normal operation. To avoid protection, a voltage can be forced on it. But often it is related (by a resistor divider) to the SUPIC and is correct when SUPIC is supplied externally.
- **RCPROT:** Several protection functions can charge the timer.

# 12. Application examples and topologies

## 12.1 Example of IC evaluation and test setup

An example of a test/evaluation setup is provided in Figure 57. This setup can be used to:

- check if an IC is still functional (not defective)
- evaluate specific IC function(s) or pin properties with limited interference from the total system

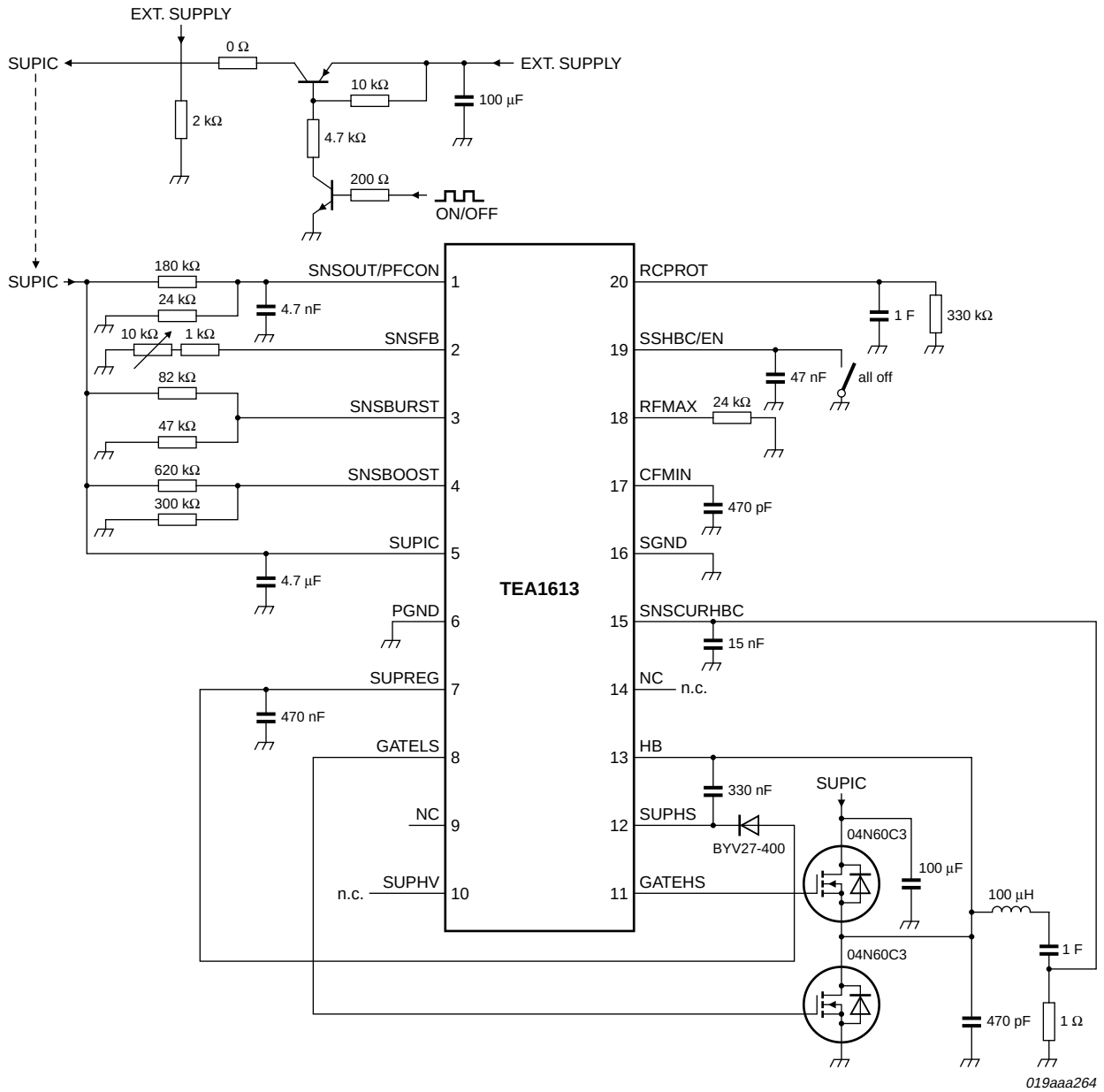


**Fig 57. Example of a basic IC test setup on a single low voltage supply (24 V)**

## 12.2 Example of a 250 W LCD-TV application

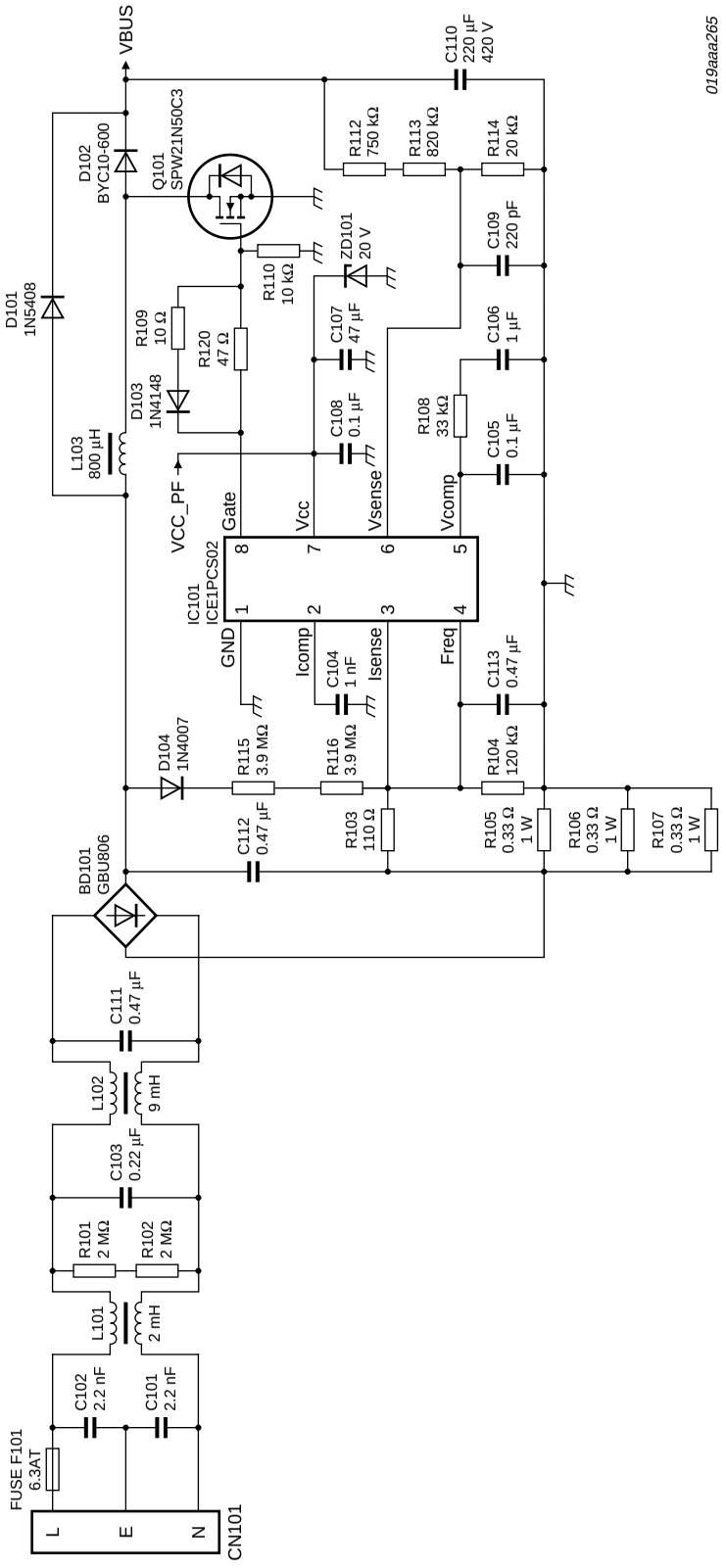


Fig 58. Example of a 250 W LCD-TV application (part 1)

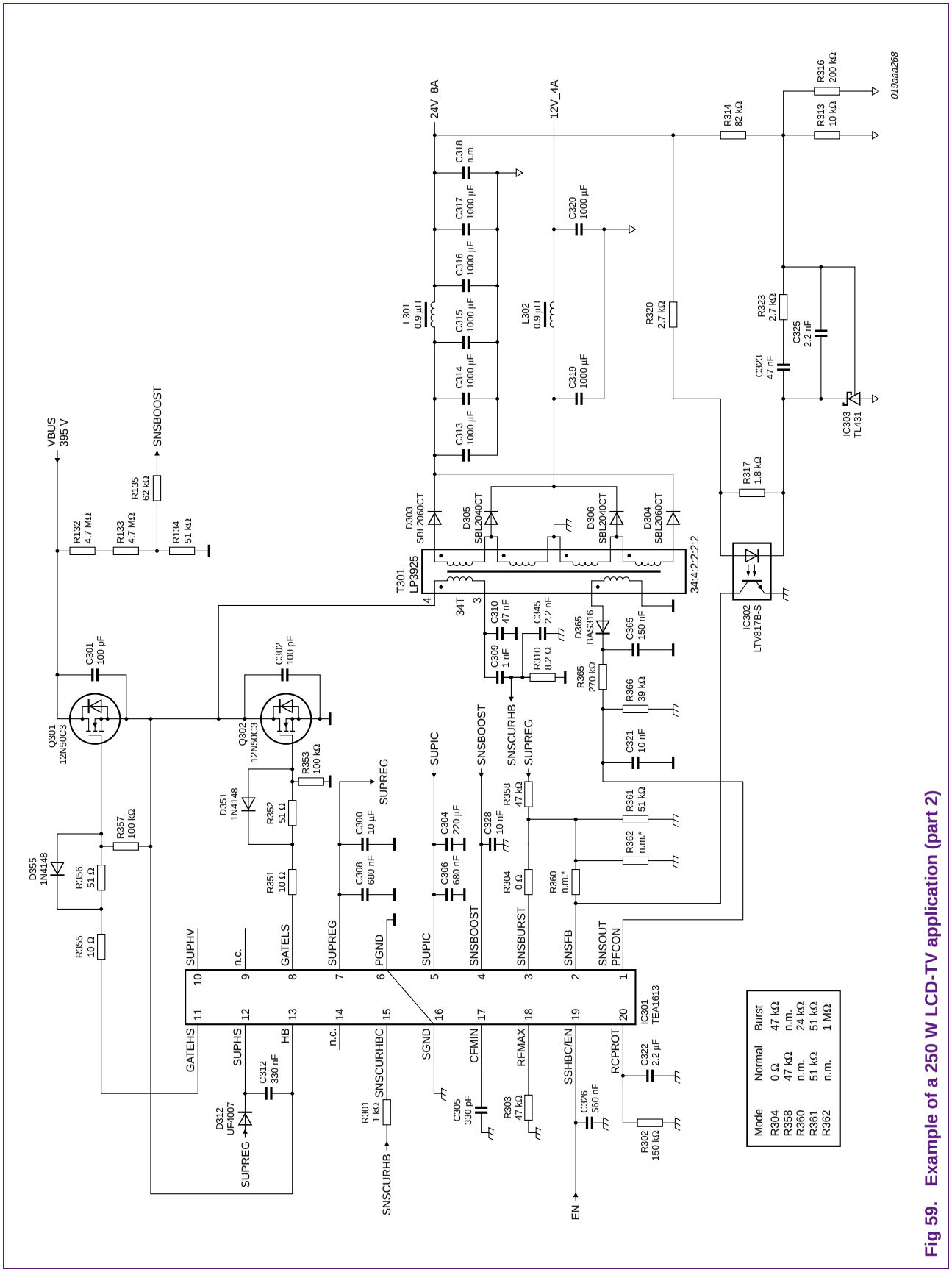


Fig 59. Example of a 250 W LCD-TV application (part 2)

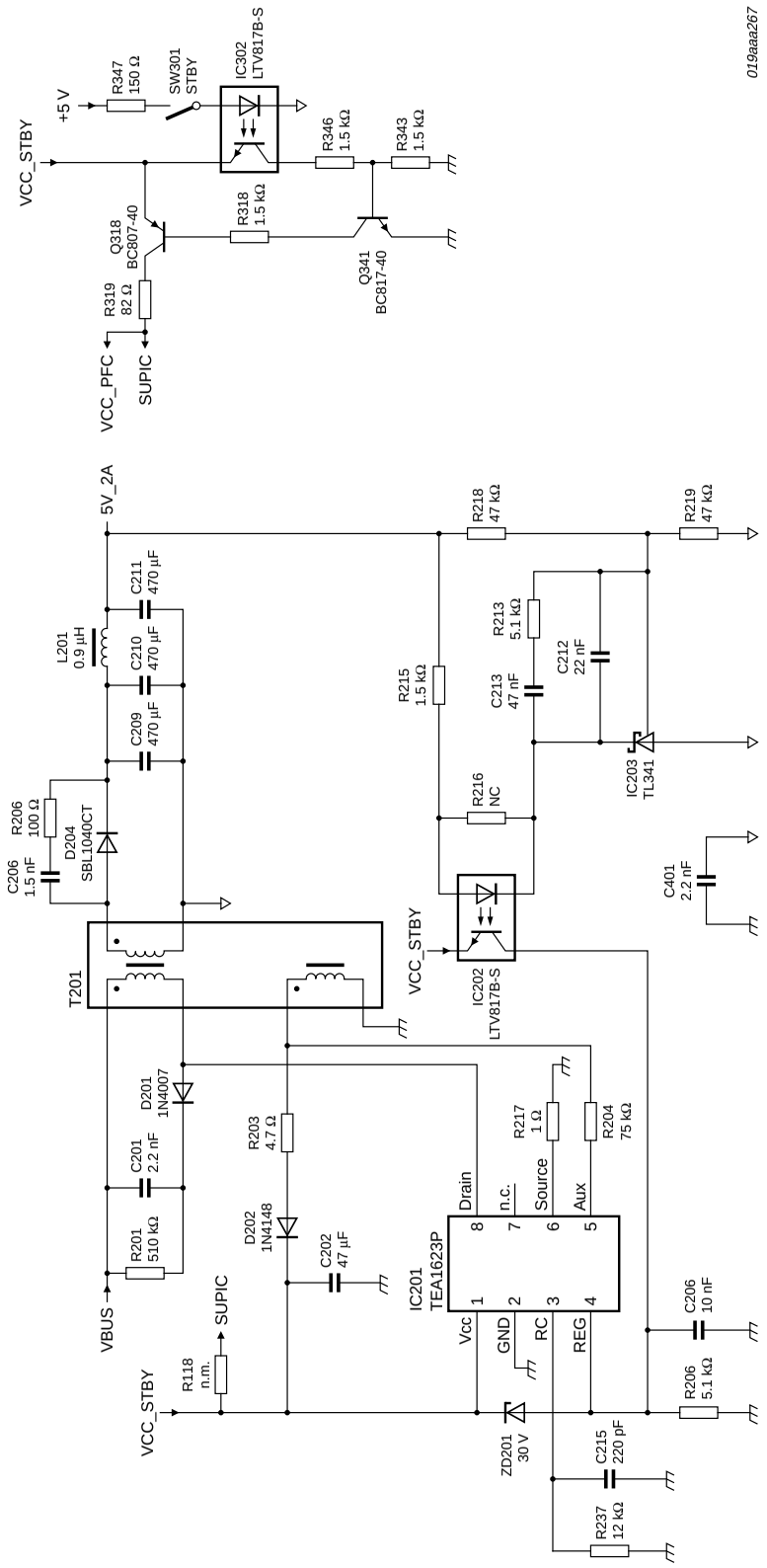


Fig 60. Example of a 250 W LCD-TV application (part 3)

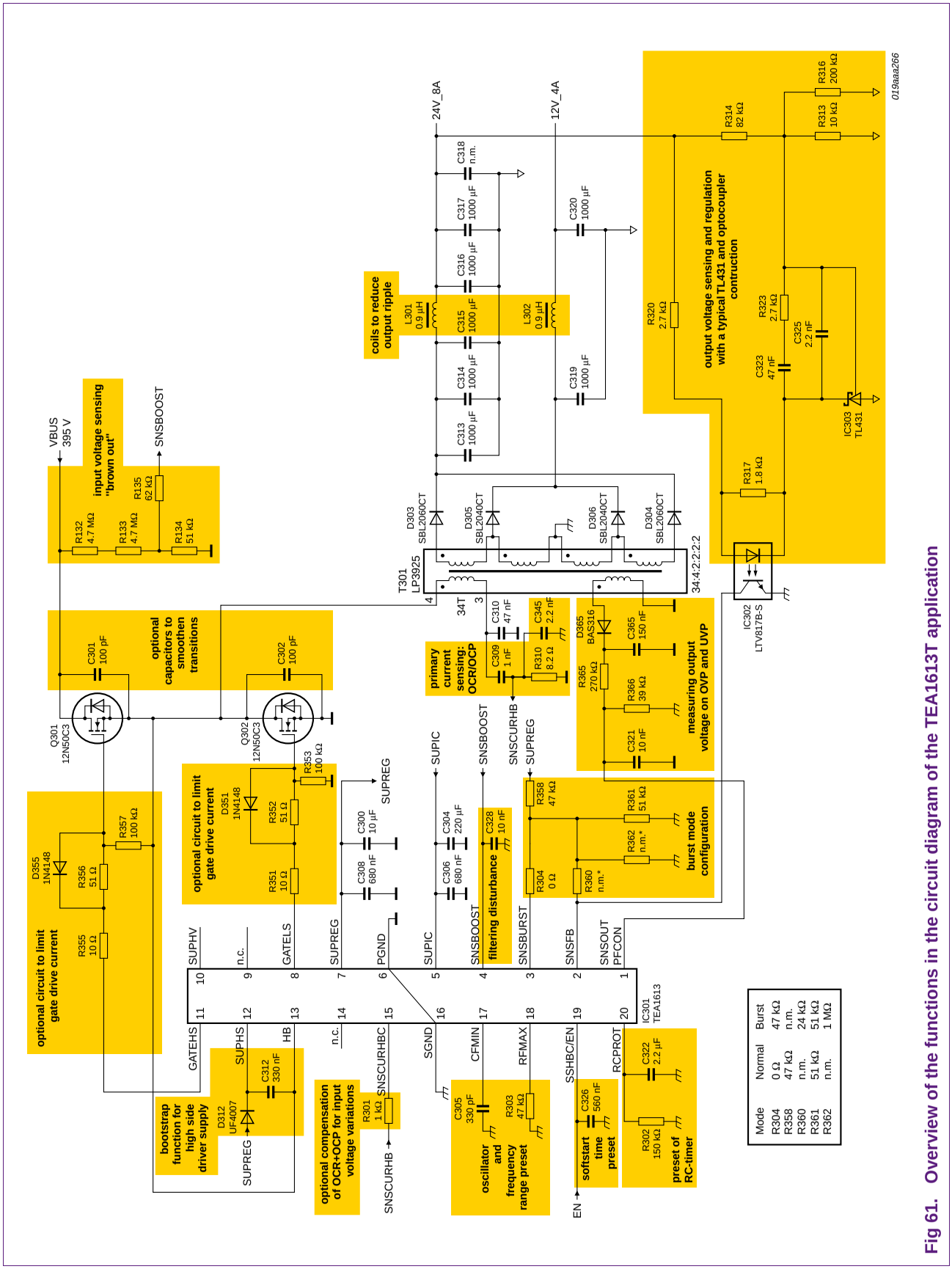


Fig 61. Overview of the functions in the circuit diagram of the TEA1613T application

# 13. Abbreviations

**Table 4. Abbreviations**

| Acronym | Description |
|---|---|
| ADT | Adaptive Dead Time |
| BCD | Bipolar CMOS DMOS |
| CMR | Capacitive Mode Regulation |
| EMC | ElectroMagnetic Compatibility |
| EMI | ElectroMagnetic Interference (or Immunity) |
| HB | Half-Bridge |
| HBC | HalfBridge Converter (or Controller) |
| HFP | High-Frequency Protection |
| HV | High Voltage |
| IC | Integrated Circuit |
| LCD | Liquid Crystal Display |
| LLC | Resonant converter (Lm + Lr + Cr in series) |
| NTC | Negative Temperature Coefficient |
| OCP | OverCurrent Protection |
| OCR | OverCurrent Regulation |
| OLP | Open Loop Protection |
| OTP | OverTemperature Protection |
| OVP | OverVoltage Protection |
| PCB | Printed-Circuit Board |
| PFC | Power Factor Converter/Controller |
| PWM | Pulse-Width Modulation |
| SCP | Short-Circuit Protection |
| SOI | Silicon-On-Insulator |
| UVP | UnderVoltage Protection |

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## 15. Tables



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