

# Analog Multiplexers/ Demultiplexers

## High-Performance Silicon-Gate CMOS

The MC54/74HC4051, MC74HC4052 and MC54/74HC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from  $V_{CC}$  to  $V_{EE}$ ).

The HC4051, HC4052 and HC4053 are identical in pinout to the metal-gate MC14051B, MC14052B and MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

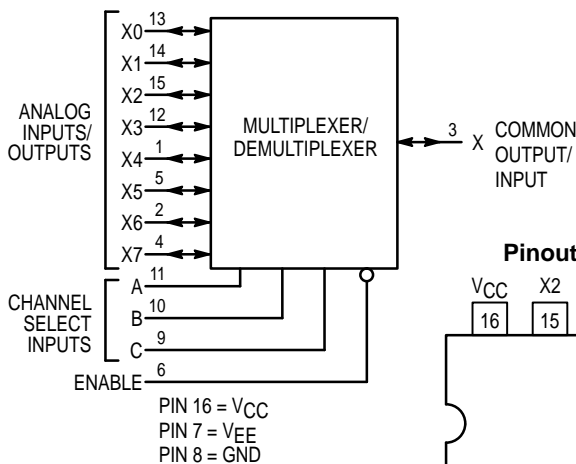
These devices have been designed so that the ON resistance ( $R_{ON}$ ) is more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

For multiplexers/demultiplexers with channel-select latches, see HC4351, HC4352 and HC4353.

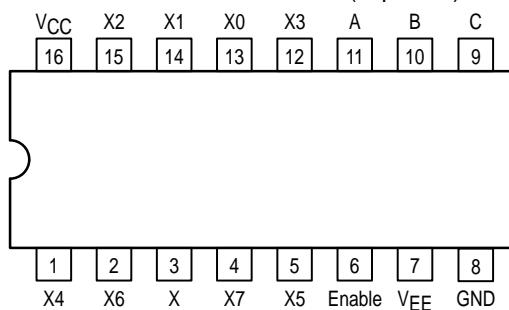
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ( $V_{CC} - V_{EE}$ ) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: HC4051 — 184 FETs or 46 Equivalent Gates  
 HC4052 — 168 FETs or 42 Equivalent Gates  
 HC4053 — 156 FETs or 39 Equivalent Gates

**LOGIC DIAGRAM**  
**MC54/74HC4051**

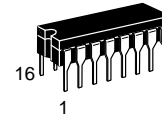
Single-Pole, 8-Position Plus Common Off



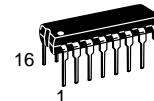
Pinout: MC54/74HC4051 (Top View)



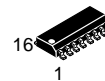
# MC54/74HC4051 MC74HC4052 MC54/74HC4053



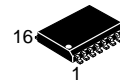
**J SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**D SUFFIX**  
SOIC PACKAGE  
CASE 751B-05



**DW SUFFIX**  
SOIC PACKAGE  
CASE 751G-02



**DT SUFFIX**  
TSSOP PACKAGE  
CASE 948F-01

**ORDERING INFORMATION**

MC54HCXXXXJ	Ceramic
MC74HCXXXXN	Plastic
MC74HCXXXXD	SOIC
MC74HCXXXXDW	SOIC Wide
MC74HCXXXXDT	TSSOP

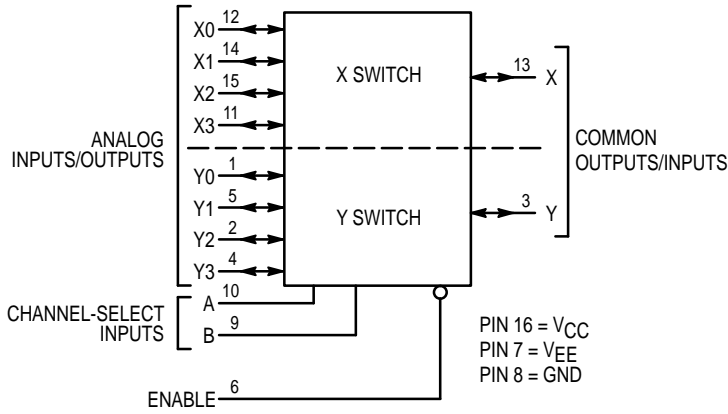
**FUNCTION TABLE - MC54/74HC4051**

Control Inputs		Select			ON Channels
Enable	C	B	A		
L	L	L	L	X0	
L	L	L	H	X1	
L	L	L	H	X2	
L	L	H	L	X3	
L	L	H	H	X4	
L	H	L	L	X5	
L	H	L	H	X6	
L	H	H	L	X7	
L	H	H	H	X7	
H	X	X	X	NONE	

X = Don't Care



**LOGIC DIAGRAM  
MC74HC4052  
Double-Pole, 4-Position Plus Common Off**

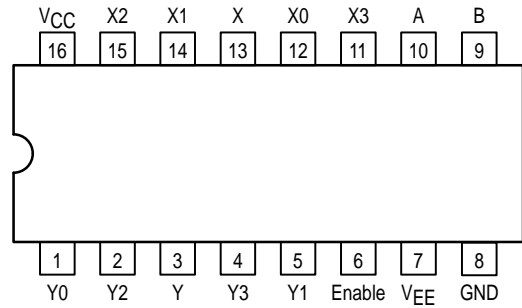


**FUNCTION TABLE – MC74HC4052**

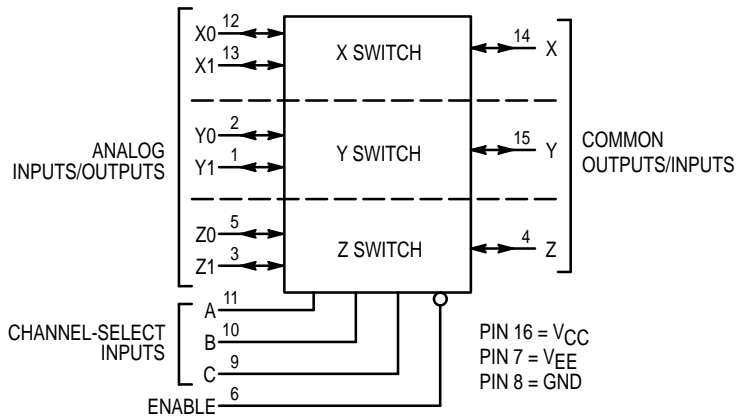
Control Inputs			ON Channels	
Enable	Select			
	B	A		
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

**Pinout: MC74HC4052 (Top View)**



**LOGIC DIAGRAM  
MC54/74HC4053  
Triple Single-Pole, Double-Position Plus Common Off**

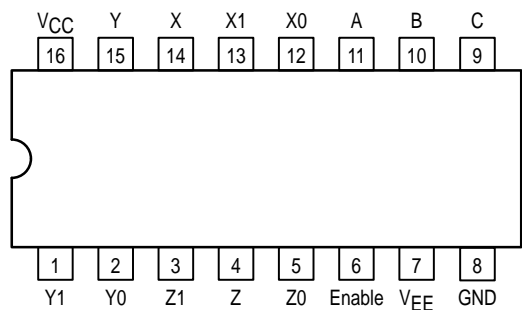


**FUNCTION TABLE – MC54/74HC4053**

Control Inputs				ON Channels		
Enable	Select					
	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

**Pinout: MC54/74HC4053 (Top View)**



NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND) (Referenced to V <sub>EE</sub> )	- 0.5 to + 7.0 - 0.5 to + 14.0	V
V <sub>EE</sub>	Negative DC Supply Voltage (Referenced to GND)	- 7.0 to + 5.0	V
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub> - 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T <sub>stg</sub>	Storage Temperature Range	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package Ceramic DIP	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
Ceramic DIP: - 10 mW/°C from 100° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND) (Referenced to V <sub>EE</sub> )	2.0 2.0	6.0 12.0	V
V <sub>EE</sub>	Negative DC Supply Voltage, Output (Referenced to GND)	- 6.0	GND	V
V <sub>IS</sub>	Analog Input Voltage	V <sub>EE</sub>	V <sub>CC</sub>	V
V <sub>in</sub>	Digital Input Voltage (Referenced to GND)	GND	V <sub>CC</sub>	V
V <sub>IO</sub> *	Static or Dynamic Voltage Across Switch		1.2	V
T <sub>A</sub>	Operating Temperature Range, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise/Fall Time (Channel Select or Enable Inputs)			ns
	V <sub>CC</sub> = 2.0 V	0	1000	
	V <sub>CC</sub> = 4.5 V	0	500	
	V <sub>CC</sub> = 6.0 V	0	400	

\* For voltage drops across switch greater than 1.2V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

MC54/74HC4051 MC74HC4052 MC54/74HC4053

**DC CHARACTERISTICS — Digital Section** (Voltages Referenced to GND)  $V_{EE} = \text{GND}$ , Except Where Noted

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
$V_{IH}$	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0	1.50	1.50	1.50	V
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
$V_{IL}$	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
$I_{in}$	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{in} = V_{CC}$ or GND, $V_{EE} = -6.0 \text{ V}$	6.0	± 0.1	± 1.0	± 1.0	μA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and $V_{IS} = V_{CC}$ or GND; $V_{EE} = \text{GND}$ $V_{IO} = 0 \text{ V}$ $V_{EE} = -6.0$	6.0	2	20	40	μA
			6.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**DC CHARACTERISTICS — Analog Section**

Symbol	Parameter	Condition	$V_{CC}$	$V_{EE}$	Guaranteed Limit			Unit	
					-55 to 25°C	≤85°C	≤125°C		
$R_{on}$	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IS} = V_{CC}$ to $V_{EE}$ ; $I_S \leq 2.0 \text{ mA}$ (Figures 1, 2)	4.5	0.0	190	240	280	Ω	
			4.5	-4.5	120	150	170		
			6.0	-6.0	100	125	140		
		$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IS} = V_{CC}$ or $V_{EE}$ (Endpoints); $I_S \leq 2.0 \text{ mA}$ (Figures 1, 2)	4.5	0.0	150	190	230		
			4.5	-4.5	100	125	140		
			6.0	-6.0	80	100	115		
$\Delta R_{on}$	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IS} = 1/2 (V_{CC} - V_{EE})$ ; $I_S \leq 2.0 \text{ mA}$	4.5	0.0	30	35	40	Ω	
			4.5	-4.5	12	15	18		
			6.0	-6.0	10	12	14		
$I_{off}$	Maximum Off-Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IO} = V_{CC} - V_{EE}$ ; Switch Off (Figure 3)	6.0	-6.0	0.1	0.5	1.0	μA	
			Maximum Off-Channel Leakage Current, Common Channel	HC4051 HC4052 HC4053	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IO} = V_{CC} - V_{EE}$ ; Switch Off (Figure 4)	6.0	-6.0		0.2
	6.0	-6.0				0.1	1.0		2.0
	6.0	-6.0				0.1	1.0		2.0
$I_{on}$	Maximum On-Channel Leakage Current, Channel-to-Channel	HC4051 HC4052 HC4053	$V_{in} = V_{IL}$ or $V_{IH}$ ; Switch-to-Switch = $V_{CC} - V_{EE}$ ; (Figure 5)	6.0	-6.0	0.2	2.0	4.0	μA
				6.0	-6.0	0.1	1.0	2.0	
				6.0	-6.0	0.1	1.0	2.0	
				6.0	-6.0	0.1	1.0	2.0	

**AC CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0	370	465	550	ns
		4.5	74	93	110	
		6.0	63	79	94	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	290	364	430	ns
		4.5	58	73	86	
		6.0	49	62	73	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	345	435	515	ns
		4.5	69	87	103	
		6.0	59	74	87	
C <sub>in</sub>	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
C <sub>I/O</sub>	Maximum Capacitance (All Switches Off)	Analog I/O	35	35	35	pF
		Common O/I: HC4051	130	130	130	
		HC4052	80	80	80	
		HC4053	50	50	50	
	Feedthrough		1.0	1.0	1.0	

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Figure 13)*		Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V			pF
			HC4051	HC4052	HC4053	
		HC4051	45			pF
		HC4052	80			
		HC4053	45			

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)**

Symbol	Parameter	Condition	V <sub>CC</sub> V	V <sub>EE</sub> V	Limit*			Unit
					25°C			
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 6)	f <sub>in</sub> = 1MHz Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>OS</sub> ; Increase f <sub>in</sub> Frequency Until dB Meter Reads -3dB; R <sub>L</sub> = 50Ω, C <sub>L</sub> = 10pF	2.25	-2.25	'51	'52	'53	MHz
			4.50	-4.50	80	95	120	
			6.00	-6.00	80	95	120	
—	Off-Channel Feedthrough Isolation (Figure 7)	f <sub>in</sub> = Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>IS</sub> f <sub>in</sub> = 10kHz, R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF	2.25	-2.25	-50			dB
			4.50	-4.50	-50			
—	Feedthrough Noise. Channel-Select Input to Common I/O (Figure 8)	V <sub>in</sub> ≤ 1MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6ns); Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0A; Enable = GND R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF	2.25	-2.25	25			mV <sub>pp</sub>
			4.50	-4.50	105			
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051)	f <sub>in</sub> = Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>IS</sub> f <sub>in</sub> = 10kHz, R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF	2.25	-2.25	-50			dB
			4.50	-4.50	-50			
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051)	f <sub>in</sub> = 1.0MHz, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 10pF	2.25	-2.25	-60			dB
			4.50	-4.50	-60			
THD	Total Harmonic Distortion (Figure 14)	f <sub>in</sub> = 1kHz, R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 50pF THD = THD <sub>measured</sub> - THD <sub>source</sub> V <sub>IS</sub> = 4.0V <sub>pp</sub> sine wave V <sub>IS</sub> = 8.0V <sub>pp</sub> sine wave V <sub>IS</sub> = 11.0V <sub>pp</sub> sine wave	2.25	-2.25	0.10			%
			4.50	-4.50	0.08			
			6.00	-6.00	0.05			

\* Limits not tested. Determined by design and verified by qualification.

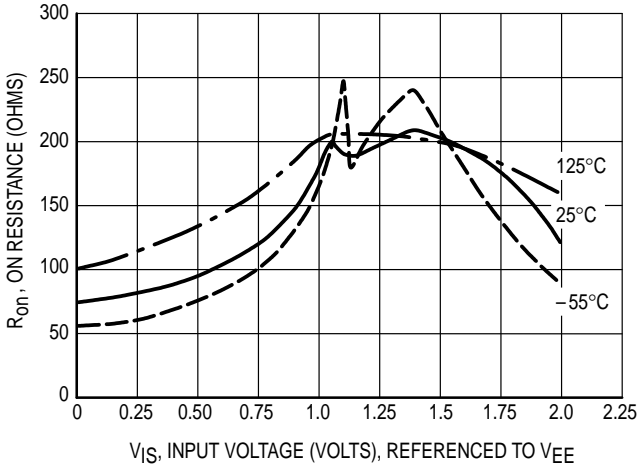


Figure 1a. Typical On Resistance,  $V_{CC} - V_{EE} = 2.0 \text{ V}$

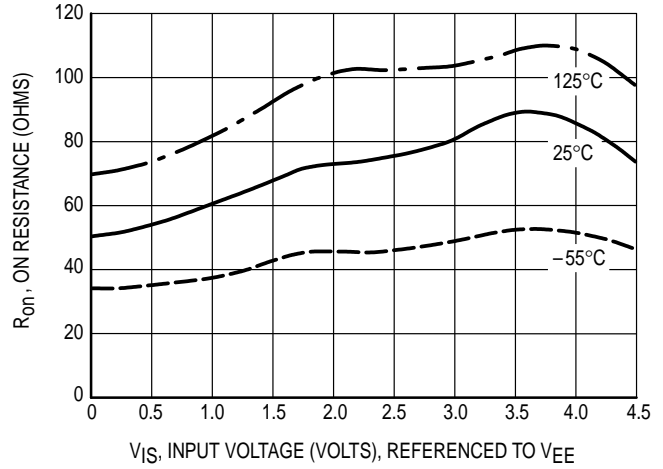


Figure 1b. Typical On Resistance,  $V_{CC} - V_{EE} = 4.5 \text{ V}$

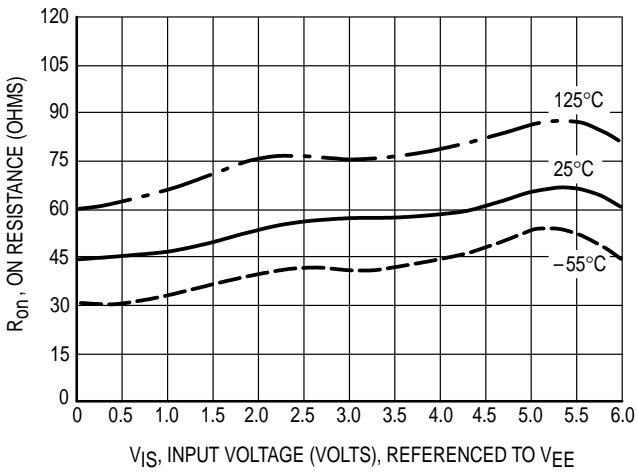


Figure 1c. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0 \text{ V}$

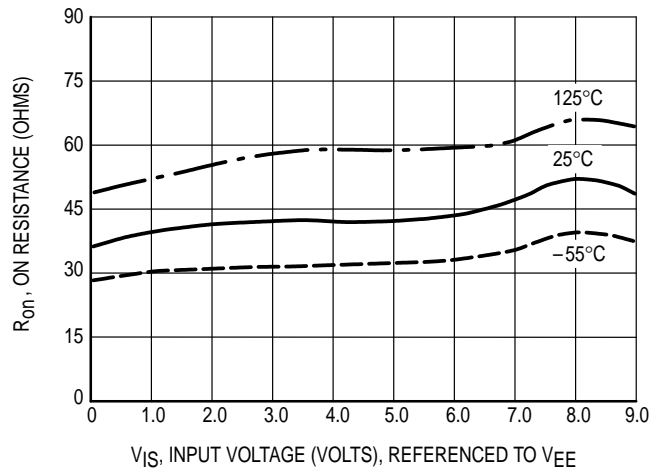


Figure 1d. Typical On Resistance,  $V_{CC} - V_{EE} = 9.0 \text{ V}$

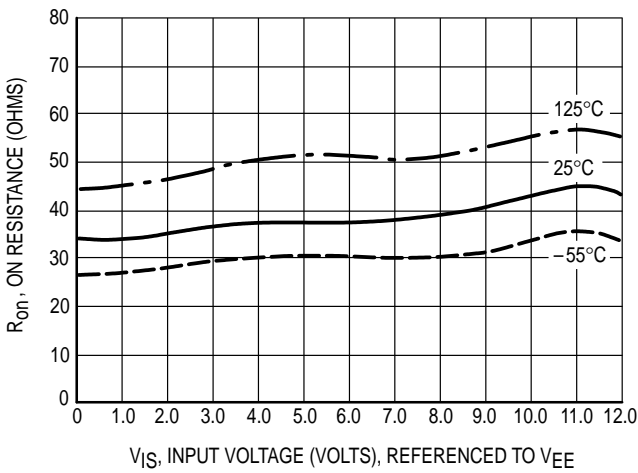


Figure 1e. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0 \text{ V}$

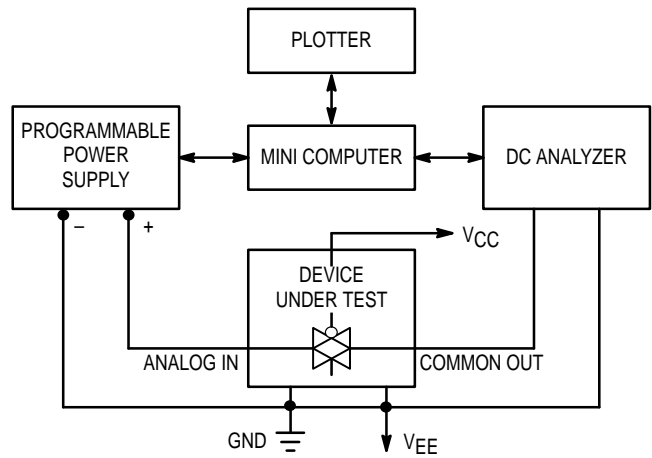


Figure 2. On Resistance Test Set-Up

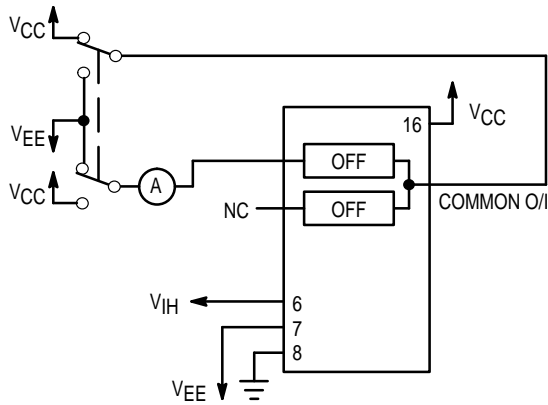


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

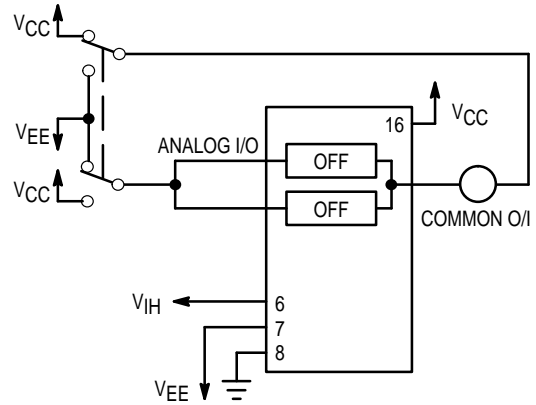


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

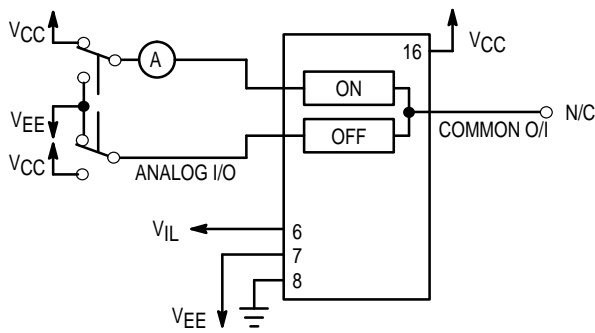
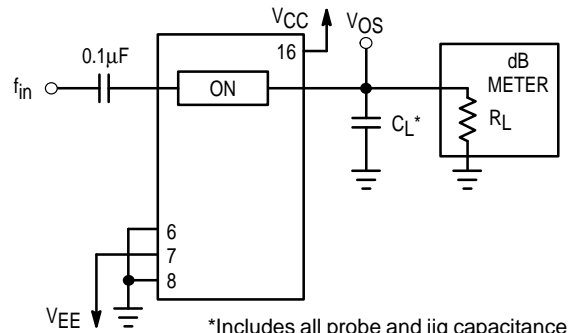
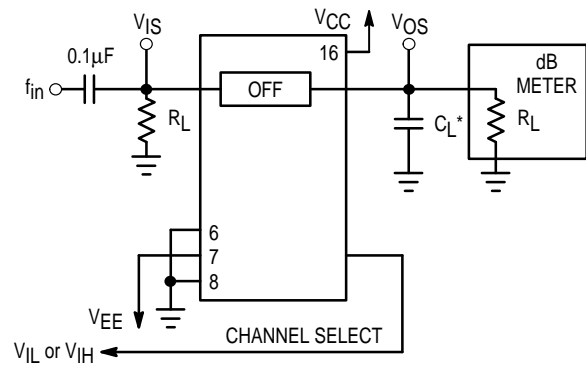


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



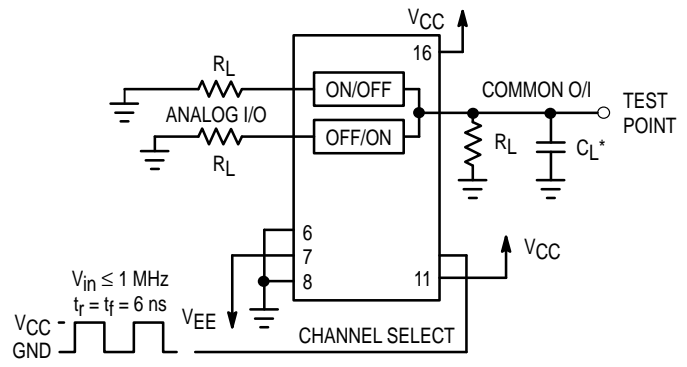
\*Includes all probe and jig capacitance

Figure 6. Maximum On Channel Bandwidth, Test Set-Up



\*Includes all probe and jig capacitance

Figure 7. Off Channel Feedthrough Isolation, Test Set-Up



\*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up



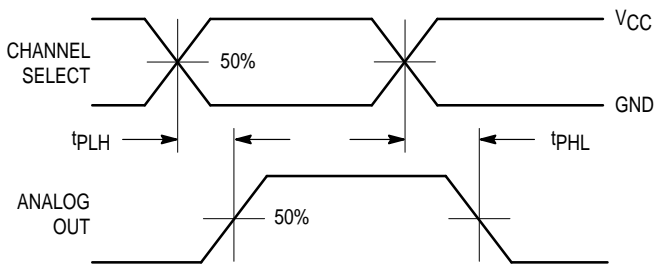
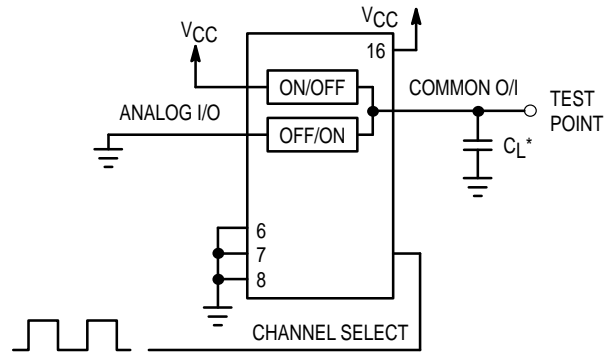


Figure 9a. Propagation Delays, Channel Select to Analog Out



\*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

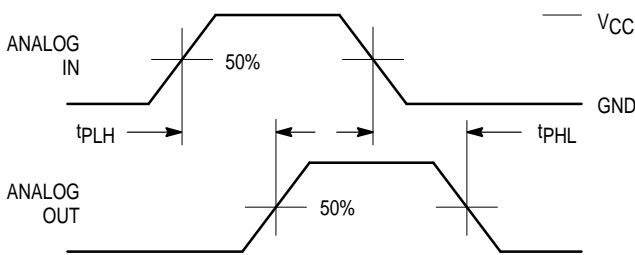
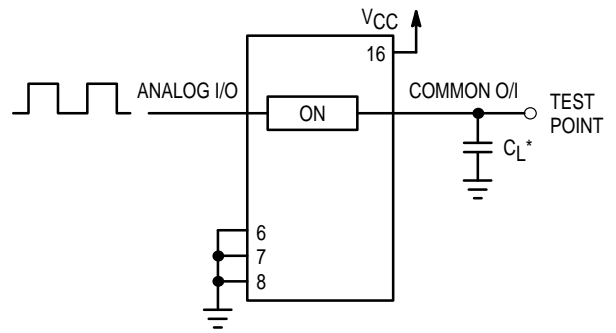


Figure 10a. Propagation Delays, Analog In to Analog Out



\*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

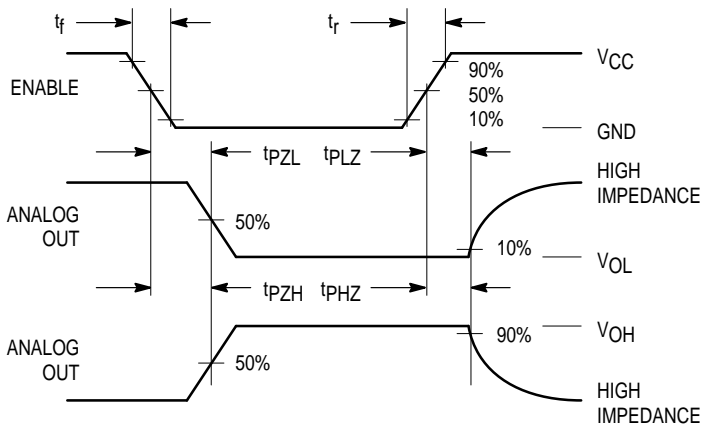


Figure 11a. Propagation Delays, Enable to Analog Out

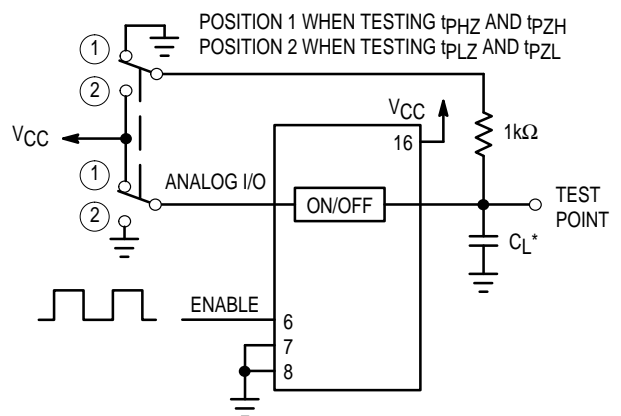
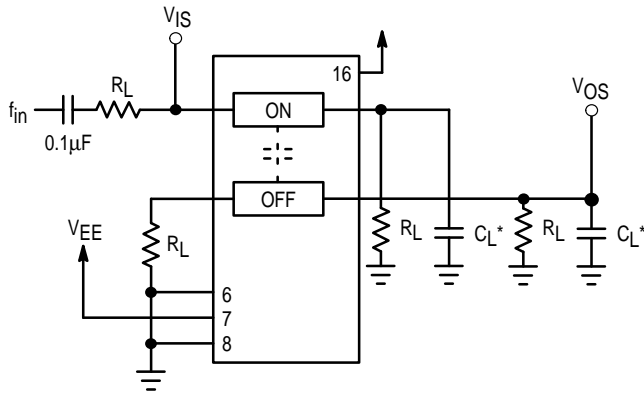
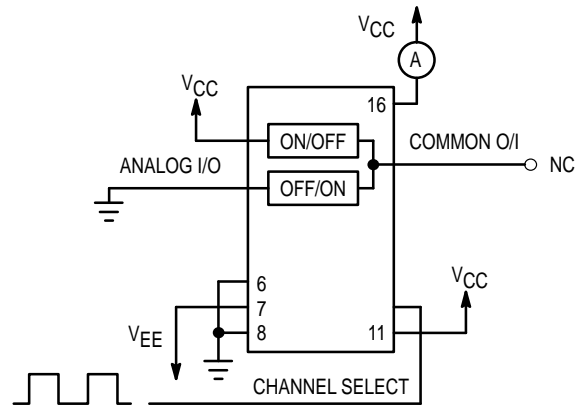


Figure 11b. Propagation Delay, Test Set-Up Enable to Analog Out

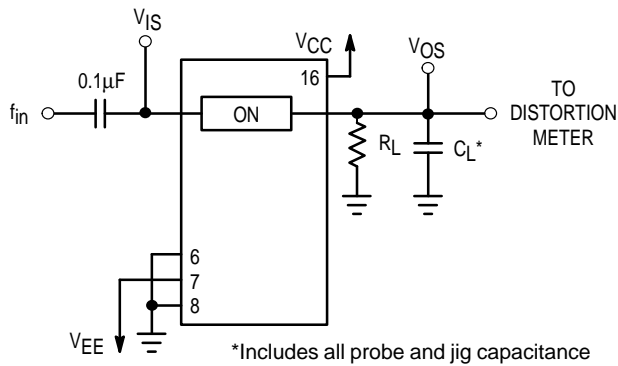


\*Includes all probe and jig capacitance

**Figure 12. Crosstalk Between Any Two Switches, Test Set-Up**

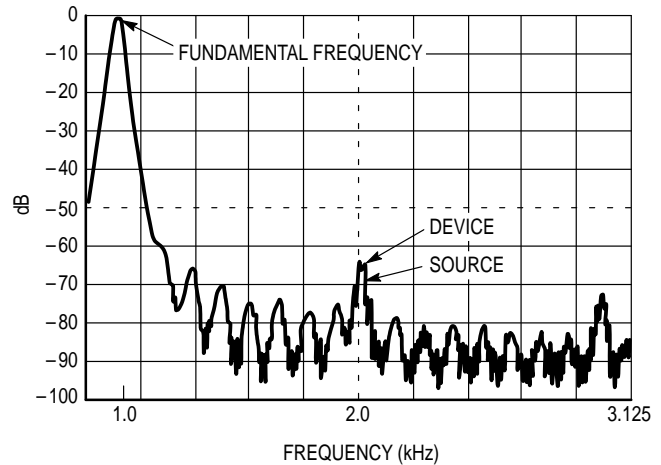


**Figure 13. Power Dissipation Capacitance, Test Set-Up**



\*Includes all probe and jig capacitance

**Figure 14a. Total Harmonic Distortion, Test Set-Up**



**Figure 14b. Plot, Harmonic Distortion**

**APPLICATIONS INFORMATION**

The Channel Select and Enable control pins should be at  $V_{CC}$  or GND logic levels.  $V_{CC}$  being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5V = \text{logic high}$$

$$GND = 0V = \text{logic low}$$

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In this example, the difference between  $V_{CC}$  and  $V_{EE}$  is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to

$V_{CC}$  or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{CC} - GND = 2 \text{ to } 6 \text{ volts}$$

$$V_{EE} - GND = 0 \text{ to } -6 \text{ volts}$$

$$V_{CC} - V_{EE} = 2 \text{ to } 12 \text{ volts}$$

and  $V_{EE} \leq GND$

When voltage transients above  $V_{CC}$  and/or below  $V_{EE}$  are anticipated on the analog channels, external Germanium or Schottky diodes ( $D_x$ ) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

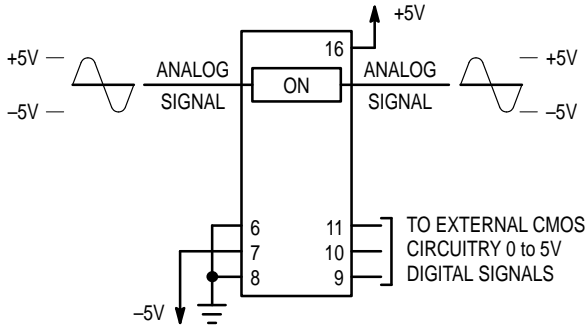


Figure 15. Application Example

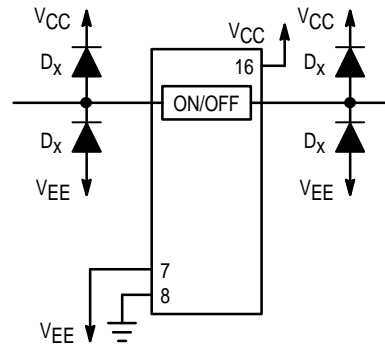
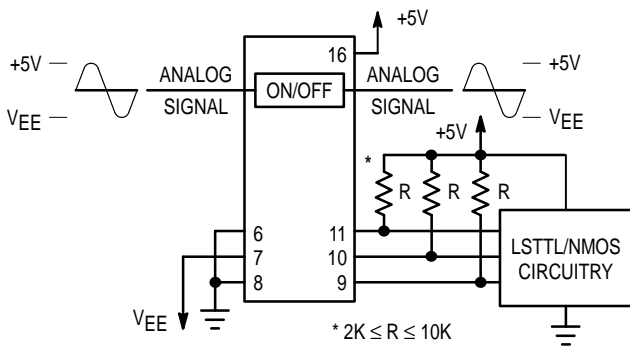
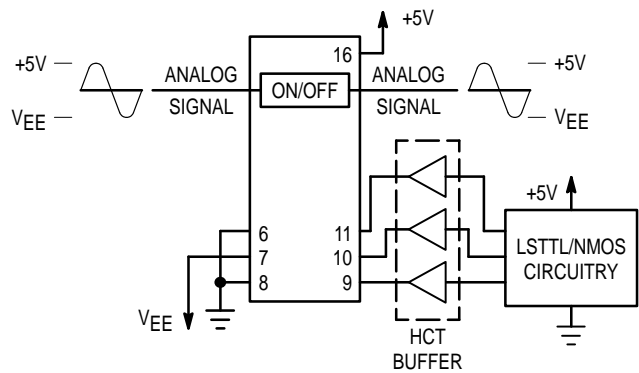


Figure 16. External Germanium or Schottky Clipping Diodes



a. Using Pull-Up Resistors



b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

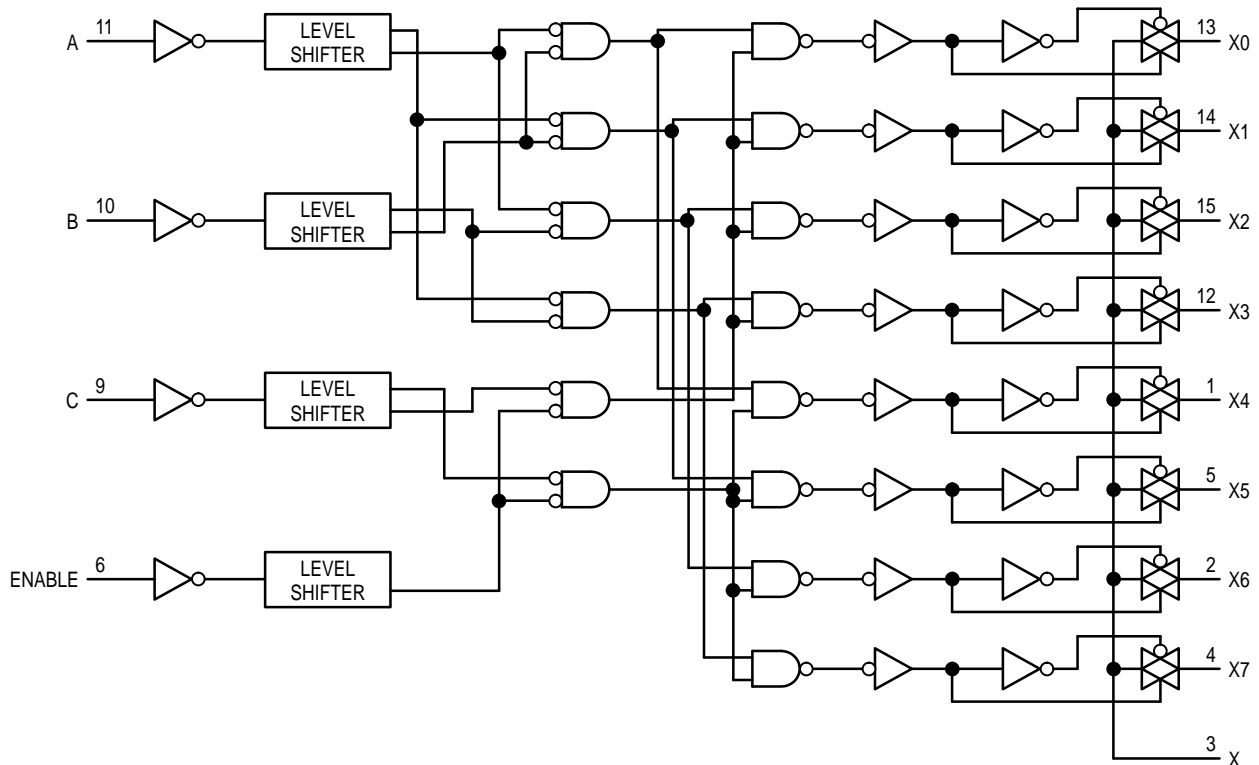


Figure 18. Function Diagram, HC4051

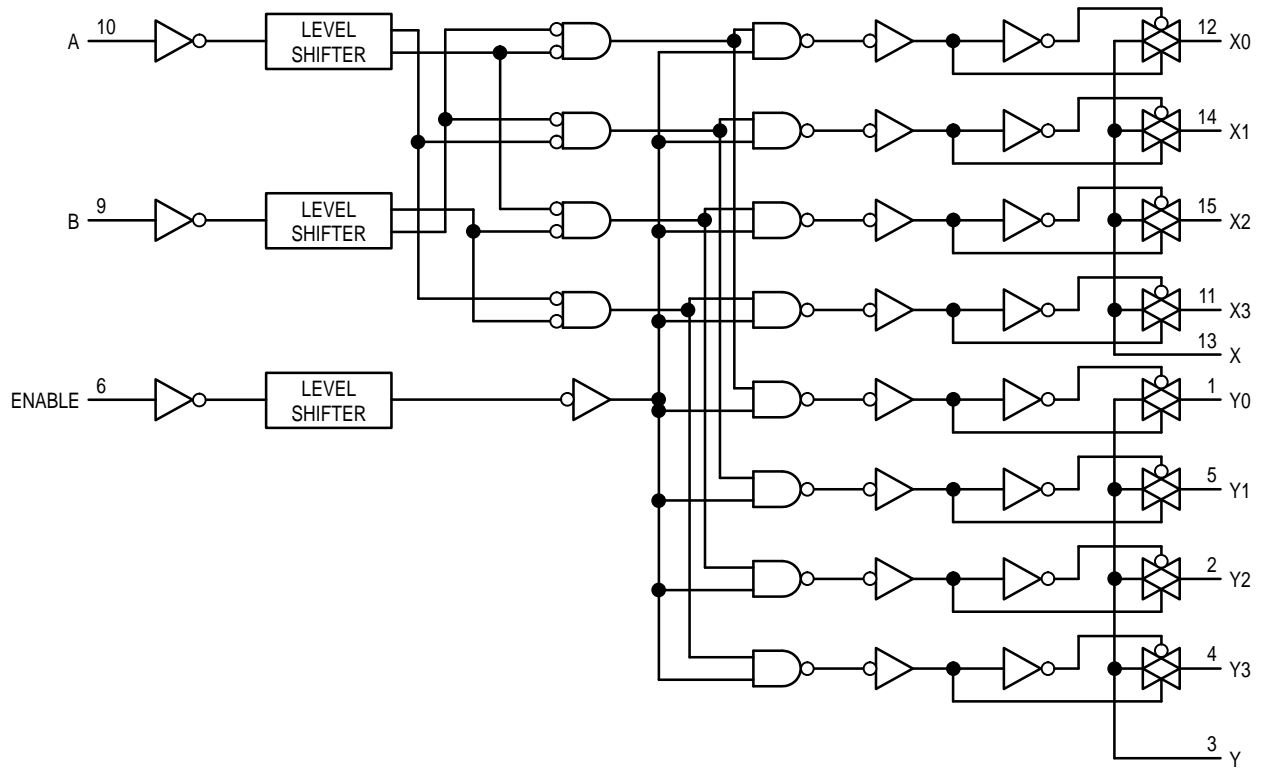


Figure 19. Function Diagram, HC4052

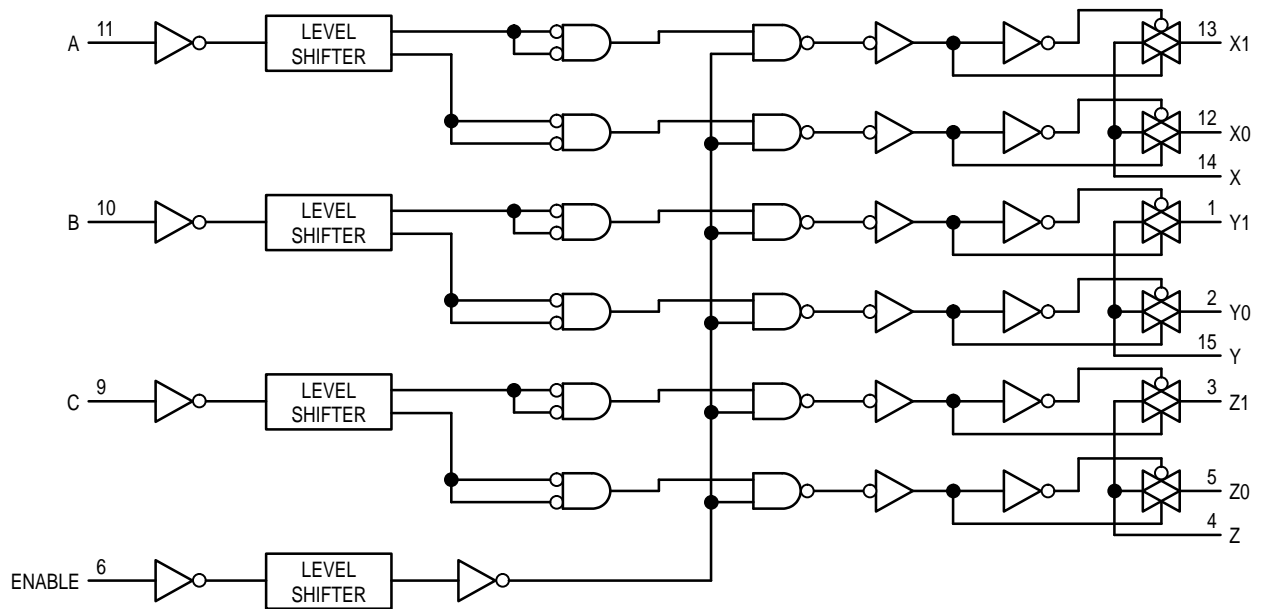
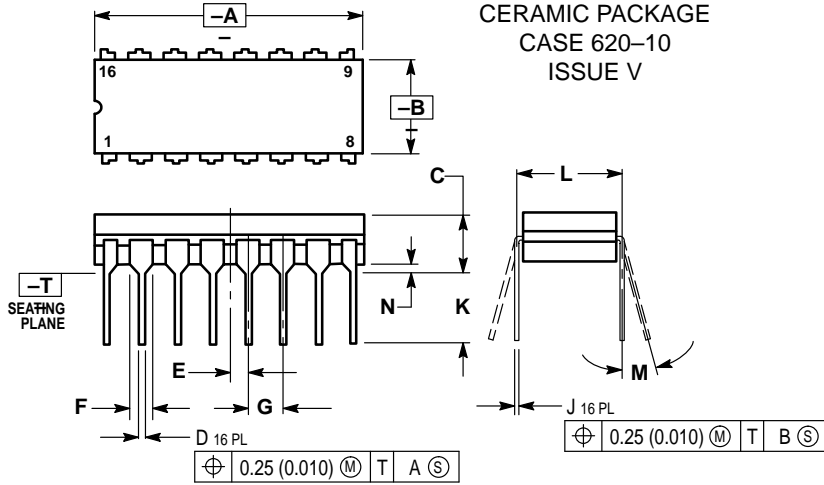


Figure 20. Function Diagram, HC4053

OUTLINE DIMENSIONS

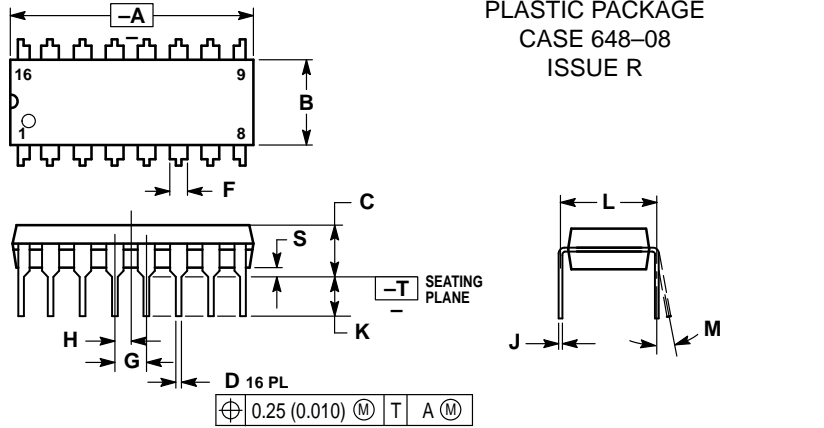
**J SUFFIX  
CERAMIC PACKAGE  
CASE 620-10  
ISSUE V**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

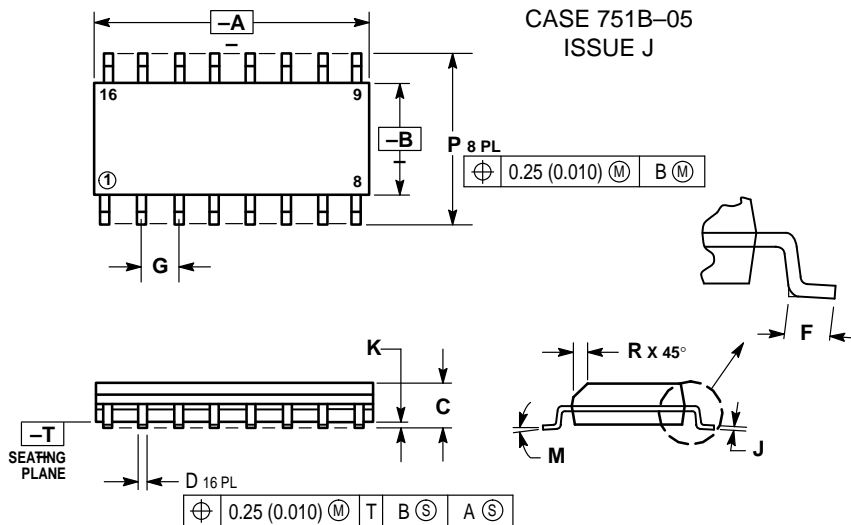
**N SUFFIX  
PLASTIC PACKAGE  
CASE 648-08  
ISSUE R**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J**

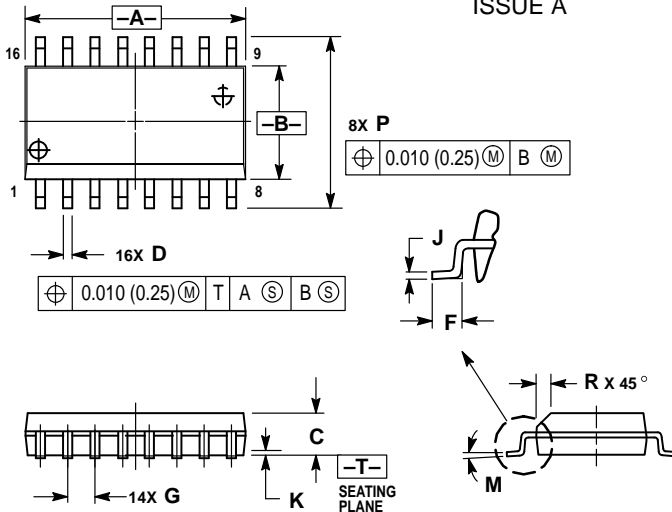


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

**OUTLINE DIMENSIONS**

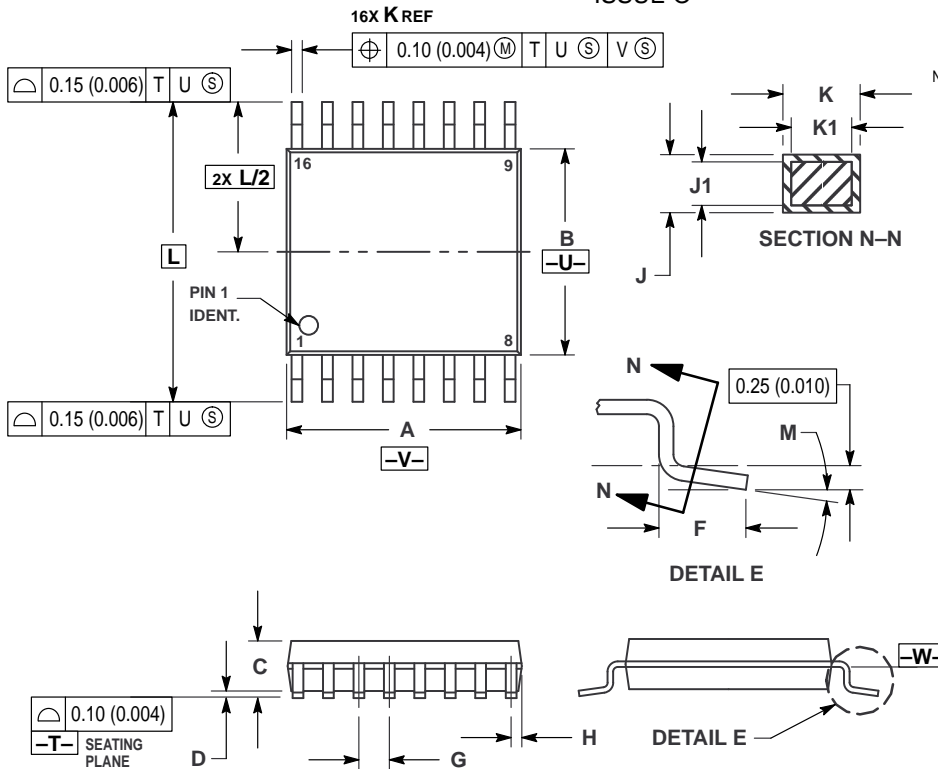
**DW SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751G-02**  
**ISSUE A**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

**DT SUFFIX**  
**PLASTIC TSSOP PACKAGE**  
**CASE 948F-01**  
**ISSUE O**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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