SX-A Family FPGAs

Leading-Edge Performance

- 250 MHz System Performance
- 3.8ns Clock-to-Out (Pad-to-Pad)
- 350 MHz Internal Performance

Specifications

- 12,000 to 108,000 Available System Gates
- Up to 360 User-Programmable I/O Pins
- Up to 2,012 Dedicated Flip-Flops
- 0.22µ/0.25µ CMOS Process Technology

Features

- Hot-Swap Compliant I/Os
- Power-Up/Down Friendly (No Sequencing Required for Supply Voltages)
- 66 MHz PCI Compliant
- CPLD and FPGA Integration
- Single-Chip Solution
- Nonvolatile
- Configurable I/O Support for 3.3V/5.0V PCI, 5.0V TTL, and 2.5 V/3.3V LVTTL
- 2.5V, 3.3V, and 5.0V Mixed Voltage Operation with 5.0V Input Tolerance and 5.0V Drive Strength
- Configurable Weak-Resistor Pull-up or Pull-down for Tristated Outputs at Power Up
- Individual Output Slew Rate Control
- Up to 100% Resource Utilization and 100% Pin Locking
- Very Low Power Consumption
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Secure Programming Technology Prevents Reverse Engineering and Design Theft

Datasheet.Directory

SX-A Product Profile

Device	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Capacity				
Typical Gates	8,000	16,000	32,000	72,000
System Gates	12,000	24,000	48,000	108,000
Logic Modules	768	1,452	2,880	6,036
Combinatorial Cells	512	924	1,800	4,024
Register Cells				
Dedicated Flip-Flops	256	528	1,080	2,012
Maximum Flip-Flops	512	990	1,980	4,024
Maximum User I/Os	130	180	249	360
Global Clocks	3	3	3	3
Quadrant Clocks	0	0	0	4
Boundary Scan Testing	Yes	Yes	Yes	Yes
3.3V/5.0V PCI	Yes	Yes	Yes	Yes
Clock-to-Out	4.2 ns	4.6 ns	4.7 ns	5.8 ns
Input Set-Up (External)	0 ns	0 ns	0 ns	0 ns
Speed Grades	–F, Std, –1, –2, –3	–F, Std, –1, –2, –3	–F, Std, –1, –2, –3	–F, Std, –1, –2, –3
Temperature Grades	C, I	C, I, M	C, I, M	C, I, M
Package (by pin count)				
PQFP	208	208	208	208
TQFP	100, 144	100, 144	100, 144, 176	—
PBGA	—	—	329	—
FBGA	144	144, 256	144, 256, 484	256, 484

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General Description

Actel's SX-A family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX-A devices simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

Actel's SX-A architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX-A devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three or fewer antifuses). The unique local and general routing structure featured in SX-A devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX-A's flexible routing structure is a hard-wired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input set-up times. SX-A devices have easy-to-use I/O cells that do not require HDL instantiation, facilitating design re-use and reducing design and verification time.

Ordering Information

A54SX16 A – 2 PQ 208

Application (Temperature Range)
- Blank = Commercial (0 to +70°C)
- I = Industrial (–40 to +85°C)
- M = Military (–55 to +125°C)
- PP = Pre-production

Package Lead Count

Package Type
- BG = 1.27mm Plastic Ball Grid Array
- FG = 1.0mm Fine Pitch Ball Grid Array
- PQ = Plastic Quad Flat Pack
- TQ = Thin (1.4mm) Quad Flat Pack

Speed Grade
- Blank = Standard Speed
- –1 = Approximately 15% Faster than Standard
- –2 = Approximately 25% Faster than Standard
- –3 = Approximately 35% Faster than Standard
- –F = Approximately 40% Slower than Standard

A = 0.22µ/0.25µ CMOS Technology

Part Number
- A54SX08 = 12,000 System Gates
- A54SX16 = 24,000 System Gates
- A54SX32 = 48,000 System Gates
- A54SX72 = 108,000 System Gates

Product Plan

	Speed Grade*					Application		
	–F	Std	–1	–2	–3	C	I†	M•
A54SX08A Device								
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	P	✔	✔	—
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	P	✔	✔	—
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	P	✔	✔	—
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	P	✔	✔	—
A54SX16A Device								
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	P
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	P
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	P
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	P	P	—
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	P	P	—
A54SX32A Device								
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	P
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	P
176-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	P
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	P
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	—
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	—
329-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔	✔	✔	✔	—
484-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	—
A54SX72A Device								
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	P
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	—
484-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	—

Contact your Actel sales representative for product availability.

Applications: *C = Commercial* *I = Industrial* *M = Military*

Availability: ✔ = *Available* *P = Planned* — = *Not Planned*

**Speed Grade:* *–1 = Approx. 15% faster than Standard* *–2 = Approx. 25% faster than Standard* *–3 = Approx. 35% faster than Standard* *–F = Approx. 40% slower than Standard*

† Only Std, –1, –2 Speed Grade

• Only Std, –1 Speed Grade

Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PQFP 208-Pin	TQFP 100-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 329-Pin	FBGA 144-Pin	FBGA 256-Pin	FBGA 484-Pin
A54SX08A	130	81	113	—	—	111	—	—
A54SX16A	175	81	113	—	—	111	180	—
A54SX32A	174	81	113	147	249	111	203	249
A54SX72A	171	—	—	—	—	—	203	360

Contact your Actel sales representative for product availability.

Package Definitions

PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = 1.27mm Plastic Ball Grid Array, FBGA = 1.0mm Fine Pitch Ball Grid Array.

SX-A Family Architecture

The SX-A family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

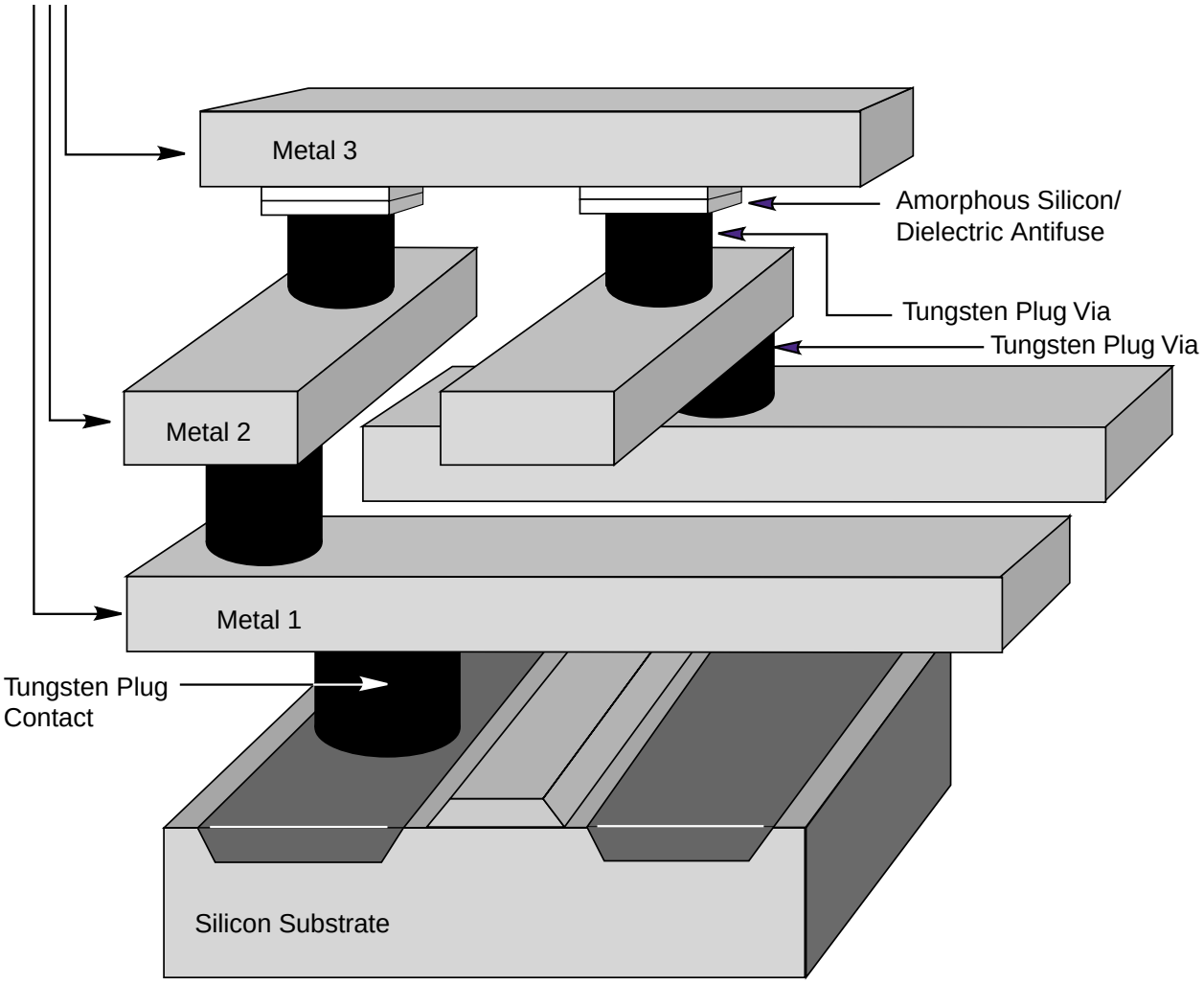
Programmable Interconnect Element

The SX-A family provides efficient use of silicon by locating the routing interconnect resources between the top two metal layers (Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX-A family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.



Note: *A54SX72A has 4 layers of metal with the antifuse between Metal 3 and Metal 4.*

Figure 1 • *SX-A Family Interconnect Elements*

Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Actel's SX-A family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions up to 5 inputs (Figure 3 on page 6). Inclusion of the DB input and its associated inverter function increases the number of combinatorial functions that can be implemented in a single module from 800 options (as in previous architectures) to more than 4,000 in the SX-A architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Chip Architecture

The SX-A family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 4 on page 6). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect,* which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 5 and Figure 6 on page 7). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

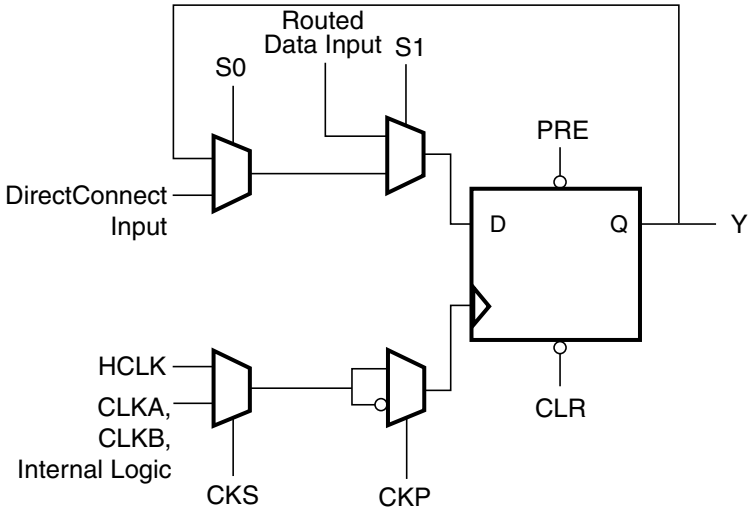


Figure 2 • *R-Cell*

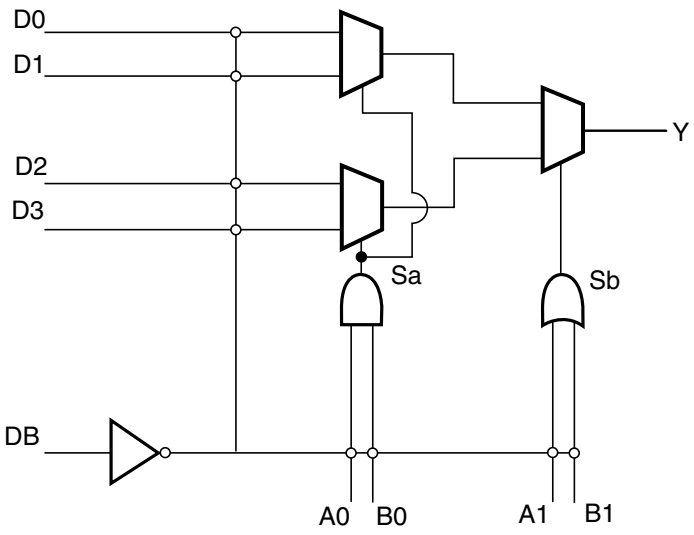


Figure 3 • *C-Cell*

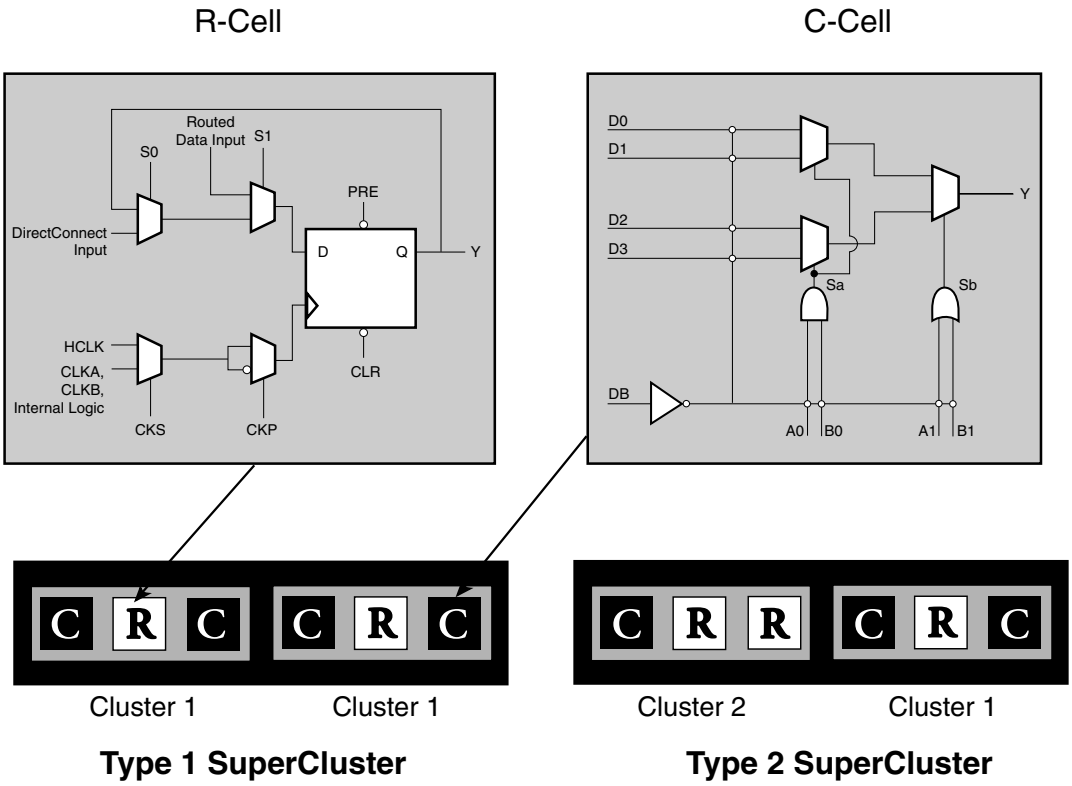


Figure 4 • *Cluster Organization*

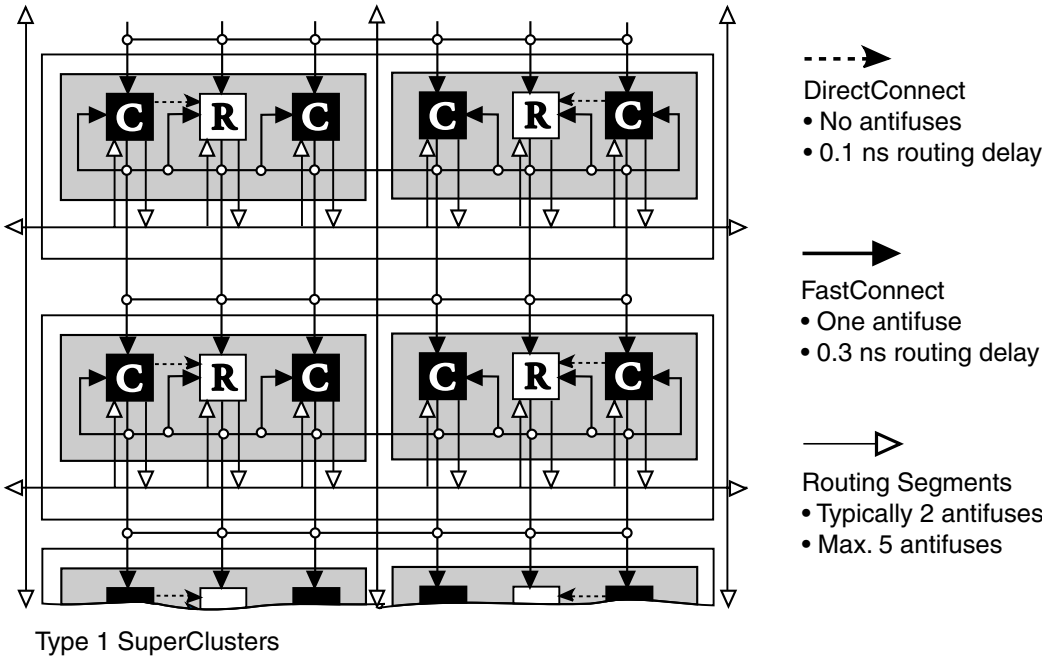


Figure 5 • *DirectConnect and FastConnect for Type 1 SuperClusters*

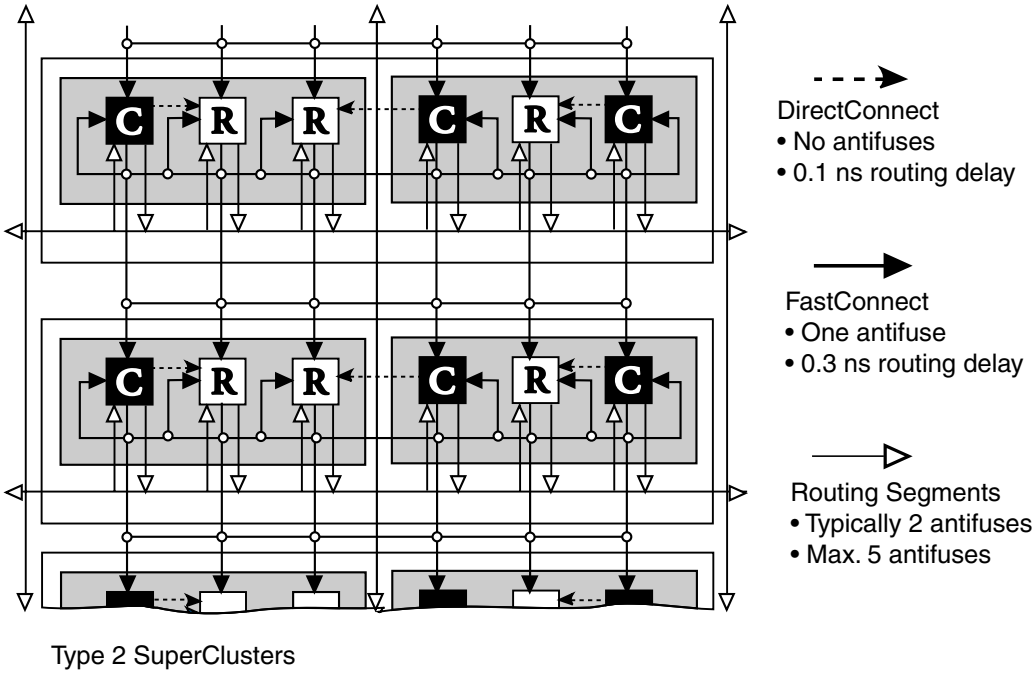


Figure 6 • *DirectConnect and FastConnect for Type 2 SuperClusters*

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

Clock Resources

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 3.8ns clock-to-out (pad-to-pad) performance of the SX-A devices. The hard-wired clock is tuned to provide clock skew less than 0.3ns worst case.

The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals then the external clock pin cannot be used for any other input and must be tied low or high. Figure 7 describes the clock circuit used for the constant load HCLK. Figure 8 describes the CLKA and CLKB circuit used in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The CLKA, CLKB, and QCLK circuits for A54SX72A are shown in Figure 9. For more information, refer to "Pin Description" on page 50.

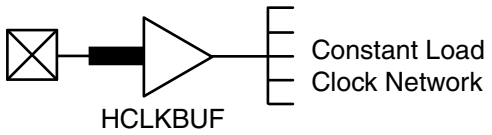


Figure 7 • SX-A HCLK Clock Pad

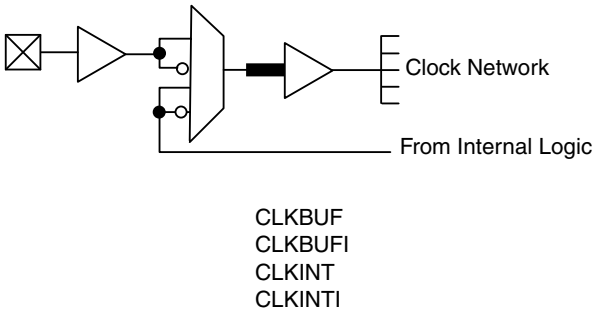


Figure 8 • SX-A Routed Clock Structure (Excluding SX72A)

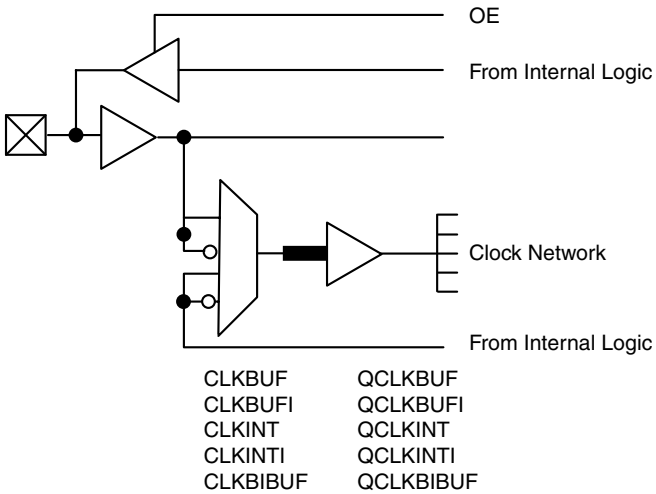


Figure 9 • SX-A Routed Clock and QClock Structure

Other Architectural Features

Technology

Actel's SX-A family is implemented on a high-voltage twin-well CMOS process using 0.22µ/0.25µ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX-A devices to operate with internal clock frequencies of 350 MHz, enabling very fast execution of even complex logic functions. Thus, the SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

I/O Modules

Each I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-output-pad timing as fast as 3.8ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. See Table 1 for more information.

SX-A inputs should be driven by high-speed push-pull devices with a low-resistance pull-up device. If the input voltage is greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below spec for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5.0V to provide the logic '1' input, and V_{CCI} is set to 3.3V on the SX-A device, the input signal may be pulled down by the SX-A input.

Hot Swapping

SX-A I/Os can be configured to be hot swappable in compliance with Compact PCI Specification. During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power up/down, and they do not require a specific power-up or power-down sequence in order to avoid damage to the SX-A devices. After the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Please see Actel's web site for future Application Notes concerning Hot Swapping.

Table 1 • I/O Features

Function	Description
Input Buffer Threshold Selections	• LVTTL/5.0V PCI/TTL • 3.3V PCI
Flexible Output Driver	• 2.5V/3.3V LVTTL • 3.3V PCI • 5.0V CMOS • 5.0V PCI/TTL
Output Buffer	"Hot-Swap" Capability • I/O on an unpowered device does not sink current • Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable low-slew option
Power-Up	Individually selectable pull-ups and pull-downs during power up (default is to power up in tristate) Enables deterministic power up of device V_{CCA} and V_{CCI} can be powered in any order

Power Requirements

The SX-A family supports 2.5V/3.3V/5.0V mixed voltage operation and is designed to tolerate 5.0V inputs in each case (Table 2). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (SRAM or EPROM do), making it the lowest-power architecture FPGA available today.

Table 2 • Supply Voltages

	V_{CCA}	V_{CCI}	Maximum Input Tolerance	Maximum Output Drive
A54SX08A **A54SX16A** **A54SX32A** **A54SX72A**	2.5V	2.5V	5.0V	2.5V
	2.5V	3.3V	5.0V	3.3V
	2.5V	5.0V	5.0V	5.0V

Boundary Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant. SX-A devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 3. In the dedicated test mode, TCK, TDI and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10kΩ. TMS can be pulled LOW to initiate the test sequence.

Table 3 • Boundary Scan Pin Functionality

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10kΩ on TMS

Configuring Diagnostic Pins

The JTAG and Probe pins (TDI, TCK, TMS, TDO, PRA, and PRB) are placed in the desired mode by selecting the appropriate check boxes in the "Variation" dialog window. This dialog window is accessible through the Design Setup Wizard under the Tools menu in Actel's Designer software.

TRST pin

When the "Reserve JTAG Reset" box is checked (default setting in Designer software), the TRST pin will become a Boundary Scan Reset pin. In this mode, the TRST pin will function as an asynchronous, active-low input to initialize or reset the BST circuit. An internal pull-up resistor will be automatically enabled on the TRST pin.

The TRST pin will function as a user I/O when "Reserve JTAG Reset" box is not checked. The internal pull-up resistor will be disabled in this mode.

Dedicated Test mode

When the "Reserve JTAG" box is checked, the SX-A is placed in Dedicated Test mode, which configures the TDI, TCK, and TDO pins for BST or in-circuit verification with Silicon Explorer II. An internal pull-up resistor is automatically enabled on both the TMS and TDI pins. In Dedicated test mode, TCK, TDI, and TDO are dedicated test pins and become unavailable for pin assignment in the Pin Editor. The TMS pin will function as specified in the IEEE 1149.1 (JTAG) Specification.

Flexible mode

When the "Reserve JTAG" box is not selected (default setting in Designer software), the SX-A is placed in Flexible mode, which allows the TDI, TCK, and TDO pins to function as user I/Os or BST pins. In this mode the internal pull-up resistors on the TMS and TDI pins are disabled. An external 10kΩ pull-up resistor to V_{CCI} is required on the TMS pin.

The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logical low. Once the BST pins are in test mode they will remain in BST mode until the internal BST state machine reaches the "logic reset" state. At this point the BST pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set to logical HIGH.

The Program fuse determines whether the device is in Dedicated Test or Flexible mode. The default (fuse not programmed) is Flexible mode.

Development Tool Support

The SX-A devices are fully supported by Actel's line of FPGA development tools, including the Actel Designer Series suite and Libero, the FPGA design tool suite. Designer Series, Actel's suite of FPGA development tools for PCs and Workstations, includes the ACTgen Macro Builder, timing driven place-and-route, timing analysis tools, and fuse file generation. Libero is a design management environment that integrates the needed design tools, streamlines the design flow, manages all design and log files, and passes necessary design data between tools. Libero includes, Synplify, ViewDraw, Actel's Designer Series, ModelSim HDL Simulator, WaveFormer Lite, and Actel Silicon Explorer.

In addition, the SX-A devices contain internal probe circuitry that provides built-in access to the output of every C-cell, R-cell, and routed clock in the design, enabling 100-percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy-to-use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to only a few seconds.

SX-A Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 10 on page 11 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification. The TRST pin is equipped with an internal pull-up resistor. To remove the boundary scan state machine from the reset state during probing, it is recommended that the TRST pin be left floating.

Design Considerations

For prototyping, the TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the security fuse should not be programmed during prototyping because doing so disables the probe circuitry.

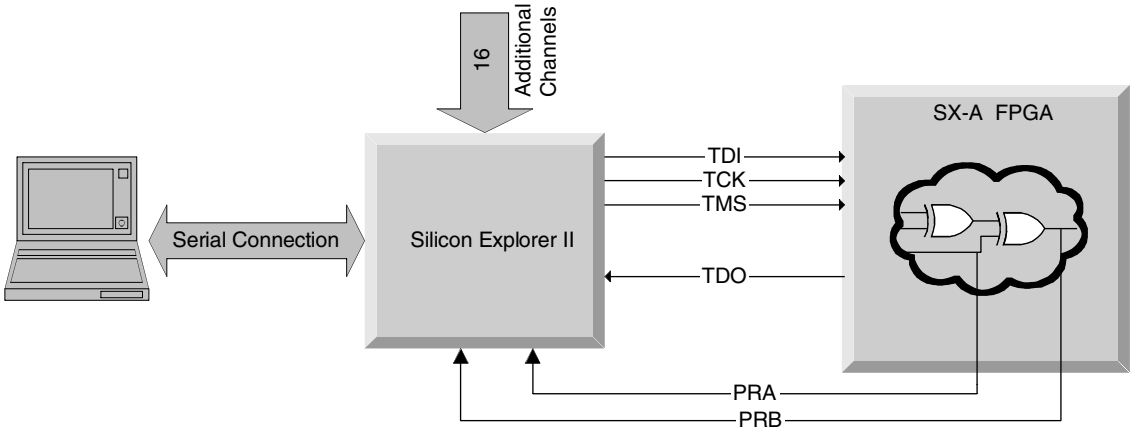


Figure 10 • Probe Setup

2.5V/3.3V/5.0V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to +V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
2.5V Power Supply Range	2.25 to 2.75	2.25 to 2.75	2.25 to 2.75	V_{CCI}
3.3V Power Supply Range	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V_{CCI}
5.0V Power Supply Range	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	V_{CCI}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

3.3V and 5.0V Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Units
V_{OH}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -1mA)	0.9 V_{CCI}		0.9 V_{CCI}		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -8mA)	2.4		2.4		V
V_{OL}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1mA)		0.1 V_{CCI}		0.1 V_{CCI}	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 12mA)		0.4		0.4	V
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0		2.0		V
I_{IL}/ I_{IH}	Input Leakage Current, V_{IN} = V_{CCI} or GND		–10	10	–10	10	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve[1]	Can be derived from the IBIS model on the web.						

Note:

1. The IBIS model can be found at www.actel.com/support/support/support_ibis.html.

2.5V Electrical Specifications

Symbol	Parameter		Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Units
V_{OH}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -100µA)	2.1		2.1		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -1 mA)	2.0		2.0		V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OH} = -2 mA)	1.7		1.7		V
V_{OL}	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 100µA)		0.2		0.2	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 1mA)		0.4		0.4	V
	V_{DD} = MIN, $V_I = V_{IH}$ or V_{IL}	(I_{OL}= 2 mA)		0.7		0.7	V
V_{IL}	Input Low Voltage, $V_{OUT} \le V_{VOL(max)}$		-0.3	0.7	-0.3	0.7	V
V_{IH}	Input High Voltage, $V_{OUT} \ge V_{VOH(min)}$		1.7	V_{DD} + 0.3	1.7	V_{DD} + 0.3	V
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND		–10	10	–10	10	µA
t_R, t_F	Input Transition Time t_R, t_F			10		10	ns
C_{IO}	I/O Capacitance			10		10	pF
I_{CC}	Standby Current			10		20	mA
IV Curve[1]	Can be derived from the IBIS model on the web.						

Note:

1. The IBIS model can be found at www.actel.com/support/support/support_ibis.html.

PCI Compliance for the SX-A Family

The SX-A family supports 3.3V and 5.0V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (5.0V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
I_{IH}	Input High Leakage Current[1]	V_{IN} = 2.7		70	µA
I_{IL}	Input Low Leakage Current[1]	V_{IN} = 0.5		–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter includes, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

AC Specifications (5.0V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$ [1]	–44		mA
		$1.4 \le V_{OUT} < 2.4$ [1, 2]	$(–44 + (V_{OUT} – 1.4)/0.024)$		mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]		Equation A on page 15	
	(Test Point)	$V_{OUT} = 3.1$ [3]		–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \ge 2.2$ [1]	95		mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$		mA
		$0.71 > V_{OUT} > 0$ [1, 3]		Equation B on page 15	
	(Test Point)	$V_{OUT} = 0.71$ [3]		206	mA
I_{CL}	Low Clamp Current	$–5 < V_{IN} \le –1$	$–25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4V to 2.4V load [4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4V to 0.4V load [4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 11 on page 15. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 11 on page 15. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*

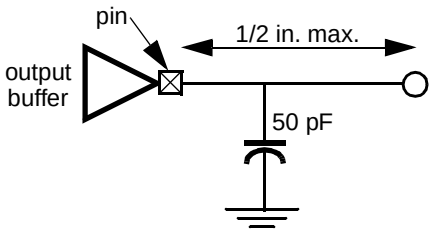


Figure 11 shows the 5.0V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

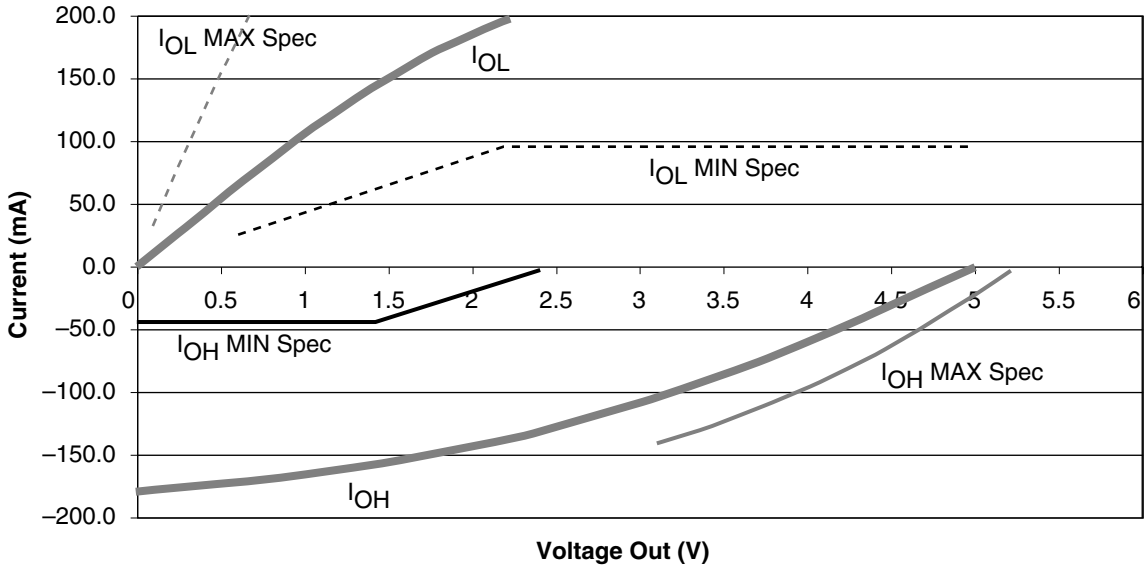


Figure 11 • *5.0V PCI V/I Curve for SX-A Family*

Equation A

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$
$$\text{for } V_{CCI} > V_{OUT} > 3.1V$$

Equation B

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.71V$$

DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CCI}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$	–10	+10	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{CCI}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

AC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$ [1]	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ [1]	$(-17.1 + (V_{CCI} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2]		Equation C on page 17	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ [1]	$16V_{CCI}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$ [1, 2]		Equation D on page 17	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load [3]	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load [3]	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 12 on page 17. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 12 on page 17. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

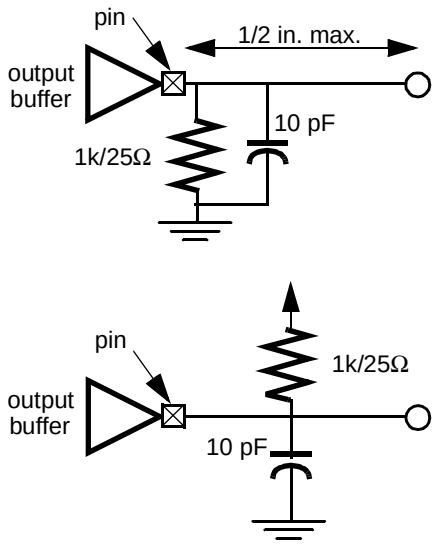


Figure 12 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

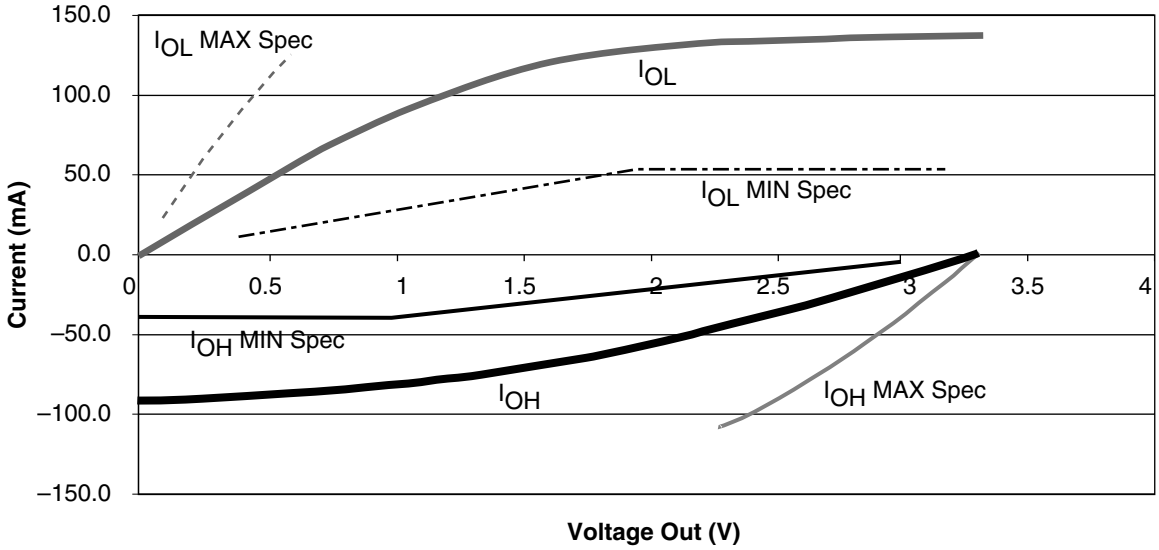


Figure 12 • *3.3V PCI V/I Curve for SX-A Family*

Equation C

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$
$$\text{for } 0.7\,V_{CCI} < V_{OUT} < V_{CCI}$$

Equation D

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.18\,V_{CCI}$$

Junction Temperature (T_J)

The temperature variable in the Designer Series software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Equation 9, shown below, can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (9)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P \quad (10)$$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the Package Thermal Characteristics table below.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

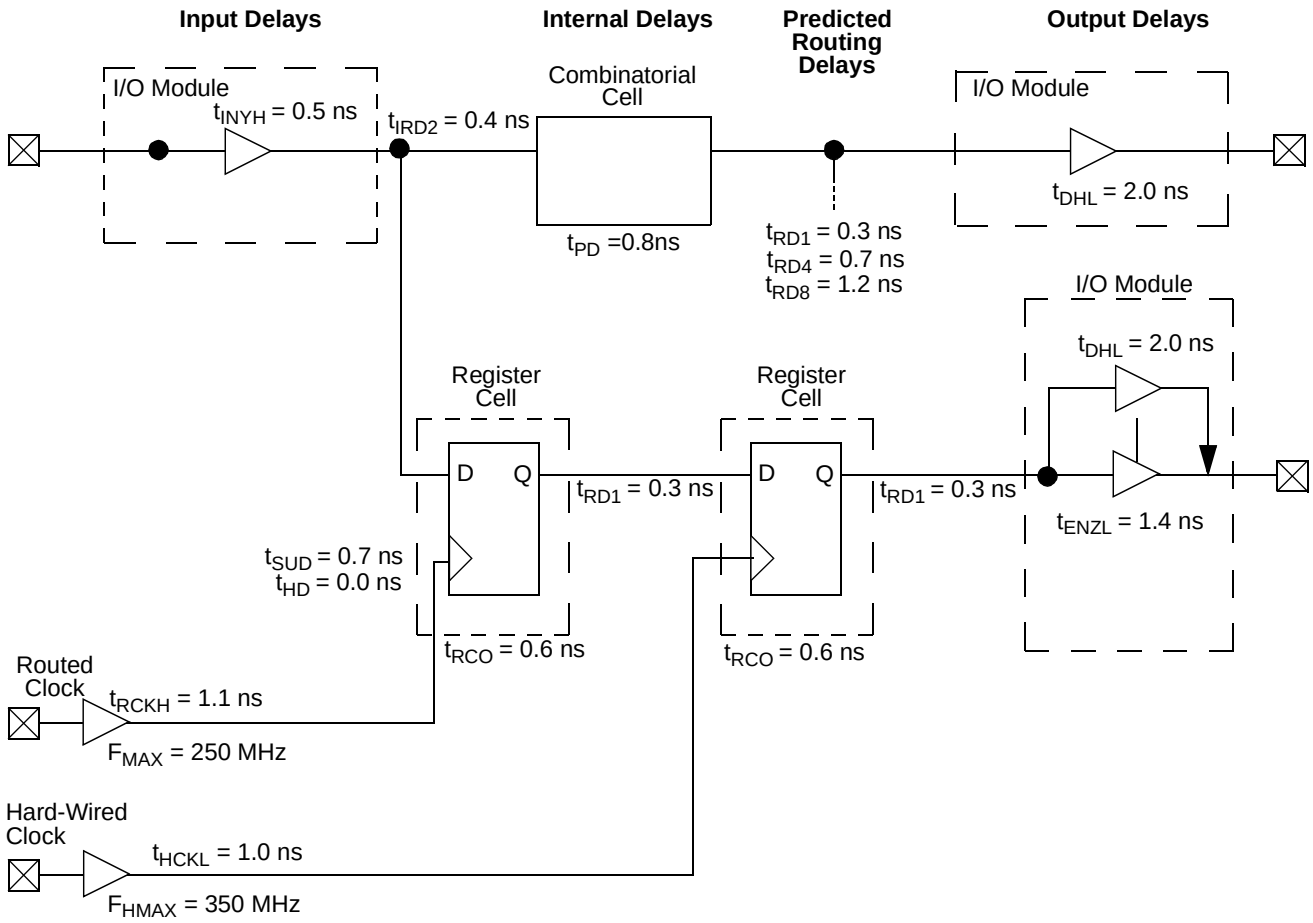
$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{28\text{°C/W}} = 2.86\text{W}$$

Package Thermal Characteristics

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Thin Quad Flat Pack (TQFP)	100	12	37.5	30	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader[2]	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.3	30	25	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3	20	15	°C/W

1. *The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.*
2. *The A54SX08A PQ208 has no heat spreader.*

SX-A Timing Model*



**Values shown for A54SX08A–3, worst-case commercial conditions at 3.3V PCI, with standard place-and-route.*

Hard-Wired Clock

External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{HCKL}$
= 0.5 + 0.3 + 0.7 – 1.0 = 0.5 ns

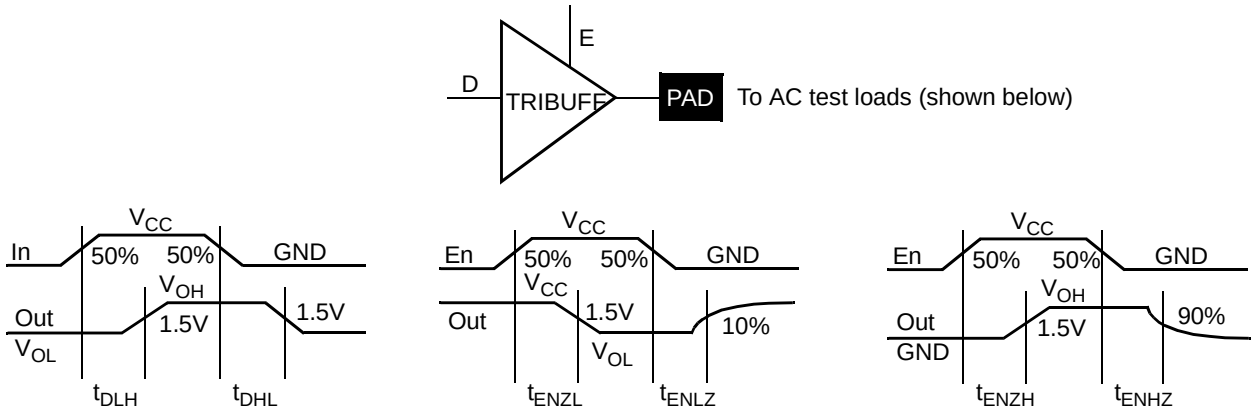
Clock-to-Out (Pad-to-Pad)
= $t_{HCKL} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.0 + 0.6 + 0.3 + 2.0= 3.9 ns

Routed Clock

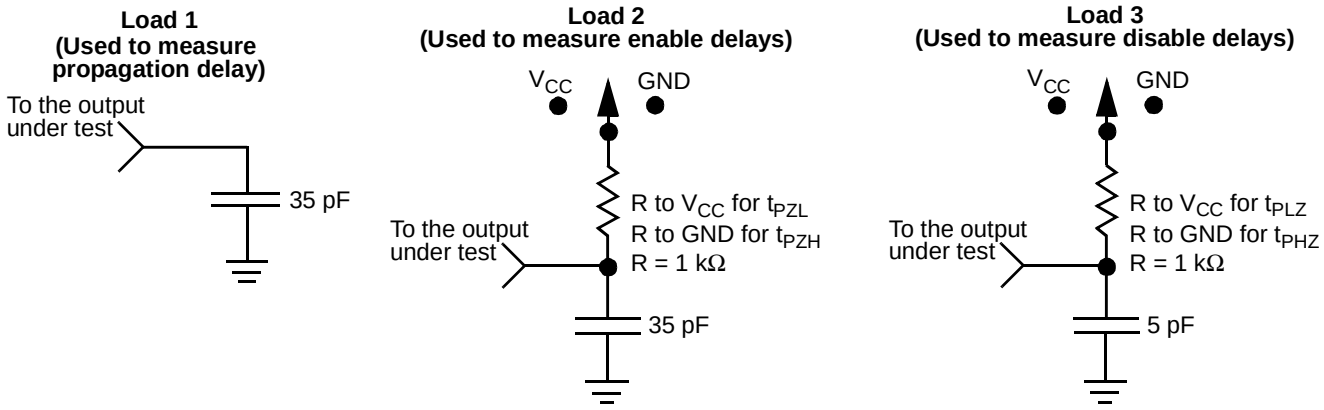
External Setup = $(t_{INYH} + t_{RD1} + t_{SUD}) - t_{RCKH}$
= 0.5 + 0.3 + 0.7– 1.1= 0.4 ns

Clock-to-Out (Pad-to-Pad)
= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.1+ 0.6 + 0.3 + 2.0 = 4.0 ns

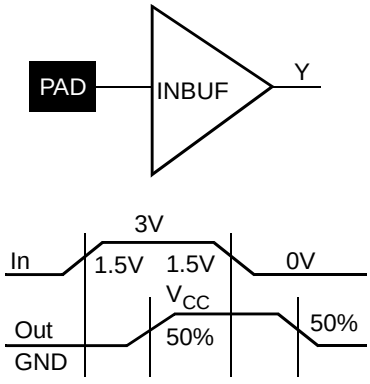
Output Buffer Delays



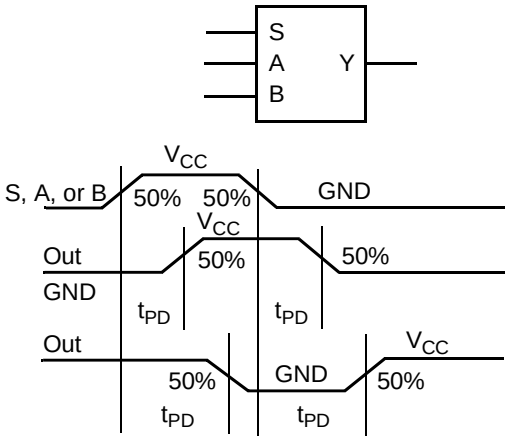
AC Test Loads



Input Buffer Delays

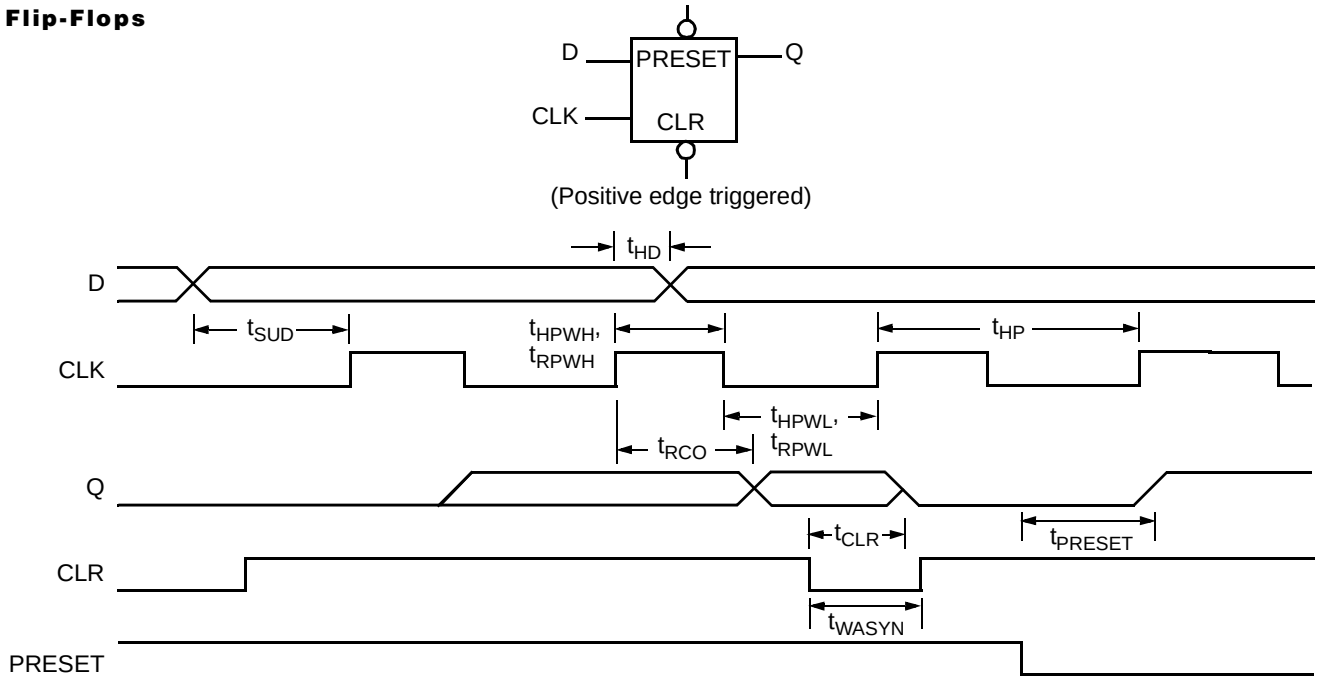


C-Cell Delays



Cell Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

(Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.3V)

	Junction Temperature (T_J)						
V_{CCA}	–55°C	–40°C	0°C	25°C	70°C	85°C	125°C
2.3V	0.75	0.79	0.88	0.89	1.00	1.04	1.16
2.5V	0.70	0.74	0.82	0.83	0.93	0.97	1.08
2.7V	0.66	0.69	0.79	0.79	0.88	0.92	1.02

A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]												
t_{PD}	Internal Array Module		0.8		1.0		1.1		1.3		1.8	ns
Predicted Routing Delays[2]												
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.7		0.8		0.9		1.1		1.6	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.1		1.6	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.1		1.6		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad-to-Y HIGH		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.0		1.0		1.3		1.8	ns
Input Module Predicted Routing Delays[2]												
t_{IRD1}	FO=1 Routing Delay		0.3		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.3		1.5		1.8		2.4	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.2		1.4		1.6		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.2		0.3		0.4	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.1		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.3		1.4		1.6		1.9		2.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.4		1.6		1.9		2.2		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.5		1.7		2.0		2.3		3.1	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.3		0.3		0.3		0.3		0.4	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.3		0.3		0.4		0.4		0.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.3		0.3		0.4		0.4		0.7	ns

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.2		1.4		1.6		2.4	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.0		1.2		1.3		1.5		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.2		0.3		0.4	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.3		1.4		1.7		2.0		2.8	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.1		1.3		1.5		1.8		2.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.4		1.5		1.9		2.2		3.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.5		1.6		2.0		2.3		3.4	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.4		0.4	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.3		0.3		0.4		0.4		0.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.3		0.3		0.4		0.4		0.7	ns

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.0		1.2		1.4		1.5		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.0		1.1		1.3		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.2		0.3		0.4	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.0		1.1		1.2		1.5		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.1		1.3		1.5		1.8		2.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.3		1.6		1.9		2.1		3.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.4		1.7		2.0		2.2		3.2	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.4		0.4	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.3		0.3		0.4		0.4		0.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.3		0.3		0.4		0.4		0.7	ns

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5V LVTTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		3.2		3.8		4.3		5.0		7.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.0		3.4		4.0		5.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		11.3		13.0		14.8		17.4		24.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.0		4.5		5.3		7.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0		4.5		5.3		7.5	ns
d_{TLH}	Delta LOW to HIGH		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}	Delta HIGH to LOW		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.057		0.060		0.071		0.086		0.117	ns/pF

Note:

1. Delays based on 35 pF loading.

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.3		2.6		3.0		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.0		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.4		1.7		1.9		2.2		3.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d_{TLH}[3]	Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3V LVTTL Output Module Timing[2]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.7		3.2		3.6		4.2		5.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.5		2.8		3.2		3.8		5.3	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		9.0		10.4		11.8		13.8		19.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.9		3.3		3.7		4.4		6.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d_{TLH}	Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}	Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *Delays based on 10 pF loading and 25Ω resistance.*
2. *Delays based on 35 pF loading.*

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5.0V PCI Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.1		3.5		4.2		5.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		7.4		8.5		9.6		11.3		15.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		3.5		5.1		5.9		6.9		9.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.3		1.5		1.7		2.0		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.5		3.9		4.6		6.4	ns
d_{TLH}[3]	Delta LOW to HIGH		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta HIGH to LOW		0.026		0.03		0.032		0.04		0.052	ns/pF
d_{THLS}[3]	Delta HIGH to LOW—low slew		0.04		0.052		0.06		0.07		0.096	ns/pF
5.0V TTL Output Module Timing[2]												
t_{DLH}	Data-to-Pad LOW to HIGH		1.9		2.2		2.5		3.0		4.2	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.5		2.9		3.3		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		6.6		7.6		8.6		10.2		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.5		3.9		4.6		6.4	ns
d_{TLH}	Delta LOW to HIGH		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}	Delta HIGH to LOW		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *Delays based on 35 pF loading*

A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]												
t_{PD}	Internal Array Module		0.8		1.0		1.1		1.3		1.8	ns
Predicted Routing Delays[2]												
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.7		0.8		0.9		1.1		1.6	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.1		1.6	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.1		1.6		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad-to-Y HIGH		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.0		1.0		1.3		1.8	ns
Input Module Predicted Routing Delays[2]												
t_{IRD1}	FO=1 Routing Delay		0.3		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.4		1.5		0.8		2.5	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.5		1.6		1.9		2.9	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.4		1.5		1.8		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.1		0.1		0.1		0.1		0.2	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.2		1.3		1.5		1.8		2.5	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.5		1.7		2.0		2.3		3.3	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.7		1.9		2.2		2.6		3.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.8		2.0		2.3		2.7		3.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.3		0.4		0.4		0.4		0.6	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8		1.3	ns

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.5		1.6		1.9		2.9	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.4		1.5		1.8		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.1		0.1		0.1		0.1		0.2	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.2		1.3		1.5		1.8		2.4	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.3		1.4		1.7		2.0		2.8	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.5		1.7		2.0		2.3		3.3	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.7		1.9		2.2		2.6		3.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.8		2.0		2.3		2.7		3.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.3		0.4		0.4		0.4		0.6	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8		1.3	ns

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.3		1.5		1.7		2.7	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.1		0.1		0.1		0.1		0.2	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.1		1.2		1.4		1.7		2.3	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.4		1.6		1.8		2.2		3.1	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.5		1.7		1.9		2.3		3.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.3		0.4		0.4		0.4		0.6	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8		1.3	ns

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5V LVTTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		3.2		3.8		4.3		5.0		7.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.0		3.4		4.0		5.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		11.3		13.0		14.8		17.4		24.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.0		4.5		5.3		7.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0		4.5		5.3		7.5	ns
d_{TLH}	Delta LOW to HIGH		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}	Delta HIGH to LOW		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.057		0.060		0.071		0.086		0.117	ns/pF

Note:

1. Delays based on 35 pF loading.

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.3		2.6		3.0		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.0		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.4		1.7		1.9		2.2		3.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d_{TLH}[3]	Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3V LVTTL Output Module Timing[2]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.7		3.2		3.6		4.2		5.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.5		2.8		3.2		3.8		5.3	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		9.0		10.4		11.8		13.8		19.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.9		3.3		3.7		4.4		6.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d_{TLH}	Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}	Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *Delays based on 10 pF loading and 25Ω resistance.*
2. *Delays based on 35 pF loading.*

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5.0V PCI Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.73		3.1		3.5		4.2		5.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		7.4		8.5		9.6		11.3		15.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		3.5		5.1		5.9		6.9		9.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.3		1.5		1.7		2.0		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.5		3.9		4.6		6.4	ns
d_{TLH}[3]	Delta LOW to HIGH		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta HIGH to LOW		0.026		0.03		0.032		0.04		0.052	ns/pF
d_{THLS}[3]	Delta HIGH to LOW—low slew		0.04		0.052		0.06		0.07		0.096	ns/pF
5.0V TTL Output Module Timing[2]												
t_{DLH}	Data-to-Pad LOW to HIGH		1.9		2.2		2.5		3.0		4.2	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.5		2.9		3.3		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		6.6		7.6		8.6		10.2		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.5		3.9		4.6		6.4	ns
d_{TLH}	Delta LOW to HIGH		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}	Delta HIGH to LOW		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *Delays based on 35 pF loading.*

A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]												
t_{PD}	Internal Array Module		0.8		1.0		1.1		1.3		1.8	ns
Predicted Routing Delays[2]												
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{RD4}	FO=4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.7		0.8		0.9		1.1		1.6	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.1		1.6	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.1		1.6		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad-to-Y HIGH		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.0		1.0		1.3		1.8	ns
Input Module Predicted Routing Delays[2]												
t_{IRD1}	FO=1 Routing Delay		0.3		0.3		0.3		0.4		0.6	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.5		0.5		0.6		0.8	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.6		0.7		0.8		1.1	ns
t_{IRD4}	FO=4 Routing Delay		0.7		0.8		0.9		1.0		1.4	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.4		1.5		1.8		2.5	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.0		2.2		2.6		3.6	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		2.0		2.3		2.7		4.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.5		1.7		1.9		2.3		3.5	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5		0.8	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.7		2.0		2.2		2.6		3.7	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.1		2.4		2.8		3.2		4.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.3		2.5		2.9		3.4		5.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.9		1.0		1.1		1.3		2.2	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.3		1.5		1.7		2.0		3.4	ns

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		2.0		2.3		2.7		4.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.5		1.7		1.9		2.3		3.5	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5		0.8	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.7		2.0		2.2		2.6		3.7	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.1		2.4		2.8		3.3		4.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.1		2.4		2.8		3.2		4.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.3		2.5		2.9		3.4		5.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.9		1.0		1.1		1.3		2.2	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.3		1.5		1.7		2.0		3.4	ns

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		1.9		2.3		2.6		4.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.5		1.7		1.9		2.2		3.5	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5		0.8	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.0		2.4		2.7		3.1		4.4	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.0		2.4		2.7		3.1		2.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.2		2.5		2.8		3.3		5.5	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.9		1.0		1.1		1.3		2.0	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.3		1.5		1.7		2.0		3.4	ns

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5V LVTTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		3.2		3.8		4.3		5.0		7.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.0		3.4		4.0		5.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		11.3		13.0		14.8		17.4		24.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.0		4.5		5.3		7.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0		4.5		5.3		7.5	ns
d_{TLH}	Delta LOW to HIGH		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}	Delta HIGH to LOW		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.057		0.060		0.071		0.086		0.117	ns/pF

Note:

1. Delays based on 35 pF loading.

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.3		2.6		3.0		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.0		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.4		1.7		1.9		2.2		3.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d_{TLH}[3]	Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3V LVTTL Output Module Timing[2]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.7		3.2		3.6		4.2		5.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.5		2.8		3.2		3.8		5.3	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		9.0		10.4		11.8		13.8		19.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.9		3.3		3.7		4.4		6.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d_{TLH}	Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}	Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *Delays based on 10 pF loading and 25Ω resistance.*
2. *Delays based on 35 pF loading.*

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5.0V PCI Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.1		3.5		4.2		5.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		7.4		8.5		9.6		11.3		15.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		3.5		5.1		5.9		6.9		9.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.3		1.5		1.7		2.0		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.5		3.9		4.6		6.4	ns
d_{TLH}[3]	Delta LOW to HIGH		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta HIGH to LOW		0.026		0.03		0.032		0.04		0.052	ns/pF
d_{THLS}[3]	Delta HIGH to LOW—low slew		0.04		0.052		0.06		0.07		0.096	ns/pF
5.0V TTL Output Module Timing[2]												
t_{DLH}	Data-to-Pad LOW to HIGH		1.9		2.2		2.5		3.0		4.2	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.5		2.9		3.3		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		6.6		7.6		8.6		10.2		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.5		3.9		4.6		6.4	ns
d_{TLH}	Delta LOW to HIGH		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}	Delta HIGH to LOW		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *Delays based on 35 pF loading.*

A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]												
t_{PD}	Internal Array Module		0.8		1.0		1.1		1.3		1.8	ns
Predicted Routing Delays[2]												
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.3		0.3		0.4		0.6	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{RD2}	FO=2 Routing Delay		0.4		0.5		0.6		0.7		1.0	ns
t_{RD3}	FO=3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{RD4}	FO=4 Routing Delay		0.7		0.9		1.0		1.1		1.5	ns
t_{RD8}	FO=8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{RD12}	FO=12 Routing Delay		1.7		2.2		2.5		3.0		4.2	ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q		0.6		0.7		0.8		0.9		1.3	ns
t_{CLR}	Asynchronous Clear-to-Q		0.7		0.8		0.9		1.1		1.6	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.1		1.6	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.1		1.6		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad-to-Y HIGH		0.5		0.6		0.7		0.8		1.1	ns
t_{INYL}	Input Data Pad-to-Y LOW		0.8		1.0		1.0		1.3		1.8	ns
Input Module Predicted Routing Delays[2]												
t_{IRD1}	FO=1 Routing Delay		0.3		0.3		0.4		0.5		0.7	ns
t_{IRD2}	FO=2 Routing Delay		0.4		0.5		0.6		0.7		1.0	ns
t_{IRD3}	FO=3 Routing Delay		0.5		0.7		0.8		0.9		1.3	ns
t_{IRD4}	FO=4 Routing Delay		0.7		0.9		1.0		1.1		1.5	ns
t_{IRD8}	FO=8 Routing Delay		1.2		1.5		1.7		2.1		2.9	ns
t_{IRD12}	FO=12 Routing Delay		1.7		2.2		2.5		3.0		4.2	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.5		1.7		2.1		3.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.3		1.5		1.9		2.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.7		0.8		0.9		1.0		1.6	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.3		2.6		2.9		3.5		4.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.6		3.1		3.4		4.0		5.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.0		3.5		3.9		4.6		6.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.3		3.8		4.2		4.9		7.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.7		4.3		4.8		5.7		8.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.0		4.6		5.1		6.0		8.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.8		2.1		2.4		2.7		3.8	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.4		1.5		1.7		2.0		3.4	ns

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.5		1.7		2.1		3.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.3		1.5		1.9		2.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.7		0.8		0.9		1.0		1.6	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.2		2.6		2.9		3.5		4.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.7		3.1		3.5		4.1		5.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.0		3.5		3.9		4.6		6.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.3		3.8		4.2		4.9		7.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.7		4.3		4.8		5.7		8.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.0		4.6		5.1		6.0		8.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.8		2.1		2.4		2.7		3.8	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.4		1.5		1.7		2.0		3.4	ns

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.4		1.7		2.0		3.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.2		1.5		1.8		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.7		0.8		0.9		1.0		1.6	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.2		2.5		2.8		3.4		4.6	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.0		3.5		3.9		4.6		6.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.3		3.8		4.2		4.9		7.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.7		4.3		4.8		5.7		8.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.0		4.6		5.1		6.0		8.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.8		2.1		2.4		2.7		3.8	ns
t_{RCKSW}	Maximum Skew (50% Load)				1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)				1.5		1.7		2.0		3.4	ns

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 2.3V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
2.5V LVTTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		3.3		3.9		4.4		5.2		7.2	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.0		3.4		4.0		5.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		11.7		13.5		15.3		18.0		25.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.0		4.5		5.3		7.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0		4.5		5.3		7.5	ns
d_{TLH}	Delta LOW to HIGH		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}	Delta HIGH to LOW		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.057		0.060		0.071		0.086		0.117	ns/pF

Note:

1. Delays based on 35 pF loading.

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.0		2.3		2.6		3.0		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.0		4.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.4		1.7		1.9		2.2		3.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d_{TLH}[3]	Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}[3]	Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3V LVTTL Output Module Timing[2]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.7		3.2		3.6		4.2		5.9	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.5		2.8		3.2		3.8		5.3	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		9.0		10.4		11.8		13.8		19.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.9		3.3		3.7		4.4		6.2	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d_{TLH}	Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d_{THL}	Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. *Delays based on 10 pF loading and 25Ω resistance.*
2. *Delays based on 35 pF loading.*

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions V_{CCA} = 2.3V, V_{CCI} = 4.75V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
5.0V PCI Output Module Timing[1]												
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3		4.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.7		3.1		3.5		4.2		5.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		7.4		8.5		9.6		11.3		15.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.3		1.5		1.7		2.0		2.8	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		3.5		5.1		5.9		6.9		9.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.3		1.5		1.7		2.0		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.0		3.5		3.9		4.6		6.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.5		3.9		4.6		6.4	ns
d_{TLH}[3]	Delta LOW to HIGH		0.016		0.016		0.02		0.022		0.032	ns/pF
d_{THL}[3]	Delta HIGH to LOW		0.026		0.03		0.032		0.04		0.052	ns/pF
d_{THLS}[3]	Delta HIGH to LOW—low slew		0.04		0.052		0.06		0.07		0.096	ns/pF
5.0V TTL Output Module Timing[2]												
t_{DLH}	Data-to-Pad LOW to HIGH		1.9		2.2		2.5		3.0		4.2	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.5		2.9		3.3		3.9		5.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		6.6		7.6		8.6		10.2		14.2	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.7		3.2		4.5	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4		8.4		9.5		11.0		15.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.6		4.2		4.7		5.6		7.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.0		3.5		3.9		4.6		6.4	ns
d_{TLH}	Delta LOW to HIGH		0.014		0.017		0.017		0.023		0.031	ns/pF
d_{THL}	Delta HIGH to LOW		0.023		0.029		0.031		0.037		0.051	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.043		0.046		0.057		0.066		0.089	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *Delays based on 35 pF loading.*

Pin Description

CLKA/B Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as user I/O.)

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only for A54SX72A. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. If not used as a clock it will behave as a regular I/O.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O Probe A/B
PRB, I/O

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 3 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 3 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 3 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 3 on page 10). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the "Reserve JTAG Reset Pin" is not selected in Designer.

V_{CCI} Supply Voltage

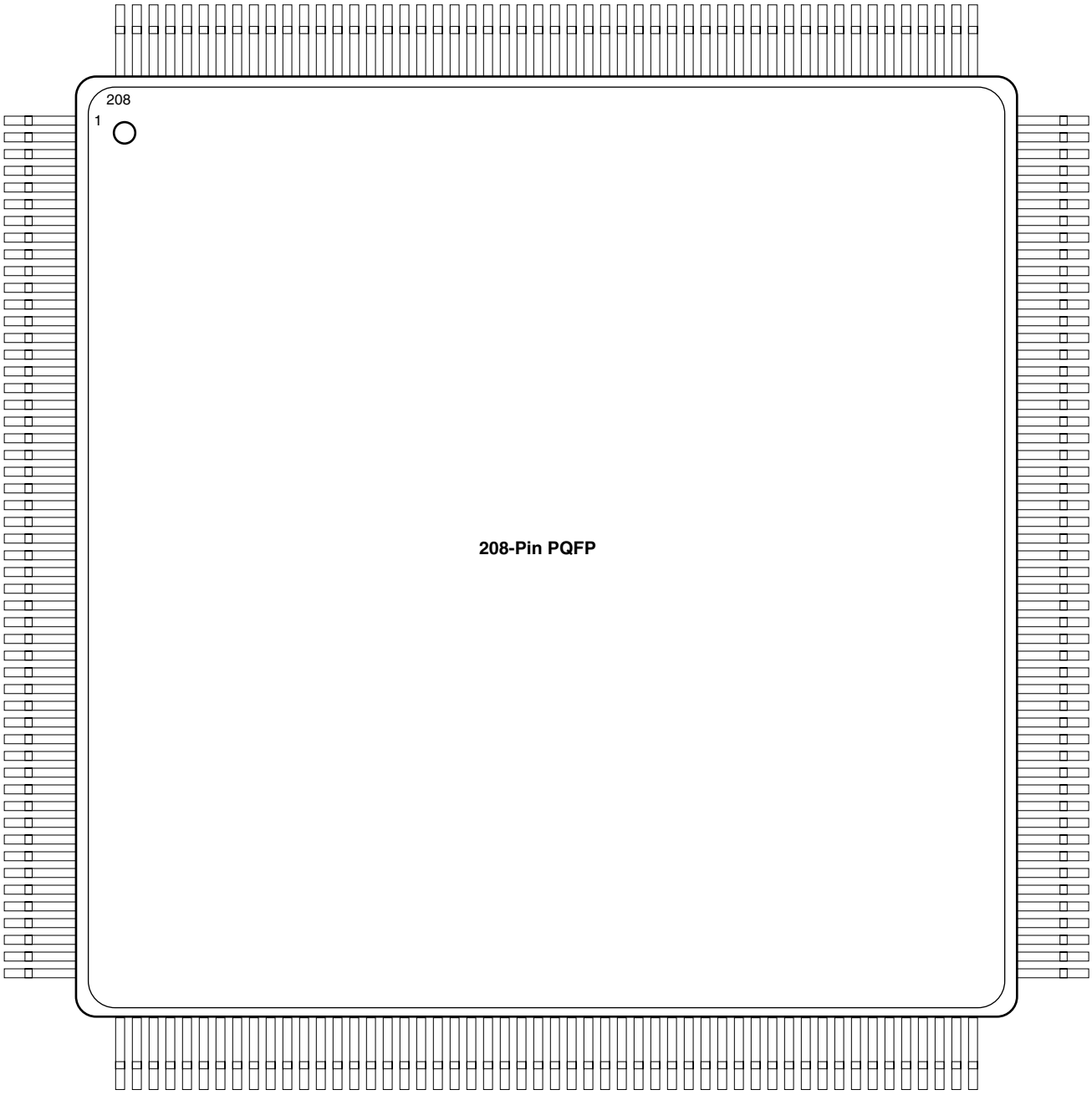
Supply voltage for I/Os. See Table 2 on page 9.

V_{CCA} Supply Voltage

Supply voltage for Array. See Table 2 on page 9.

Package Pin Assignments

208-Pin PQFP (Top View)



208-Pin PQFP

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V_{CCA}
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O

208-Pin PQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O
73	NC	I/O	I/O	I/O
74	I/O	I/O	I/O	QCLKA
75	NC	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB,I/O
77	GND	GND	GND	GND
78	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND	GND
80	NC	NC	NC	NC
81	I/O	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	HCLK
83	I/O	I/O	I/O	V_{CCI}
84	I/O	I/O	I/O	QCLKB
85	NC	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	NC	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	I/O	I/O	I/O	I/O
91	NC	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O

208-Pin PQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
93	I/O	I/O	I/O	I/O
94	NC	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	I/O	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O	I/O
105	GND	GND	GND	GND
106	NC	I/O	I/O	I/O
107	I/O	I/O	I/O	I/O
108	NC	I/O	I/O	I/O
109	I/O	I/O	I/O	I/O
110	I/O	I/O	I/O	I/O
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
116	NC	I/O	I/O	GND
117	I/O	I/O	I/O	V_{CCA}
118	I/O	I/O	I/O	I/O
119	NC	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	NC	I/O	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	NC	I/O	I/O	I/O
126	I/O	I/O	I/O	I/O
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	GND	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND	GND
132	NC	NC	NC	I/O
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	NC	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	NC	I/O	I/O	I/O

208-Pin PQFP (Continued)

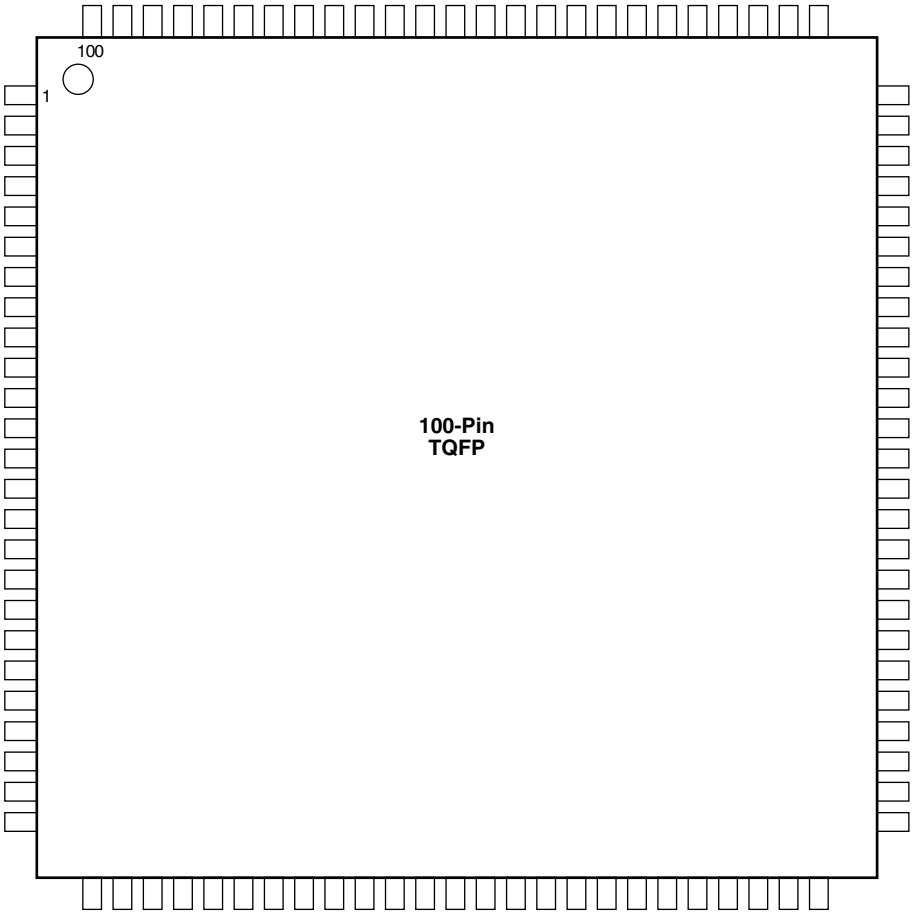
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}

208-Pin PQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V_{CCI}
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (Continued)

100-Pin TQFP (Top View)



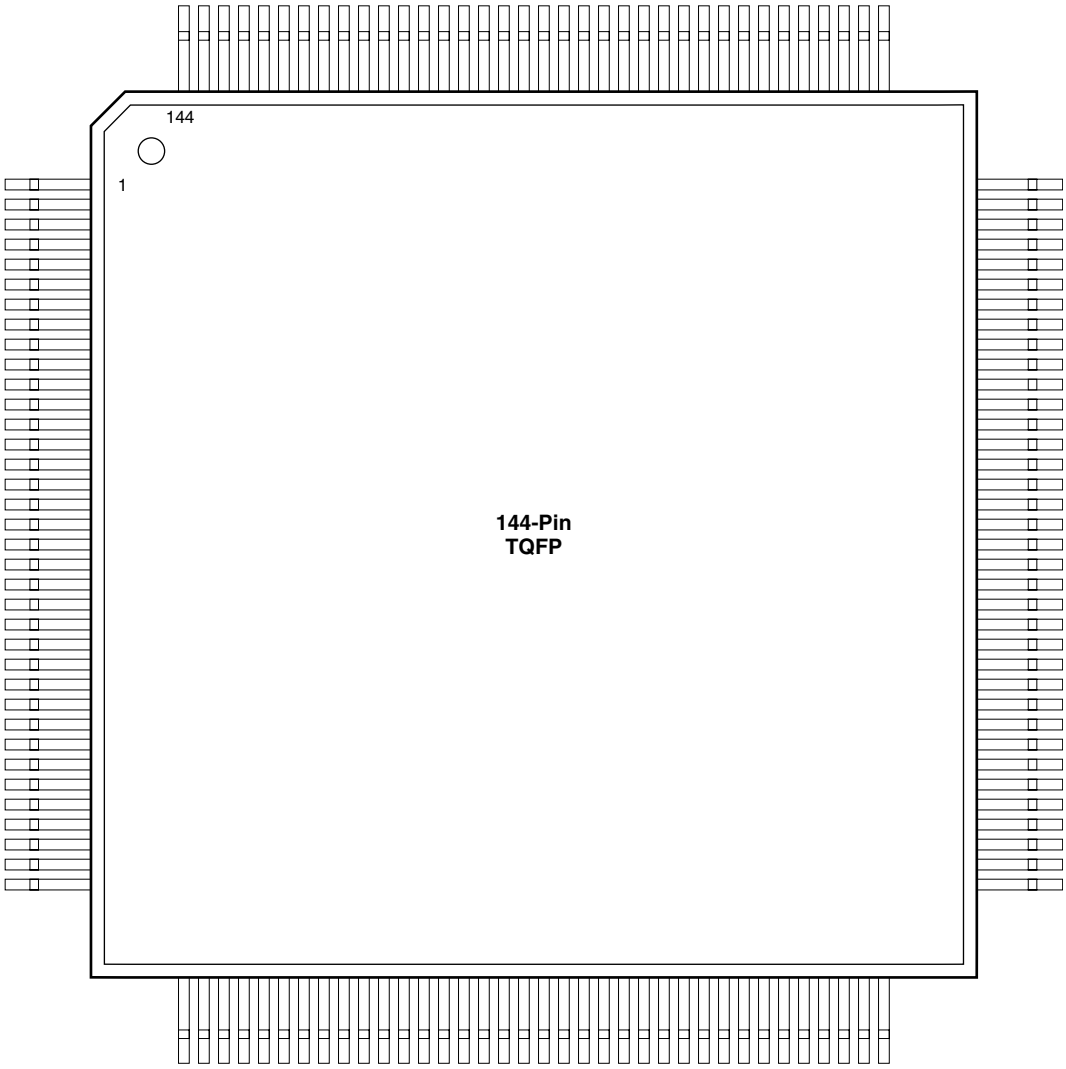
100-TQFP

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V_{CCI}	V_{CCI}	V_{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V_{CCI}	V_{CCI}	V_{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}	V_{CCA}
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V_{CCA}	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}	V_{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V_{CCA}	V_{CCA}	V_{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V_{CCA}	V_{CCA}	V_{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

144-Pin TQFP (Top View)



144-Pin TQFP

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V_{CCI}	V_{CCI}	V_{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	NC	NC	NC
20	V_{CCA}	V_{CCA}	V_{CCA}
21	I/O	I/O	I/O
22	TRST, I/O	TRST, I/O	TRST, I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V_{CCI}	V_{CCI}	V_{CCI}
30	V_{CCA}	V_{CCA}	V_{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V_{CCA}	V_{CCA}	V_{CCA}
57	GND	GND	GND
58	NC	NC	NC
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V_{CCI}	V_{CCI}	V_{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O

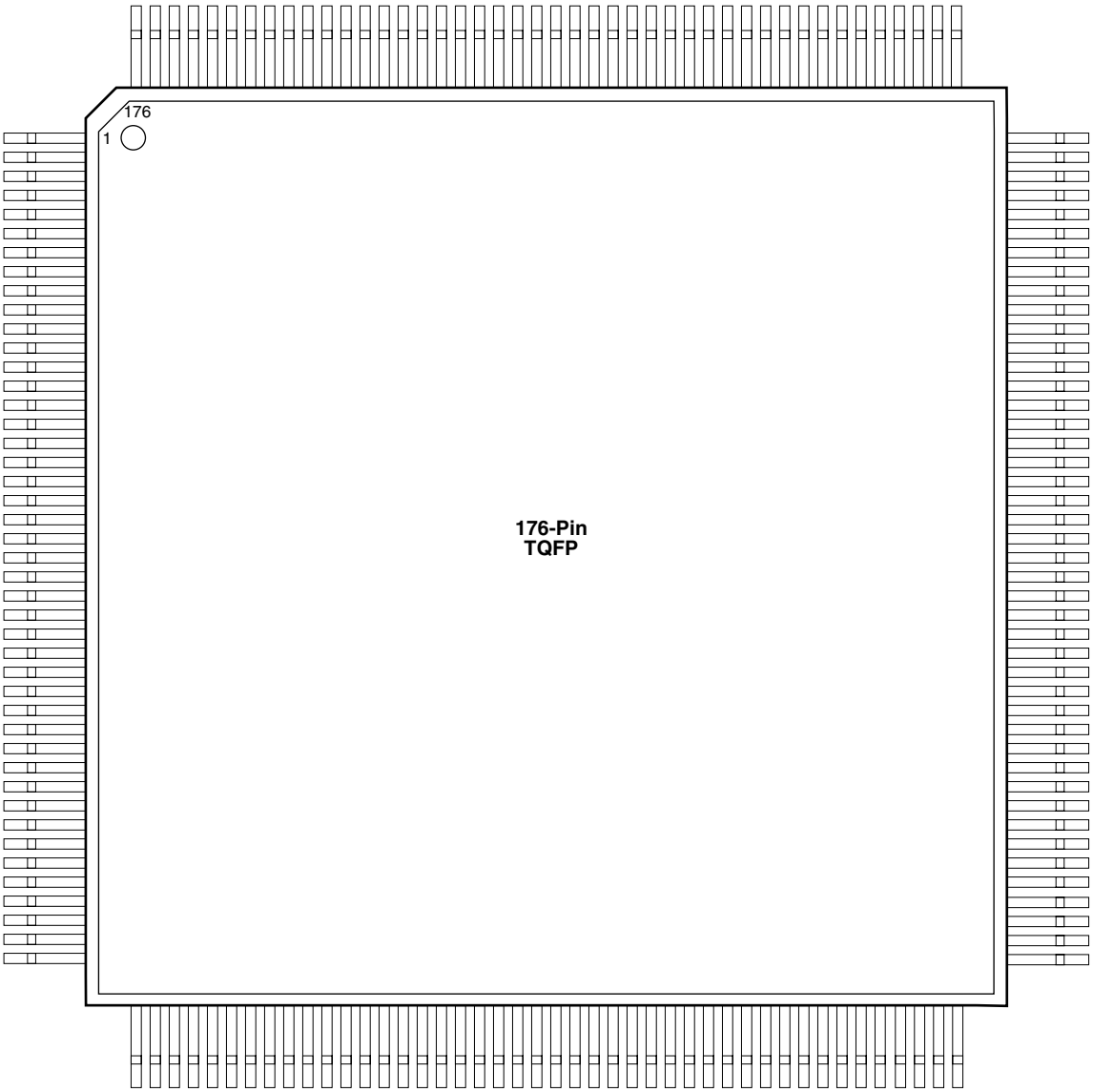
144-Pin TQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V_{CCA}	V_{CCA}	V_{CCA}
80	V_{CCI}	V_{CCI}	V_{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{CCA}	V_{CCA}	V_{CCA}
90	NC	NC	NC
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V_{CCI}	V_{CCI}	V_{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	NC	NC	NC
128	GND	GND	GND
129	V_{CCA}	V_{CCA}	V_{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (Continued)

176-Pin TQFP (Top View)

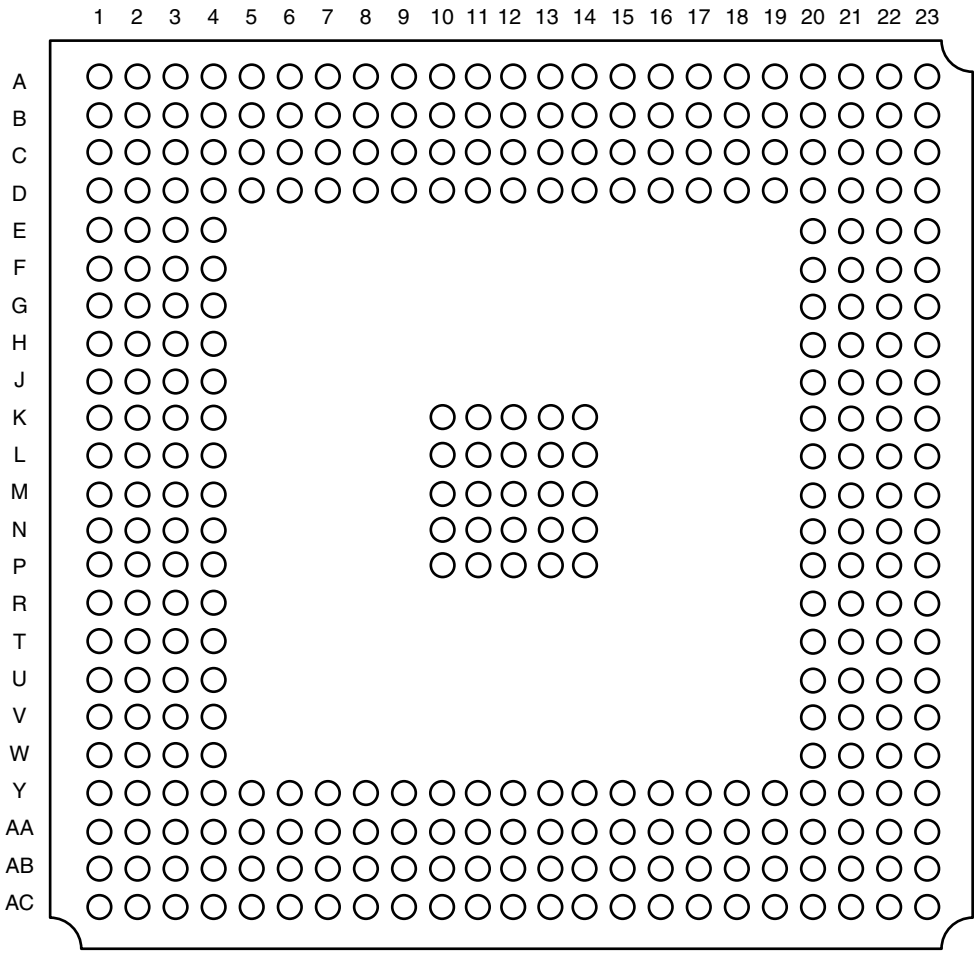


176-Pin TQFP

Pin Number	A54SX32A Function
1	GND
2	TDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	TMS
11	V_{CCI}
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND
22	V_{CCA}
23	GND
24	I/O
25	TRST, I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	V_{CCI}
33	V_{CCA}
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	GND
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	V_{CCI}
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	PRB, I/O
65	GND
66	V_{CCA}
67	NC
68	I/O
69	HCLK
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	V_{CCI}
83	I/O
84	I/O
85	I/O
86	I/O
87	TDO, I/O
88	I/O
89	GND
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	V_{CCA}
99	V_{CCI}
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	GND
109	V_{CCA}
110	GND
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	V_{CCA}
123	GND
124	V_{CCI}
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	GND
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	V_{CCI}
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	CLKA
153	CLKB
154	NC
155	GND
156	V_{CCA}
157	PRA, I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	V_{CCI}
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	TCK, I/O

Package Pin Assignments (Continued)

329-Pin PBGA (Top View)



329-Pin PBGA

Pin Number	A54SX32A Function
A1	GND
A2	GND
A3	V_{CCI}
A4	NC
A5	I/O
A6	I/O
A7	V_{CCI}
A8	NC
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	CLKB
A14	I/O
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	NC
A22	V_{CCI}
A23	GND
AA1	V_{CCI}
AA2	I/O
AA3	GND
AA4	I/O
AA5	I/O
AA6	I/O
AA7	I/O
AA8	I/O
AA9	I/O
AA10	I/O
AA11	I/O
AA12	I/O
AA13	I/O
AA14	I/O
AA15	I/O
AA16	I/O
AA17	I/O
AA18	I/O
AA19	I/O
AA20	TDO, I/O
AA21	V_{CCI}
AA22	I/O

Pin Number	A54SX32A Function
AA23	V_{CCI}
AB1	I/O
AB2	GND
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	PRB, I/O
AB12	I/O
AB13	HCLK
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	I/O
AB21	I/O
AB22	GND
AB23	I/O
AC1	GND
AC2	V_{CCI}
AC3	NC
AC4	I/O
AC5	I/O
AC6	I/O
AC7	I/O
AC8	I/O
AC9	V_{CCI}
AC10	I/O
AC11	I/O
AC12	I/O
AC13	I/O
AC14	I/O
AC15	NC
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	I/O
AC21	NC

Pin Number	A54SX32A Function
AC22	V_{CCI}
AC23	GND
B1	V_{CCI}
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	I/O
B11	I/O
B12	PRA, I/O
B13	CLKA
B14	I/O
B15	I/O
B16	I/O
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	GND
B23	V_{CCI}
C1	NC
C2	TDI, I/O
C3	GND
C4	I/O
C5	I/O
C6	I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O
C13	I/O
C14	I/O
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O

Pin Number	A54SX32A Function
C21	V_{CCI}
C22	GND
C23	NC
D1	I/O
D2	I/O
D3	I/O
D4	TCK, I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	V_{CCA}
D12	NC
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	I/O
D22	I/O
D23	I/O
E1	V_{CCI}
E2	I/O
E3	I/O
E4	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
F1	I/O
F2	TMS
F3	I/O
F4	I/O
F20	I/O
F21	I/O
F22	I/O
F23	I/O
G1	I/O
G2	I/O
G3	I/O

329-Pin PBGA (Continued)

Pin Number	A54SX32A Function
G4	I/O
G20	I/O
G21	I/O
G22	I/O
G23	GND
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H20	V_{CCA}
H21	I/O
H22	I/O
H23	I/O
J1	NC
J2	I/O
J3	I/O
J4	I/O
J20	I/O
J21	I/O
J22	I/O
J23	I/O
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K20	I/O
K21	I/O
K22	I/O
K23	I/O
L1	I/O
L2	I/O
L3	I/O
L4	NC
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND

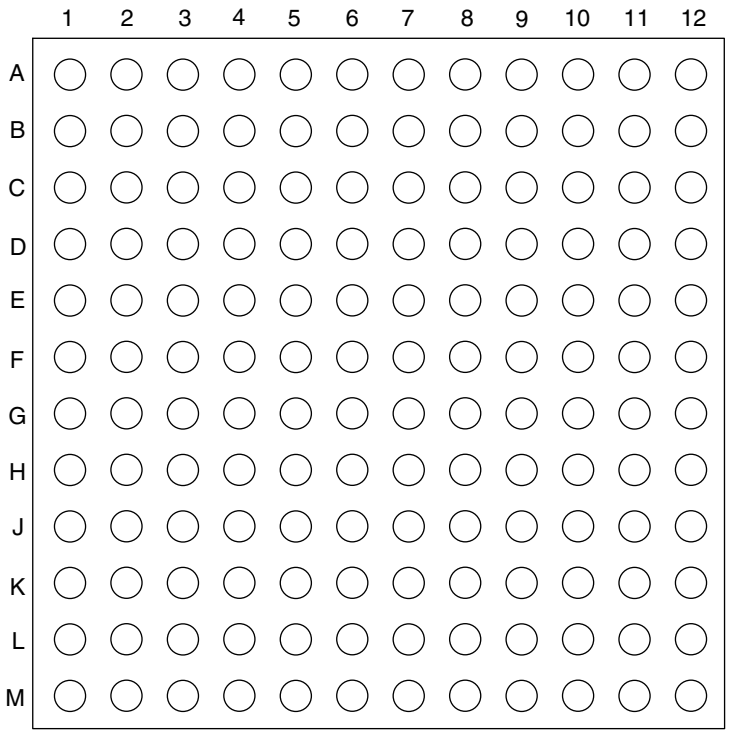
Pin Number	A54SX32A Function
L20	NC
L21	I/O
L22	I/O
L23	NC
M1	I/O
M2	I/O
M3	I/O
M4	V_{CCA}
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M20	V_{CCA}
M21	I/O
M22	I/O
M23	V_{CCI}
N1	I/O
N2	TRST, I/O
N3	I/O
N4	I/O
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N20	NC
N21	I/O
N22	I/O
N23	I/O
P1	I/O
P2	I/O
P3	I/O
P4	I/O
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P20	I/O
P21	I/O
P22	I/O
P23	I/O

Pin Number	A54SX32A Function
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R20	I/O
R21	I/O
R22	I/O
R23	I/O
T1	I/O
T2	I/O
T3	I/O
T4	I/O
T20	I/O
T21	I/O
T22	I/O
T23	I/O
U1	I/O
U2	I/O
U3	V_{CCA}
U4	I/O
U20	I/O
U21	V_{CCA}
U22	I/O
U23	I/O
V1	V_{CCI}
V2	I/O
V3	I/O
V4	I/O
V20	I/O
V21	I/O
V22	I/O
V23	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W20	I/O
W21	I/O
W22	I/O
W23	NC
Y1	NC
Y2	I/O
Y3	I/O

Pin Number	A54SX32A Function
Y4	GND
Y5	I/O
Y6	I/O
Y7	I/O
Y8	I/O
Y9	I/O
Y10	I/O
Y11	I/O
Y12	V_{CCA}
Y13	NC
Y14	I/O
Y15	I/O
Y16	I/O
Y17	I/O
Y18	I/O
Y19	I/O
Y20	GND
Y21	I/O
Y22	I/O
Y23	I/O

Package Pin Assignments (Continued)

144-Pin FBGA (Top View)



144-Pin FBGA

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
A1	I/O	I/O	I/O
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	V_{CCA}	V_{CCA}	V_{CCA}
A6	GND	GND	GND
A7	CLKA	CLKA	CLKA
A8	I/O	I/O	I/O
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	I/O	I/O	I/O
C3	TCK, I/O	TCK, I/O	TCK, I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	PRA, I/O	PRA, I/O	PRA, I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	V_{CCI}	V_{CCI}	V_{CCI}
D3	TDI, I/O	TDI, I/O	TDI, I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	TMS	TMS	TMS
E6	V_{CCI}	V_{CCI}	V_{CCI}
E7	V_{CCI}	V_{CCI}	V_{CCI}
E8	V_{CCI}	V_{CCI}	V_{CCI}
E9	V_{CCA}	V_{CCA}	V_{CCA}
E10	I/O	I/O	I/O
E11	GND	GND	GND
E12	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	NC	NC	NC
F4	I/O	I/O	I/O
F5	GND	GND	GND
F6	GND	GND	GND
F7	GND	GND	GND
F8	V_{CCI}	V_{CCI}	V_{CCI}
F9	I/O	I/O	I/O
F10	GND	GND	GND
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O
G1	I/O	I/O	I/O
G2	GND	GND	GND
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O

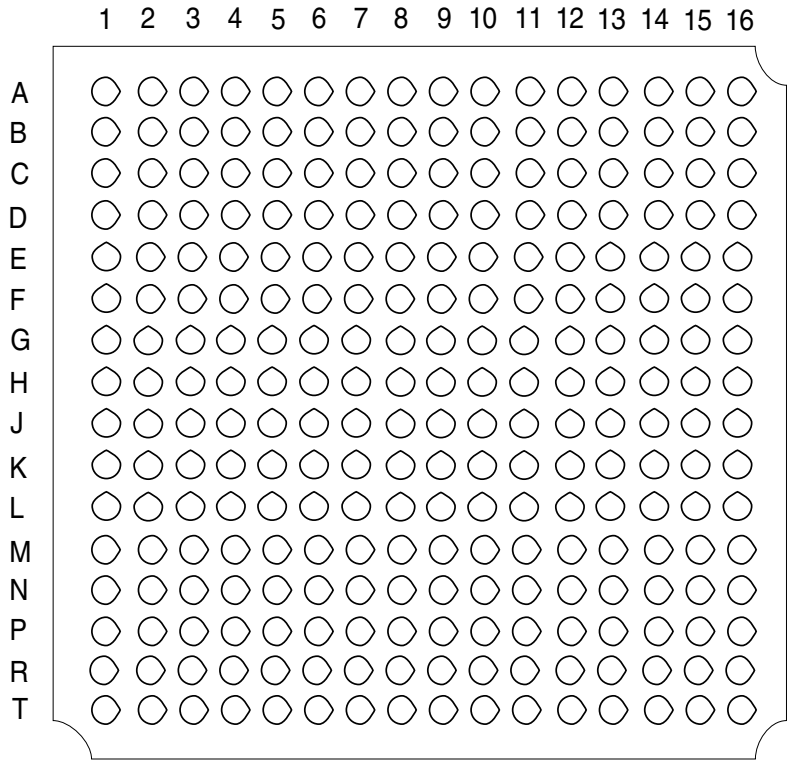
144-Pin FBGA (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	V_{CCI}	V_{CCI}	V_{CCI}
G9	I/O	I/O	I/O
G10	I/O	I/O	I/O
G11	I/O	I/O	I/O
G12	I/O	I/O	I/O
H1	TRST, I/O	TRST, I/O	TRST, I/O
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V_{CCA}	V_{CCA}	V_{CCA}
H6	V_{CCA}	V_{CCA}	V_{CCA}
H7	V_{CCI}	V_{CCI}	V_{CCI}
H8	V_{CCI}	V_{CCI}	V_{CCI}
H9	V_{CCA}	V_{CCA}	V_{CCA}
H10	I/O	I/O	I/O
H11	I/O	I/O	I/O
H12	NC	NC	NC
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	PRB, I/O	PRB, I/O	PRB, I/O
J7	I/O	I/O	I/O
J8	I/O	I/O	I/O
J9	I/O	I/O	I/O
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	V_{CCA}	V_{CCA}	V_{CCA}
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	I/O	I/O	I/O
K7	GND	GND	GND
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	GND	GND	GND
K11	I/O	I/O	I/O
K12	I/O	I/O	I/O
L1	GND	GND	GND
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	HCLK	HCLK	HCLK
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V_{CCA}	V_{CCA}	V_{CCA}
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	TDO, I/O	TDO, I/O	TDO, I/O
M12	I/O	I/O	I/O

Package Pin Assignments (Continued)

256-Pin FBGA (Top View)



256-Pin FBGA

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
A1	GND	GND	GND
A2	TCK, I/O	TCK, I/O	TCK, I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	I/O	I/O	I/O
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	CLKB	CLKB	CLKB
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	NC	I/O	I/O
A13	I/O	I/O	I/O
A14	I/O	I/O	I/O
A15	GND	GND	GND
A16	GND	GND	GND
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	NC	I/O	I/O
B7	I/O	I/O	I/O
B8	V_{CCA}	V_{CCA}	V_{CCA}
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	NC	I/O	I/O
B12	I/O	I/O	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	GND	GND	GND
B16	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	TDI, I/O	TDI, I/O	TDI, I/O
C3	GND	GND	GND
C4	I/O	I/O	I/O
C5	NC	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	CLKA	CLKA	CLKA
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
C14	I/O	I/O	I/O
C15	I/O	I/O	I/O
C16	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	PRA, I/O	PRA, I/O	PRA, I/O
D9	I/O	I/O	QCLKD
D10	I/O	I/O	I/O
D11	NC	I/O	I/O
D12	I/O	I/O	I/O
D13	I/O	I/O	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	I/O	I/O	I/O
E6	I/O	I/O	I/O
E7	I/O	I/O	QCLKC
E8	I/O	I/O	I/O
E9	I/O	I/O	I/O
E10	I/O	I/O	I/O
E11	I/O	I/O	I/O
E12	I/O	I/O	I/O
E13	NC	I/O	I/O
E14	I/O	I/O	I/O
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	TMS	TMS	TMS
F5	I/O	I/O	I/O
F6	I/O	I/O	I/O
F7	V_{CCI}	V_{CCI}	V_{CCI}
F8	V_{CCI}	V_{CCI}	V_{CCI}
F9	V_{CCI}	V_{CCI}	V_{CCI}
F10	V_{CCI}	V_{CCI}	V_{CCI}

256-Pin FBGA (Continued)

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
F11	I/O	I/O	I/O
F12	VCCA	VCCA	VCCA
F13	I/O	I/O	I/O
F14	I/O	I/O	I/O
F15	I/O	I/O	I/O
F16	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	I/O	I/O	I/O
G3	NC	I/O	I/O
G4	I/O	I/O	I/O
G5	I/O	I/O	I/O
G6	V_{CCI}	V_{CCI}	V_{CCI}
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	V_{CCI}	V_{CCI}	V_{CCI}
G12	I/O	I/O	I/O
G13	GND	GND	GND
G14	NC	I/O	I/O
G15	V_{CCA}	V_{CCA}	V_{CCA}
G16	I/O	I/O	I/O
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O
H3	V_{CCA}	V_{CCA}	V_{CCA}
H4	TRST, I/O	TRST, I/O	TRST, I/O
H5	I/O	I/O	I/O
H6	V_{CCI}	V_{CCI}	V_{CCI}
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	V_{CCI}	V_{CCI}	V_{CCI}
H12	I/O	I/O	I/O
H13	I/O	I/O	I/O
H14	I/O	I/O	I/O
H15	I/O	I/O	I/O
H16	NC	I/O	I/O
J1	NC	I/O	I/O
J2	NC	I/O	I/O
J3	NC	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	V_{CCI}	V_{CCI}	V_{CCI}
J7	GND	GND	GND

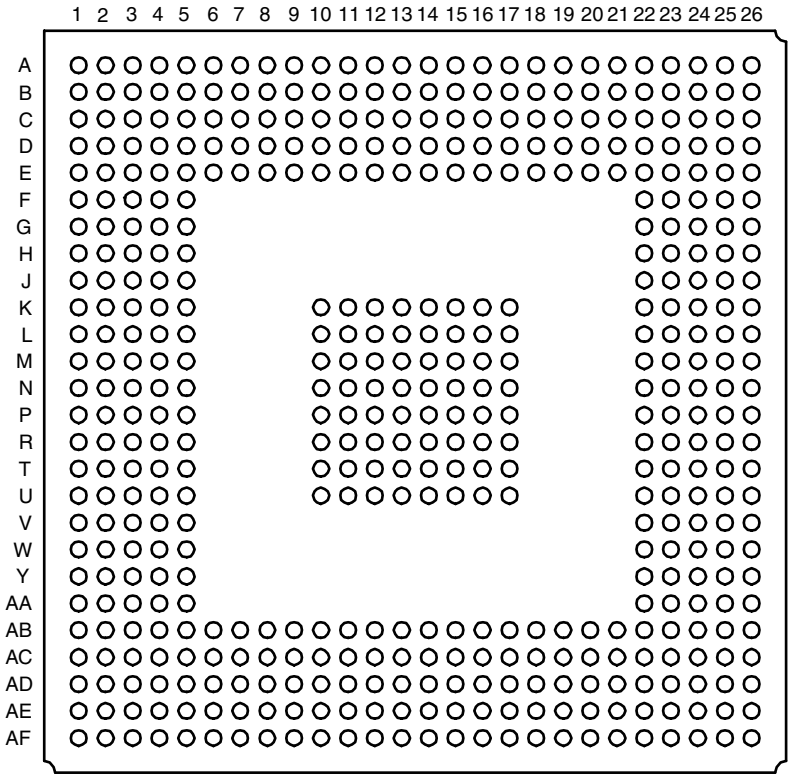
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	V_{CCI}	V_{CCI}	V_{CCI}
J12	I/O	I/O	I/O
J13	I/O	I/O	I/O
J14	I/O	I/O	I/O
J15	I/O	I/O	I/O
J16	I/O	I/O	I/O
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	NC	I/O	I/O
K4	V_{CCA}	V_{CCA}	V_{CCA}
K5	I/O	I/O	I/O
K6	V_{CCI}	V_{CCI}	V_{CCI}
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	V_{CCI}	V_{CCI}	V_{CCI}
K12	I/O	I/O	I/O
K13	I/O	I/O	I/O
K14	I/O	I/O	I/O
K15	NC	I/O	I/O
K16	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	V_{CCI}	V_{CCI}	V_{CCI}
L8	V_{CCI}	V_{CCI}	V_{CCI}
L9	V_{CCI}	V_{CCI}	V_{CCI}
L10	V_{CCI}	V_{CCI}	V_{CCI}
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
L13	I/O	I/O	I/O
L14	I/O	I/O	I/O
L15	I/O	I/O	I/O
L16	NC	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O

256-Pin FBGA (Continued)

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	I/O	I/O	QCLKA
M8	PRB, I/O	PRB, I/O	PRB, I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	NC	I/O	I/O
M13	I/O	I/O	I/O
M14	NC	I/O	I/O
M15	I/O	I/O	I/O
M16	I/O	I/O	I/O
N1	I/O	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N6	I/O	I/O	I/O
N7	I/O	I/O	I/O
N8	I/O	I/O	I/O
N9	I/O	I/O	I/O
N10	I/O	I/O	I/O
N11	I/O	I/O	I/O
N12	I/O	I/O	I/O
N13	I/O	I/O	I/O
N14	I/O	I/O	I/O
N15	I/O	I/O	I/O
N16	I/O	I/O	I/O
P1	I/O	I/O	I/O
P2	GND	GND	GND
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	NC	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	NC	I/O	I/O
P11	I/O	I/O	I/O
P12	I/O	I/O	I/O
P13	V_{CCA}	V_{CCA}	V_{CCA}
P14	I/O	I/O	I/O
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V_{CCA}	V_{CCA}	V_{CCA}
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

Package Pin Assignments (Continued)

484-Pin FBGA (Top View)



484-Pin FBGA

Pin Number	A54SX32A Function	A54SX72A Function
A1	NC	NC
A2	NC	NC
A3	NC	I/O
A4	NC	I/O
A5	NC	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	NC	I/O
A12	NC	I/O
A13	I/O	I/O
A14	NC	NC
A15	NC	I/O
A16	NC	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
A21	NC	I/O
A22	NC	I/O
A23	NC	I/O
A24	NC	I/O
A25	NC	NC
A26	NC	NC
AA1	NC	I/O
AA2	NC	I/O
AA3	V_{CCA}	V_{CCA}
AA4	I/O	I/O
AA5	I/O	I/O
AA22	I/O	I/O
AA23	I/O	I/O
AA24	I/O	I/O
AA25	NC	I/O
AA26	NC	I/O
AB1	NC	NC
AB2	V_{CCI}	V_{CCI}
AB3	I/O	I/O
AB4	I/O	I/O
AB5	NC	I/O
AB6	I/O	I/O
AB7	I/O	I/O
AB8	I/O	I/O
AB9	I/O	I/O
AB10	I/O	I/O
AB11	I/O	I/O
AB12	PRB, I/O	PRB, I/O
AB13	V_{CCA}	V_{CCA}
AB14	I/O	I/O
AB15	I/O	I/O
AB16	I/O	I/O
AB17	I/O	I/O
AB18	I/O	I/O
AB19	I/O	I/O
AB20	TDO, I/O	TDO, I/O
AB21	GND	GND
AB22	NC	I/O
AB23	I/O	I/O
AB24	I/O	I/O
AB25	NC	I/O
AB26	NC	I/O
AC1	I/O	I/O
AC2	I/O	I/O
AC3	I/O	I/O
AC4	NC	I/O
AC5	V_{CCI}	V_{CCI}
AC6	I/O	I/O
AC7	V_{CCI}	V_{CCI}
AC8	I/O	I/O
AC9	I/O	I/O
AC10	I/O	I/O
AC11	I/O	I/O
AC12	I/O	QCLKA
AC13	I/O	I/O
AC14	I/O	I/O
AC15	I/O	I/O
AC16	I/O	I/O
AC17	I/O	I/O
AC18	I/O	I/O
AC19	I/O	I/O
AC20	V_{CCI}	V_{CCI}
AC21	I/O	I/O
AC22	I/O	I/O
AC23	NC	I/O
AC24	I/O	I/O
AC25	NC	I/O
AC26	NC	I/O
AD1	I/O	I/O
AD2	I/O	I/O
AD3	GND	GND
AD4	I/O	I/O
AD5	I/O	I/O
AD6	I/O	I/O
AD7	I/O	I/O
AD8	I/O	I/O
AD9	V_{CCI}	V_{CCI}
AD10	I/O	I/O
AD11	I/O	I/O
AD12	I/O	I/O
AD13	V_{CCI}	V_{CCI}
AD14	I/O	I/O
AD15	I/O	I/O
AD16	I/O	I/O
AD17	V_{CCI}	V_{CCI}
AD18	I/O	I/O
AD19	I/O	I/O
AD20	I/O	I/O
AD21	I/O	I/O
AD22	I/O	I/O
AD23	V_{CCI}	V_{CCI}
AD24	NC	I/O
AD25	NC	I/O
AD26	NC	I/O
AE1	NC	NC
AE2	I/O	I/O
AE3	NC	I/O
AE4	NC	I/O
AE5	NC	I/O
AE6	NC	I/O
AE7	I/O	I/O
AE8	I/O	I/O
AE9	I/O	I/O
AE10	I/O	I/O
AE11	NC	I/O
AE12	I/O	I/O
AE13	I/O	I/O
AE14	I/O	I/O
AE15	NC	I/O
AE16	NC	I/O
AE17	I/O	I/O
AE18	I/O	I/O
AE19	I/O	I/O
AE20	I/O	I/O
AE21	NC	I/O
AE22	NC	I/O
AE23	NC	I/O
AE24	NC	I/O

484-Pin FBGA (Continued)

Pin Number	A54SX32A Function	A54SX72A Function
AE25	NC	NC
AE26	NC	NC
AF1	NC	NC
AF2	NC	NC
AF3	NC	I/O
AF4	NC	I/O
AF5	NC	I/O
AF6	NC	I/O
AF7	I/O	I/O
AF8	I/O	I/O
AF9	I/O	I/O
AF10	I/O	I/O
AF11	NC	I/O
AF12	NC	NC
AF13	HCLK	HCLK
AF14	I/O	QCLKB
AF15	NC	I/O
AF16	NC	I/O
AF17	I/O	I/O
AF18	I/O	I/O
AF19	I/O	I/O
AF20	NC	I/O
AF21	NC	I/O
AF22	NC	I/O
AF23	NC	I/O
AF24	NC	I/O
AF25	NC	NC
AF26	NC	NC
B1	NC	NC
B2	NC	NC
B3	NC	I/O
B4	NC	I/O
B5	NC	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	NC	I/O
B12	NC	I/O
B13	V_{CCI}	V_{CCI}
B14	CLKA	CLKA
B15	NC	I/O
B16	NC	I/O
B17	I/O	I/O
B18	V_{CCI}	V_{CCI}
B19	I/O	I/O
B20	I/O	I/O
B21	NC	I/O
B22	NC	I/O
B23	NC	I/O
B24	NC	I/O
B25	I/O	I/O
B26	NC	NC
C1	NC	I/O
C2	NC	I/O
C3	NC	I/O
C4	NC	I/O
C5	I/O	I/O
C6	V_{CCI}	V_{CCI}
C7	I/O	I/O
C8	I/O	I/O
C9	V_{CCI}	V_{CCI}
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	PRA, I/O	PRA, I/O
C14	I/O	I/O
C15	I/O	QCLKD
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O
C19	I/O	I/O
C20	V_{CCI}	V_{CCI}
C21	I/O	I/O
C22	I/O	I/O
C23	I/O	I/O
C24	I/O	I/O
C25	NC	I/O
C26	NC	I/O
D1	NC	I/O
D2	TMS	TMS
D3	I/O	I/O
D4	V_{CCI}	V_{CCI}
D5	NC	I/O
D6	TCK, I/O	TCK, I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	QCLKC
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I/O	I/O
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
D21	V_{CCI}	V_{CCI}
D22	GND	GND
D23	I/O	I/O
D24	I/O	I/O
D25	NC	I/O
D26	NC	I/O
E1	NC	I/O
E2	NC	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	GND	GND
E6	TDI, IO	TDI, IO
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	V_{CCA}	V_{CCA}
E14	CLKB	CLKB
E15	I/O	I/O
E16	I/O	I/O
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
E21	I/O	I/O
E22	I/O	I/O
E23	I/O	I/O
E24	I/O	I/O
E25	V_{CCI}	V_{CCI}
E26	GND	GND
F1	V_{CCI}	V_{CCI}
F2	NC	I/O
F3	NC	I/O
F4	I/O	I/O
F5	I/O	I/O
F22	I/O	I/O

484-Pin FBGA (Continued)

Pin Number	A54SX32A Function	A54SX72A Function
F23	I/O	I/O
F24	I/O	I/O
F25	I/O	I/O
F26	NC	I/O
G1	NC	I/O
G2	NC	I/O
G3	NC	I/O
G4	I/O	I/O
G5	I/O	I/O
G22	I/O	I/O
G23	V_{CCA}	V_{CCA}
G24	I/O	I/O
G25	NC	I/O
G26	NC	I/O
H1	NC	I/O
H2	NC	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H22	I/O	I/O
H23	I/O	I/O
H24	I/O	I/O
H25	NC	I/O
H26	NC	I/O
J1	NC	I/O
J2	NC	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	I/O	I/O
J22	I/O	I/O
J23	I/O	I/O
J24	I/O	I/O
J25	V_{CCI}	V_{CCI}
J26	NC	I/O
K1	I/O	I/O
K2	V_{CCI}	V_{CCI}
K3	I/O	I/O
K4	I/O	I/O
K5	V_{CCA}	V_{CCA}
K10	GND	GND
K11	GND	GND
K12	GND	GND
K13	GND	GND
K14	GND	GND
K15	GND	GND
K16	GND	GND
K17	GND	GND
K22	I/O	I/O
K23	I/O	I/O
K24	NC	NC
K25	NC	I/O
K26	NC	I/O
L1	NC	I/O
L2	NC	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L10	GND	GND
L11	GND	GND
L12	GND	GND
L13	GND	GND
L14	GND	GND
L15	GND	GND
L16	GND	GND
L17	GND	GND
L22	I/O	I/O
L23	I/O	I/O
L24	I/O	I/O
L25	I/O	I/O
L26	I/O	I/O
M1	NC	NC
M2	I/O	I/O
M3	I/O	I/O
M4	I/O	I/O
M5	I/O	I/O
M10	GND	GND
M11	GND	GND
M12	GND	GND
M13	GND	GND
M14	GND	GND
M15	GND	GND
M16	GND	GND
M17	GND	GND
M22	I/O	I/O
M23	I/O	I/O
M24	I/O	I/O
M25	NC	I/O
M26	NC	I/O
N1	I/O	I/O
N2	V_{CCI}	V_{CCI}
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N10	GND	GND
N11	GND	GND
N12	GND	GND
N13	GND	GND
N14	GND	GND
N15	GND	GND
N16	GND	GND
N17	GND	GND
N22	V_{CCA}	V_{CCA}
N23	I/O	I/O
N24	I/O	I/O
N25	I/O	I/O
N26	NC	NC
P1	NC	I/O
P2	NC	I/O
P3	I/O	I/O
P4	I/O	I/O
P5	V_{CCA}	V_{CCA}
P10	GND	GND
P11	GND	GND
P12	GND	GND
P13	GND	GND
P14	GND	GND
P15	GND	GND
P16	GND	GND
P17	GND	GND
P22	I/O	I/O
P23	I/O	I/O
P24	V_{CCI}	V_{CCI}
P25	I/O	I/O
P26	I/O	I/O
R1	NC	I/O
R2	NC	I/O
R3	I/O	I/O
R4	I/O	I/O
R5	TRST, I/O	TRST, I/O
R10	GND	GND
R11	GND	GND
R12	GND	GND
R13	GND	GND
R14	GND	GND
R15	GND	GND
R16	GND	GND
R17	GND	GND
R22	I/O	I/O

484-Pin FBGA (Continued)

Pin Number	A54SX32A Function	A54SX72A Function
R23	I/O	I/O
R24	I/O	I/O
R25	NC	I/O
R26	NC	I/O
T1	NC	I/O
T2	NC	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC	I/O
T26	NC	I/O
U1	I/O	I/O
U2	V_{CCI}	V_{CCI}
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V_{CCI}	V_{CCI}
U26	I/O	I/O
V1	NC	I/O
V2	NC	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V_{CCA}	V_{CCA}
V23	I/O	I/O
V24	I/O	I/O
V25	NC	I/O
V26	NC	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V_{CCA}	V_{CCA}
W24	I/O	I/O
W25	NC	I/O
W26	NC	I/O
Y1	NC	I/O
Y2	NC	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V_{CCI}	V_{CCI}
Y25	I/O	I/O
Y26	I/O	I/O

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v3.0)	Page
v2.0.1	The section, "Development Tool Support" on page 10 has been updated.	page 10
	The section, "I/O Modules" on page 9, and the table, I/O Features, Table 1 on page 9 have been updated.	page 9
	The "SX-A Timing Model*" on page 19 and several timing tables on pages 22-49 have new timing numbers.	pages 19, 22-49

Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. These data sheets are marked as "Advanced" or Preliminary" data sheets. The definition of these categories are as follows:

Advanced

The data sheet contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Preliminary

The data sheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

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The data sheet contains information that is considered to be final.

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