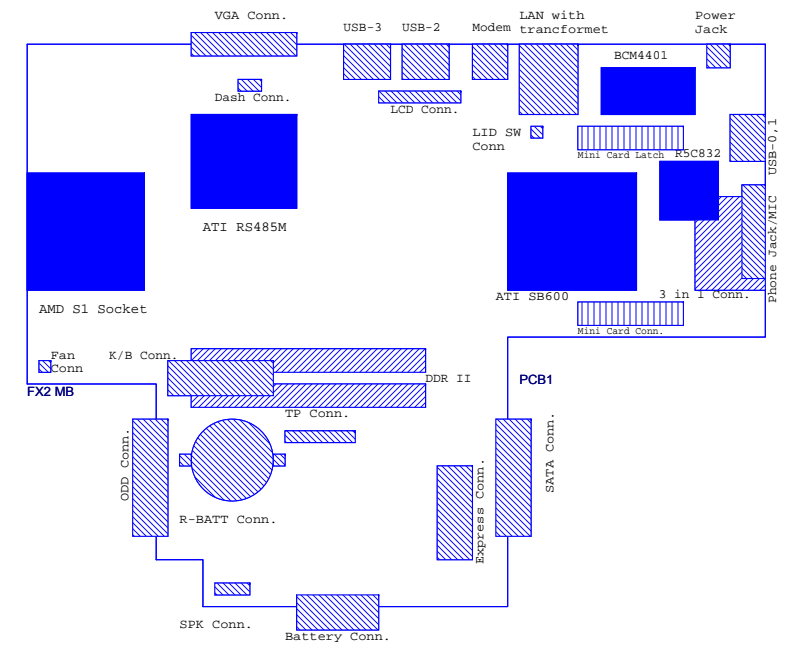
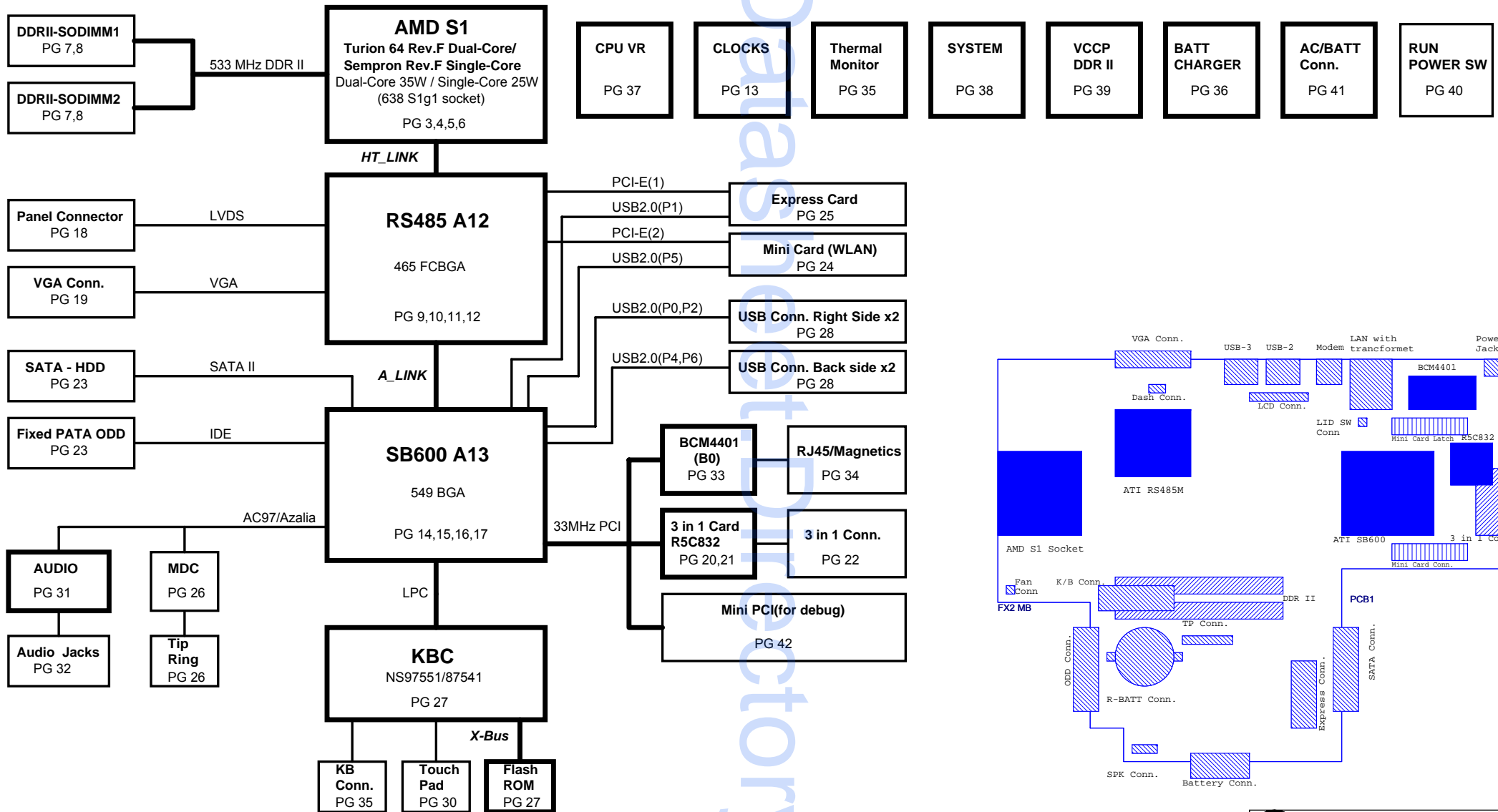


Kirin (FX2 with NS) VER : 1A



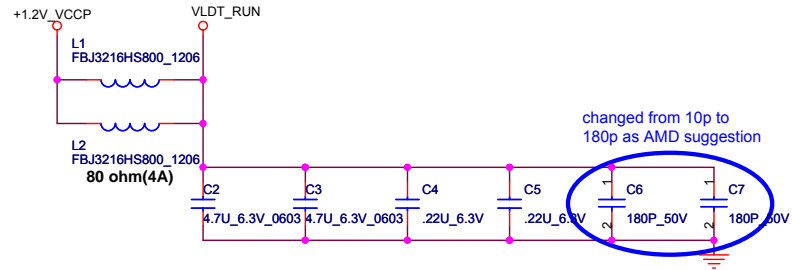
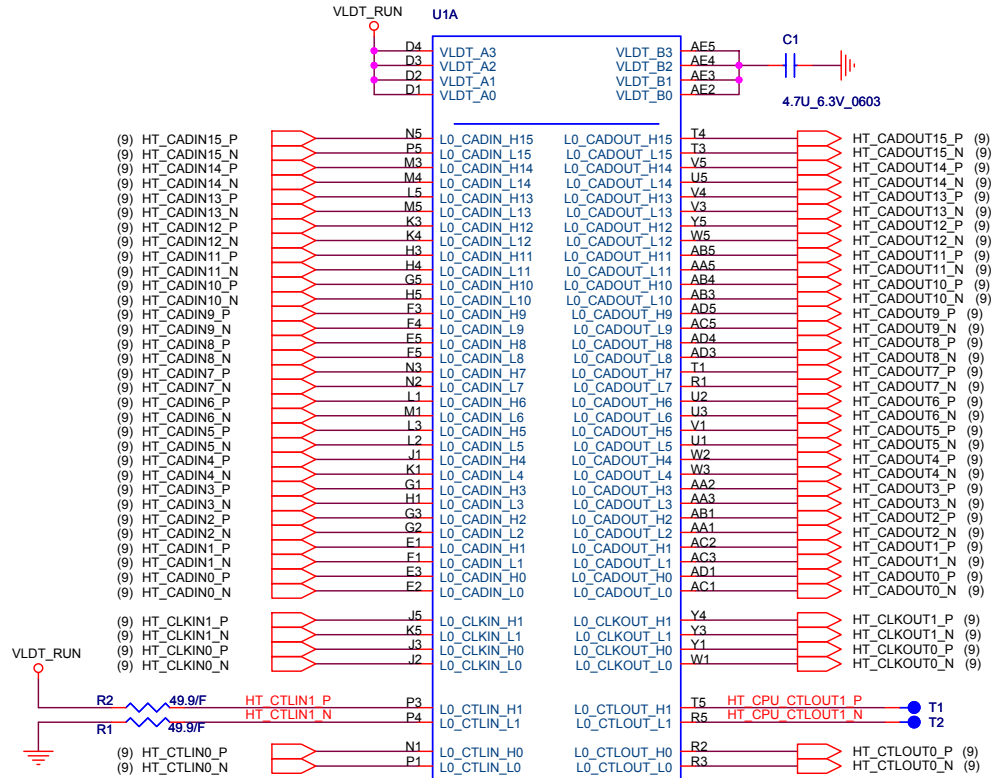
INDEX

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1	BLOCK DIAGRAM
2	FRONT PAGE
3	ATHLON64 HT I/F
4	ATHLON64 DDRII MEMORY
5	ATHLON64 CTRL & DEBUG
6	ATHLON64 PWR & GND
7	DDRII SODIMMX2
8	DDRII TERMINATION
9	RS485-HT LINK0 I/F
10	RS485-PCIE LINK I/F
11	RS485-LVDS
12	RS485-POWER
13	CLOCK GENERATOR
14	SB600M-PCIE/PCI/LPC
15	SB600M ACPI/USB/AC97
16	SB600M HDD/POWER
17	SB600M STRAPS
18	LCD CONN
19	CRT
20	5C832/PCI
21	CARD READER
22	CARD READER CONN
23	SATA HDD & PATA ODD
24	MINI Card
25	MINI Card
26	MDC CONN
27	PC97551 & FLASH
28	USB
29	EMI & Screw hole
30	SWITCH & TP & LED
31	Azelia CODEC
32	AUDIO CONN
33	LAN(BCM4401)
34	LAN JACK
35	KB & THERMAL & FAN
36	CHARGER (MAX8731)
37	VHCORE (MAX8774)
38	SYSTEM (MAX8734)
39	VCCP & DDR2 (MAX8743)
40	RUN POWER SW
41	DCIN,Batt
42	MINI PCI(for debug)
43	Power On Sequence
44	Power On Diagram
45	SMBUS BLOCK



PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



LAYOUT: Place bypass cap on topside of board

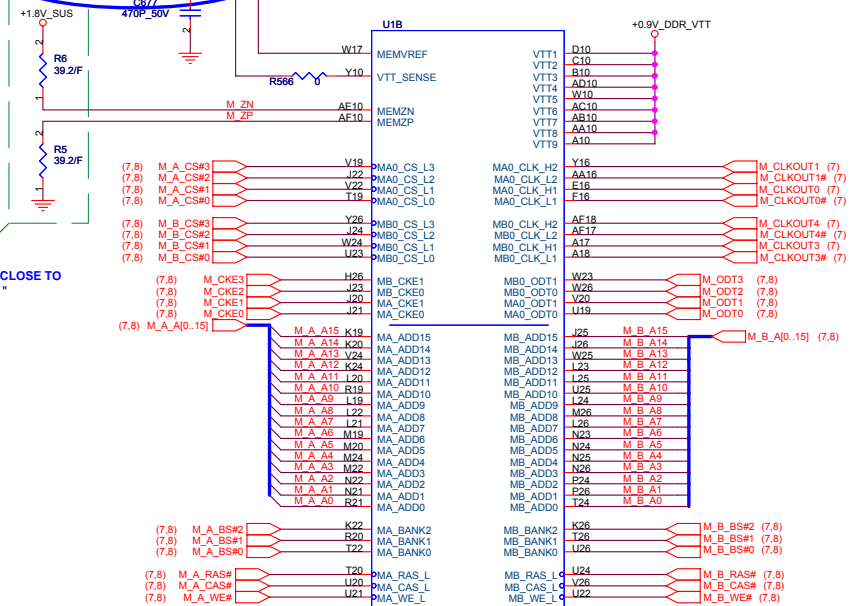
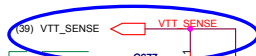
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDT0 POWER PINS



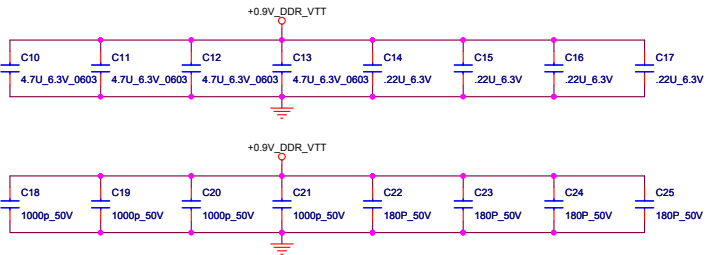
Title		ATHLON64 HT I/F
Size	Document Number	Rev
	FX2	1A
Date:	Friday, May 05, 2006	Sheet 3 of 47

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

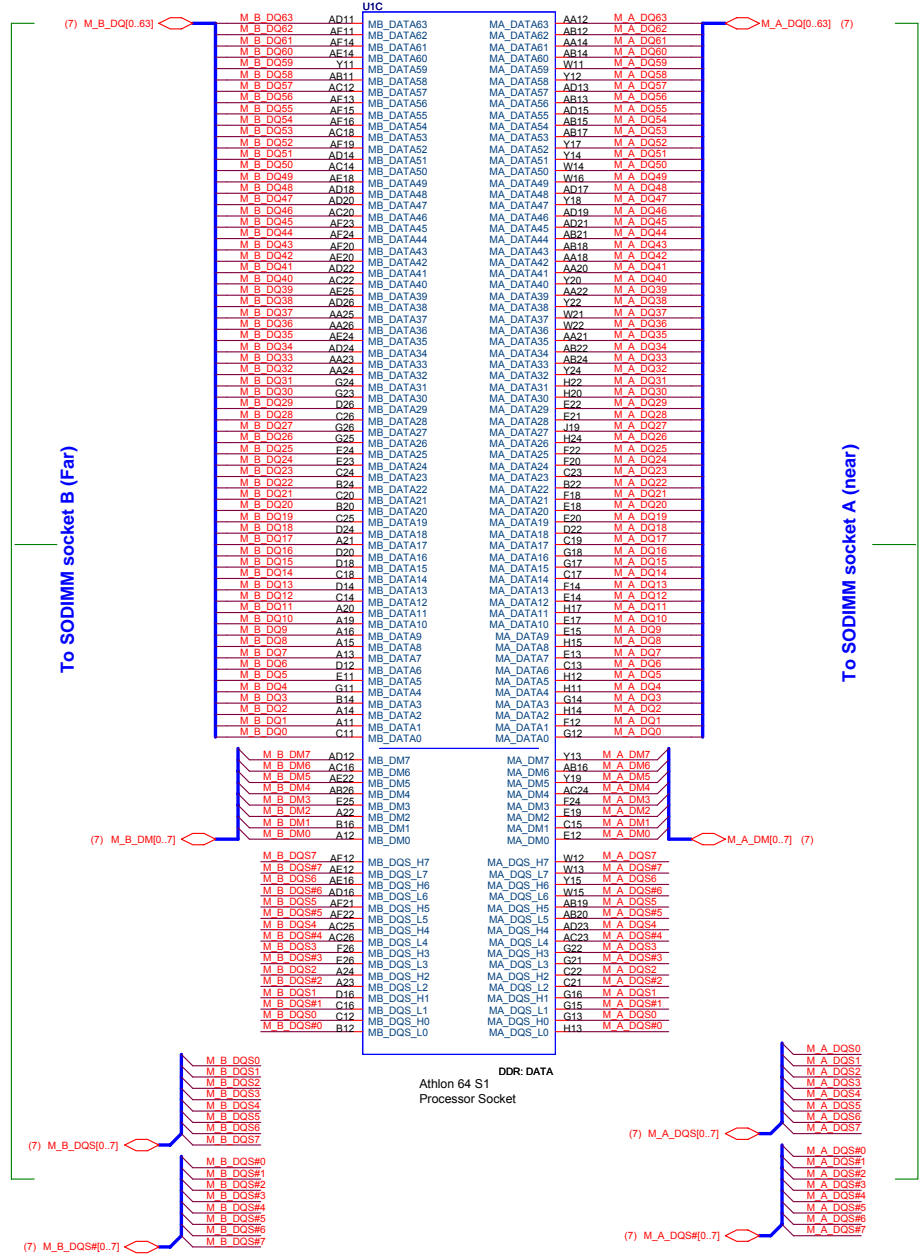
for +0.9V_DDR_VTT feedback



PLACE THEM CLOSE TO CPU WITHIN 1"



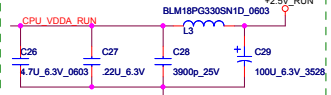
Processor DDR2 Memory Interface



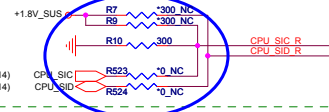
ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

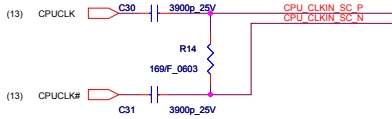


If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

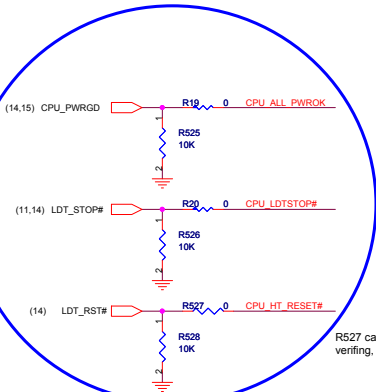


for CPU rev.F; if for rev.G, populate R7,R9,R523,R524 and depopulate R10

place them to CPU within 1"

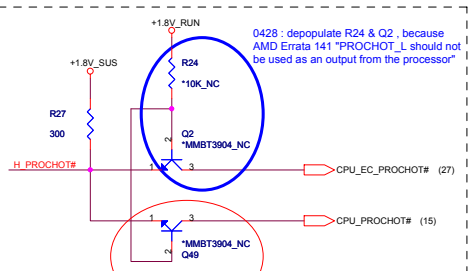


R14 close U1 within 600 mil, C30 & C31 close U1 within 1250 mil



change for SB800 from SB460

R527 can be used for EMI verifying, place close to CPU



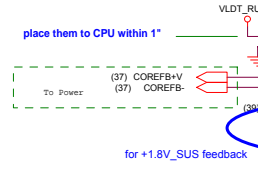
0428: depopulate R24 & Q2, because AMD Errata 141 *PROCHOT_L should not be used as an output from the processor*

SB this pin is 3.3V, need it level-shift.

delete ED5_H_THERMTRIP# circuit



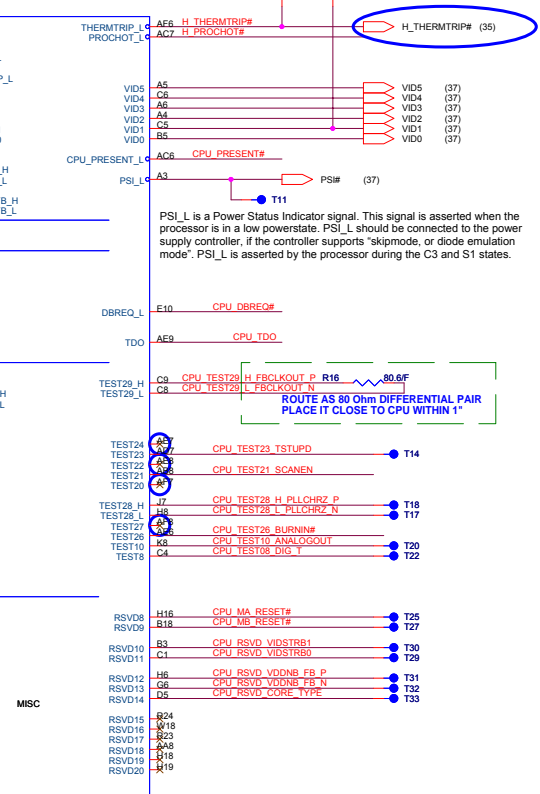
delete ED5 thermal sensor



for +1.8V_SUS feedback

add port to Page 35 U36 Thermal IC

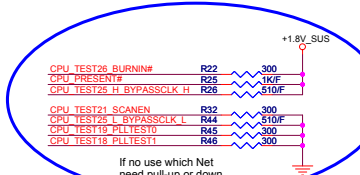
Table listing pin connections for the AMD NPT S1 SOCKET Processor Socket. Includes pins for CPU_VDDA_RUN, CPU_SID, CPU_SIC, CPU_CLKIN, CPU_DBRDY, CPU_TMS, CPU_TCK, CPU_TRST#, CPU_TDI, CPU_TEST#, CPU_RSVD, and MISC.



PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller. If the controller supports 'skipmode, or diode emulation mode', PSI_L is asserted by the processor during the C3 and S1 states.

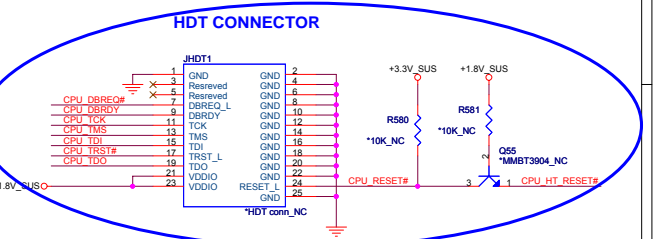
ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

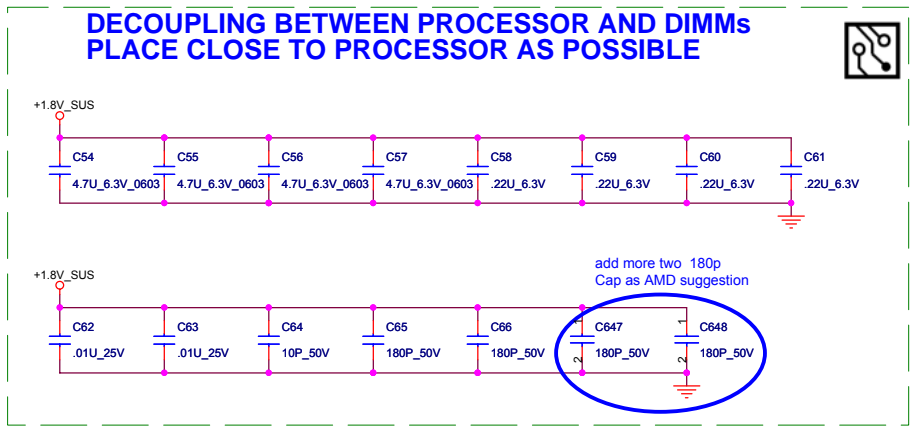
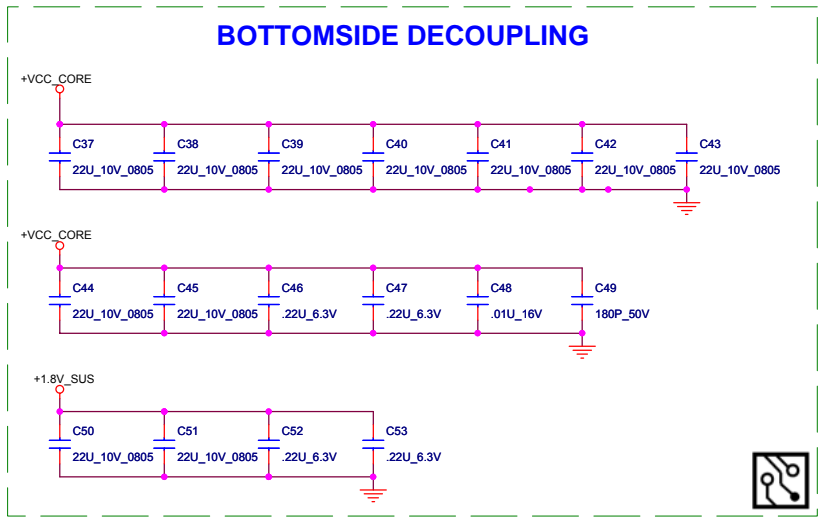
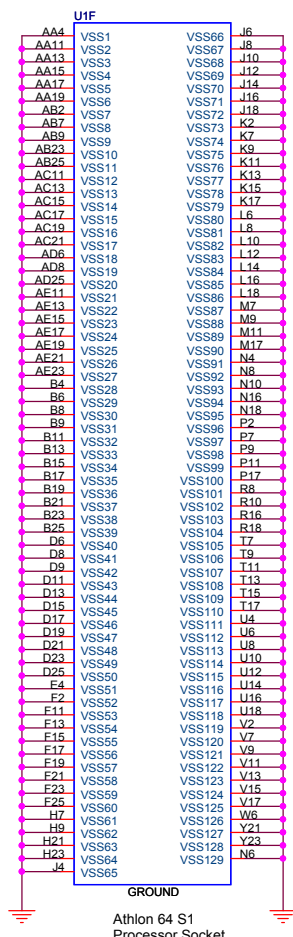
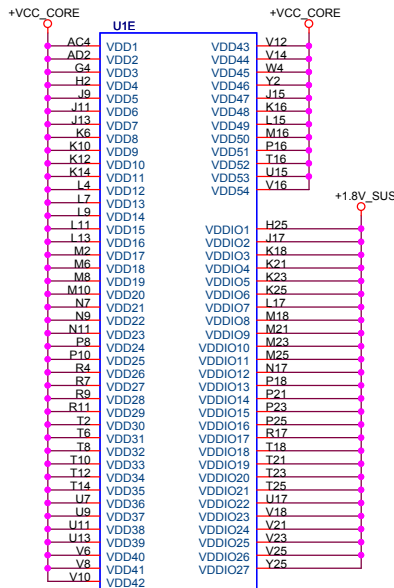
change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down



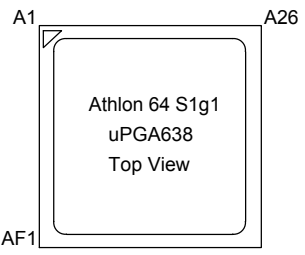
If no use which Net need pull-up or down

add HDT connector for debug convenience





PROCESSOR POWER AND GROUND



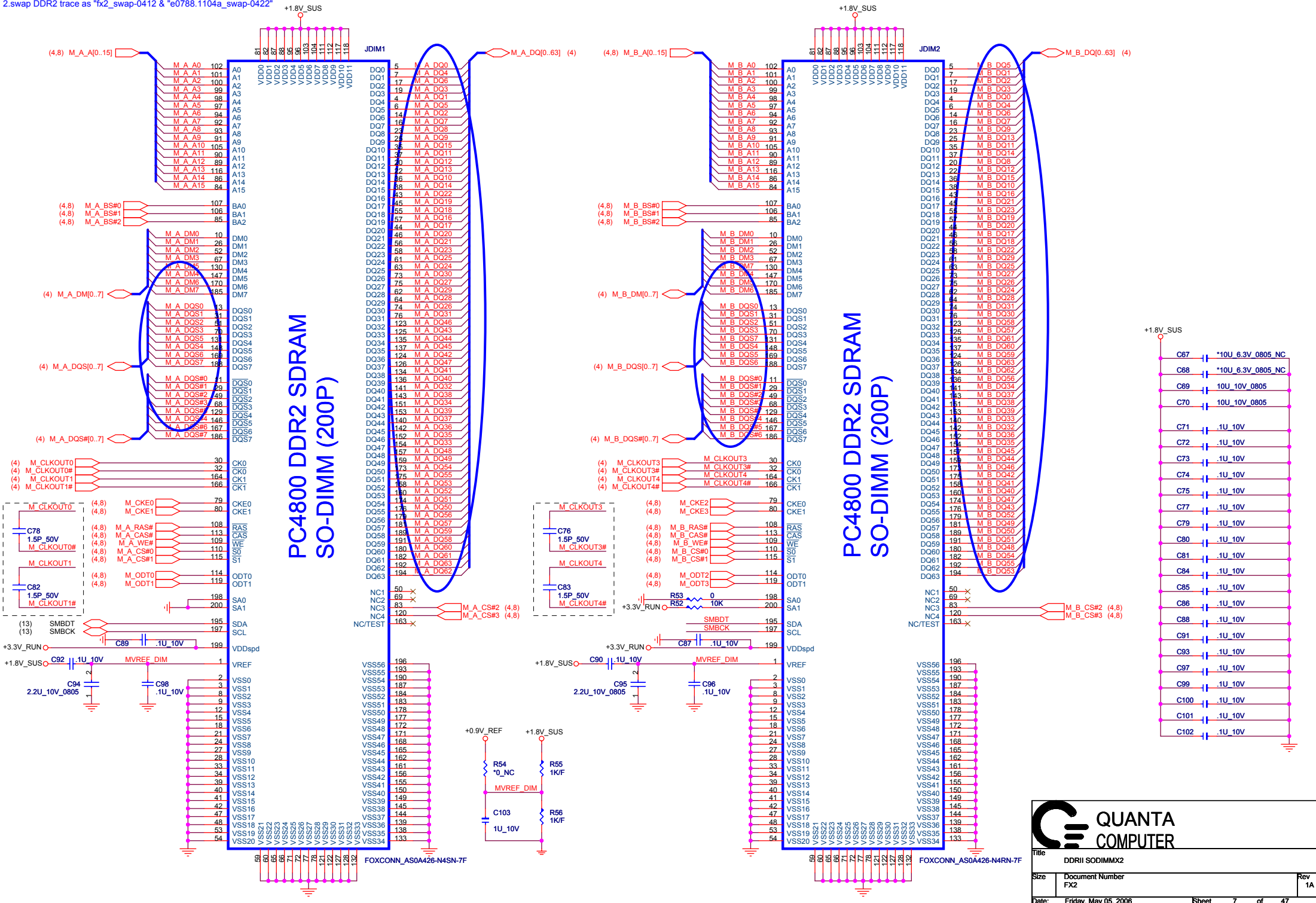
QUANTA COMPUTER

Title: ATHLON64 PWR & GND

Size: FX2 Document Number: Rev 1A

Date: Thursday, May 04, 2006 Sheet 6 of 47

1. Change DDR2 socket(P/N, Description, footprint, part reference, value)
 2. swap DDR2 trace as "fx2_swap-0412 & "e0788.1104a_swap-0422"

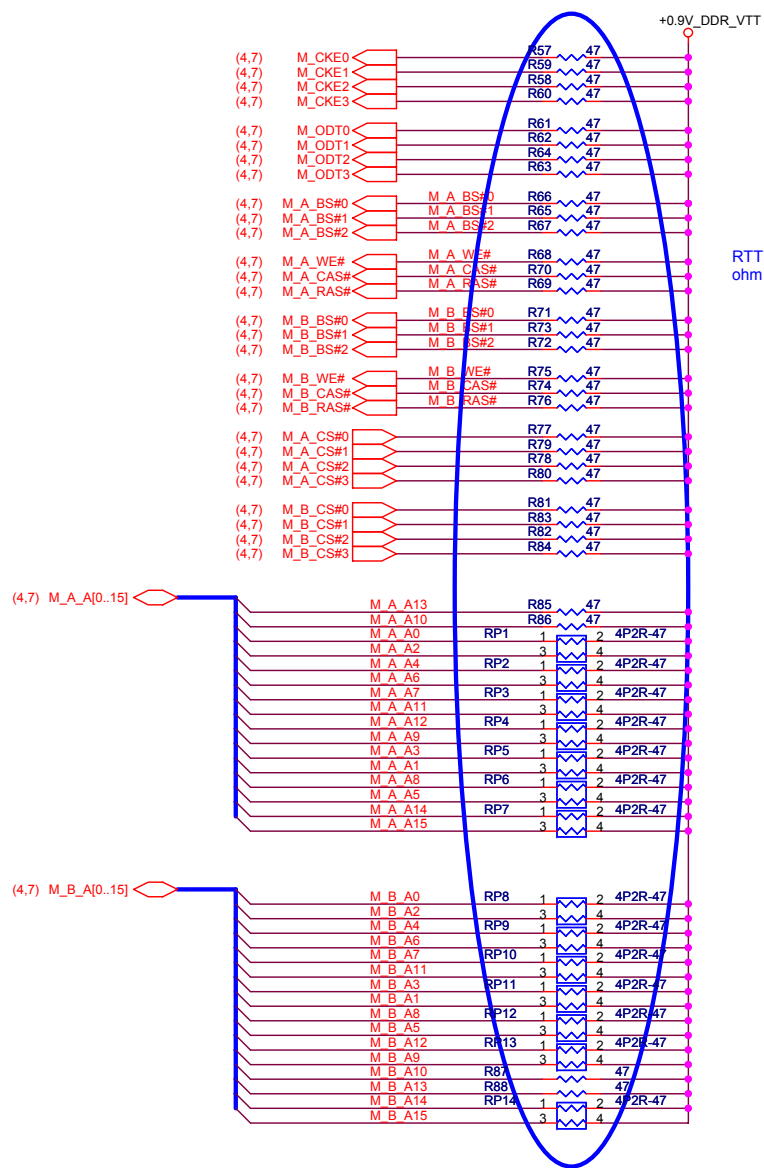
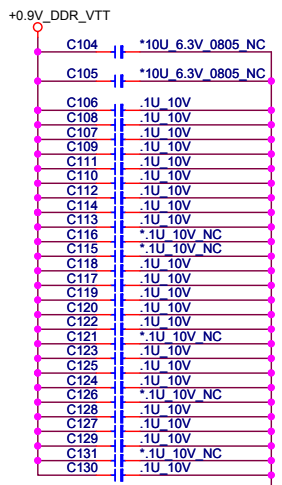


QUANTA COMPUTER

Title: **DDRII SODIMMx2**

Size: **Document Number FX2** Rev: **1A**

Date: **Friday, May 05, 2006** Sheet: **7 of 47**



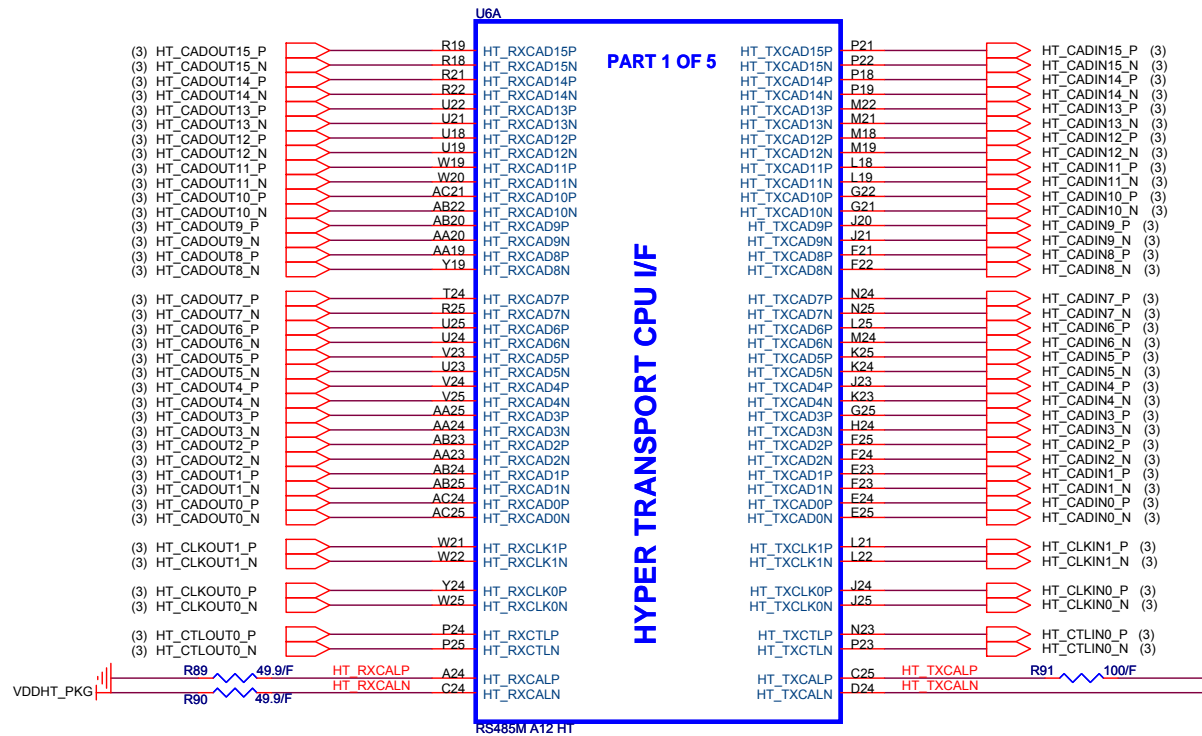
RTT termination changed from 56 ohm to 47 ohm as AMD suggestion

**QUANTA
COMPUTER**

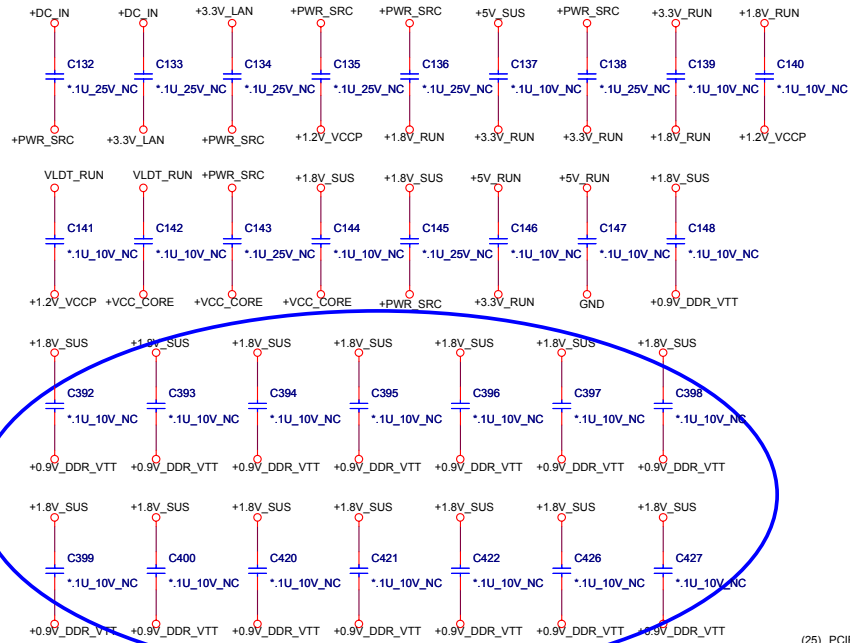
Title: DDRII TERMINATION

Size: Document Number FX2 Rev 1A

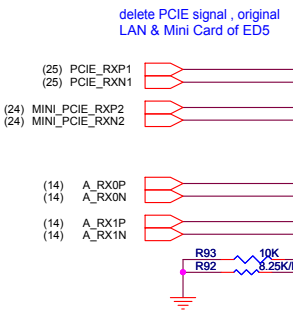
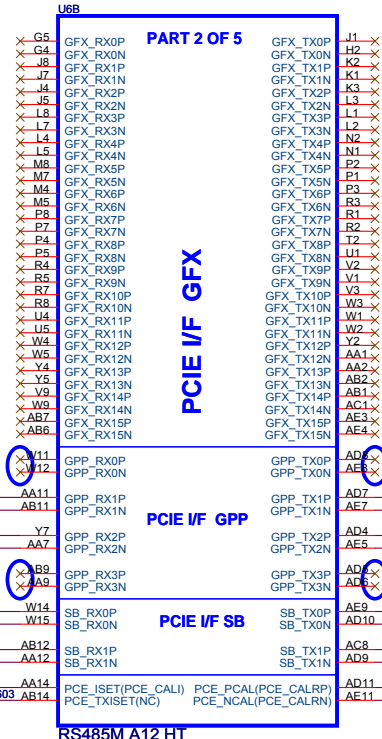
Date: Friday, May 05, 2006 Sheet 8 of 47



Title			RS485-HT LINK0 I/F
Size	Document Number	Rev	
	FX2	1A	
Date:	Friday, May 05, 2006	Sheet	9 of 47



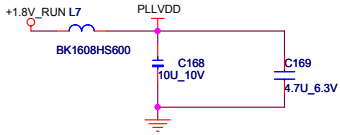
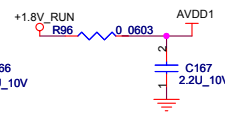
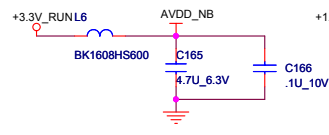
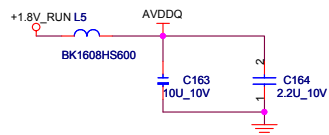
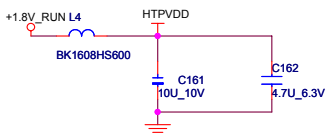
reserve more 14 Cap. between +0.9V_DDR_VTT & +1.8V_SUS



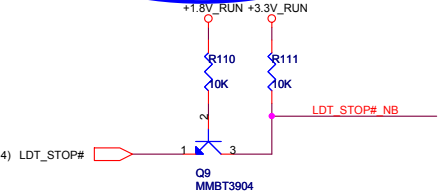
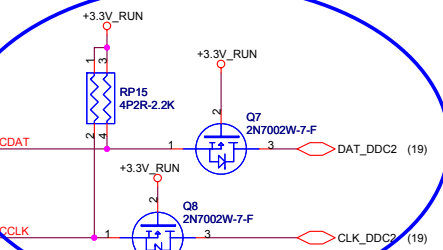
R93: 10KOhm FOR RS485
1.47KOhm FOR RS690
R92: 8.25KOhm FOR RS485
DNI FOR RS690

R95: 150 Ohm FOR RS485
562 Ohm FOR RS690
R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690



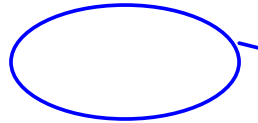


added as FM1 application for ED5

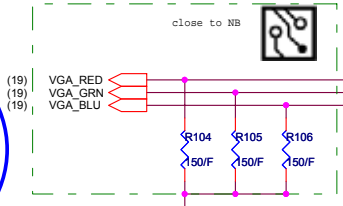


LOAD_ROM#: LOAD ROM STRAP ENABLE

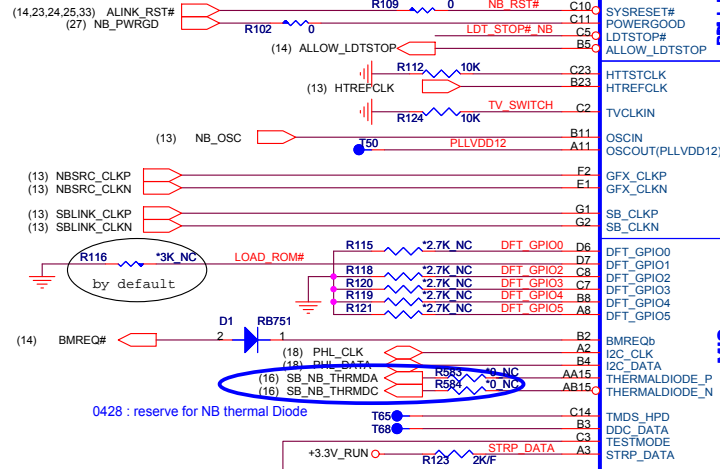
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE



deleted caused by Svideo defeature



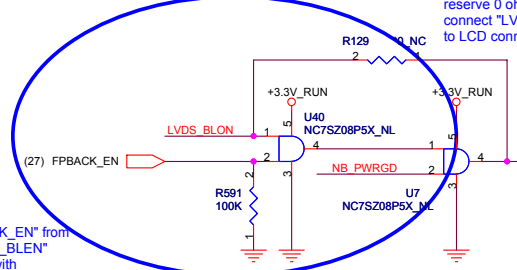
external trace become to internal trace



0428 : reserve for NB thermal Diode

	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

0504 : change "FPBACK_EN" from connected with "LVDS_BLEN" directly to connected with "LVDS_BLON" by a AND gate



PART 3 OF 5

CRT/TVOUT

LVDS

PLL PWR

CLOCKS

MIS.

DVO

DVO

DVO

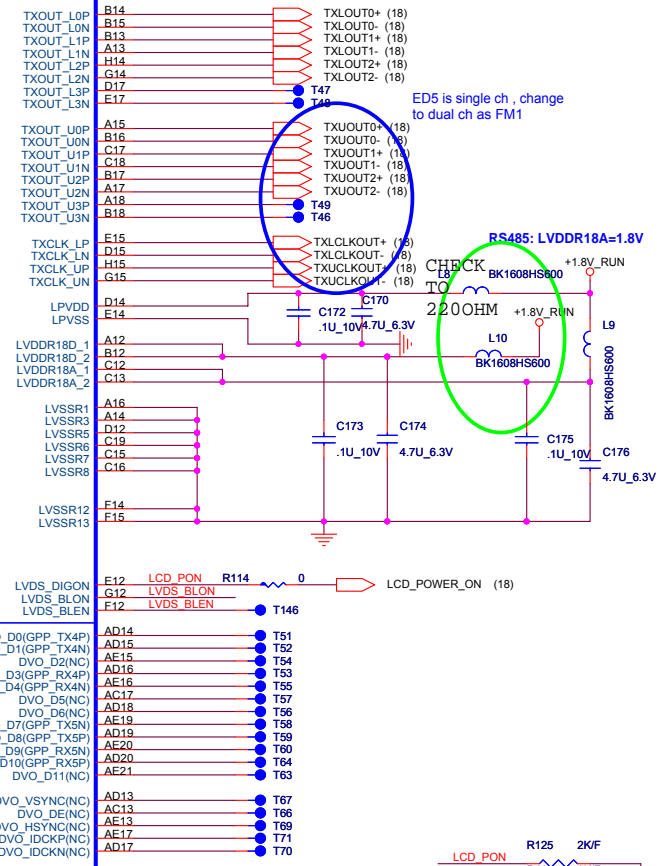
DVO

DVO

DVO

DVO

DVO



ED5 is single ch., change to dual ch as FM1

RS485: LVDDR18A=1.8V



220OHM

1.8V_RUN

4.7U_6.3V

1.8V_RUN

4.7U_6.3V

1.8V_RUN

4.7U_6.3V

1.8V_RUN

4.7U_6.3V

1.8V_RUN

4.7U_6.3V

1.8V_RUN

4.7U_6.3V

1.8V_RUN

4.7U_6.3V

1.8V_RUN

4.7U_6.3V

1.8V_RUN

4.7U_6.3V

1.8V_RUN

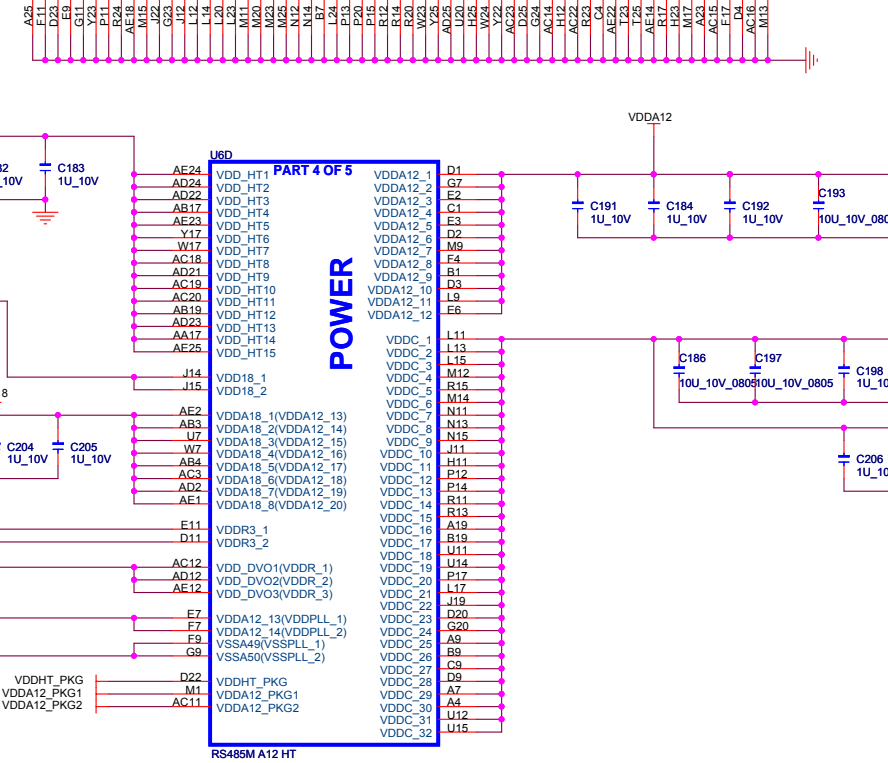
4.7U_6.3V

QUANTA COMPUTER

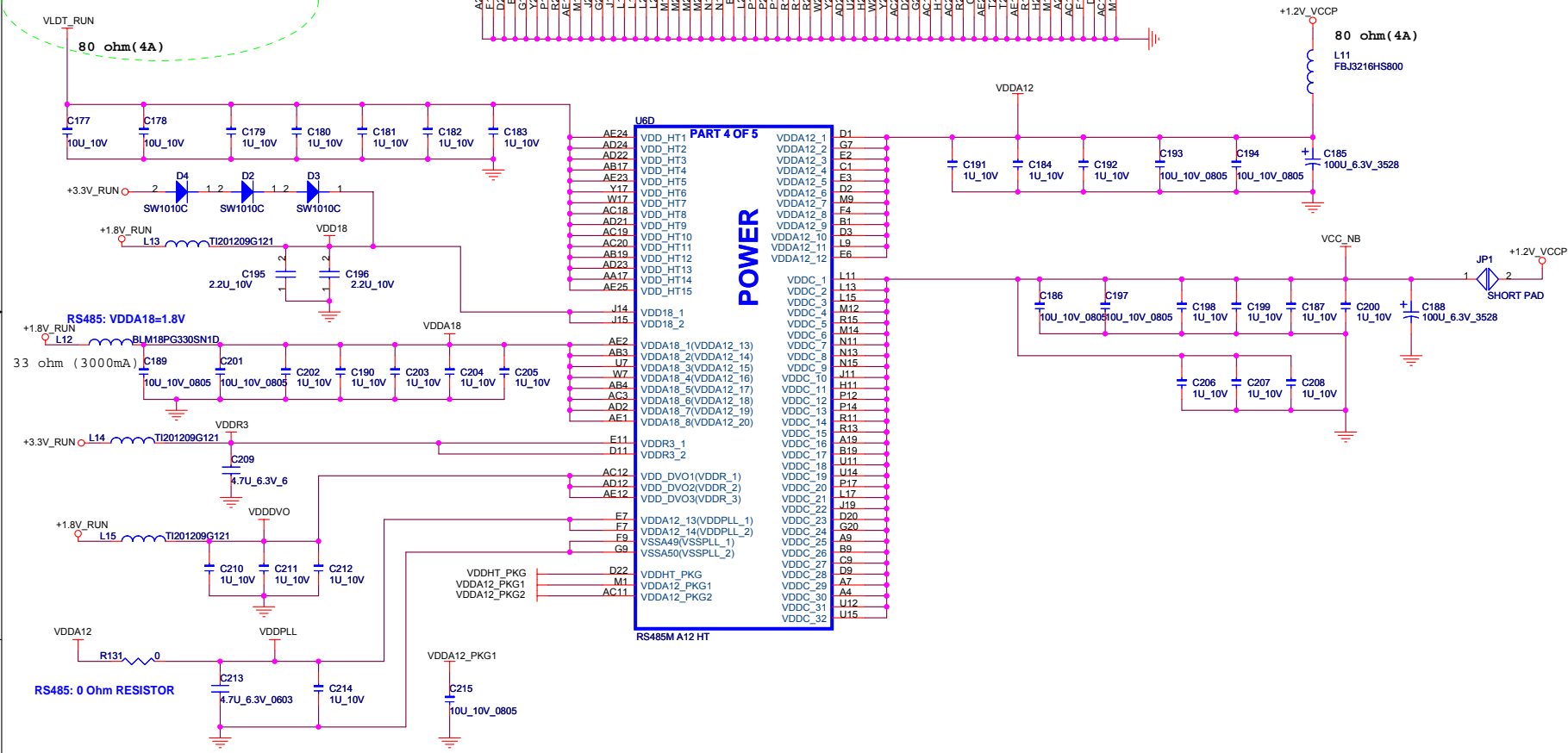
RS485-LVDS

Size: FX2 Document Number: Rev 1A

Date: Friday, May 05, 2006 Sheet 11 of 47



SUGGEST REMOVE L11 BEAD SAME AS CPU
 .2 PLAN FSB UNDER THIS PLAN

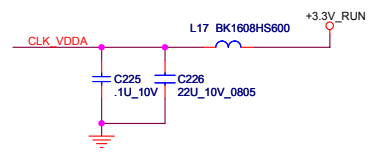
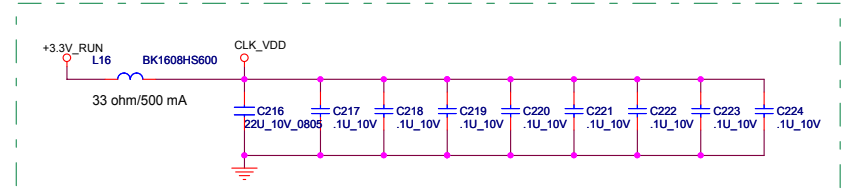


NB RS485 POWER STATES

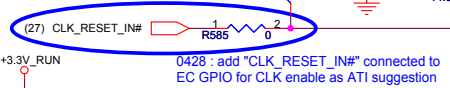
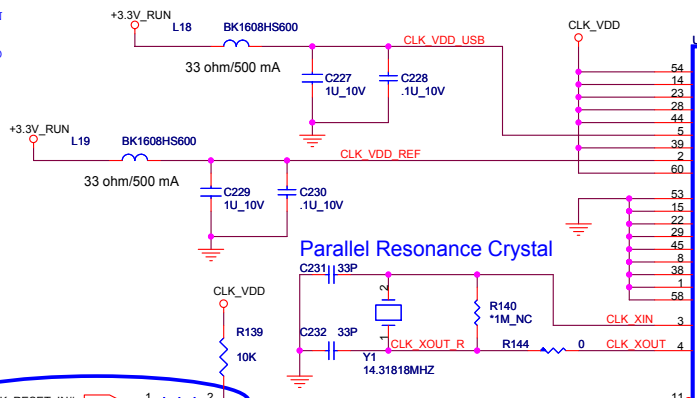
Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

QUANTA
COMPUTER

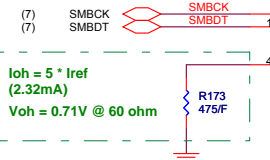
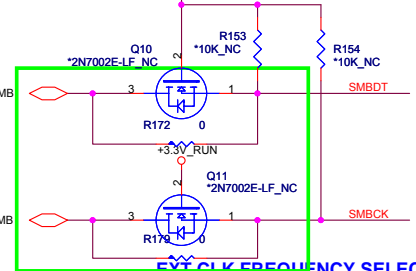
Title: RS485-POWER
 Size: Document Number FX2
 Date: Thursday, May 04, 2006
 Sheet 12 of 47
 Rev 1A



- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO Clock Gen.POWER PIN



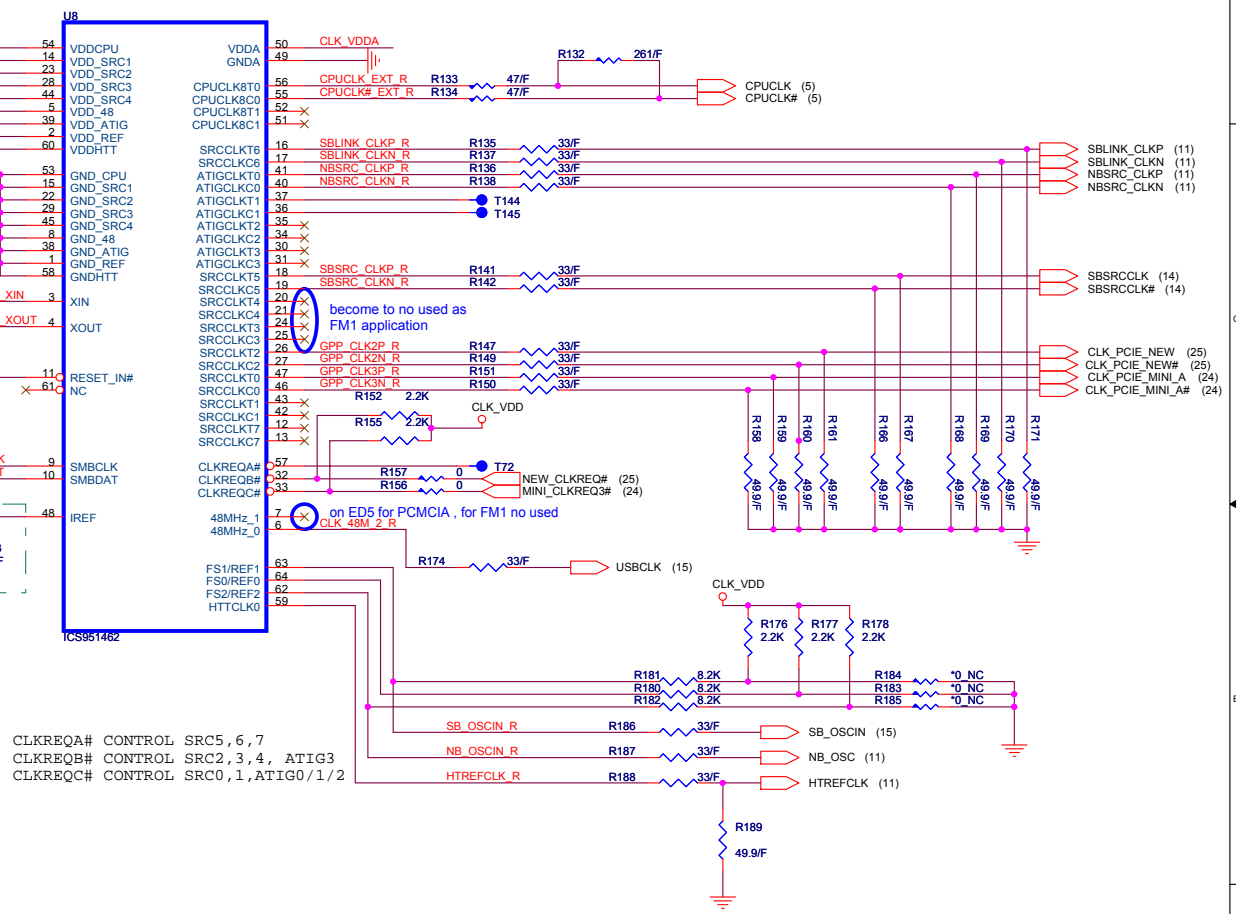
042B : add "CLK_RESET_IN#" connected to EC GPIO for CLK enable as ATI suggestion



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock



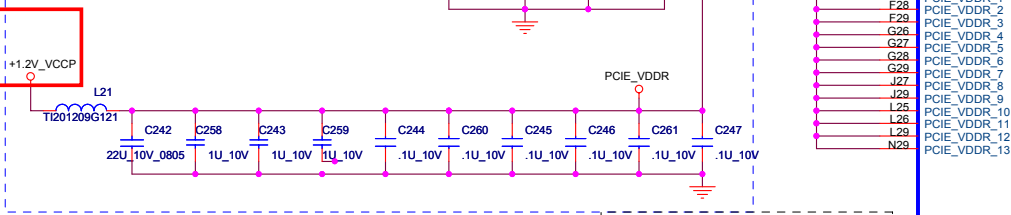
CLKREQA# CONTROL SRC5,6,7
 CLKREQB# CONTROL SRC2,3,4, ATIG3
 CLKREQC# CONTROL SRC0,1,ATIG0/1/2

Title: CLOCK GENERATOR

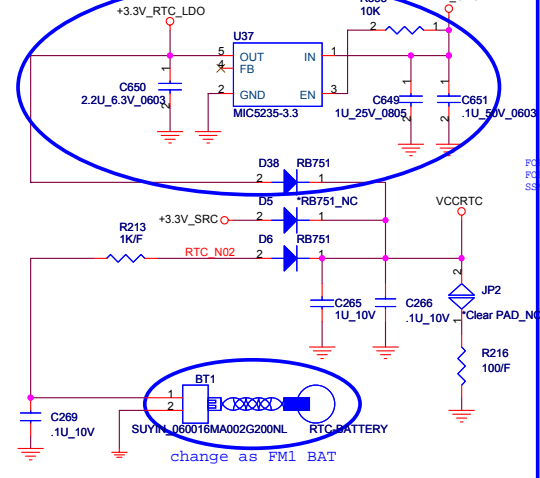
Size: FX2	Document Number: FX2	Rev: 1A
Date: Friday, May 05, 2006	Sheet: 13	of 47

SB CALIBRATION RESISTOR VALUE		
BALL	SB600	SB460
CALRP	562 OHM 1%	150 OHM 1%
CALRN	2.05K 1%	150 OHM 1%
CALI	0 ohm	4.12K 1%

PCIE Power

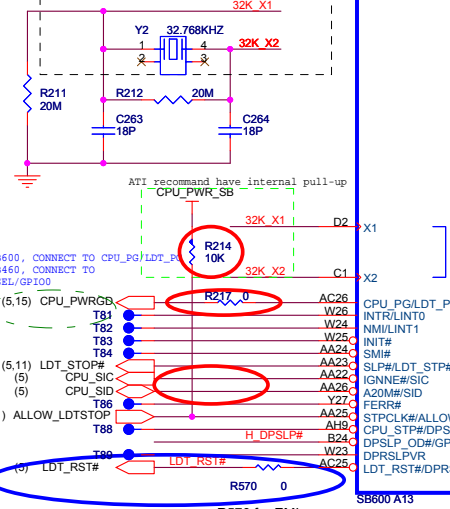


RTC add +3.3V LDO circuit for VCCRTC



0503 : pull down for SB600 , reserve R229 connected to +3.3V_RUN

ATI Recommend Vendor: NSK Part Number: NXG 32.768KAE12FD 16 PPM.



reserve R570 for EMI verifying, place close to SB

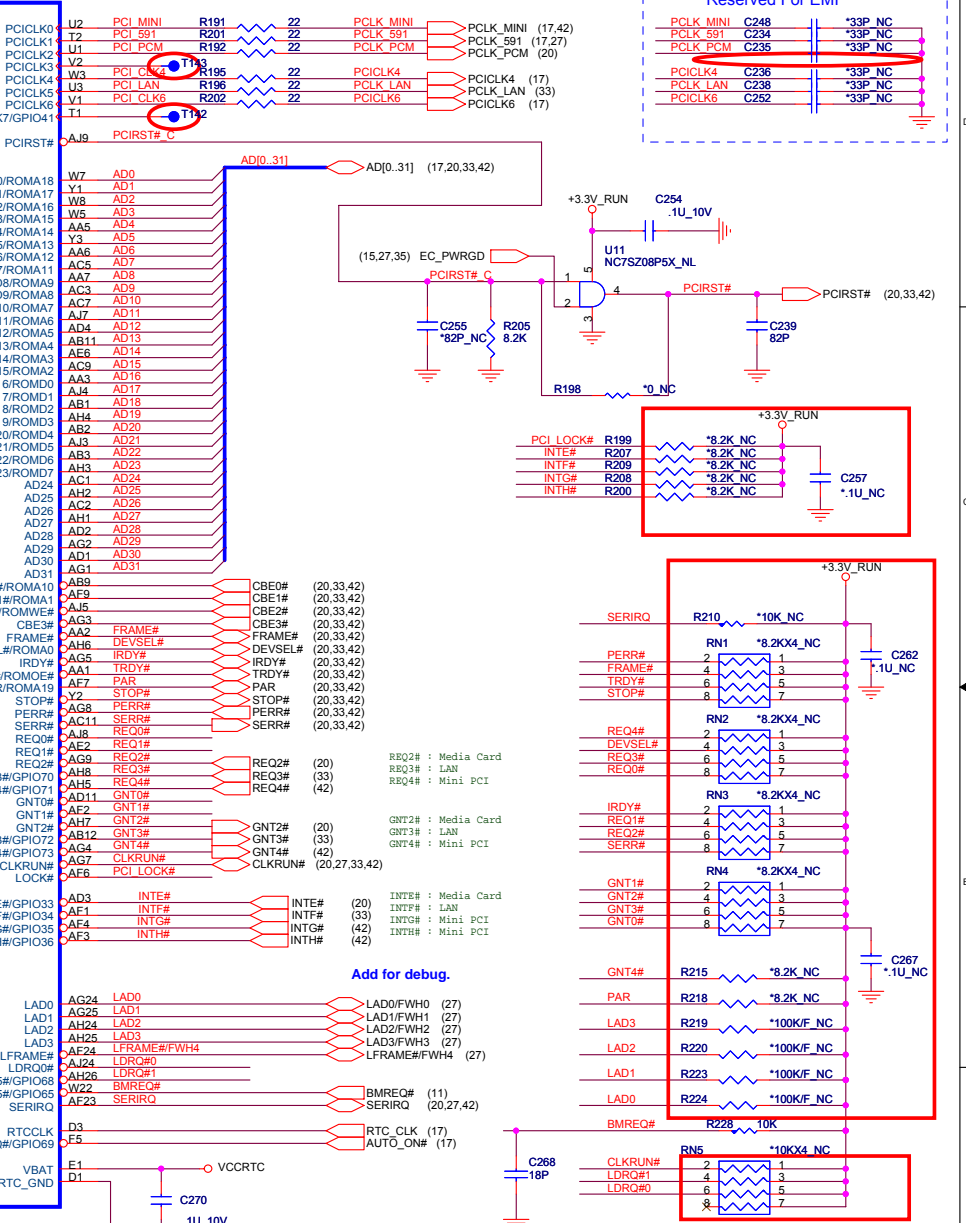
H_DPSLP# should be put down, reserve R229 for verifying

PCI EXPRESS INTERFACE

PCI INTERFACE

LPC

RTC



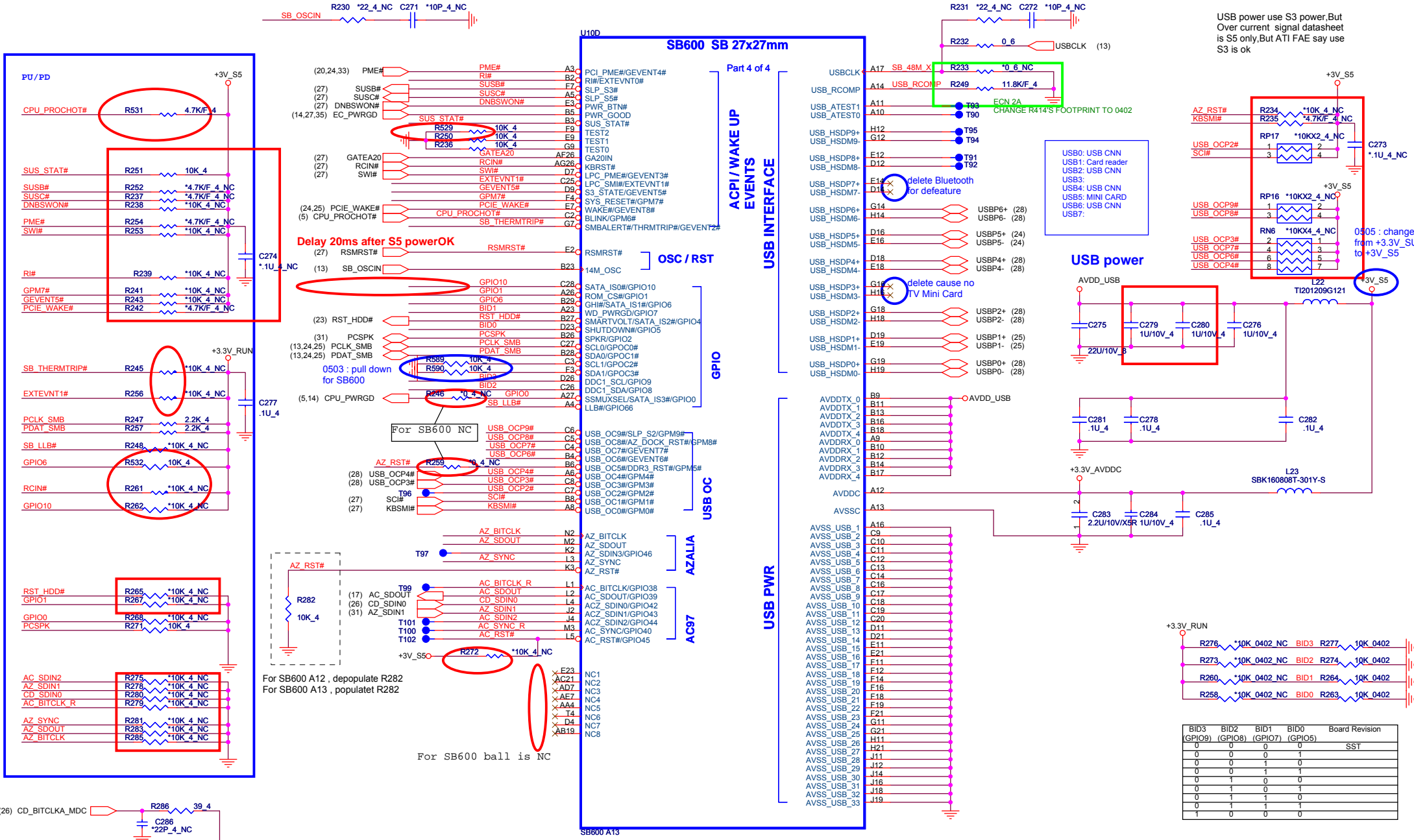
Reserved For EMI

PCLK_MINI	C248	*33P_NC
PCLK_S91	C234	*33P_NC
PCLK_PCM	C235	*33P_NC
PCICLK4	C236	*33P_NC
PCICLK_LAN	C238	*33P_NC
PCICLK6	C262	*33P_NC

PCI_LOCK#	R199	*8.2K_NC
INTE#	R207	*8.2K_NC
INTF#	R209	*8.2K_NC
INTG#	R208	*8.2K_NC
INTH#	R200	*8.2K_NC

SERIRQ	R210	*10K_NC
PERR#	RN1	*8.2KX4_NC
FRAME#	2	1
TRDY#	4	3
STOP#	6	5
REQ0#	8	7
REQ4#	RN2	*8.2KX4_NC
DEVSEL#	2	1
REQ3#	4	3
REQ0#	6	5
REQ0#	8	7
IRDY#	RN3	*8.2KX4_NC
REQ0#	2	1
REQ2#	4	3
REQ3#	6	5
SERR#	8	7
GNT1#	RN4	*8.2KX4_NC
GNT2#	2	1
GNT3#	4	3
GNT#	6	5
GNT#	8	7
GNT4#	R215	*8.2K_NC
PAR	R218	*8.2K_NC
LAD3	R219	*100KF_NC
LAD2	R220	*100KF_NC
LAD1	R223	*100KF_NC
LAD0	R224	*100KF_NC
BMREQ#	R228	10K
CLKRUN#	RN5	*10KX4_NC
LDRQ#1	2	1
LDRQ#0	4	3
LDRQ#0	6	5
LDRQ#0	8	7





USB power use S3 power, But Over current signal datasheet is S5 only, But ATI FAE say use S3 is ok

USB0: USB CNN
 USB1: Card reader
 USB2: USB CNN
 USB3:
 USB4: USB CNN
 USB5: MINI CARD
 USB6: USB CNN
 USB7:

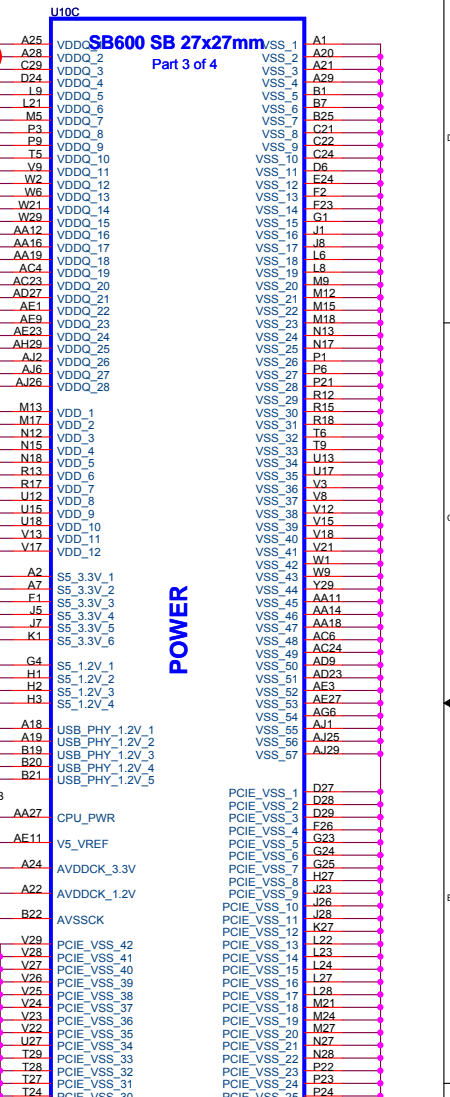
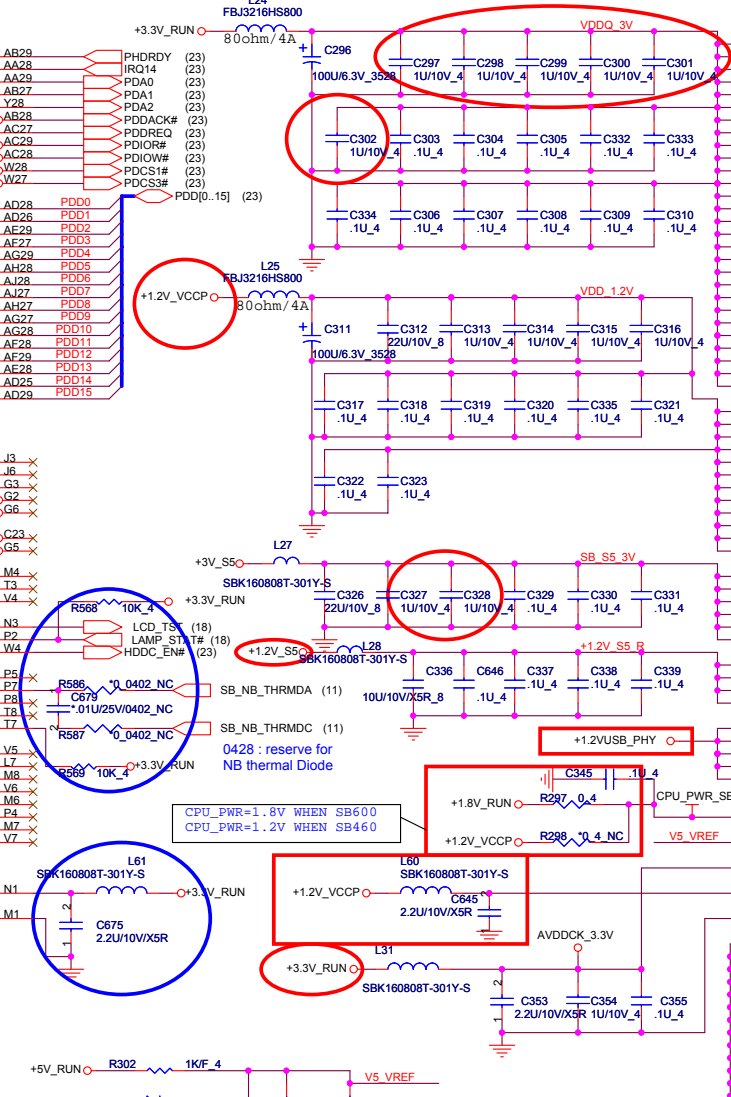
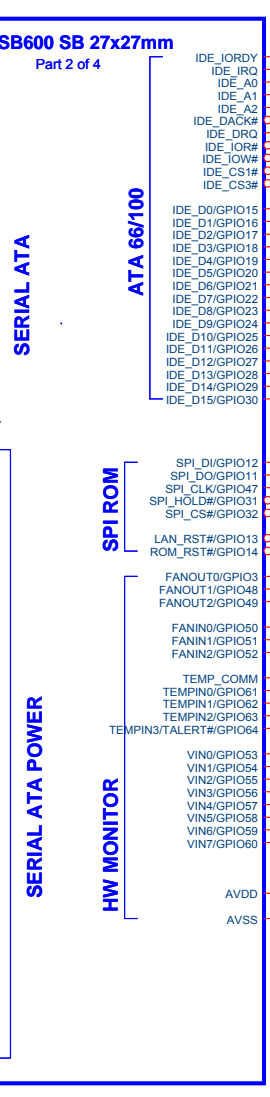
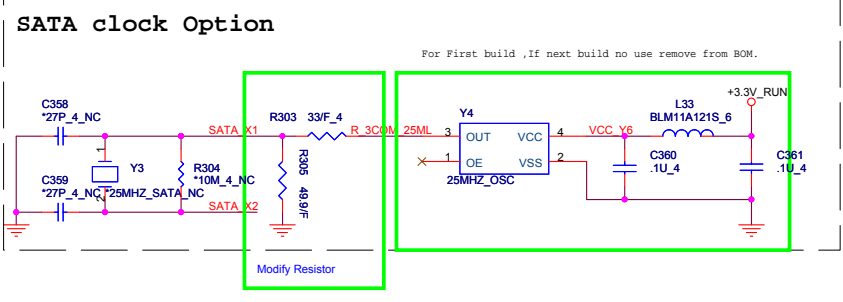
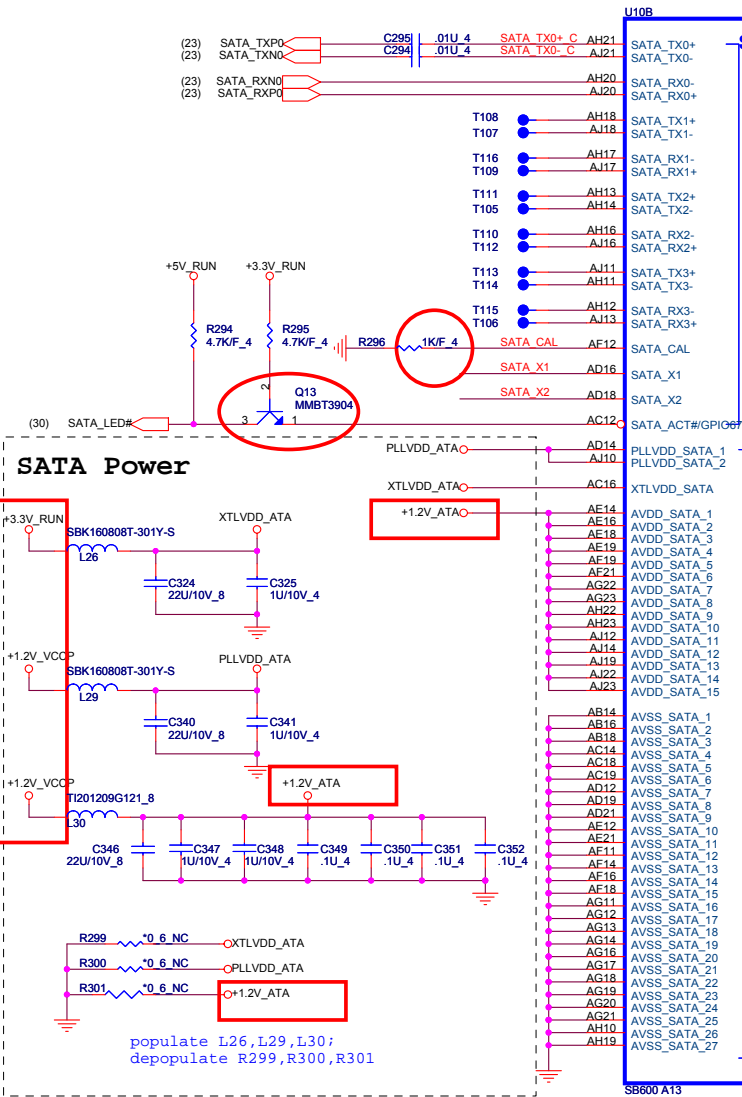
0505 : change from +3.3V_S5 to +3V_S5

BID3 (GPIO9)	BID2 (GPIO8)	BID1 (GPIO7)	BID0 (GPIO5)	Board Revision
0	0	0	0	SST
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
0	1	1	1	
1	0	0	0	

QUANTA COMPUTER

File: SB600M ACPI/USB/AC97

Size	Document Number FX2	Rev 1A
Date:	Friday, May 05, 2006	Sheet 15 of 47



QUANTA COMPUTER

Title: SB600M HDD/POWER

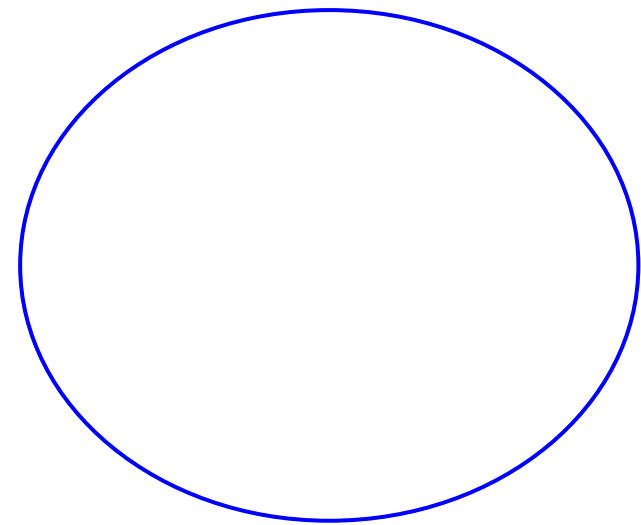
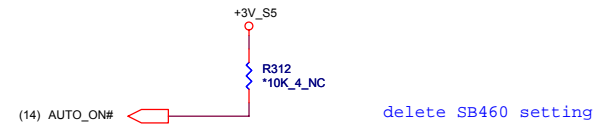
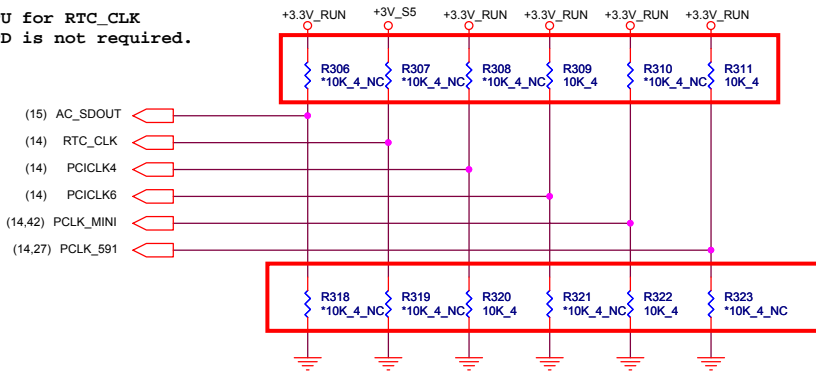
Size: Document Number FX2

Rev: 1A

Date: Friday, May 05, 2006

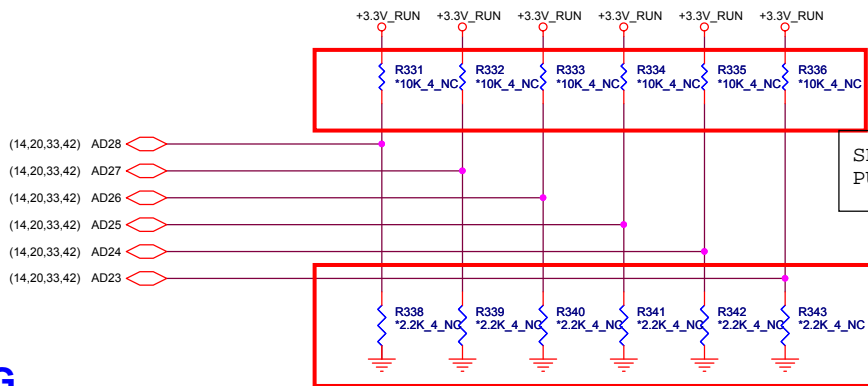
Sheet: 16 of 47

SB600 has 15K internal PD for AC_SDOUT
 15K internal PU for RTC_CLK
 ,External PU/PD is not required.



REQUIRED STRAPS

					PCLK_MINI	PCLK_591
PULL HIGH	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	H, H = PCI ROM H, L = SPI ROM	
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	L, H = LPC ROM	DEFAULT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	L, L = FWH ROM	



SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	Use Long Reset	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	boot fail time disabled
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled

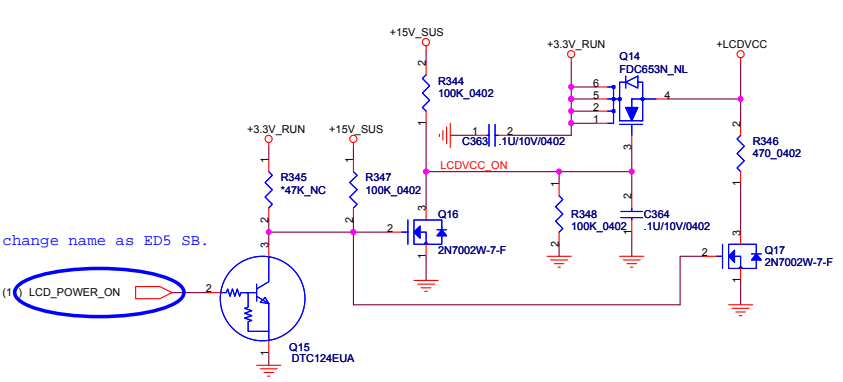
SB460 Only

SB600 Only

SB600 Only

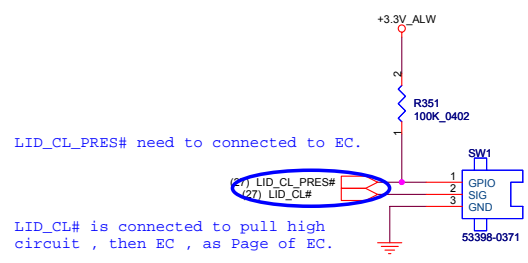


Title SB600M STRAPS		
Size	Document Number FX2	Rev 1A
Date:	Friday, May 05, 2006	Sheet 17 of 47



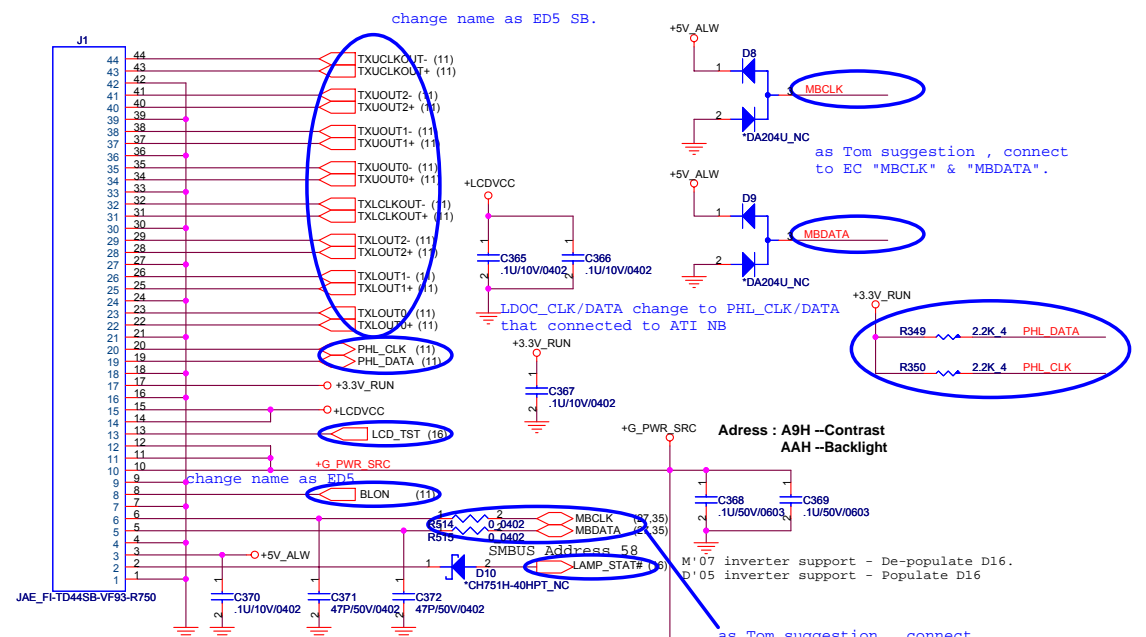
change name as ED5 SB.

(1) LCD_POWER_ON



LID_CL_PRES# need to connected to EC.

LID_CL# is connected to pull high circuit , then EC , as Page of EC.



change name as ED5 SB.

as Tom suggestion , connect to EC "MBCLK" & "MBDATA".

LDO0_CLK/DATA change to PHL_CLK/DATA that connected to ATI NB

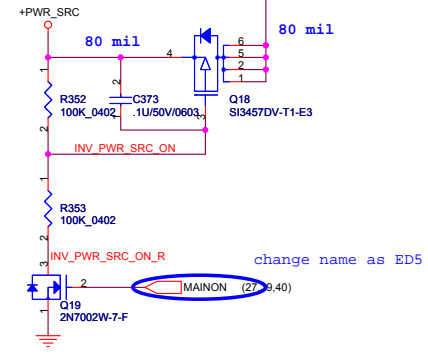
Address : A9H --Contrast
AAH --Backlight

M'07 inverter support - De-populate D16.
D'05 inverter support - Populate D16

as Tom suggestion , connect to EC "MBCLK" & "MBDATA".

For Discrete:
De-populate J1,R230,C311,C331,C332,
D16,C333,C329,C341,C324,C326

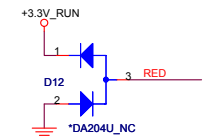
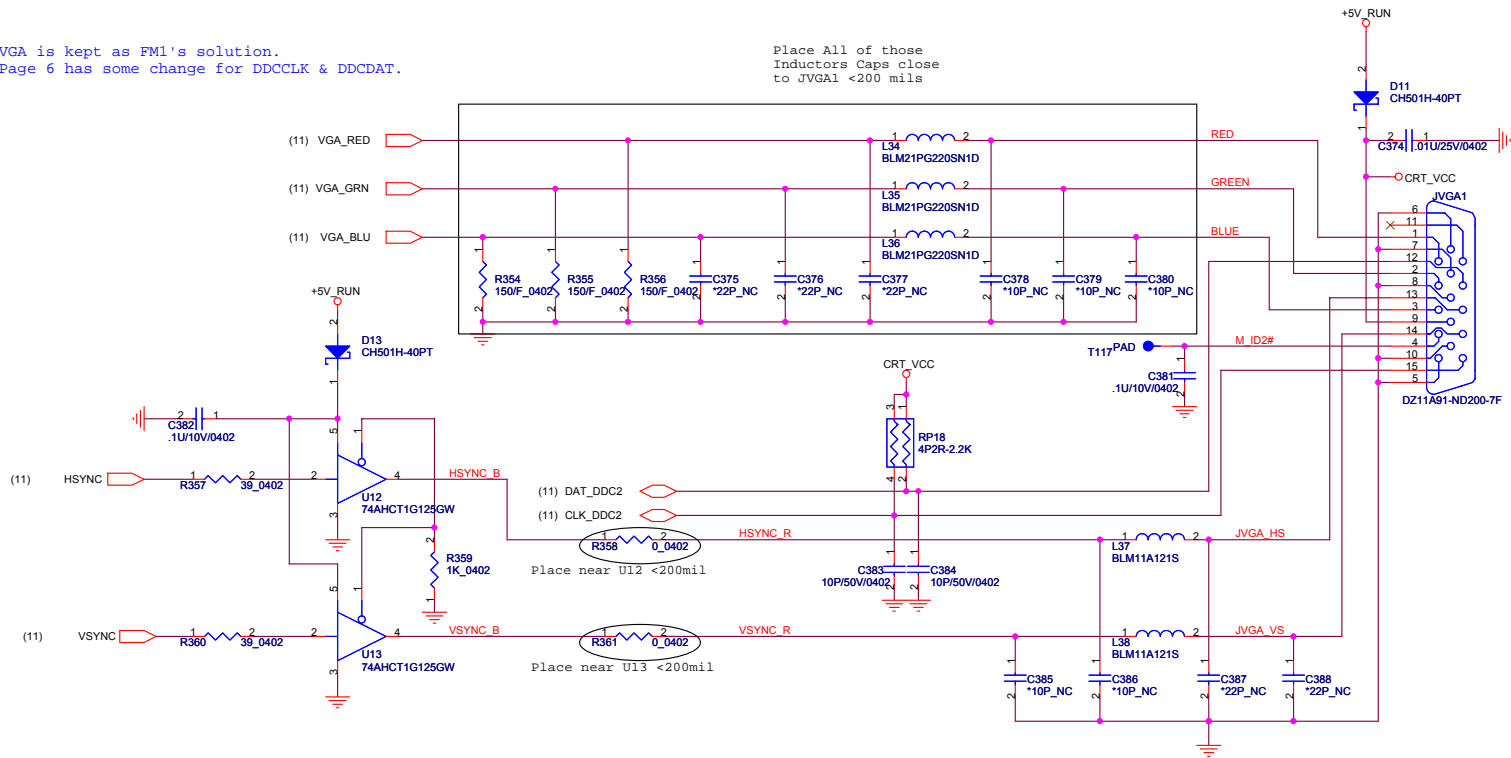
On FM1,LCD_TST & LAMP_STAT connect to SB ; on FX2 ??.



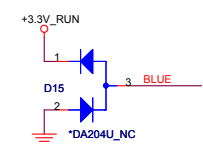
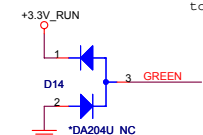
change name as ED5

VGA is kept as FMI's solution.
 Page 6 has some change for DDCLK & DDCDAT.

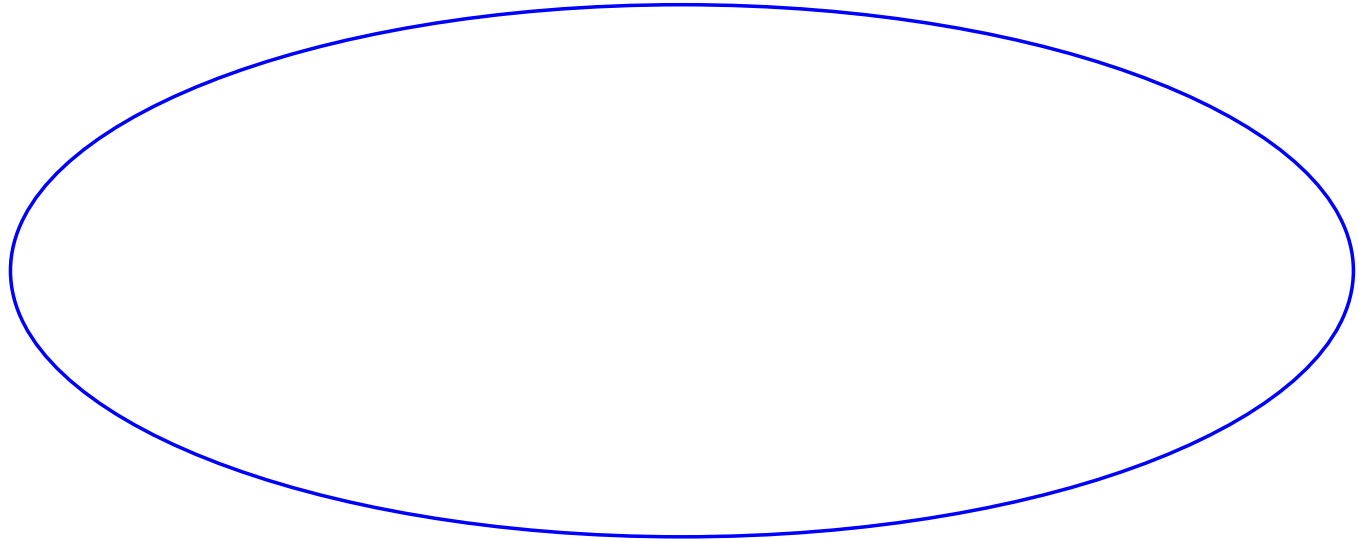
Place All of those
 Inductors Caps close
 to JVG1 <200 mils

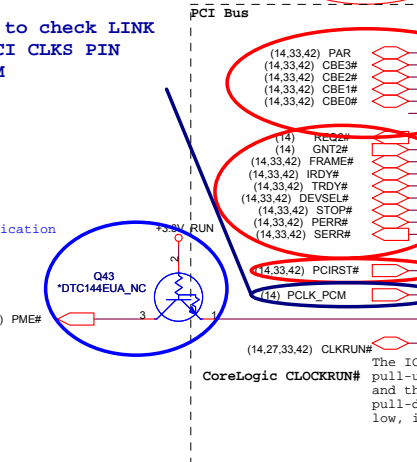
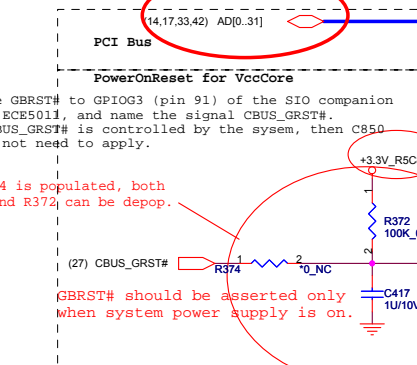
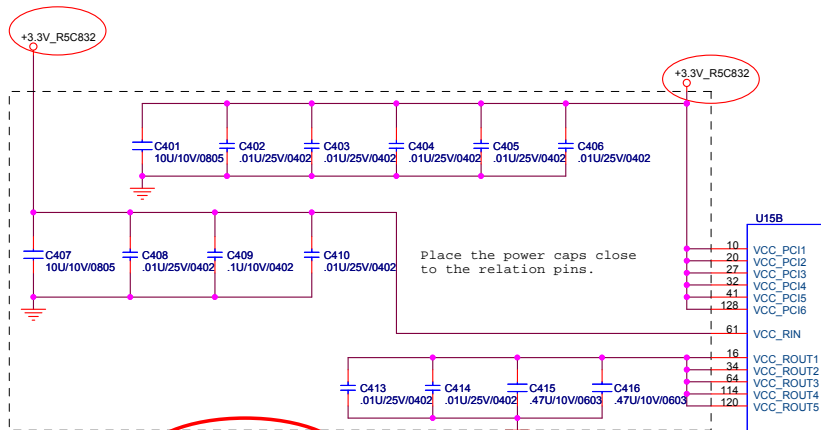


Place D4,D5,D6 close
 to JVG1 <200 mils



delete Svideo for defeature

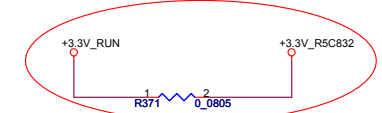
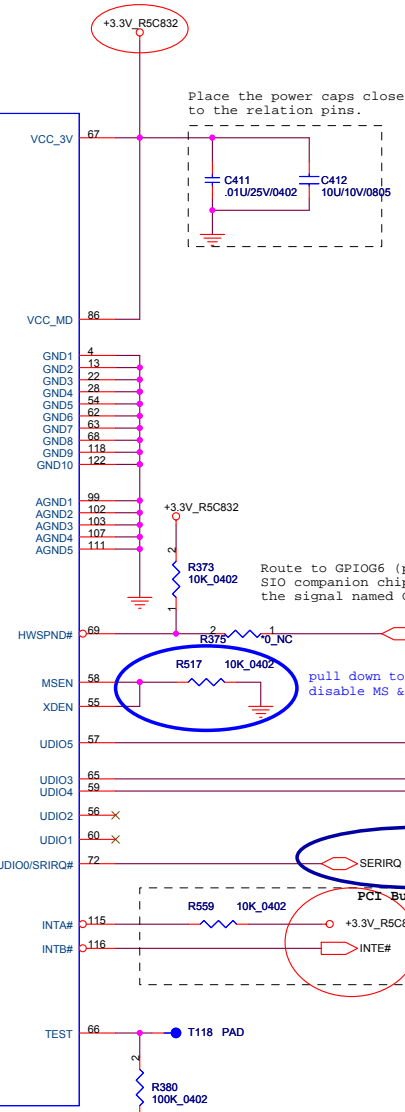




U15B

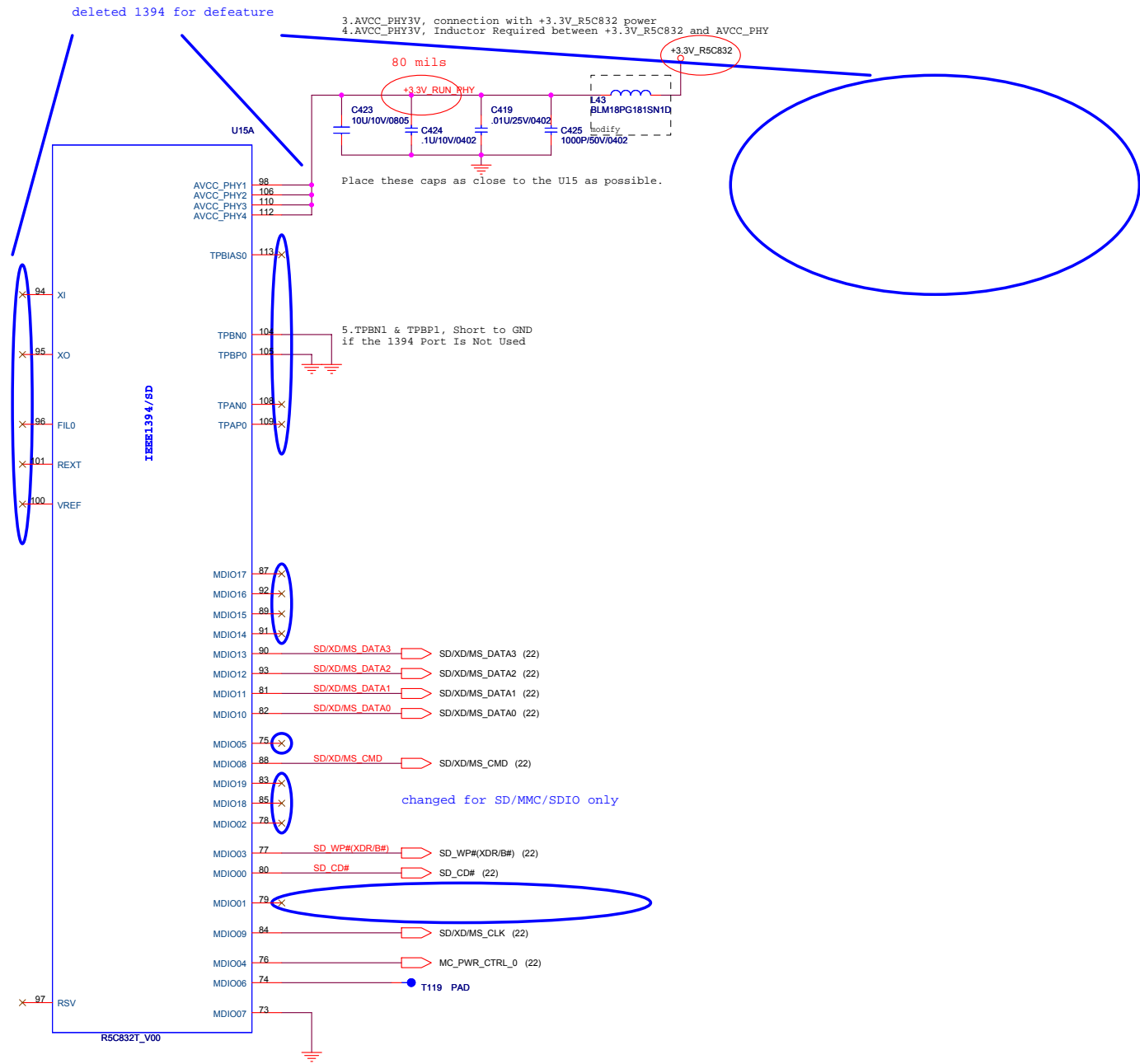
10	VCC_PCI1
20	VCC_PCI2
27	VCC_PCI3
32	VCC_PCI4
41	VCC_PCI5
128	VCC_PCI6
61	VCC_RIN
18	VCC_ROUT1
34	VCC_ROUT2
64	VCC_ROUT3
114	VCC_ROUT4
120	VCC_ROUT5
125	AD31
126	AD30
127	AD29
2	AD28
3	AD27
5	AD26
6	AD25
8	AD24
9	AD23
11	AD22
12	AD21
14	AD20
15	AD19
17	AD18
18	AD17
19	AD16
36	AD15
37	AD14
38	AD13
39	AD12
40	AD11
42	AD10
43	AD9
44	AD8
46	AD7
47	AD6
48	AD5
49	AD4
50	AD3
51	AD2
52	AD1
53	AD0
33	PAR
7	CBE2#
21	CBE1#
35	CBE0#
45	IDSEL
124	REQ#
123	GNT#
23	FRAME#
24	IRDY#
25	TRDY#
26	DEVSEL#
29	STOP#
30	PERR#
31	SERR#
71	GBRST#
119	PCIRST#
121	PCICLK
70	PME#
117	CLKRUN#

PCI / OTHER



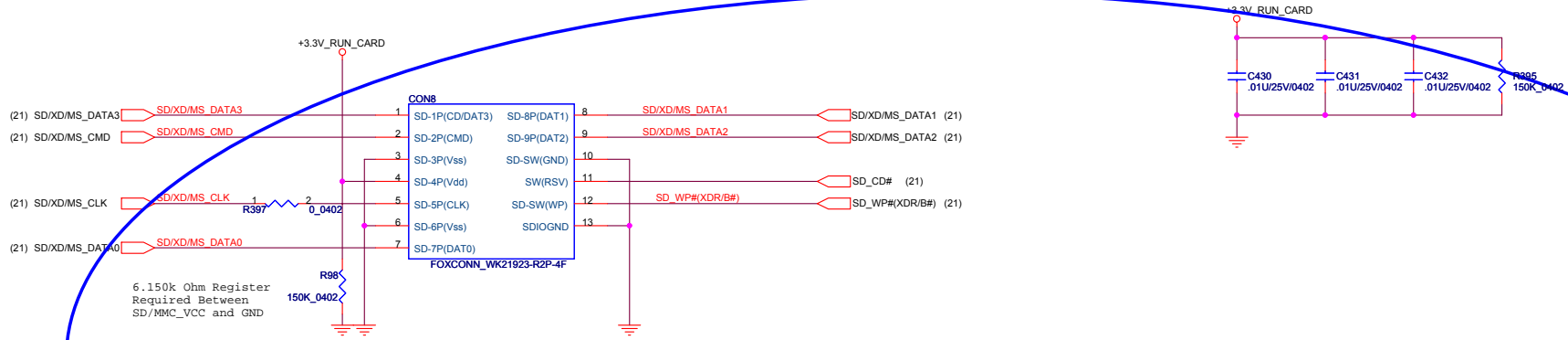
— change name for ED5
 — copy ED5 to FX2
 — Waiting to check

Waiting to check
 LINK SB460
 SERIRQ PIN
 PCLK_PCM



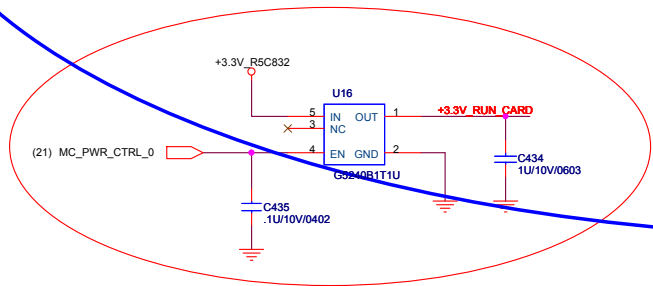
DO NOT INSERT SD/MMC SIMULTANEOUSLY.

changed for SD/MMC/SDIO only

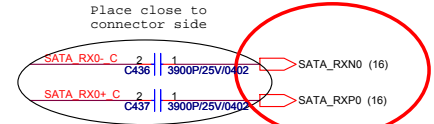
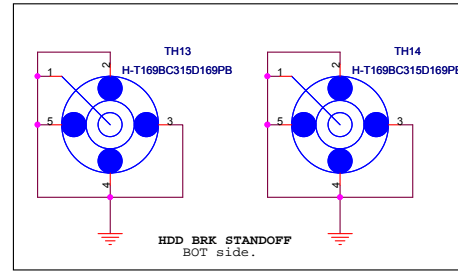


3 IN 1 CARD READER

For SD/MS power



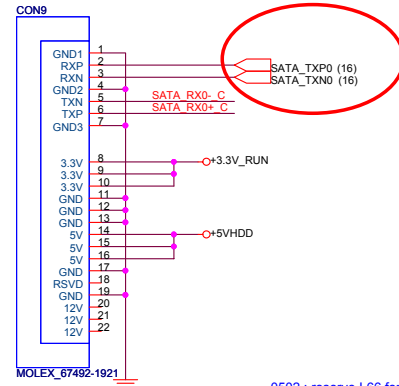
SATA HDD



Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

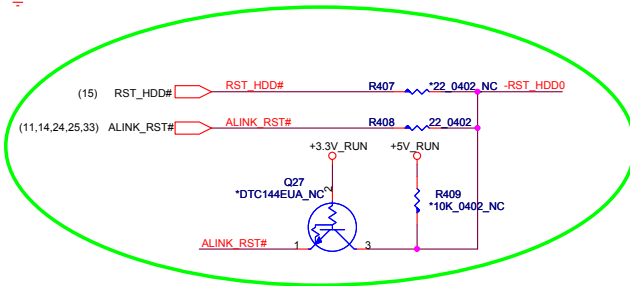
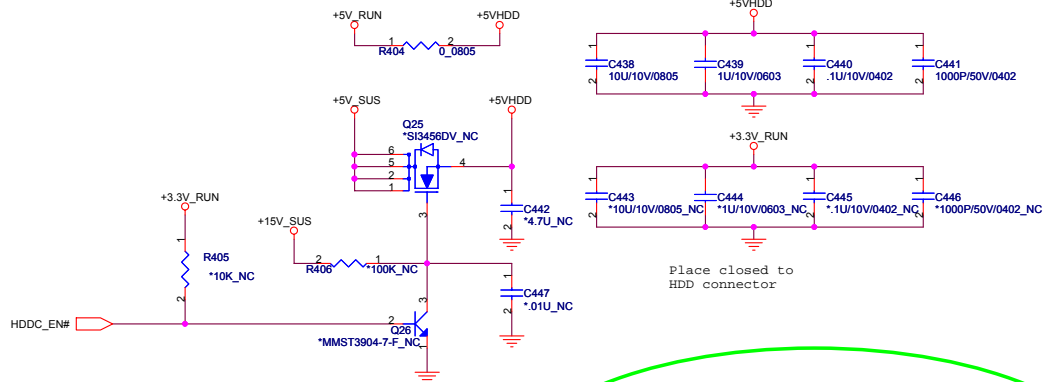
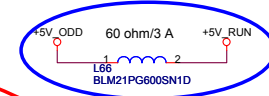
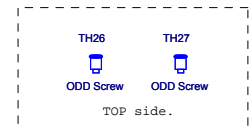
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

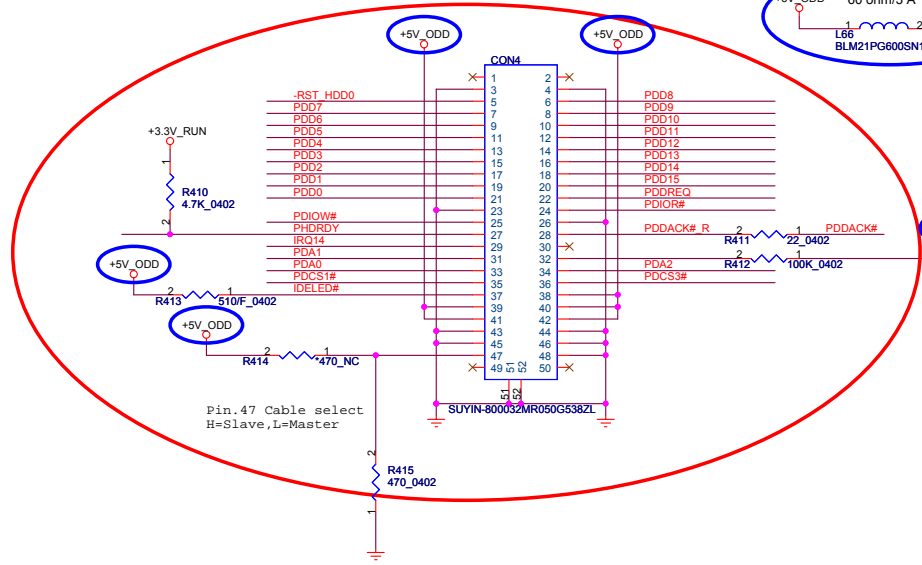
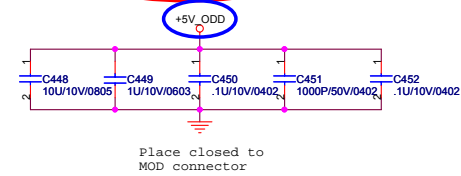
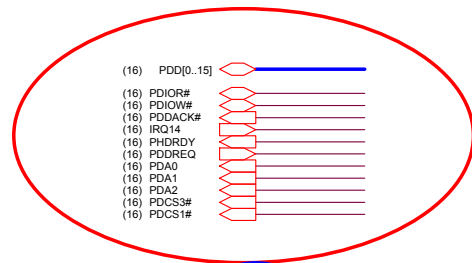


- change name for ED5
- copy ED5 to FX2
- Waiting to check

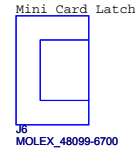
0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power



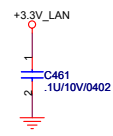
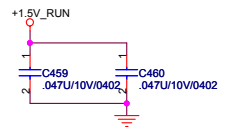
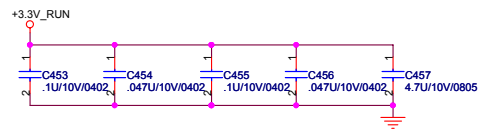
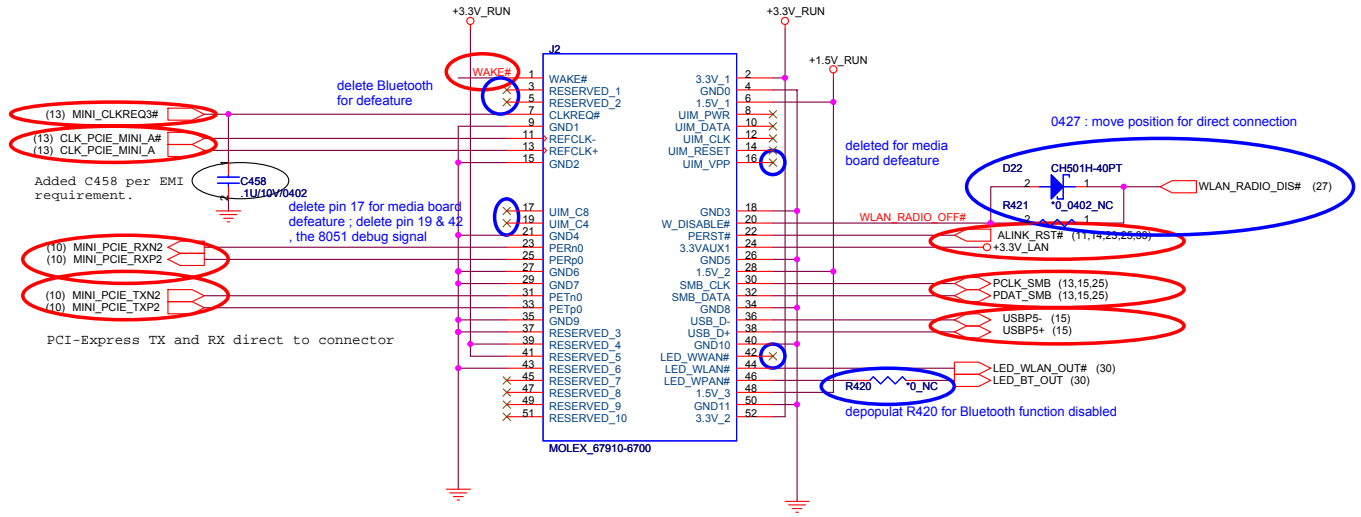
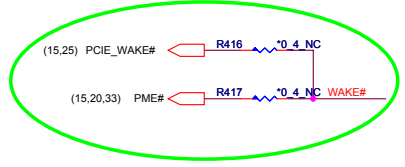
PATA ODD



MINI CARD



- change name for ED5
- copy ED5 to FX2
- Waiting to check



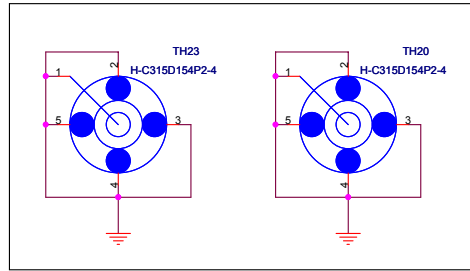
**QUANTA
COMPUTER**

Title: MINI Card

Size: FX2	Document Number: FX2	Rev: 1A
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Date: Friday, May 05, 2006 Sheet: 24 of 47

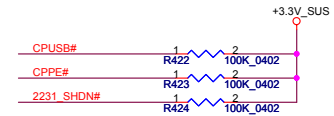
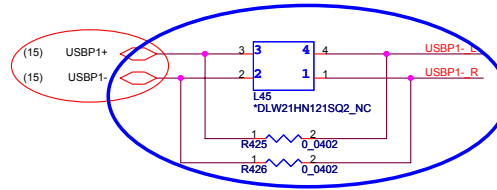
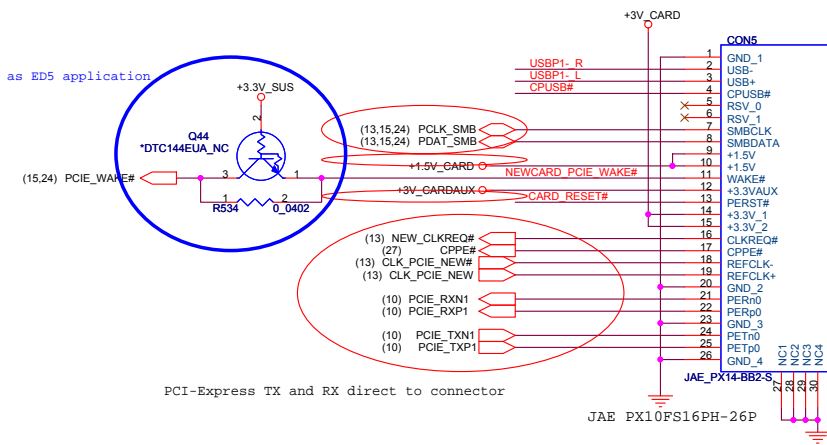
Express Card



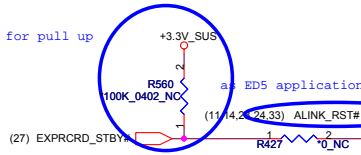
- change name for ED5
- copy ED5 to FX2
- Waiting to check

NEW CARD GUIDE POST
TOP side.

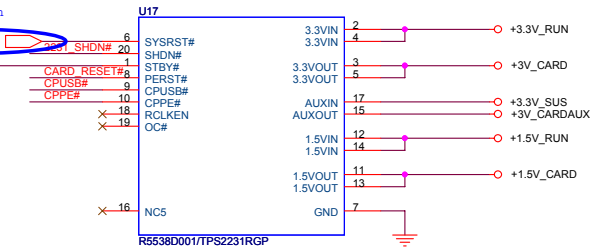
swap traces as "fx2_swap-0412"



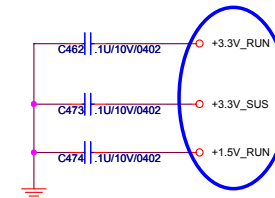
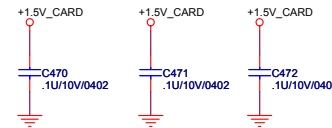
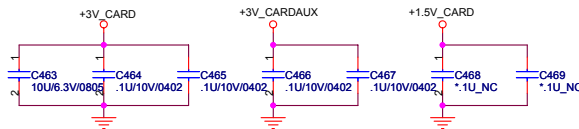
reserve for pull up



+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



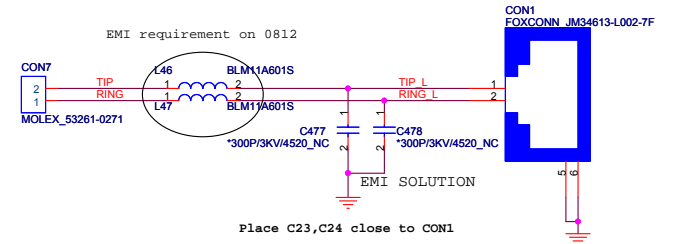
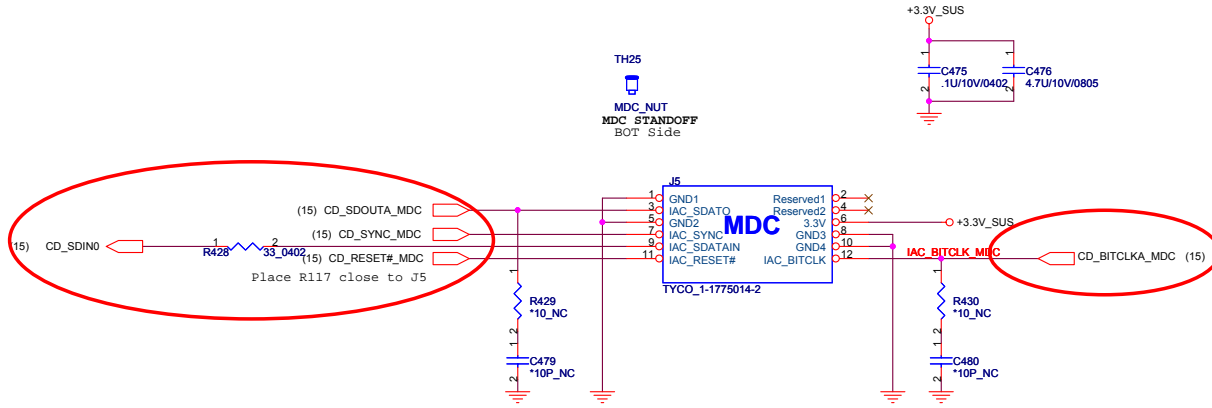
0427 : change from only net name to symbol "power point"

MDC INTERFACE

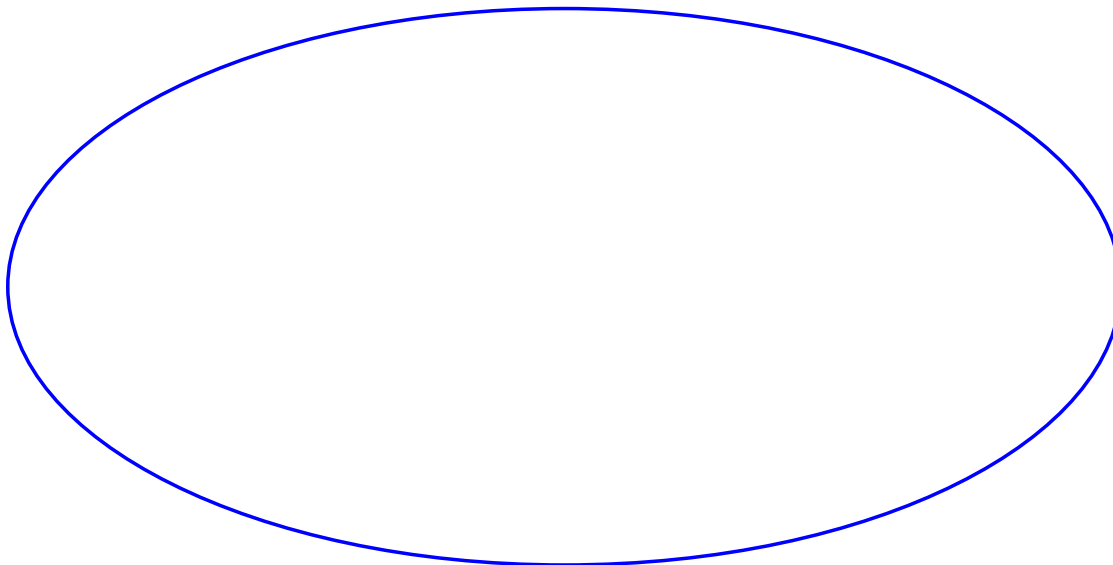
MDC Layout Notes

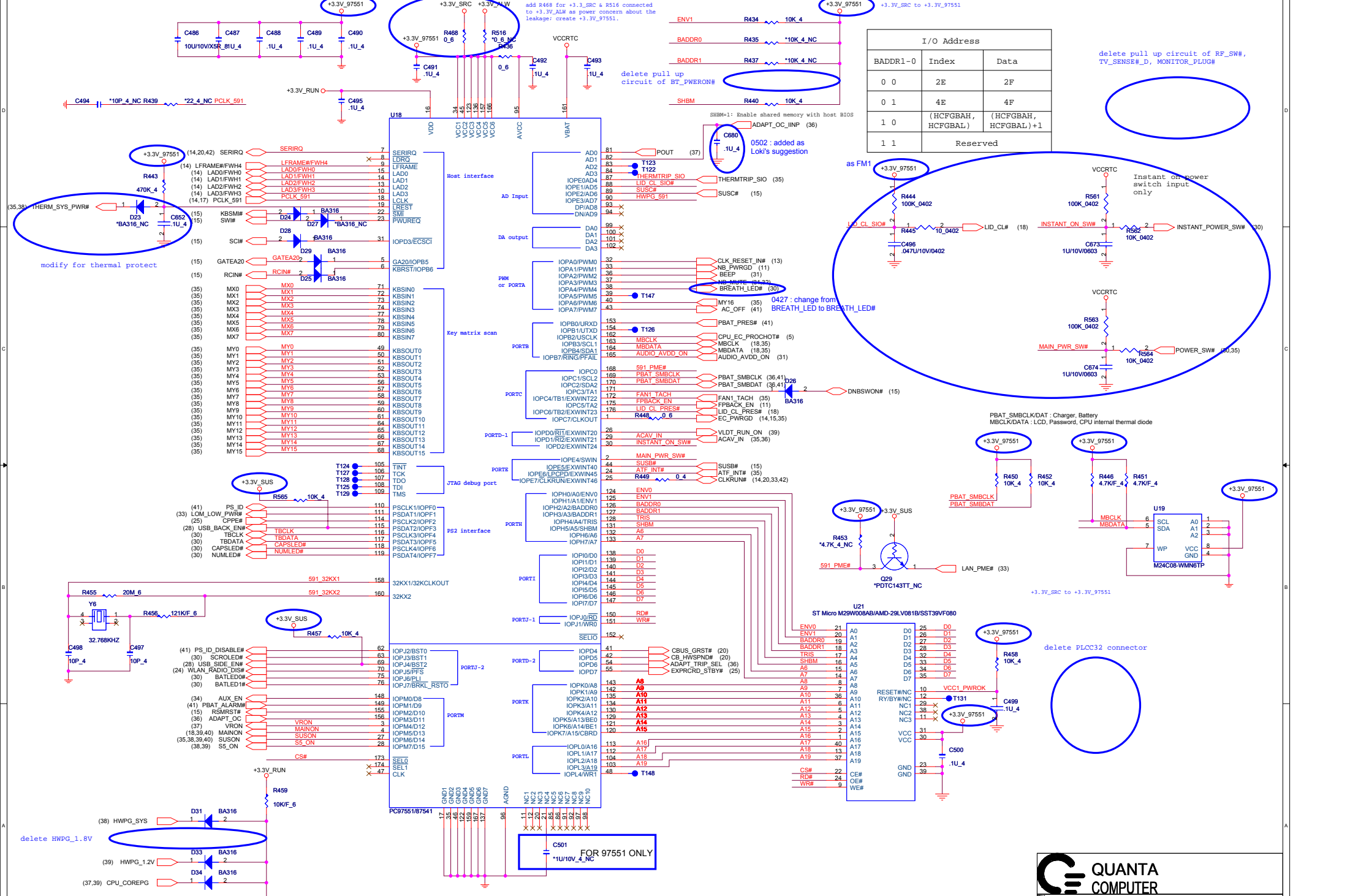
1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG (stranded or twisted pair wire)

- change name for ED5
- copy ED5 to FX2
- Waiting to check

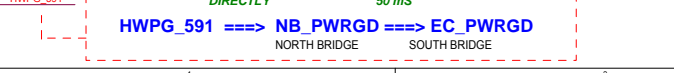


delete Bluetooth
for defeature





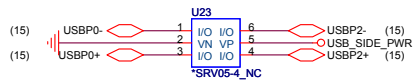
EC & FLASH ROM



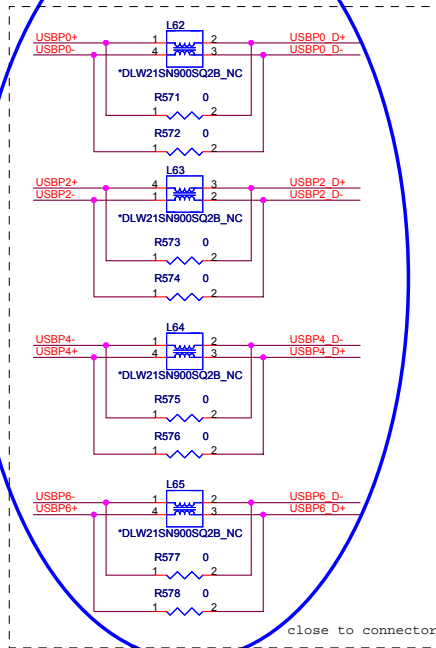
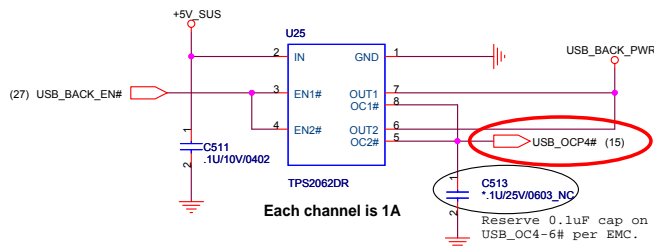
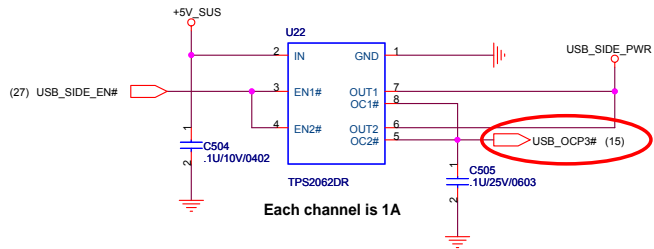
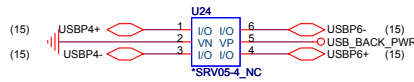
8Mbit (1M Byte), SPI



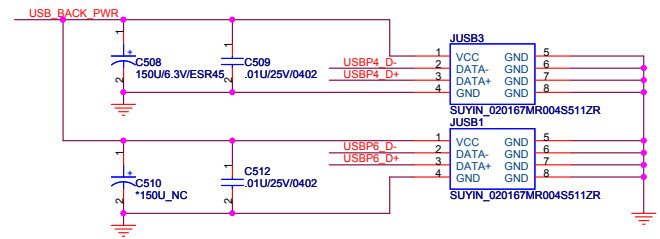
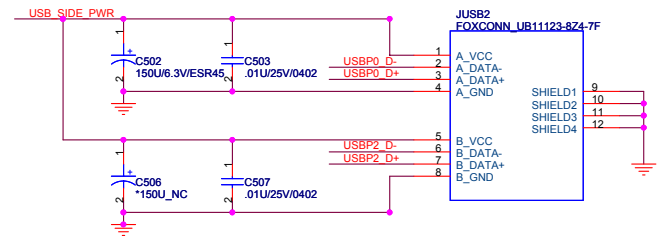
- change name for ED5
- copy ED5 to FX2
- Waiting to check



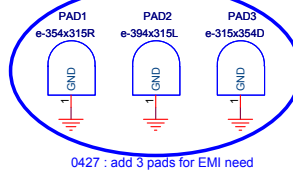
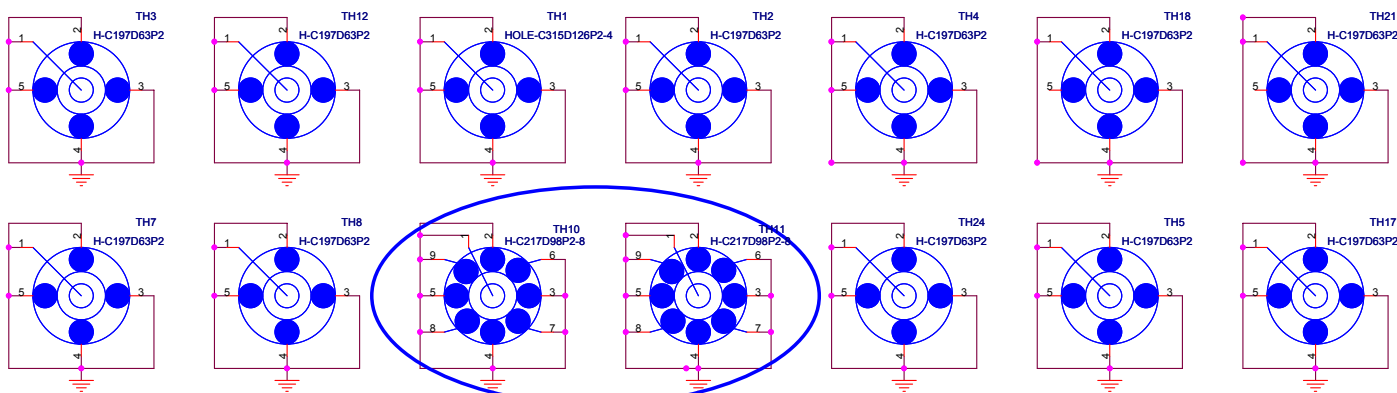
Place ESD diodes as close as USB connector.



add for EMI suggestion ,
0502 : swap P0/P2 traces as "fx2-swap-0502"

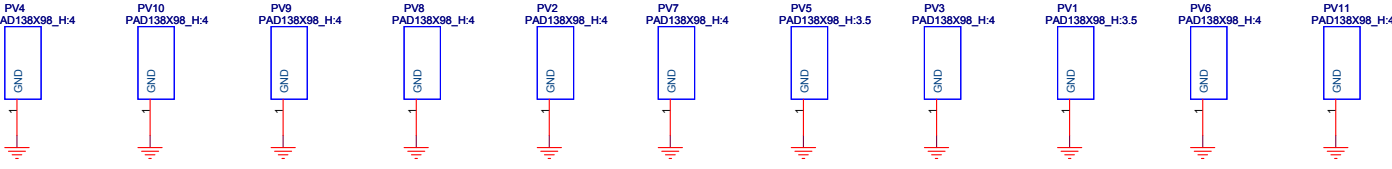


Title USB			Rev 1A
Size FX2	Document Number FX2	Date Friday, May 05, 2006	
Sheet 28		of 47	

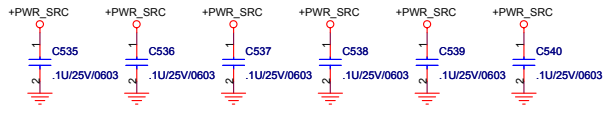
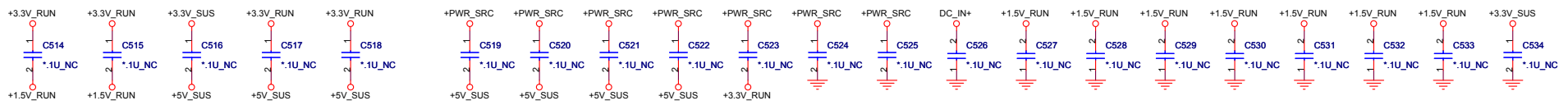


0427 : add 3 pads for EMI need

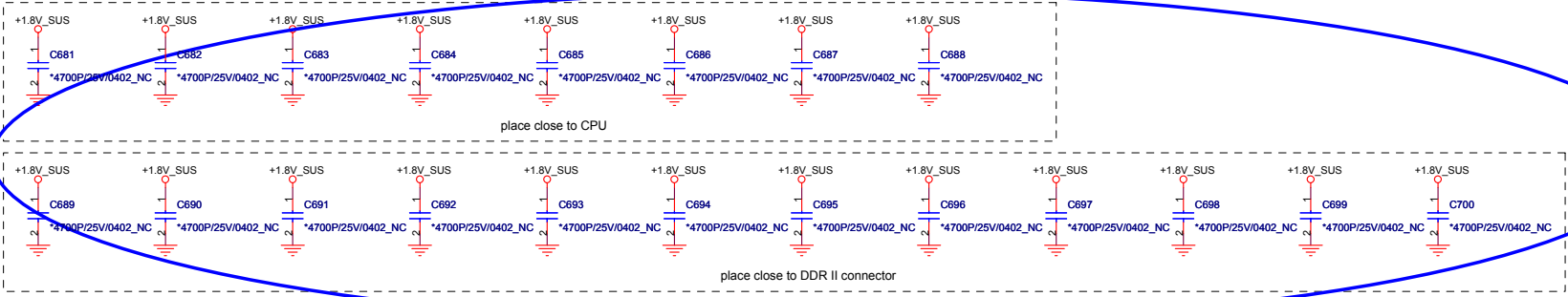
change footprint from "H-C315D98P2-4" to "H-C217D98P2-8".

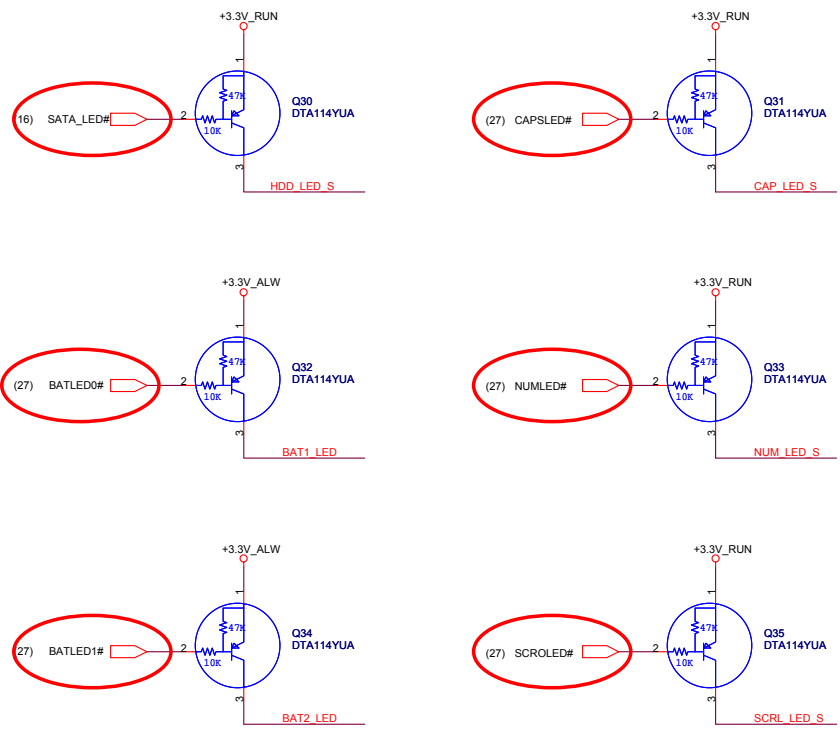


0505 : delete PV12 , caused interference with power component , EMI confirm no concern

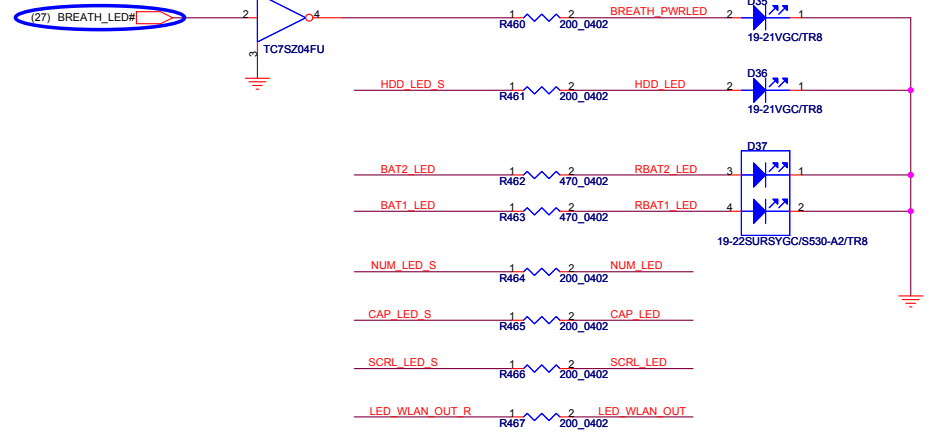


0502 : reserve 20 pcs of 4700pF stitching Cap. from +1.8V_SUS to GND for EMI concern

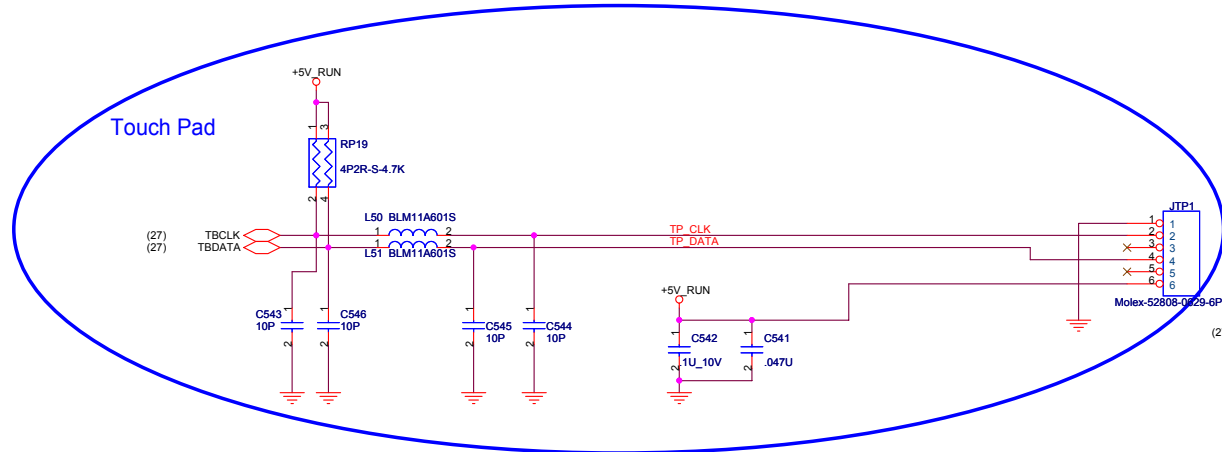




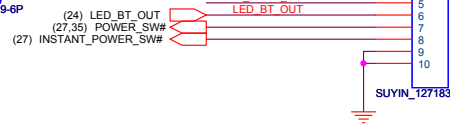
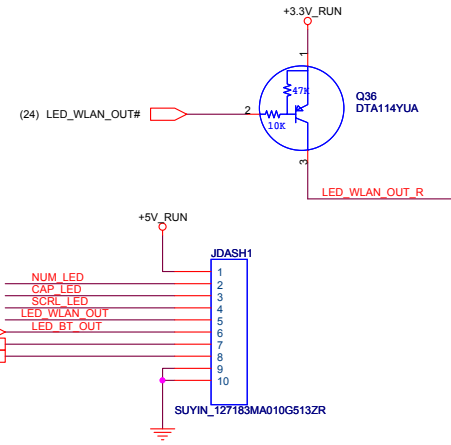
0427 : change from BREATHE_LED to BREATHE_LED#

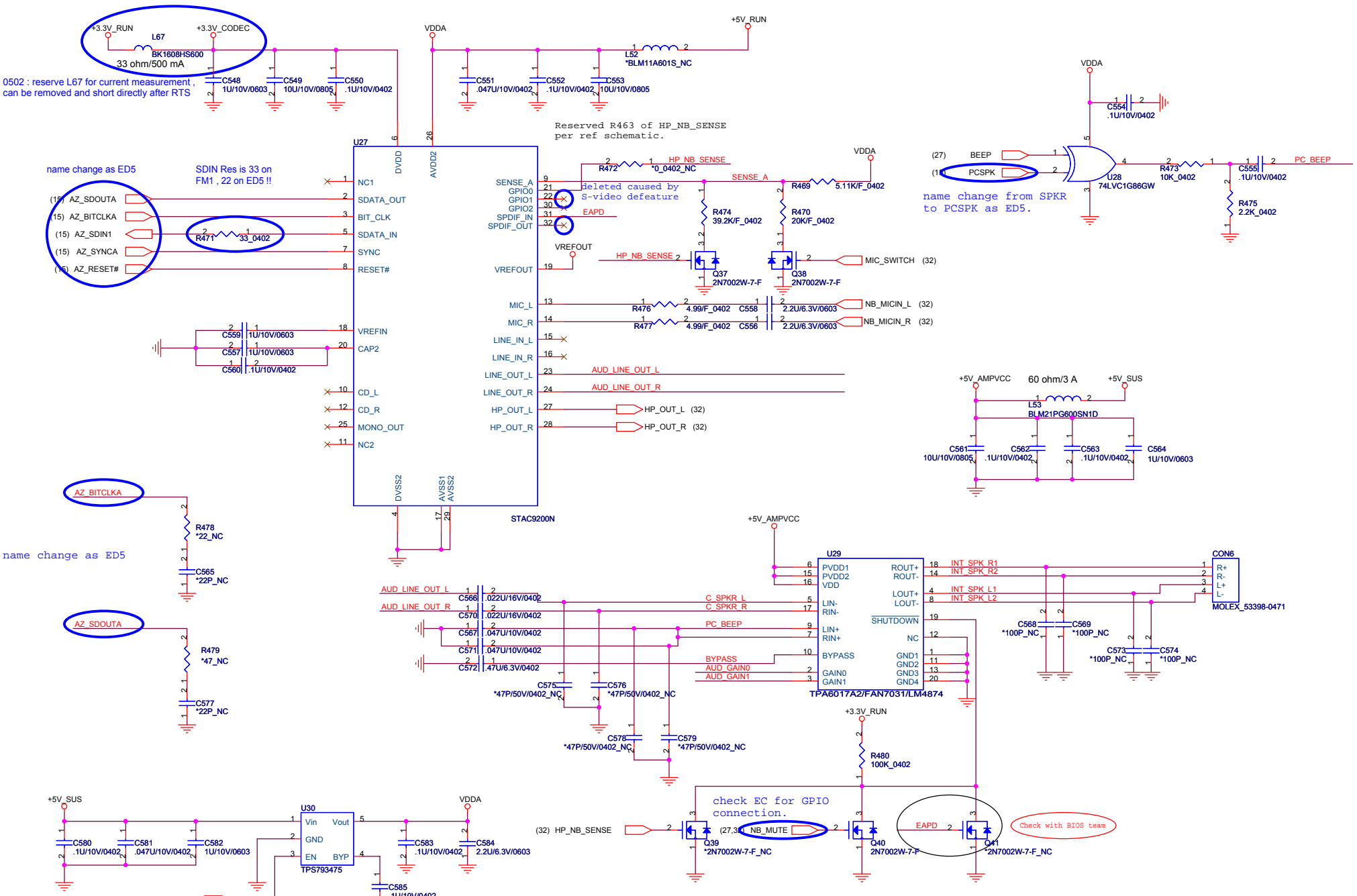


— change name for ED5
 — copy ED5 to FX2
 — Waiting to check



FM1 media board changed to TP only as DM5





0502 : reserve L67 for current measurement , can be removed and short directly after RTS

name change as ED5

SDIN Res is 33 on FM1 , 22 on ED5 !!

Reserved R463 of HP_NB_SENSE per ref schematic.

name change from SPKR to PCSPK as ED5.

name change as ED5

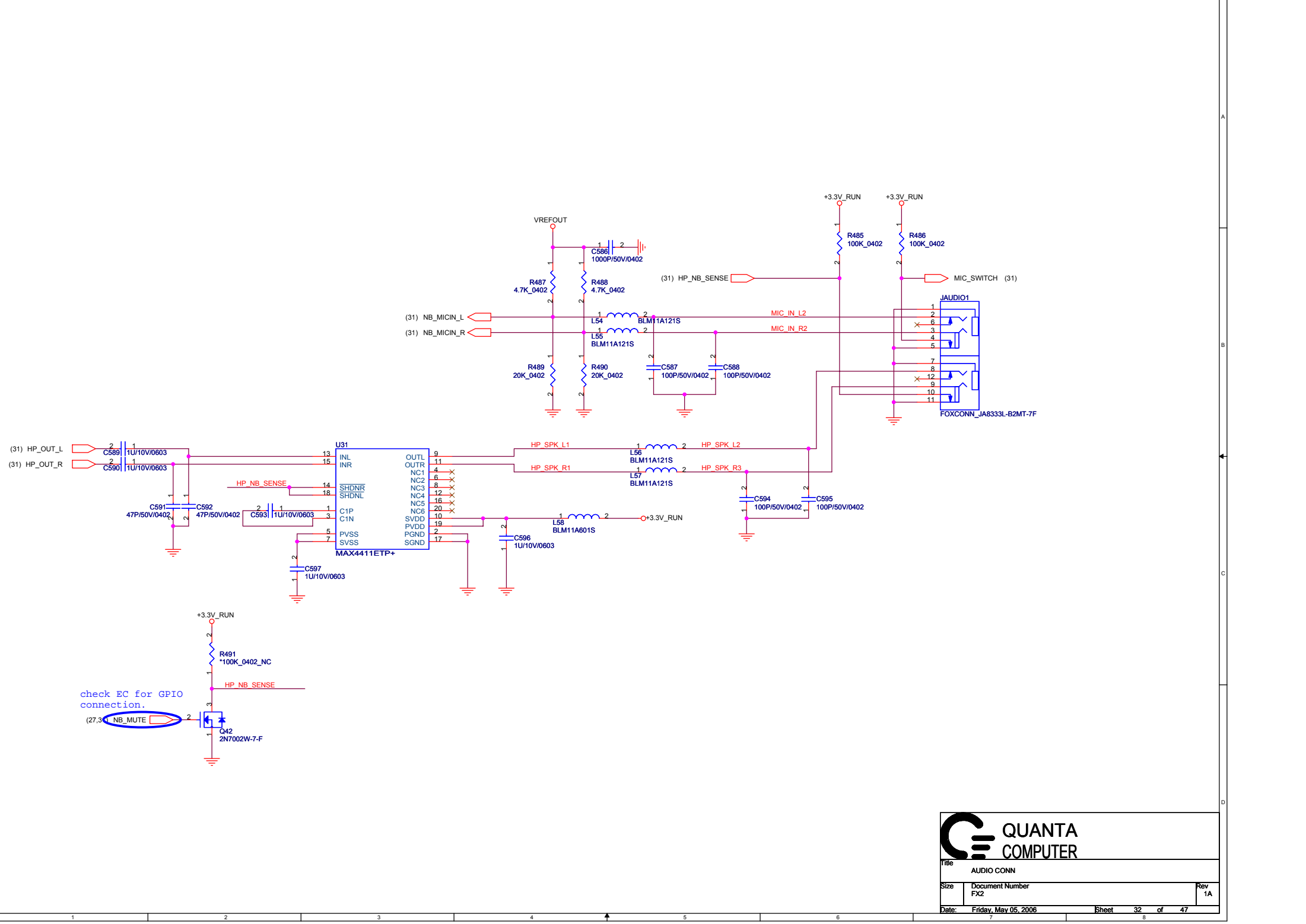
check EC for GPIO connection.

Check with BIOS team

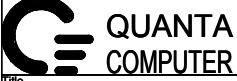
GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

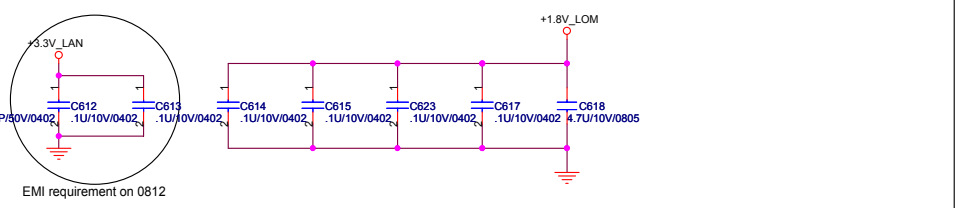
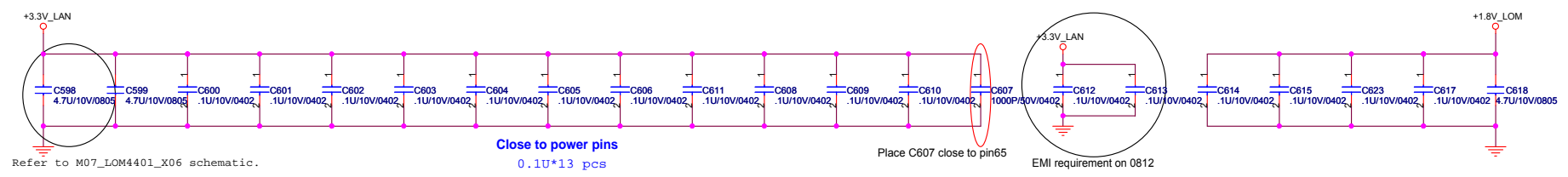


Title		Azella CODEC
Size	Document Number	Rev
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check EC for GPIO connection.

		
QUANTA COMPUTER		
Title: AUDIO CONN		
Size:	Document Number:	Rev:
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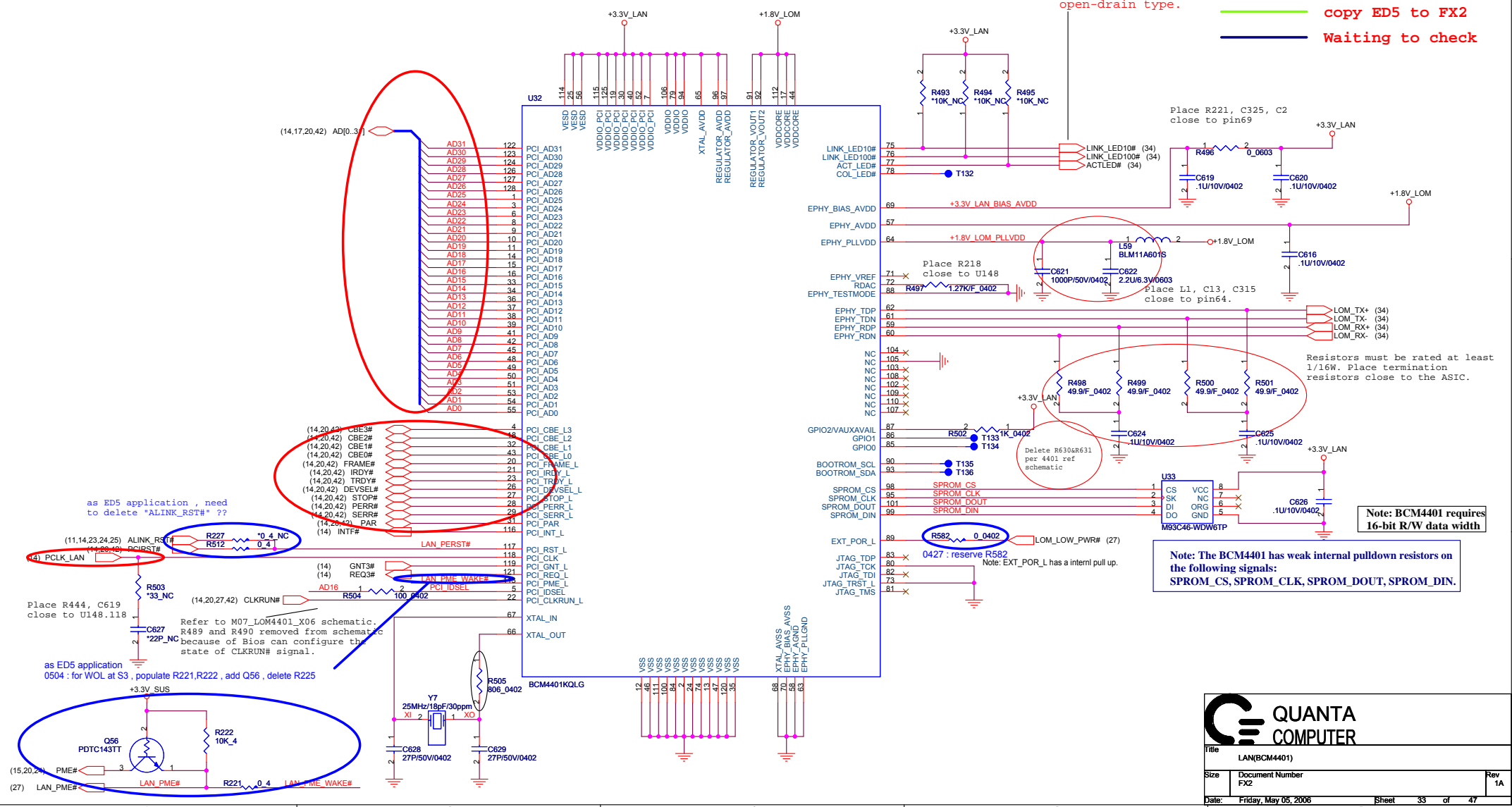


These three pin LINK_LED10#, LINK_LED100#, ACT_LED are open-drain type.

change name for ED5

copy ED5 to FX2

Waiting to check

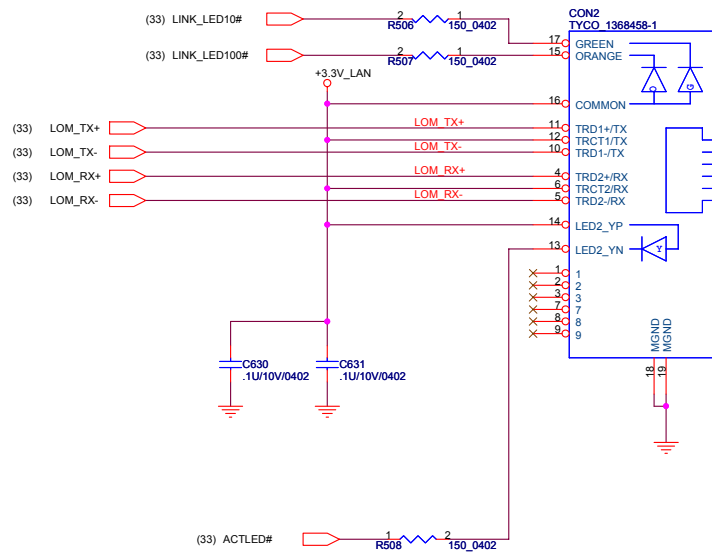


QUANTA COMPUTER

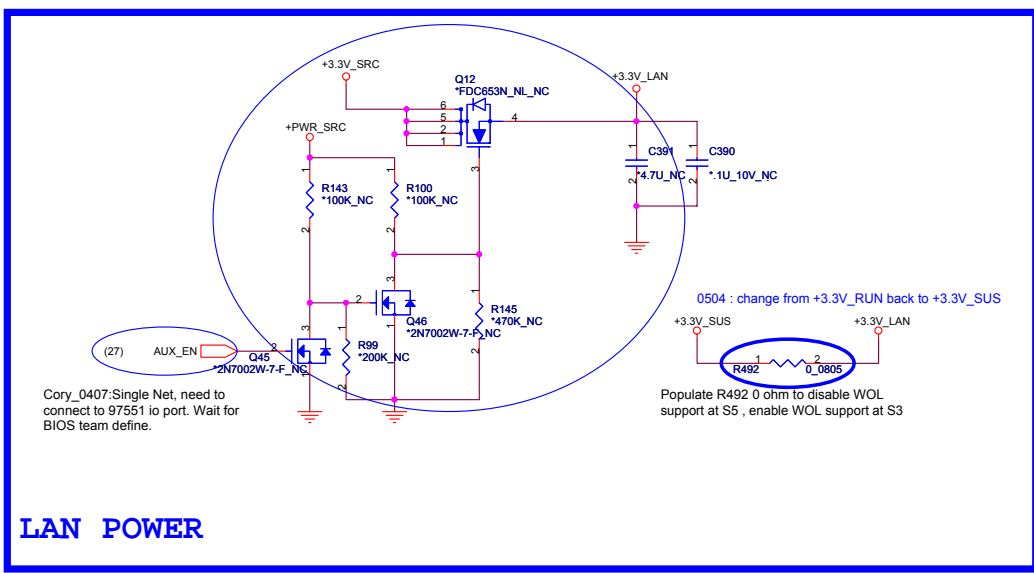
File: LAN(BCM4401)

Size	Document Number	Rev
FX2		1A

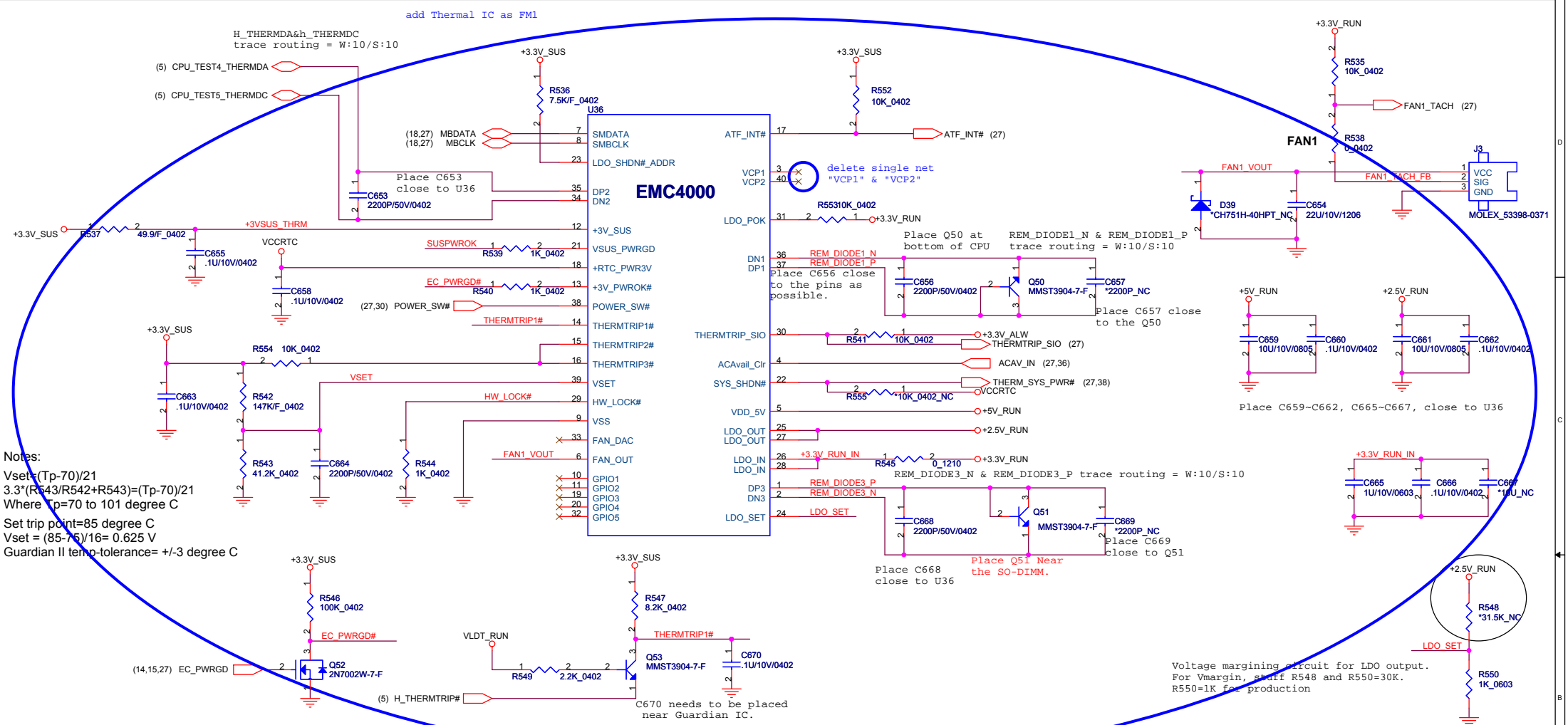
Date: Friday, May 05, 2006 Sheet 33 of 47



- change name for ED5
- copy ED5 to FX2
- Waiting to check
- copy DM5 to FX2

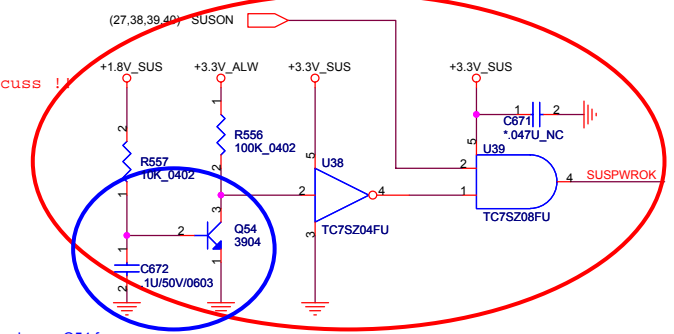
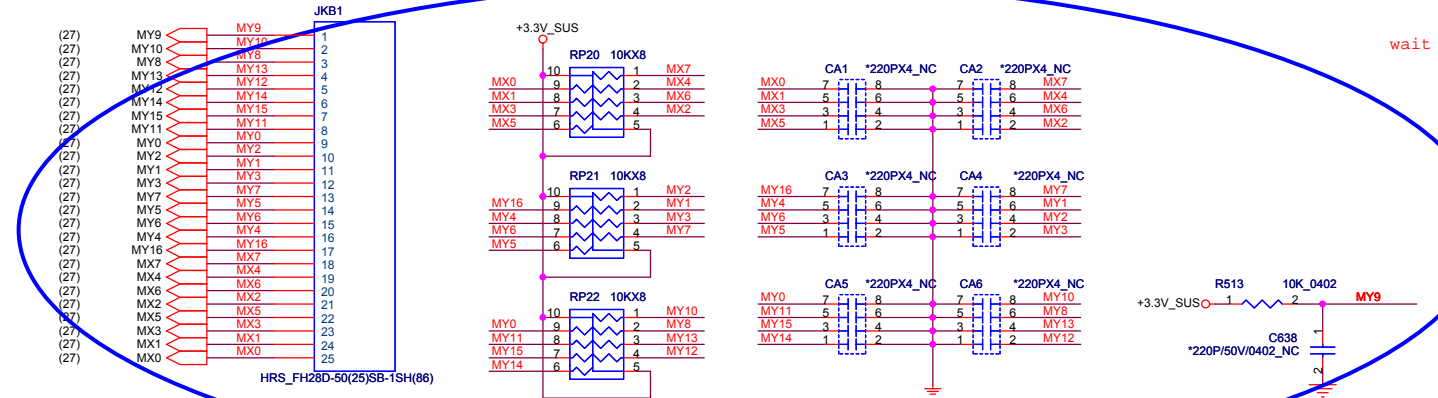


LAN POWER



Notes:
 $V_{set} = (T_p - 70) / 21$
 $3.3 * (R_{43} / R_{542} + R_{543}) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degree C
 Set trip point = 85 degree C
 $V_{set} = (85 - 70) / 16 = 0.625 V$
 Guardian II temp-tolerance = +/- 3 degree C

as FMI keyboard matrix & "e0788.1104a_swap-0422"



Voltage margining circuit for LDO output.
 For Vmargin, stuff R548 and R550=30K.
 R550=1K for production



QUANTA COMPUTER

Title: KB & THERMAL & FAN

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	FX2	1A

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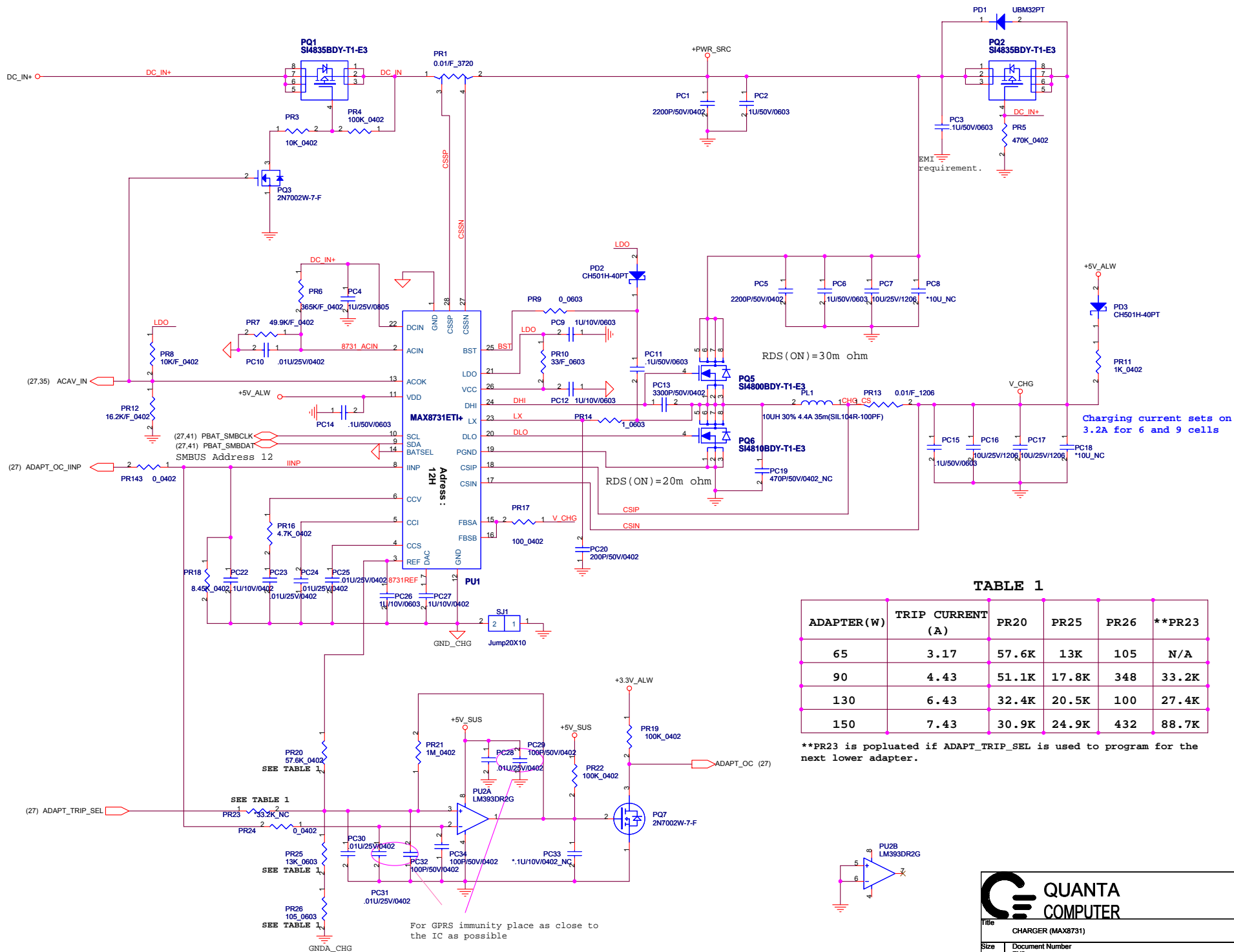


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR20	PR25	PR26	**PR23
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

**PR23 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

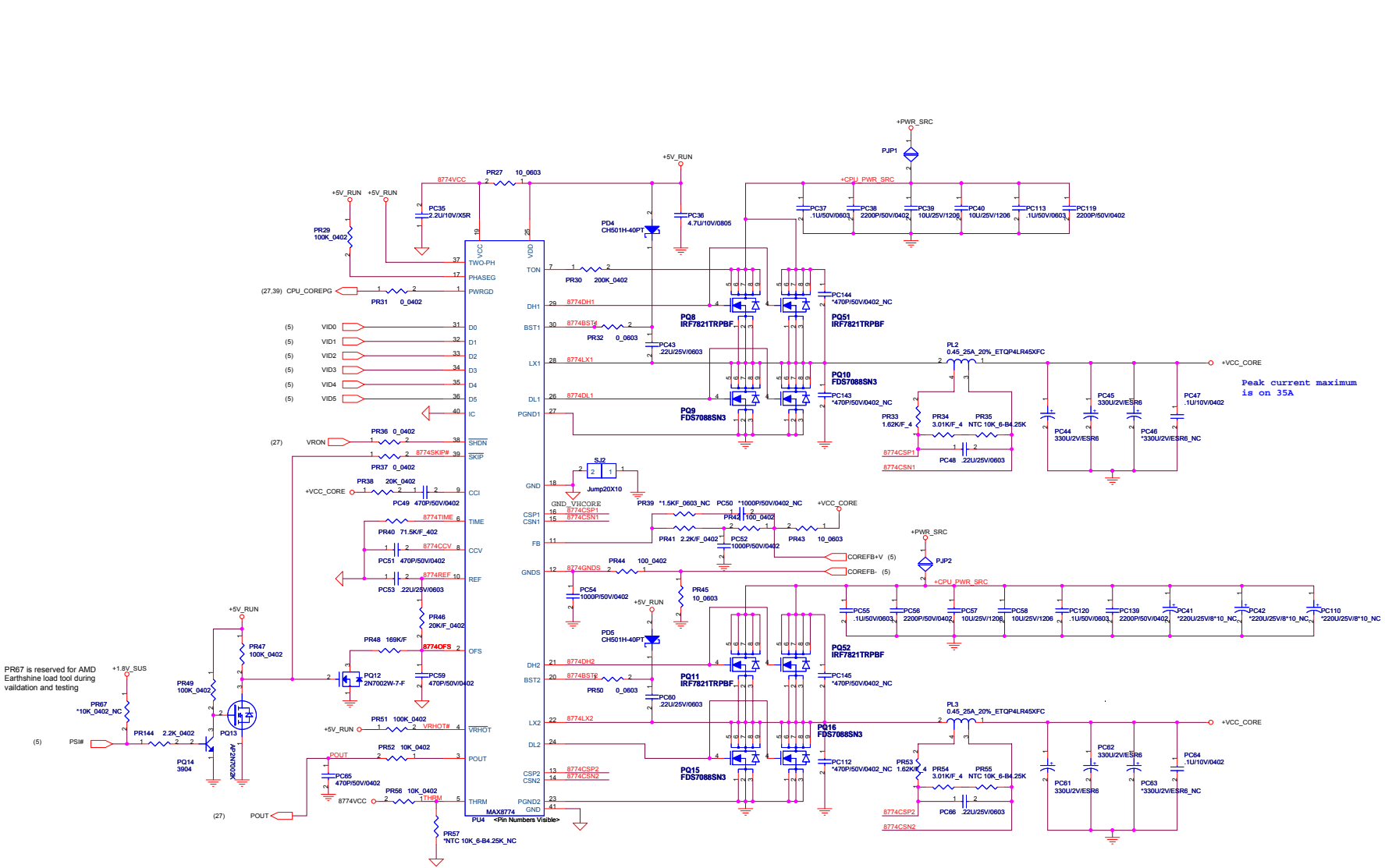
For GPRS immunity place as close to the IC as possible

QUANTA COMPUTER

Title: CHARGER (MAX8731)

Size: FX2	Document Number: 2005/4/21	Rev: 1A
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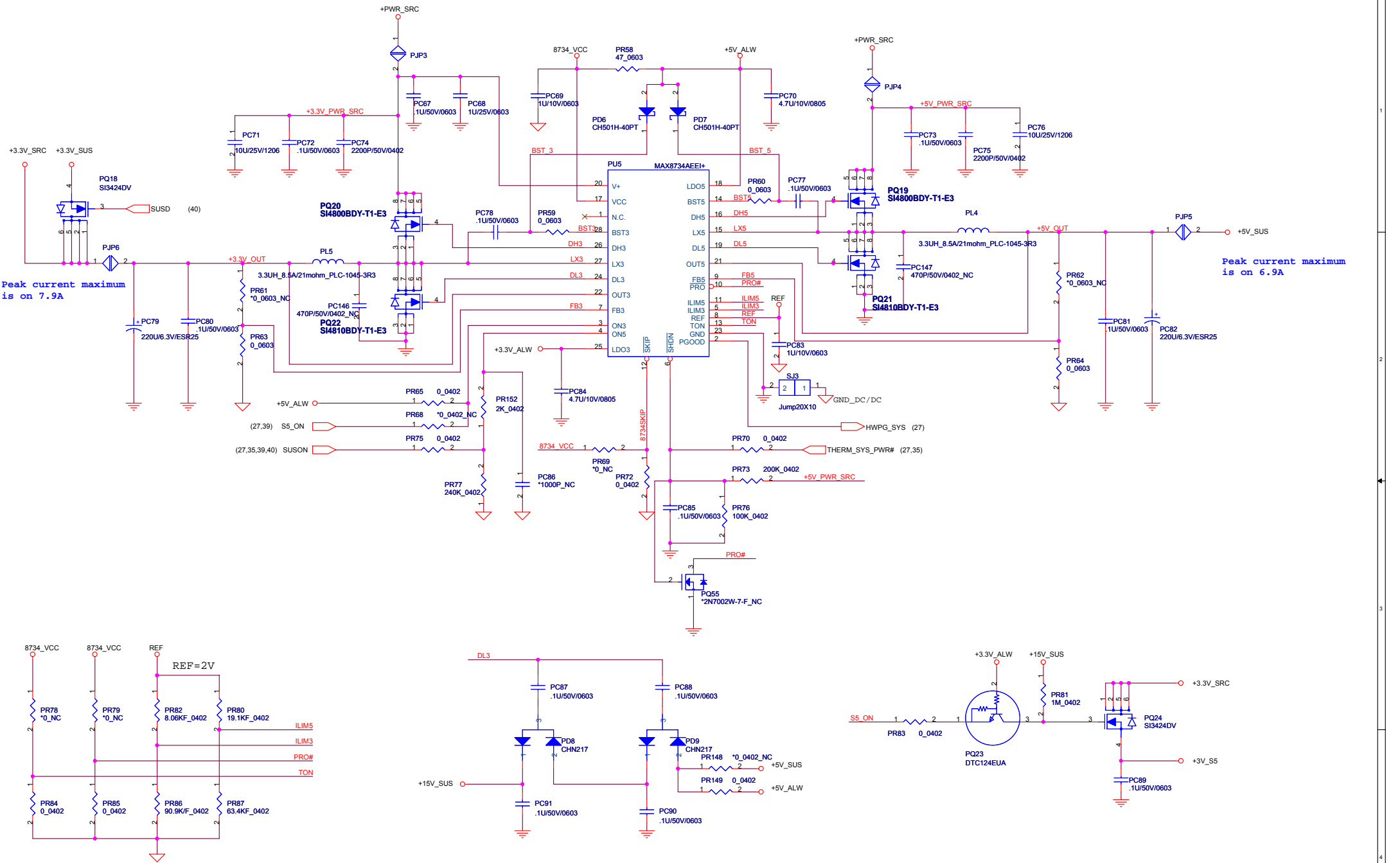
Peak current maximum is on 35A

PR67 is reserved for AMD Earthshine load tool during validation and testing

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.550V	1	0	0	0	0	0	0.750V
0	0	0	0	0	1	1.525V	1	0	0	0	0	1	0.735V
0	0	0	0	0	1	1.500V	1	0	0	0	0	1	0.720V
0	0	0	0	0	1	1.475V	1	0	0	0	1	1	0.705V
0	0	0	0	0	1	1.450V	1	0	0	0	1	0	0.690V
0	0	0	0	0	1	1.425V	1	0	0	0	1	1	0.675V
0	0	0	0	0	1	1.400V	1	0	0	0	1	0	0.660V
0	0	0	0	0	1	1.375V	1	0	0	0	1	1	0.645V
0	0	0	0	0	1	1.350V	1	0	0	0	0	0	0.630V
0	0	0	0	0	1	1.325V	1	0	0	0	1	0	0.615V
0	0	0	0	0	1	1.300V	1	0	0	0	1	1	0.600V
0	0	0	0	0	1	1.275V	1	0	0	0	1	0	0.585V
0	0	0	0	0	1	1.250V	1	0	0	0	1	1	0.570V
0	0	0	0	0	1	1.225V	1	0	0	0	1	0	0.555V
0	0	0	0	0	1	1.200V	1	0	0	0	1	1	0.540V
0	0	0	0	0	1	1.175V	1	0	0	0	1	0	0.525V
0	0	0	0	0	1	1.150V	1	0	0	0	1	1	0.510V
0	0	0	0	0	1	1.125V	1	0	0	0	1	0	0.495V
0	0	0	0	0	1	1.100V	1	0	0	0	1	1	0.480V
0	0	0	0	0	1	1.075V	1	0	0	0	1	0	0.465V
0	0	0	0	0	1	1.050V	1	0	0	0	1	1	0.450V
0	0	0	0	0	1	1.025V	1	0	0	0	1	0	0.435V
0	0	0	0	0	1	1.000V	1	0	0	0	1	1	0.420V
0	0	0	0	0	1	0.975V	1	0	0	0	1	0	0.405V
0	0	0	0	0	1	0.950V	1	0	0	0	1	1	0.390V
0	0	0	0	0	1	0.925V	1	0	0	0	1	0	0.375V
0	0	0	0	0	1	0.900V	1	0	0	0	1	1	0.360V
0	0	0	0	0	1	0.875V	1	0	0	0	1	0	0.345V
0	0	0	0	0	1	0.850V	1	0	0	0	1	1	0.330V
0	0	0	0	0	1	0.825V	1	0	0	0	1	0	0.315V
0	0	0	0	0	1	0.800V	1	0	0	0	1	1	0.300V
0	0	0	0	0	1	0.775V	1	0	0	0	1	0	0.285V

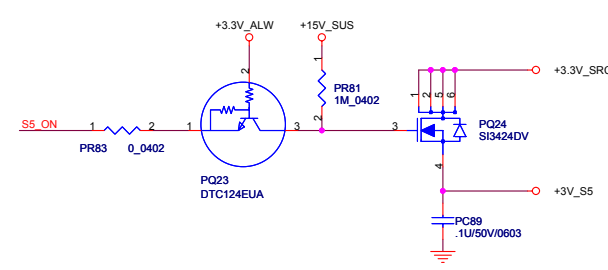
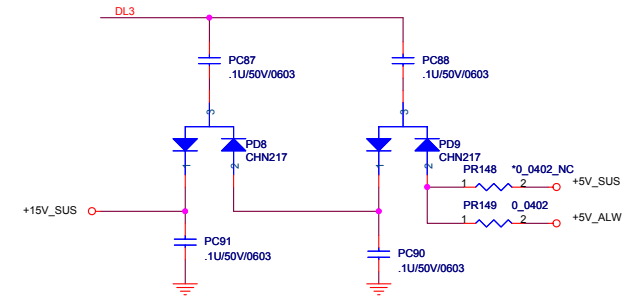
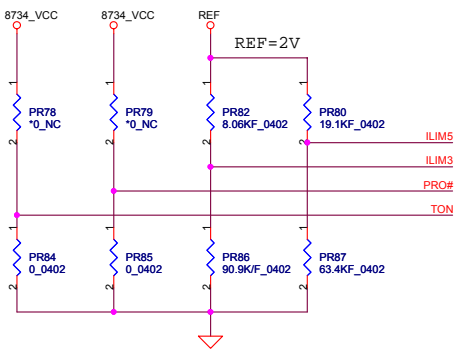
QUANTA COMPUTER

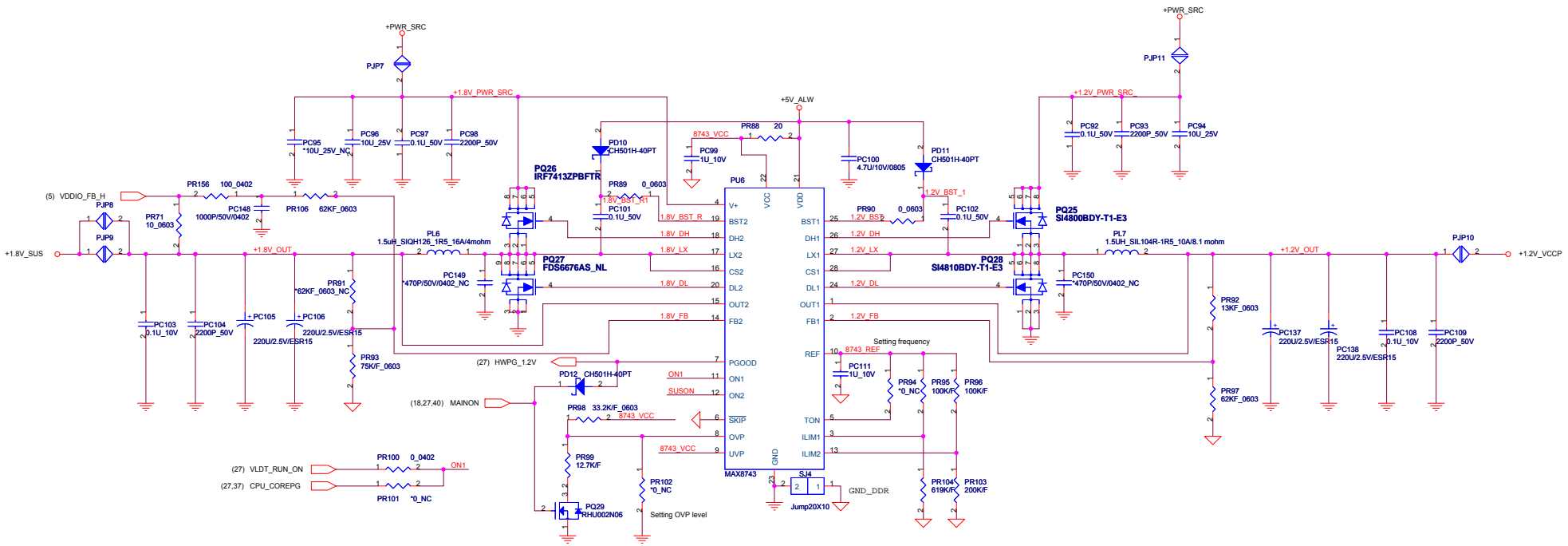
File: VHCORE (MAX8774)
 Size: Document Number
 PK2
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 Rev 1A



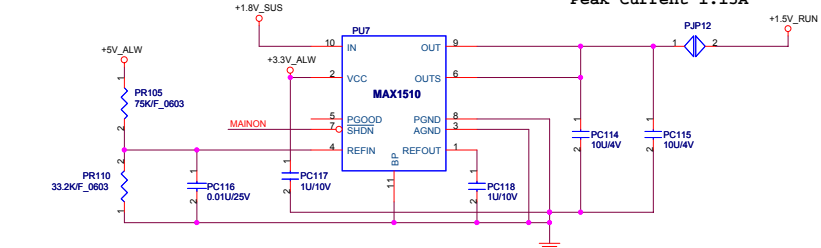
Peak current maximum is on 7.9A

Peak current maximum is on 6.9A

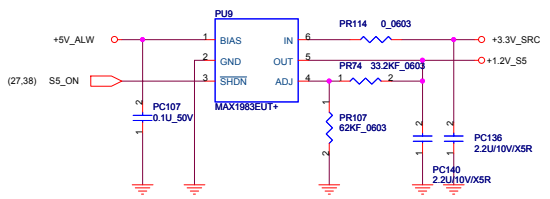
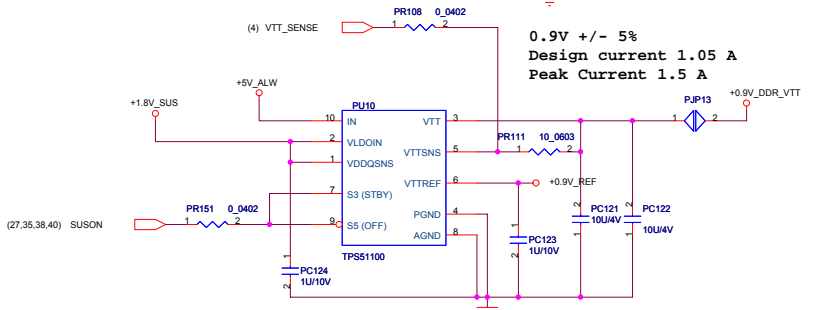


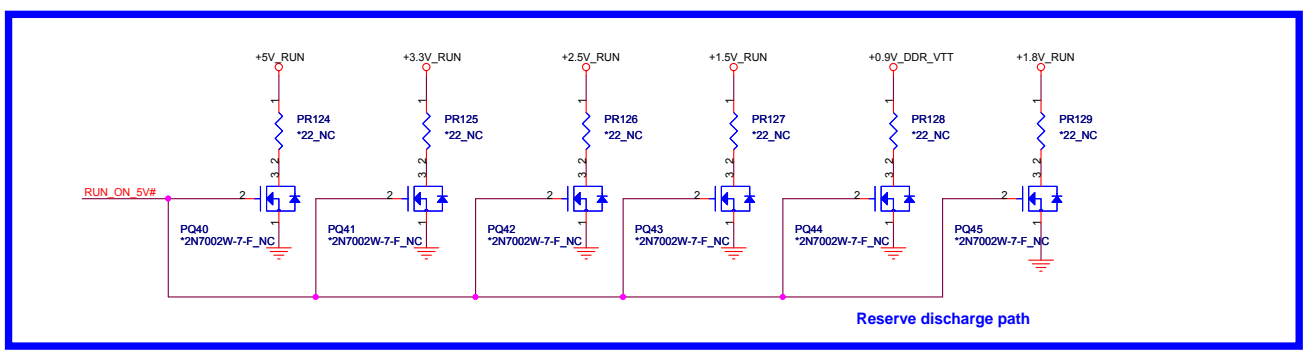
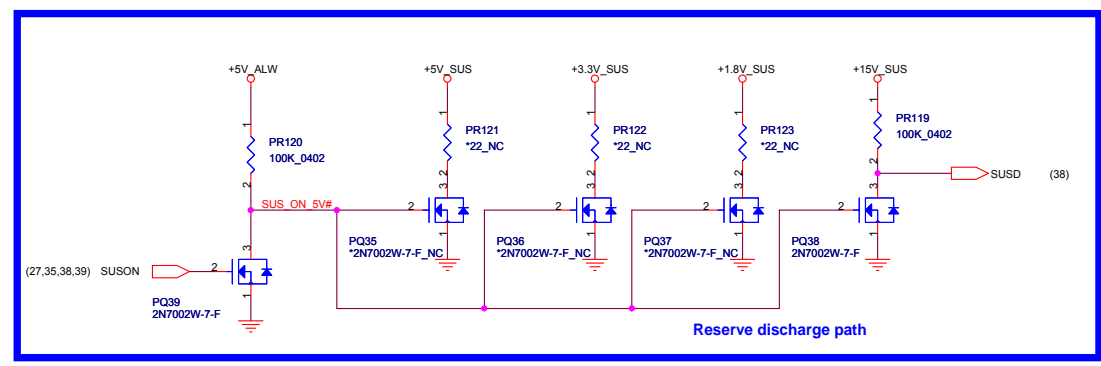
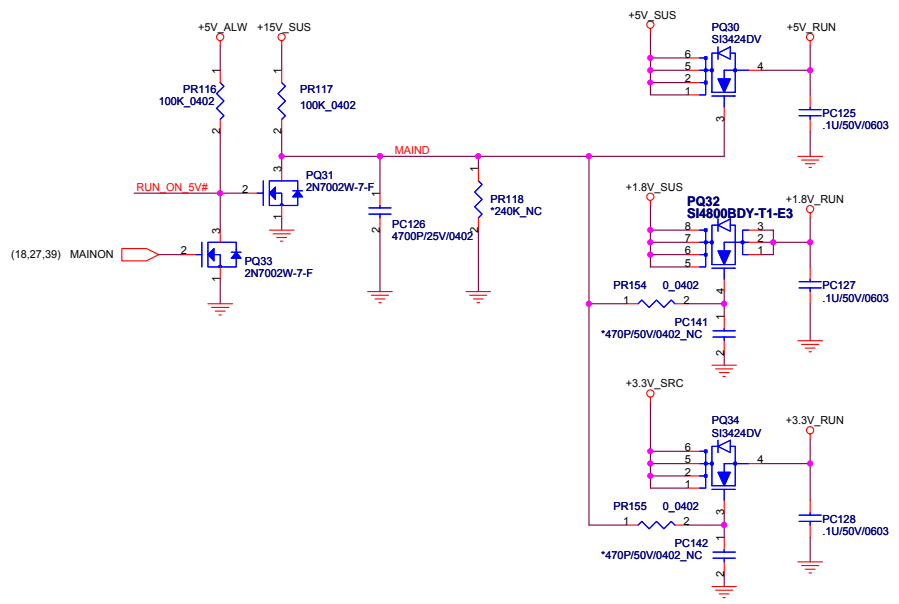



1.5 Volt +/- 5%
 Design current 0.7A
 Peak Current 1.15A



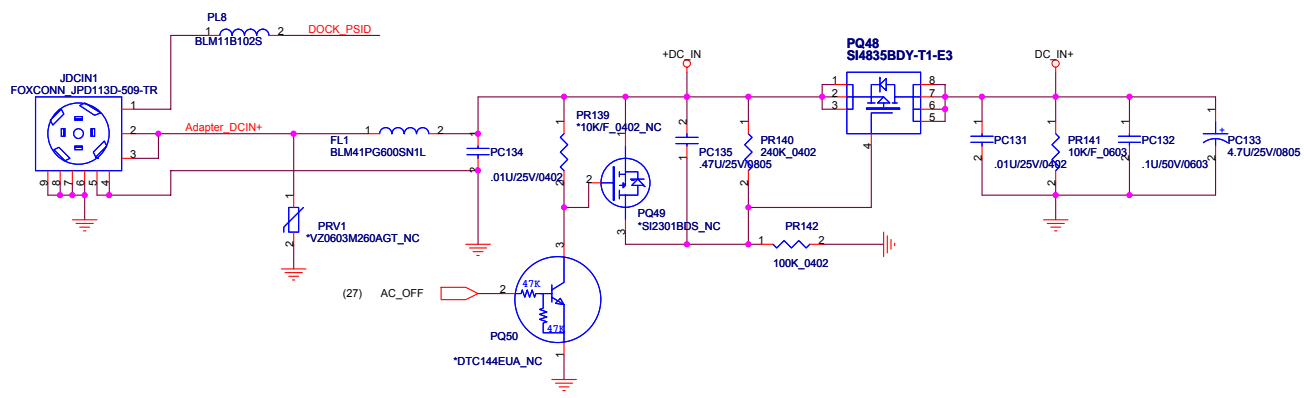
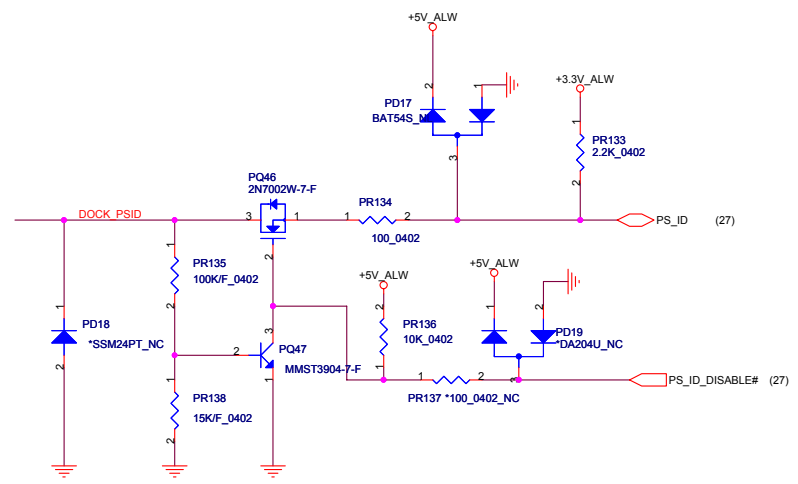
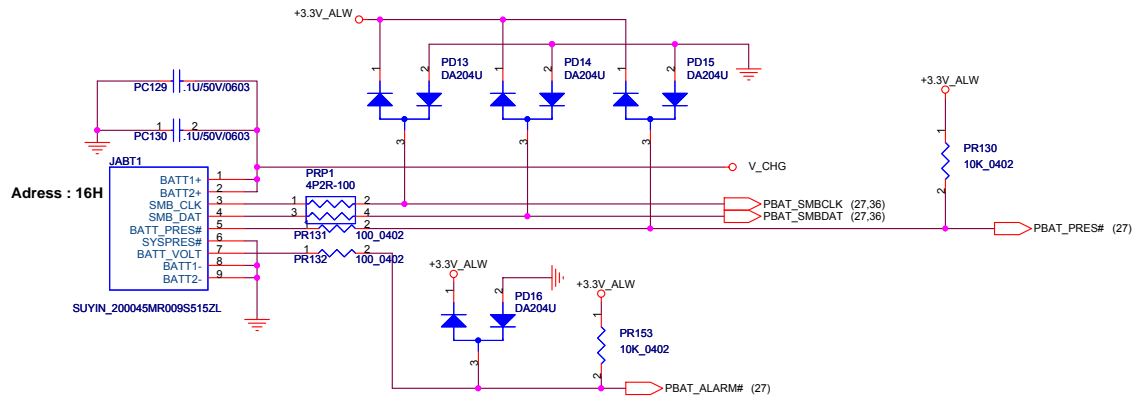
0.9V +/- 5%
 Design current 1.05 A
 Peak Current 1.5 A






QUANTA
COMPUTER

Title		RUN POWER SW
Size	Document Number	Rev
FX2		1A
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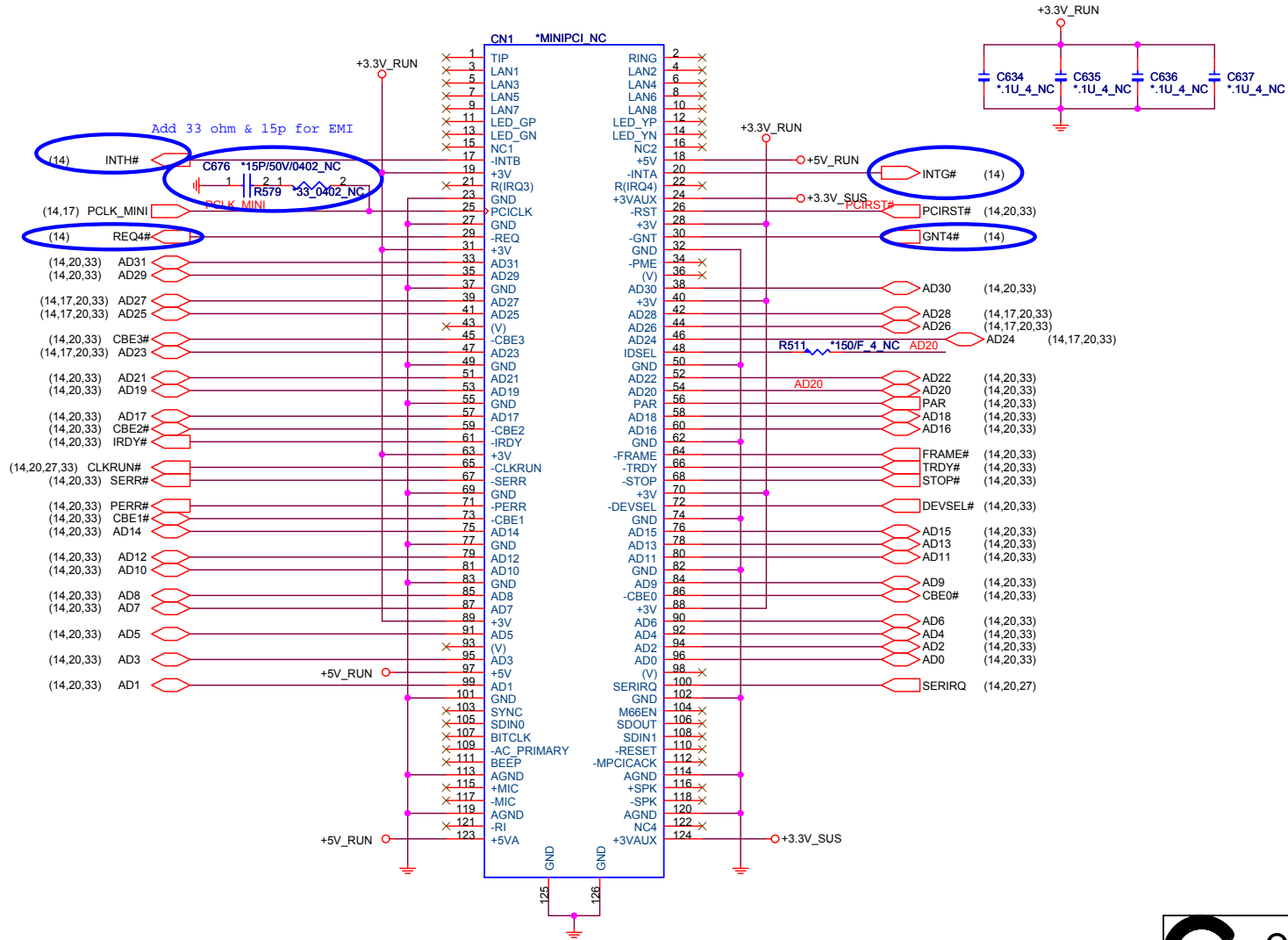


**QUANTA
COMPUTER**


Title		DCIN_Batt
Size	Document Number	Rev
FX2		1A
Date:	Friday, May 05, 2006	Sheet 41 of 47

ID Select : AD20
 Interrupt Pin : INTG# , INTH#
 Request Indicate : REQ4#
 Grant Indicate : GNT4#

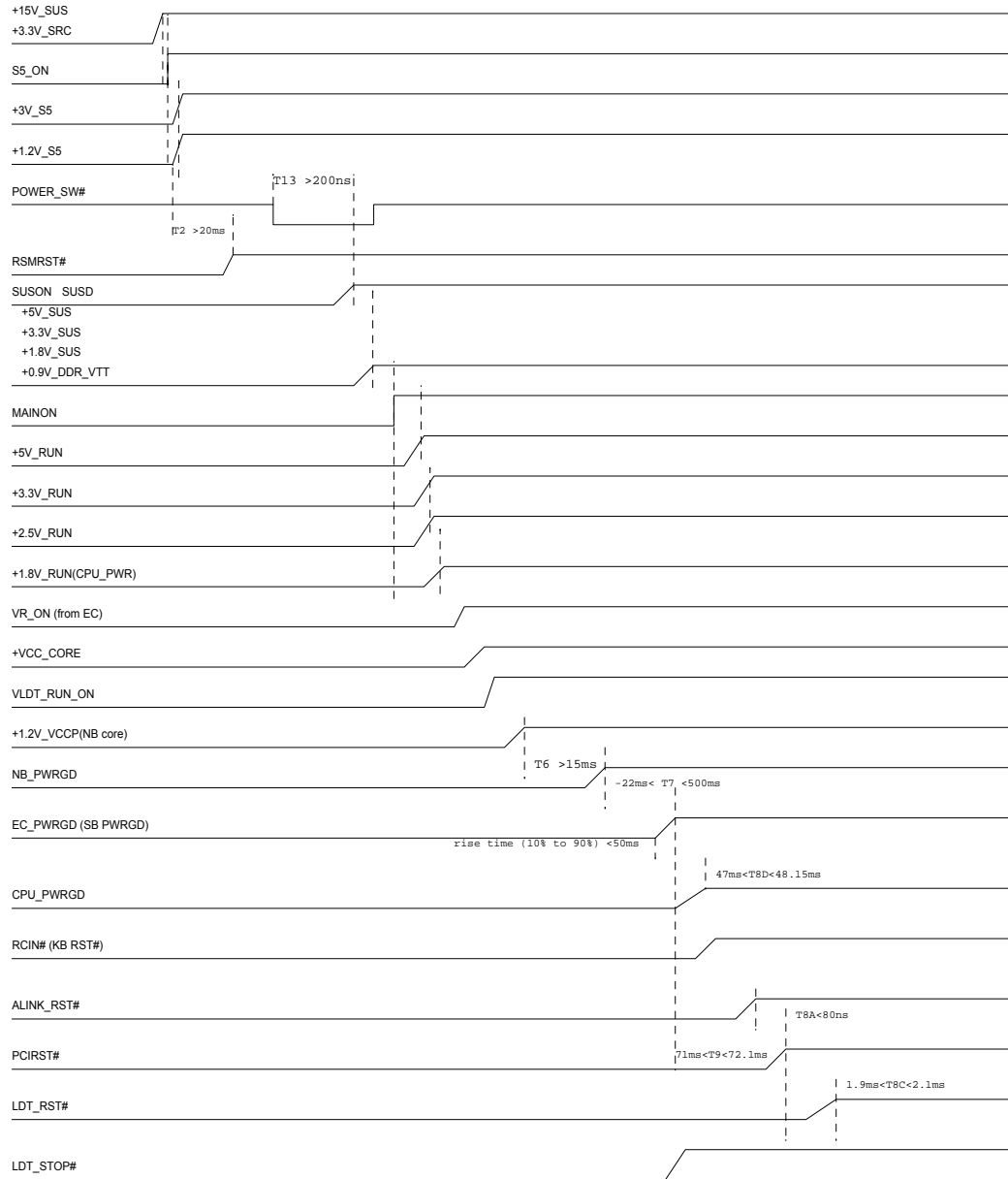
DEBUG PURPOSE ONLY



MPC


 QUANTA COMPUTER		Title	
		MINI PCI(for debug)	
Size	Document Number	Rev	
	FX2	1A	
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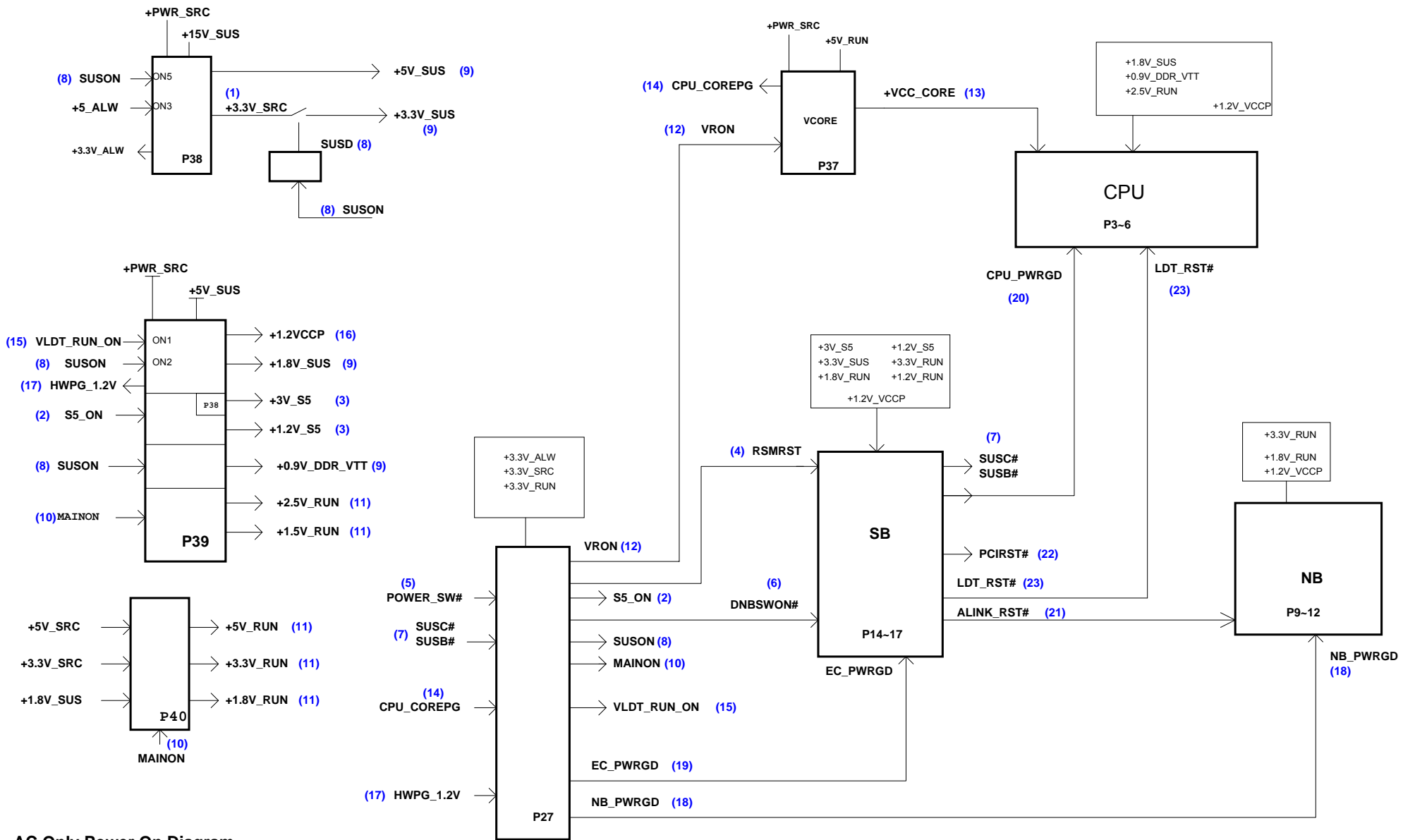
Power On Sequence



T6: NB core voltage to NB_PWRGD
 T7: NB_PWRGD to SB_PWRGD
 T8D: SB_PWRGD to CPU_PWRGD

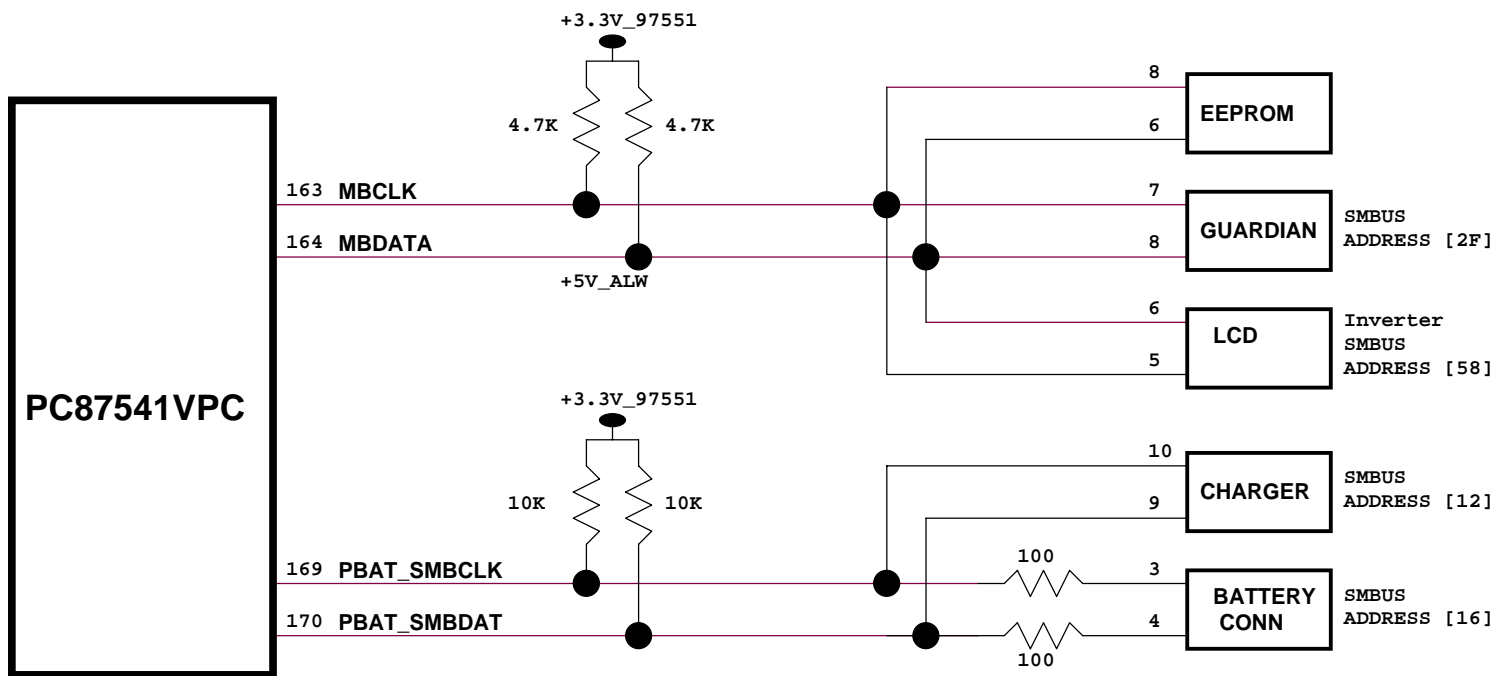
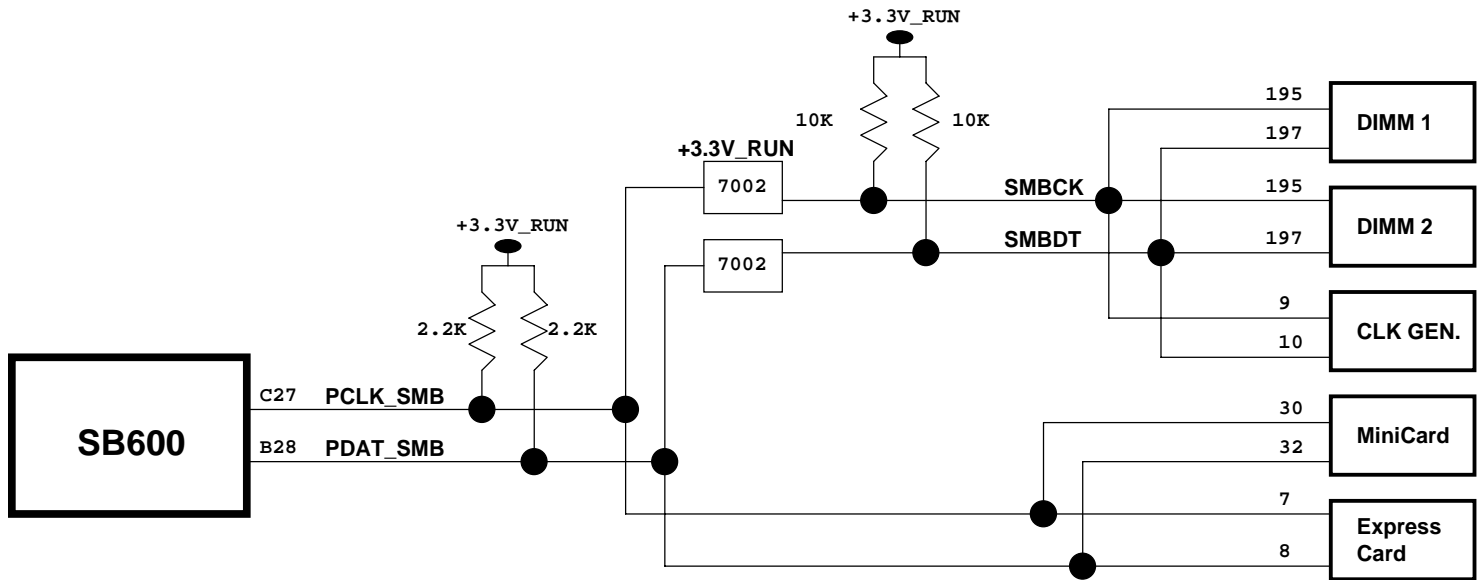
T8A: ALINK_RST# to PCIRST#
 T9: SB_PWRGD to PCIRST#
 T8C: PCIRST# to LDT_RST#

 QUANTA COMPUTER		Title	
		Power On Sequence	
Size	Document Number	Rev	
	FX2	1A	
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AC Only Power On Diagram

- | | | | |
|----------------------|-------------------------------------|------------------|-----------------|
| (1) +3.3V_SRC | (8) SUSON, SUSD | (13) +VCC_CORE | (20) CPU_PWRGD |
| (2) S5_ON | (9) +5V_SUS | (14) CPU_COREPG | (21) ALINK_RST# |
| (3) +3V_S5, +1.2V_S5 | +0.9V_DDR_VTT, +3.3V_SUS, +1.8V_SUS | (15) VLDT_RUN_ON | (22) PCI_RST# |
| (4) RSMRST | (10) MAINON | (16) +1.2_VCCP | (23) LDT_RST# |
| (5) POWER_SW# | (11) +5V_RUN, +3.3V_RUN | (17) HWPG_1.2V | |
| (6) DNBSWON# | +2.5V_RUN, +1.8V_RUN, +1.5V_RUN | (18) NB_PWRGD | |
| (7) SUSC#, SUSB# | (12) VRON | (19) EC_PWRGD | |



Temp Sensor
SMBUS
ADDRESS [2F]
ADDRESS [98]

Inverter
SMBUS
ADDRESS [58]

