## NCP3063, NCP3063B, NCV3063

### 1.5 A, Step-Up/Down/ Inverting Switching Regulators

The NCP3063 Series is a higher frequency upgrade to the popular MC34063A and MC33063A monolithic DC-DC converters. These devices consist of an internal temperature compensated reference, comparator, a controlled duty cycle oscillator with an active current limit circuit, a driver and a high current output switch. This series was specifically designed to be incorporated in Step-Down, Step-Up and Voltage-Inverting applications with a minimum number of external components.

## Features

- Operation to 40 V Input
- Low Standby Current
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation of 150 kHz
- Precision 1.5\% Reference
- New Features: Internal Thermal Shutdown with Hysteresis Cycle-by-Cycle Current Limiting
- Pb-Free Packages are Available


## Applications

- Step-Down, Step-Up and Inverting supply applications
- High Power LED Lighting
- Battery Chargers


Figure 1. Typical Buck Application Circuit


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> MARKING DIAGRAMS


DFN-8 CASE 488AF


NCP3063x
$=$ Specific Device Code X = B
A $\quad=$ Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

- = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

## NCP3063, NCP3063B, NCV3063



Figure 2. Pin Connections


NOTE: EP Flag must be tied to GND Pin 4 on PCB
Figure 3. Pin Connections


Figure 4. Block Diagram

PIN DESCRIPTION

| Pin No. | Pin Name | Description |
| :---: | :---: | :--- |
| 1 | Switch Collector | Internal Darlington switch collector |
| 2 | Switch Emitter | Internal Darlington switch emitter |
| 3 | Timing Capacitor <br> Oscillator Input | Timing Capacitor |
| 4 | GND | Ground pin for all internal circuits |
| 5 | Comparator <br> Inverting Input | Inverting input pin of internal comparator |
| 6 | $\mathrm{~V}_{\mathrm{CC}}$ | Voltage Supply |
| 7 | Ipk Sense | Peak Current Sense Input to monitor the voltage drop across an external resistor to limit the peak <br> current through the circuit |
| 8 | N.C. | Pin Not Connected |
| Exposed <br> Pad | Exposed Pad | The exposed pad beneath the package must be connected to GND (Pin 4). Additionally, using <br> proper layout techniques, the exposed pad can greatly enhance the power dissipation capabilities <br> of the NCP3063. |

MAXIMUM RATINGS (measured vs. Pin 4, unless otherwise noted)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ pin 6 | $\mathrm{V}_{\mathrm{CC}}$ | 0 to +40 | V |
| Comparator Inverting Input pin 5 | $\mathrm{V}_{\mathrm{CII}}$ | -0.2 to $+\mathrm{V}_{\mathrm{CC}}$ | V |
| Darlington Switch Collector pin 1 | $\mathrm{V}_{\mathrm{SWC}}$ | 0 to +40 | V |
| Darlington Switch Emitter pin 2 (transistor OFF) | $\mathrm{V}_{\mathrm{SWE}}$ | -0.6 to $+\mathrm{V}_{\mathrm{CC}}$ | V |
| Darlington Switch Collector to Emitter pin 1-2 | $\mathrm{V}_{\mathrm{SWCE}}$ | 0 to +40 | V |
| Darlington Switch Current | $\mathrm{I}_{\mathrm{SW}}$ | 1.5 | A |
| $\mathrm{I}_{\mathrm{pk}}$ Sense Pin 7 | $\mathrm{V}_{\mathrm{IPK}}$ | -0.2 to $\mathrm{V}_{\mathrm{CC}}+0.2$ | V |
| Timing Capacitor Pin 3 | $\mathrm{V}_{\mathrm{TCAP}}$ | -0.2 to +1.4 | V |

POWER DISSIPATION AND THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| PDIP-8 Thermal Resistance, Junction-to-Air | $\mathrm{R}_{\theta \mathrm{JA}}$ | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\begin{array}{cc} \text { SOIC-8 } & \begin{array}{c} \text { Thermal Resistance, Junction-to-Air } \\ \text { Thermal Resistance, Junction-to-Case } \end{array} \end{array}$ | $R_{\theta J A}$ <br> $R_{\text {日JC }}$ | $\begin{gathered} 180 \\ 45 \end{gathered}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| DFN-8 Thermal Resistance, Junction-to-Air | $\mathrm{R}_{\theta \mathrm{JA}}$ | 80 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {STG }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $T_{J \text { MAX }}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
|  | $\mathrm{T}_{J}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+125 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:

Pin 1-8: Human Body Model 2000 V per AEC Q100-002; 003 or JESD22/A114; A115
Machine Model Method 200 V
2. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. The relation between junction temperature, ambient temperature and Total Power dissipated in IC is $T_{J}=T_{A}+R_{\theta} \cdot P_{D}$
4. The pins which are not defined may not be loaded by external signals

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~T}_{J}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 5], unless otherwise specified)

| Symbol | Characteristic | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |  |
| fosc | Frequency | $\begin{gathered} \left(\mathrm{V}_{\text {Pin }} 5=0 \mathrm{~V}, \mathrm{CT}=2.2 \mathrm{nF},\right. \\ \left.\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{gathered}$ | 110 | 150 | 190 | kHz |
| $\mathrm{I}_{\mathrm{DISCHG}} /$ $\mathrm{I}_{\mathrm{CHG}}$ | Discharge to Charge Current Ratio | (Pin 7 to $\mathrm{V}_{\mathrm{CC}}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | 5.5 | 6.0 | 6.5 | - |
| IDISCHG | Capacitor Discharging Current | (Pin 7 to $\mathrm{V}_{\mathrm{CC}}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) |  | 1650 |  | $\mu \mathrm{A}$ |
| $I_{\text {CHG }}$ | Capacitor Charging Current | (Pin 7 to $\mathrm{V}_{\mathrm{Cc}}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) |  | 275 |  | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {IPK (Sense) }}$ | Current Limit Sense Voltage | $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)($ Note 6) | 165 | 200 | 235 | mV |

OUTPUT SWITCH (Note 7)

| $\mathrm{V}_{\text {SWCE(DROP) }}$ | Darlington Switch Collector to <br> Emitter Voltage Drop | $\left(\mathrm{I}_{\mathrm{SW}}=1.0 \mathrm{~A}\right.$, Pin 2 to GND, <br> $\left.\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)($ Note 7$)$ | 1.0 | 1.3 | V |  |
| :---: | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{C}(\mathrm{OFF})}$ | Collector Off-State Current | $\left(\mathrm{V}_{\mathrm{CE}}=40 \mathrm{~V}\right)$ |  | 0.01 | 100 | $\mu \mathrm{~A}$ |

COMPARATOR

| $\mathrm{V}_{\text {TH }}$ | Threshold Voltage | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 1.250 |  | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | NCP3063 | -1.5 |  | +1.5 | \% |
|  |  | NCP3063B, NCV3063 | -2 |  | +2 | \% |
| REGLiNE | Threshold Voltage Line Regulation | $\left(\mathrm{V}_{\text {CC }}=5.0 \mathrm{~V}\right.$ to 40 V ) | -6.0 | 2.0 | 6.0 | mV |
| $\mathrm{I}_{\mathrm{ClI}}$ in | Input Bias Current | $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {th }}\right)$ | -1000 | -100 | 1000 | nA |

TOTAL DEVICE

| $\mathrm{I}_{\mathrm{CC}}$ | Supply Current | $\begin{gathered} \left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \text { to } 40 \mathrm{~V},\right. \\ \mathrm{CT}=2.2 \mathrm{nF}, \mathrm{Pin} 7=\mathrm{V}, \\ \mathrm{~V}_{\text {Pin }} 5>\mathrm{V}_{\text {th }}, \text { Pin } 2=\mathrm{GND}, \\ \text { remaining pins open }) \end{gathered}$ |  | 7.0 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Thermal Shutdown Threshold |  | 160 |  | ${ }^{\circ} \mathrm{C}$ |
|  | Hysteresis |  | 10 |  | ${ }^{\circ} \mathrm{C}$ |

5. NCP3063: $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$;

NCP3063B, NCV3063: $T_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
6. The $\mathrm{V}_{\mathrm{IPK}(\text { Sense })}$ Current Limit Sense Voltage is specified at static conditions. In dynamic operation the sensed current turn-off value depends on comparator response time and di/dt current slope. See the Operating Description section for details.
7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
8. NCV prefix is for automotive and other applications requiring site and change control.


Figure 5. Oscillator Frequency vs. Oscillator Timing Capacitor


Figure 7. Emitter Follower Configuration Output Darlington Switch Voltage Drop vs. Temperature


Figure 6. Oscillator Frequency vs. Supply Voltage


Figure 8. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Temperature

$\mathrm{I}_{\mathrm{C}}$, COLLECTOR CURRENT (A)
Figure 10. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Collector Current


Figure 11. Comparator Threshold Voltage vs. Temperature


Figure 12. Current Limit Sense Voltage vs. Temperature


Figure 13. Standby Supply Current vs. Supply Voltage

## NCP3063, NCP3063B, NCV3063

## INTRODUCTION

The NCP3063 is a monolithic power switching regulator optimized for dc to dc converter applications. The combination of its features enables the system designer to directly implement step-up, step-down, and voltageinverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for industrial markets. A representative block diagram is shown in Figure 4.

## Operating Description

The NCP3063 is a hysteretic, dc-dc converter that uses a gated oscillator to regulate output voltage. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 14. The output voltage waveform shown is for a step-down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle
controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the output switch next cycle turning on is inhibited. The feedback comparator will enable the switching immediately when the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be enabled for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles. (See AN920/D for more information).

## Oscillator

The oscillator frequency and off-time of the output switch are programmed by the value selected for timing capacitor $\mathrm{C}_{\mathrm{T}}$. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged and discharged by a 1 to 6 ratio internal current source and sink, generating a positive going sawtooth waveform at Pin 3. This ratio sets the maximum $\mathrm{t}_{\mathrm{ON}} /\left(\mathrm{t}_{\mathrm{ON}}+\mathrm{t}_{\mathrm{OFF}}\right)$ of the switching converter as $6 /(6+1)$ or 0.857 (typical) The oscillator peak and valley voltage difference is 500 mV typically. To calculate the $\mathrm{C}_{\mathrm{T}}$ capacitor value for required oscillator frequency, use the equations found in Figure 15. An Excel based design tool can be found at www.onsemi.com on the NCP3063 product page.


Figure 14. Typical Operating Waveforms

## Peak Current Sense Comparator

With a voltage ripple gated converter operating under normal conditions, output switch conduction is initiated by the Voltage Feedback comparator and terminated by the oscillator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the $\mathrm{I}_{\mathrm{pk}}$ Current Sense comparator will protect the Darlington output Switch. The switch current is converted to a voltage by inserting a fractional ohm resistor, $\mathrm{R}_{\mathrm{SC}}$, in series with $\mathrm{V}_{\mathrm{CC}}$ and the Darlington output switch. The voltage drop across $\mathrm{R}_{\mathrm{SC}}$ is monitored by the Current Sense comparator. If the voltage drop exceeds 200 mV with respect to $\mathrm{V}_{\mathrm{CC}}$, the comparator will set the latch and terminate output switch conduction on a cycle-by-cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on-time during a given oscillator cycle.


The $\mathrm{V}_{\text {IPK(Sense) }}$ Current Limit Sense Voltage threshold is specified at static conditions. In dynamic operation the sensed current turn-off value depends on comparator response time and di/dt current slope.

Real $\mathrm{V}_{\text {turn-off }}$ on $\mathrm{R}_{\text {sc }}$ resistor

$$
V_{\text {turn_off }}=V_{\text {ipk }}(\text { sense })+R s \cdot\left(t \_d e l a y \cdot d i / d t\right)
$$

Typical $\mathrm{I}_{\mathrm{pk}}$ comparator response time t _delay is 350 ns . The di/dt current slope is growing with voltage difference on the inductor pins and with decreasing inductor value.
It is recommended to check the real max peak current in the application at worst conditions to be sure that the max peak current will never get over the 1.5 A Darlington Switch Current max rating.

## Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at $160^{\circ} \mathrm{C}$, the Output Switch is disabled. The temperature sensing circuit is designed with $10^{\circ} \mathrm{C}$ hysteresis. The Switch is enabled again when the chip temperature decreases to at least $150^{\circ} \mathrm{C}$ threshold. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

## Output Switch

The output switch is designed in a Darlington configuration. This allows the application designer to operate at all conditions at high switching speed and low voltage drop. The Darlington Output Switch is designed to switch a maximum of 40 V collector to emitter voltage and current up to 1.5 A .

## APPLICATIONS

Figures 16 through 24 show the simplicity and flexibility of the NCP3063. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 15 gives the relevant design equations for the key parameters. Additionally, a complete application design aid for the NCP3063 can be found at www.onsemi.com.

Figures 25 through 31 show typical NCP3063 applications with external transistors. This solution helps to
increase output current and helps with efficiency still keeping low cost bill of materials. Typical schematics of boost configuration with NMOS transistor, buck configuration with PMOS transistor and buck configuration with LOW $\mathrm{V}_{\mathrm{CE}(\text { sat })}$ PNP are shown.
Another advantage of using the external transistor is higher operating frequency which can go up to 250 kHz . Smaller size of the output components such as inductor and capacitor can be used then.

| (See Notes 9, 10, 11) | Step-Down | Step-Up | Voltage-Inverting |
| :---: | :---: | :---: | :---: |
| $\frac{t_{\mathrm{ton}}}{\mathrm{t}_{\mathrm{off}}}$ | $\frac{V_{\text {out }}+V_{F}}{V_{\text {in }}-V_{\text {SWCE }}-V_{\text {out }}}$ | $\frac{V_{\text {out }}+V_{F}-V_{\text {in }}}{V_{\text {in }}-V_{S W C E}}$ | $\frac{\left\|V_{\text {out }}\right\|+V_{F}}{V_{\text {in }}-V_{\text {SWCE }}}$ |
| $\mathrm{t}_{\text {on }}$ | $\frac{\frac{t_{\text {on }}}{t_{\text {off }}}}{f\left(\frac{t_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right)}$ |  | $\frac{\frac{\mathrm{ton}_{\text {on }}}{\mathrm{t}_{\text {off }}}}{f\left(\frac{\text { ton }}{\mathrm{t}_{\text {off }}}+1\right)}$ |
| $\mathrm{C}_{\text {T }}$ | $C_{\top}=\frac{381.6 \cdot 10^{-6}}{f_{\mathrm{OSC}}}-343 \cdot 10^{-12}$ |  |  |
| $\mathrm{I}_{\mathrm{L}(\mathrm{avg})}$ | lout | $l_{\text {out }}\left(\frac{t_{\text {on }}}{t_{\text {off }}}+1\right)$ | $\mathrm{I}_{\text {out }}\left(\frac{t_{\text {on }}}{t_{\text {off }}}+1\right)$ |
| $\mathrm{I}_{\mathrm{pk}}$ (Switch) | $\mathrm{l}(\mathrm{avg})+\frac{\Delta \mathrm{l}_{\mathrm{L}}}{2}$ | l (avg) $+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2}$ | $\mathrm{LL}(\mathrm{avg})+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2}$ |
| $\mathrm{R}_{\text {SC }}$ | $\frac{0.20}{\operatorname{lpk}(S w i t c h)}$ | $\frac{0.20}{\operatorname{lpk}(S w i t c h)}$ | $\frac{0.20}{\text { Ipk (Switch) }}$ |
| L | $\left(\frac{V_{\text {in }}-V_{\text {SWCE }}-V_{\text {out }}}{\Delta l_{\mathrm{L}}}\right) \mathrm{t}_{\text {on }}$ | $\left(\frac{V_{\text {in }}-V_{\text {SWCE }}}{\Delta I_{\mathrm{L}}}\right) \mathrm{t}_{\text {on }}$ | $\left(\frac{V_{\text {in }}-V_{\text {SWCE }}}{\Delta l_{\text {L }}}\right) \mathrm{t}_{\text {on }}$ |
| $\mathrm{V}_{\text {ripple }}(\mathrm{pp})$ | $\Delta \mathrm{IL} \sqrt{\left(\frac{1}{8 f \mathrm{CO}_{\mathrm{O}}}\right)^{2}+(\mathrm{ESR})^{2}}$ | $\approx \frac{t_{\text {on }} \mathrm{l}_{\mathrm{out}}}{\mathrm{CO}_{\mathrm{O}}}+\Delta \mathrm{I}_{\mathrm{L}} \cdot \mathrm{ESR}$ | $\approx \frac{t_{\text {on }} \mathrm{l}_{\mathrm{out}}}{\mathrm{CO}}+\Delta \mathrm{I}_{\mathrm{L}} \cdot \mathrm{ESR}$ |
| $V_{\text {out }}$ | $\mathrm{V}_{\mathrm{TH}}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)$ | $\mathrm{V}_{\mathrm{TH}}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)$ | $\mathrm{V}_{\mathrm{TH}}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)$ |

9. $\mathrm{V}_{\text {SWCE }}$ - Darlington Switch Collector to Emitter Voltage Drop, refer to Figures 7, 8, 9 and 10.
10. $\mathrm{V}_{\mathrm{F}}$ - Output rectifier forward voltage drop. Typical value for 1 N 5819 Schottky barrier rectifier is 0.4 V .
11. The calculated $t_{\mathrm{on}} / \mathrm{t}_{\text {off }}$ must not exceed the minimum guaranteed oscillator charge to discharge ratio.

The Following Converter Characteristics Must Be Chosen:
$\mathrm{V}_{\text {in }}$ - Nominal operating input voltage.
$\mathrm{V}_{\text {out }}$ - Desired output voltage.
$\mathrm{I}_{\text {out }}$ - Desired output current.
$\Delta \mathrm{I}_{\mathrm{L}}$ - Desired peak-to-peak inductor ripple current. For maximum output current it is suggested that $\Delta \mathrm{I}_{\mathrm{L}}$ be chosen to be less than $10 \%$ of the average inductor current $\mathrm{I}_{\mathrm{L}(\text { avg })}$. This will help prevent $\mathrm{I}_{\mathrm{pk}}$ (Switch) from reaching the current limit threshold set by $\mathrm{R}_{\mathrm{SC}}$. If the design goal is to use a minimum inductance value, let $\Delta \mathrm{I}_{\mathrm{L}}=2\left(\mathrm{I}_{\mathrm{L}(\mathrm{avg})}\right)$. This will proportionally reduce converter output current capability.
$f$ - Maximum output switch frequency.
$\mathrm{V}_{\text {ripple }}(\mathrm{pp})$ - Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor $C_{O}$ should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

Figure 15. Design Equations


Figure 16. Typical Buck Application Schematic
Value of Components

| Name | Value |
| :--- | :--- |
| L201 | $47 \mu \mathrm{H}, \mathrm{I}_{\text {sat }}>1.5 \mathrm{~A}$ |
| D201 | $1 \mathrm{~A}, 40 \mathrm{~V}$ Schottky Rectifier |
| C202 | $220 \mu \mathrm{~F}, 50 \mathrm{~V}$, Low ESR |
| C205 | $470 \mu \mathrm{~F}, 25 \mathrm{~V}$, Low ESR |
| C203 | 2.2 nF Ceramic Capacitor |


| Name | Value |
| :--- | :--- |
| R201 | $150 \mathrm{~m} \Omega, 0.5 \mathrm{~W}$ |
| R202 | $2.40 \mathrm{k} \Omega$ |
| R203 | $3.90 \mathrm{k} \Omega$ |
| C201 | 100 nF Ceramic Capacitor |
| C202 | 100 nF Ceramic Capacitor |

## Test Results

| Test | Condition | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=9 \mathrm{~V}$ to $12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=800 \mathrm{~mA}$ | 8 mV |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=80 \mathrm{~mA}$ to 800 mA | 9 mV |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{o}}=40 \mathrm{~mA}$ to 800 mA | $\leq 85 \mathrm{mV} \mathrm{V}_{\mathrm{pp}}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=400 \mathrm{~mA}$ to 800 mA | $>73 \%$ |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{R}_{\text {load }}=0.15 \Omega$ | 1.25 A |



Figure 17. Buck Demoboard Layout


Figure 18. Efficiency vs. Output Current for the Buck Demo Board at $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{~V}_{\text {out }}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$


Figure 19. Typical Boost Application Schematic

Value of Components

| Name | Value |
| :--- | :--- |
| L101 | $100 \mu \mathrm{H}, \mathrm{I}_{\text {sat }}>1.5 \mathrm{~A}$ |
| D101 | $1 \mathrm{~A}, 40 \mathrm{~V}$ Schottky Rectifier |
| C102 | $470 \mu \mathrm{~F}, 25 \mathrm{~V}$, Low ESR |
| C105 | $330 \mu \mathrm{~F}, 50 \mathrm{~V}$, Low ESR |
| C103 | 2.2 nF Ceramic Capacitor |$\quad$| Name | Value |
| :--- | :--- |
| R101 | $150 \mathrm{~m} \Omega, 0.5 \mathrm{~W}$ |
| R102 | $1.00 \mathrm{k} \Omega$ |
| R103 | $18.00 \mathrm{k} \Omega$ |
| C101 | 100 nF Ceramic Capacitor |
| C106 | 100 nF Ceramic Capacitor |

Test Results

| Test | Condition | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=9 \mathrm{~V}$ to $15 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}$ | 2 mV |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=30 \mathrm{~mA}$ to 350 mA | 5 mV |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}$ to 350 mA | $\leq 350 \mathrm{mV} \mathrm{Vpp}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}$ to 350 mA | $>85.5 \%$ |



Figure 20. Boost Demoboard Layout


Figure 21. Efficiency vs. Output Current for the Boost Demo Board at $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{~V}_{\text {out }}=24 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$


Figure 22. Typical Voltage Inverting Application Schematic

Value of Components

| Name | Value |
| :--- | :--- |
| L501 | $22 \mu \mathrm{H}, \mathrm{I}_{\text {sat }}>1.5 \mathrm{~A}$ |
| D501 | $1 \mathrm{~A}, 40 \mathrm{~V}$ Schottky Rectifier |
| C502 | $330 \mu \mathrm{~F}, 25 \mathrm{~V}$, Low ESR |
| C505 | $470 \mu \mathrm{~F}, 35 \mathrm{~V}$, Low ESR |
| C503 | 2.2 nF Ceramic Capacitor |


| Name | Value |
| :--- | :--- |
| R501 | $150 \mathrm{~m} \Omega, 0.5 \mathrm{~W}$ |
| R502 | $16.9 \mathrm{k} \Omega$ |
| R503 | $1.96 \mathrm{k} \Omega$ |
| C501 | 100 nF Ceramic Capacitor |
| C506 | 100 nF Ceramic Capacitor |

Test Results

| Test | Condition | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=4.5 \mathrm{~V}$ to $6 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}$ | 1.5 mV |
| Load Regulation | $\mathrm{V}_{\text {in }}=5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}$ to 100 mA | 1.6 mV |
| Output Ripple | $\mathrm{V}_{\text {in }}=5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ to 100 mA | $\leq 300 \mathrm{mV} \mathrm{V}_{\mathrm{pp}}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | $49.8 \%$ |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=5 \mathrm{~V}, \mathrm{R}_{\text {load }}=0.15 \Omega$ | 0.885 A |



Figure 23. Voltage Inverting Demoboard Layout


Figure 24. Efficiency vs. Output Current for the Voltage Inverting Demo Board at $\mathrm{V}_{\text {in }}=+5 \mathrm{~V}$, $\mathrm{V}_{\text {out }}=-12 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$


Figure 25. Typical Boost Application Schematic with External NMOS Transistor


Figure 26. Typical Efficiency for Application Shown in Figure 25.

External transistor is recommended in applications where wide input voltage ranges and higher power is required. The suitable schematic with an additional NMOS transistor and its driving circuit is shown in the Figure 25. The driving circuit is controlled from SWE Pin of the NCP3063 through frequency compensated resistor divider R7/R8. The driver IC2 is ON Semiconductor low cost dual NPN/PNP transistor BC846BPD. Its NPN transistor is connected as a super diode for charging the gate capacitance. The PNP transistor works as an emitter follower for discharging the gate capacitor. This configuration assures sharp driving edge between $50-100 \mathrm{~ns}$ as well as it limits power consumption of R7/R8 divider down to 50 mW . The output current limit is balanced by resistor R3. The fast switching with low $\mathrm{R}_{\mathrm{DS}(\text { on })}$ NMOS transistor will achieve efficiencies up to $85 \%$ in automotive applications.


Figure 27. Typical Buck Application Schematic with External PMOS Transistor


Figure 28. NCP3063 Efficiency vs. Output Current for Buck External PMOS at $\mathrm{V}_{\text {out }}=\mathbf{3 . 3} \mathrm{V}, \mathrm{f}=\mathbf{2 2 0} \mathbf{~ k H z}$, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

Figure 27 shows typical buck configuration with external PMOS transistor. The principle of driving the Q2 gate is the same as shown in Figure 27.

Resistor R6 connected between TC and SWE pin provides a pulsed feedback voltage. It is recommended to use this pulsed feedback approach on applications with a wide input voltage range, applications with the input voltage over +12 V or applications with tighter specifications on output ripple. The suitable value of resistor R6 is between 10k - 68k. The pulse feedback approach increases the operating frequency by about $20 \%$. It also creates more regular switching waveforms with constant operating frequency which results in lower output ripple voltage and improved efficiency.

The pulse feedback resistor value has to be selected so that the capacitor charge and discharge currents as listed in the electrical characteristic table, are not exceeded. Improper selection will lead to errors in the oscillator operation. The maximum voltage at the TC Pin cannot exceed 1.4 V when implementing pulse feedback.


Figure 29. Typical Buck Application Schematic with External Low VCE(sat) PNP Transistor


Figure 30. NCP3063 Efficiency vs. Output Current for External Low $\mathrm{V}_{\mathrm{CE}(\mathrm{sat})}$ at $\mathrm{V}_{\mathrm{in}}=+5 \mathrm{~V}, \mathrm{f}=\mathbf{1 6 0} \mathbf{~ k H z}$, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

Typical application of the buck converter with external bipolar transistor is shown in the Figure 29. It is an ideal solution for configurations where the input and output voltage difference is small and high efficiency is required. NSS35200, the low $\mathrm{V}_{\mathrm{CE}}(\mathrm{sat})$ transistor from ON Semiconductor will be ideal for applications with 1 A output current, the input voltages up to 15 V and operating frequency $100-150 \mathrm{kHz}$. The switching speed could be improved by using desaturation diode D 2 .


Figure 31. Typical Schematic of Buck Converter with RC Snubber and Pulse Feedback

In some cases where there are oscillations on the output due to the input/output combination, output load variations or PCB layout a snubber circuit on the SWE Pin will help
minimize the oscillation. Typical usage is shown in the Figure 31. C3 values can be selected between 2.2 nF and 6.8 nF and R 4 can be from $10 \Omega$ to $22 \Omega$.

ORDERING INFORMATION

| Device | Package | Shipping ${ }^{\dagger}$ |
| :--- | :---: | :---: |
| NCP3063PG | PDIP-8 <br> (Pb-Free) | 50 Units / Rail |
| NCP3063BPG | PDIP-8 <br> (Pb-Free) | 50 Units / Rail |
| NCP3063BMNTXG | DFN-8 <br> (Pb-Free) | $4000 /$ Tape \& Reel |
| NCP3063DR2G | SOIC-8 <br> (Pb-Free) | $2500 /$ Tape \& Reel |
| NCP3063BDR2G | SOIC-8 <br> (Pb-Free) | $2500 /$ Tape \& Reel |
| NCP3063MNTXG | DFN-8 <br> (Pb-Free) | $4000 /$ Tape \& Reel |
| NCV3063PG | PDIP-8 <br> (Pb-Free) | 50 Units / Rail |
| NCV3063DR2G | SOIC-8 <br> (Pb-Free) | $2500 /$ Tape \& Reel |
| NCV3063MNTXG | DFN-8 <br> (Pb-Free) | $4000 /$ Tape \& Reel |

[^0]
## PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AJ


| $母$ | $0.25(0.010)(\mathbb{M})$ | $Z$ | $Y(5)$ | $X(5)$ |
| :--- | :--- | :--- | :--- | :--- |

NOTES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE 0.127 ( 0.005 ) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

|  | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 | BSC | 0.050 BSC |  |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | $0{ }^{\circ}$ | $80^{\circ}$ | 0 | 0 |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCP3063, NCP3063B, NCV3063

## PACKAGE DIMENSIONS

## 8 LEAD PDIP <br> CASE 626-05



## NOTES:

1. DIMENSION LTO CENTER OF LEAD WHEN FORMED PARALLEL
PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS
2. DIMENSIONING AND TOLERANCING PER ANS Y14.5M, 1982.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC |  | 0.300 BSC |  |
| M | --- | $10^{\circ}$ | - | $10^{\circ}$ |
| N | 0.76 | 1.01 | 0.030 | 0.040 |
| STYLE 1: |  |  |  |  |
| PIN 1. AC IN |  |  |  |  |
| 2. $\mathrm{DC}+\mathrm{IN}$ |  |  |  |  |
| 3. $\mathrm{DC}-\mathrm{IN}$ |  |  |  |  |
| 4. AC IN |  |  |  |  |
| 5. GROUND |  |  |  |  |
| 6. OUTPUT |  |  |  |  |
| 7. AUXILIARY |  |  |  |  |
| 8. $\mathrm{V}_{\mathrm{CC}}$ |  |  |  |  |

## PACKAGE DIMENSIONS

8 PIN DFN, 4x4
CASE 488AF-01
ISSUE C


SIDE VIEW
NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS

|  | MILLIMETERS |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX |  |  |
| A | 0.80 | 1.00 |  |  |
| A1 | 0.00 | 0.05 |  |  |
| A3 | 0.20 |  |  | REF |
| b | 0.25 |  |  |  |
| D | 0.35 |  |  |  |
| D2 | 4.00 |  |  |  |



BOTTOM VIEW

SOLDERING FOOTPRINT*

*For additional information on our Pb -Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

[^1]
## PUBLICATION ORDERING INFORMATION

## LITERATURE FULFILLMENT

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ON Semiconductor Website: www.onsemi.com Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative


[^0]:    $\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
    NCV prefix is for automotive and other applications requiring site and change control.

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