

## Avalanche-Energy-Rated N-Channel Power MOSFETs

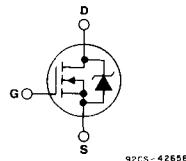
25 A and 22 A, 400 V

$r_{DS(on)} = 0.20 \Omega$  and  $0.25 \Omega$

### Features:

- Single pulse avalanche energy rated
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance

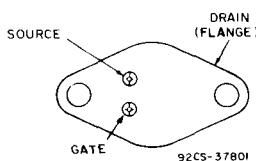
### N-CHANNEL ENHANCEMENT MODE



92CS-42658

TERMINAL DIAGRAM

### TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AE

The IRF360 and IRF362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

### ABSOLUTE MAXIMUM RATINGS

Parameter	IRF360	IRF362	Units
$I_D @ T_C = 25^\circ C$ Continuous Drain Current	25	22	A
$I_D @ T_C = 100^\circ C$ Continuous Drain Current	16	14	A
$I_{DM}$ Pulsed Drain Current ①	100	88	A
$P_D @ T_C = 25^\circ C$ Max. Power Dissipation	300		W
Linear Derating Factor	2.4		W/ $^\circ C$
$V_{GS}$ Gate-to-Source Voltage	$\pm 20$		V
EAS Single Pulse Avalanche Energy ②	980 (See Fig. 14)		mJ
$I_{AR}$ Avalanche Current ③ (Repetitive or Non-Repetitive)	25		A
$T_J$ Operating Junction Temperature	-55 to 150		$^\circ C$
$T_{STG}$ Storage Temperature Range			
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		$^\circ C$

**IRF360, IRF362****ELECTRICAL CHARACTERISTICS At Case Temperature ( $T_J = 25^\circ C$ ) Unless Otherwise Specified**

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$ Drain-to-Source Breakdown Voltage	ALL	400	—	—	V	$V_{GS} = 0V, I_D = 250 \mu A$
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance ③	IRF360	—	0.18	0.20	$\Omega$	$V_{GS} = 10V, I_D = 14A$
	IRF362	—	0.20	0.25		
$I_{D(on)}$ On-State Drain Current ③	IRF360	25	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ Max.}$ $V_{GS} = 10V$
	IRF362	22	—	—		
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
$g_{fs}$ Forward Transconductance ③	ALL	14	21	—	S (Ω)	$I_{DS} = 14A, V_{DS} \geq 50V$
$I_{DSS}$ Zero Gate Voltage Drain Current	ALL	—	—	250	$\mu A$	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$
	ALL	—	—	1000		$V_{DS} = 0.8 \times \text{Max. Rating}$ $V_{GS} = 0V, T_J = 125^\circ C$
$I_{GSS}$ Gate-to-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
$I_{GSR}$ Gate-to-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
$Q_g$ Total Gate Charge	ALL	—	120	170	nC	$V_{GS} = 10V, I_D = 25A$
$Q_{gs}$ Gate-to-Source Charge	ALL	—	19	28	nC	$V_{DS} = 0.8 \times \text{Max. Rating}$
$Q_{gd}$ Gate-to-Drain ("Miller") Charge	ALL	—	60	90	nC	See Fig. 16 (Independent of operating temperature)
$t_{d(on)}$ Turn-On Delay Time	ALL	—	22	33	ns	$V_{DD} = 200V, I_D = 25A, R_G = 4.3\Omega$ $R_D = 7.5\Omega$ See Fig. 15
$t_r$ Rise Time	ALL	—	94	140	ns	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	80	120	ns	
$t_f$ Fall Time	ALL	—	66	99	ns	
$L_D$ Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
$L_S$ Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
$C_{iss}$ Input Capacitance	ALL	—	4000	—	pF	$V_{GS} = 0V, V_{DS} = 25V$
$C_{oss}$ Output Capacitance	ALL	—	550	—	pF	$f = 1.0 \text{ MHz}$
$C_{rss}$ Reverse Transfer Capacitance	ALL	—	97	—	pF	See Fig. 10
$R_{thJC}$ Junction-to-Case	ALL	—	—	0.42	°C/W	
$R_{thCS}$ Case-to-Sink	ALL	—	0.12	—	°C/W	Mounting surface flat, smooth, and greased
$R_{thJA}$ Junction-to-Ambient	ALL	—	—	30	°C/W	Typical socket mount

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
$I_S$ Continuous Source Current (Body Diode)	ALL	—	—	25	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier
$I_{SM}$ Pulsed Source Current (Body Diode) ①	ALL	—	—	100	A	
$V_{SD}$ Diode Forward Voltage ③	ALL	—	—	1.8	V	$T_J = 25^\circ C, I_S = 25A, V_{GS} = 0V$
$t_{rr}$ Reverse Recovery Time	ALL	200	460	1000	ns	$T_J = 25^\circ C, I_F = 25A, dI/dt = 100 A/\mu s$
$Q_{RR}$ Reverse Recovery Charge	ALL	3.1	7.1	16	μC	
$t_{on}$ Forward Turn-On Time	ALL	—	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$			



① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5)

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

② @  $V_{DD} = 50V$ , Starting  $T_J = 25^\circ C$ ,  $L = 2.8 \text{ mH}$ , Peak  $I_L = 25A$ ,

## IRF360, IRF362

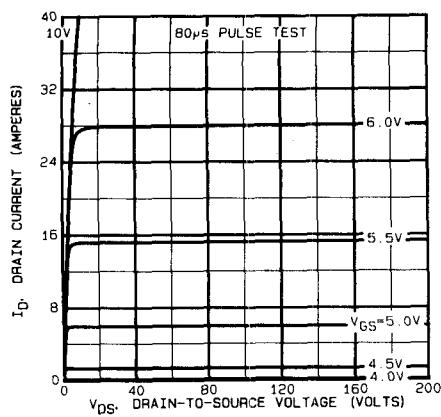


Fig. 1 - Typical output characteristics.

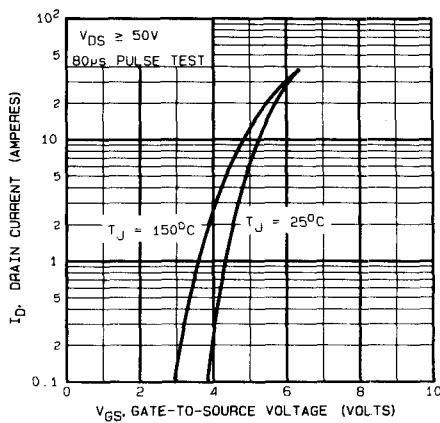


Fig. 2 - Typical transfer characteristics.

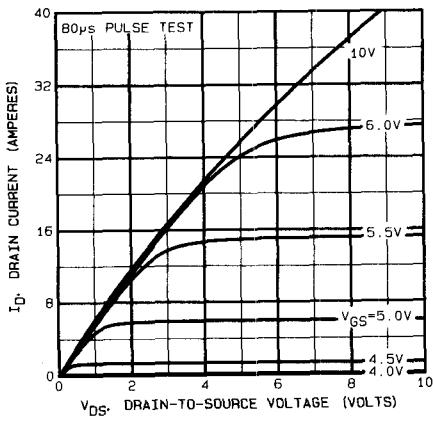


Fig. 3 - Typical saturation characteristics.

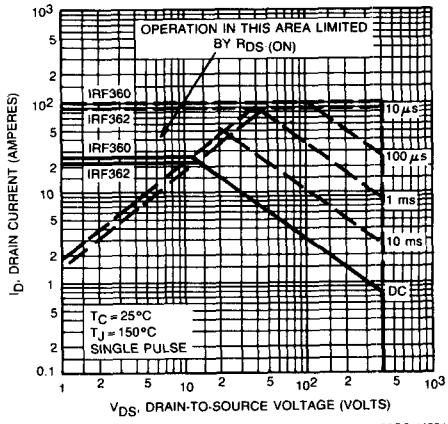


Fig. 4 - Maximum safe operating area.

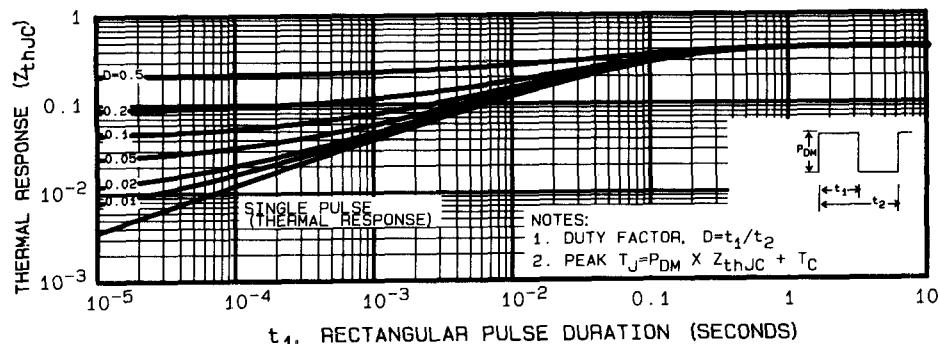


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

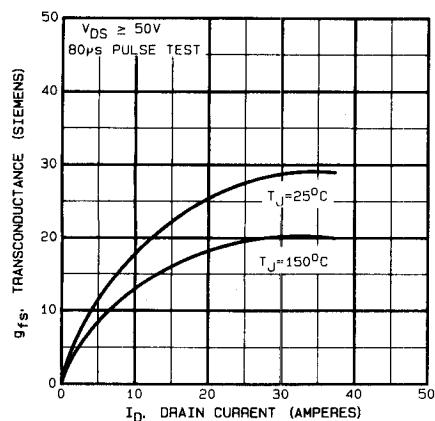
**IRF360, IRF362**

Fig. 6 - Typical transconductance vs. drain current.

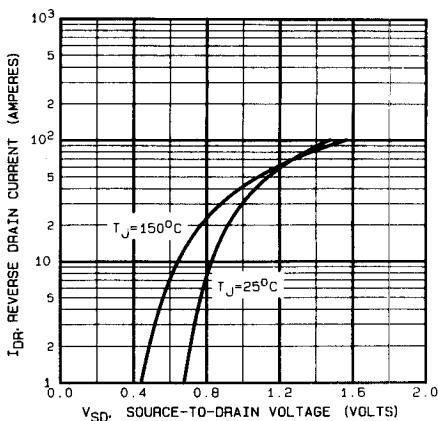


Fig. 7 - Typical source-drain diode forward voltage.

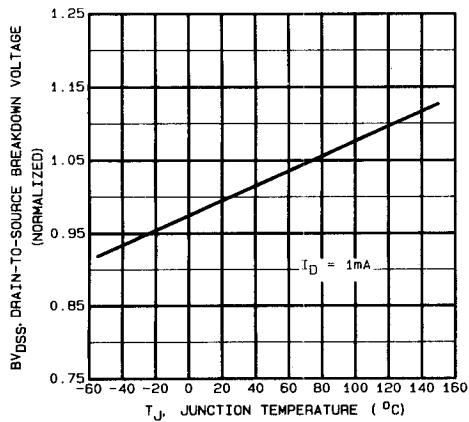


Fig. 8 - Breakdown voltage vs. temperature.

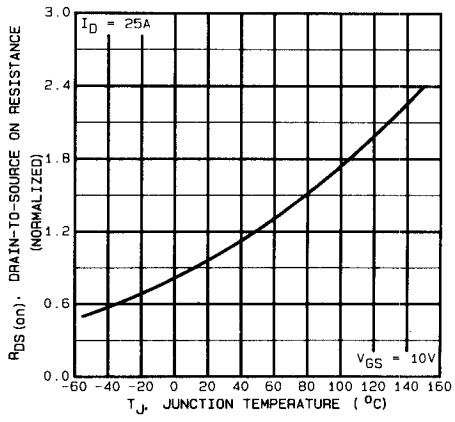


Fig. 9 - Normalized on-resistance vs. temperature.

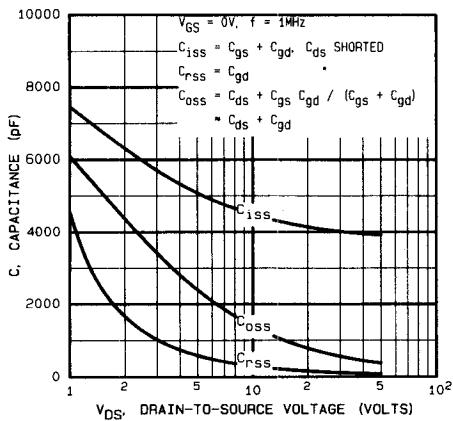


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

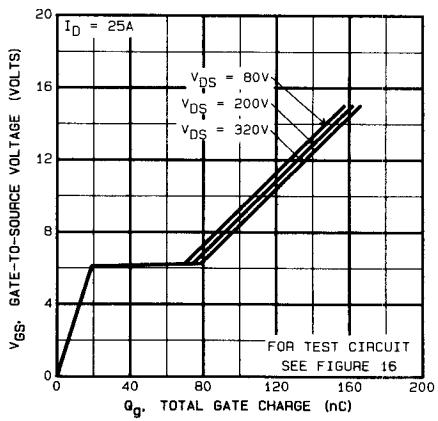


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

## IRF360, IRF362

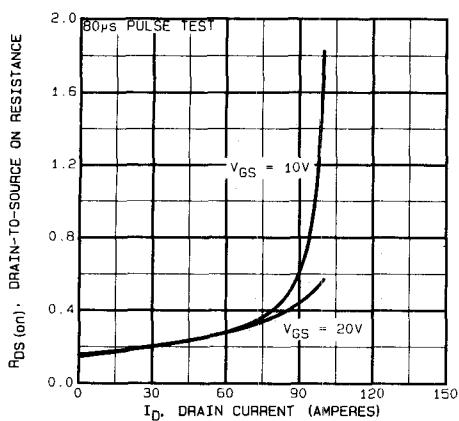


Fig. 12 - Typical on-resistance vs. drain current.

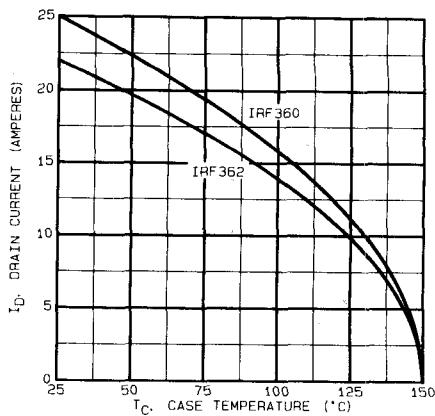


Fig. 13 - Maximum drain current vs. case temperature.

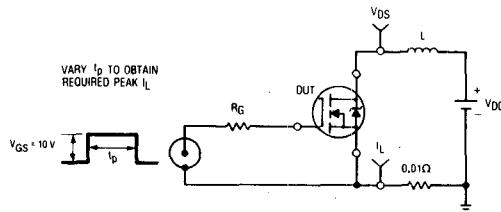


Fig. 14a - Unclamped inductive test circuit.

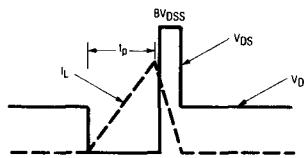


Fig. 14b - Unclamped inductive waveforms.

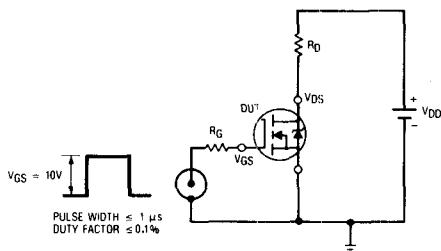


Fig. 15a - Switching time test circuit.

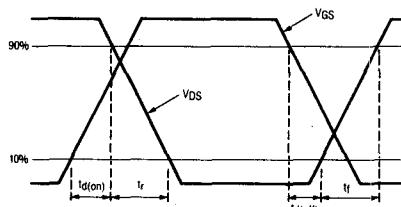


Fig. 15b - Switching time waveforms.

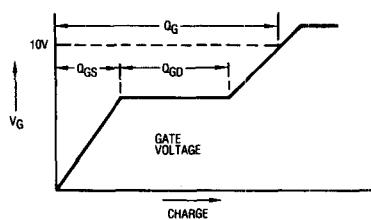


Fig. 16a - Basic gate charge waveform.

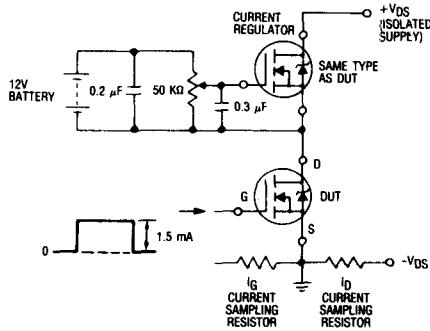


Fig. 16b - Gate charge test circuit.