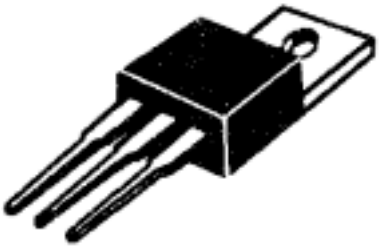
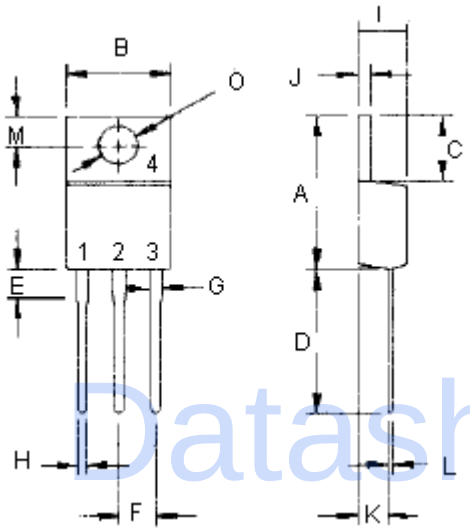
Silicon Power Transistor

TO-220



Features:

- Collector-Emitter Sustaining Voltage -
  $V_{CE(SUS)}$ = 100 V (Minimum) TIP117
- Collector-Emitter Saturation Voltage
  $V_{CE(Sat)}$ = 2.5 V (Maximum) at I_C = 2 A
- Monolithic Construction with Built-in Base-Emitter Shunt Resistor



Pin
1. Base
2. Collector
3. Emitter
4. Collector (Case)

Dimensions	Millimetres	
	Minimum	Maximum
A	14.68	15.31
B	9.78	10.42
C	5.01	6.52
D	13.06	14.62
E	3.57	4.07
F	2.42	3.66
G	1.12	1.36
H	0.72	0.96
I	4.22	4.96
J	1.14	1.38
K	2.2	2.97
L	0.33	0.55
M	2.48	2.98
O	3.7	3.9

Plastic medium-power Silicon Transistors designed for general purpose amplifier and low speed switching applications

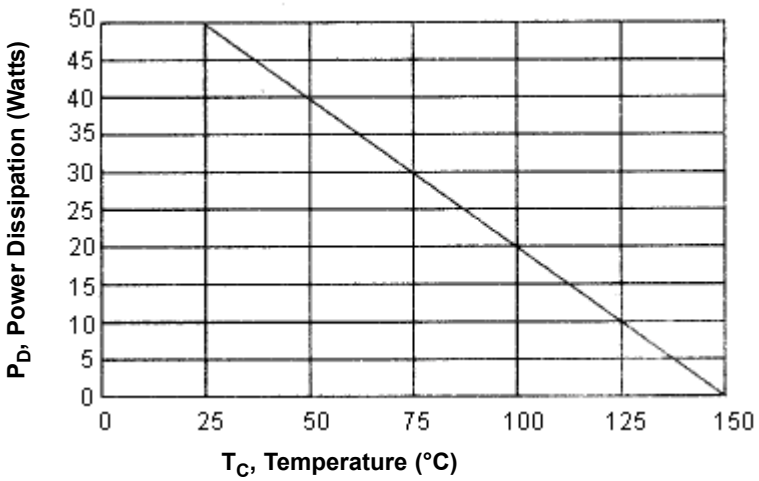
Maximum Ratings

Characteristics	Symbol	TIP117	Unit
Collector-Emitter Voltage	V_{CEO}	100	V
Collector-Emitter Voltage	V_{CBO}	100	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current - Continuous Peak	I_C I_{CM}	2 4	A
Base Current	I_B	50	mA
Total Power Dissipation at T_c = 25°C Derate above 25°C	P_D	50 0.4	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-65 to +150	°C

Maximum Ratings

Characteristics	Symbol	Maximum	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	2.5	°C/W

Figure 1 Power Derating



Electrical Characteristics (T_c = 25°C Unless Otherwise Noted)

Characteristics	Symbol	Minimum	Maximum	Unit
OFF Characteristics				
Collector-Emitter Sustaining Voltage (1)	$V_{CEO(SUS)}$	100		V
Collector Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}		2	mA
Collector Cutoff Current (V_{EB} = 5 V, I_C = 0)	I_{EBO}		2	mA
ON Characteristics (1)				
DC Current Gain (I_C = 1 A, V_{CE} = 4 V) (I_C = 2 A, V_{CE} = 4 V)	hFE	1,000 500		
Collector-Emitter Saturation Voltage (I_C = 2 A, I_B = 8 mA)	$V_{CE(Sat)}$		2.5	V
Base-Emitter On Voltage (I_C = 2 A, V_{CE} = 4 mA)	$V_{BE(ON)}$		2.8	V
Dynamic Characteristics				
Small-Signal Current Gain (I_c = 0.75 A, V_{CE} = 10 V, f = 1 MHz)	h_{fe}	25		
Output Capacitance	C_{ob}	150		$_P$F

(1) Pulse Test : Pulse Width = 300 us, Duty Cycle ≤ 2%

Internal Schematic Diagram

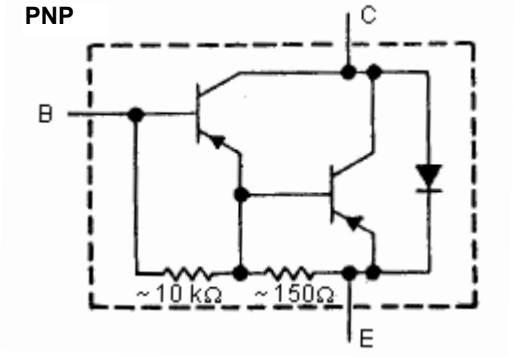


Fig-1 Switching Time

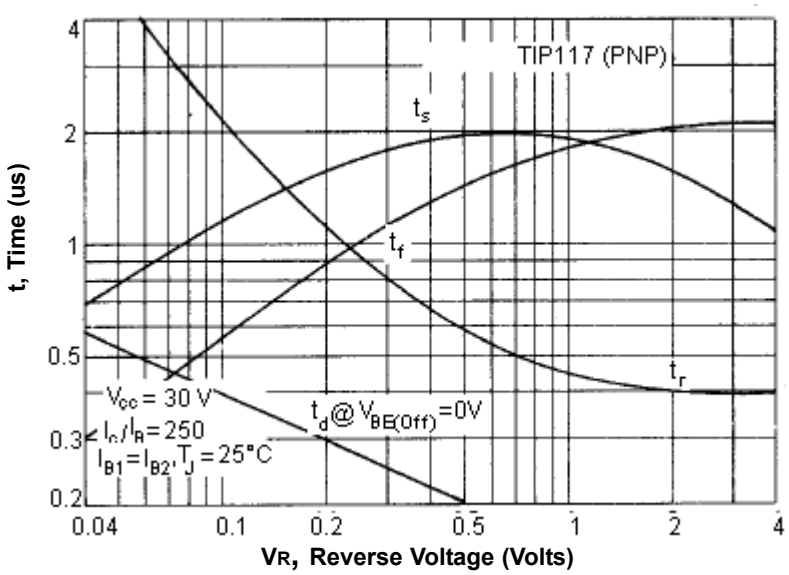


Fig-2 Capacitances

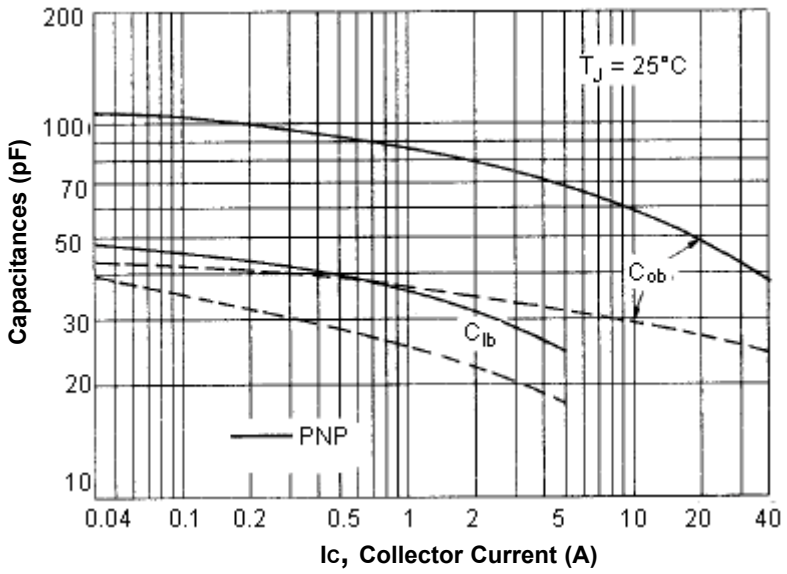
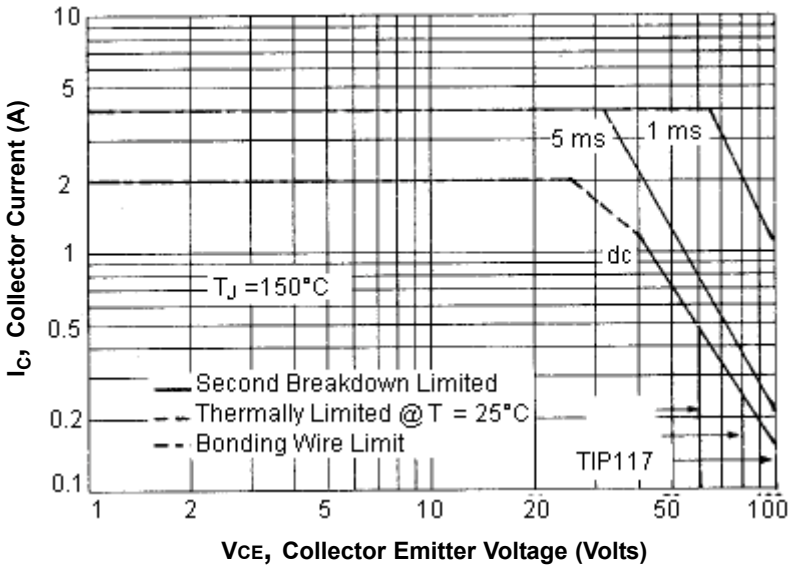


Fig-3 Active Region Safe Operating Area



There are two limitation on the power handling ability of a transistor : average junction temperature and second breakdown safe operating area curves indicate $I_C \sim V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of Fig-3 is base on $T_{J(PK)}$=150°C; TC is variable depending on power level, second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)} \leq 150°C$, at high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Part Number Table

Description	Part Number
Silicon Power Transistor	TIP117