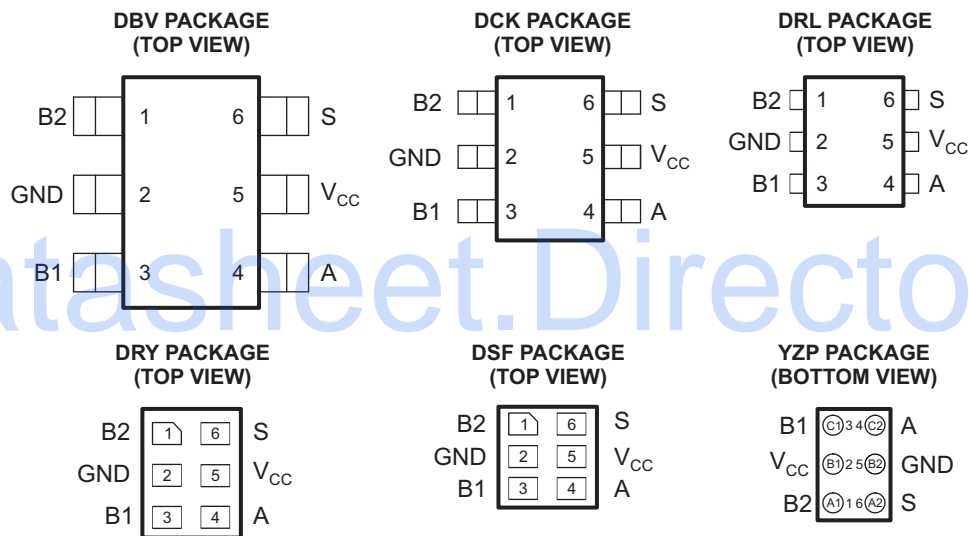


SINGLE-POLE DOUBLE-THROW ANALOG SWITCH

Check for Samples: [SN74LVC1G3157](#)

FEATURES

- 1.65-V to 5.5-V V_{CC} Operation
- Useful for Both Analog and Digital Applications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- High Degree of Linearity
- High Speed, Typically 0.5 ns ($V_{CC} = 3\text{ V}$, $C_L = 50\text{ pF}$)
- Low On-State Resistance, Typically $\approx 6\ \Omega$ ($V_{CC} = 4.5\text{ V}$)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single-pole double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G3157 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

ORDERING INFORMATION

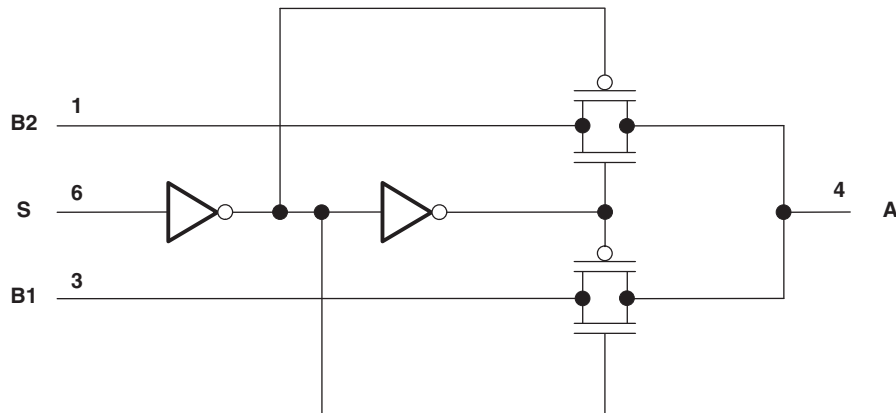
| T _A | PACKAGE ^{(1) (2)} | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|----------------|--|--------------|-----------------------|---------------------------------|
| -40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74LVC1G3157YZPR | _ _ _ C5_ |
| | SON – DRY | Reel of 5000 | SN74LVC1G3157DRYR | C5_ |
| | SON – DSF | Reel of 5000 | SN74LVC1G3157DSFR | C5 |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74LVC1G3157DBVR | CC5_ |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74LVC1G3157DCKR | C5_ |
| | SOT (SOT-553) – DRL | Reel of 4000 | SN74LVC1G3157DRLR | C5_ |

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DBV/DCK/DRL/DRY: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Table 1. FUNCTION TABLE

| CONTROL INPUT S | ON CHANNEL |
|-----------------|------------|
| L | B1 |
| H | B2 |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|--|-----------------------|------|
| V _{CC} | Supply voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V _{IN} | Control input voltage range ^{(2) (3)} | -0.5 | 6.5 | V |
| V _{I/O} | Switch I/O voltage range ^{(2) (3) (4) (5)} | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Control input clamp current | V _{IN} < 0 | -50 | mA |
| I _K | I/O port diode current | V _{I/O} < 0 or V _{I/O} > V _{CC} | ±50 | mA |
| I _{I/O} | On-state switch current ⁽⁶⁾ | V _{I/O} = 0 to V _{CC} | ±128 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| θ _{JA} | Package thermal impedance ⁽⁷⁾ | DBV package | 165 | °C/W |
| | | DCK package | 259 | |
| | | DRL package | 142 | |
| | | DRY package | 234 | |
| | | YZP package | 123 | |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for V_{I/O}.
- (6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for I_{I/O}.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|------------------------------------|------------------------|------|
| V _{CC} | Supply voltage | 1.65 | 5.5 | V |
| V _{I/O} | Switch input/output voltage | 0 | V _{CC} | V |
| V _{IN} | Control input voltage | 0 | 5.5 | V |
| V _{IH} | High-level input voltage, control input | V _{CC} = 1.65 V to 1.95 V | V _{CC} × 0.75 | V |
| | | V _{CC} = 2.3 V to 5.5 V | V _{CC} × 0.7 | |
| V _{IL} | Low-level input voltage, control input | V _{CC} = 1.65 V to 1.95 V | V _{CC} × 0.25 | V |
| | | V _{CC} = 2.3 V to 5.5 V | V _{CC} × 0.3 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.65 V to 1.95 V | 20 | ns/V |
| | | V _{CC} = 2.3 V to 2.7 V | 20 | |
| | | V _{CC} = 3 V to 3.6 V | 10 | |
| | | V _{CC} = 4.5 V to 5.5 V | 10 | |
| T _A | Operating free-air temperature | –40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---------------------------------|---|---|--------|--------------------|-------------------------------|------|
| r _{on} | On-state switch resistance ⁽²⁾ See Figure 1 and Figure 2 | V _I = 0 V, I _O = 4 mA | 1.65 V | 11 | 20 | Ω |
| | | V _I = 1.65 V, I _O = –4 mA | | 15 | 50 | |
| | | V _I = 0 V, I _O = 8 mA | 2.3 V | 8 | 12 | |
| | | V _I = 2.3 V, I _O = –8 mA | | 11 | 30 | |
| | | V _I = 0 V, I _O = 24 mA | 3 V | 7 | 9 | |
| | | V _I = 3 V, I _O = –24 mA | | 9 | 20 | |
| | | V _I = 0 V, I _O = 30 mA | 4.5 V | 6 | 7 | |
| | | V _I = 2.4 V, I _O = –30 mA | | 7 | 12 | |
| | | V _I = 4.5 V, I _O = –30 mA | | 7 | 15 | |
| r _{range} | On-state switch resistance over signal range ^{(2) (3)} 0 ≤ V _{Bn} ≤ V _{CC} (see Figure 1 and Figure 2) | I _A = –4 mA, 1.65 V | | | 140 | Ω |
| | | I _A = –8 mA, 2.3 V | | | 45 | |
| | | I _A = –24 mA, 3 V | | | 18 | |
| | | I _A = –30 mA, 4.5 V | | | 10 | |
| Δr _{on} | Difference of on-state resistance between switches ^{(2) (4) (5)} See Figure 1 | V _{Bn} = 1.15 V, I _A = –4 mA | 1.65 V | 0.5 | | Ω |
| | | V _{Bn} = 1.6 V, I _A = –8 mA | 2.3 V | 0.1 | | |
| | | V _{Bn} = 2.1 V, I _A = –24 mA | 3 V | 0.1 | | |
| | | V _{Bn} = 3.15 V, I _A = –30 mA | 4.5 V | 0.1 | | |
| r _{on(Flat)} | ON resistance flatness ^{(2) (4) (6)} 0 ≤ V _{Bn} ≤ V _{CC} | I _A = –4 mA, 1.65 V | | 110 | | Ω |
| | | I _A = –8 mA, 2.3 V | | 26 | | |
| | | I _A = –24 mA, 3 V | | 9 | | |
| | | I _A = –30 mA, 4.5 V | | 4 | | |
| I _{off} ⁽⁷⁾ | Off-state switch leakage current 0 ≤ V _I , V _O ≤ V _{CC} (see Figure 3) | 1.65 V to 5.5 V | | | ±1 ±0.05 ±1 ⁽¹⁾ | μA |

(1) T_A = 25°C

(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. On-state resistance is determined by the lower of the voltages on the two (A or B) ports.

(3) Specified by design

(4) Δr_{on} = r_{on(max)} – r_{on(min)} measured at identical V_{CC}, temperature, and voltage levels

(5) This parameter is characterized, but not production tested.

(6) Flatness is defined as the difference between the maximum and minimum values of on-state resistance over the specified range of conditions.

(7) I_{off} is the same as I_{S(off)} (off-state switch leakage current).

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--|---------------------------------|--|-----------------|-----|--------------------|-------------------------|------|
| I _{S(on)} | On-state switch leakage current | V _I = V _{CC} or GND, V _O = Open (see Figure 4) | 5.5 V | | | ±1 | μA |
| | | | | | | ±0.1 ⁽¹⁾ | |
| I _{IN} | Control input current | 0 ≤ V _{IN} ≤ V _{CC} | 0 V to 5.5 V | | | ±1 | μA |
| | | | | | | ±0.05 ±1 ⁽¹⁾ | |
| I _{CC} | Supply current | V _{IN} = V _{CC} or GND | 5.5 V | | | 1 10 | μA |
| ΔI _{CC} | Supply-current change | V _{IN} = V _{CC} – 0.6 V | 5.5 V | | | 500 | μA |
| C _{Control input capacitance} | Control input capacitance | S | 5 V | | | 2.7 | pF |
| C _{io(off)} | Switch input/output capacitance | Bn | 5 V | | | 5.2 | pF |
| C _{io(on)} | Switch input/output capacitance | Bn | 5 V | | | 17.3 | pF |
| | | A | | | | 17.3 | |

Analog Switch Characteristics

 $T_A = 25^\circ\text{C}$

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|---|--------------|-------------|--|-----------------|-------|------|
| Frequency response ⁽¹⁾ (switch on) | A or Bn | Bn or A | R _L = 50 Ω, f _{in} = sine wave (see Figure 6) | 1.65 V | 300 | MHz |
| | | | | 2.3 V | 300 | |
| | | | | 3 V | 300 | |
| | | | | 4.5 V | 300 | |
| Crosstalk ⁽²⁾ (between switches) | B1 or B2 | B2 or B1 | R _L = 50 Ω, f _{in} = 10 MHz (sine wave) (see Figure 7) | 1.65 V | -54 | dB |
| | | | | 2.3 V | -54 | |
| | | | | 3 V | -54 | |
| | | | | 4.5 V | -54 | |
| Feed through attenuation ⁽²⁾ (switch off) | A or Bn | Bn or A | C _L = 5 pF, R _L = 50 Ω, f _{in} = 10 MHz (sine wave) (see Figure 8) | 1.65 V | -57 | dB |
| | | | | 2.3 V | -57 | |
| | | | | 3 V | -57 | |
| | | | | 4.5 V | -57 | |
| Charge injection ⁽³⁾ | S | A | C _L = 0.1 nF, R _L = 1 MΩ (see Figure 9) | 3.3 V | 3 | pC |
| | | | | 5 V | 7 | |
| Total harmonic distortion | A or Bn | Bn or A | V _I = 0.5 V _{p-p} , R _L = 600 Ω, f _{in} = 600 Hz to 20 kHz (sine wave) (see Figure 10) | 1.65 V | 0.1 | % |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

(3) Specified by design

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5 and Figure 11)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|---------------------------------|--------------|-------------|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} ⁽¹⁾ | A or Bn | Bn or A | 2 | | 1.2 | | 0.8 | | 0.3 | | ns |
| t _{en} ⁽²⁾ | S | Bn | 7 | 24 | 3.5 | 14 | 2.5 | 7.6 | 1.7 | 5.7 | ns |
| t _{dis} ⁽³⁾ | | | 3 | 13 | 2 | 7.5 | 1.5 | 5.3 | 0.8 | 3.8 | |
| t _{B-M} ⁽⁴⁾ | | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

(2) t_{en} is the slower of t_{PZL} or t_{PZH}.

(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.

(4) Specified by design

PARAMETER MEASUREMENT INFORMATION

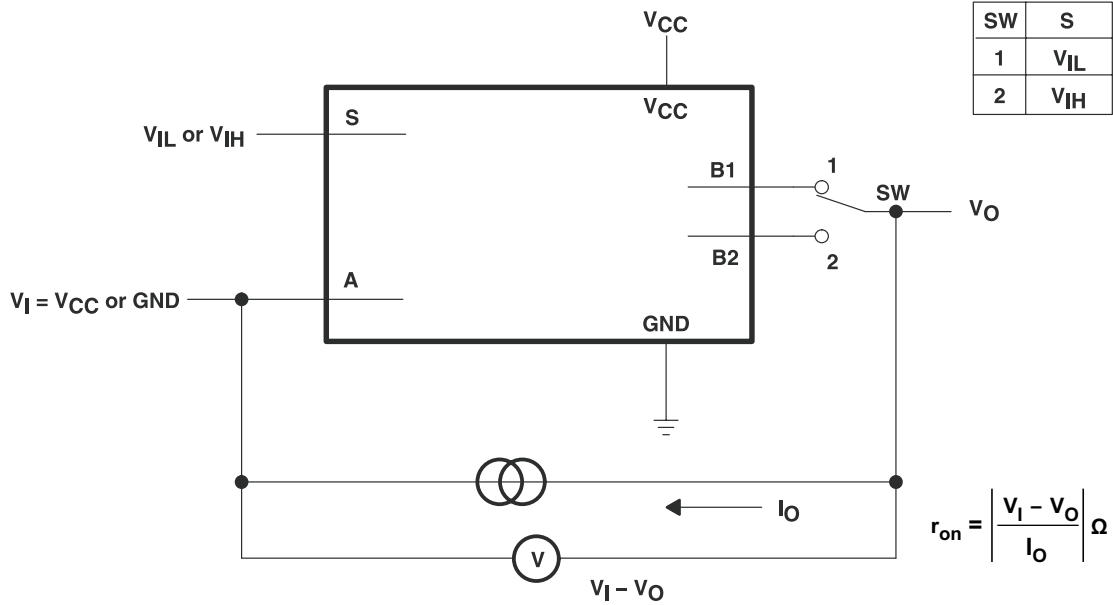


Figure 1. On-State Resistance Test Circuit

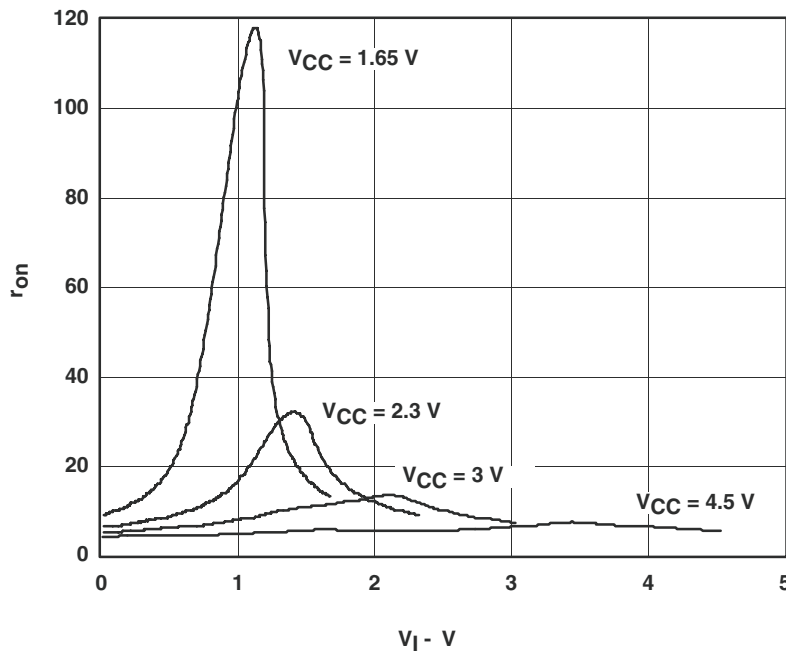
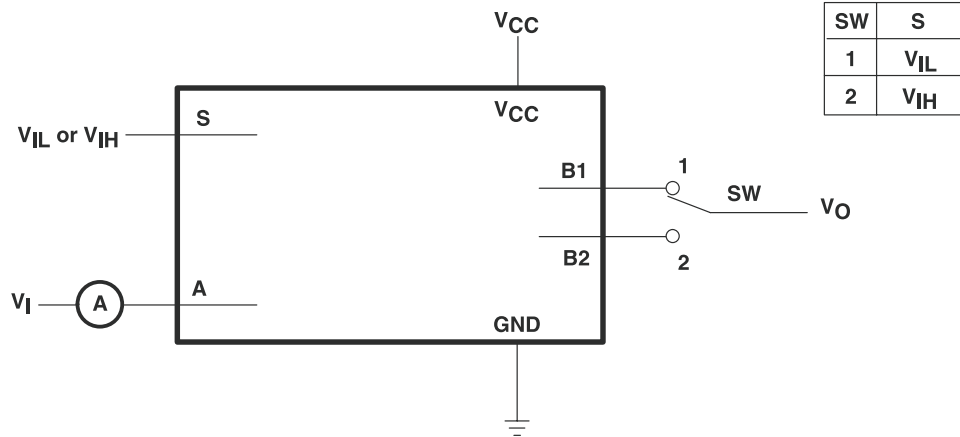


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for $V_I = 0$ to V_{CC}

PARAMETER MEASUREMENT INFORMATION (continued)



Condition 1: V_I = GND, V_O = V_{CC}
 Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. Off-State Switch Leakage-Current Test Circuit

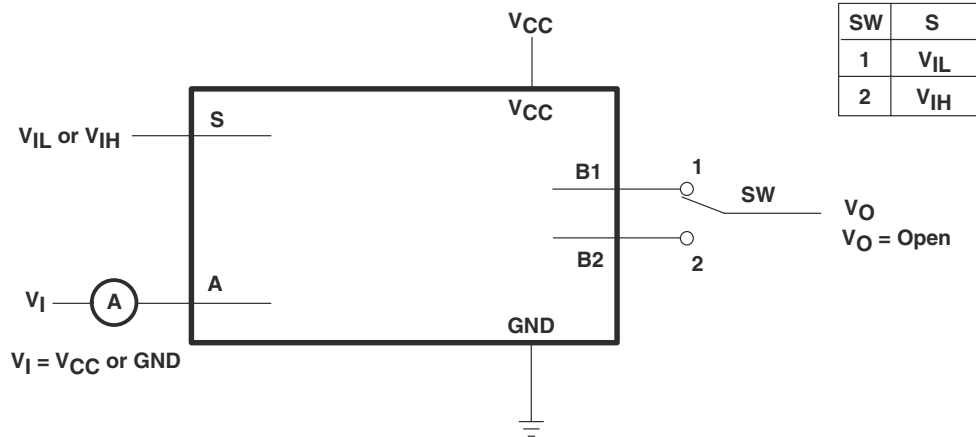
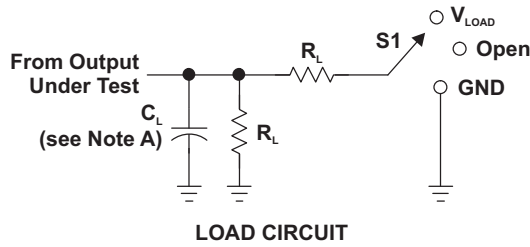


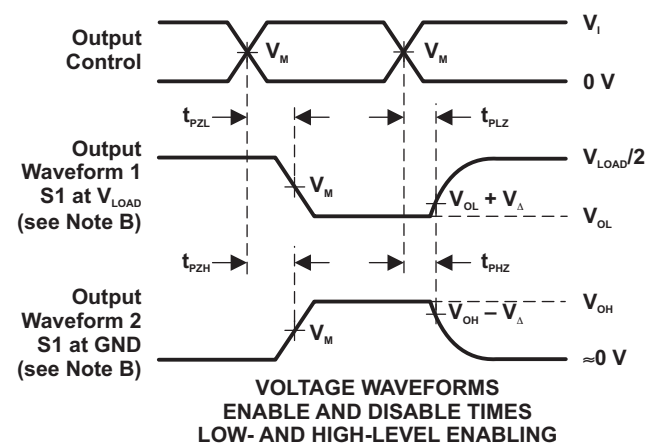
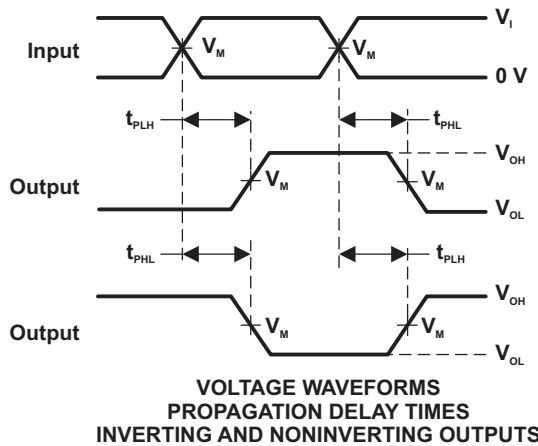
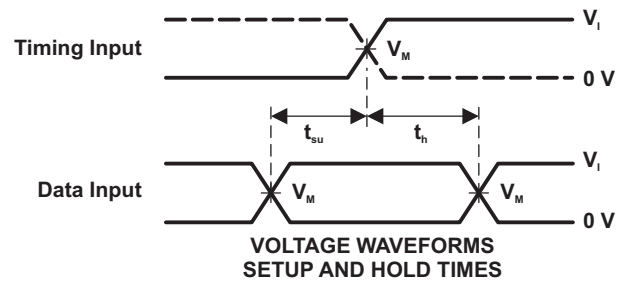
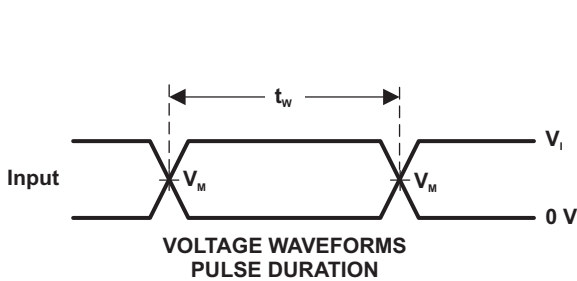
Figure 4. On-State Switch Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|--------------------|----------|-----------------------|------------|-------------------|-------|--------------|--------------|
| | V_i | t_r/t_f | | | | | |
| $1.8 V \pm 0.15 V$ | V_{CC} | $\leq 2 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |
| $2.5 V \pm 0.2 V$ | V_{CC} | $\leq 2 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |
| $3.3 V \pm 0.3 V$ | V_{CC} | $\leq 2.5 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |
| $5 V \pm 0.5 V$ | V_{CC} | $\leq 2.5 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_o = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

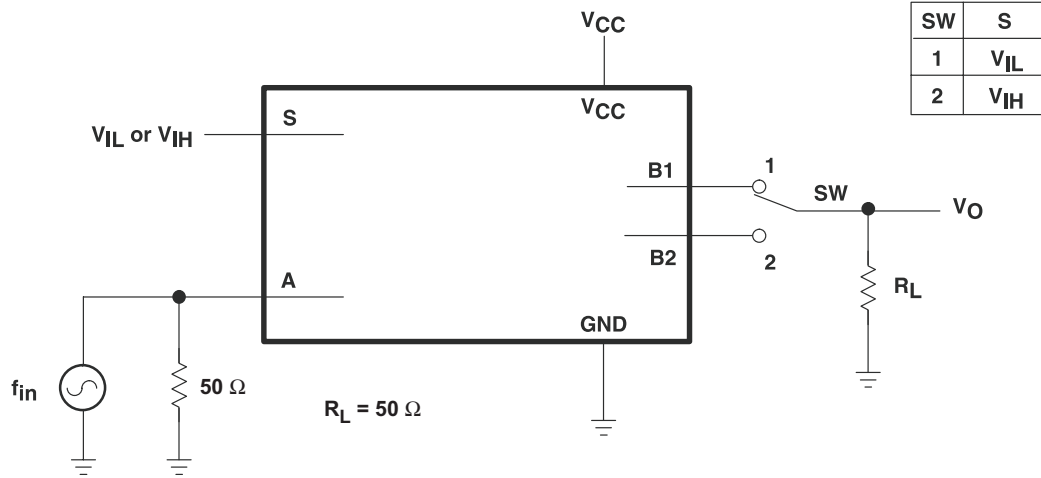


Figure 6. Frequency Response (Switch On)

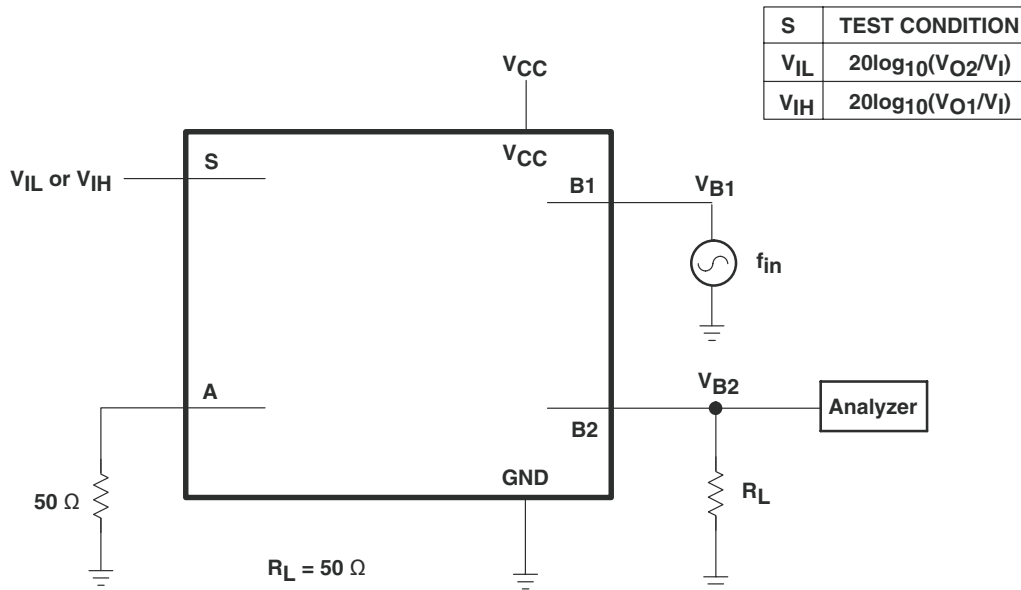


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION (continued)

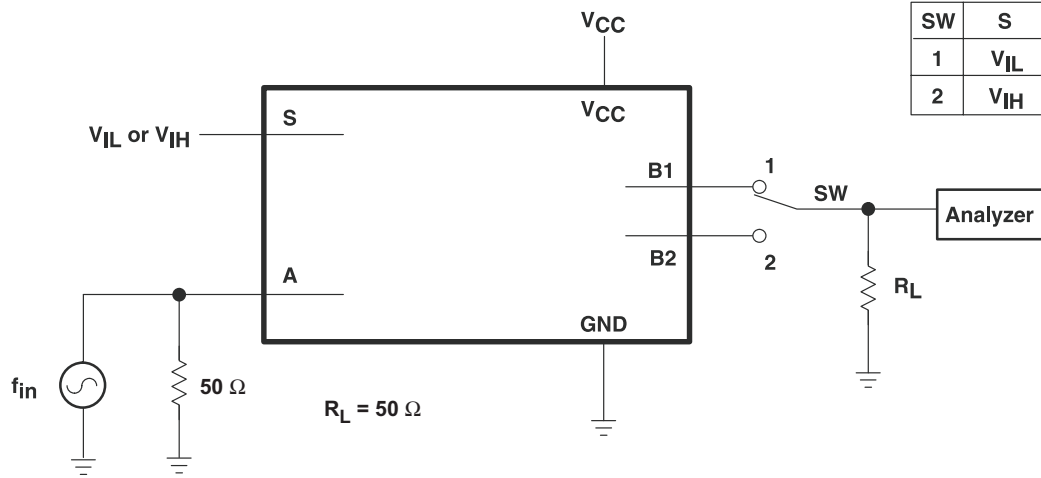


Figure 8. Feedthrough

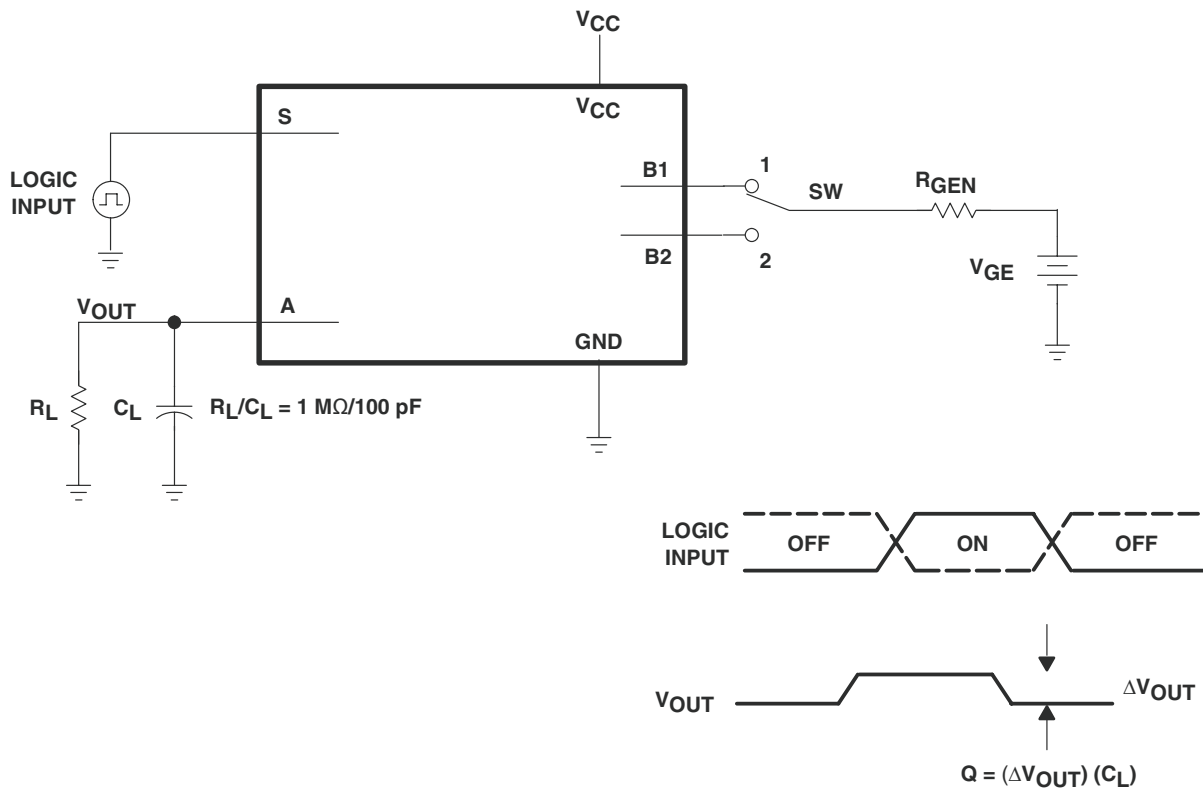


Figure 9. Charge-Injection Test

PARAMETER MEASUREMENT INFORMATION (continued)

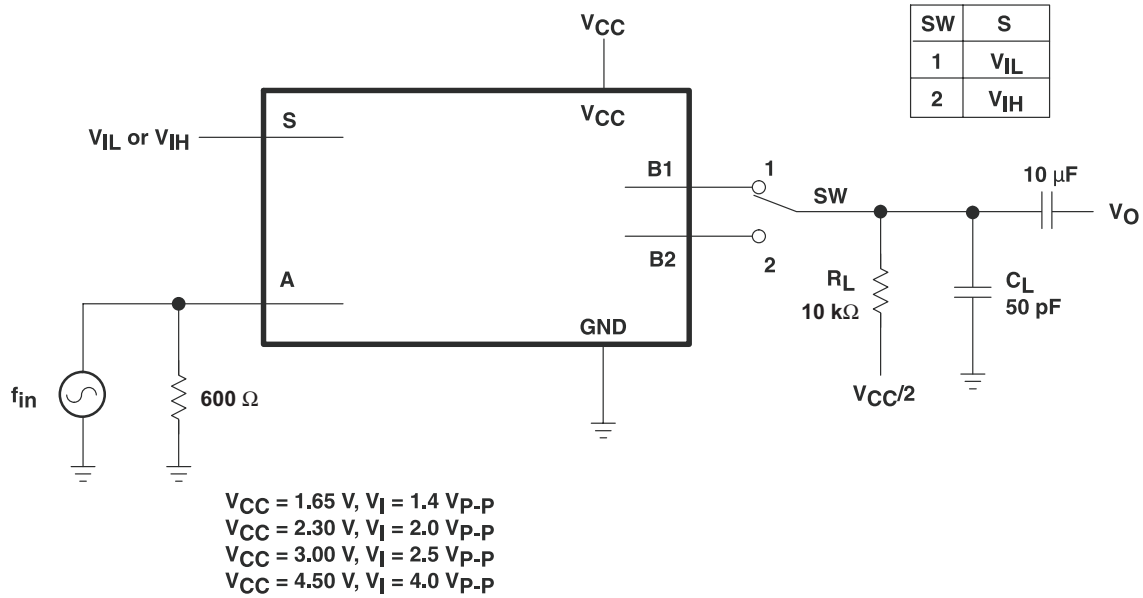


Figure 10. Total Harmonic Distortion

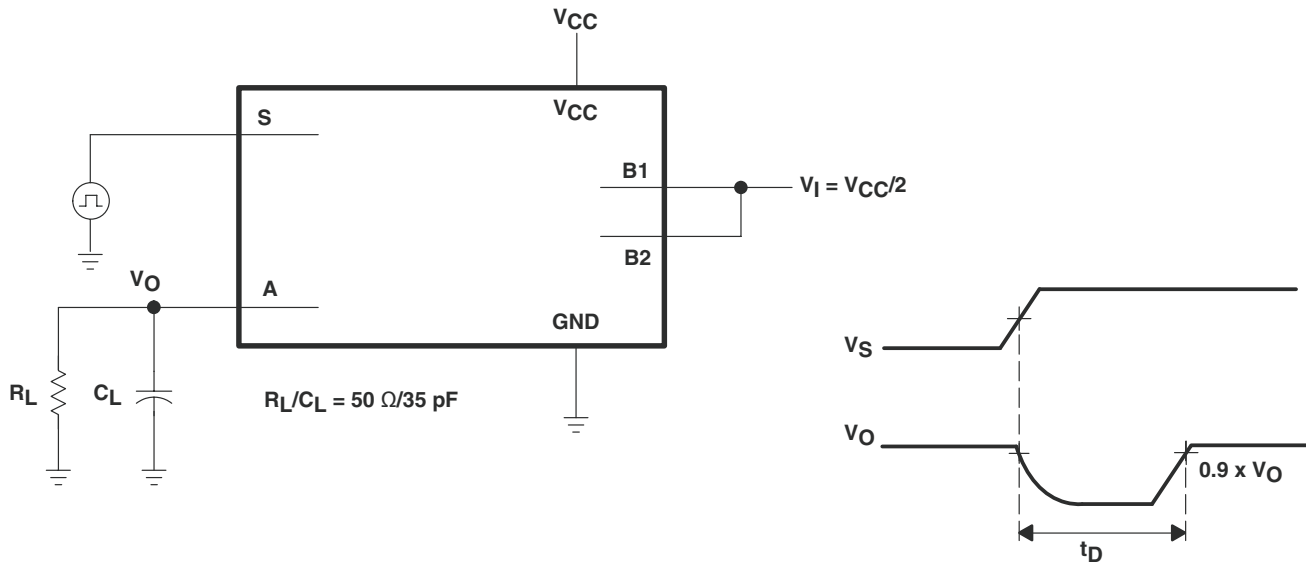


Figure 11. Break-Before-Make Internal Timing

REVISION HISTORY

| Changes from Revision F (February 2007) to Revision G | Page |
|--|-------------------|
| • Added DSF package to datasheet. | 1 |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| 74LVC1G3157DBVRE4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74LVC1G3157DBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74LVC1G3157DCKRE4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74LVC1G3157DCKRG4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74LVC1G3157DRLRG4 | ACTIVE | SOT | DRL | 6 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74LVC1G3157DRYRG4 | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC1G3157DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC1G3157DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC1G3157DGVR | PREVIEW | SOT-23 | DBV | 6 | | TBD | Call TI | Call TI | |
| SN74LVC1G3157DRLR | ACTIVE | SOT | DRL | 6 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC1G3157DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC1G3157DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVC1G3157YZPR | ACTIVE | DSBGA | YZP | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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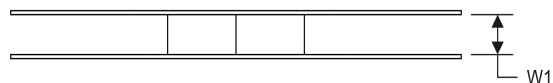
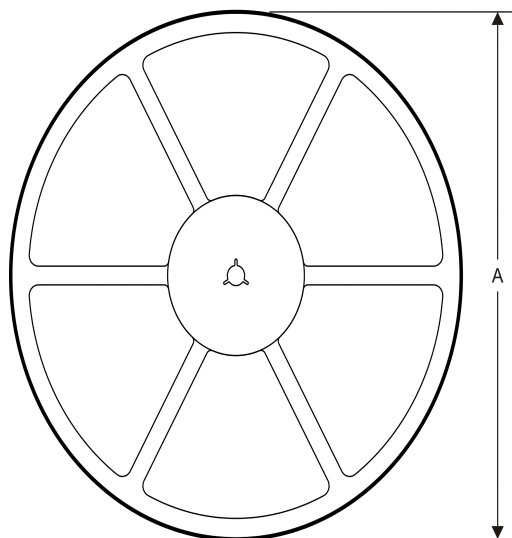
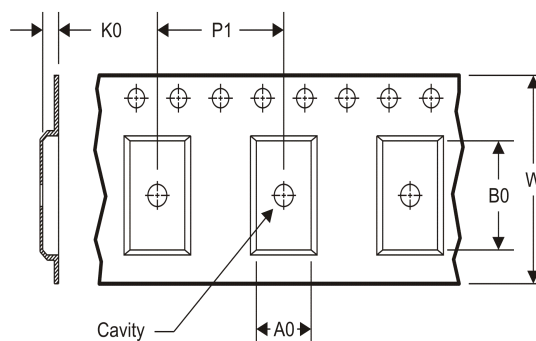
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OTHER QUALIFIED VERSIONS OF SN74LVC1G3157 :

- Automotive: [SN74LVC1G3157-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G3157DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G3157DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 9.2 | 3.17 | 3.23 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G3157DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G3157DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G3157DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G3157DRLR | SOT | DRL | 6 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G3157DRYR | SON | DRY | 6 | 5000 | 179.0 | 8.4 | 1.2 | 1.65 | 0.7 | 4.0 | 8.0 | Q1 |
| SN74LVC1G3157DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G3157YZPR | DSBGA | YZP | 6 | 3000 | 180.0 | 8.4 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G3157DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G3157DBVR | SOT-23 | DBV | 6 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G3157DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G3157DCKR | SC70 | DCK | 6 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G3157DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G3157DRLR | SOT | DRL | 6 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G3157DRYR | SON | DRY | 6 | 5000 | 203.0 | 203.0 | 35.0 |
| SN74LVC1G3157DSFR | SON | DSF | 6 | 5000 | 180.0 | 180.0 | 30.0 |
| SN74LVC1G3157YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 34.0 |

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- $\triangle E$ Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

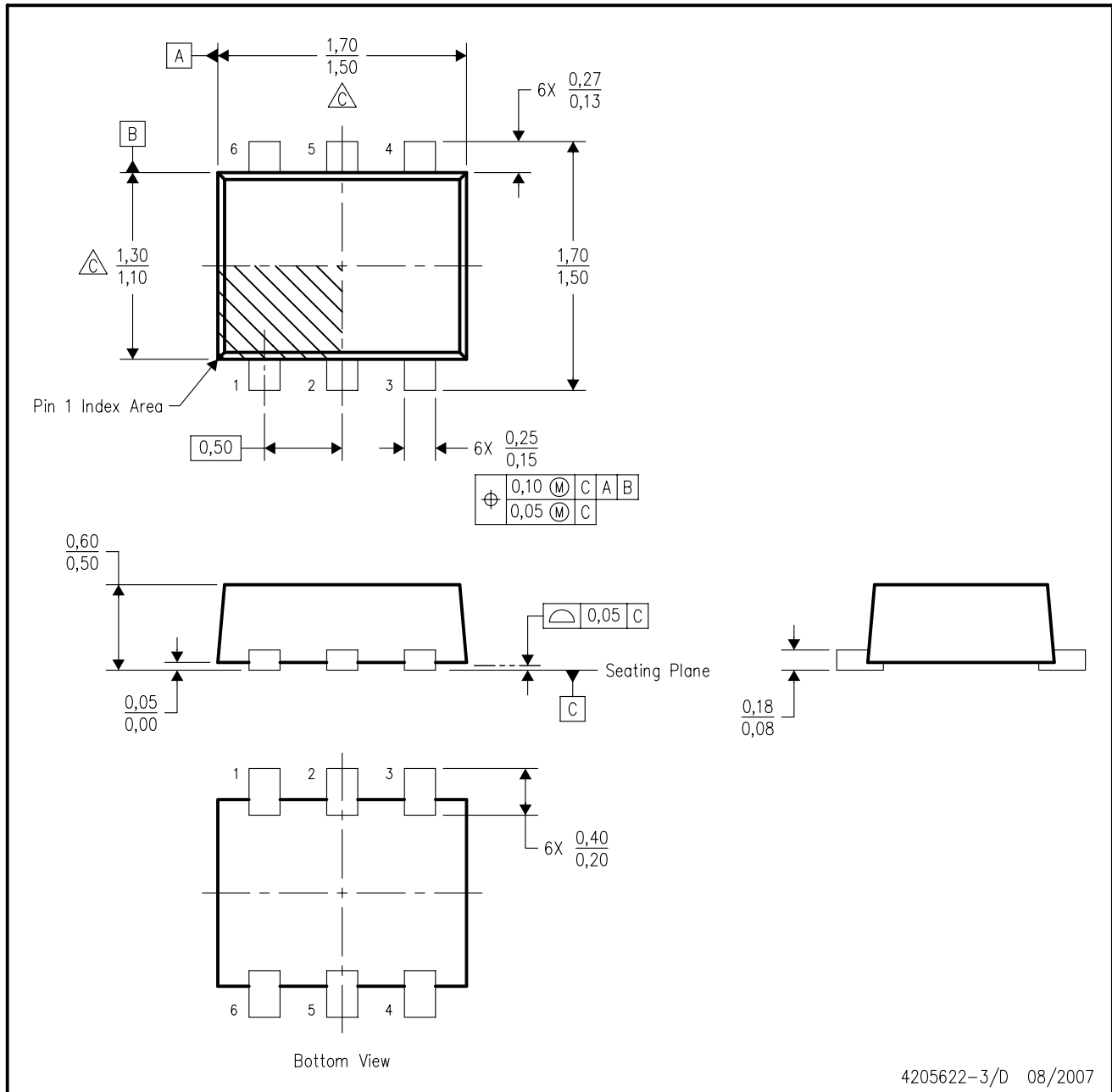
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRL (R-PDSO-N6)

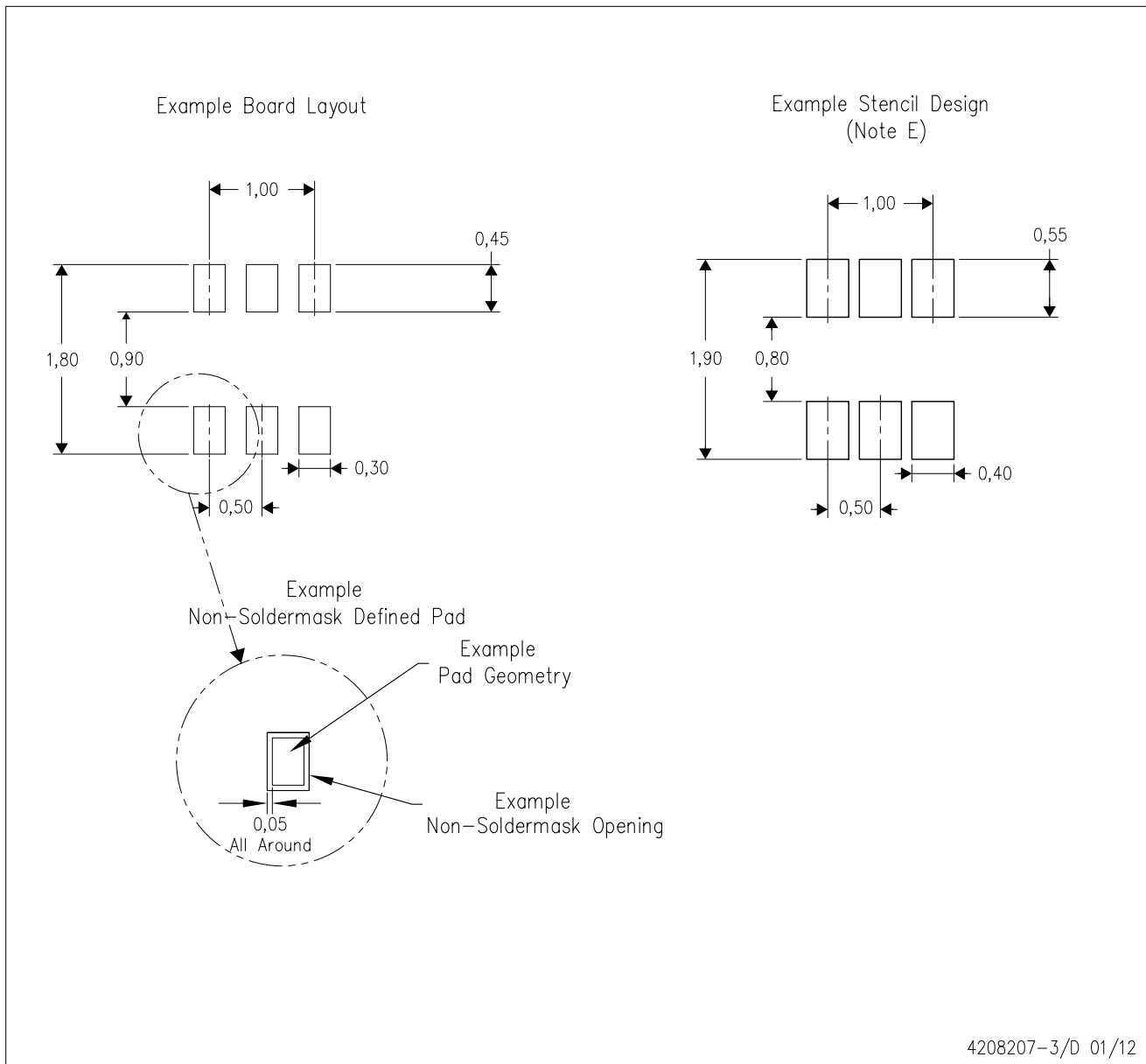
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

DRL (R-PDSO-N6)

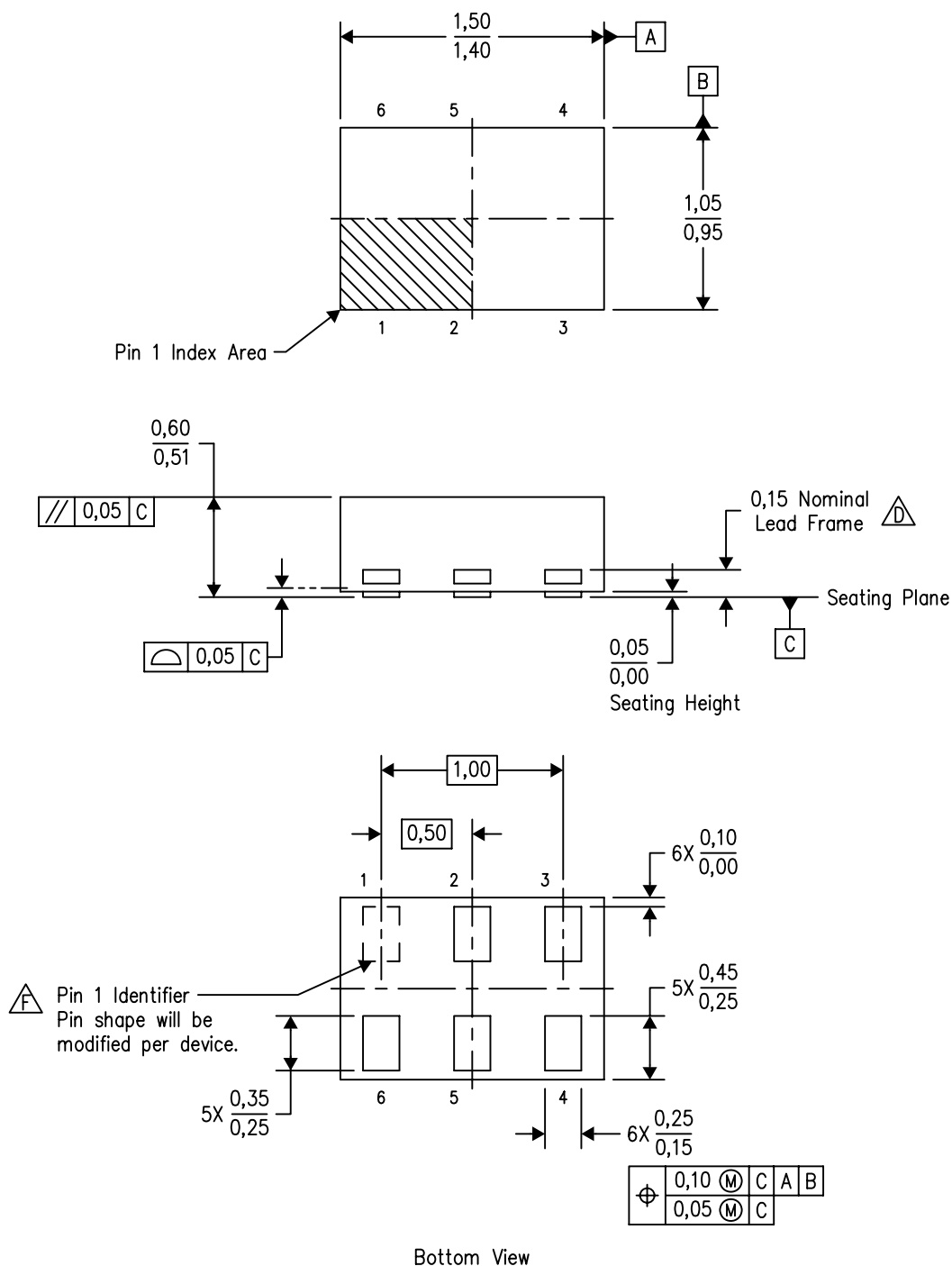
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

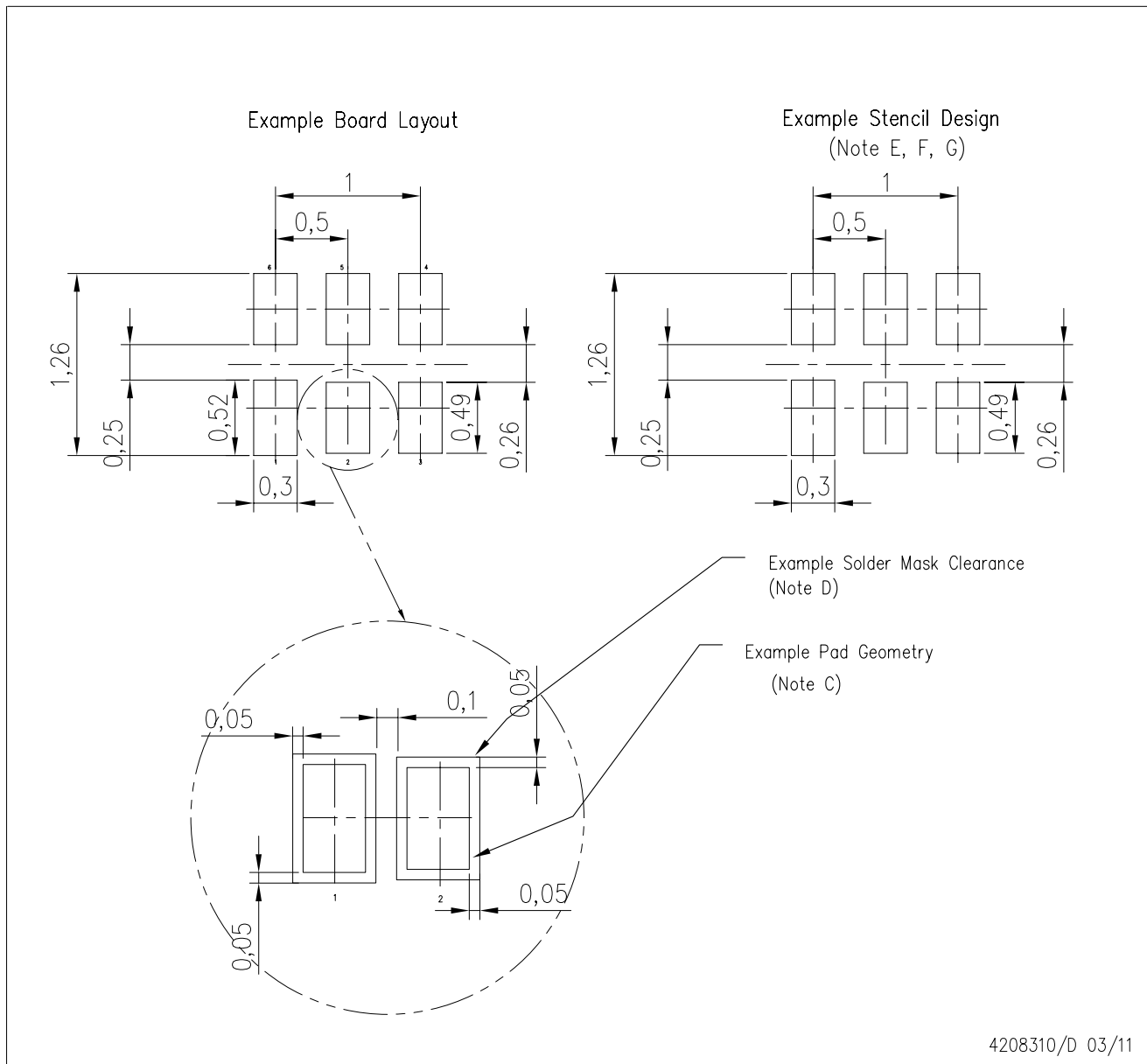


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - $\triangle D$ The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
 - E. This package complies to JEDEC MO-287 variation UFAD.
 - $\triangle F$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (S-PUSON-N6)

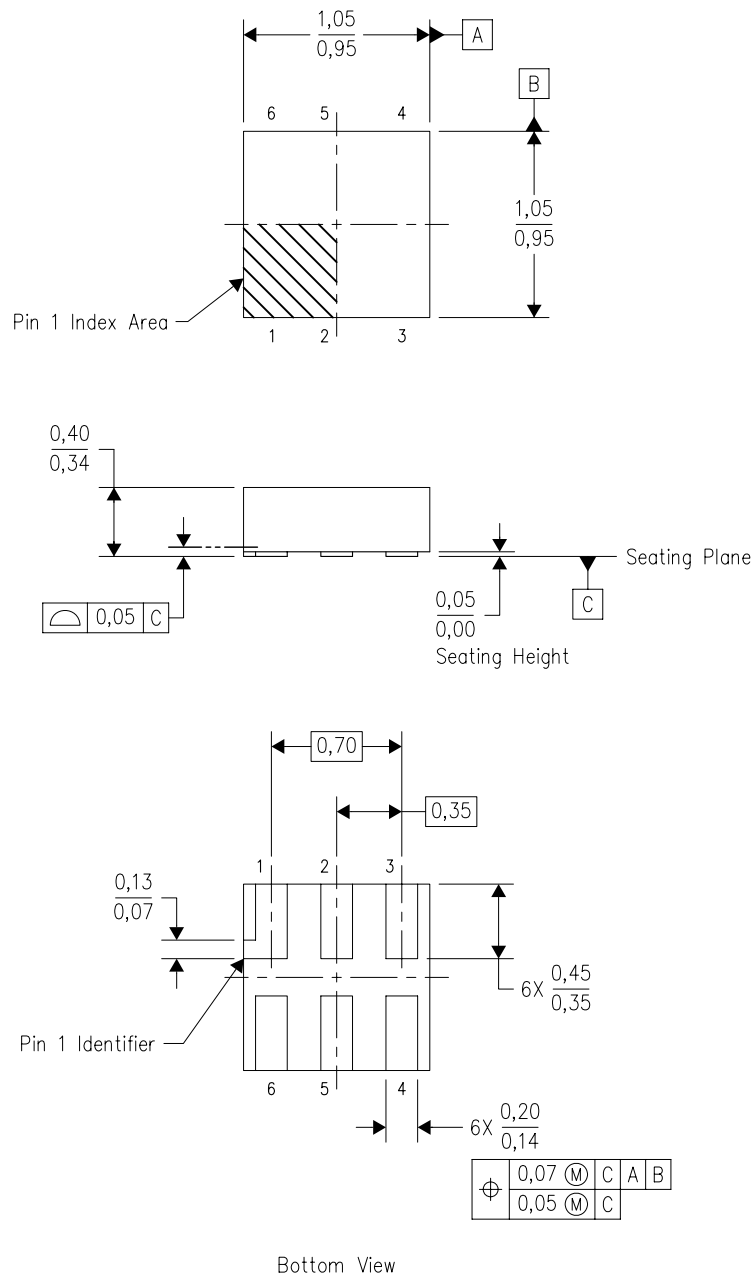
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

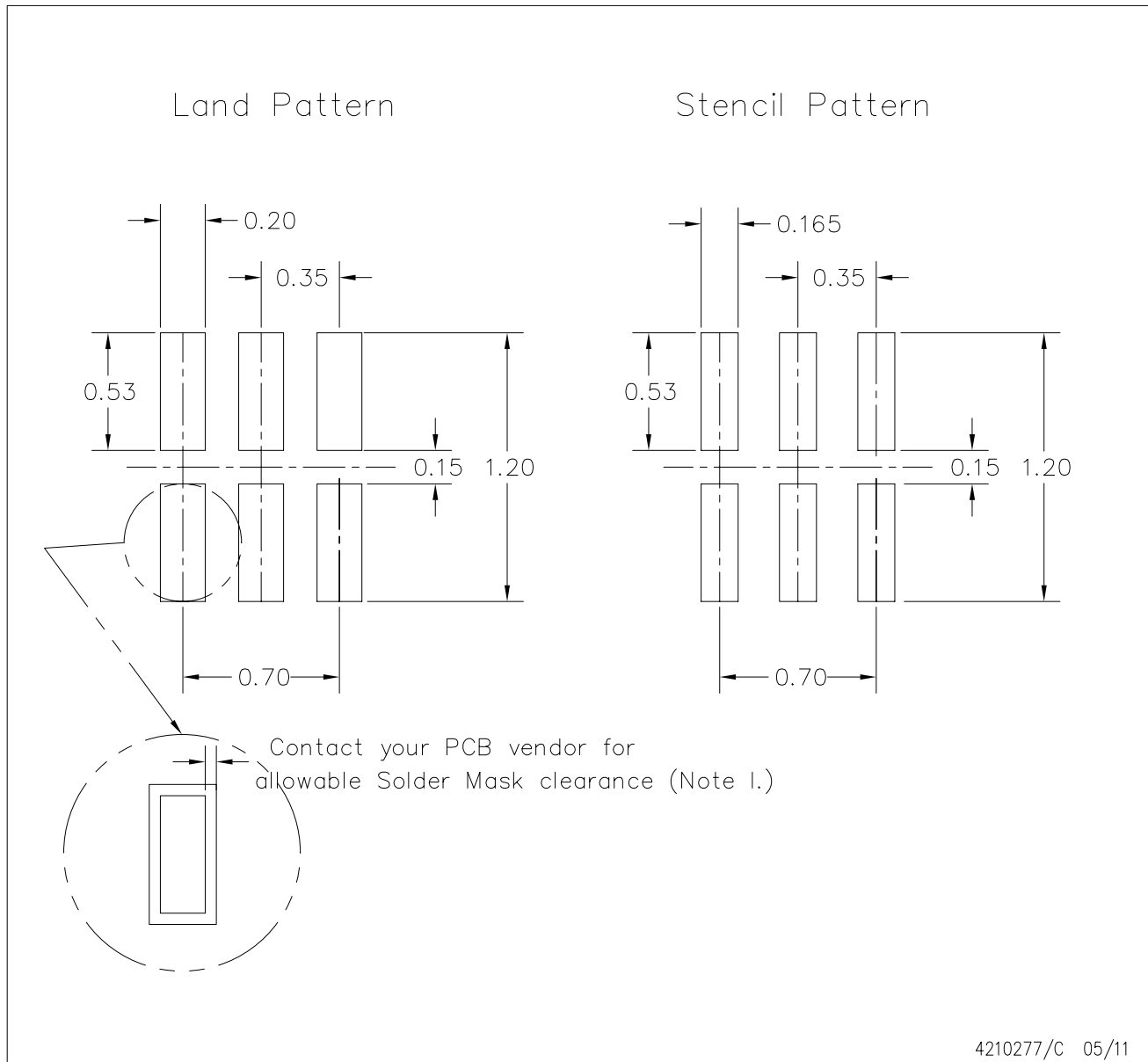


4208186/E 03/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - SON (Small Outline No-Lead) package configuration.
 - This package complies to JEDEC MO-287 variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

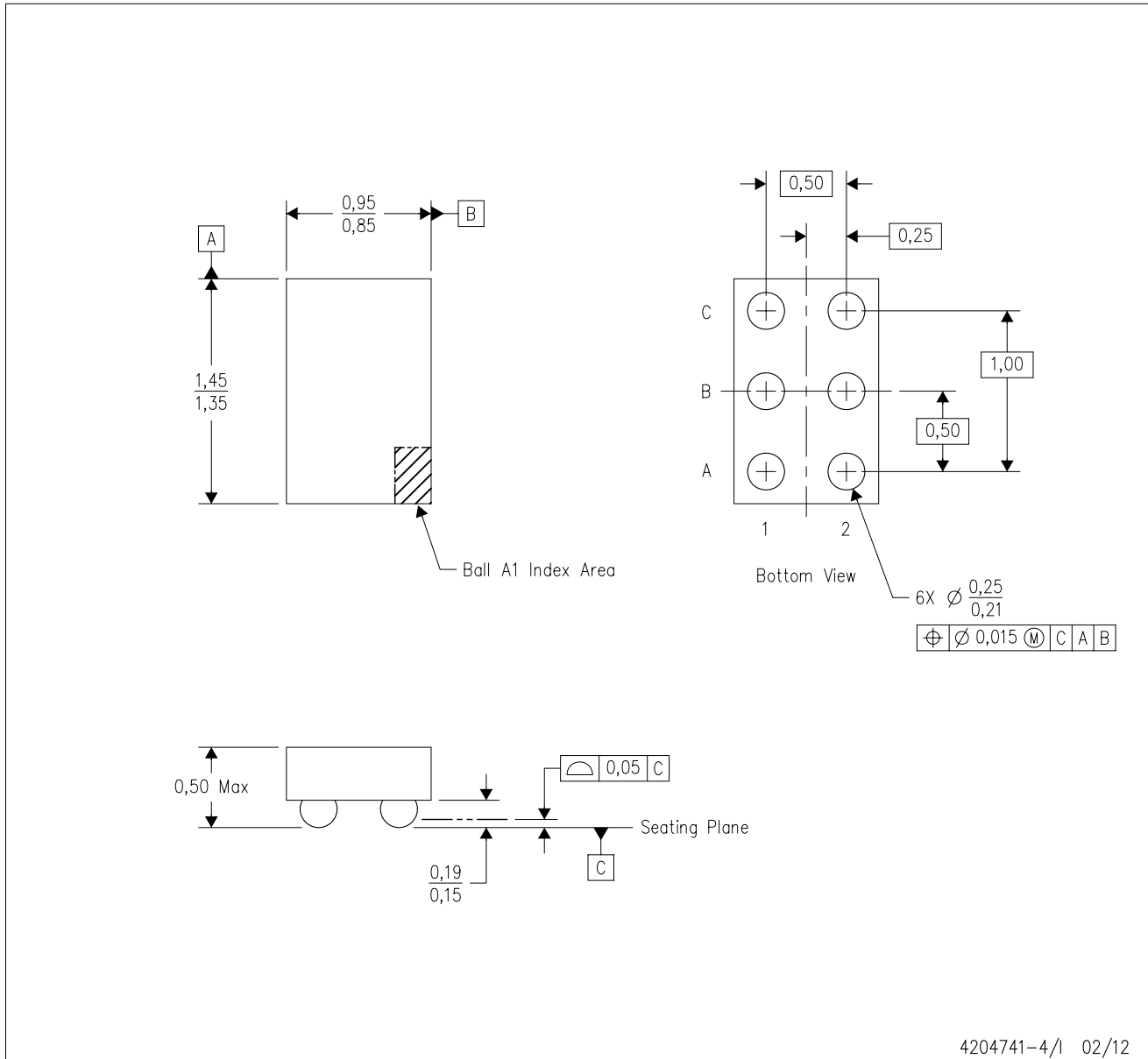


4210277/C 05/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
 - H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - I. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



4204741-4/1 02/12

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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