

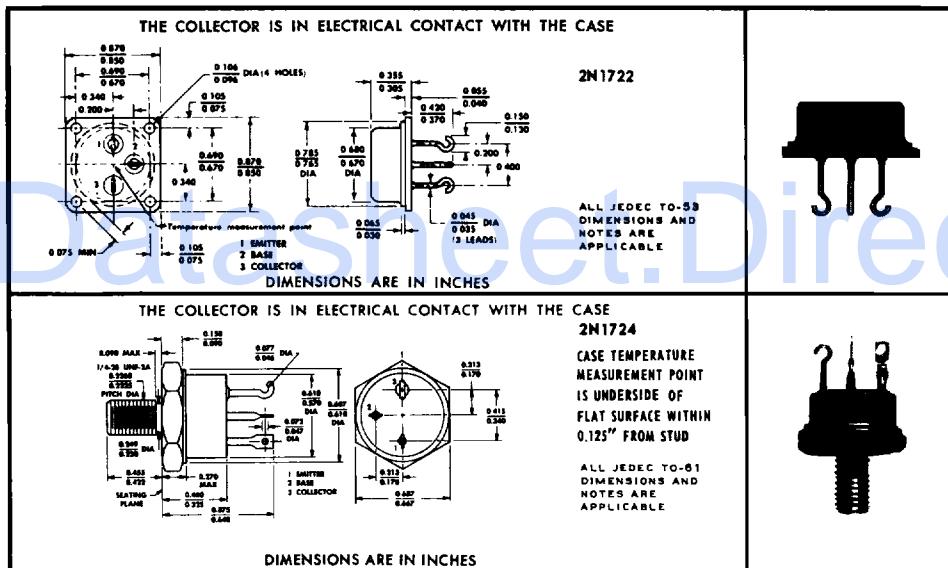
TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

HIGH-FREQUENCY POWER TRANSISTORS

- 50 Watts at 100°C Case Temperature
- Maximum R_{CS} of 0.5 Ohm at 2 Amperes I_C
- Minimum f_T of 10 Megacycles
- Maximum V_{BE} of 2 Volts at 2 Amperes I_C

mechanical data



absolute maximum ratings at 25°C ambient temperature (unless otherwise noted)

Collector-Emitter Voltage (See Note 1)	80	v
Emitter-Base Voltage	10	v
Collector Current, Continuous	5	a
Collector Current, Peak (See Note 2)	7.5	a
Total Device Dissipation at 100°C Case Temperature (See Note 3)	50	w
Total Device Dissipation at 25°C Ambient Temperature (See Note 4)	3	w
Collector Junction Operating Temperature	+ 175	°C
Storage Temperature Range	- 65°C to + 200°C	

Note 1 This is the voltage at which $|h_{FE}|$ approaches one when the emitter-base diode is open-circuited. Maximum allowable collector-emitter voltage shall be derated with increasing collector current as shown in the maximum V_{CE} curve which appears with the collector characteristics. Average power dissipation shall not exceed the maximum ratings for this device.

Note 2 Maximum peak collector current may be allowed if maximum junction temperature is not exceeded. See Figure 2, "Junction Temperature Response vs Pulse Width and Duty Cycle."

Note 3 Derate linearly to 175°C case temperature at the rate of 0.67 w/ $^{\circ}$ C.

Note 4 Derate linearly to 175°C ambient temperature at the rate of 20 mw/ $^{\circ}$ C.

Note 5 For correct measurement of I_{CES} , the base must be shorted to the emitter. The current meter must not be placed in the base-emitter short-circuit loop. I_{CES} may be used in place of I_{CEO} for circuit-stability calculations.

Note 6 For typical BV_{CER} at finite values of R_{BE} refer to BV_{CER} vs R_{BE} curve. Peak collector-emitter voltage of 120 v may be allowed in the cutoff-current region if the emitter-base diode is short-circuited.

Note 7 Heat-sinking sufficient to limit case temperature to 40°C or less over a 10-second measurement period must be used for this test.

Note 8 DC collector current should not be applied longer than 5 seconds to maintain case temperature less than 40°C without a heat sink.

Note 9 To obtain f_T , the $|h_{fe}|$ response with frequency is extrapolated at 6 db/octave to $|h_{fe}| = 1$ from $f = 10$ mc. The product of $f_T \times 1$ has been referred to as the gain-bandwidth product.

TYPES 2N1722, 2N1724
BULLETIN NO. DL-S-691315, APRIL 1961
REVISED DECEMBER 1969

TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

electrical characteristics at 25°C ambient temperature (unless otherwise noted)

Parameter	Test Conditions	Min	Max	Unit
I_{CES} Collector Reverse Current	$V_{CE} = 60\text{ v}, V_{BE} = 0$ (See note 5)		1	ma
I_{CES} Collector Reverse Current	$V_{CE} = 60\text{ v}, V_{BE} = 0,$ $T_C = +150^\circ\text{C}$ (See note 5)		2	ma
I_{CES} Collector Reverse Current	$V_{CE} = 120\text{ v}, V_{BE} = 0,$ $T_C = +150^\circ\text{C}$ (See note 5)		10	ma
I_{EBO} Emitter Reverse Current	$V_{EB} = 10\text{ v}, I_C = 0$		10	ma
* BV_{CEO} Collector-Emitter Breakdown Voltage	$I_C = 200\text{ ma}, I_B = 0$ (See notes 6 & 7)	80		v
* h_{FE} DC Forward Current Transfer Ratio	$V_{CE} = 15\text{ v}, I_C = 2\text{ a}$	20	90	
* h_{FE} DC Forward Current Transfer Ratio	$V_{CE} = 15\text{ v}, I_C = 2\text{ a},$ $T_A = -55^\circ\text{C}$	12		
* h_{FE} DC Forward Current Transfer Ratio	$V_{CE} = 15\text{ v}, I_C = 100\text{ ma}$	20		
* V_{BE} Base-Emitter Voltage	$I_B = 200\text{ ma}, I_C = 2\text{ a}$		2.0	v
* $V_{CE(sat)}$ Collector-Emitter Saturation Voltage	$I_B = 200\text{ ma}, I_C = 2\text{ a}$		1.0	v
h_{ie} AC Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 15\text{ v}, I_C = 500\text{ ma},$ $f = 10\text{ mc}$ (See note 8)	1.0		
C_{ob} Common-Base Output Capacitance	$V_{CE} = 15\text{ v}, I_E = 0, f = 1\text{ mc}$		550	pf

5

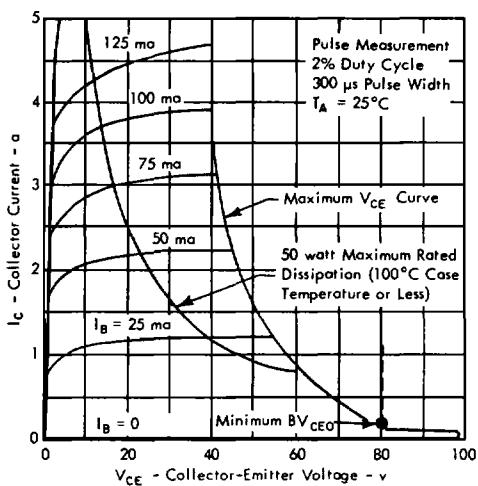
thermal characteristics

θ_{J-C}	Thermal Resistance, Junction to Case (Bottom, Center of Case)	1.5	C°/w
----------------	---	-----	---------------------------

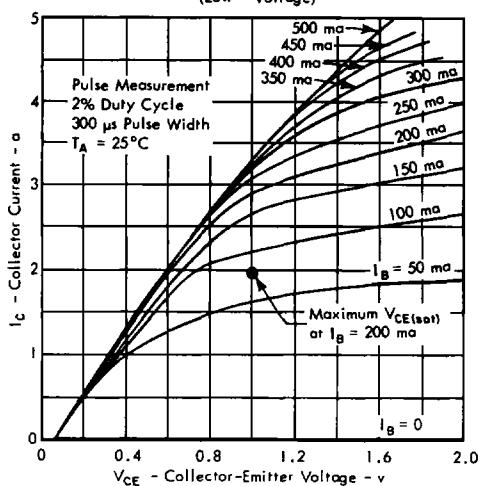
*Semi-automatic testing is facilitated by using pulse techniques to measure these parameters. A 300 μsec pulse (approximately 2% duty cycle) is utilized.

TYPICAL CHARACTERISTICS

COMMON-EMITTER COLLECTOR CHARACTERISTICS



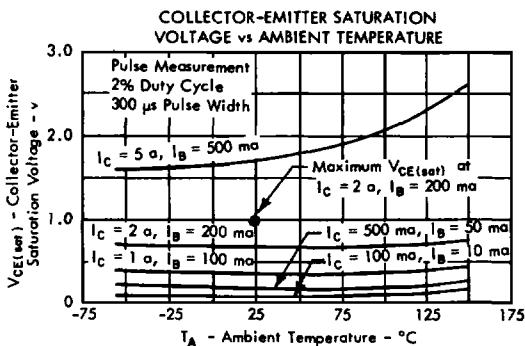
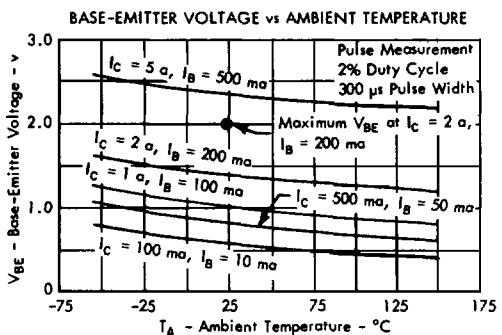
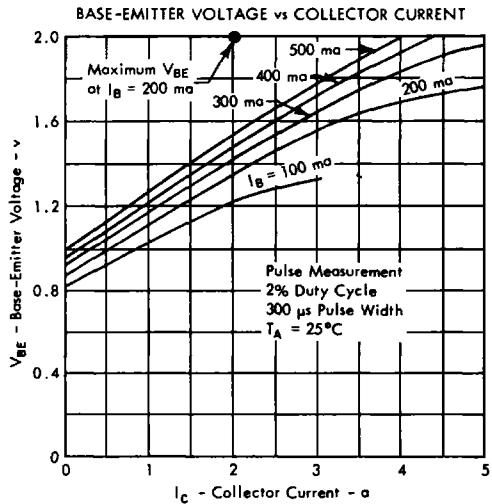
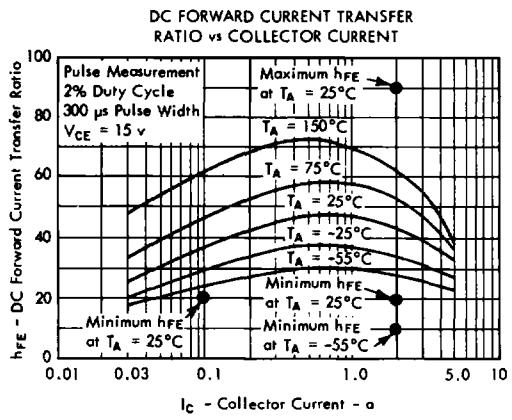
COMMON-EMITTER COLLECTOR CHARACTERISTICS
(Low - Voltage)



TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL CHARACTERISTICS

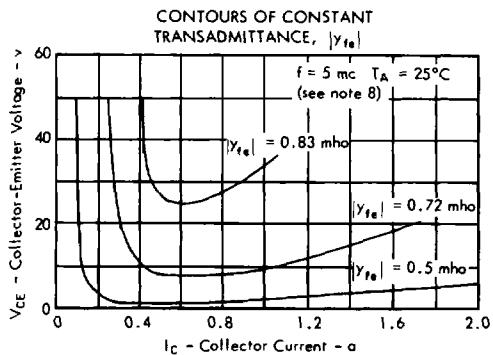
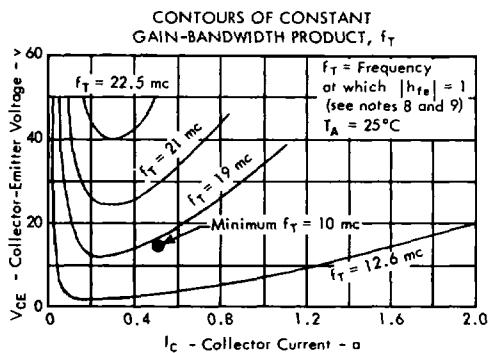
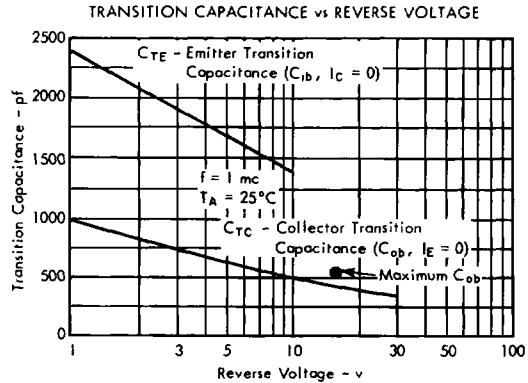
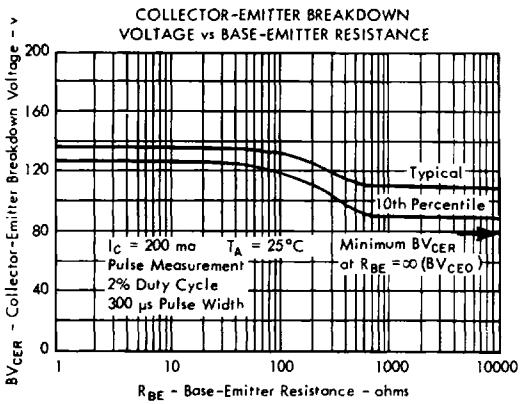


5

TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

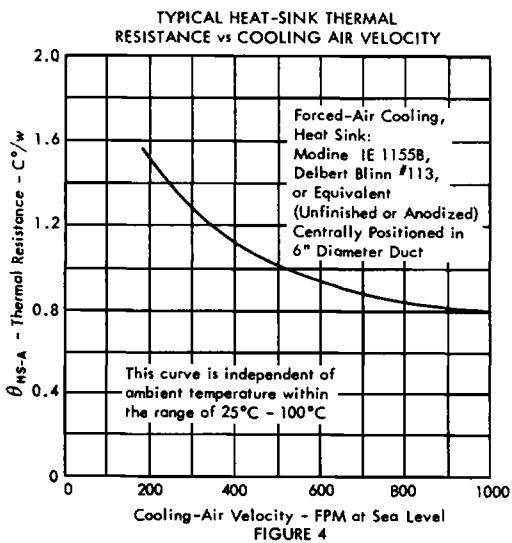
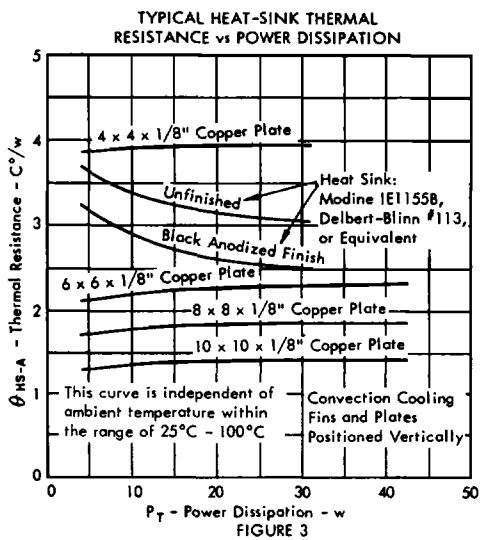
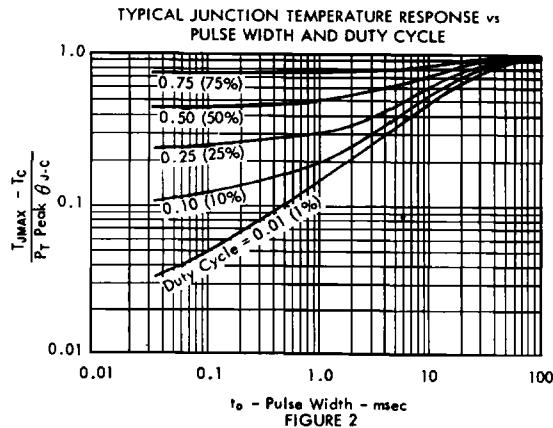
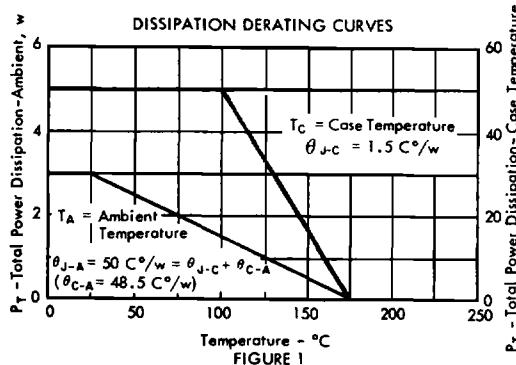
TYPICAL CHARACTERISTICS



TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

THERMAL INFORMATION



5

TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

Thermal Information

TABLE I

Mounting Conditions	2N1722 mounted with four 2-56 screws at 4 in-lb torque 2N1724 mounted at 30 in-lb. torque			
	Unfinished Alum. or Copper	Alum. or Copper with .0025" mica ins.	Anodized Aluminum	Anodized Alum. with DC-200 Oil
θ_{C-HS} — contact thermal resistance $^{\circ}\text{C}/\text{w}$	0.15	0.45	0.40	0.28

Symbol	Definition	Unit
P_T	DC or average total power dissipation	w
P_{Tpeak}	Peak total power dissipation (pulsed operation)	w
θ_{HS-A}	Heat-sink-to-ambient thermal resistance	$^{\circ}\text{C}/\text{w}$
θ_{C-HS}	Case-to-heat-sink (contact) thermal resistance	$^{\circ}\text{C}/\text{w}$
θ_{J-C}	Junction-to-case thermal resistance	$^{\circ}\text{C}/\text{w}$
θ_{J-A}	Junction-to-ambient thermal resistance (no heat sink)	$^{\circ}\text{C}/\text{w}$
θ_{C-A}	Case-to-ambient thermal resistance (no heat sink)	$^{\circ}\text{C}/\text{w}$
T_A	Ambient temperature	$^{\circ}\text{C}$
T_{HS}	Heat-sink mounting surface temperature	$^{\circ}\text{C}$
T_C	Case temperature (transistor mounting surface)	$^{\circ}\text{C}$
T_{Jmax}	Maximum junction temperature	$^{\circ}\text{C}$
t_o	Pulse width	msec

For steady-state power dissipation or pulsed dissipation with $t_o < 100 \mu\text{sec}$, maximum junction temperature may be considered equal to the ambient temperature plus the product of average power dissipation and total junction-to-ambient thermal resistance. Under these pulse conditions, the junction-to-case temperature gradient varies so slightly with instantaneous power dissipation that average dissipation may be used in thermal calculations. When a heat sink is used, junction-to-ambient thermal resistance may be broken down into three quantities: θ_{J-C} , θ_{C-HS} , and θ_{HS-A} . Thermal performance can then be calculated using the following equation:

$$T_{Jmax} = T_A + P_T(\theta_{J-C} + \theta_{C-HS} + \theta_{HS-A})$$

Or, if no heat sink is used,

$$T_{Jmax} = T_A + P_T \theta_{J-A}$$

θ_{J-C} , θ_{J-A} , and θ_{C-A} are shown in Figure 1. To minimize contact thermal resistance, θ_{C-HS} , the heat sink mounting surface should be as smooth as possible. θ_{C-HS} for several surface and mounting conditions is given in Table I. These figures represent maximum values encountered on surfaces equivalent to those of most commercially available heat sinks. Note that in some cases, as with the anodized aluminum finish, θ_{C-HS} can be reduced substantially by the application of a film of silicone grease between transistor and heat sink.

As t_o exceeds 100 μsec during pulsed operation, the instantaneous variation of the junction-to-case temperature gradient increases sharply. Therefore, maximum rather than average junction temperature must be considered. Figure 2 shows the ratio of maximum instantaneous case-to-junction temperature rise at any pulse width and duty cycle to the rise which would occur at 100% duty cycle. Use of this curve is best explained by the equations below and by the example problems. Provided the other operating conditions are known, T_{Jmax} or P_{Tpeak} may be found using the relation

$$T_{Jmax} = T_A + P_{Tpeak} \times \text{duty cycle} \times (\theta_{C-HS} + \theta_{HS-A}) + \left[\frac{T_{Jmax} - T_C}{P_{Tpeak} \theta_{J-C}} \right] P_{Tpeak} \theta_{J-C}$$

Or, if no heat sink is used,

$$T_{Jmax} = T_A + P_{Tpeak} \times \text{duty cycle} \times \theta_{C-A} + \left[\frac{T_{Jmax} - T_C}{P_{Tpeak} \theta_{J-C}} \right] P_{Tpeak} \theta_{J-C}$$

Note that the ambient-to-transistor case temperature rise remains constant at a value proportional to average power dissipation throughout the pulse width and duty cycle range shown in Figure 2. Values for θ_{HS-A} taken from Figures 3 and 4 are used in the example problems. However, the curves in Figures 1 and 2 may be used for any heat sink provided its thermal resistance is known. Under no circumstances should peak power dissipation exceed the value indicated by the maximum V_{CE} curve on the collector characteristics.

Example 1. Find T_{Jmax}

Operating Conditions

Heat sink = Modine 1E1155B, Delbert Blinn 113, or equivalent, anodized finish, convection cooling

$t_o = 1 \mu\text{sec}$

duty cycle = 0.10 (10%)

$P_{Tpeak} = 50 \text{ w}$

$T_A = 50^{\circ}\text{C}$

$$T_{Jmax} = T_A + P_{Tpeak} \times \text{duty cycle} \times (\theta_{CHS} + \theta_{HS-A}) + \left[\frac{T_{Jmax} - T_C}{P_{Tpeak} \theta_{J-C}} \right] P_{Tpeak} \theta_{J-C}$$

From Figure 1, $\theta_{J-C} = 15^{\circ}\text{C}/\text{w}$

From Figure 1, $\theta_{HS-A} = 3.15^{\circ}\text{C}/\text{w}$ ($P_T = P_{Tpeak} \times \text{duty cycle}$)

From Table I, $\theta_{CHS} = 0.40^{\circ}\text{C}/\text{w}$

$$\text{From Figure 2, } \left[\frac{T_{Jmax} - T_C}{P_{Tpeak} \theta_{J-C}} \right] = 0.20$$

then

$$T_{Jmax} = 50^{\circ}\text{C} + 50 \text{ w} \times 0.10 \times (3.15 + 0.40)^{\circ}\text{C}/\text{w} + 0.20 \times 50 \text{ w} \times 1.5^{\circ}\text{C}/\text{w}$$

$$= 50 + 17.7 + 15$$

$$= 82.7^{\circ}\text{C}$$

Example 2. Find P_{Tpeak}

Operating Conditions

heat sink = none

$t_o = 10 \mu\text{sec}$

duty cycle = 0.01 (1%)

T_{Jmax} (design limit) = 175°C

$T_A = 25^{\circ}\text{C}$

$$T_{Jmax} = T_A + P_{Tpeak} \times \text{duty cycle} \times \theta_{C-A} + \left[\frac{T_{Jmax} - T_C}{P_{Tpeak} \theta_{J-C}} \right] P_{Tpeak} \theta_{J-C}$$

From Figure 1, $\theta_{C-A} = 48.5^{\circ}\text{C}/\text{w}$

From Figure 1, $\theta_{J-C} = 1.5^{\circ}\text{C}/\text{w}$

$$\text{From Figure 2, } \left[\frac{T_{Jmax} - T_C}{P_{Tpeak} \theta_{J-C}} \right] = 0.50$$

then

$$175^{\circ}\text{C} = 25^{\circ}\text{C} + P_{Tpeak} \times 0.01 \times 48.5^{\circ}\text{C}/\text{w} + 0.50 \times P_{Tpeak} \times 1.5^{\circ}\text{C}/\text{w}$$

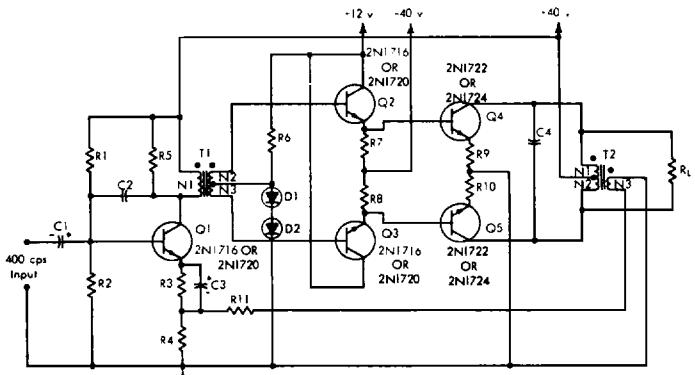
$$P_{Tpeak} = \frac{150}{0.485 + 0.75} \equiv 121 \text{ watts}$$

TYPES 2N1722, 2N1724

N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL APPLICATION DATA, $T_A = -55^\circ\text{C}$ TO 125°C

35 watt, 400 cps SERVO AMPLIFIER



R_L - 68, 35 w
 R1 - 4.32 K, 1/2 w
 R2 - 3.32 K, 1/2 w
 R3 - 1.00 K, 1 w
 R4 - 33.2, 1/2 w

R5 - 2.21 K, 1/2 w
 R6 - 390, 1/2 w
 R7 & R8 - 2.00 K, 1 w
 R9 & R10 - 1.00, 2 w
 R11 - 1.00 K, 1/2 w

C1 - 40 μF , 25 v
 C2 - 500 μF , 100 v
 C3 - 1000 μF , 25 v
 C4 - 2.0 μF , 100 v
 D1 & D2 - TI 1N538
 Q1, Q2, & Q3 - TI 2N1716
 OR TI 2N1720
 Q4 & Q5 - TI 2N1722
 OR TI 2N1724

Circuit Characteristics at 35 w Power Output:

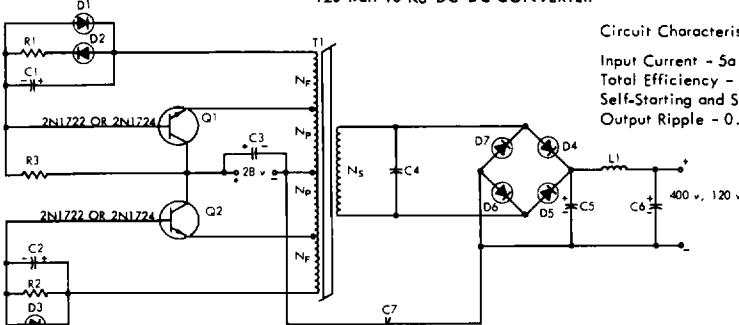
- Power Gain - 45 db min.
- Voltage Amplification - 36.5 ± 1.5 db
- Circuit Input Resistance - 700 Ω min.
- Total Harmonic Distortion - 5%

T1: N1 = 755 T, #30 AWG; N2 = N3 = 330 T, #28 AWG Bifilar Wound.
 Core - Magnetic Metals 75EI SL14 or equivalent - 1 x 1 interleaved.
T2: N1 = N2 = 100 T, #20 AWG Bifilar Wound; N3 = 67 T, #28 AWG.
 Core - Magnetic Metals 100 EI SL14 or equivalent - Butt Joint.

- NOTES:**
- All Resistance Values in ohms - 5% Tolerance
 - Resistor Wattage Ratings at 125°C Ambient
 - Capacitor Voltage Ratings at 125°C Ambient
 - Q1 on Heat Sink with $\theta_{C-HS} + \theta_{HS-A} \leq 40^\circ\text{C}/\text{w}$
 - Q2 and Q3 on same Heat Sink. $\theta_{C-HS} + \theta_{HS-A} \leq 40^\circ\text{C}/\text{w}$ each. h_{FE} 's matched within 10%.
 - Q4 and Q5 on Heat Sinks with $\theta_{C-HS} + \theta_{HS-A} \leq 1.5^\circ\text{C}/\text{w}$. h_{FE} 's matched within 10%.

5

120 watt 10 Kc DC-DC CONVERTER



Q1 & Q2 - TI 2N1722
 OR TI 2N1724
 D1 - D3 - TI 1N645
 D4 - D7 - TI 1N1096
 C1 & C2 - 22 μF , 15 v
 C3 - 100 μF , 35 v
 C4 - 510 μF , 500 v

C5 - 0.1 μF , 500 v
 C6 - 3 μF , 500 v
 C7 - 0.01 μF , 500 v

T1: Np = 18 T #16 AWG
 Ns = 290 T #25 AWG
 Nf = 3 T #22 AWG
 Core: Toroid, Magnetic Metals Inc. 51026-ID or equivalent.

- NOTES:**
- All Resistance Values in ohms, 5% Tolerance.
 - All Resistor Wattage Ratings at 125°C Ambient.
 - Capacitor Voltage Ratings at 125°C Ambient.
 - Q1 and Q2 on Same Heat Sink, $\theta_{C-HS} + \theta_{HS-A} \leq 4^\circ\text{C}/\text{w}$ each.

TYPES 2N1722, 2N1724 N-P-N TRIPLE-DIFFUSED MESA SILICON TRANSISTORS

TYPICAL APPLICATION DATA, $T_A = -55^\circ\text{C}$ TO 125°C

30-volt, 0 – 2.5-a VOLTAGE REGULATOR

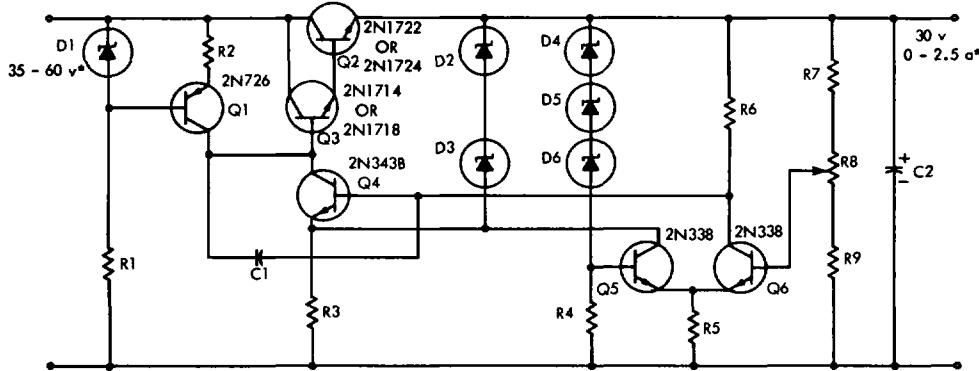
Circuit Characteristics:

$$\frac{\Delta V_{\text{OUT}}}{\Delta I_{\text{OUT}}} \Big|_{\Delta V_{\text{IN}} = 0} = \text{Output Resistance} \leq 0.007 \text{ ohm}$$

$$100X \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \Big|_{\Delta I_{\text{OUT}} = 0} = \text{Input Regulation} \leq 0.05\% \text{ at } I_{\text{OUT}} = 2.0 \text{ a}$$

$$100X \frac{\Delta V_{\text{OUT}} / V_{\text{OUT}}}{\Delta T_A} \Big|_{\Delta V_{\text{IN}} = 0} = \text{Output Voltage Temperature Coefficient} \leq 0.007\% / ^\circ\text{C} \text{ at } I_{\text{OUT}} = 2.0 \text{ a}, V_{\text{IN}} = 45 \text{ v}$$

$$\frac{\text{Input Ripple}}{\text{Output Ripple}} = \text{Ripple Reduction} \geq 10,000$$



Q1 - TI 2N726

Q2 - TI 2N1722 OR

TI 2N1724

Q3 - TI 2N1714 OR

TI 2N1718

Q4 - TI 2N343B

Q5 & Q6 - TI 2N338

TI 2N746

D2 & D3 - TI 1N751

D4 - D6 - TI 1N752A

C1 - 0.01 μF , 50 v

C2 - 100 μF , 50 v

R1 - 5.11 K, 1/2 w

R2 - 681, 1/4 w

R3 - 2.00 K, 1/4 w

R4 - 2.43 K, 1/4 w (Wirewound)

R5 - 35.7 K, 1/4 w

R6 - 35.7 K, 1/4 w

R7 & R9 - 3.57 K, 1/4 w (Wirewound)

R8 - 200, 1/4 w (Wirewound)

NOTES: 1. All Resistor Values in ohms, 5% Tolerance.

2. Resistor Wattage Ratings at 125°C Ambient.

3. Capacitor Voltage Ratings at 125°C Ambient.

4. Q2 and Q3 on Same Heat Sink: $Q2: \theta_{c-HS} + \theta_{HS-A} \leq 22^\circ\text{C}/\text{w}$

$Q3: \theta_{c-HS} + \theta_{HS-A} \leq 22^\circ\text{C}/\text{w}$

5. Q5 and Q6 on Same Heat Sink: Each, $\theta_{c-HS} + \theta_{HS-A} \leq 80^\circ\text{C}/\text{w}$

*See Voltage - Current Derating Curves Below

MAXIMUM ALLOWABLE INPUT VOLTAGE vs OUTPUT CURRENT - 0-2.5 a VOLTAGE REGULATOR

