

IRFP450, IRFP451, IRFP452, IRFP453

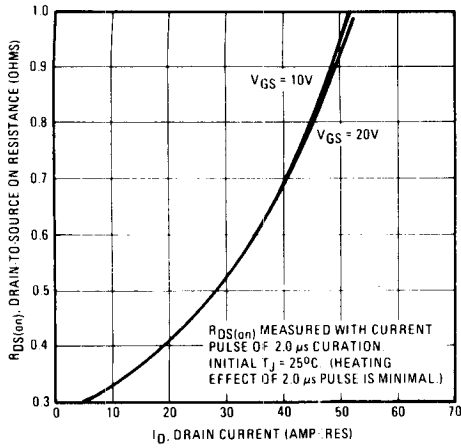


Fig. 12 – Typical On-Resistance Vs. Drain Current

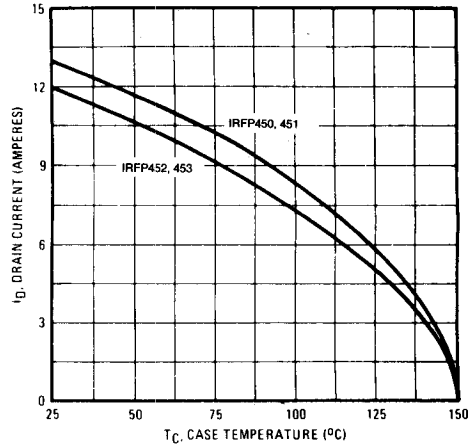


Fig. 13 – Maximum Drain Current Vs. Case Temperature

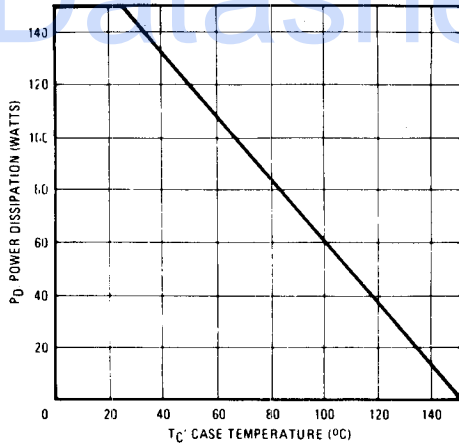


Fig. 14 – Power Vs. Temperature Derating Curve

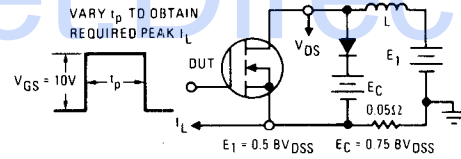


Fig. 15 – Clamped Inductive Test Circuit

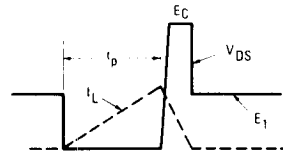


Fig. 16 – Clamped Inductive Waveforms

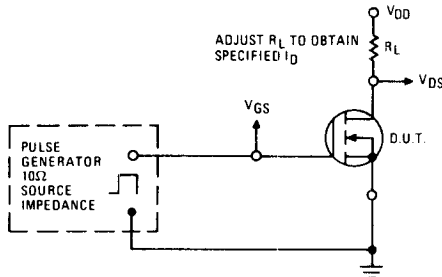


Fig. 17 – Switching Time Test Circuit

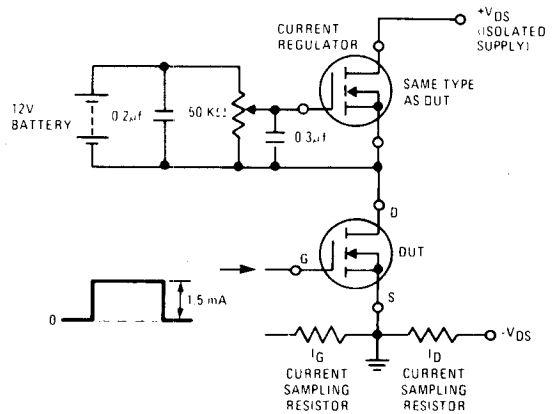


Fig. 18 – Gate Charge Test Circuit

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A and 13 A, 450 V – 500 V

$r_{DS(on)}$ = 0.4 Ω and 0.5 Ω

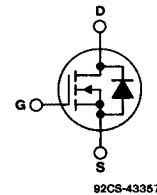
Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRFP450, IRFP451, IRFP452, and IRFP453 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

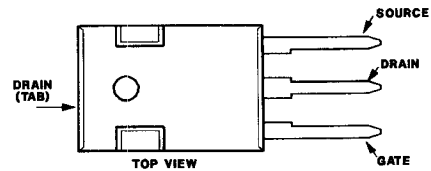
The IRFP-types are supplied in the JEDEC TO-247 plastic package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



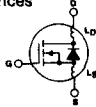
JEDEC TO-247

Absolute Maximum Ratings

Parameter	IRFP450	IRFP451	IRFP452	IRFP453	Units
V_{DS} Drain - Source Voltage ①	500	450	500	450	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ K}\Omega$) ①	500	450	500	450	V
$I_D @ T_c = 25^\circ\text{C}$ Continuous Drain Current	13	13	12	12	A
$I_D @ T_c = 100^\circ\text{C}$ Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM} Pulsed Drain Current ③	52	52	48	48	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_c = 25^\circ\text{C}$ Max. Power Dissipation	150 (See Fig. 14)				W
Linear Derating Factor	1.2 (See Fig. 14)				W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped ④	52	52	48	48	A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

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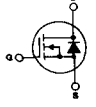
Electrical Characteristics @ T_c = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain - Source Breakdown Voltage	IRFP450 IRFP452	500	—	—	V	V _{GS} = 0V I _D = 250μA	
	IRFP451 IRFP453	450	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V	
I _{D(on)} On-State Drain Current ②	IRFP450 IRFP451	13	—	—	A	V _{DS} > I _{D(on)} × R _{DSON} max., V _{GS} = 10V	
	IRFP452 IRFP453	12	—	—	A		
R _{DSON} Static Drain-Source On-State Resistance ②	IRFP450 IRFP451	—	0.3	0.4	Ω	V _{GS} = 10V, I _D = 7.0A	
	IRFP452 IRFP453	—	0.4	0.5	Ω		
g _{fs} Forward Transconductance ②	ALL	6.0	11	—	S(V)	V _{DS} > I _{D(on)} × R _{DSON} max., I _D = 7.0A	
C _{iss} Input Capacitance	ALL	—	2000	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz	
C _{oss} Output Capacitance	ALL	—	400	—	pF	See Fig. 10	
C _{rss} Reverse Transfer Capacitance	ALL	—	100	—	pF		
t _{don} Turn-On Delay Time	ALL	—	—	35	ns	V _{DD} = 210V, I _D = 7.0A, Z ₀ = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	—	50	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	—	150	ns		
t _f Fall Time	ALL	—	—	70	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	82	140	nC	V _{GS} = 10V, I _D = 16A, V _{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	40	60	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	42	63	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances 
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	0.83	°C/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRFP450 IRFP451	—	—	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	IRFP452 IRFP453	—	—	12	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRFP450 IRFP451	—	—	52	A	
	IRFP452 IRFP453	—	—	48	A	
V _{SD} Diode Forward Voltage ②	IRFP450 IRFP451	—	—	1.4	V	T _c = 25°C, I _S = 13A, V _{GS} = 0V
	IRFP452 IRFP453	—	—	1.3	V	T _c = 25°C, I _S = 12A, V _{GS} = 0V
t _{rr} Reverse Recovery Time	ALL	—	1300	—	ns	T _J = 150°C, I _F = 13A, dI _F /dt = 100A/μs
Q _{RR} Reverse Recovered Charge	ALL	—	7.4	—	μC	T _J = 150°C, I _F = 13A, dI _F /dt = 100A/μs
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ L = 100 μH (See Fig. 15)

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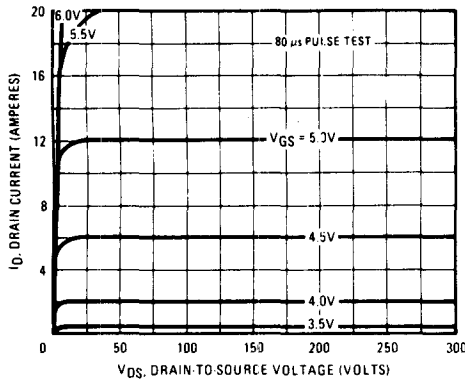


Fig. 1 - Typical Output Characteristics

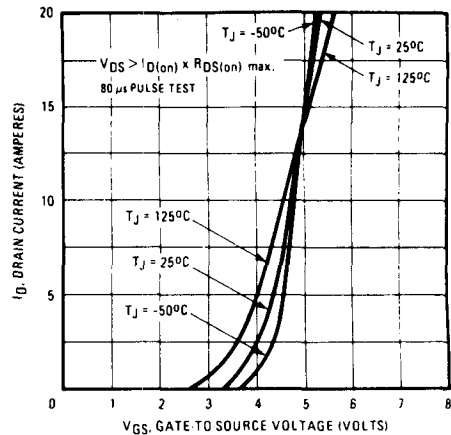


Fig. 2 - Typical Transfer Characteristics

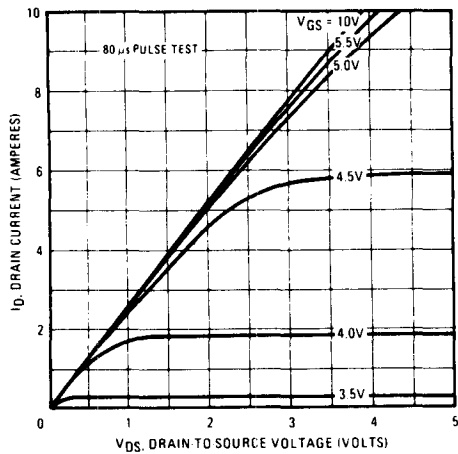


Fig. 3 - Typical Saturation Characteristics

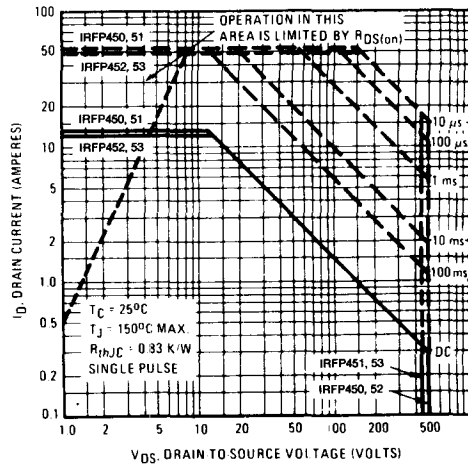


Fig. 4 - Maximum Safe Operating Area

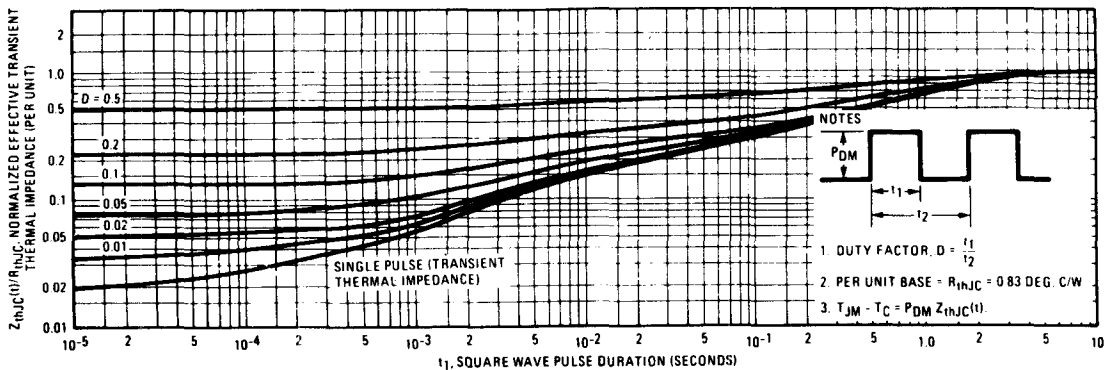


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRFP450, IRFP451, IRFP452, IRFP453

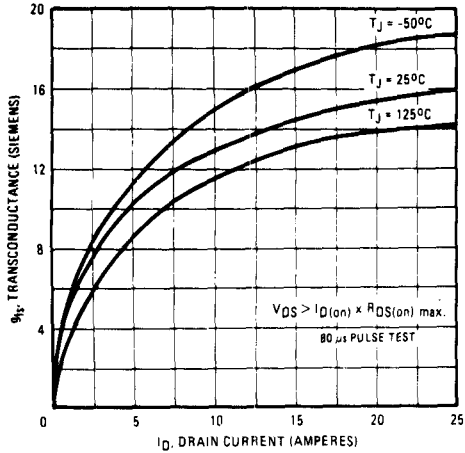


Fig. 6 - Typical Transconductance Vs. Drain Current

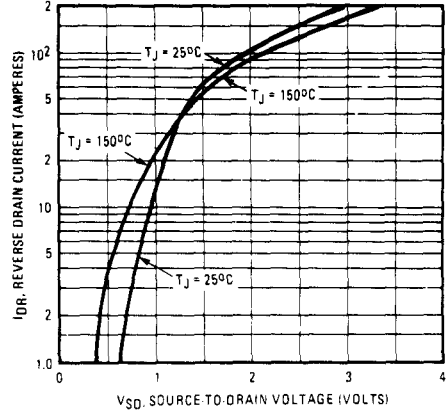


Fig. 7 - Typical Source-Drain Diode Forward Voltage

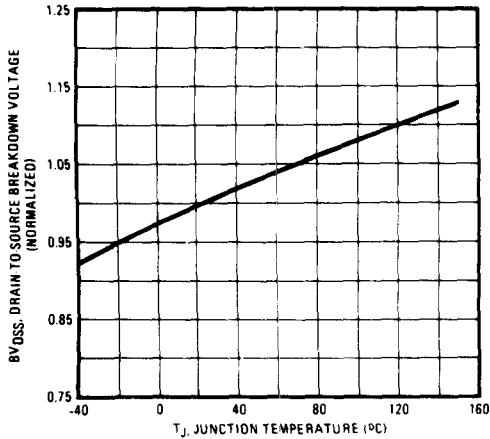


Fig. 8 - Breakdown Voltage Vs. Temperature

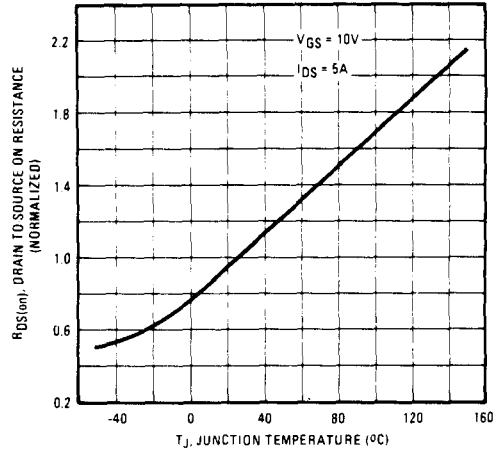


Fig. 9 - Normalized On-Resistance Vs. Temperature

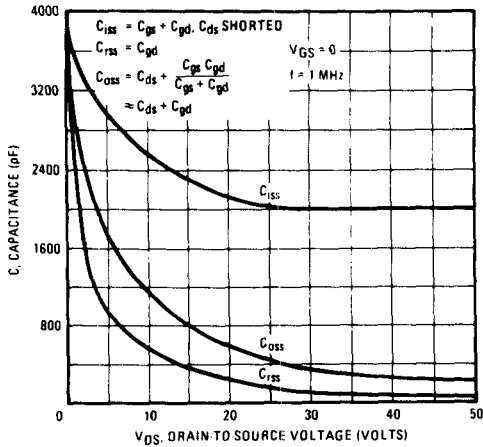


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

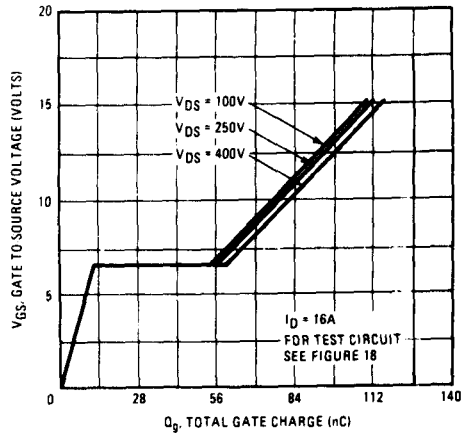


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage