

Evaluating the **SSM3582** 2×, 31.76 W, Digital Input, Filterless Stereo Class-D Audio Amplifier

FEATURES

2×, 31.76 W into 4 Ω at 16 V, THD + N = 10%

EVALUATION KIT CONTENTS

USBi USB interface board

USB cable

EVAL-SSM3582Z evaluation board

ONLINE RESOURCES

Documents

[SSM3582 data sheet](#)

[EVAL-SSM3582Z user guide](#)

Dynamic link library (DLL) for the [SigmaStudio](#) software

GENERAL DESCRIPTION

The **EVAL-SSM3582Z** is the evaluation board for the **SSM3582**, an integrated stereo, 31.76 W, high efficiency, Class-D, audio amplifier with digital input. The application circuit requires few external components and can operate from a single 4.5 V to 16 V supply. The **EVAL-SSM3582Z** is capable of delivering 14.67 W of continuous output power to a 4 Ω load from a 12 V power supply, with <1% THD + N, or 31.76 W into a 4 Ω load from 16 V, 10% THD + N.

The **SSM3582** features a high efficiency, low noise modulation scheme that requires no external reconstruction filter (LC) output filters. This scheme provides high efficiency, even at low output power.

The **EVAL-SSM3582Z** and the **SSM3582** operate with 93.8% efficiency at 10 W into an 8 Ω load or 90.6% efficiency at 18 W into 4 Ω load from a 12 V supply. The **EVAL-SSM3582Z** and the **SSM3582** have a typical noise floor of 38.5 μV rms A weighted.

This user guide describes how to configure and use the **SSM3582** evaluation board. Read this user guide in conjunction with the **SSM3582** data sheet, which provides specifications, internal block diagrams, a register map, and application guidance for the amplifier.

Figure 1 shows the top view of the evaluation board, and Figure 2 shows the bottom view of the evaluation board.

EVALUATION BOARD PHOTOGRAPHS

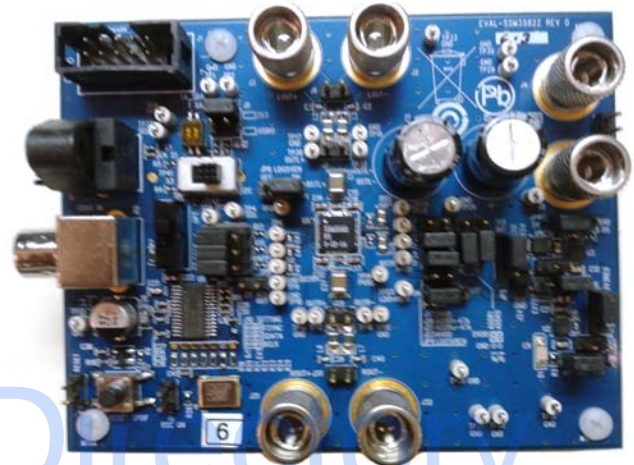


Figure 1. **SSM3582** Evaluation Board, Top View

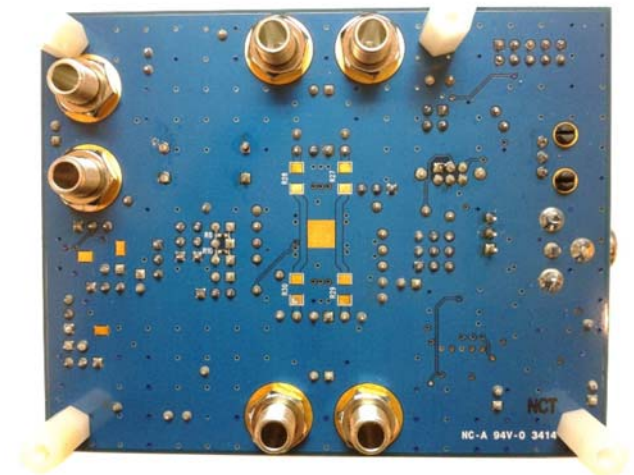


Figure 2. **SSM3582** Evaluation Board, Bottom View

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REVISION HISTORY

4/16—Revision 0: Initial Version

SETTING UP THE HARDWARE

INPUT CONFIGURATION

There are several ways to source audio to the [SSM3582](#) on the evaluation board. The evaluation board can accept direct digital I²S/time division multiplex (TDM) data or it can convert SPDIF/optical digital audio data to I²S data using an on-board digital audio receiver (U6).

Use the 3-way × 3-way header, J10, to connect either the on-board SPDIF audio receiver circuitry or the external digital audio signals to the [SSM3582](#) device pins. The evaluation board comes set with three jumpers for receiving the SPDIF audio data.

To use the external I²S/TDM data, remove the three jumpers on the J10 header and connect the signal sources (FSYNC, BCLK, and SDATA) to the center pins on the J10 header.

If the user does not have a direct I²S or TDM source, the on-board digital audio receiver can accept SPDIF data from a digital audio source, such as the digital audio output of a compact disk player. In this case, select either the optical or coaxial option using the S2 switch to properly connect the desired input to the digital audio receiver.

I²C MODE

The [SSM3582](#) supports I²C control for setting the internal registers. In this mode, Switch S3 must be set to the I²C mode. The 10-way header, J1, connects the external I²C master controlling the board. The board can be set for the desired I²C address using four headers: J18, J21, JP3, and JP4. The JP3 and JP4 headers set the pull-up or pull-down resistors to DVDD or GND, whereas the J18 and J21 headers can bypass either the R8 or R10 47 k Ω resistor. Refer to the data sheet for address selection options. Removing the jumper across Header J18 or Header J21 inserts either the R8 or R10 47 k Ω resistor in the signal path for pull-up or pull-down operation. To properly float the ADDR_x pins to a no connect state, do not insert jumpers on the JP3, JP4, J18, and J21 headers. By default, the J18 and J21 headers are inserted and the JP3 and JP4 headers are pulled to GND. This sets the 7-bit device address to 0x10.

STANDALONE MODE

The [SSM3582](#) also supports standalone (SA) mode operation. In this mode, Switch S3 must be set to SA mode. In SA mode, the ADDR_x, SCL, and SDA pins configure the functionality of the [SSM3582](#), including the I²S/TDM configuration and sample rate. Refer to the [SSM3582](#) data sheet for a complete list of options. In SA mode, the duty cycle of FSYNC dictates whether the device is in I²S or TDM mode. If the duty cycle is 50%, use I²S; otherwise, use TDM.

The following is an example of the settings that select a 32 kHz to 48 kHz sample rate, utilizing TDM Slot 1 and Slot 2 or the left and right channels of an I²S stream, depending on the FSYNC duty cycle:

- Set Switch S1 so that SCL and SDA are pulled to GND.

- Set Header JP4 to GND and insert Header J21, leaving Header JP3 and Header J18 open.
- Set Switch S3 to SA mode.

OUTPUT CONFIGURATION

The binding post output terminals, OUTL⁻, OUTL⁺, OUTF⁻, OUTF⁺, provide the option to connect the speakers with standard banana connectors. The OUTL \pm terminals are for the left channel and the OUTF \pm terminals are for the right channel. In addition, the 2-pin, 0.100 inch headers, J6 and J30, are provided as alternate options.

To reduce the system radiated emission, especially if the speaker cable length exceeds 20 cm, it may be necessary to include an output filter. The recommended filter uses L2, L3, L6, and L7 ferrite beads and the C1, C2, C39, and C40 capacitors. Refer to Figure 6 for more details.

Note that the addition of ferrite beads other than the type used on the evaluation board may affect the total harmonic distortion (THD) and signal-to-noise ratio (SNR) performance as specified in the [SSM3582](#) data sheet. For best performance, the Murata ferrite bead type in Table 1 and Table 2 is recommended.

POWER SUPPLY CONFIGURATION

The J5 (PVDD) and J4 (GND) binding posts provide the power supply to the board. Take care when connecting the dc power with correct polarity and voltage; reverse polarity or overvoltage can damage the board permanently. Permissible supply voltages range from 4.5 V to 16 V; higher voltages may damage the amplifier. In addition, use the appropriate current rated power supply to the board. Typically, a 5 A rating supply is recommended if using 4 Ω speakers and 12 V.

The board has an option to generate 5 V (AVDD), 3.3 V, and 1.8 V (DVDD) supply voltages from the PVDD supply. These voltages are generated using the linear regulators on the board: U3 for 5 V, U2 for 3.3 V, and U4 for 1.8 V. The 5 V and 3.3 V regulators can be turned off using Header JP11 for 5 V and Header JP10 for 3.3 V. The 3.3 V supply is used for the on-board SPDIF digital audio receiver. The 5 V and 1.8 V supplies can provide AVDD and DVDD to the [SSM3582](#) if required. By default, the evaluation board is set up for generating 5 V and 1.8 V supplies from the [SSM3582](#) internal regulators by removing the jumpers from the J17 and J23 headers.

The JP8 and JP9 headers enable or disable the [SSM3582](#) internal regulators. By default, these regulators are enabled. If using the on-board regulators or the external 5 V or 1.8 V sources for the AVDD and DVDD pins, Jumper JP8 and Jumper JP9 must be fitted to the GND position and the J17 and J23 headers must be inserted.

EDGE MODE

To reduce the radiated emissions from the SSM3582 amplifier, an edge rate control mode is available. Register 0x05, Bit 3, controls the edge rate of the switching. This low electromagnetic interference (EMI) mode is enabled by default. To disable the low EMI mode, set Bit 3 of Register 0x05 to 0. To return to the low EMI mode, set Bit 3 of Register 0x05 to 1.

MONO OPERATION

The board is configured for stereo operation by default, but can be changed to mono operation.

For mono operation, the R27 through R30 resistors must be fitted with 0 Ω or use 16 AWG wires to short the OUTL+ terminal to the OUTF+ pin, and, similarly, to short the OUTL- terminal to the OUTF- pin. Note that the device must be configured to mono operation by setting the MONO bit (Bit 4, Register 0x04) to 0 before turning on the power stage.

Set this bit by writing Register 0x04 with the hexadecimal value, 0xB1. This ensures the power stage turns on in mono operation.

COMPONENT SELECTION

Selecting the proper capacitors and ferrites for the evaluation board is key to achieving the performance required at the cost budgeted.

Output Shunting Capacitors

There are four output filter capacitors, C1, C2, C39, and C40, that work with the L2, L3, L6, and L7 ferrite beads. Use small size (0603 or 0402), multilayer, ceramic capacitors of dielectric type X7R or COG (NPO) materials. The recommended value of the capacitors is 220 pF.

Output Ferrites

If ferrite beads are preferred for EMI filtering at the output nodes, Table 1 shows the recommended components to avoid excessive noise induced by the nonlinear behavior of ferrite beads.

Table 1. Recommended Output Ferrite Beads¹

| Part No. | Manufacturer | Z (Ω at 100 MHz) | I _{MAX} (mA) | DC Resistance (DCR) (Ω) | Size (mm) |
|----------------|--------------------------|------------------|-----------------------|-------------------------|-----------------|
| NFZ2MSM101SN10 | Murata Manufacturing Co. | 100 | 4000 | 0.014 | 2.0 × 1.6 × 0.9 |
| NFZ2MSM181SN10 | Murata Manufacturing Co. | 180 | 3400 | 0.020 | 2.0 × 1.6 × 0.9 |
| NFZ2MSM301SN10 | Murata Manufacturing Co. | 300 | 3100 | 0.024 | 2.0 × 1.6 × 0.9 |

¹ Contact Murata Manufacturing Co. for further options.

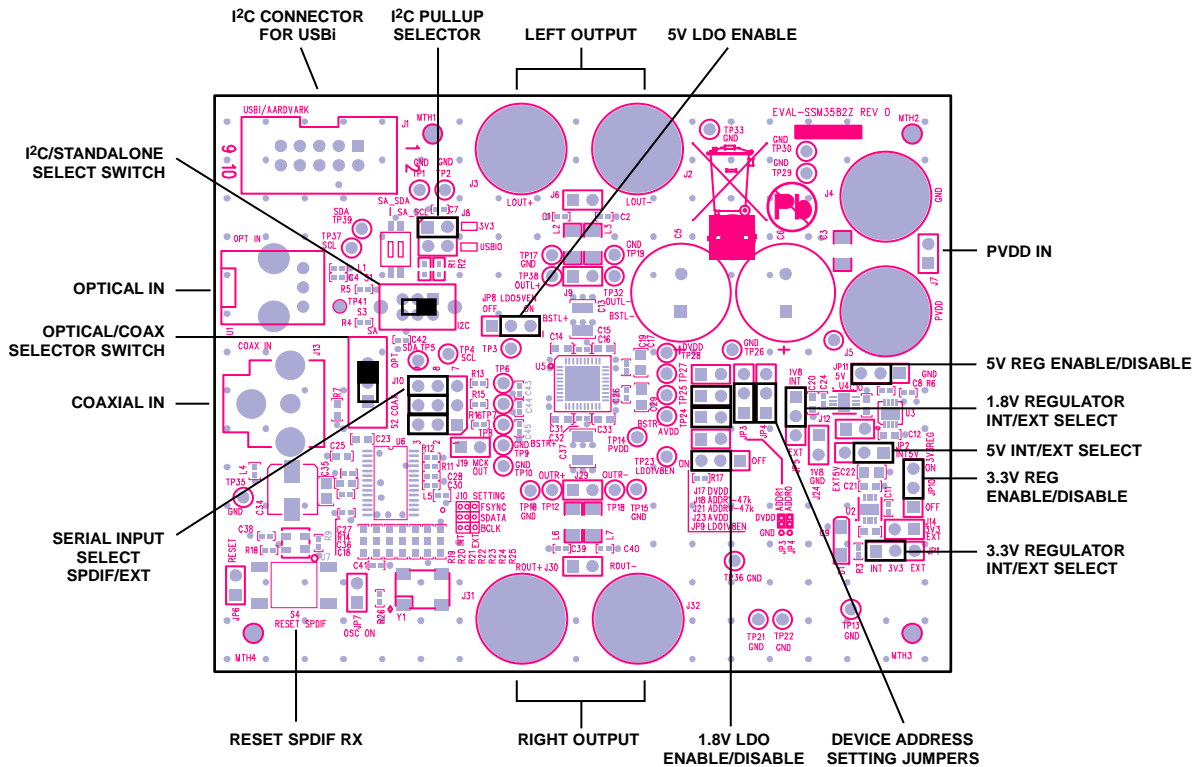


Figure 3. Board Settings

14262-003

GETTING STARTED

To set up the **SSM3582** to work in a simple, single-supply configuration for quick evaluation, follow these steps:

1. Download the **SigmaStudio™** software and follow the installation steps provided.
2. Connect the USBi board to the USB port on the PC and ensure the USB driver for the USBi board is installed.
3. Copy the provided **SigmaStudio** software file to the **C:\Program files\Analog Devices** folder.
4. After the **SigmaStudio** software is installed, the **SigmaStudio** icon on the desktop appears. Double-click the icon. This opens up the **SigmaStudio** graphical user interface.
5. Start a new project by dragging the **USBi** and **SSM3582** icons to the **Hardware Configuration** tab.
6. Connect the USBi board to the **SSM3582** block on the **Hardware Configuration** tab schematic (see Figure 4).

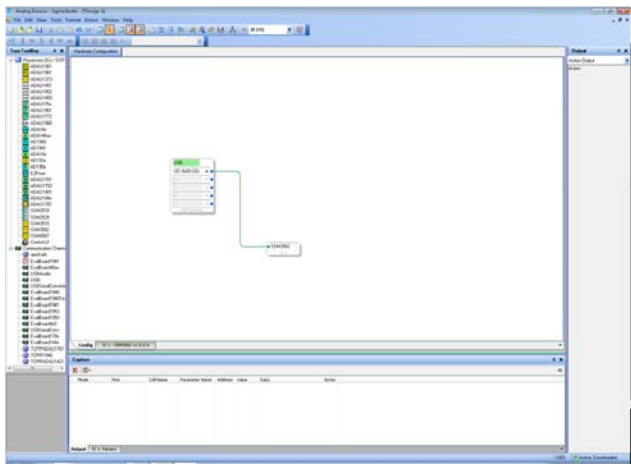


Figure 4. USBi to SSM3582 Configuration

7. Connect the 12 V power supply source to the evaluation board.
8. Connect the USBi board to Header J1 on the evaluation board.
9. Select the digital audio source for the SDATA, FSYNC, and BCLK pins of the **SSM3582**. By default, the board is set for the SPDIF source. Connect the optical or coaxial cable to the appropriate connector on the board.

10. Ensure the jumpers are inserted across all three rows of Header JP10 to establish direct connection of the digital audio signal lines to the inputs of the **SSM3582**.
11. Connect speakers to the left and right binding posts.
12. If using the on-board SPDIF to I²S circuitry, press the S4 button on the board to synchronize the audio signals by resetting the digital audio receiver device.
13. Click the **IC-SSM3582** tab. When clicking the **GetID** button, the 3582 with die revision numbers appears in the **Capture** window (see Figure 4).

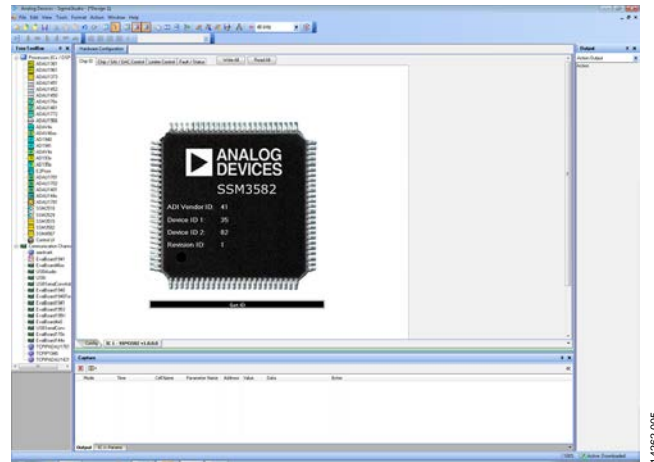


Figure 5. SSM3582 Device Setup

14. Click to the **Chip/SAI/DAC Control** tab.
15. Click the **Software Master Powered** button. It then turns green and the **SSM3582** powers up with audio on the output.

SUGGESTED SYSTEM LEVEL AND AUDIO TESTS

It is recommended to test the following specifications:

- SNR.
- Output noise. Ensure that an A weighted filter filters the output before reading the measurement meter.
- Maximum output power.
- Distortion.
- Efficiency.

EVALUATION BOARD SCHEMATICS AND ARTWORK

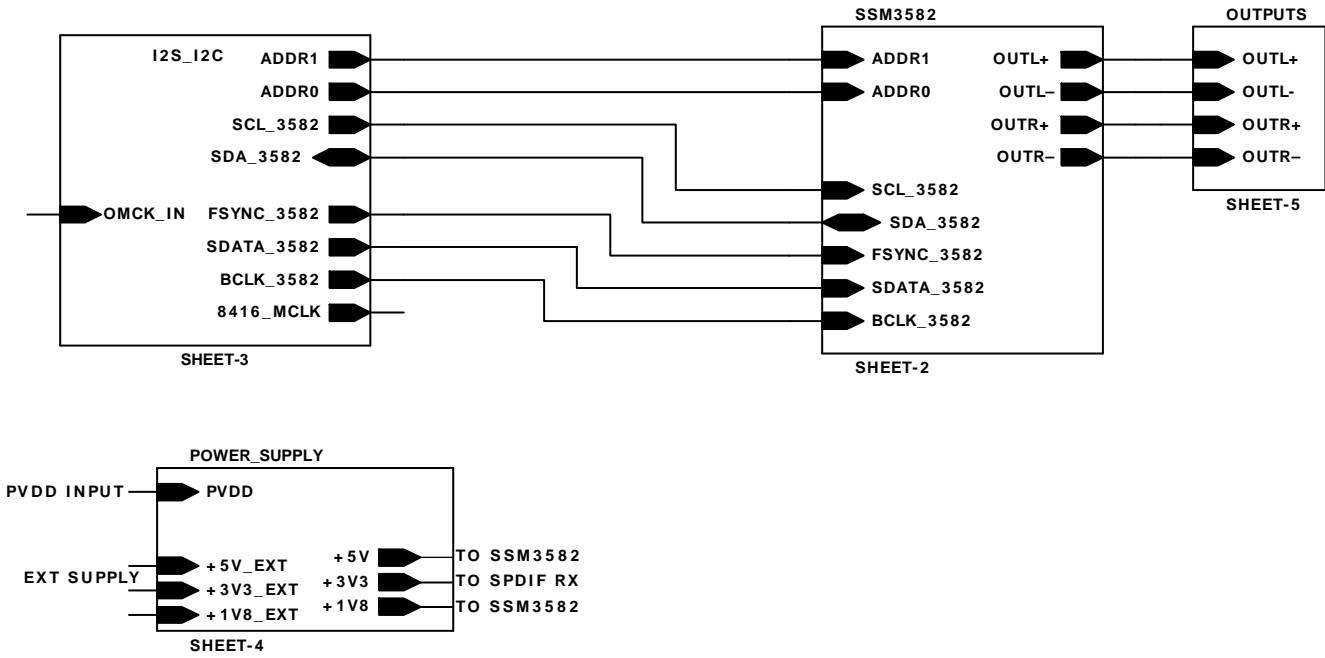


Figure 6. Schematic of the SSM3582 Evaluation Board Block Diagram

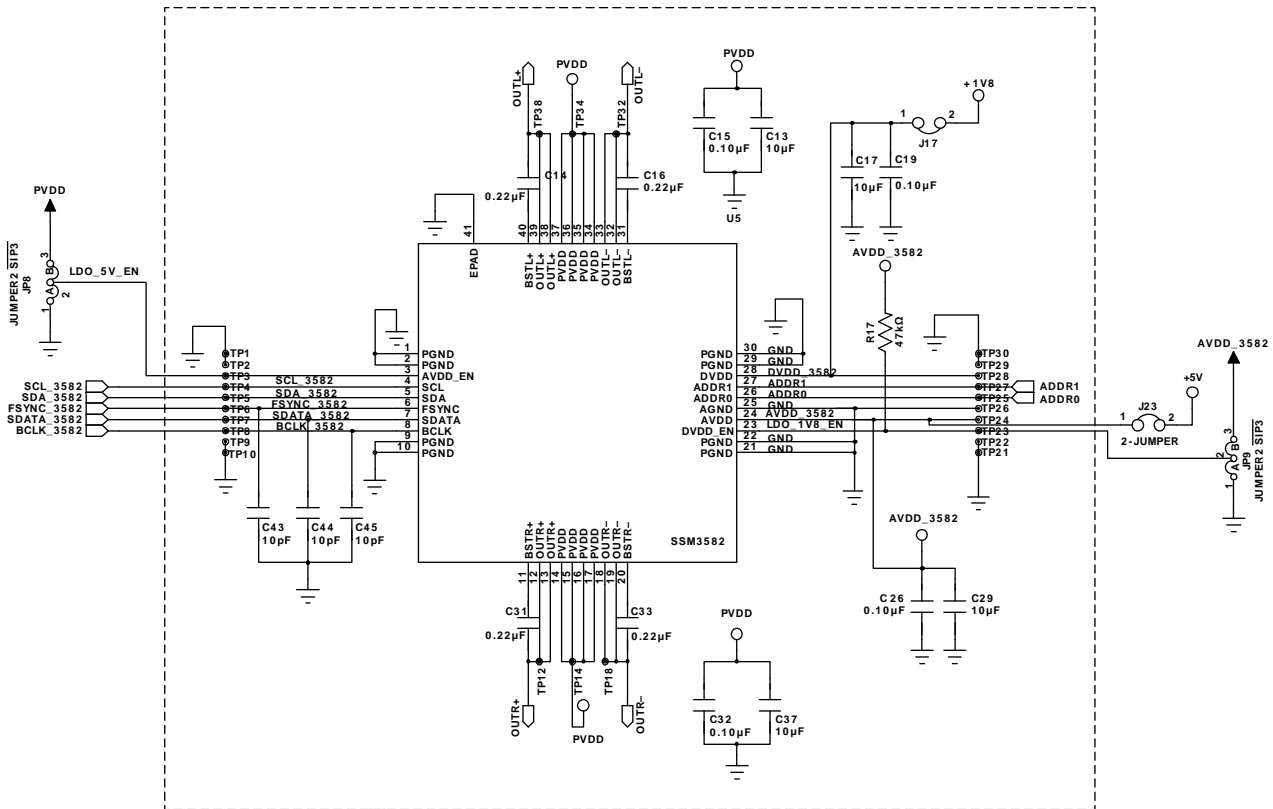


Figure 7. Schematic of the SSM3582 Evaluation Board, SSM3582 Section

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14282-007

14262-008

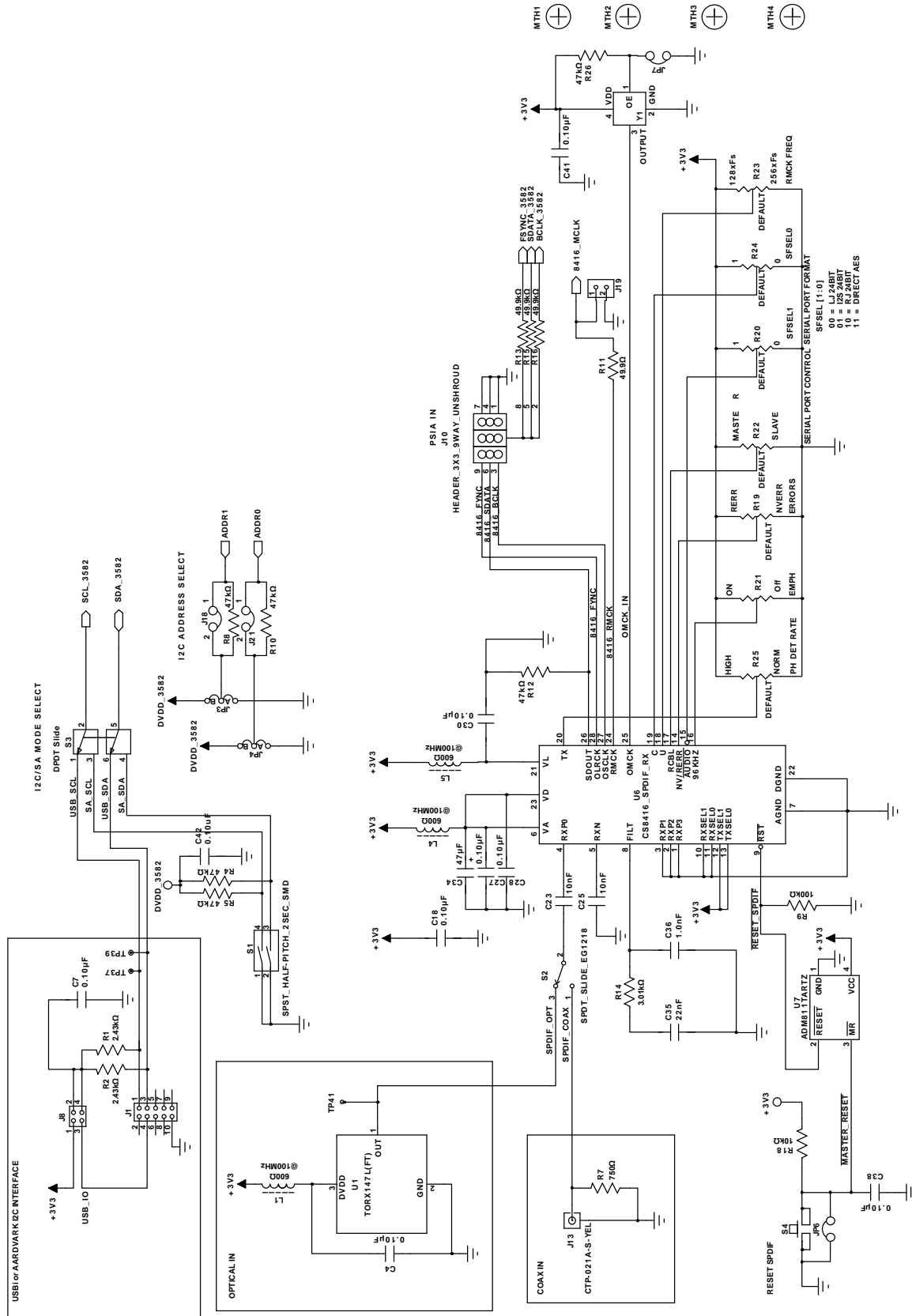


Figure 8. Schematic of the SSM3582 Evaluation Board PC, Digital Input Section

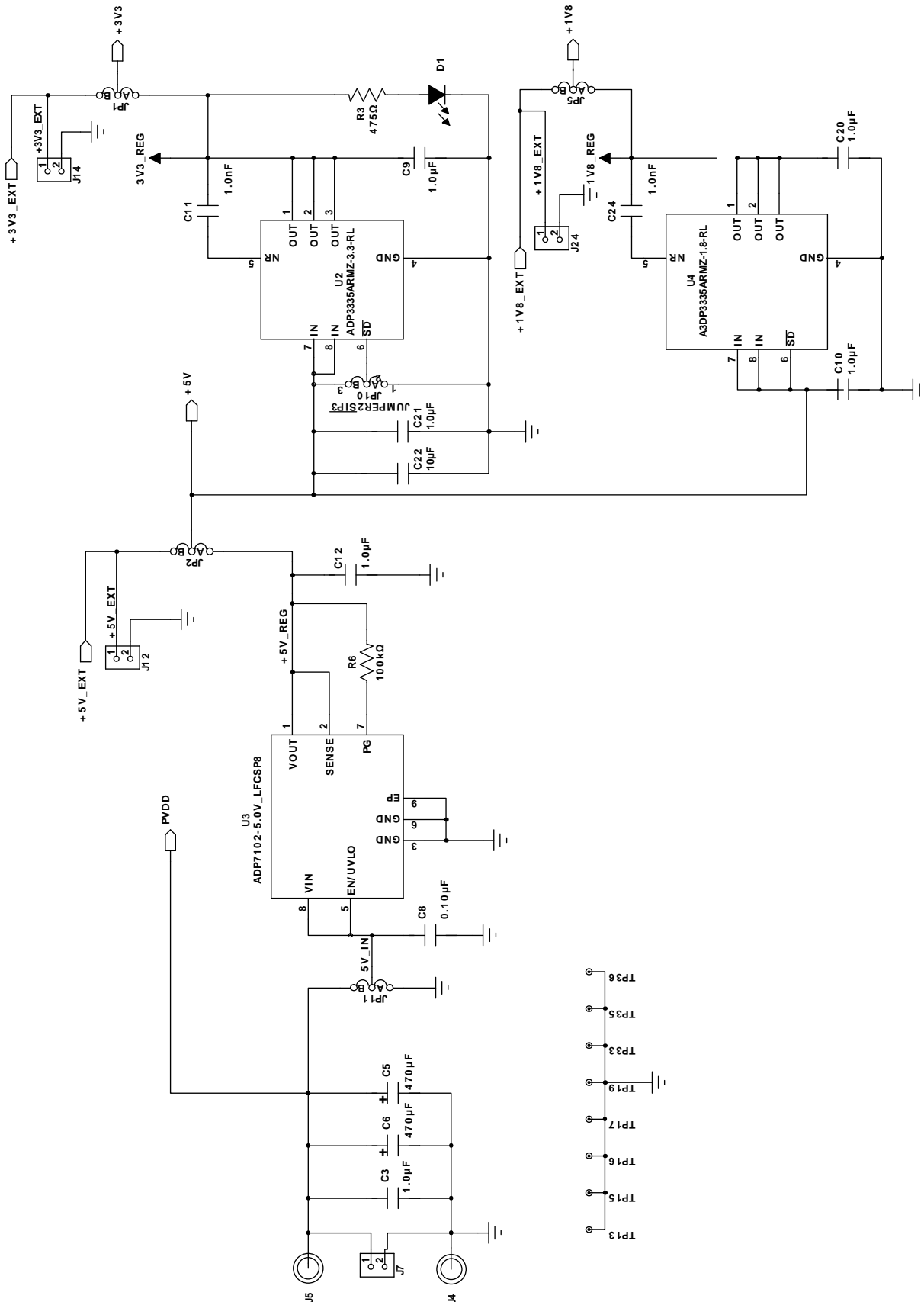
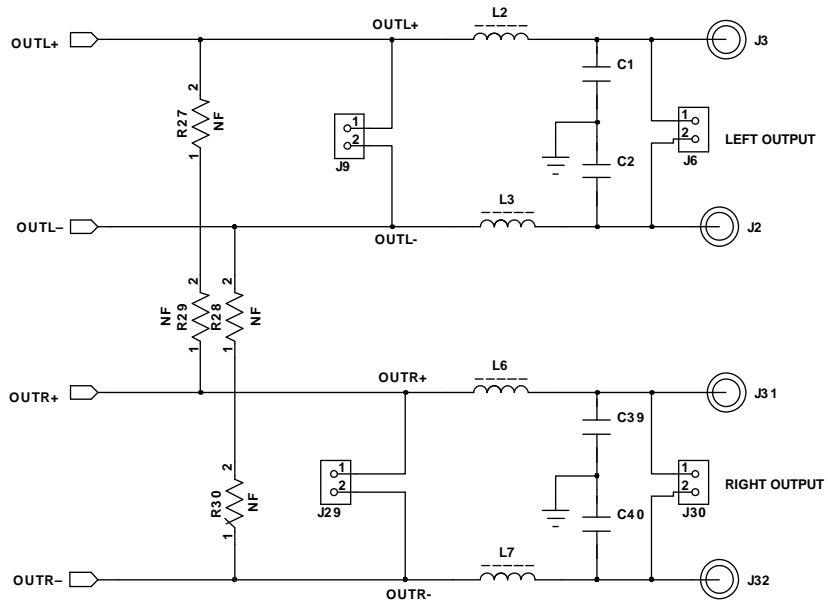


Figure 9. Schematic of the SSM3582Z Evaluation Board Power Supply Section



R2 THROUGH R30 NOT FITTED FOR STEREO
 R27 THROUGH R300OHM FOR MONO

Figure 10. Schematic of the SSM3582 Evaluation Board Output Section

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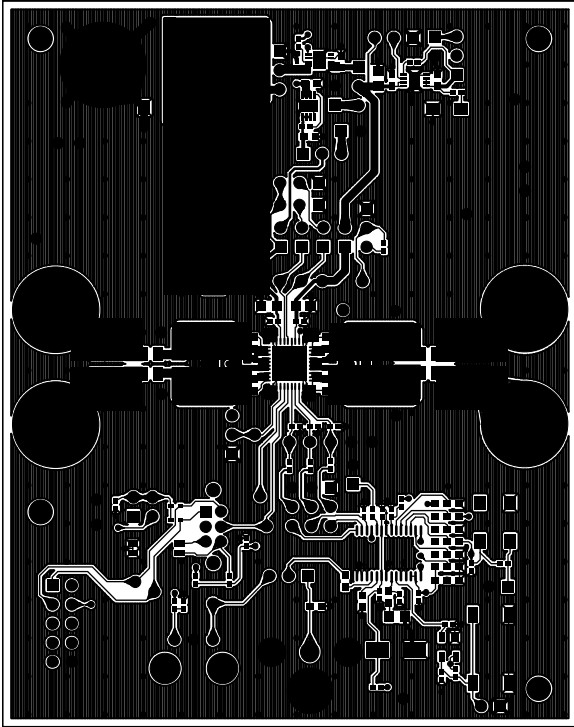


Figure 11. SSM3582 Evaluation Board Top Layer, Copper

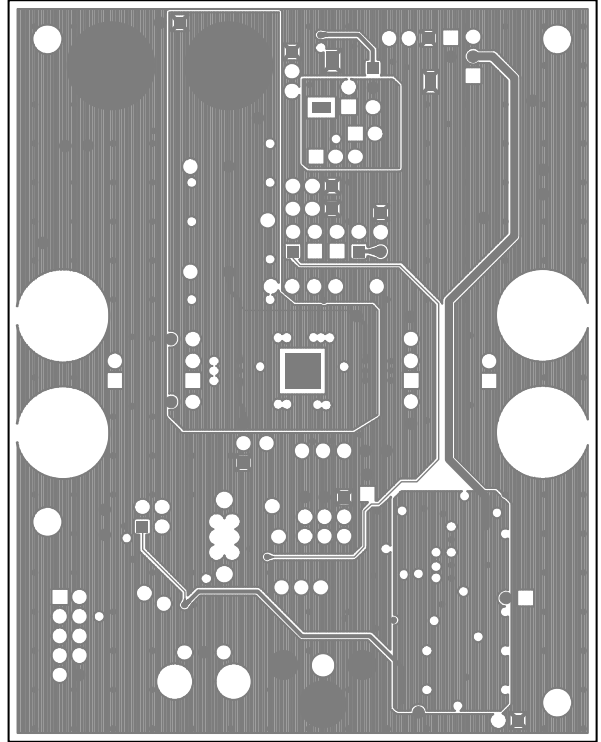


Figure 13. SSM3582 Evaluation Board Third Layer, Copper

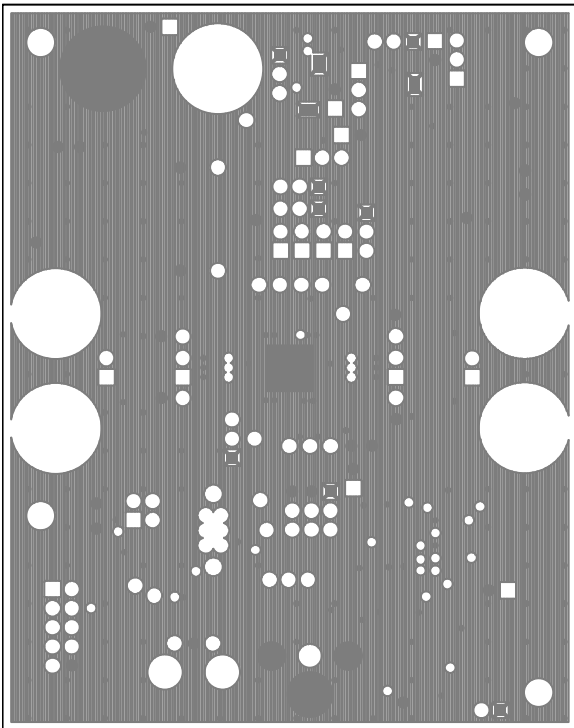


Figure 12. SSM3582 Evaluation Board Second Layer, Copper

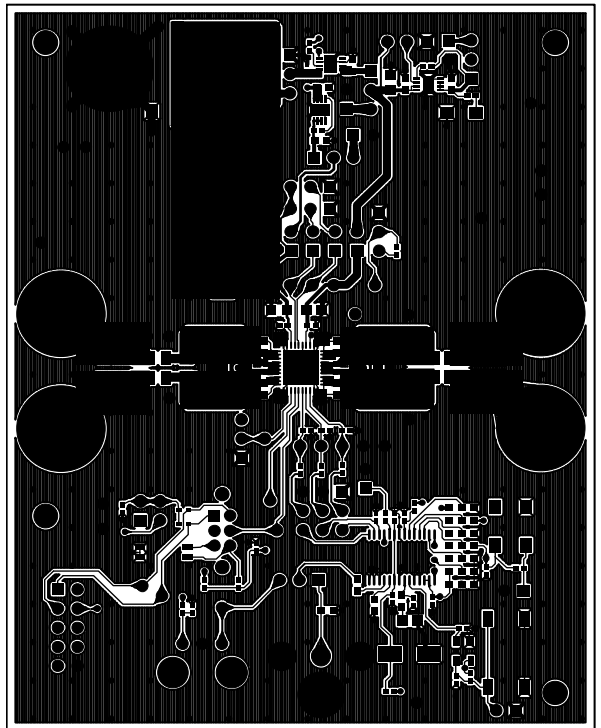


Figure 14. SSM3582 Evaluation Board Bottom Layer, Copper

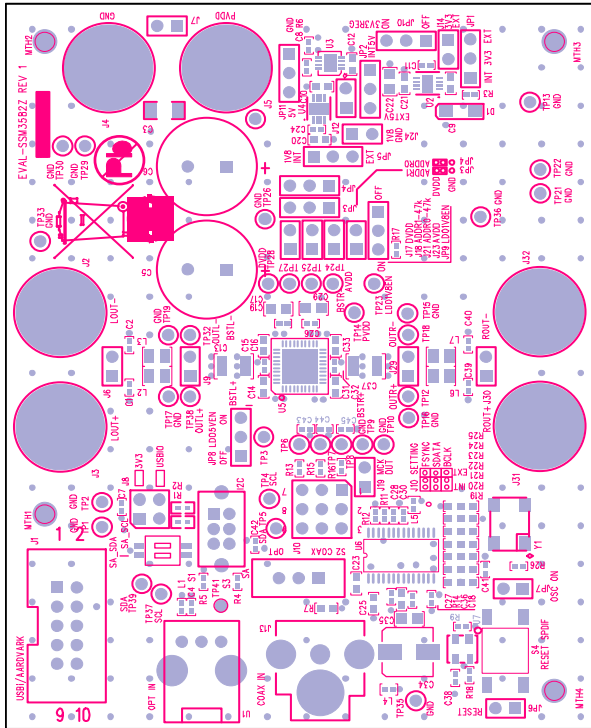
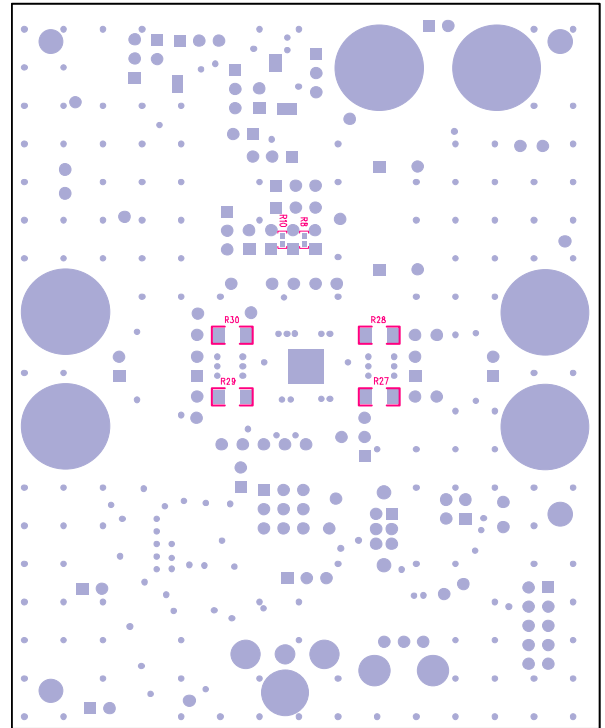


Figure 15. SSM3582Z Evaluation Board Top Silkscreen

142822-015



ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

| Qty | Reference Designator | Description | Manufacturer | Part Number |
|-----|--|--|---------------------------------|-------------------------------|
| 1 | Board | Evaluation Board EVAL-SSM3582Z , 4-layer, 3.8" x 3" | Analog Devices, Inc. | EVAL-SSM3582Z |
| 4 | C1, C2, C39, C40 | Multilayer ceramic capacitors, 220 pF, 50 V, NP0, 0402 | Murata ENA | GRM1555C1H221JA01D |
| 1 | C3 | Multilayer ceramic capacitors, 1 μF, 25 V, X7R, 1206 | Panasonic EC | ECJ-3YB1E105K |
| 11 | C4, C7, C18, C19, C26 to C28, C30, C38, C41 to C42 | Multilayer ceramic capacitors, 0.1 μF, 16 V, X7R, 0402 | Murata ENA | GRM155R71C104KA88D |
| 2 | C5, C6 | Aluminum electrolytic capacitors, HE, 470 μF, 25 V, 105°C, 5 mm | Nichicon | UHE1E471MPD6 |
| 3 | C8, C15, C32 | Multilayer ceramic capacitors, 0.1 μF, 35 V, X7R, 0402 | TDK Corp | CGA2B3X7R1V104K050BB |
| 5 | C9, C10, C12, C20 to C21 | Multilayer ceramic capacitors, 1 μF, 16 V, X7R, 0603 | Murata ENA | GRM188R71C105KA12D |
| 3 | C11, C24, C36 | Multilayer ceramic capacitors, 1 nF, 50 V, NP0, 0402 | Murata ENA | GRM1555C1H102JA01D |
| 2 | C13, C37 | Multilayer ceramic capacitors, 10 μF, 25 V, X7R, 1210 | Murata ENA | GCM32ER71E106KA57L |
| 4 | C14, C16, C31, C33 | Multilayer ceramic capacitors, 0.22 μF, 25 V, X7R, 0603 | Murata ENA | GRM188R71E224KA88D |
| 3 | C17, C22, C29 | Multilayer ceramic capacitors, 10 μF, 10 V, X7R, 0805 | Murata ENA | GRM21BR71A106KE51L |
| 2 | C23, C25 | Multilayer ceramic capacitors, 10 nF, 25 V, NP0, 0603 | TDK Corp | C1608C0G1E103J |
| 1 | C34 | Aluminum electrolytic capacitor, FC, 47 μF, 16 V, 105°C, SMD_D | Panasonic EC | EEE-FC1C470P |
| 1 | C35 | Multilayer ceramic capacitor, 22 nF, 25 V, NP0, 0805 | Murata ENA | GRM21B5C1H223JA01L |
| 3 | C43 to C45 | Multilayer ceramic capacitors, 10 pF, 50 V, NP0, 0402 | Murata ENA | GRM1555C1H100JZ01D |
| 1 | D1 | Red, diffused, 6.0 mcd, 635 nm, 1206 | Lumex Opto | SML-LX1206IW-TR |
| 1 | J1 | 10-way, shroud polarized header | 3M | N2510-6002RB |
| 6 | J2 to J5, J31, J32 | Binding posts, mini uninsulated base, through-hole | Johnson | 111-2223-001 |
| 9 | J6, J7, J9, J12, J14, J19, J24, J29, J30 | 2-pin headers, unshrouded jumper, 0.10", use Tyco shunt 881545-2 | Sullins Electronics Corp | PBC02SAAN; or cut PBC36SAAN |
| 1 | J8 | 4-way unshrouded header | 3M | PBC02DAAN, or cut PBC36DAAN |
| 1 | J10 | 9-way unshrouded header | TE Connectivity | 103817-2 |
| 1 | J13 | RCA jack, printed circuit board, through-hole mount, right angle, yellow | Connect-Tech Products Corp. | CTP-021A-S-YEL |
| 3 | J17, J18, J21 | 2-pin headers, unshrouded jumper, 0.10", use Tyco shunt 881545-2 | Sullins Electronics Corp | PBC02SAAN; or cut PBC36SAAN |
| 1 | J23 | 2-pin header, unshrouded jumper, 0.10", use Tyco shunt 881545-2 | Sullins Electronics Corp | PBC02SAAN; or cut PBC36SAAN |
| 9 | JP1 to JP5, JP8 to JP11 | Three-position SIP headers | Sullins | PBC03SAAN; or cut PBC36SAAN |
| 2 | JP6, JP7 | 2-pin headers, unshrouded jumper, 0.10", use Tyco shunt 881545-2 | Sullins Electronics Corp | PBC02SAAN; or cut PBC36SAAN |
| 3 | L1, L4, L5 | Chip ferrite beads, 600 Ω at 100 MHz | TDK Corp | MMZ1005S601C |
| 4 | L2, L3, L6, L7 | Chip ferrite beads, 180 Ω at 100 MHz, NFZ2MSM181 | Murata | NFZ2MSM181SN10L |
| 4 | MTH1 to MTH14 | 6-32 nylon screws and 1/2" standoff | Building Fasteners and Keystone | NY PMS 632 0025 PH and 1903C |
| 2 | R1, R2 | Chip resistors, 2.43 kΩ, 1%, 63 mW, thick film, 0402 | Vishay/Dale | CRCW04022K43FKED |
| 1 | R3 | Chip resistors, 475 Ω, 1%, 63 mW, thick film, 0402 | Vishay/Dale | CRCW0402475RFKED |
| 7 | R4, R5, R8, R10, R12, R17, R26 | Chip resistors, 47 kΩ, 1%, 63 mW, thick film, 0402 | Yageo | RC0402FR-0747K0L |
| 2 | R6, R9 | Chip resistors, 100 kΩ, 1%, 100 mW, thick film, 0402 | Panasonic EC | ERJ-2RKF1003X |
| 1 | R7 | Chip resistor, 75 Ω, 1%, 100mW Thick Film 0603 | Panasonic EC | ERJ-3EKF75R0V |
| 4 | R11, R13, R15, R16 | Chip resistors, 49.9 Ω, 1%, 63 mW thick film 0402 | Yageo | RC0402FR-0749R9L |
| 1 | R14 | Chip resistor, 3.01 kΩ, 1%, 100 mW, thick film, 0603 | Rohm | MCR03EZPFX3011 |
| 1 | R18 | Chip resistor, 10 kΩ, 1%, 63 mW thick film 0402 | Rohm | MCR01MZPF1002 |

| Qty | Reference Designator | Description | Manufacturer | Part Number |
|-----|---|---|----------------------|-------------------------------------|
| 7 | R19 to R25 | Chip resistors, 47.5 kΩ, 1%, 100 mW, thick film, 0603 | Panasonic EC | ERJ-3EKF4752V |
| 4 | R27 to R30 | Chip resistors, 0 Ω, 5%, 250 mW, thick film, 1206 | Panasonic EC | ERJ-8GEY0R00V |
| 1 | S1 | Switch, dual inline package, 4-poles, sealed SMD (half-pitch) | Omron | A6H-2102 |
| 1 | S2 | Single-pole double throw, slide switch, PC mount | E-Switch | EG1218 |
| 1 | S3 | Dual-pole, dual-throw, slide switch, vertical | E-Switch | EG2207 |
| 1 | S4 | Tact switch, 6 mm, gull wing | Tyco/Alcoswitch | FSM6J5MA |
| 36 | TP1 to T10, TP12 to T19, TP21 to T30, TP32 to T39 | Mini test points, white, 1", OD | Keystone Electronics | 5002 |
| 1 | TP41 | Gold pad only | Do not install | Do not install |
| 1 | U1 | 15 Mb/s, fiber optic receiving module with shutter | Toshiba | TORX147L(FT) |
| 1 | U2 | High accuracy, ultralow IQ, 500 mA, any capacitor, low dropout regulator | Analog Devices, Inc. | Not applicable |
| 1 | U3 | Fixed 5 V output, 20 V Input, 300 mA, low noise, CMOS LDO | Analog Devices, Inc. | ADP7102ACPZ-5.0 |
| 1 | U4 | High accuracy, ultralow IQ, 500 mA, any capacitor, low dropout regulator | Analog Devices, Inc. | Not applicable |
| 1 | U5 | IC 2x, 31.76 W, Class-D amplifier SSM3582 , 40-lead LFCSP | Analog Devices, Inc. | SSM3582 |
| 1 | U6 | 192 kHz digital receiver, 28-TSSOP | Cirrus Logic | CS8416-CZZ |
| 1 | U7 | Microprocessor voltage supervisor, logic low, RESET output | Analog Devices, Inc. | ADM811TARTZ-REEL7 |
| 1 | Y1 | 12.288 MHz, fixed SMD oscillator, 3.3 V to 5 V dc | Cardinal Components | CPPFX C 7 LT - A7 BR - 12.288MHz TS |

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

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UG14262-0-4/16(0)



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