19-0168; Rev 3; 7/95

MAXIM

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

General Description

The MAX530 is a low-power, 12-bit, voltage-output digital-to-analog converter (DAC) that uses single +5V or dual ±5V supplies. This device has an on-chip voltage reference plus an output buffer amplifier. Operating current is only 250µA from a single +5V supply, making it ideal for portable and battery-powered applications. In addition, the SSOP (Shrink-Small-Outline-Package) measures only 0.1 square inches, using less board area than an 8-pin DIP. 12-bit resolution is achieved through laser trimming of the DAC, op amp, and reference. No further adjustments are necessary.

Internal gain-setting resistors can be used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V, or ±2.048V. Four-quadrant multiplication is possible without the use of external resistors or op amps. The parallel logic inputs are double buffered and are compatible with 4-bit, 8-bit, and 16-bit microprocessors. For DACs with similar features but with a serial data interface, refer to the MAX531/MAX538/MAX539 data sheet.

Applications

Battery-Powered Data-Conversion Products
Minimum Component-Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Microprocessor-Controlled Calibration

Features

- **Buffered Voltage Output**
- **Internal 2.048V Voltage Reference**
- **Operates from Single +5V or Dual ±5V Supplies**
- **Low Power Consumption:**
  250µA Operating Current
  40µA Shutdown-Mode Current
- **SSOP Package Saves Space**
- **Relative Accuracy: ±1/2 LSB Max Over Temperature**
- **Guaranteed Monotonic Over Temperature**
- **4-Quadrant Multiplication with No External Components**
- **Power-On Reset**
- **Double-Buffered Parallel Logic Inputs**

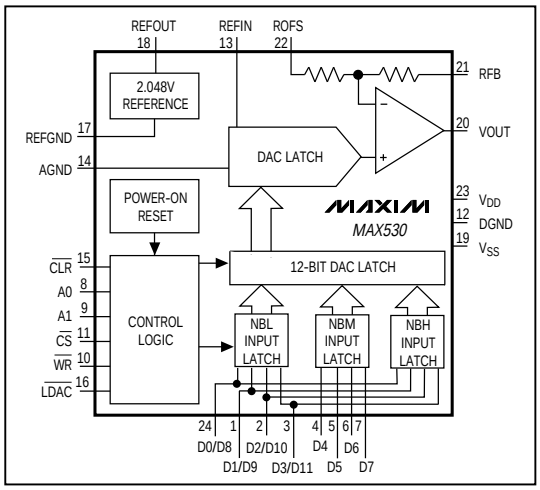
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX530ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX530BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX530ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX530BCWG	0°C to +70°C	24 Wide SO	±1
MAX530ACAG	0°C to +70°C	24 SSOP	±1/2
MAX530BCAG	0°C to +70°C	24 SSOP	±1
MAX530BC/D	0°C to +70°C	Dice*	±1

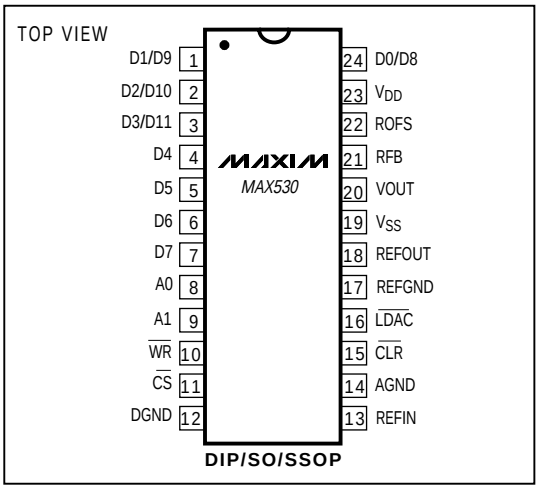
Ordering Information continued on last page.

** Dice are tested at T_A = +25°C, DC parameters only.*

Functional Diagram



Pin Configuration



+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND and V_{DD} to AGND .....-0.3V, +6V
V_{SS} to DGND and V_{SS} to AGND .....-6V, +0.3V
V_{DD} to V_{SS} ..... -0.3V, +12V
AGND to DGND.....-0.3V, +0.3V
REFGND to AGND.....-0.3V, (V_{DD} + 0.3V)
Digital Input Voltage to DGND ..... -0.3V, (V_{DD} + 0.3V)
REFIN.....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
REFOUT .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
REFOUT to REFGND..... -0.3V, (V_{DD} + 0.3V)
RFB .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
ROFS .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)

VOUT to AGND (Note 1) ..... V_{SS}, V_{DD}
Continuous Current, Any Input .....±20mA
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C).....1067mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges:
MAX530_C_ _ .....0°C to +70°C
MAX530_E_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The output may be shorted to V_{DD}, V_{SS}, DGND, or AGND if the continuous package power dissipation and current ratings are not exceeded. Typical short-circuit currents are 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = 5V ±10%, V_{SS} = 0V, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	V_{DD} = 5V (Note 2)	MAX530AC/AE			±0.5	LSB
			MAX530BC/BE			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Unipolar Offset Error	V_{OS}	V_{DD} = 5V	MAX530_C/E	0	1	8	LSB
Unipolar Offset Temperature Coefficient	TCV_{OS}				3		ppm/°C
Unipolar Offset-Error Power-Supply Rejection	PSRR	4.5V ≤ V_{DD} ≤ 5.5V (Note 3)			0.4	1	LSB/V
Gain Error (Note 2)	GE	DAC latch = all 1s, VOUT < V_{DD} - 0.4V (Note 2)	MAX530_C/E			±1	LSB
Gain-Error Temperature Coefficient					1		ppm/°C
Gain-Error Power-Supply Rejection	PSRR	4.5V ≤ V_{DD} ≤ 5.5V (Note 3)			0.4	1	LSB/V
DAC VOLTAGE OUTPUT (VOUT)							
Output Voltage Range				0		V_{DD} - 0.4	V
Resistive Load		VOUT = 2V, load regulation ≤ ±1LSB		2			kΩ
DC Output Impedance					0.2		Ω
Short-Circuit Current	I_{SC}				20		mA
REFERENCE INPUT (REFIN)							
Reference Input Range				0		V_{DD} - 2	V
Reference Input Resistance		Code dependent, minimum at code 555hex		40			kΩ
Reference Input Capacitance		Code dependent (Note 4)		10		50	pF
AC Feedthrough		(Note 5)			-80		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V_{DD} = 5V ±10%, V_{SS} = 0V, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT)							
Reference Tolerance	V_{REFOUT}	V_{DD} = 5.0V	T_A = +25°C	2.024	2.048	2.072	V
			MAX530BC	2.017		2.079	
			MAX530BE	2.013		2.083	
Reference Output Resistance	R_{REFOUT}	(Note 8)				2	Ω
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V				300	µV/V
Noise Voltage	e_n	0.1Hz to 10kHz			400		µVp-p
Temperature Coefficient		MAX530AC/AE			30	50	ppm/°C
		MAX530BC/BE			30		
Minimum Required External Capacitor	C_{MIN}			3.3			µF
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		T_A = +25°C		0.15	0.25		V/µs
Voltage Output Settling Time		To ±0.5LSB, VOUT = 2V			25		µs
Digital Feedthrough		$\overline{WR}$ = V_{DD}, digital inputs all 1s to all 0s			5		nV-s
Signal-to-Noise Plus Distortion Ratio	SINAD	Unity gain (Note 5)			68		dB
		Gain = 2 (Note 5)			68		
DIGITAL INPUTS (D0-D7, $\overline{LDAC}$, $\overline{CLR}$, $\overline{CS}$, $\overline{WR}$, A0, A1)							
Logic High Input	V_{IH}			2.4			V
Logic Low Input	V_{IL}					0.8	V
Digital Leakage Current		V_{IN} = 0V or V_{DD}				±1	µA
Digital Input Capacitance					8		pF
POWER SUPPLIES							
Positive Supply-Voltage Range	V_{DD}	(Note 6)		4.5		5.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}			250	400	µA
SWITCHING CHARACTERISTICS							
Address to $\overline{WR}$ Setup	t_{AWS}			5			ns
Address to $\overline{WR}$ Hold	t_{AWH}			5			ns
$\overline{CS}$ to $\overline{WR}$ Setup	t_{CWS}			0			ns
$\overline{CS}$ to $\overline{WR}$ Hold	t_{CWH}			0			ns
Data to $\overline{WR}$ Setup	t_{DS}			45			ns
Data to $\overline{WR}$ Hold	t_{DH}			0			ns
$\overline{WR}$ Pulse Width	t_{WR}			45			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}			45			ns
$\overline{CLR}$ Pulse Width	t_{CLR}			45			ns
Internal Power-On Reset Pulse Width	t_{POR}	(Note 4)			1.3	10	µs

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies

(V_{DD} = 5V ±10%, V_{SS} = -5V ±10%, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	V_{DD} = 5V, V_{SS} = -5V	MAX530AC/AE			±0.5	LSB
			MAX530BC/BE			±1.5	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Bipolar Offset Error	V_{OS}	V_{DD} = 5V, V_{SS} = -5V	MAX530_C/E		0	±8	LSB
Bipolar Offset Temperature Coefficient	TCV_{OS}				3		ppm/°C
Bipolar Offset-Error Power-Supply Rejection	PSRR	4.5V ≤ V_{DD} ≤ 5.5V -5.5V ≤ V_{SS} ≤ -4.5V (Note 3)			0.4	1	LSB/V
Gain Error		MAX530_C/E				±1	LSB
Gain-Error Temperature Coefficient	TC				1		ppm/°C
Gain-Error Power-Supply Rejection	PSRR	4.5V ≤ V_{DD} ≤ 5.5V, -5.5V ≤ V_{SS} ≤ -4.5V (Note 3)			0.4	1	LSB/V
DAC VOLTAGE OUTPUT (VOUT)							
Output Voltage Range				V_{SS} + 0.4		V_{DD} - 0.4	V
Resistive Load		VOUT = 2V, load regulation ≤ ±1LSB		2			kΩ
DC Output Impedance					0.2		Ω
Short-Circuit Current	I_{SC}				20		mA
REFERENCE INPUT (REFIN)							
Reference Input Range				V_{SS} + 2		V_{DD} - 2	V
Reference Input Resistance		Code dependent, minimum at code 555hex		40			kΩ
Reference Input Capacitance		Code dependent (Note 4)		10		50	pF
AC Feedthrough		(Note 5)			-80		dB
REFERENCE OUTPUT (REFOUT)—Specifications are identical to those under Single +5V Supply							
DYNAMIC PERFORMANCE—Specifications are identical to those under Single +5V Supply							
DIGITAL INPUTS (D0-D7, $\overline{LDAC}$, $\overline{CLR}$, $\overline{CS}$, $\overline{WR}$, A0, A1)—Specifications are identical to those under Single +5V Supply							
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	(Note 6)		4.5		5.5	V
Negative Supply Voltage	V_{SS}	(Note 7)		-5.5		-4.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}			250	400	µA
Negative Supply Current	I_{SS}	Outputs unloaded, all digital inputs = 0V or V_{DD}			150	200	µA
SWITCHING CHARACTERISTICS—Specifications are identical to those under Single +5V Supply							

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies (continued)

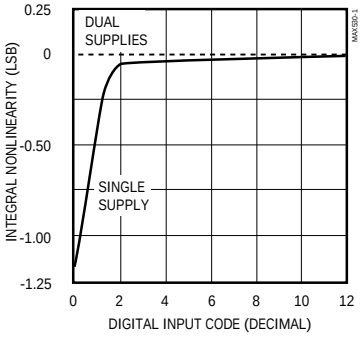
(V_{DD} = 5V ±10%, V_{SS} = -5V ±10%, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Note 2: In single supply, INL and GE are calculated from code 11 to code 4095.
Note 3: Zero Code, Bipolar and Gain Error PSRR are input referred specifications. In Unity Gain, the specification is 500µV. In Gain = 2 and Bipolar modes, the specification is 1mV.
Note 4: Guaranteed by design.
Note 5: REFIN = 1kHz, 2.0Vp-p.
Note 6: For specified performance, V_{DD} = 5V ±10% is guaranteed by PSRR tests.
Note 7: For specified performance, V_{SS} = -5V ±10% is guaranteed by PSRR tests.
Note 8: Tested at I_{OUT} = 100µA. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

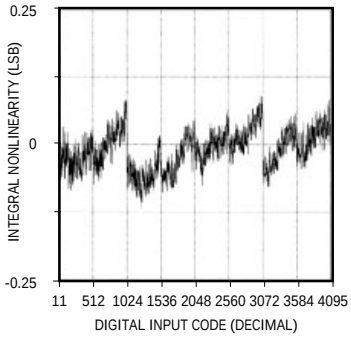
Typical Operating Characteristics

(T_A = +25°C, single supply (+5V), unity gain, code = all 1s, unless otherwise noted).

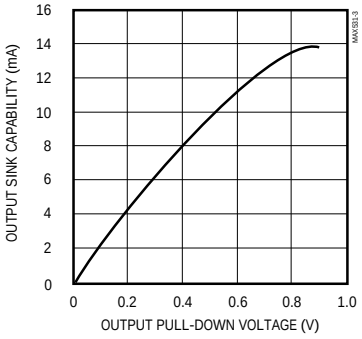
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (0–11)



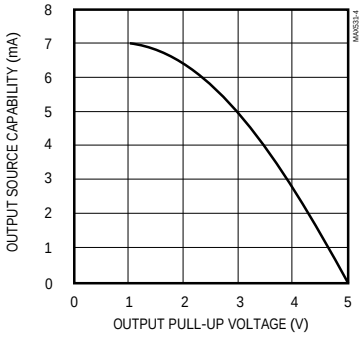
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (11–4095)



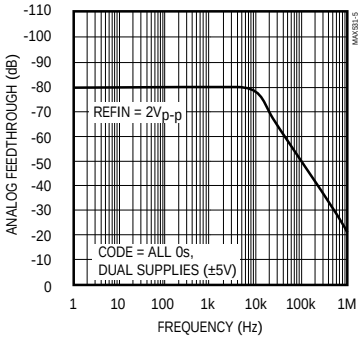
OUTPUT SINK CAPABILITY vs. OUTPUT PULL-DOWN VOLTAGE



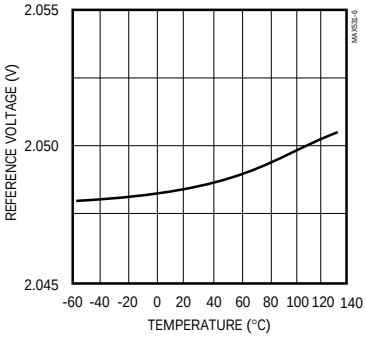
OUTPUT SOURCE CAPABILITY vs. OUTPUT PULL-UP VOLTAGE



ANALOG FEEDTHROUGH vs. FREQUENCY



REFERENCE VOLTAGE vs. TEMPERATURE

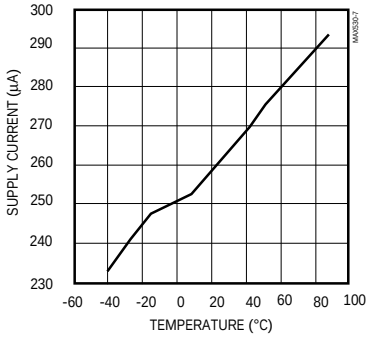


+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

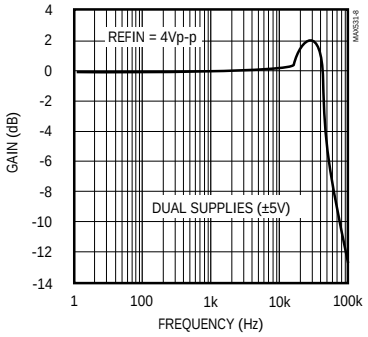
Typical Operating Characteristics (continued)

(T_A = +25°C, single supply (+5V), unity gain, code = all 1s, unless otherwise noted).

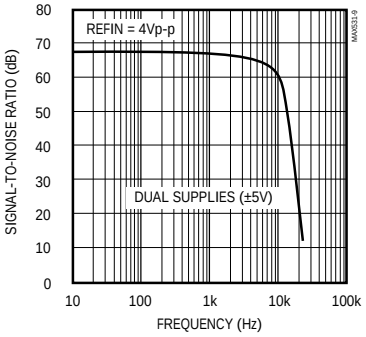
SUPPLY CURRENT vs. TEMPERATURE



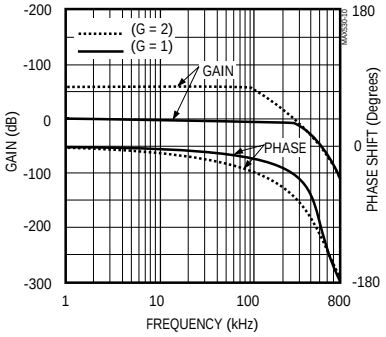
GAIN vs. FREQUENCY



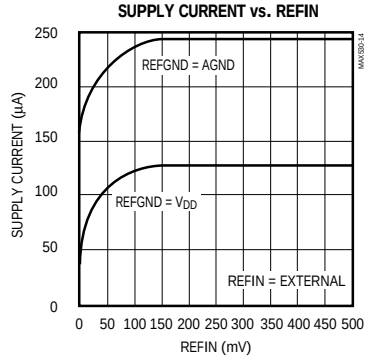
AMPLIFIER SIGNAL-TO- NOISE RATIO



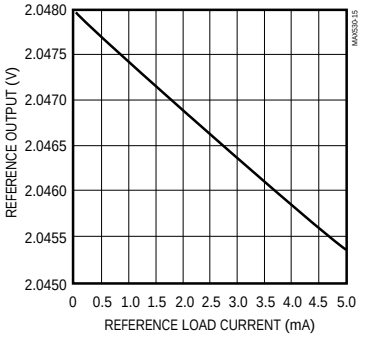
GAIN AND PHASE vs. FREQUENCY



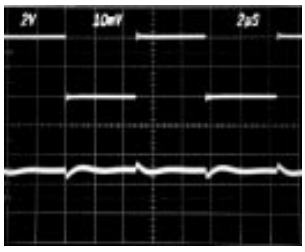
SUPPLY CURRENT vs. REFIN



REFERENCE OUTPUT VOLTAGE vs. REFERENCE LOAD CURRENT



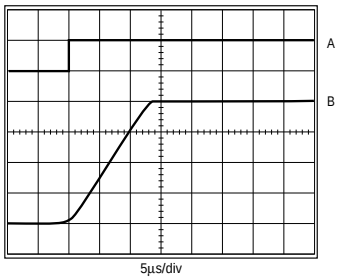
DIGITAL FEEDTHROUGH



2µs/div

A: D0...D7 = 100kHz, 4Vp-p
B: VOUT, 10mV/div
LDAC = CS = HIGH

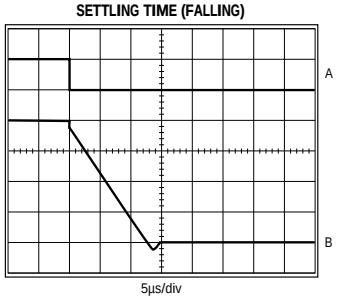
SETTLING TIME (RISING)



5µs/div

A: DIGITAL INPUTS RISING EDGE,
B: VOUT, NO LOAD, 1V/div
DUAL SUPPLY (±5V)
LDAC = LOW
BIPOLAR CONFIGURATION
V_{REFIN} = 2V

SETTLING TIME (FALLING)



5µs/div

A: DIGITAL INPUTS FALLING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div
DUAL SUPPLY (±5V)
LDAC = LOW
BIPOLAR CONFIGURATION
V_{REFIN} = 2V

Pin Description

PIN	NAME	FUNCTION
1	D1/ D9	D1 Input Dta, when A0 = 0 and A1 = 1, or D9 Input when A0 = A1 = 1*
2	D2/ D10	D2 Input Dta, when A0 = 0 and A1 = 1, or D10 Input when A0 = A1 = 1*
3	D3/ D11	D3 Input Dta, when A0 = 0 and A1 = 1, or D11 (MSB) Input when A0 = A1 =1*
4	D4	D4 Input Dta, or tie to D0 and multiplex when A0 = 1 and A1 = 0*
5	D5	D5 Input Dta, or tie to D1 and multiplex when A0 = 1 and A1 = 0*
6	D6	D6 Input Dta, or tie to D2 and multiplex when A0 = 1 and A1 = 0*
7	D7	D7 Input Dta, or tie to D3 and multiplex when A0 = 1 and A1 = 0*
8	A0	Address Line A0. With A1, used to multiplex 4 of 12 data lines to load low (NBL), middle (NBM), and high (NBH) 4-bit nibbles. (12 bits can also be loaded as 8+4.)
9	A1	Address Line A1. Set A0 = A1 = 0 for NBL and NBM, A0 = 0 and A1 = 1 for NBL, A0 = 1 and A1 = 0 for NBM, or A0 = A1 = 1 for NBH. See Table 2 for complete input latch addressing.
10	$\overline{WR}$	Write Input (active low). Used with $\overline{CS}$ to load data into the input latch selected by A0 and A1.
11	$\overline{CS}$	Chip Select (active low). Enables addressing and writing to this chip from common bus lines.
12	DGND	Digital Ground
13	REFIN	Reference Input. Input for the R-2R DAC. Connect an external reference to this pin or a jumper to REFOUT (pin 18) to use the internal 2.048V reference.
14	AGND	Analog Ground
15	$\overline{CLR}$	Clear (active low). A low on $\overline{CLR}$ resets the DAC latches to all 0s.
16	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of the input latch to the DAC latch and updates VOUT.
17	REFGND	Reference Ground must be connected to AGND when using the internal reference. Connect to V_{DD} to disable the internal reference and save power.
18	REFOUT	Reference Output. Output of the internal 2.048V reference. Tie to REFIN to drive the R-2R DAC.
19	V_{SS}	Negative Power Supply. Usually ground for single-supply or -5V for dual-supply operation.
20	VOUT	Voltage Output. Op-amp buffered DAC output.
21	RFB	Feedback Pin. Op-amp feedback resistor. Always connect to VOUT.
22	ROFS	Offset Resistor Pin. Connect to VOUT for G = 1, to AGND for G = 2, or to REFIN for bipolar output.
23	V_{DD}	Positive Power Supply (+5V)
24	D0/D8	D0 (LSB) Input Dta when A0 = 0 and A1 = 1, or D8 Input when A0 = A1= 1*

* This applies to 4 + 4 + 4 input loading mode. See Table 2 for 8 + 4 input loading mode.

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

Detailed Description

The MAX530 consists of a parallel-input logic interface, a 12-bit R-2R ladder, a reference, and an op amp. The *Functional Diagram* shows the control lines and signal flow through the input data latch to the DAC latch, as well as the 2.048V reference and output op amp. Total supply current is typically 250µA with a single +5V supply. This circuit is ideal for battery-powered, microprocessor-controlled applications where high accuracy, no adjustments, and minimum component count are key requirements.

R-2R Ladder

The MAX530 uses an "inverted" R-2R ladder network with a BiCMOS op amp to convert 12-bit digital data to analog voltage levels. Figure 1 shows a simplified diagram of the R-2R DAC and op amp. Unlike a standard DAC, the MAX530 uses an "inverted" ladder network. Normally, the REFIN pin is the current output of a standard DAC and would be connected to the summing junction, or virtual ground, of an op amp. In this standard DAC configuration, however, the output voltage would be the inverse of the reference voltage. The MAX530's topology makes the ladder output voltage the same polarity as the reference input, which makes the device suitable for single-supply operation. The BiCMOS op amp is then used to buffer, invert, or amplify the ladder signal.

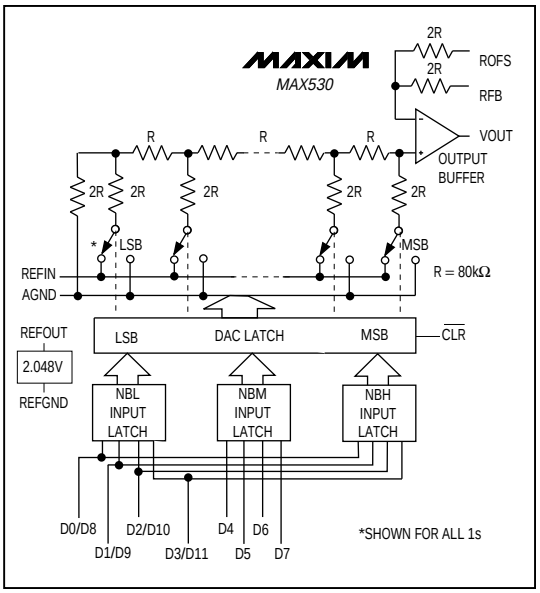


Figure 1. Simplified MAX530 DAC Circuit

Ladder resistors are nominally 80kΩ to conserve power and are laser trimmed for gain and linearity. The input impedance at REFIN is code dependent. When the DAC register is all 0s, all rungs of the ladder are grounded and REFIN is open or no load. Maximum loading (minimum REFIN impedance) occurs at code 010101... or 555hex. Minimum reference input impedance at this code is guaranteed to be not less than 40kΩ.

The REFIN and REFOUT pins allow the user to choose between driving the R-2R ladder with the on-chip reference or an external reference. REFIN may be below analog ground when using dual supplies. See the *External Reference* and *Four-Quadrant Multiplication* sections for more information.

Internal Reference

The on-chip reference is laser trimmed to generate 2.048V at REFOUT. The output stage can source and sink current so REFOUT can settle to the correct voltage quickly in response to code-dependent loading changes. Typically source current is 5mA and sink current is 100µA.

REFOUT connects the internal reference to the R-2R DAC ladder at REFIN. The R-2R ladder draws 50µA maximum load current. If any other connection is made to REFOUT, ensure that the total load current is less than 100µA to avoid gain errors.

A separate REFGND pin is provided to isolate reference currents from other analog and digital ground currents. To achieve specified noise performance, connect a 33µF capacitor from REFOUT to REFGND (see Figure 2). Using smaller capacitance values increases noise, and values less than 3.3µF may compromise the reference's stability. For applications requiring the lowest noise, insert a buffered RC filter between REFOUT and REFIN. When using the internal reference, REFGND must be connected to AGND. In applications not requiring the internal reference, connect REFGND to V_{DD}, which shuts down the reference and saves typically 100µA of V_{DD} supply current.

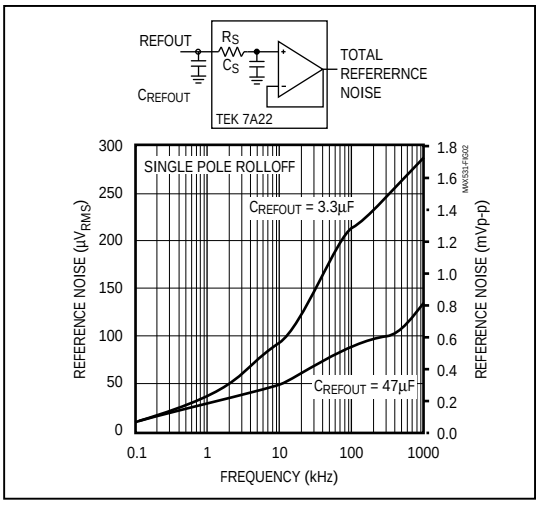


Figure 2. Reference Noise vs. Frequency

Output Buffer

The output amplifier uses a folded cascode input stage and a type AB output stage. Large output devices with low series resistance allow the output to swing to ground in single-supply operation. The output buffer is unity-gain stable. Input offset voltage and supply current are laser trimmed. Settling time is 25µs to 0.01% of final value. The output is short-circuit protected and can drive a 2kΩ load with more than 100pF of load capacitance. The op amp may be placed in unity-gain (G = 1), in a gain of two (G = 2), or in a bipolar-output mode by using the ROFS and RFB pins. These pins are used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V or ±2.048V, by connecting ROFS to VOUT, GND, or REFIN. RFB is always connected to VOUT. Table 1 summarizes ROFS usage.

Table 1. ROFS Usage

ROFS CONNECTED TO:	DAC OUTPUT RANGE	OP-AMP GAIN
VOUT	0V to 2.048V	G = 1
AGND	0V to 4.096V	G = 2
REFIN	-2.048V to +2.048V	Bipolar

Note: Assumes RFB = VOUT and REFIN = REFOUT = 2.048V

External Reference

An external reference in the range (V_{SS} + 2V) to (V_{DD} - 2V) may be used with the MAX530 in dual-supply, unity-gain operation. In single-supply, unity-gain operation, the reference must be positive and may not exceed (V_{DD} - 2V). The reference voltage determines the DAC's full-scale output. Because of the code-dependent nature of reference input impedances, a high-quality, low-output-impedance amplifier (such as the MAX480 low-power, precision op amp) should be used to drive REFIN.

If an upgrade to the internal reference is required, the 2.5V MAX873A is ideal: ±15mV initial accuracy, 7ppm/°C (max) temperature coefficient.

Power-On Reset

An internal power-on reset (POR) circuit forces the DAC register to reset to all 0s when V_{DD} is first applied. The POR pulse is typically 1.3µs; however, it may take 2ms for the internal reference to charge its large filter capacitor and settle to its trimmed value.

In addition to POR , a clear ($\overline{CLR}$) pin, when held low, sets the DAC register to all 0s. $\overline{CLR}$ operates asynchronously and independently from chip select ($\overline{CS}$). With the DAC input at all 0s, the op-amp output is at zero for unity-gain and G = 2 configurations, but it is at -V_{REF} for the bipolar configuration.

Shutdown Mode

The MAX530 is designed for low power consumption. Understanding the circuit allows power consumption management for maximum efficiency. In single-supply mode (V_{DD} = +5V, V_{SS} = GND) the initial supply current is typically only 160µA, including the reference, op amp, and DAC. This low current occurs when the power-on reset circuit clears the DAC to all 0s and forces the op-amp output to zero (unipolar mode only). See the Supply Current vs. REFIN graph in the *Typical Operating Characteristics*. Under this condition, there is no internal load on the reference (DAC = 000hex, REFIN is open circuit) and the op amp operates at its minimum quiescent current. The $\overline{CLR}$ signal resets the MAX530 to these same conditions and can be used to control a power-saving mode when the DAC is not being used by the system.

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

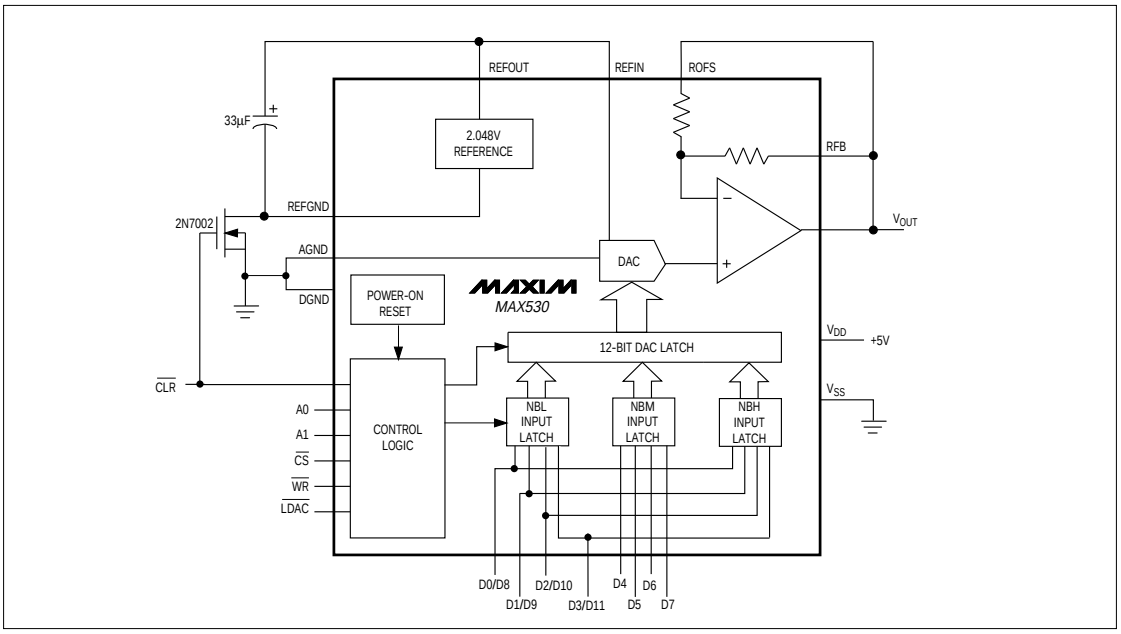


Figure 3. Low-Current Shutdown Mode

An additional 110µA of supply current can be saved when the internal reference is not used by connecting REFGND to V_{DD}. A low on resistance N-channel FET, such as the 2N7002, can be used to turn off the internal reference to create a shutdown mode with minimum current drain (Figure 3). When $\overline{CLR}$ is high, the transistor pulls REFGND to AGND and the reference and DAC operate normally. When $\overline{CLR}$ goes low, REFGND is pulled up to V_{DD} and the reference is shut down. At the same time, $\overline{CLR}$ resets the DAC register to all 0s, and the op-amp output goes to 0V for unity-gain and G = 2 modes. This reduces the total single-supply operating current from 250µA (400µA max) to typically 40µA in shutdown mode.

A small error voltage is added to the reference output by the reference current flowing through the N-channel pull-down transistor. The switch's on resistance should be less than 5Ω. A typical reference current of 100µA would add 0.5mV to REFOUT. Since the reference current and on resistance increase with temperature, the overall temperature coefficient will degrade slightly.

As data is loaded into the DAC and the output moves above GND, the op-amp quiescent current increases to its nominal value and the total operating current averages 250µA. Using dual supplies (±5V), the op amp is fully biased continuously, and the V_{DD} supply current is more constant at 250µA. The V_{SS} current is typically 150µA.

The MAX530 logic inputs are compatible with TTL and CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Table 2. Input Latch Addressing

$\overline{CLR}$	$\overline{CS}$	$\overline{WR}$	$\overline{LDAC}$	A0	A1	DATA UPDATED
L	X	X	X	X	X	Reset DAC Latches
H	H	X	H	X	X	No Operation
H	X	H	H	X	X	No Operation
H	L	L	H	H	H	NBH (D8-D11)
H	L	L	H	H	L	NBM (D4-D7)
H	L	L	H	L	H	NBL (D0-D3)
H	H	H	L	X	X	Update DAC Only
H	L	L	X	L	L	DAC NOT UPDATED
H	L	L	L	H	H	NBH and Update DAC

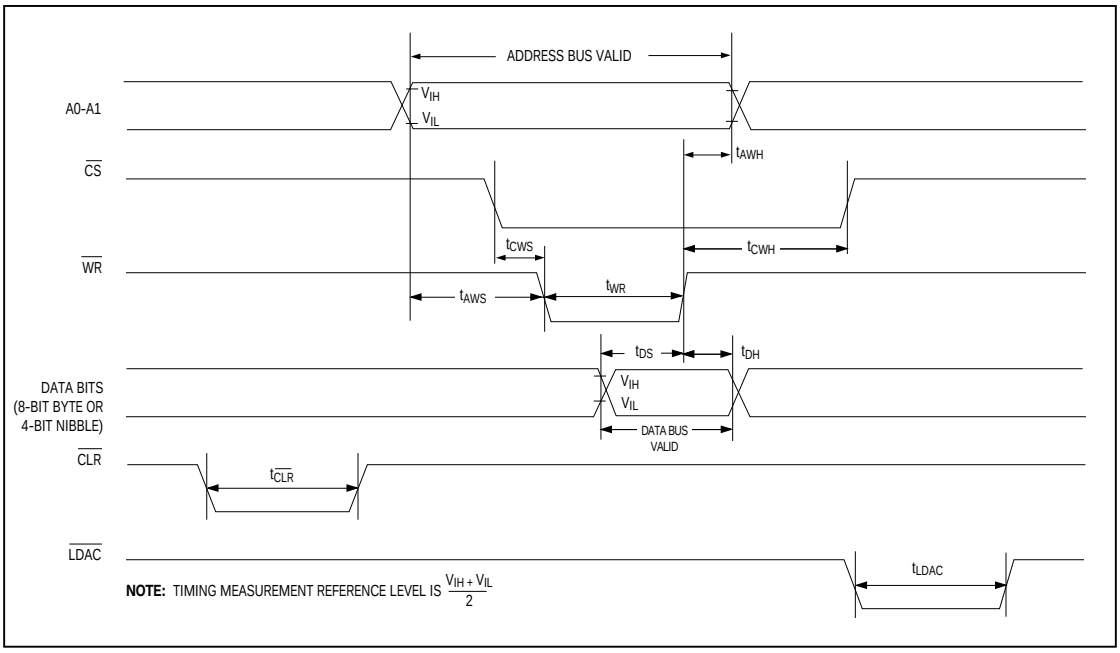


Figure 4. MAX530 Write-Cycle Timing Diagram

Parallel Logic Interface

Designed to interface with 4-bit, 8-bit, and 16-bit microprocessors (µPs), the MAX530 uses 8 data pins and double-buffered logic inputs to load data as 4 + 4 + 4 or 8 + 4. The 12-bit DAC latch is updated simultaneously through the control signal $\overline{LDAC}$. Signals A0, A1, $\overline{WR}$, and $\overline{CS}$ select which input latches to update. The 12-bit data is broken down into nibbles (NB); NBL is the enable signal for the lowest 4 bits, NBM is the enable for the middle 4 bits, and NBH is the enable for the highest and most significant 4 bits. Table 2 lists the address decoding scheme.

Refer to Figure 4 for the MAX530 write-cycle timing diagram.

Figure 5 shows the circuit configuration for a 4-bit µP application. Figure 6 shows the corresponding timing sequence. The 4 low bits (D0-D3) are connected in parallel to the other 4 bits (D4-D7) and then to the µP bus. Address lines A0 and A1 enable the input data latches for the high, middle, or low data nibbles. The µP sends chip select ($\overline{CS}$) and write ($\overline{WR}$) signals to latch in each of three nibbles in three cycles when the data is valid.

Figure 7 shows a typical interface to an 8-bit or a 16-bit µP. Connect 8 data bits from the data bus to pins D0-D7 on the MAX530. With $\overline{LDAC}$ held high, the user can load NBH or NBL + NBM in any order. Figure 8a shows the corresponding timing sequence. For fastest throughput, use Figure 8b's sequence. Address lines A0 and A1 are tied together and the DAC is loaded in 2 cycles as 8 + 4. In this scheme, with $\overline{LDAC}$ held low, the DAC latch is transparent. Always load NBL and NBM first, followed by NBH.

$\overline{LDAC}$ is asynchronous with respect to $\overline{WR}$. If $\overline{LDAC}$ is brought low before or at the same time $\overline{WR}$ goes high, $\overline{LDAC}$ must remain low for at least 50ns to ensure the correct data is latched. Data is latched into DAC registers on $\overline{LDAC}$'s rising edge.

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

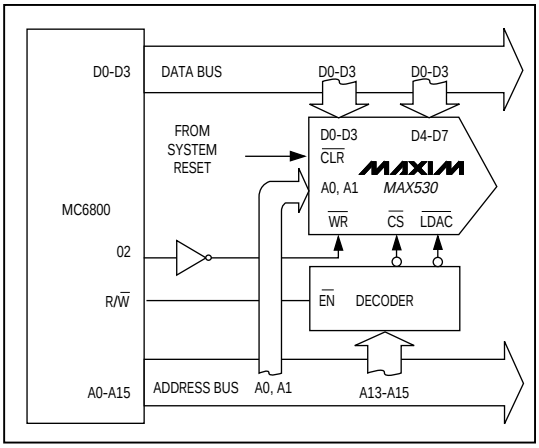


Figure 5. 4-Bit µP Interface

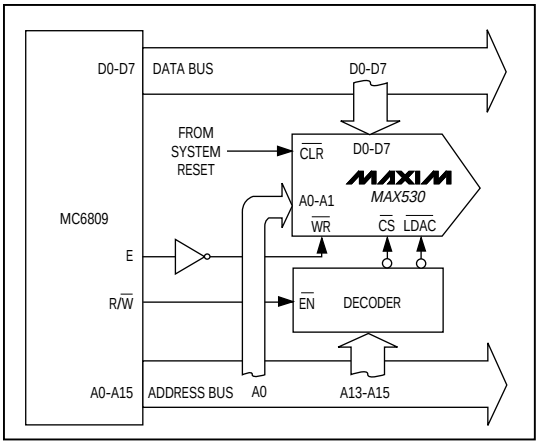


Figure 7. 8-Bit and 16-Bit µP Interface

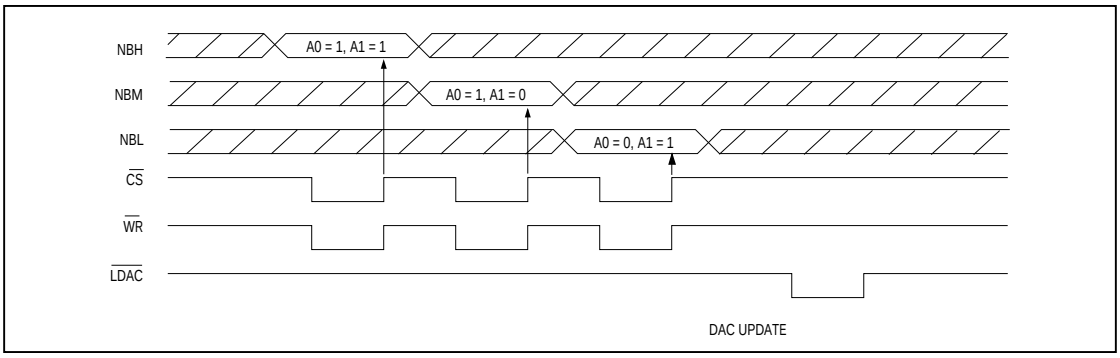


Figure 6. 4-Bit µP Timing Sequence

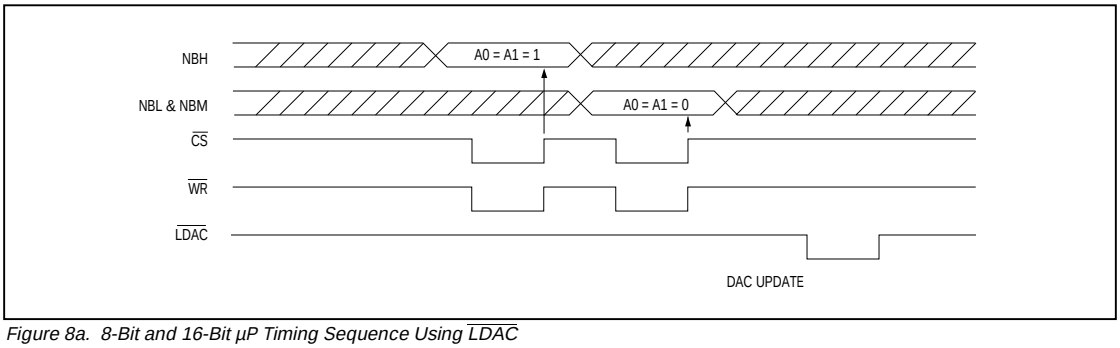


Figure 8a. 8-Bit and 16-Bit µP Timing Sequence Using $\overline{LDAC}$

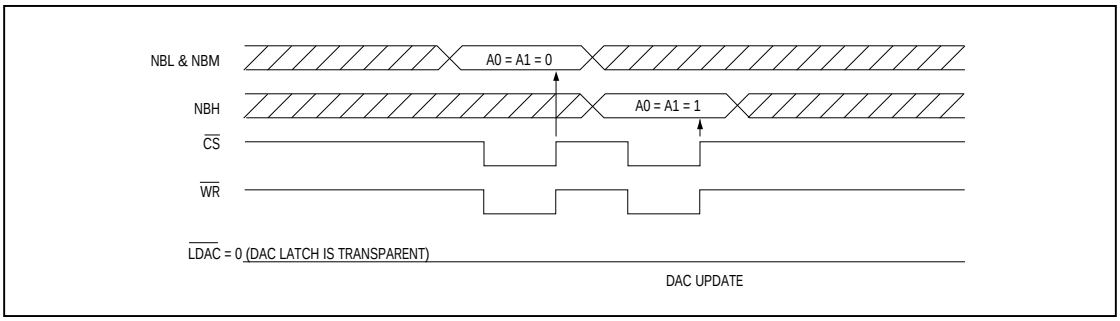


Figure 8b. 8-Bit and 16-Bit µP Timing Sequence with $\overline{LDAC}$ = 0

Unipolar Configuration

The MAX530 is configured for a 0V to +2.048V unipolar output range by connecting ROFS and RFB to VOUT (Figure 9). The converter operates from either single or dual supplies in this configuration. See Table 3 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, 1LSB = REFIN (2^{-12}).

A 0V to 4.096V unipolar output range is set up by connecting ROFS to AGND and RFB to VOUT (Figure 10). Table 4 shows the DAC-latch contents vs. VOUT. The MAX530 operates from either single or dual supplies in this mode. In this range, 1LSB = (2)(REFIN)(2^{-12}) = (REFIN)(2^{-11}).

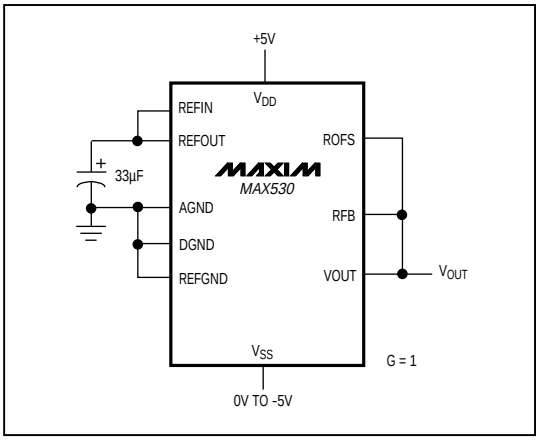


Figure 9. Unipolar Configuration (0V to +2.048V Output)

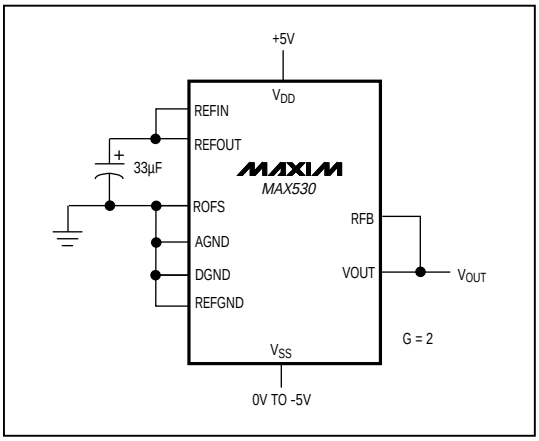


Figure 10. Unipolar Configuration (0V to +4.096V Output)

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

Table 3. Unipolar Binary Code Table (0V to V_{REFIN} Output), Gain = 1

INPUT	OUTPUT
1111 1111 1111	$(V_{REFIN})\frac{4095}{4096}$
1000 0000 0001	$(V_{REFIN})\frac{2049}{4096}$
1000 0000 0000	$(V_{REFIN})\frac{2048}{4096} = +V_{REFIN}/2$
0111 1111 1111	$(V_{REFIN})\frac{2047}{4096}$
0000 0000 0001	$(V_{REFIN})\frac{1}{4096}$
0000 0000 0000	0V

Table 4. Unipolar Binary Code Table (0V to $2V_{REFIN}$ Output), Gain = 2

INPUT	OUTPUT
1111 1111 1111	$+2\ (V_{REFIN})\frac{4095}{4096}$
1000 0000 0001	$+2\ (V_{REFIN})\frac{2049}{4096}$
1000 0000 0000	$+2\ (V_{REFIN})\frac{2048}{4096} = +V_{REFIN}$
0111 1111 1111	$+2\ (V_{REFIN})\frac{2047}{4096}$
0000 0000 0001	$+2\ (V_{REFIN})\frac{1}{4096}$
0000 0000 0000	0V

Bipolar Configuration

A $-V_{REFIN}$ to $+V_{REFIN}$ bipolar range is set up by connecting ROFS to REFIN and RFB to VOUT, and operating from dual (±5V) supplies (Figure 11). Table 5 shows the DAC-latch contents (input) vs. VOUT (output). In this range, 1 LSB = REFIN (2^{-11}).

Four-Quadrant Multiplication

The MAX530 can be used as a four-quadrant multiplier by connecting ROFS to REFIN and RFB to VOUT and, using (1) an offset binary digital code, (2) bipolar power supplies, and (3) a bipolar analog input at REFIN within the range V_{SS} + 2V to V_{DD} - 2V, as shown in Figure 12.

In general, a 12-bit DAC's output is $(D)(V_{REFIN})(G)$, where "G" is the gain (1 or 2) and "D" is the binary representation of the digital input divided by 2^{12} or 4,096. This formula is precise for unipolar operation. However, for bipolar, offset binary operation, the MSB is really a polarity bit. No resolution is lost, because there is the same number of steps. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V (G = 2) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. The negative full scale is $-V_{REFIN}$, while the positive full scale is $+V_{REFIN}$ - 1LSB.

Table 5. Bipolar (Offset Binary) Code Table ($-V_{REFIN}$ to $+V_{REFIN}$ Output)

INPUT	OUTPUT
1111 1111 1111	$(+V_{REFIN})\frac{2047}{2048}$
1000 0000 0001	$(+V_{REFIN})\frac{1}{2048}$
1000 0000 0000	0V
0111 1111 1111	$(-V_{REFIN})\frac{1}{2048}$
0000 0000 0001	$(-V_{REFIN})\frac{2047}{2048}$
0000 0000 0000	$(-V_{REFIN})\frac{2048}{2048} = -V_{REFIN}$

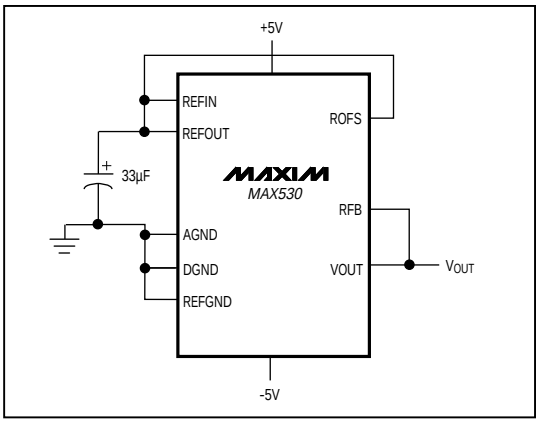


Figure 11. Bipolar Configuration (-2.048V to +2.048V Output)

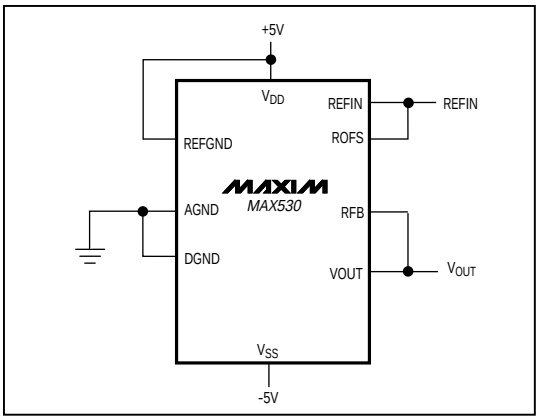


Figure 12. Four-Quadrant Multiplying Circuit

Applications Information

Single-Supply Linearity

As with any amplifier, the MAX530's output op amp offset can be positive or negative. When the offset is positive, it is easily accounted for. However, when the offset is negative, the output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive. The resulting transfer function is shown in Figure 13.

Normally, linearity is measured after allowing for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. In the MAX530, linearity and gain error are measured from code 11 to code 4095 (see Note 2 under *Electrical Characteristics*). The output amplifier offset does not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 4095.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

AGND and REFGND should be connected together, and then to DGND at the chip. For single-supply applications, connect V_{SS} to AGND at the chip. The best ground connection may be achieved by connecting the AGND, REFGND, and DGND pins together and connecting that point to the system analog ground plane. If DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass V_{DD} (and V_{SS} in dual-supply mode) with a 0.1µF ceramic capacitor connected between V_{DD} and AGND (and between V_{SS} and AGND). Mount the capacitors with short leads close to the device.

AC Considerations

Digital Feedthrough

High-speed data at any of the digital input pins may couple through the DAC package and cause internal stray capacitance to appear as noise at the DAC output, even though $\overline{LDAC}$ and $\overline{CS}$ are held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding $\overline{LDAC}$ and $\overline{CS}$ high and toggling the data inputs from all 1s to all 0s.

Analog Feedthrough

Because of internal stray capacitance, higher-frequency analog input signals at REFIN may couple to the output, even when the input digital code is all 0s, as shown in the *Typical Operating Characteristics* graph Analog Feedthrough vs. Frequency. It is tested by setting $\overline{CLR}$ to low (which sets the DAC latches to all 0s) and sweeping REFIN.

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

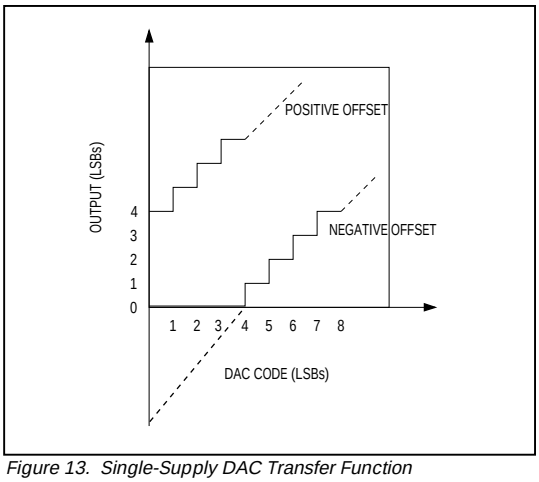
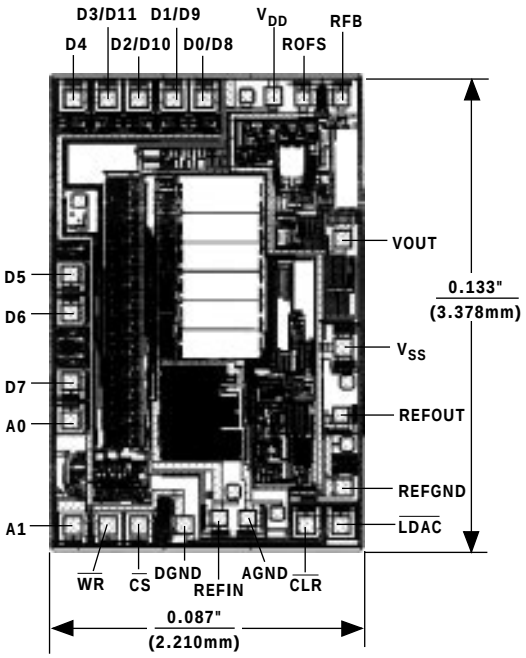


Figure 13. Single-Supply DAC Transfer Function

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX530AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX530BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX530AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX530BEWG	-40°C to +85°C	24 Wide SO	±1
MAX530AEAG	-40°C to +85°C	24 SSOP	±1/2
MAX530BEAG	-40°C to +85°C	24 SSOP	±1

_Chip Topography



TRANSISTOR COUNT: 913;
SUBSTRATE CONNECTED TO V_{DD}.