ADC0820-N 8-Bit High Speed µP Compatible A/D Converter with Track/Hold Function

Check for Samples: ADC0820-N

FEATURES

- **Built-In Track-and-Hold Function**
- **No Missing Codes**
- **No External Clocking**
- **Single Supply—5 V_{DC}**
- **Easy Interface to All Microprocessors, or Operates Stand-Alone**
- **Latched TRI-STATE Output**
- **Logic Inputs and Outputs Meet Both MOS and T^2L Voltage Level Specifications**
- **Operates Ratiometrically or with any Reference Value Equal to or Less than V_{CC}**
- **0V to 5V Analog Input Voltage Range with Single 5V Supply**
- **No Zero or Full-Scale Adjust Required**
- **Overflow Output Available for Cascading**
- **0.3 in. Standard Width 20-Pin PDIP**
- **20-Pin PLCC**
- **20-Pin SOIC**

KEY SPECIFICATIONS

- **Resolution: 8 Bits**
- **Conversion Time**
  - **2.5 µs Max (RD Mode)**
  - **1.5 µs Max (WR-RD Mode)**
- **Low Power: 75 mW Max**
- **Total Unadjusted Error: ±½ LSB and ± 1 LSB**

DESCRIPTION

By using a half-flash conversion technique, the 8-bit ADC0820-N CMOS A/D offers a 1.5 µs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820-N is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/µs.

For ease of interface to microprocessors, the ADC0820-N has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Datasheet.Directory

Connection and Functional Diagrams

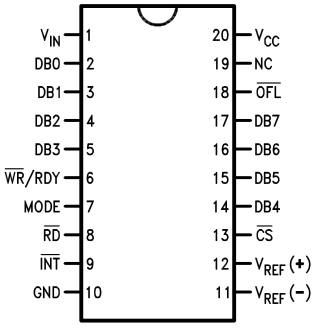

Figure 1. CDIP, PDIP, and SOIC Packages (Top View)

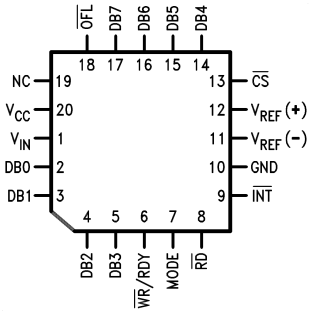

Figure 2. PLCC Package

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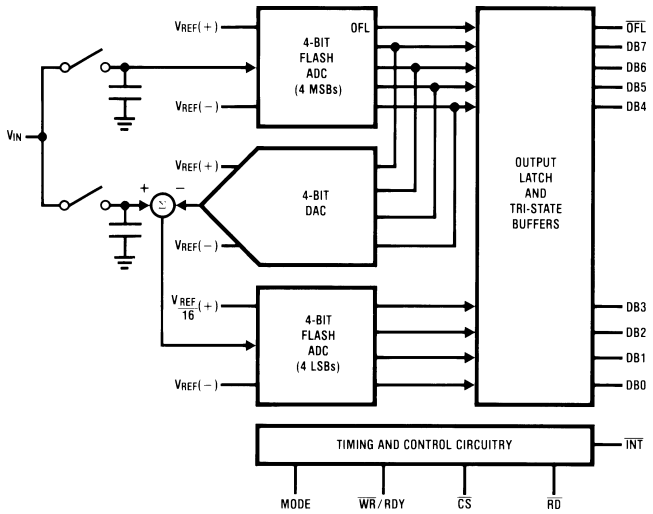

Figure 3. Functional Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)(3)]

Supply Voltage (V_{CC})			10V
Logic Control Inputs			−0.2V to V_{CC} +0.2V
Voltage at Other Inputs and Output			−0.2V to V_{CC} +0.2V
Storage Temperature Range			−65°C to +150°C
Package Dissipation at T_A = 25°C			875 mW
Input Current at Any Pin[(4)]			1 mA
Package Input Current[(4)]			4 mA
ESD Susceptibility[(5)]			900V
Lead Temp. (Soldering, 10 sec.)	PDIP Package		260°C
	CDIP Package		300°C
	SOIC Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(2) All voltages are measured with respect to the GND pin, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.
(5) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Ratings[(1)(2)]

Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	ADC0820CCJ, ADC0820CIWM	$-40°C \le T_A \le +85°C$
	ADC0820BCN, ADC0820CCN, ADC0820BCV, ADC0820BCWM, ADC0820CCWM	$0°C \le T_A \le 70°C$
V_{CC} Range		4.5V to 8V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(2) All voltages are measured with respect to the GND pin, unless otherwise specified.

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Converter Characteristics

The following specifications apply for RD mode (pin 7 = 0), V_{CC} = 5V, $V_{REF}(+)$ = 5V,and $V_{REF}(-)$ = GND unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC0820CCJ			ADC0820BCN, ADC0820CCN, ADC0820BCV, ADC0820BCWM, ADC0820CCWM, ADC0820CIWM			Limit Units
		Typ (1)	Tested Limit (2)	Design Limit (3)	Typ (1)	Tested Limit (2)	Design Limit (3)	
Resolution			**8**			8	**8**	Bits
Total Unadjusted Error (4)	ADC0820BCN, BCWM					±½	**±½**	LSB
	ADC0820CCJ		**±1**					LSB
	ADC0820CCN, CCWM, CIWM					±1	**±1**	LSB
	ADC0820CCMSA					±1	**±1**	LSB
Minimum Reference Resistance		2.3	**1.00**		2.3	1.2		kΩ
Maximum Reference Resistance		2.3	**6**		2.3	5.3	**6**	kΩ
Maximum $V_{REF}(+)$ Input Voltage			**V_{CC}**			V_{CC}	**V_{CC}**	V
Minimum $V_{REF}(-)$ Input Voltage			**GND**			GND	**GND**	V
Minimum $V_{REF}(+)$ Input Voltage			**$V_{REF}(-)$**			$V_{REF}(-)$	**$V_{REF}(-)$**	V
Maximum $V_{REF}(-)$ Input Voltage			**$V_{REF}(+)$**			$V_{REF}(+)$	**$V_{REF}(+)$**	V
Maximum V_{IN} Input Voltage			**V_{CC}+0.1**			V_{CC}+0.1	**V_{CC}+0.1**	V
Minimum V_{IN} Input Voltage			**GND−0.1**			GND−0.1	**GND−0.1**	V
Maximum Analog Input Leakage Current	$\overline{CS}$ =V_{CC}							
	V_{IN}=V_{CC}		**3**			0.3	**3**	µA
	V_{IN}=GND		**−3**			−0.3	**−3**	µA
Power Supply Sensitivity	V_{CC}=5V±5%	±1/16	**±¼**		±1/16	±¼	**±¼**	LSB

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(3) Design limits are specified but not 100% tested. These limits are not used to calculate outgoing quality levels.
(4) Total unadjusted error includes offset, full-scale, and linearity errors.

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DC Electrical Characteristics

The following specifications apply for V_{CC} = 5V, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_J$ = 25°C.

Parameter	Conditions		ADC0820CCJ			ADC0820BCN, ADC0820CCN, ADC0820BCV, ADC0820BCWM, ADC0820CCWM, ADC0820CIWM			Limit Units
			Typ (1)	Tested Limit (2)	Design Limit (3)	Typ (1)	Tested Limit (2)	Design Limit (3)	
$V_{IN(1)}$, Logical "1" Input Voltage	V_{CC}=5.25V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**2.0**			2.0	**2.0**	V
		Mode		**3.5**			3.5	**3.5**	V
$V_{IN(0)}$, Logical "0" Input Voltage	V_{CC}=4.75V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**0.8**			0.8	**0.8**	V
		Mode		**1.5**			1.5	**1.5**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN(1)}$=5V; $\overline{CS}$, $\overline{RD}$		0.005	**1**		0.005		**1**	µA
	$V_{IN(1)}$=5V; $\overline{WR}$		0.1	**3**		0.1	0.3	**3**	µA
	$V_{IN(1)}$=5V; Mode		50	**200**		50	170	**200**	µA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN(0)}$=0V; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−0.005	**−1**		−0.005		**−1**	µA
$V_{OUT(1)}$, Logical "1" Output Voltage	V_{CC}=4.75V, I_{OUT}=−360 µA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**2.4**			2.8	**2.4**	V
	V_{CC}=4.75V, I_{OUT}=−10 µA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**4.5**			4.6	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	V_{CC}=4.75V, I_{OUT}=1.6 mA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY			**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current	V_{OUT}=5V; DB0–DB7, RDY		0.1	**3**		0.1	0.3	**3**	µA
	V_{OUT}=0V; DB0–DB7, RDY		−0.1	**−3**		−0.1	−0.3	**−3**	µA
I_{SOURCE}, Output Source Current	V_{OUT}=0V; DB0–DB7, $\overline{OFL}$		−12	**−6**		−12	−7.2	**−6**	mA
	$\overline{INT}$		−9	**−4.0**		−9	−5.3	**−4.0**	mA
I_{SINK}, Output Sink Current	V_{OUT}=5V; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		14	**7**		14	8.4	**7**	mA
I_{CC}, Supply Current	$\overline{CS}$ =$\overline{WR}$ =$\overline{RD}$ =0		7.5	**15**		7.5	13	**15**	mA

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(3) Design limits are specified but not 100% tested. These limits are not used to calculate outgoing quality levels.

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AC Electrical Characteristics

The following specifications apply for V_{CC} = 5V, $t_r = t_f$ = 20 ns, $V_{REF}(+)$ = 5V, $V_{REF}(-)$ = 0V and T_A = 25°C unless otherwise specified.

Parameter		Conditions	Typ(1)	Tested Limit(2)	Design Limit(3)	Units
t_{CRD}, Conversion Time for RD Mode		Pin 7 = 0 (Figure 4)	1.6		2.5	µs
t_{ACC0}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = 0 (Figure 4)	t_{CRD} + 20		t_{CRD} + 50	ns
t_{CWR-RD}, Conversion Time for WR-RD Mode		Pin 7 = V_{CC}; t_{WR} = 600 ns, t_{RD}=600 ns (Figure 5 & Figure 6)			1.52	µs
t_{WR}, Write Time	Min	Pin 7 = V_{CC} (Figure 5 & Figure 6)		600		ns
	Max	Figure 11(4)	50			µs
t_{RD}, Read Time	Min	Pin 7 = V_{CC} (Figure 5 & Figure 6 & Figure 12)(4)		600		ns
t_{ACC1}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD} < t_I$, C_L = 15pF (Figure 5)	190		280	ns
		C_L = 100 pF	210		320	ns
t_{ACC2}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD} > t_I$, C_L = 15pF (Figure 6)	70		120	ns
		C_L=100 pF	90		150	ns
t_{ACC3}, Access Time (Delay from Rising Edge of RDY to Output Valid)		R_{PULLUP} = 1k and C_L = 15 pF	30			ns
t_I, Internal Comparison Time		Pin 7 = V_{CC}, C_L = 50pF (Figure 6 & Figure 7)	800		1300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)		R_L = 1k, C_L = 10 pF	100		200	ns
$t_{\overline{INTL}}$, Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$		Pin 7 = V_{CC}, C_L = 50 pF $t_{RD} > t_I$ (Figure 6)			t_I	ns
		$t_{RD} < t_I$ (Figure 5)	t_{RD}+200		t_{RD}+290	ns
$t_{\overline{INTH}}$, Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$		C_L = 50pF (Figure 4 & Figure 5 & Figure 6)	125		225	ns
$t_{\overline{INTHWR}}$, Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$		CL = 50pF (Figure 7)	175		270	ns
t_{RDY}, Delay from $\overline{CS}$ to RDY		C_L = 50 pF, Pin 7 = 0 (Figure 4)	50		100	ns
t_{ID}, Delay from $\overline{INT}$ to Output Valid		See Figure 7	20		50	ns
t_{RI}, Delay from $\overline{RD}$ to $\overline{INT}$		Pin 7 = V_{CC}, $t_{RD}<t_I$ Figure 5	200		290	ns
t_P, Delay from End of Conversion to Next Conversion		(Figure 4 & Figure 5 & Figure 6 & Figure 7 & Figure 13)(4)			500	ns
Slew Rate, Tracking			0.1			V/µs
C_{VIN}, Analog Input Capacitance			45			pF
C_{OUT}, Logic Output Capacitance			5			pF
C_{IN}, Logic Input Capacitance			5			pF

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(3) Design limits are specified but not 100% tested. These limits are not used to calculate outgoing quality levels.
(4) Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Figure 11 and Figure 12 graphs.

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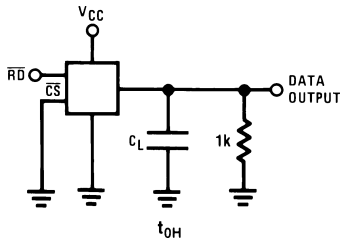
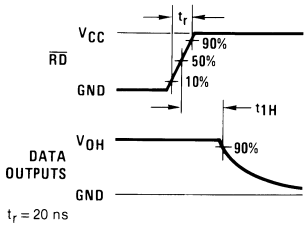
TRI-STATE Test Circuits and Waveforms

t_r=20 ns

t_{1H} Circuit

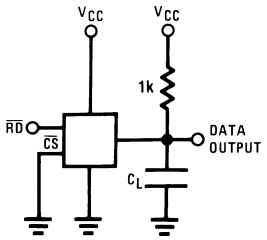


t_{1H} Waveform

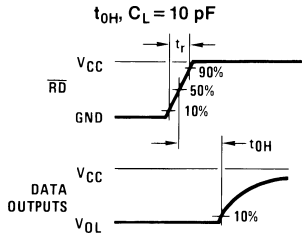


t_r=20 ns

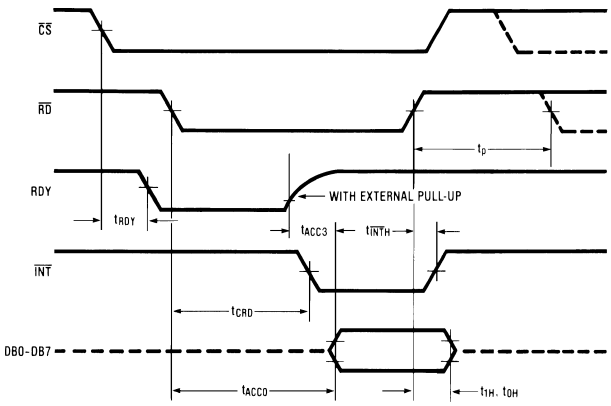
t_{0H} Circuit



t_{0H} Waveform



Timing Diagrams



Note: On power-up the state of $\overline{INT}$ can be high or low.

Figure 4. RD Mode (Pin 7 is Low)

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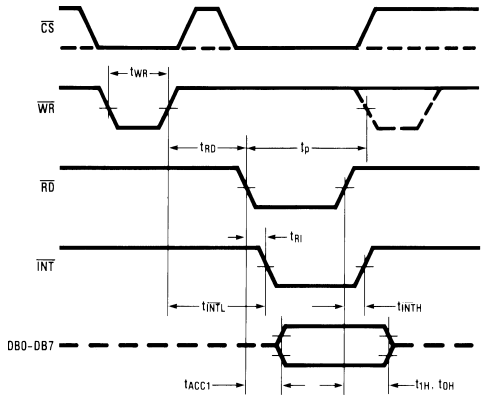

Figure 5. WR-RD Mode (Pin 7 is High and $t_{RD}<t_I$)

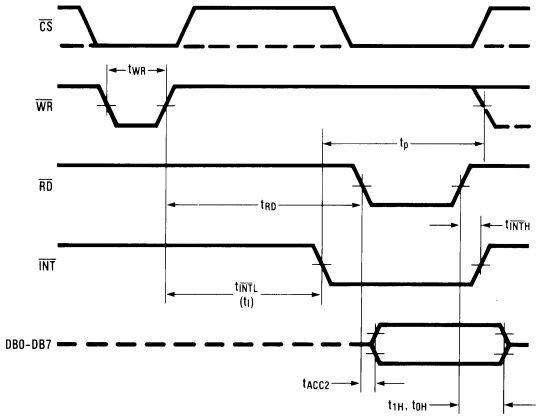

Figure 6. WR-RD Mode (Pin 7 is High and $t_{RD}>t_I$)

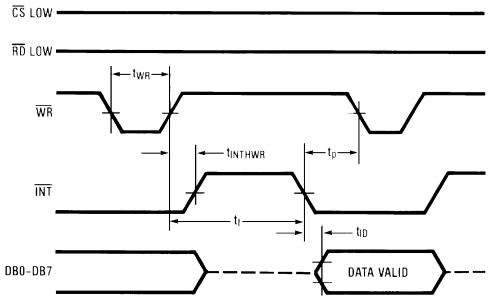

Figure 7. WR-RD Mode (Pin 7 is High)
Stand-Alone Operation

Typical Performance Characteristics

Logic Input Threshold Voltage vs. Supply Voltage

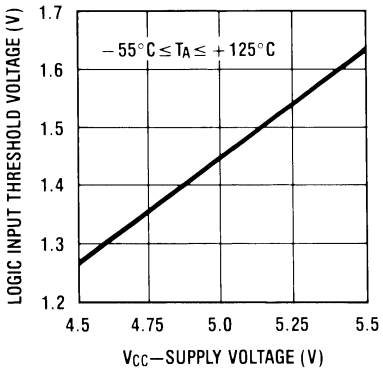

Figure 8.

Conversion Time (RD Mode) vs. Temperature

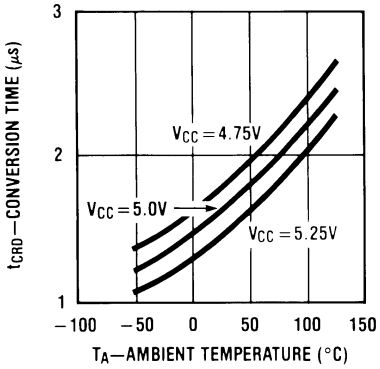

Figure 9.

Power Supply Current vs. Temperature (not including reference ladder)

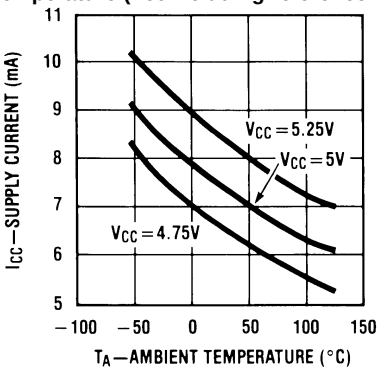

Figure 10.

Accuracy vs. t_{WR}

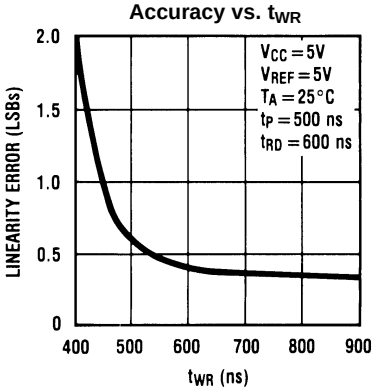

Figure 11.

Accuracy vs. t_{RD}

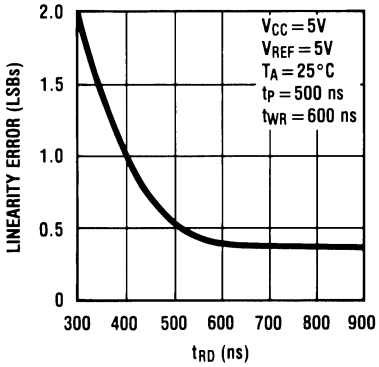

Figure 12.

Accuracy vs. t_p

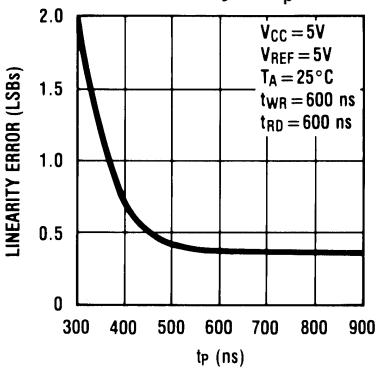

Figure 13.

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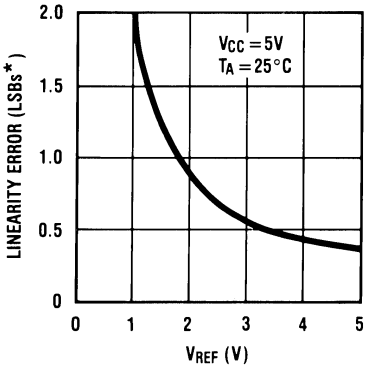
Typical Performance Characteristics (continued)

Accuracy vs. V_{REF} [$V_{REF}=V_{REF}(+)-V_{REF}(-)$]



$*1\ LSB = \frac{V_{REF}}{256}$

Figure 14.

t_I, Internal Time Delay vs. Temperature

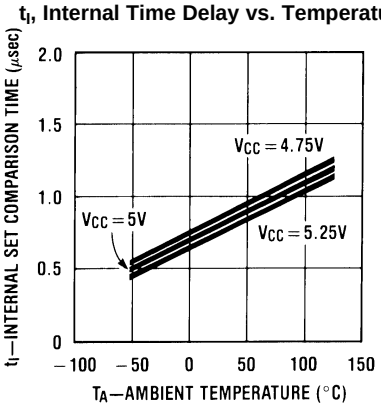


Figure 15.

Output Current vs. Temperature

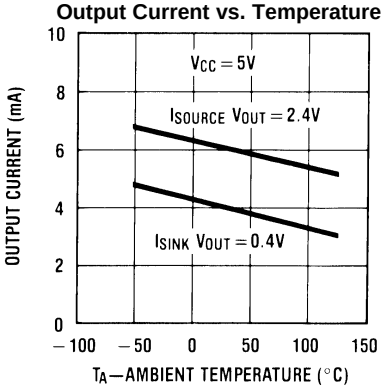


Figure 16.

PIN DESCRIPTIONS

Pin	Name	Function	
1	V_{IN}	Analog input; range =GND≤V_{IN}≤V_{CC}	
2	DB0	TRI-STATE data output—bit 0 (LSB)	
3	DB1	TRI-STATE data output—bit 1	
4	DB2	TRI-STATE data output—bit 2	
5	DB3	TRI-STATE data output—bit 3	
6	$\overline{WR}$ / RDY	**WR-RD Mode**	**$\overline{WR}$:** With $\overline{CS}$ low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800 ns (the preset internal time out, t_I) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (See Figure 5 & Figure 6).
		RD Mode	**RDY:** This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (See Figure 4).
7	Mode	**Mode:** Mode selection input—it is internally tied to GND through a 50 µA current source.	
		RD Mode: When mode is low	
		WR-RD Mode: When mode is high	
8	$\overline{RD}$	**WR-RD Mode**	With $\overline{CS}$ low, the TRI-STATE data outputs (DB0-DB7) will be activated when $\overline{RD}$ goes low (See Figure 7). $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (t_I, ~800 ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (See Figure 5 & Figure 6).
		RD Mode	With $\overline{CS}$ low, the conversion will start with $\overline{RD}$ going low, also $\overline{RD}$ will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and $\overline{INT}$ going low indicates the completion of the conversion (See Figure 4).
9	$\overline{INT}$	**WR-RD Mode**	$\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go low, ~800 ns (the preset internal time out, t_I) after the rising edge of $\overline{WR}$ (See Figure 6); or $\overline{INT}$ will go low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes low prior to the 800 ns time out (See Figure 5). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (See Figure 5 & Figure 6).
		RD Mode	$\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (See Figure 4).
10	GND	Ground	
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: GND≤$V_{REF}(-)$≤$V_{REF}(+)$ (1)	
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-)$≤$V_{REF}(+)$≤V_{CC} (1)	
13	$\overline{CS}$	$\overline{CS}$ must be low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.	
14	DB4	TRI-STATE data output—bit 4	
15	DB5	TRI-STATE data output—bit 5	
16	DB6	TRI-STATE data output—bit 6	
17	DB7	TRI-STATE data output—bit 7 (MSB)	
18	$\overline{OFL}$	Overflow output—If the analog input is higher than the $V_{REF}(+)$, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit). This output is always active and does not go into TRI-STATE as DB0–DB7 do.	
19	NC	No connection	
20	V_{CC}	Power supply voltage	

(1) When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.

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FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The ADC0820-N uses two 4-bit flash A/D converters to make an 8-bit measurement (Figure 3). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the “sampled-data” comparators used in the ADC0820-N provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

THE SAMPLED-DATA COMPARATOR

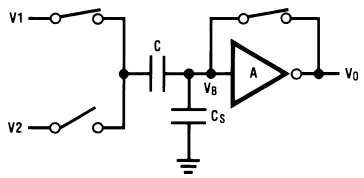
Each comparator in the ADC0820-N consists of a CMOS inverter with a capacitively coupled input (Figure 17 Figure 18). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (Figure 17) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_B, approximately 1.2V). In the second cycle (Figure 18), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input (V_B') becomes

$$V_B - (V1 - V2)\frac{C}{C + C_S} \tag{1}$$

and the output will go high or low depending on the sign of $V_B' - V_B$.

The actual circuitry used in the ADC0820-N is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (Figure 19), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor and opening all of the other switches (S switches). The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.



- $V_O = V_B$
- V on C = $V1 - V_B$
- C_S = stray input node capacitor
- V_B = inverter input bias voltage

Zeroing Phase

Figure 17. Sampled-Data Comparator

Compare Phase

$$\bullet V_B' - V_B = (V2 - V1)\frac{C}{C + C_S}$$

$$\bullet V_O' = \frac{-A}{C + C_S}[CV2 - CV1]$$

$\bullet V_O'$ is dependent on $V2 - V1$

Figure 18. Sampled-Data Comparator

$$V_O = \frac{-A}{C1 + C2 + C_S}[C1(V2 - V1) + C2(V4 - V3)]$$

$$= \frac{-A}{C1 + C2 + C_S}[\Delta Q_{C1} + \Delta Q_{C2}]$$

Figure 19. ADC0820-N Comparator (from MS Flash ADC)

ARCHITECTURE

In the ADC0820-N, one bank of 15 comparators is used in each 4-bit flash A/D converter (Figure 25). The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.

When a typical conversion is started, the $\overline{WR}$ line is brought low. At this instant the MS comparators go from zeroing to comparison mode (Figure 24). When $\overline{WR}$ is returned high after at least 600 ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600 ns later, the $\overline{RD}$ line may be pulled low to latch the lower 4 data bits and finish the 8-bit conversion. When $\overline{RD}$ goes low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 24 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is low. In RD mode, sampling occurs during the first 800 ns of $\overline{RD}$. Because of the input connections to the ADC0820-N's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant (see Inherent Sample-Hold), despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is low the MS flash is in compare mode (connected to V_{IN}), and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

DIGITAL INTERFACE

The ADC0820-N has two basic interface modes which are selected by strapping the MODE pin high or low.

RD Mode

With the MODE pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ low until output data appears. An $\overline{INT}$ line is provided which goes low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

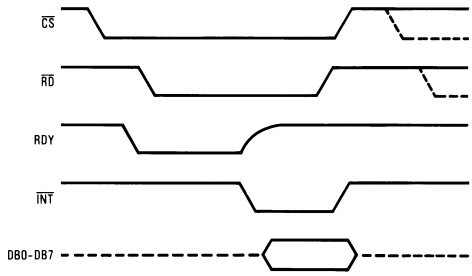


Figure 20. RD Mode (Pin 7 is Low)

When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800 ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800 ns, the lower 4 bits are recovered.

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WR then RD Mode

With the MODE pin tied high, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt driven scheme is desired, the user can wait for $\overline{INT}$ to go low before reading the conversion result (Figure 22). $\overline{INT}$ will typically go low 800 ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 600 ns (Figure 21). If this is done, $\overline{INT}$ will immediately go low and data will appear at the outputs.

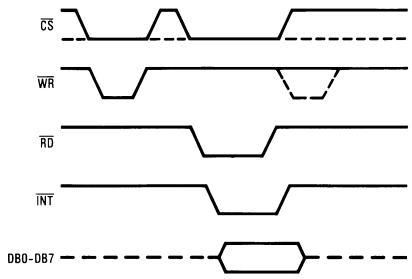


Figure 21. WR-RD Mode (Pin 7 is High and $t_{RD}<t_I$)

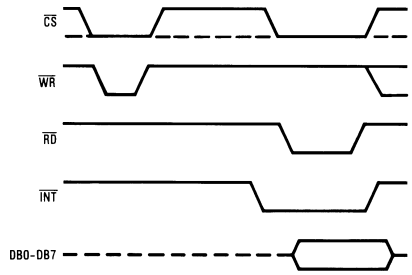


Figure 22. WR-RD Mode (Pin 7 is High and $t_{RD}>t_I$)

Stand-Alone

For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800 ns following $\overline{WR}$'s rising edge.

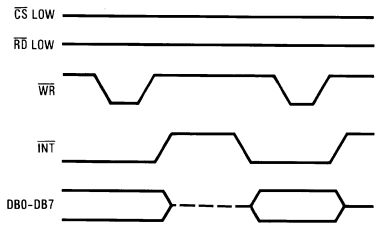
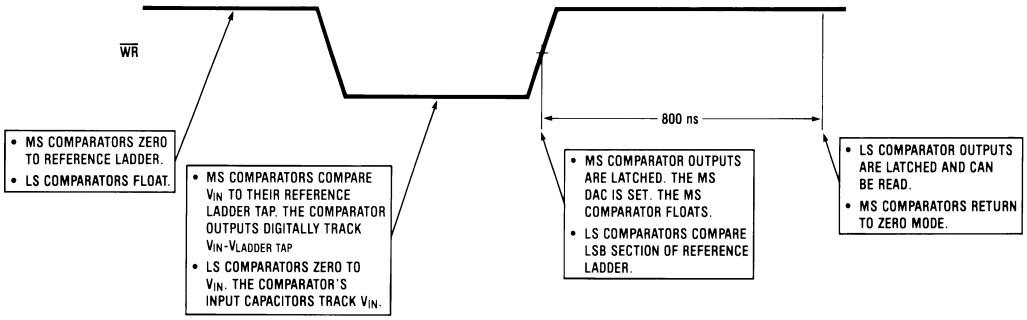


Figure 23. WR-RD Mode (Pin 7 is High) Stand-Alone Operation



Note: MS means most significant
LS means least significant

Figure 24. Operating Sequence (WR-RD Mode)

OTHER INTERFACE CONSIDERATIONS

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50 µs. When the MS flash ADC's sampled-data comparators (see The Sampled-Data Comparator) are in comparison mode ($\overline{WR}$ is low), the input capacitors (C, Figure 19) must hold their charge. Switch leakage and inverter bias current can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion (see Architecture), a new conversion cannot be started until this phase is complete. The minimum spec for this time (t_P, see Figure 4 & Figure 5 & Figure 6 & Figure 7) is 500 ns.

Detailed Block Diagram

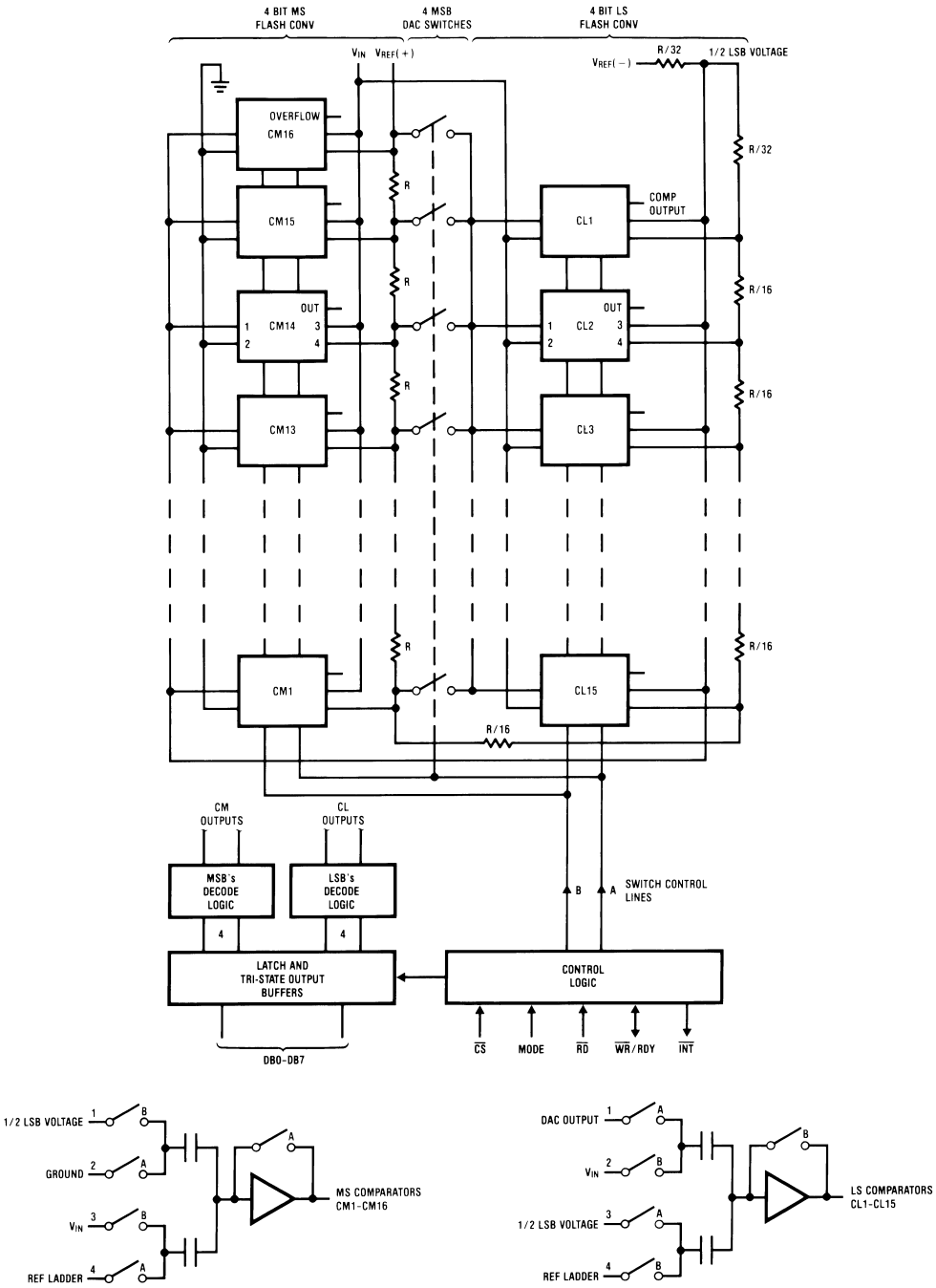


Figure 25.

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Analog Considerations

REFERENCE AND INPUT

The two V_{REF} inputs of the ADC0820-N are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing V_{REF}(V_{REF} = $V_{REF}(+) - V_{REF}(-)$) to less than 5V, the sensitivity of the converter can be increased (i.e., if V_{REF} = 2V then 1 LSB = 7.8 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. Figure 26 shows some of the configurations that are possible.

INPUT CURRENT

Due to the unique conversion techniques employed by the ADC0820-N, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820-N is shown in Figure 27. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, connecting V_{IN} to thirty-one 1 pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase (see Architecture). In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5 kΩ to 10 kΩ). In addition, about 12 pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in Figure 28. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800 ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is low. Since other factors force this time to be at least 600 ns, input time constants of 100 ns can be accommodated without special consideration. Typical total input capacitance values of 45 pF allow R_S to be 1.5 kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

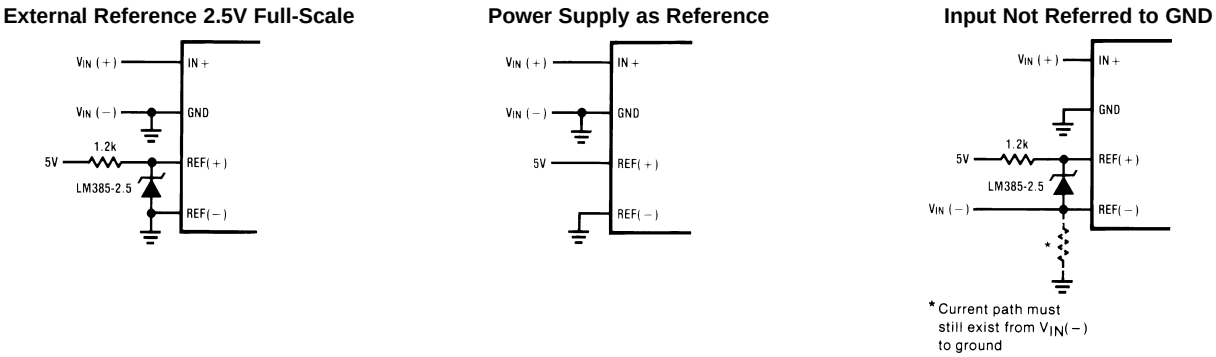

Figure 26. Analog Input Options

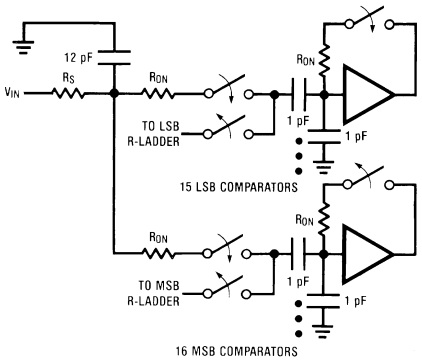

Figure 27. ADC0820-N Input Circuit

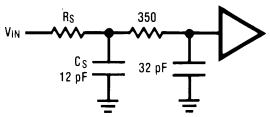

Figure 28. Analog Input, RC Network Model

INPUT FILTERING

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect the ADC0820-n does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600 ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal.

INHERENT SAMPLE-HOLD

Another benefit of the ADC0820-N's input mechanism is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least ½ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled-data comparators, by nature of their input switching, already accomplish this function to a large degree (see The Sampled Data Comparator). Although the conversion time for the ADC0820-N is 1.5 µs, the time through which V_{IN} must be ½ LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820-N only "samples" V_{IN} when $\overline{WR}$ is low (see Architecture and Input Current). Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100 ns after the rising edge of $\overline{WR}$ (100 ns due to internal logic prop delay) will be the measured value.

Input signals with slew rates typically below 100 mV/µs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820-N's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1 µs would still not be able to measure a 5V 1 kHz sine wave without the aid of an external sample-and-hold. The ADC0820-N, with no such help, can typically measure 5V, 7 kHz waveforms.

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Typical Applications

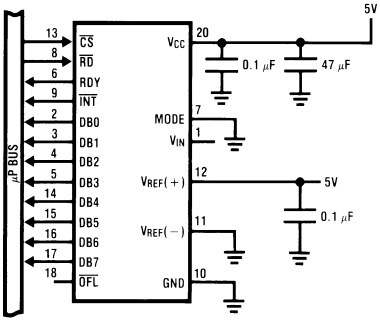

Figure 29. 8-Bit Resolution Configuration

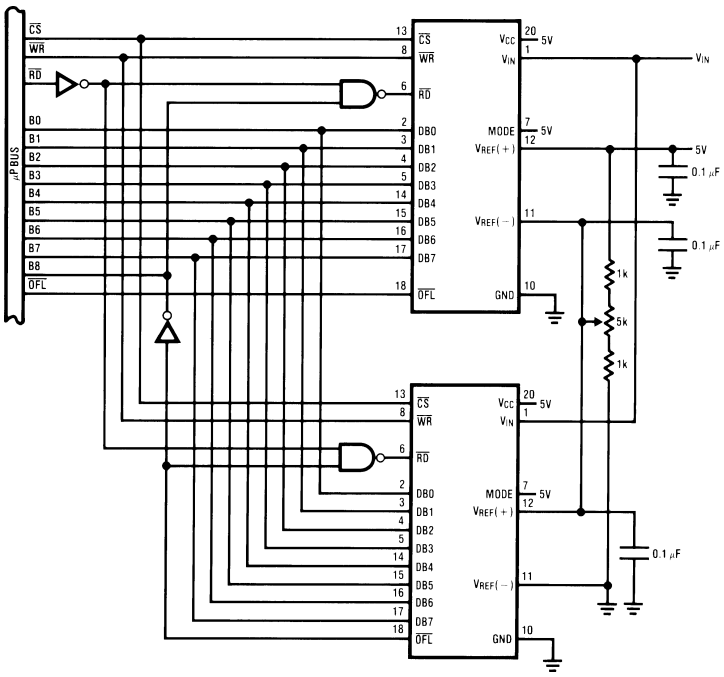

Figure 30. 9-Bit Resolution Configuration

- V_{IN}=3 kHz max ± 4V_P
- No track-and-hold needed
- Low power consumption

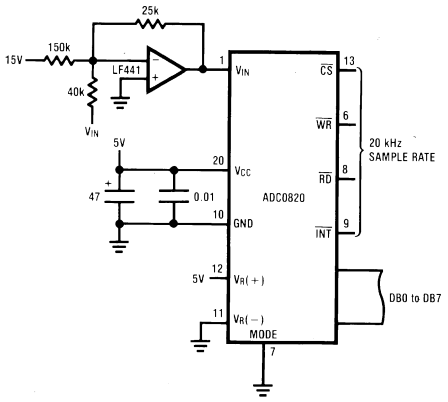

Figure 31. Telecom A/D Converter

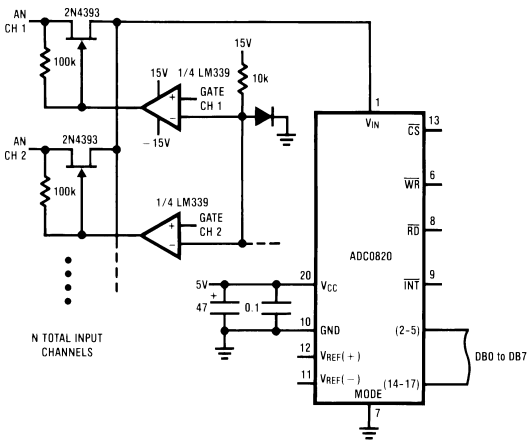

Figure 32. Multiple Input Channels

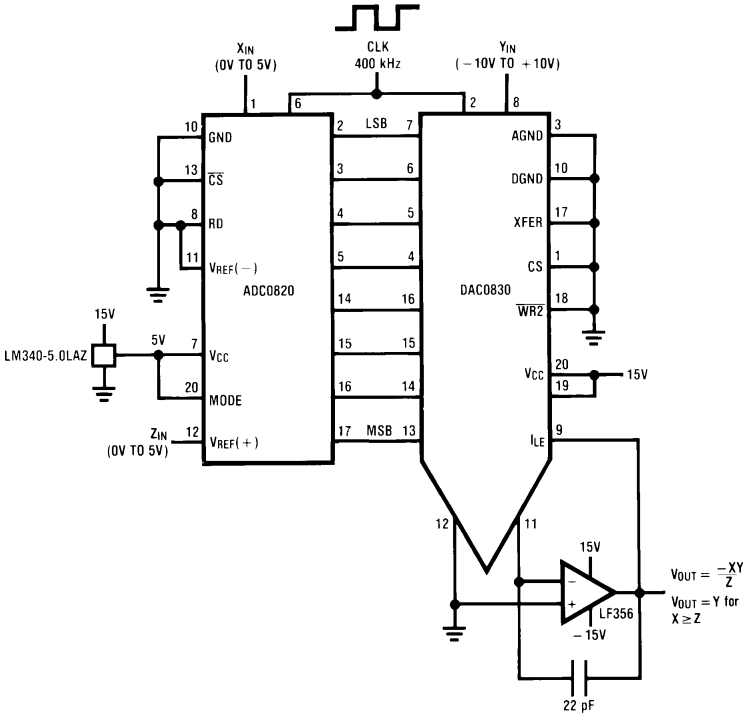

Figure 33. 8-Bit 2-Quadrant Analog Multiplier

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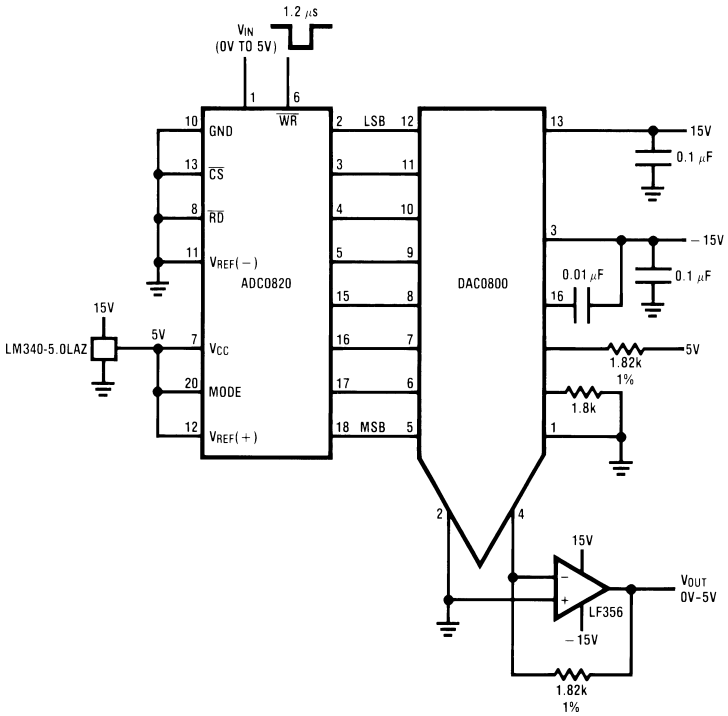

Figure 34. Fast Infinite Sample-and-Hold

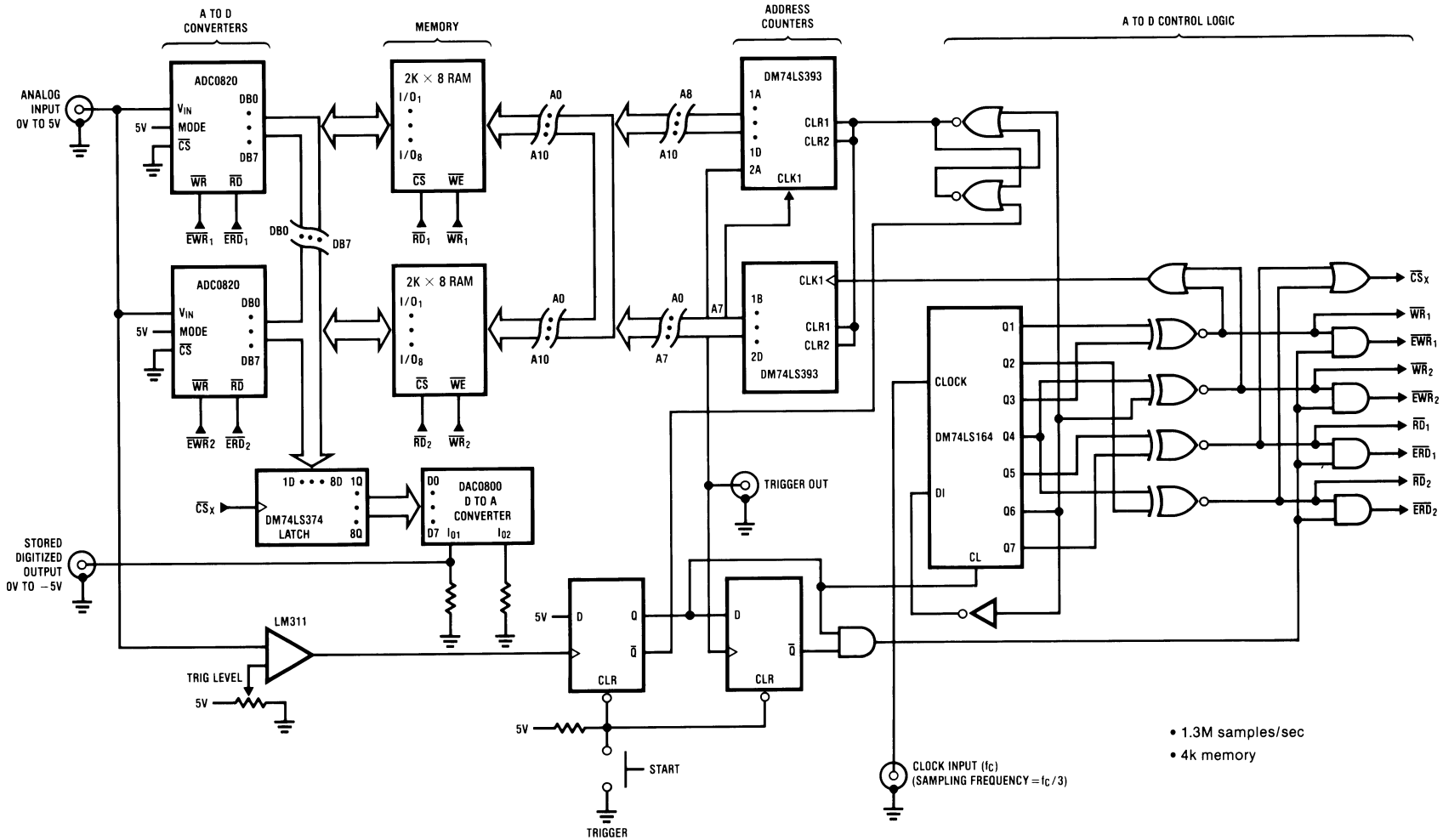

Figure 35. Digital Waveform Recorder

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REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC0820BCWMX/NOPB	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	SN | CU SN	Level-3-260C-168 HR	-40 to 85	ADC0820 BCWM	Samples
ADC0820CCN/NOPB	ACTIVE	PDIP	NFH	20	18	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	ADC0820CCN	Samples
ADC0820CCN/PB	NRND	PDIP	NFH	20	18	TBD	Call TI	Call TI		ADC0820CCN	
ADC0820CCWM	NRND	SOIC	DW	20	36	TBD	Call TI	Call TI	-40 to 85	ADC0820 CCWM	
ADC0820CCWM/NOPB	ACTIVE	SOIC	DW	20	36	Green (RoHS & no Sb/Br)	SN | CU SN	Level-3-260C-168 HR	-40 to 85	ADC0820 CCWM	Samples
ADC0820CCWMX/NOPB	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	SN | CU SN	Level-3-260C-168 HR	-40 to 85	ADC0820 CCWM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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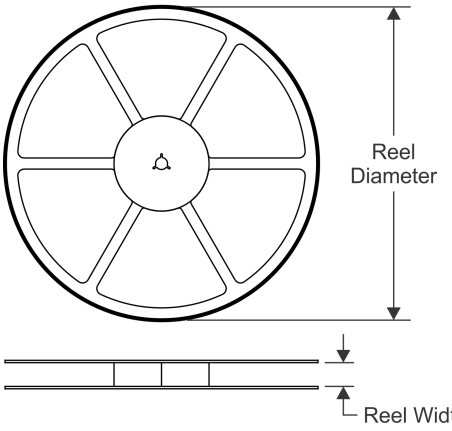
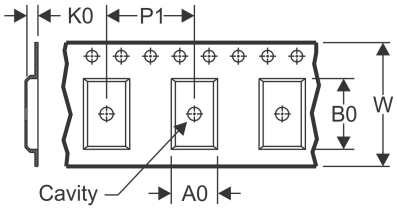
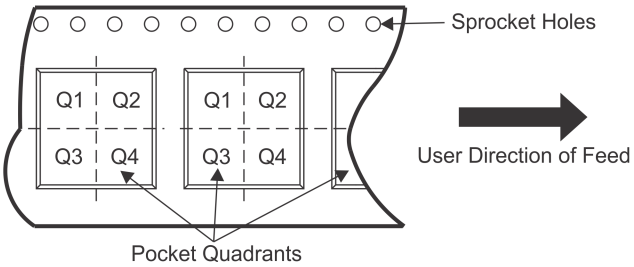


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

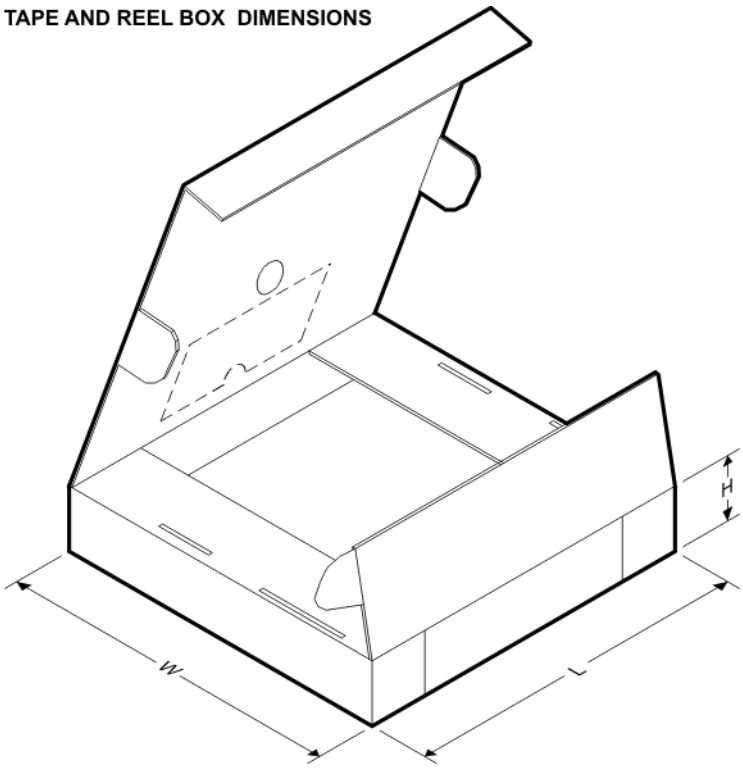
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC0820BCWMX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1
ADC0820CCWMX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1

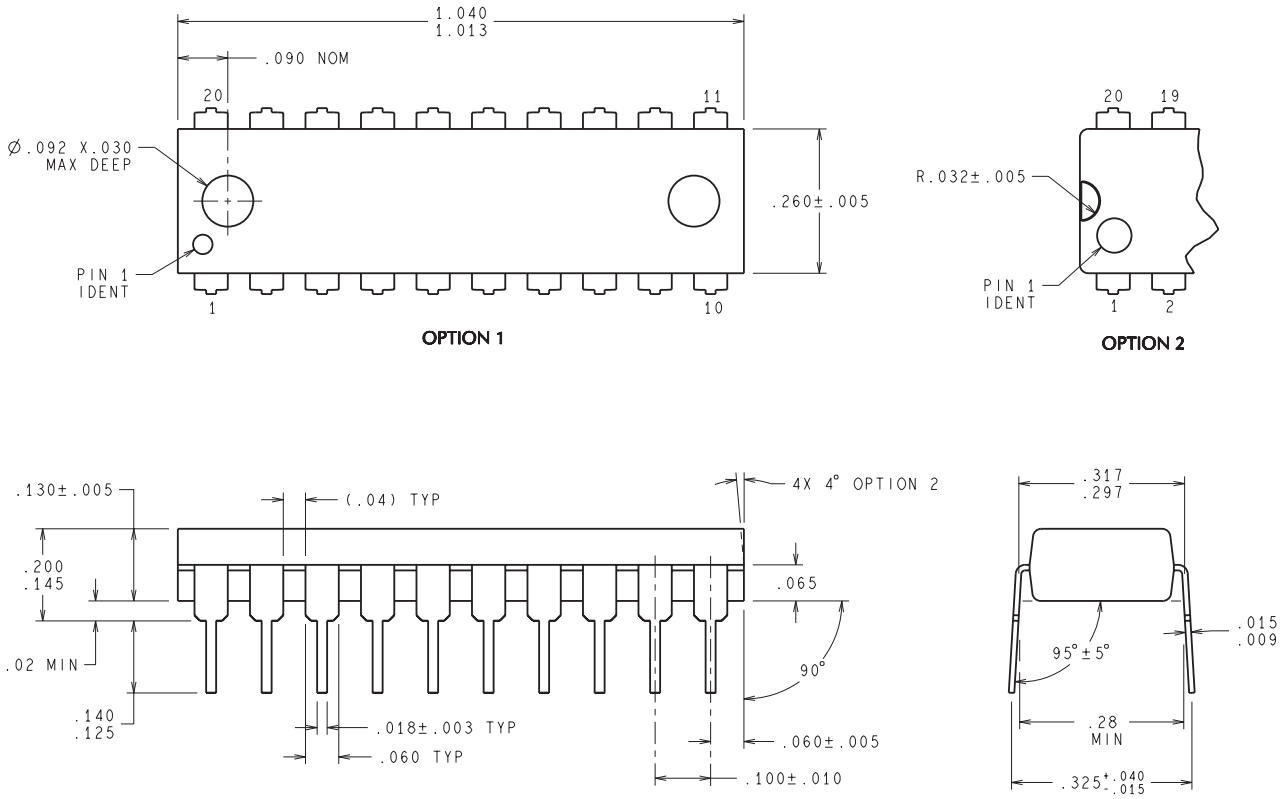
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

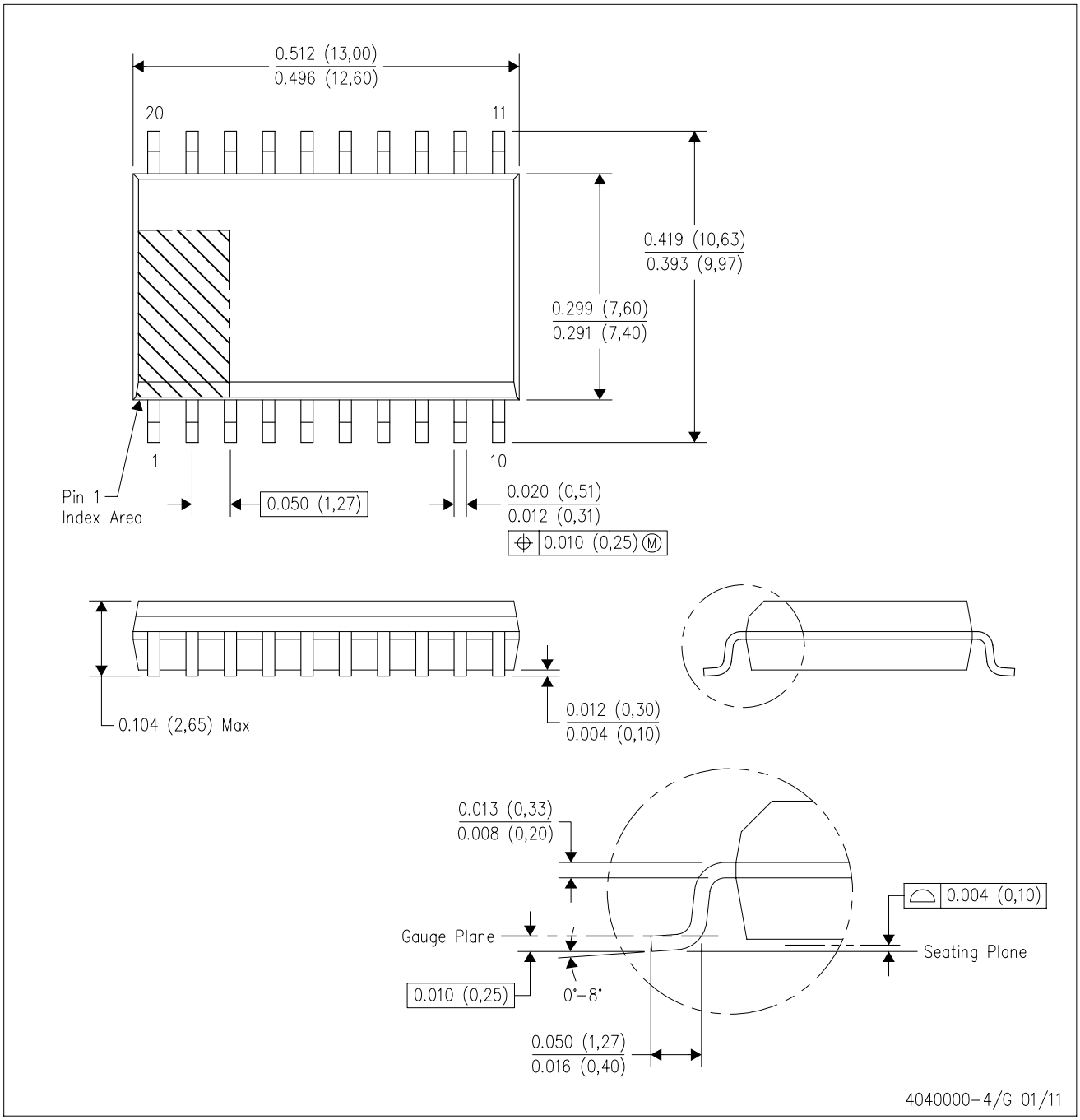
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC0820BCWMX/NOPB	SOIC	DW	20	1000	367.0	367.0	45.0
ADC0820CCWMX/NOPB	SOIC	DW	20	1000	367.0	367.0	45.0

NFH0020A



N20A (Rev G)

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

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