Application Report
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Solving Noise Problems Using Low Voltage Differential Signaling

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ABSTRACT

This report analyzes the use of low-voltage differential signaling (LVDS) to solve noise problems that affect the transmission of low-power data. This is accomplished through a discussion of the differential input advantages and an analysis of the signal-to-noise ratio benefits offered by the SN65LVDT2DBVR LVDS receiver.

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Introduction

The electronic transmission of data from one device to another has the problem of degraded or corrupted information being transmitted because of induced or generated noise. This is particularly an issue when using a high-speed, low-power transmission technique, which has become commonplace in the electronic industry today. This type of signaling technique uses signaling voltages much lower than 5 V, such as the levels defined in the differential standards of TIA/EIA-422B. Many of the problems associated with this low-voltage signaling, such as common-mode noise problems, have been addressed by the LVDS TIA/EIA-644 standard. This paper explains how LVDS can help solve such noise problems with a discussion of the differential input advantages and an analysis of the signal-to-noise ratio benefits of the SN65LVDT2DBVR LVDS receiver.

The Noise Solution

LVDS is a data transmission standard that utilizes low-voltage swings and a balanced interface to solve many of the problems associated with existing signaling technologies. Lower signal amplitudes shorten the output transition time and reduce the power used by line circuits. In addition, balanced differential signaling reduces noise coupling and allows higher signaling rates. Balanced means that the current flowing in each signal line is equal but opposite in direction, resulting in a field-canceling effect. This is one of the keys to the low-noise performance of an LVDS differential bus.

Basically, there are two main methods used in LVDS to address the noise problem: balanced differential input signals to eliminate induced noise with efficient common-mode rejection (CMR), and internal chip design techniques to reduce the noise generated by inductive and capacitive mutual coupling, thereby increasing signal integrity.

Test Procedure

The test procedure presented on this report demonstrates the common-mode rejection capability of the Texas Instruments LVDS receiver. The test uses the SN65LVDS1DBVR high-speed differential driver and the SN65LVDT2DBVR terminated high-speed differential receiver. One channel of the signal generator supplies a 100-Mbs input signal to the input of the SN65LVDS1DBVR driver. A second channel of the signal generator induces a ±2 Vp-p noise signal onto both of the differential input lines of the receiver. The test demonstrates that power/ground shifts, EMI, and crosstalk appear equally on each differential line.

Test Set-Up

The TIA/EIA-644 LVDS standard specifies the use of 90-Ω to 132-Ω transmission lines (although other values may also be used in nonstandard applications), and the one-meter cable used for this setup is a Belden-M DataTwist™ (stock number 1583A CM 4PR24) 100-Ω UTP CAT5. Figure 1 displays the circuit under consideration, with the transmission line being probed at the output of both the SN65LVDS1DBVR driver and the SN65LVDT2DBVR receiver.

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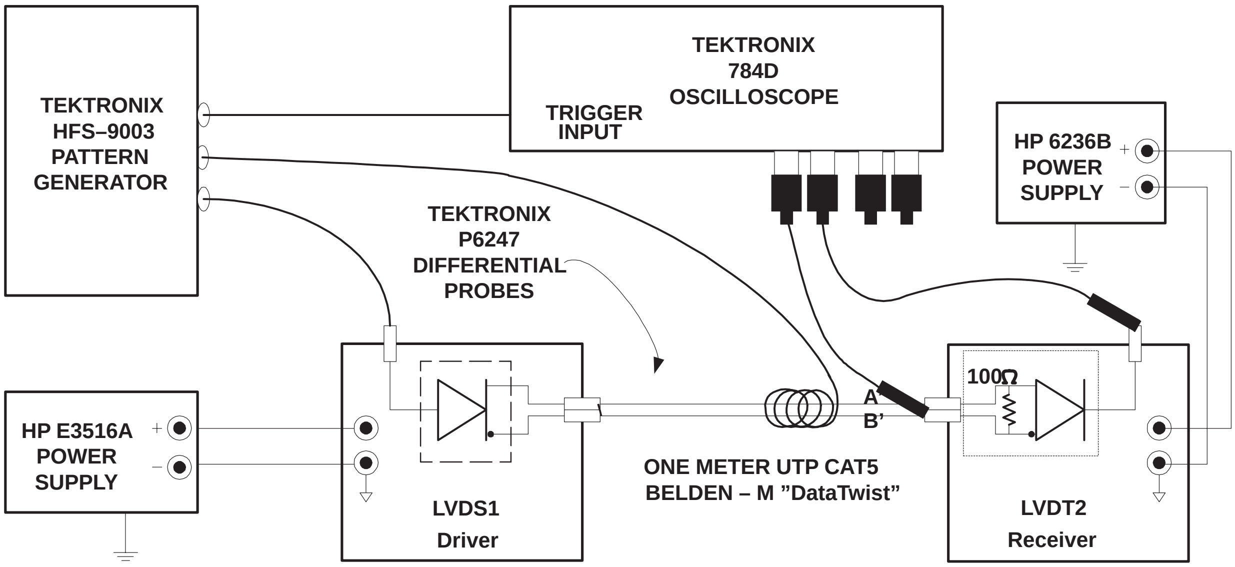

Figure 1. Test Setup

Test Equipment

A Tektronics PS2521G DC power supply provides the required 3.3-V to the LVDS driver and to the receiver in the circuit. A Tektronix HFS9003 signal generator is employed as a nonreturn-to-zero (NRZ), pseudo-random binary sequence (PRBS) signal source for the driver, and is adjusted for the balanced input as follows:

- Pattern: NRZ, PRBS
- Input high level: 2.0 V
- Input low level: 0.8 V
- Transition time: 800 ps

The influence of the equipment used to measure a signal of concern should be minimized at high signaling rates. A Tektronix 784D oscilloscope and Tektronix P6247 differential probes are used for differential tests. Each unit has a bandwidth of 1 GHz, and the probes have a capacitance of less than 1 pF. Individual Tektronix P6243 1-GHz probes are used to monitor each side of the differential output on the pulse input test.

Figure 2 shows the reference waveform, the LVDS signal, and the receiver output. Figure 3 shows the reference waveform with induced noise. Figures 3 and 4 clearly demonstrate the strong CMR capabilities of the SN65LVDT2DBVR receiver. Any issues arising from a concern over noise immunity of LVDS signals due to low-voltage swings (equal to ± 350-mV transitions, with ±100-mV thresholds) are automatically resolved, since the differential signals run close together in twisted pairs through controlled-impedance media. Obviously, much of the noise on the LVDS lines is common-mode noise and is rejected by the receiver.

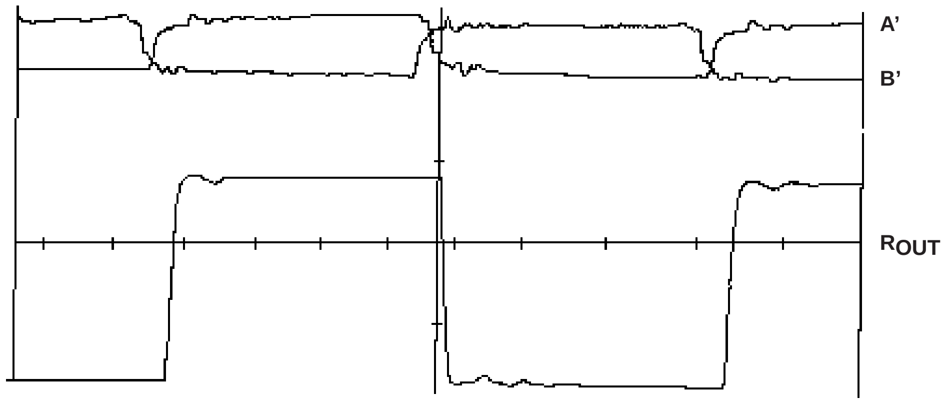

Figure 2. Reference Waveform of LVDS Receiver Input and Output Signals

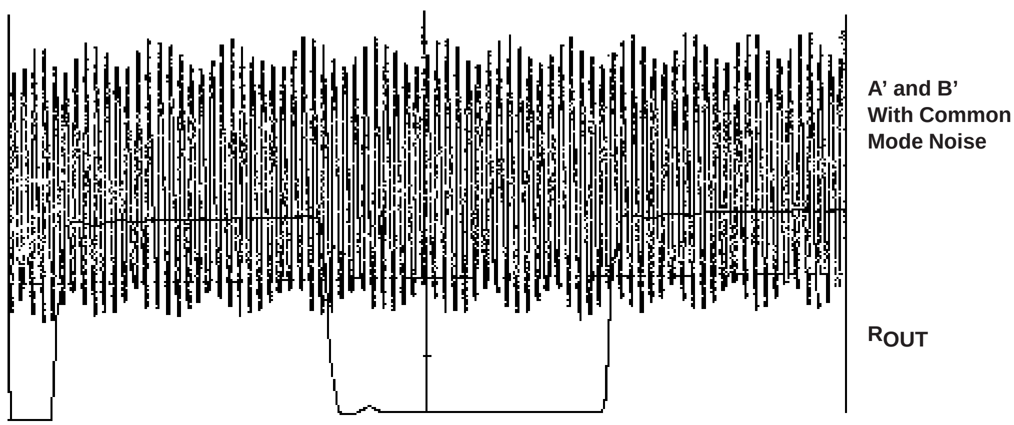

Figure 3. Common-Mode Noise and Receiver Output

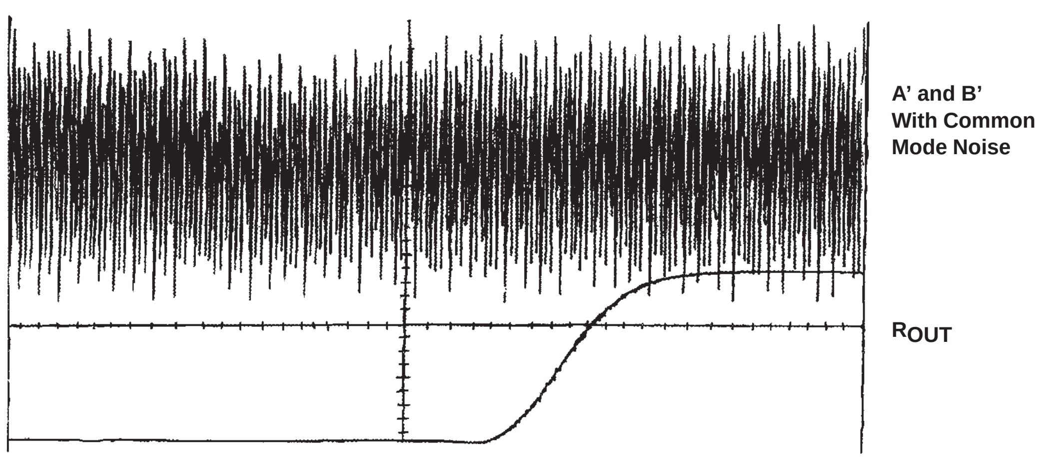

Figure 4. (Expanded) Common-Mode Noise and Receiver Output

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