

TC74AC74P/F/FN

DUAL D-TYPE FLIP FLOP PRESET AND CLEAR

The TC74AC74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

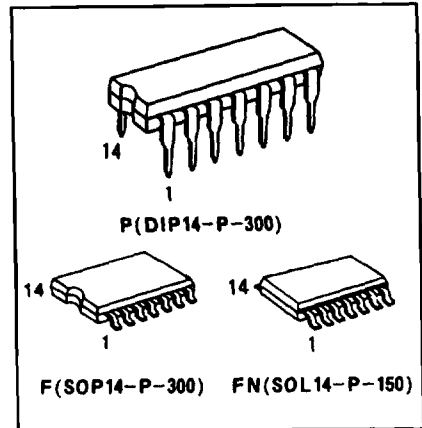
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{\text{CLR}}$ and $\overline{\text{PR}}$ are independent of the CK and are accomplished by setting the appropriate input low.

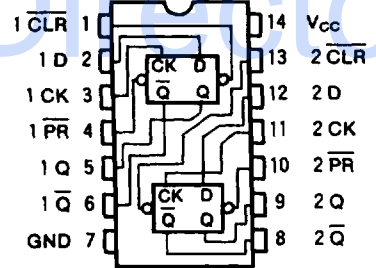
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed $f_{\text{max}}=200\text{MHz}(\text{typ.})$ at $V_{\text{CC}}=5\text{V}$
- Low Power Dissipation $I_{\text{CC}}=4\mu\text{A}(\text{Max.})$ at $T_a=25^\circ\text{C}$
- High Noise Immunity $V_{\text{NIH}}=V_{\text{NIL}}=28\% V_{\text{CC}}(\text{Min.})$
- Symmetrical Output Impedance $|I_{\text{OH}}|=I_{\text{OL}}=24\text{mA}(\text{Min.})$
Capability of driving 50 Ω transmission lines.
- Balanced Propagation Delays $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range $V_{\text{CC}}(\text{opr})=2\text{V}\sim 5.5\text{V}$
- Pin and Function Compatible with 74F 74



PIN ASSIGNMENT



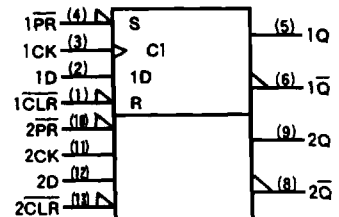
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	\uparrow	L	H	—
H	H	H	\uparrow	H	L	—
H	H	X	\downarrow	Q_n	$\overline{\text{Q}}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 6.0	V
DC Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC} /Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)* / 180(SOP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

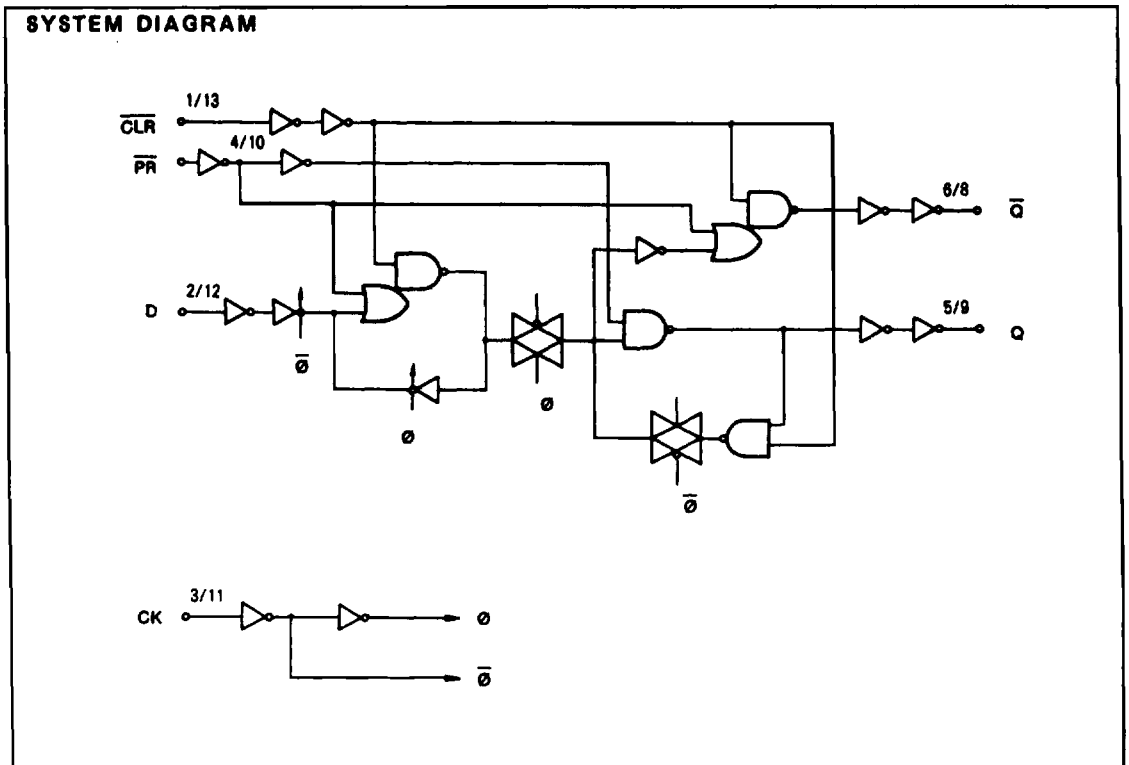
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	dt/dv	0 ~ 100 ($V_{CC} = 3.3 \pm 0.3\text{V}$)	ns/v
		0 ~ 20 ($V_{CC} = 5 \pm 0.5\text{V}$)	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V_{IH}		2.0	1.50	-	-	1.50	-	V	
			3.0	2.10	-	-	2.10	-		
			5.5	3.85	-	-	3.85	-		
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.50	-	0.50	V	
			3.0	-	-	0.90	-	0.90		
			5.5	-	-	1.65	-	1.65		
High-Level Output Voltage	V_{OH}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OH} = -50\mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V
				3.0	2.9	3.0	-	2.9	-	
		4.5	4.4	4.5	-	4.4	-			
		5.5	-	-	-	-	-			
Low-Level Output Voltage	V_{OL}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OL} = 50\mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V
				3.0	-	0.0	0.1	-	0.1	
		4.5	-	0.0	0.1	-	0.1			
		5.5	-	-	-	-	-			
				$I_{OL} = 12\text{mA}$	3.0	-	-	0.36	-	0.44
				$I_{OL} = 24\text{mA}$	4.5	-	-	0.36	-	0.44
				$I_{OL} = 75\text{mA}^*$	5.5	-	-	-	-	1.65
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	-	-	4.0	-	40.0		

* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

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TIMING REQUIREMENTS (Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	$T_a=25^\circ C$		$T_a=-40\sim 85^\circ C$	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$		3.3 ± 0.3	-	7.0	7.0	ns
	$t_{W(H)}$		5.0 ± 0.5	-	5.0	5.0	
Minimum Pulse Width (\overline{CLR} , \overline{PR})	$t_{W(L)}$		3.3 ± 0.3	-	7.0	7.0	
			5.0 ± 0.5	-	5.0	5.0	
Minimum Set-up Time	t_s		3.3 ± 0.3	-	6.0	6.0	
			5.0 ± 0.5	-	3.5	3.5	
Minimum Hold Time	t_h		3.3 ± 0.3	-	1.0	1.0	
			5.0 ± 0.5	-	1.0	1.0	
Minimum Removal Time (\overline{CLR} , \overline{PR})	t_{rem}		3.3 ± 0.3	-	4.0	4.0	
			5.0 ± 0.5	-	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=500Ω, Input t_r=t_f=3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC}	T _a =25°C			T _a =-40 ~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-Q, Q̄)	t _{pd1}		3.3±0.3	-	8.2	13.9	1.0	16.0	ns
	t _{pd2}		5.0±0.5	-	6.1	8.7	1.0	10.0	
Propagation Delay Time (CLR, PR-Q, Q̄)	t _{pd1}		3.3±0.3	-	8.0	13.1	1.0	15.0	ns
	t _{pd2}		5.0±0.5	-	5.7	8.2	1.0	9.4	
Maximum Clock Frequency	f _{MAX}		3.3±0.3	60	120	-	60	-	MHz
			5.0±0.5	100	160	-	100	-	
Input Capacitance	C _{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C _{PD(1)}			-	77	-	-	-	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opp)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2(\text{per F/F})$$