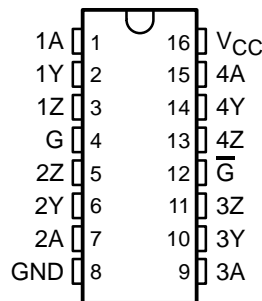


AM26LS31 QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS114F – JANUARY 1979 – REVISED OCTOBER 2001

- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B and ITU Recommendation V.11
- Operates From a Single 5-V Supply
- TTL Compatible
- Complementary Outputs
- High Output Impedance in Power-Off Conditions
- Complementary Output-Enable Inputs

D, DB, OR N PACKAGE
(TOP VIEW)



description

The AM26LS31 is a quadruple complementary-output line driver designed to meet the requirements of ANSI TIA/EIA-422-B and ITU (formerly CCITT) Recommendation V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable (G, \bar{G}) input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

The AM26LS31 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		
	PLASTIC SMALL OUTLINE (D)	PLASTIC SHRINK SMALL OUTLINE (DB)	PLASTIC DIP (N)
0°C to 70°C	AM26LS31CD	AM26LS31CDB	AM26LS31CN

The DB package is only available taped and reeled. Add the suffix R to the device type (e.g., AM26LS31CDBR).

FUNCTION TABLE (each driver)

INPUT A	ENABLES		OUTPUTS	
	G	\bar{G}	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

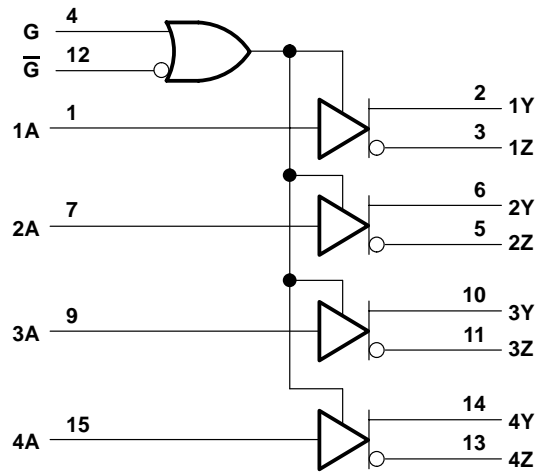
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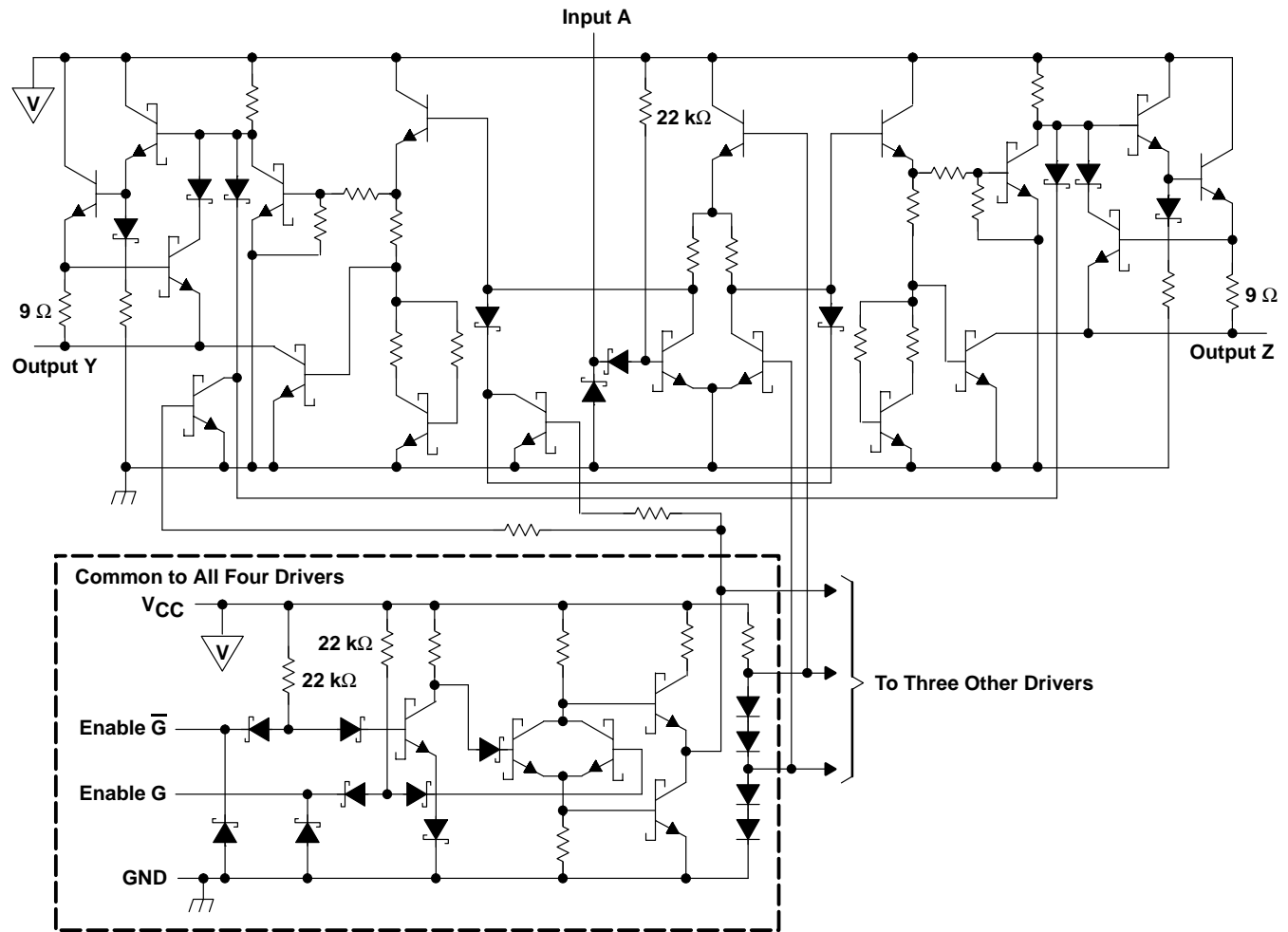
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logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Output off-state voltage	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
DB package	82°C/W
N package	67°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential output voltage V_{OD} , are with respect to network GND.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			–20	mA
I_{OL} Low-level output current			20	mA
T_A Operating free-air temperature	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK} Input clamp voltage	$V_{CC} = 4.75$ V, $I_I = -18$ mA			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = 4.75$ V, $I_{OH} = -20$ mA	2.5			V
V_{OL} Low-level output voltage	$V_{CC} = 4.75$ V, $I_{OL} = 20$ mA			0.5	V
I_{OZ} Off-state (high-impedance-state) output current	$V_{CC} = 4.75$ V			–20	μ A
				20	
I_I Input current at maximum input voltage	$V_{CC} = 5.25$ V, $V_I = 7$ V			0.1	mA
I_{IH} High-level input current	$V_{CC} = 5.25$ V, $V_I = 2.7$ V			20	μ A
I_{IL} Low-level input current	$V_{CC} = 5.25$ V, $V_I = 0.4$ V			–0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = 5.25$ V	–30		–150	mA
I_{CC} Supply current	$V_{CC} = 5.25$ V, All outputs disabled		32	80	mA

‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.



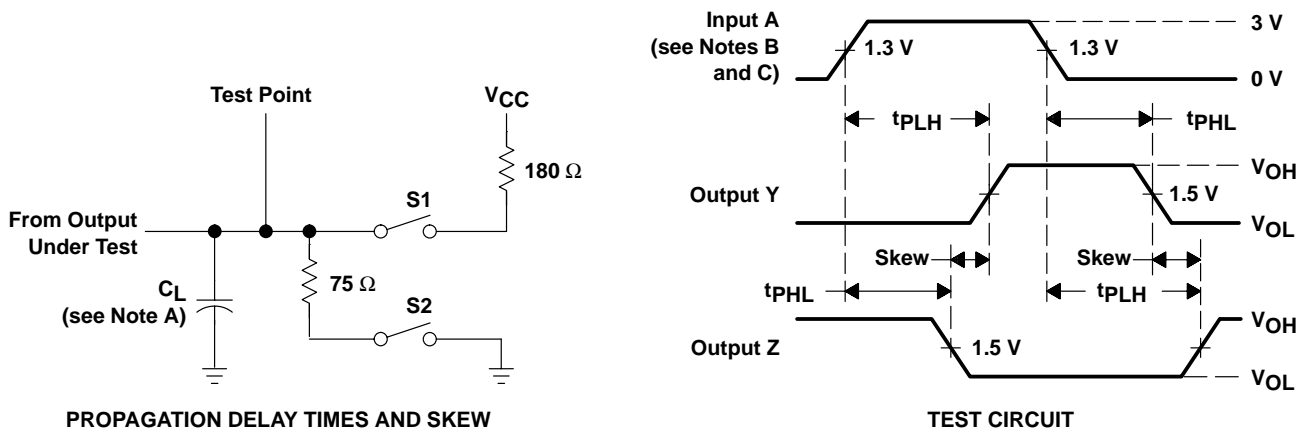
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

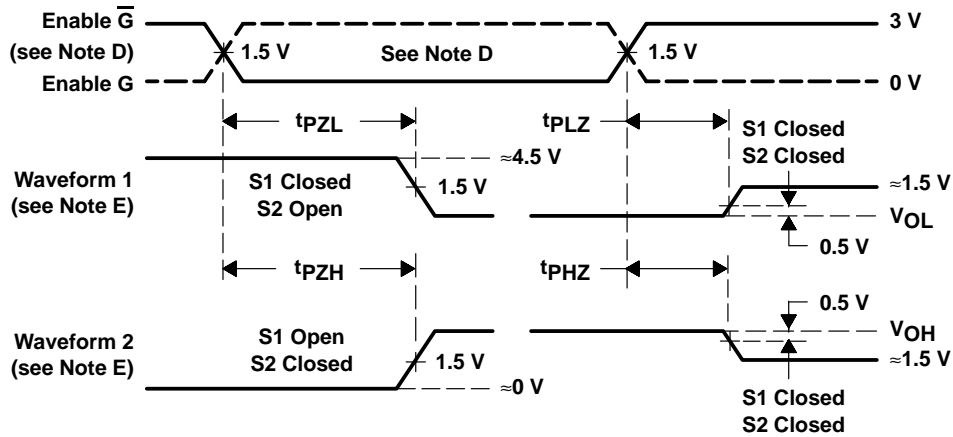
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 30\text{ pF}$, S1 and S2 open		14	20	ns
t_{PHL} Propagation delay time, high-to-low-level output			14	20	
t_{PZH} Output enable time to high level	$C_L = 30\text{ pF}$	$R_L = 75\ \Omega$		25	ns
t_{PZL} Output enable time to low level			$R_L = 180\ \Omega$	37	
t_{PHZ} Output disable time from high level	$C_L = 10\text{ pF}$, S1 and S2 closed		21	30	ns
t_{PLZ} Output disable time from low level			23	35	
Output-to-output skew	$C_L = 30\text{ pF}$, S1 and S2 open		1	6	ns

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES AND SKEW

TEST CIRCUIT



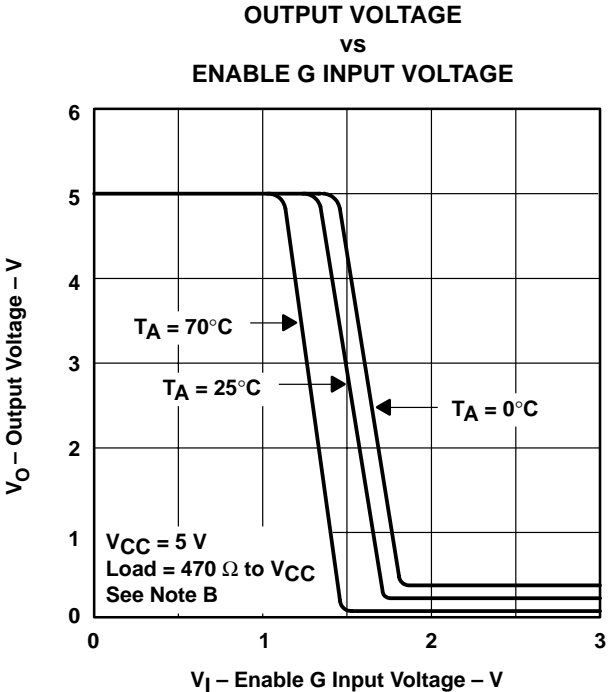
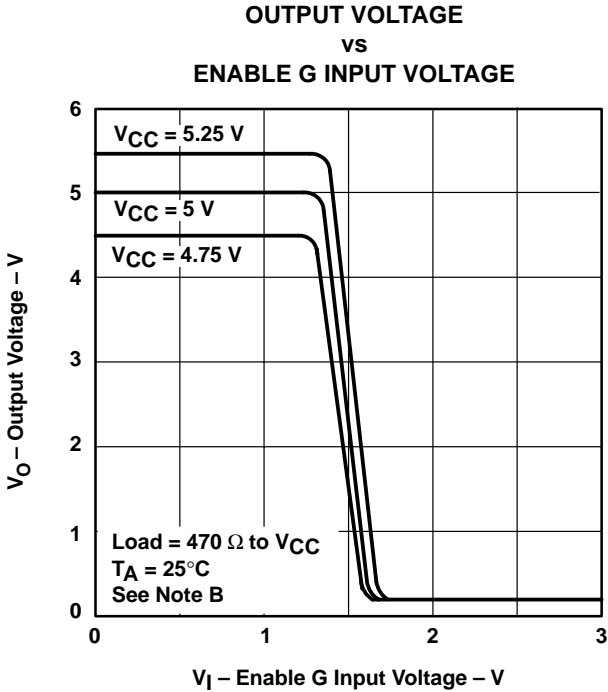
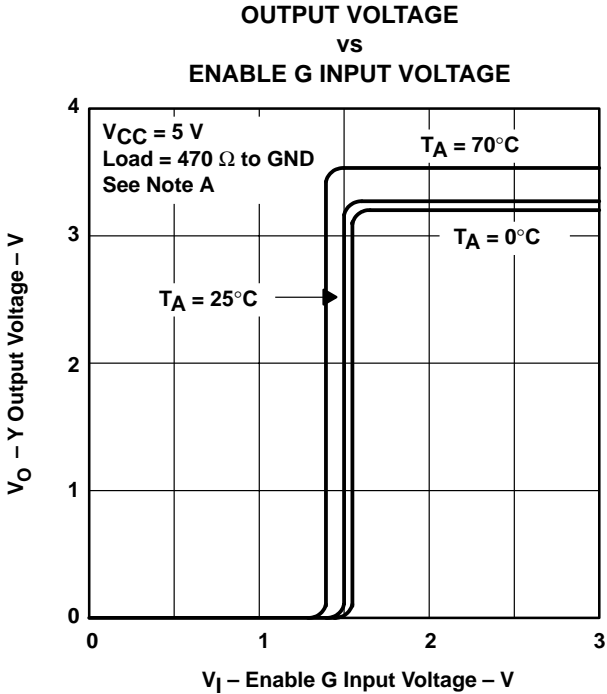
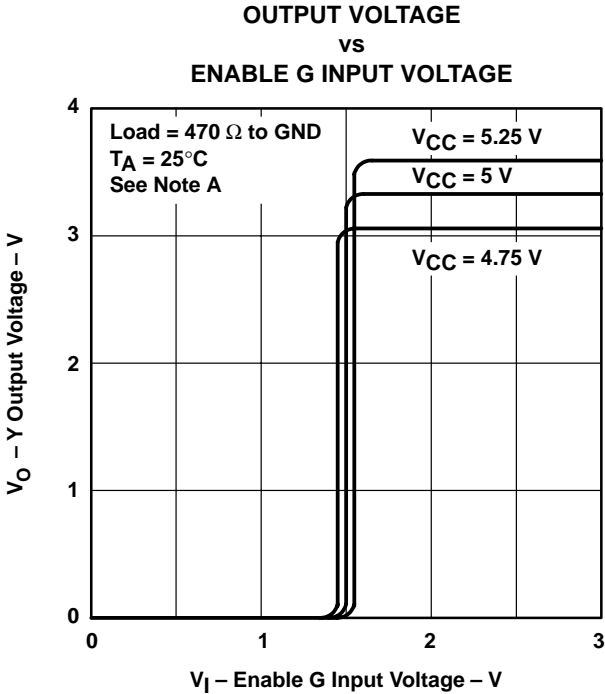
ENABLE AND DISABLE TIME WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O \approx 50\ \Omega$, $t_r \leq 15\text{ ns}$, $t_f \leq 6\text{ ns}$.
 C. When measuring propagation delay times and skew, switches S1 and S2 are open.
 D. Each enable is tested separately.
 E. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Test Circuit and Voltage Waveforms



TYPICAL CHARACTERISTICS



NOTES: A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.
 B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z outputs.



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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

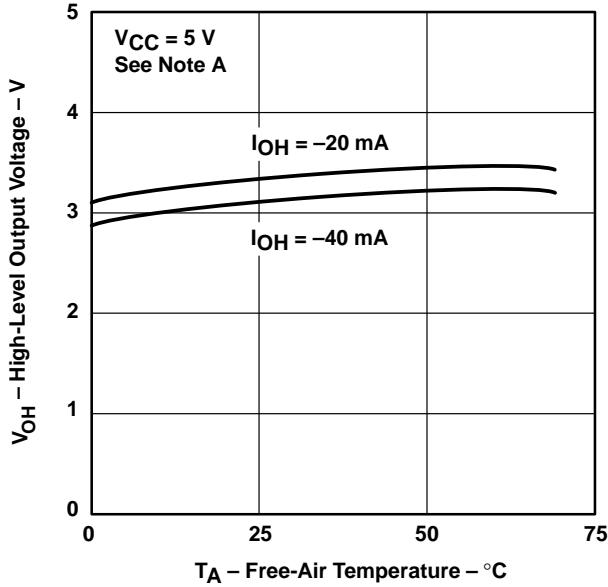


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

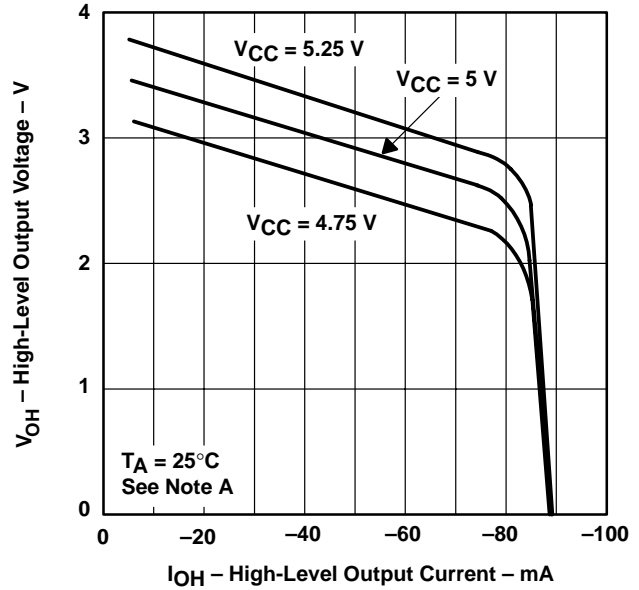


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

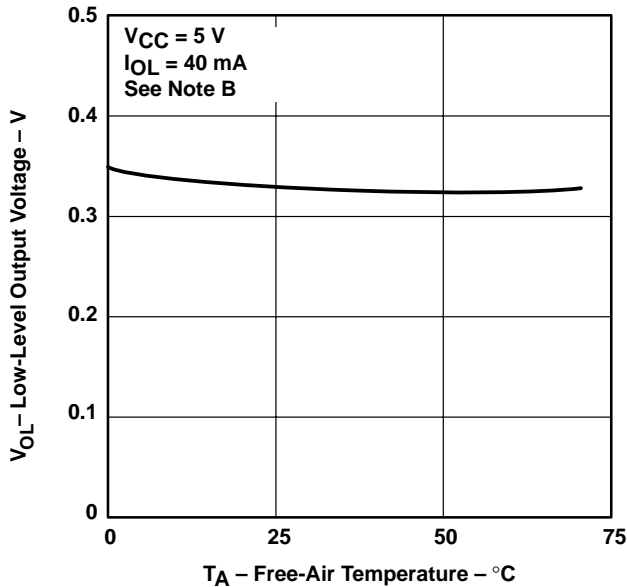


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

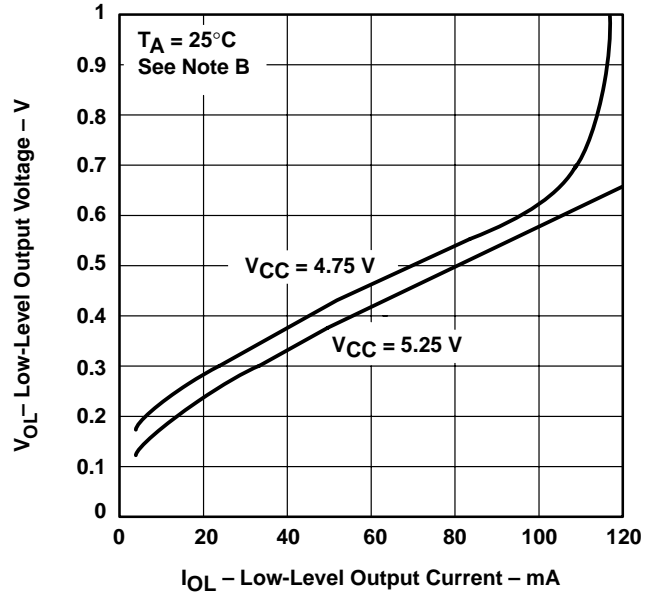


Figure 9

NOTES: A. The A input is connected to V_{CC} during testing of the Y outputs and to ground during testing of the Z outputs.
B. The A input is connected to ground during testing of the Y outputs and to V_{CC} during testing of the Z inputs.

TYPICAL CHARACTERISTICS

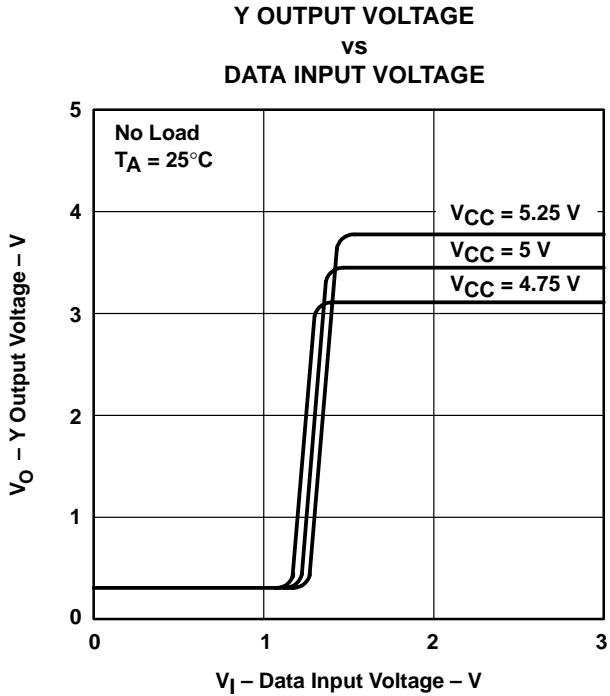


Figure 10

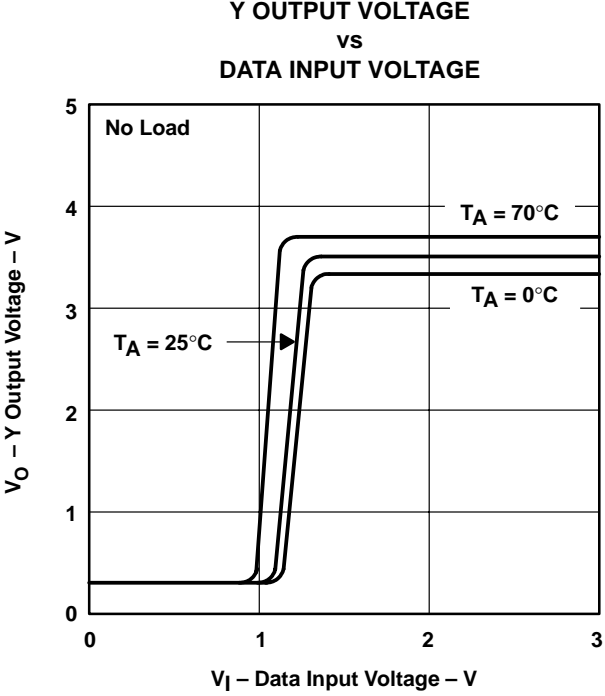


Figure 11

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