XC4000EX Electrical Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

All specifications subject to change without notice.

XC4000EX DC Characteristics

Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1 V to 4 V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction Temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC excursion above V_{cc} or below Ground must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. Maximum total combined current on all dedicated inputs and Tri-state outputs must not exceed 200 mA. During transitions, the device pins may undershoot to -2.0 V or overshoot toV_{CC} +2.0 V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage (Note1)	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage (Note1)	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Note 1: Maximum DC excursion above V_{cc} or below Ground must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. Maximum total combined current on all dedicated inputs and Tri-state outputs must not exceed 200 mA. During transitions, the device pins may undershoot to -2.0 V or overshoot toV_{CC} +2.0 V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Notes: At junction temperatures above those listed , all delay parameters increase by 0.35% per °C.
Input and output measurement thresholds for TTL are 1.5 V and for CMOS are 2.5 V.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0 mA	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		3.0		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			25	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 5.5 V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND.

XC4000EX Switching Characteristics

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Global Buffer Switching Characteristic Guidelines

		Speed Grade	-4	-3	-2	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
From pad through Global Low Skew buffer, to any clock K	T_{GLS}	XC4028EX XC4036EX	9.2 9.8	7.5 7.9	6.4 7.1	ns ns
From pad through Global Early buffer, to any clock K in same quadrant	T_{GE}	XC4028EX XC4036EX	5.7 5.9	4.4 4.6	4.2 4.4	ns ns

Horizontal Longline Switching Characteristic Guidelines

		Speed Grade	-4	-3	-2	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
TBUF driving a Horizontal Longline						
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T_{IO1}	XC4028EX XC4036EX	13.7 16.5	11.3 13.6	10.9 13.2	ns ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T_{ON}	XC4028EX XC4036EX	14.7 17.4	12.1 14.4	11.7 14.0	ns ns
TBUF driving Half a Horizontal Longline						
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T_{HIO1}	XC4028EX XC4036EX	6.3 7.3	5.6 6.0	4.6 5.7	ns ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T_{HON}	XC4028EX XC4036EX	7.2 8.2	6.4 6.8	5.4 6.5	ns ns

Note: These values include a minimum load of one output, spaced as far as possible from the activated pullup(s). Use the static timing analyzer to determine the delay for each destination.

XC4000EX CLB Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devicees unless otherwise noted.

CLB Switching Characteristic Guidelines

Description	Speed Grade / Symbol	-4 Min	-4 Max	-3 Min	-3 Max	-2 Min	-2 Max	Units
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		2.2		1.8		1.5	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		3.8		3.2		2.7	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		3.2		2.7		2.5	ns
C inputs via SR/H0 via H' to X/Y outputs	T_{HH0O}		3.6		3.0		2.5	ns
C inputs via H1 via H' to X/Y outputs	T_{HH1O}		3.0		2.5		2.3	ns
C inputs via DIN/H2 via H' to X/Y outputs	T_{HH2O}		3.6		3.0		2.5	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CBYP}		2.0		1.6		1.4	ns
CLB Fast Carry Logic								
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		2.5		2.2		1.9	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		4.1		3.6		3.1	ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.9		1.6		1.4	ns
CIN through function generators to X/Y outputs	T_{SUM}		3.0		2.6		2.2	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.60		0.50		0.40	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.18		0.15		0.15	ns
Sequential Delays								
Clock K to Flip-Flop outputs Q	T_{CKO}		2.2		1.9		1.7	ns
Clock K to Latch outputs Q	T_{CKLO}		2.2		1.9		1.7	ns
Setup Time before Clock K								
F/G inputs	T_{ICK}	1.3		1.1		1.1		ns
F/G inputs via H'	T_{IHCK}	3.0		2.5		2.2		ns
C inputs via H0 through H'	T_{HH0CK}	2.8		2.3		2.0		ns
C inputs via H1 through H'	T_{HH1CK}	2.2		1.8		1.8		ns
C inputs via H2 through H'	T_{HH2CK}	2.8		2.3		2.0		ns
C inputs via DIN	T_{DICK}	1.2		0.9		0.9		ns
C inputs via EC	T_{ECCK}	1.2		1.0		0.9		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.8		0.7		0.6		ns
CIN input via F'/G'	T_{CCK}	2.2		1.8		2.1		ns
CIN input via F'/G' and H'	T_{CHCK}	3.9		3.2		3.2		ns
Hold Time after Clock K								
F/G inputs	T_{CKI}	0		0		0		ns
F/G inputs via H'	T_{CKIH}	0		0		0		ns
C inputs via SR/H0 through H'	T_{CKHH0}	0		0		0		ns
C inputs via H1 through H'	T_{CKHH1}	0		0		0		ns
C inputs via DIN/H2 through H'	T_{CKHH2}	0		0		0		ns
C inputs via DIN/H2	T_{CKDI}	0		0		0		ns
C inputs via EC	T_{CKEC}	0		0		0		ns
C inputs via SR, going Low (inactive)	T_{CKR}	0		0		0		ns
Clock								
Clock High time	T_{CH}	3.5		3.0		3.0		ns
Clock Low time	T_{CL}	3.5		3.0		3.0		ns
Set/Reset Direct								
Width (High)	T_{RPW}	3.5		3.0		3.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		4.5		3.8		3.6	ns
Global Set/Reset								
Minimum GSR Pulse Width	T_{MRW}		13.0		11.5		11.5	ns
Delay from GSR input to any Q (XC4028EX)	T_{MRQ}		22.8		19.0		19.0	ns
Delay from GSR input to any Q (XC4036EX)	T_{MRQ}		24.0		21.0		21.0	ns
Toggle Frequency) (for export control purposes)	F_{TOG}		143		166		166	MHz

CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

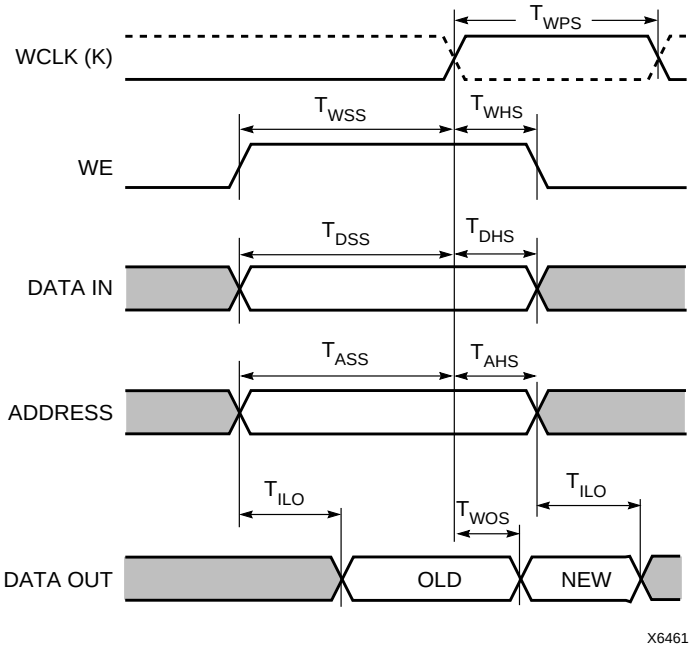
Single Port RAM	Speed Grade		-4		-3		-2		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	11.0 11.0		9.0 9.0		9.0 9.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	5.5 5.5		4.5 4.5		4.5 4.5		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	2.7 2.6		2.3 2.2		2.2 2.2		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0 0		0 0		0 0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	2.4 2.9		2.0 2.5		2.0 2.5		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0 0		0 0		0 0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	2.3 2.1		2.0 1.8		2.0 1.8		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0 0		0 0		0 0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		8.2 10.1		6.8 8.4		6.8 8.2	ns ns

Notes:: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Applicable Read timing specifications are identical to Level-Sensitive Read timing.

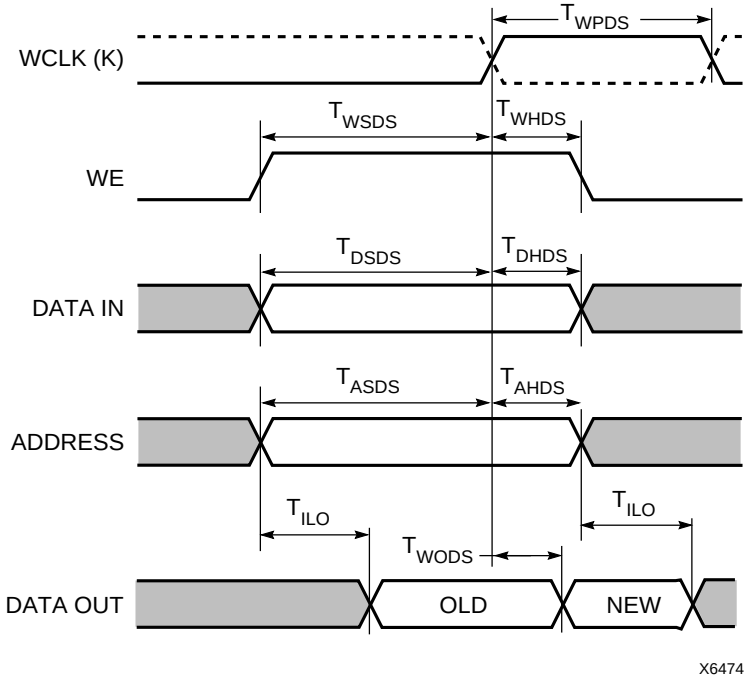
Dual-Port RAM	Speed Grade		-4		-3		-2		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x1	T_{WCDS}	11.0		9.0		9.0		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	5.5		4.5		4.5		ns
Address setup time before clock K	16x1	T_{ASDS}	3.1		2.6		2.5		ns
Address hold time after clock K	16x1	T_{AHDS}	0		0		0		ns
DIN setup time before clock K	16x1	T_{DSDS}	2.9		2.5		2.5		ns
DIN hold time after clock K	16x1	T_{DHDS}	0		0		0		ns
WE setup time before clock K	16x1	T_{WSDS}	2.1		1.8		1.8		ns
WE hold time after clock K	16x1	T_{WHDS}	0		0		0		ns
Data valid after clock K	16x1	T_{WODS}		9.4		7.8		7.8	ns

Note:: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

CLB Single-Port RAM Synchronous (Edge-Triggered) Write Timing Waveforms



CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing Waveforms



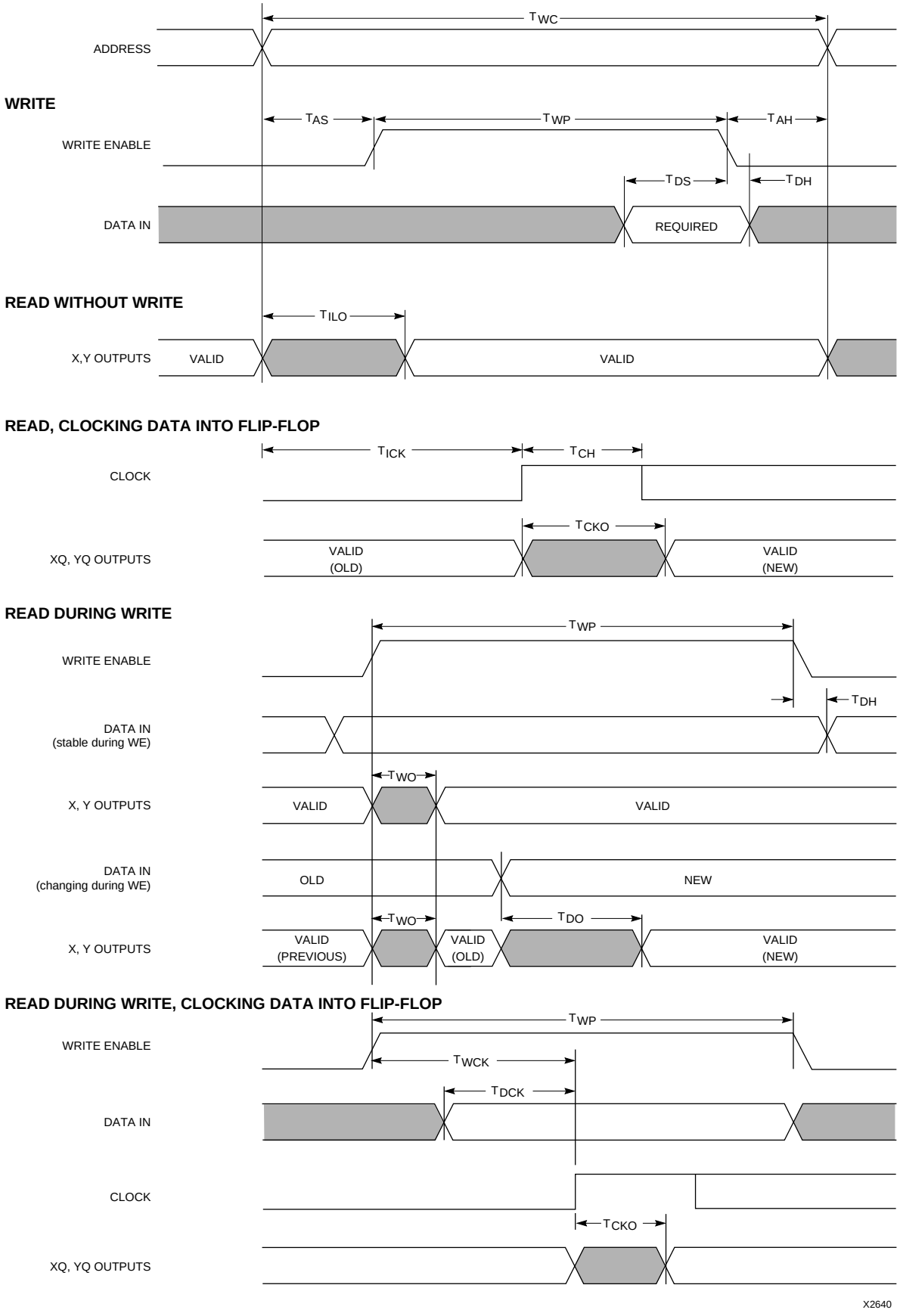
CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

	Speed Grades		-4		-3		-2		Units
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Operation									
Address write cycle time	16x2 32x1	T_{WC} T_{WCT}	10.6 10.6		9.2 9.2		8.0 8.0		ns ns
Write Enable pulse width (High)	16x2 32x1	T_{WP} T_{WPT}	5.3 5.3		4.6 4.6		4.0 4.0		ns ns
Address setup time before WE	16x2 32x1	T_{AS} T_{AST}	2.8 2.9		2.4 2.5		2.0 2.0		ns ns
Address hold time after end of WE	16x2 32x1	T_{AH} T_{AHT}	1.7 1.7		1.4 1.4		1.4 1.4		ns ns
DIN setup time before end of WE	16x2 32x1	T_{DS} T_{DST}	1.1 1.1		0.9 0.9		0.8 0.8		ns ns
DIN hold time after end of WE	16x2 32x1	T_{DH} T_{DHT}	6.6 6.6		5.7 5.7		5.0 5.0		ns ns
Read Operation									
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	4.5 6.5		3.1 5.5		3.1 5.5		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		2.2 3.8		1.8 3.2		1.5 2.7	ns ns
Read Operation, Clocking Data into Flip-Flop									
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	1.5 3.2		1.2 2.6		1.2 2.6		ns ns
Read During Write									
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	T_{WO} T_{WOT}		6.5 7.4		5.7 6.5		4.9 5.6	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	T_{DO} T_{DOT}		7.7 8.2		6.7 7.2		5.8 6.2	ns ns
Read During Write, Clocking Data into Flip-Flop									
WE setup time before clock K	16x2 32x1	T_{WCK} T_{WCKT}	7.1 9.2		6.2 8.1		5.5 7.0		ns ns
Data setup time before clock K	16x2 32x1	T_{DCK} T_{DCKT}	5.9 8.4		5.2 7.4		4.6 6.4		ns ns

Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

CLB RAM Asynchronous (Level-Sensitive) Timing Waveforms



XC4000EX Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000EX devices unless otherwise noted.

Output Flip-Flop, Clock to Out Guidelines

		Speed Grade	-4	-3	-2	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
Global Low Skew Clock to TTL Output (fast) using OFF	T_{ICKOF}	XC4028EX XC4036EX	16.6 17.2	13.7 14.1	12.4 13.1	ns ns
Global Early Clock to TTL Output (fast) using OFF	T_{ICKEOF}	XC4028EX XC4036EX	13.1 13.3	10.6 10.8	10.2 10.4	ns ns

OFF = Output Flip Flop

Output MUX, Clock to Out Guidelines

		Speed Grade	-4	-3	-2	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
Global Low Skew Clock to TTL Output (fast) using OMUX	T_{PFPF}	XC4028EX XC4036EX	15.9 16.5	13.1 13.5	11.8 12.5	ns ns
Global Early Clock to TTL Output (fast) using OMUX	T_{PEFPF}	XC4028EX XC4036EX	12.4 12.6	10.0 10.2	9.6 9.8	ns ns

OMUX = Output MUX

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at TTL threshold with 50 pF external capacitive load.
Set-up time is measured with the fastest route and the lightest load. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

Output Level and Slew Rate Adjustments

The following table must be used to adjust output parameters and output switching characteristics.

	Speed Grade		-4	-3	-2	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
For TTL output FAST add	T_{TTLOF}	All Devices	0	0	0	ns
For TTL output SLOW add	T_{TTLO}	All Devices	2.9	2.4	2.4	ns
For CMOS FAST output add	T_{CMOSOF}	All Devices	1.0	0.8	0.8	ns
For CMOS SLOW output add	T_{CMOSO}	All Devices	3.6	3.0	3.0	ns

XC4000EX Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000EX devices unless otherwise noted

Global Low Skew Clock, Set-Up and Hold Guidelines

		Speed Grade	-4	-3	-2	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup Time, using Global Low Skew clock and IFF (full delay)	T_{PSD}	XC4028EX	8.0	6.8	6.8	ns
		XC4036EX	8.0	6.8	6.8	ns
Input Hold Time, using Global Low Skew clock and IFF (full delay)	T_{PHD}	XC4028EX	0	0	0	ns
		XC4036EX	0	0	0	ns

IFF = Input Flip-Flop or Latch

Global Early Clock, Set-Up and Hold for IF Guidelines

		Speed Grade	-4	-3	-2	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup Time, using Global Early clock and IFF (partial delay)	T_{PSEP}	XC4028EX	6.5	5.4	5.4	ns
		XC4036EX	6.5	5.4	5.4	ns
Input Hold Time, using Global Early clock and IFF (partial delay)	T_{PHEP}	XC4028EX	0	0	0	ns
		XC4036EX	0	0	0	ns

IFF = Input Flip-Flop or Latch

Note: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

Global Early Clock, Set-Up and Hold for FCL Guidelines

		Speed Grade	-4	-3	-2	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup Time, using Global Early clock and FCL (partial delay)	T_{PFSEP}	XC4028EX	3.4	3.4	3.4	ns
		XC4036EX	4.4	4.2	4.2	ns
Input Hold Time, using Global Early clock and FCL (partial delay)	T_{PFHEP}	XC4028EX	0	0	0	ns
		XC4036EX	0	0	0	ns

FCL = Fast Capture Latch

Notes: For CMOS input levels, see the "Input Threshold Adjustments" on page 96.

Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions.

Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6.

Input Threshold Adjustments

The following table must be used to adjust input parameters and input switching characteristics.

	Speed Grade		-4	-3	-2	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
For TTL input add	T_{TTLI}	All Devices	0	0	0	ns
For CMOS input add	T_{CMOSI}	All Devices	0.3	0.2	0.2	ns

XC4000EX IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

		Speed Grade	-4	-3	-2	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Clocks						
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All devices	3.2	2.6	2.6	ns
Propagation Delays			**Max**	**Max**	**Max**	
Pad to I1, I2	T_{PID}	All devices	2.2	1.9	1.8	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices	3.8	3.2	3.0	ns
Pad to I1, I2 via transparent input latch, partial delay	T_{PPLI}	XC4028EX XC4036EX	13.3 14.5	11.1 12.1	10.9 11.9	ns ns
Pad to I1, I2 via transparent input latch, full delay	T_{PDLI}	XC4028EX XC4036EX	18.2 19.4	15.2 16.2	14.9 15.9	ns ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All devices	5.3	4.4	4.2	ns
Pad to I1, I2 via transparent FCL and input latch, partial delay	T_{PPFLI}	XC4028EX XC4036EX	13.6 14.8	11.3 12.3	11.1 12.1	ns ns
Propagation Delays						
Clock (IK) to I1, I2 (flip-flop) Clock (IK) to I1, I2 (latch enable, active Low) FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{IKRI} T_{IKLI} T_{OKLI}	All devices All devices All devices	3.0 3.2 6.2	2.5 2.7 5.2	2.4 2.6 5.0	ns ns ns
Global Set/Reset						
Minimum GSR Pulse Width Delay from GSR input to any Q Delay from GSR input to any Q	T_{MRW} T_{RRI} T_{RRI}	All devices XC4028EXX C4036EX	13.0 22.8 24.0	11.5 19.0 21.0	11.5 19.0 21.0	ns ns ns

FCL = Fast Captur Latch, IFF = Input Flip-Flop or Latch

Notes: For CMOS input levels, see the "Input Threshold Adjustments" on page 96.

For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 96.

XC4000EX IOB Input Switching Characteristic Guidelines (Continued)

Description	Symbol	Speed Grade / Device	-4 Min	-3 Min	-2 Min	Units
Setup Times						
Pad to Clock (IK), no delay	T_{PICK}	All devices	2.5	2.0	2.0	ns
Pad to Clock (IK), partial delay	T_{PICKP}	XC4028EX	10.8	9.0	9.0	ns
		XC4036EX	12.0	10.0	10.0	ns
Pad to Clock (IK), full delay	T_{PICKD}	XC4028EX	15.7	13.1	13.1	ns
		XC4036EX	16.9	14.1	14.1	ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	All devices	3.9	3.3	3.3	ns
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	T_{PICKFP}	XC4028EX	12.3	10.2	10.2	ns
		XC4036EX	13.5	11.2	11.2	ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All devices	0.8	0.7	0.7	ns
Pad to Fast Capture Latch Enable (OK), partial delay	T_{POCKP}	XC4028EX	9.1	7.6	7.6	ns
		XC4036EX	10.3	8.6	8.6	ns
Setup Times (TTL or CMOS Inputs)						
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All devices	0.3	0.2	0.2	ns
Hold Times						
Pad to Clock (IK),						
no delay	T_{IKPI}	All devices	0	0	0	ns
partial delay	T_{IKPIP}	All devices	0	0	0	ns
full delay	T_{IKPID}	All devices	0	0	0	ns
Pad to Clock (IK) via transparent Fast Capture Latch,						
no delay	T_{IKFPI}	All devices	0	0	0	ns
partial delay	T_{IKFPIP}	All devices	0	0	0	ns
full delay	T_{IKFPID}	All devices	0	0	0	ns
Clock Enable (EC) to Clock (IK),						
no delay	T_{IKEC}	All devices	0	0	0	ns
partial delay	T_{IKECP}	All devices	0	0	0	ns
full delay	T_{IKECD}	All devices	0	0	0	ns
Pad to Fast Capture Latch Enable (OK),						
no delay	T_{OKPI}	All devices	0	0	0	ns
partial delay	T_{OKPIP}	All devices	0	0	0	ns

Notes: For CMOS input levels, see the "Input Threshold Adjustments" on page 96.
For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 96.

XC4000EX IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000EX devices unless otherwise noted.

	Speed Grade	-4		-3		-2		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays								
Clock (OK) to Pad	T_{OKPOF}		7.4		6.2		6.0	ns
Output (O) to Pad	T_{OPF}		6.2		5.2		5.0	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		4.9		4.1		4.1	ns
3-state to Pad active and valid	T_{TSONF}		6.2		5.2		5.0	ns
Output MUX Select (OK) to Pad	T_{OKFPF}		6.7		5.6		5.4	ns
Fast Path Output MUX Input (EC) to Pad	T_{CEFPF}		6.2		5.1		5.0	ns
Slowest Path Output MUX Input (O) to Pad	T_{OFPF}		7.3		6.0		5.9	ns
Setup and Hold Times								
Output (O) to clock (OK) setup time	T_{OOK}	0.6		0.5		0.5		ns
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0		ns
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	0		0		0		ns
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	0		0		0		ns
Clock								
Clock High	T_{CH}	3.5		3.0		3.0		ns
Clock Low	T_{CL}	3.5		3.0		3.0		ns
Global Set/Reset								
Minimum GSR pulse width	T_{MRW}	13.0		11.5		11.5		ns
Delay from GSR input to any Pad (XC4028EX)	T_{RPO}	**30.2**		**25.2**		**25.0**		ns
Delay from GSR input to any Pad (XC4036EX)	T_{RPO}	**31.4**		**27.2**		**27.0**		ns

Notes: Output timing is measured at TTL threshold, with 35pF external capacitive loads.
For CMOS output levels, see the "Output Level and Slew Rate Adjustments" on page 95

Revision Control

Version	Description
2/1/99 (1.5)	Release included in 1999 data book, section 6
5/14/99 (1.6)	Replaced Electrical Specification pages for XLA and XV families with separate updates and added URL link on placeholder page for electrical specifications/pinouts for WebLINX users.